WIRELESS TRANSCEIVER MODULE SPEC

Client：

Product name：2.4G Transceiver module

Part number：JRF 201103-1_V1.1

Edition：V1.1

Page numbering：1/42

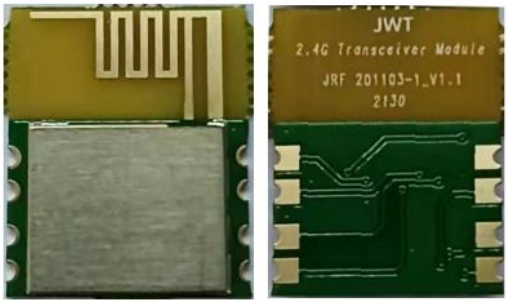
Date：2020/1/06

Manufacture：Jiangsu Jingweite

Approval ：	Audit：	Producer：
Customer back sign：	Approval：	Audit：

Catalog

One. Product picture



Picture 1-1

Illustrate:

Row 1: JWT LOGO

Row 2: Product name

Row 3: Product model

Row 4: Date Year Week

Two. Summarize

JRF JRF201103-1_V1.1 module use JD0069C* chip, JD0069C chip is a single integrated wireless transceiver chip that works in the 2.4GHz world general ISM spectrum. The chip incorporates an rf receiver、RF Transmitter、frequency synthesize、GFSK modulator、GFSK demodulator and other functional modules。Through the SPI interface the output power, channel selection and protocol can be flexibly configured. And built-in CRC、FEC，automatic answer and automatic retransmission mechanism，It can greatly simplify system design and optimize performance.

This module is designed with a complete circuit, and few peripheral devices need to be connected，In the simplest case，The user only needs to connect the power, ground, RST，MOSI, MISO, CS and CLK and IRQ. Then they are ready for use, and are designed with stamp holes. With

the advantages of small volume, low power consumption and high sensitivity of transceiver, it is suitable for batch patch production.

* * The JD0069C chip silk screen is RC2516S, hereby explain.

limit value

parameter	symbol	Minimum value	Maximum value	Unit
operating temperature	Top	-10	50	℃
Storage Temperature	Tstor	-20	70	℃
working voltage	VDD	1.9	3.6	V
Input rf signal strength	Pin_max		+10	dBm
ESD(Mannequin)	ESD_HBM		2	KV

Table 2-1

* Attention：Forcing more than one or more extreme values can lead to permanent damage to the device。

* Be careful： The chip is an electrostatic sensitive device. Please observe the protective rules when operating。

Major electrical parameters

Characteristics	Condition(unless otherwise specified，VCC= 3.3V ，TA=25℃)	parameter values			Unit
		Minimum	Typical	Maximum	
ICC	Sleep Mode		0.8		uA
	standby mode		600		uA
	Transmit mode (7dBm)		32		mA
	receive mode		16		mA
System indicators					
f_{OP}	Operating frequency	2402		2480	MHz
f_{XTAL}	Crystal frequency		12		MHz

PLL_stable	PLL Settling time		150		us
	code rate		1		Mbps
FCH 1M	Channel spacing		1		MHz
Emission pattern index					
PRF	maximum power output		8		dBm
PRF	Typical output		0		dBm
PRFC	Output Power Range	-24		8	dBm
PBW1	Carrier modulated 20dB Mbps（1Mbps）		1	1.1	MHz
Receiving mode index					
RXSENS2	receiving sensitivity （0.1%BER）		-89		dBm
Immunity characteristics					
C / I *CO*	Co-channel Interference		9		dBc
C / I1ST	Phase 1 lead interference		5		dBc
C /I2ND	Phase 2 lead interference		-12		dBc
C / I 3RD	Phase 3 lead interference		-24		dBc
operating conditions					
VDD	Power Supply	1.9	3	3.6	V
VSS	processing chip.		0		V
VOH	high -level output voltage	VDD-0.3		VDD	V
VOL	Low Level Output Voltage	VSS		VSS+0.3	V
VIH	high-level input voltage	2.0	3	3.6	V
VIL	Low Level Input Voltage	VSS		VSS+0.3	V
Cin	input capacitance			10	pF
	Working Temperature	-10	27	+50	℃
	Storage Temperature	-20	27	+70	℃

Table 2-2

Notes: 12MHz The load capacitance of the crystal oscillator is 8.2pF

Three.Product characteristics

low power consumption

When work is in launch mode（Transmitted power 0.066dBm）Current consumption 32mA；

The current consumption is 16mA when the work is in receiving mode；

Current consumption is lower than 1uA when working in hibernation mode。

low-cost

Low-cost system solutions；

The peripheral components are less than 5；

Internal integrated power reset and software reset function， Peripheral control is simple；

Double layer PCB can be used for plate antenna；

high performance

Operating frequency 2402-2480MHz；

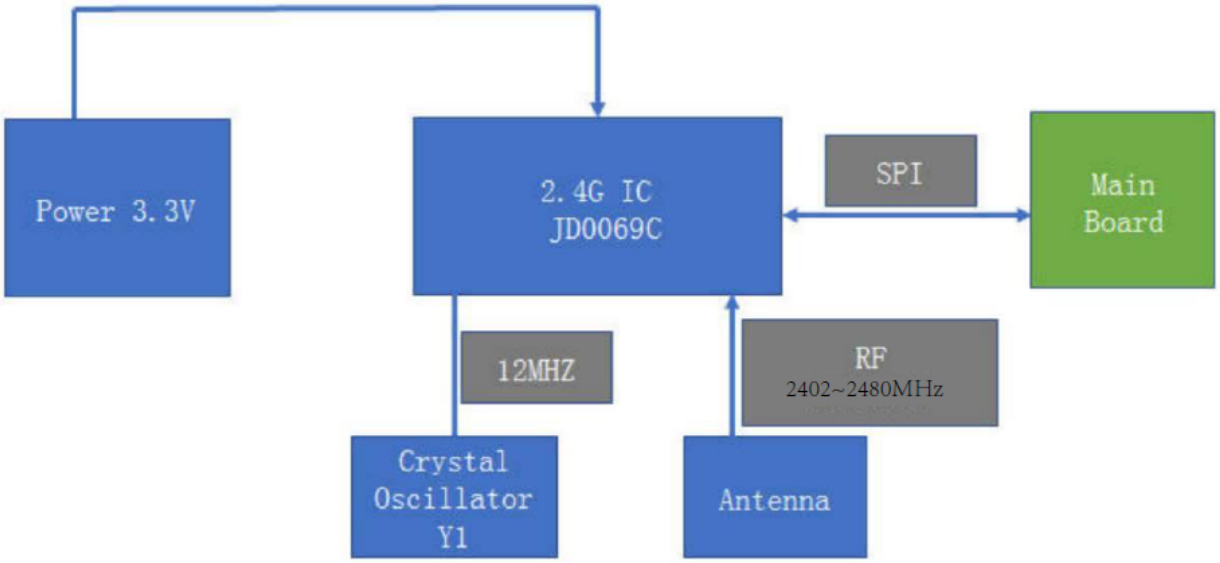
Maximum data rate 1Mbps；

Four.Application fields

Industrial sensors and wireless & Industrial control equipment Smart TV remote control

Wireless game equipment	Wireless label
Telemetry	Wireless access
Security System	Intelligent sports equipment
Remote Control	Wireless toys

2.4G Receiver Module Block Diagram



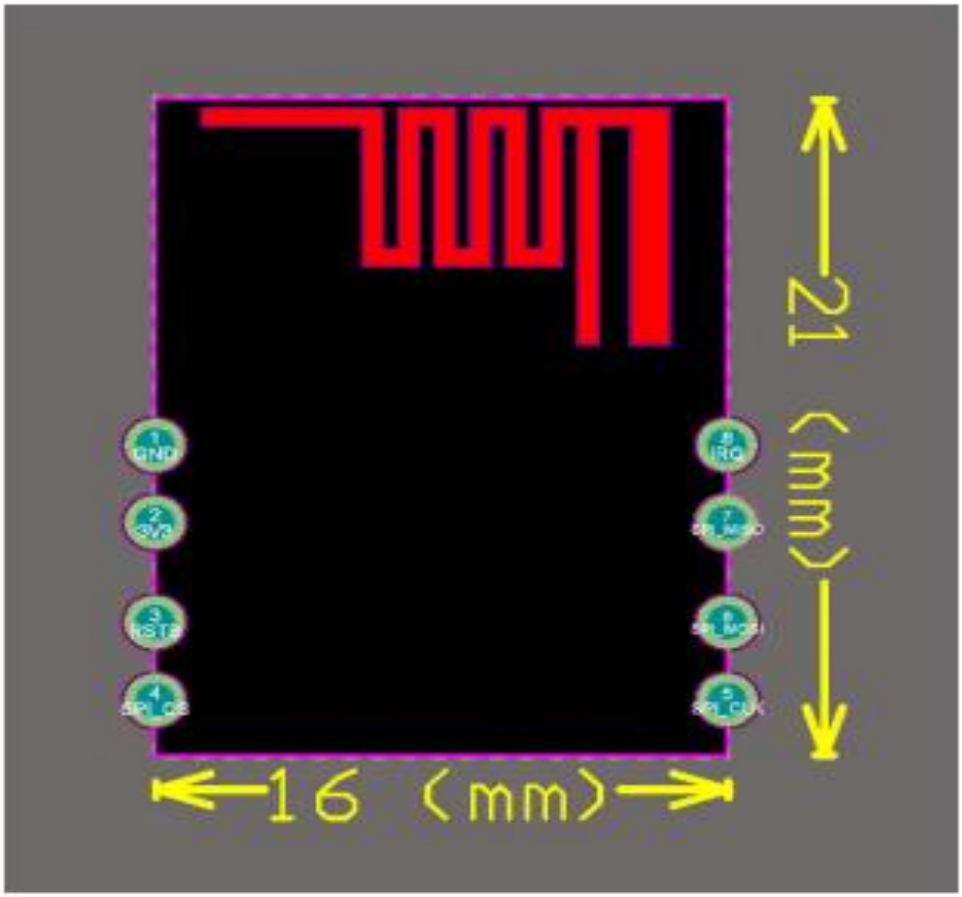
Six. Description of pin function

Pin number	Name	type	functional description
1	GND	GND	GND
2	VCC	PWR	3.3V mains input
3	RST	DI	Chip reset pin, active low, the register value is lost after reset, all become the default value
4	CS	DI	Enable signal, active low, pull low to make the chip exit sleep mode
5	CLK	DI	SPI clock input pin, IIC SCL clock line
6	MOSI	DI	SPI data input pin

7	MISO	DI	SPI data output pin
8	IRQ	DI	Transmit and receive status flag

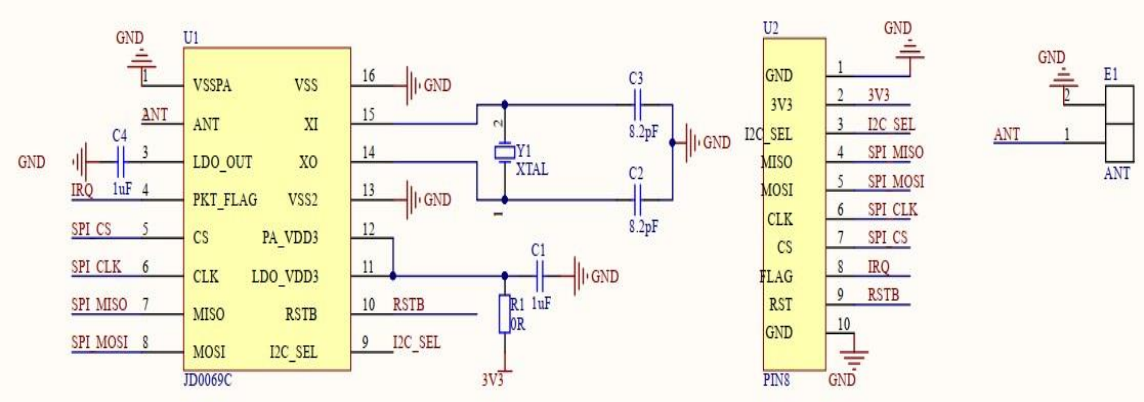
Table 6

Seven. External dimension



Eight. Application wiring diagram

3.3V System application circuit



Nine. PCB-layout and installation considerations

Module considerations：

1. No line under the antenna, keep the antenna part clear。

2. 3.3V power supply should be kept stable and clean, If the noise or interference of 3.3V power supply is relatively large, it is suggested that the RF module should be supplied after the RC or LC filtering.

3. The RF shield should be well grounded to improve the anti-interference ability of the module

4. Installation instructions：

a. Before installation, check whether the shield shape is intact and the logo is complete。

b. The module adopts the half-hole welding mode, and it is necessary to ensure that the semi-hole welding position of the main plate is coincident with the half hole of the module to avoid welding short circuit.

c. The welding position of the main plate and half hole shall overlap with the half hole of

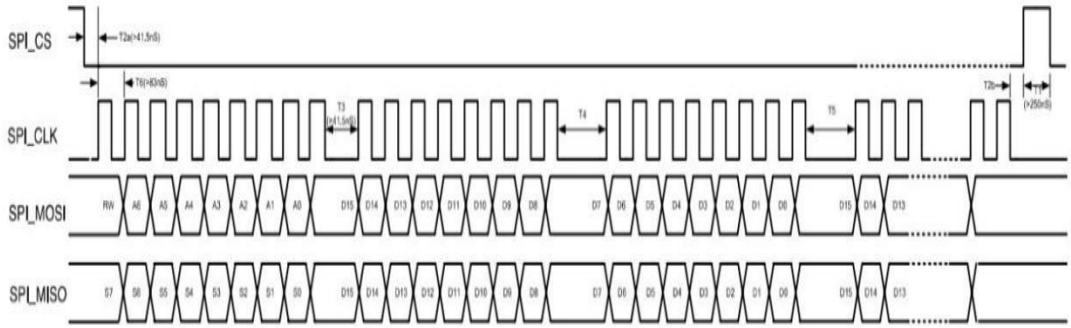
the module to avoid welding short circuit。

d. The MCU is used to drive software, which can communicate with other modules。

Warning: after all equipment has been installed, switch on power。

Ten. Communication Interface

SPI time-sequential format



Picture 10-1

Notes:

1. SPI to drop along sampling data，rise along the change data；MCU under control SPI_MOSI be bound after SPI_CLK raise that to change the data。

2. SPI read write bit： write=0，read=1。

3. The access to FIFO register 0X28 can be read by byte. Access to multiple FIFO data can be used with a SPI_ CS cycle.

4. When accessing other registers except FIFO, one reads and reads 16bits.

5.When accessing multiple registers except FIFO, you can use a SPI CS cycle. At this point, the address will only be written once, then the 16bit data, and the chip will automatically increase the register address when a register value is written.

SPI Timing requirements

Name	Min	Typ.	Max	Description
T1	250ns			Interval between two SPI visits
T2a,T2b	41.5ns			Interval between SPI_CS and SPI_CLK
T3	Note1			Address and data interval
T4	Note1			High byte and low byte interval
T5	Note2			Interval between two registers
T6	83ns			Clock cycle of SPI_CLK

picture 10-2

Notes:

1. In the FIFO data in the access register 0x28, the chip needs 450ns to find the correct pointer address read by FIFO.

2. When reading FIFO data in register 0x28, at least wait for 450ns. When reading other registers, T5min=41.5ns

Eleven. Partial register description

RF Synthesizer TX/RX control Register 0x00 default : 0x0030

Bit	Name	R/W	Description	Default
15	TX_EN	R/W	Enable the chip to enter the sending state, 1 is valid	0
14	RX_EN	R/W	To enable the chip to enter the receiving state, 1 is valid Note: TX EN and RX EN cannot be 1 at the same time, while at 0, the chip is in IDLE state	0
13-12	reserved	R/W		00
11-7	SWALLOW[4:0]	R/W	When RF PLL DIIRECT= 1, the carrier frequency is set directly by the register：	00000

			RF={reg0[6:0],reg0[13:9]}	
6-0	RF_PLL_CH_NO[6:0]	R/W	When RF PLL DIIRECT= 0, the carrier frequency is set by the channel number： RF=2402+RF_PLL_CH_NO[6:0]	110000 f=2450MHz

Table 11-1

Miscellaneous configuration Register 0x01 default: 0x2077

Bit	Name	R/W	Description	Default
15	Sleep_mode	R/W	Enable the chip to enter the sleep mode, 1 is valid（SPI CS must maintain high level simultaneously）	0
14		R/W		0
13	CRC_EN	R/W	0: CRC close 1: CRC open	1
12				
11				
10	RF_PLL_DIRECT	R/W	当 RF_PLL_DIIRECT=1 RF={reg0[6:0],reg0[13:9]} otherwise RF=2402+RF_PLL_CH_NO[6:0]	0
9	Pkt_hint_pority	R/W	1: PKT/FIFO flag Low effective 0: PKT/FIFO flag High effective	0
8	Miso_tri_opt	R/W	0: SPI_CS=1 time SPI_MISO For high impedance output 1: SPI_CS=1 time SPI_MISO For low level output	0
7	Reset_system	W/R	1：Enable the chip to perform software reset Note: reg0x1e[0] must be put 1 before reset.	0
6-4				
3	Auto-ack	R/W	1:Send an ACK after receiving the data 0: After receiving the data, no ACK is sent to enter IDLE directly	0
2	Pack_lenth_en	R/W	1: The first byte of the payload is the package length	1
1	Fw_term_tx	R/W	0: The MCU controls when the TX state is terminated 1: When FIFO writes a pointer equal	1

			to read a pointer, the chip automatically ends the TX state	
0	SCRAMBLE_EN	R/W	0: scramble off 1: scramble on	1

Table 11-2

PA Power Control Register 0x02 default: 0x4060

Bit	Name	R/W	Description	Default
15-12	reserved	R/W		0011
11-8	reserved	R/W	rev	0000
7-4	reserved	R/W		1000
3-0	PA_PW_SET[4:0]	R/W	PA output power control： 1111: min 1000: med 0000: max	0000

Table 11-3

Operation configuration Register 0x03 default: 0x5800

Bit	Name	R/W	Description	Default
15-13	Preamble_len[2:0]	R/W	000: 1 byte, 10101010 001: 2 byte, 10101010 10101010 111: 8 byte, 10101010	010
12-11	Syncword_len[1:0]	R/W	00: 16 bits,{reg31[15:0]} 01: 32 bits, {reg31[15:0], reg34[15:0]} 10: 48 bits, {reg31[15:0], reg33[15:0], reg34[15:0]} 11: 64 bits, {reg31[15:0], reg32[15:0], reg33[15:0], reg34[15:0]}	11
10-8	Trailer_len[2:0]	R/W	000: 4 bits, 1010 001: 6 bits, 101010 ..... 111: 18 bits,101010.....101010	000
7-6	Data packet type[1:0]	R/W	00: NRZ law data 01:Manchester data type 10: 8/10 line code 11: interleave data type	00
5-4	FEC type[1:0]	R/W	00: No FEC 01: FEC 13 10: FEC 23	00

			11: reserve, same as 00	
3				
2-0	brclk_sel[2:0]	R/W	000: brclk keep 0 001: xtal_core out 010: crystal divided by 6, 2M out 011: crystal divided by 12, 1M out 100: APLL_clk out 101: clk_tx_out	000

Table 11-4

Operating configuration Register 0x07 default: 0x7311

Bit	Name	R/W	Description	Default
15	EN_VCO_CAL_IDLE	R/W	1:Manually enable the VCO calibration process in IDLE state	0
14	TXRX_VCO_CAL_EN	R/W	1: In TX/RX state, VCO is automatically calibrated	1
13-10	TXRX_vco_tim[3:0]	R/W	VCO automatic calibration waiting time in TXRX state： 0000: 12us 0001: 14us 1111: 42us	1100
9-0				

Table 11-5

Timing configuration Register 0x0b default: 0x837F

Bit	Name	R/W	Description	Default
15-12	TX_CW_DLY[3:0]	R/W	PA After opening, send the CW's time： 0000: 4us 0001: 6us 1111: 34us	1000
11-8	Re_transmit_time	R/W	ACK When the function is turned on, the maximum retransmission： 2H: 2 times 3H: 3 times	0011
7-6		R/W	01	
5-0	Rx_ack_time[5:0]	R/W	The time the transmitter waits for ACK to return ： T=16us x	111111

			Rx_ack_time[5:0] （More than this time, if you haven't received an ACK signal back, it will automatically resend）	

Table 11-6

Timing configuration Register 0x0c default: 0x3E11

Bit	Name	R/W	Description	Default
15-10	VCO_ON_DLY[5:0]	R/W	After starting TX/RX state, wait for VCO to stabilize time： 000000: 4us 000001: 8us 111111: 256us	001111
9-8	TX_PA_OFF_DLY[1:0]	R/W	PA OFF-Delay： 00: 4us 01: 6us 10: 8us 11: 10us	10
7-4	TX_PA_ON_DLY[3:0]	R/W	PA Open the time delay： x000: 4us x001: 8us x1111: 32us	0001
3-0	TX_SW_ON_DELAY[3:0]	R/W	TX_SW Open the time delay： 0000: 8us 0001: 12us 11111: 68us	0001

Table 11-7

RSSI value Register 0x11 Read only

Bit	Name	R	Description	Default
15-8	RAW_RSSI[7:0]	R	8 bit RSS value（Update in real time and keep maximum value）	
7-0	rssi_lat[7:0]	R	RSSI latch	

Table 11-8

Block status Register 0x12 Read only

Bit	Name	R	Description	Default	Optium

15-14					
13	FIFO_FLAG	R	1: FIFO An empty or full mark bit		
12	reserved	R			
11					
10	VCO_CAL_ERROR	R	1： VCO Calibration failure		
9-0					

Table 11-9

Main status Register 0x16 Read only

Bit	Name	R	Description	Default	Optium
15	CRC_error	R	1： CRC wrong 0: CRC correct		
14	FEC23_error	R	1： FEC23 wrong 0: FEC23 correct		
13-8	Framer_st	R	Framer state： 31H: ST_SLEEP 33H: ST_WAKE_UP.....		
7	Syncword_rev	R	1: Receiving syncword is valid only in the receiving state		
6	PKT_FLAG	R	Packet flag zone bit		
5-3	Tx_st[2:0]	R	Transmit packet control state 000: TX_IDLE 001:TX_ID 010: TX_CRC 011: TX_DATA 110: TX_DONE		
2-0	Rx_st[2:0]	R	Receive packet control state 000: RX_IDLE 001:RX_ID 010: RX_DATA 011: RX_TRAILER 100: RX_DONE 110: RX_CRC		

Table 11-10

AMS TEST Control Register 0x1c default: 0x4008

Bit	Name	R/W	Description	Default	Optim
15	RSSI_PDN	R/W	1: close RSSI function 0：open RSSI function	0	

14-0	R/W				

Table 11-11

Operating Control Register 0x1e default: 0x7FF4

Bit	Name	R/W	Description	Default	Optim
15-14	R/W	7FF4H			
0	Reg_Reset_EN	R/W	1:Open software reset function, 1 is valid. the reset of the chip can be accomplished by enabling the rewriteable regicao 7 to 1 to be 1 .		

Table 11-12

SYN_WORD_1 Register 0x1f default: 0x0101

Bit	Name	R/W	Description	Default
15-0	SYNC_WORD[15:0]	R/W	LSB bits of SYN_WORD is first	0101H

Table 11-13

SYN_WORD_2 Register 0x20 default: 0x0202

Bit	Name	R/W	Description	Default
15-0	SYNC_WORD[31:16]	R/W	LSB bits of SYN_WORD is first	0202H

Table 11-14

SYN_WORD_3 Register 0x21 default: 0x0303

Bit	Name	R/W	Description	Default
15-0	SYNC_WORD[47:32]	R/W	LSB bits of SYN_WORD is first	0303H

Table 11-15

SYN_WORD_4 Register 0x22 default: 0x0404

Bit	Name	R/W	Description	Default
15-0	SYNC_WORD[63:48]	R/W	LSB bits of SYN_WORD is first	0404H

Table 11-16

Register 0x23 default: 0x8001

Bit	Name	R/W	Description	Default

15	FIFO_share_en	R/W	1: RX/TX FIFO share，overall length 64bytes 0： RX/TX FIFO Unshare，each 32bytes	1
14:0				

Table 11-17

FIFO threshold_reg Register 0x24 default: 0x4401

Bit	Name	R/W	Description	Default
15-11	FIFO_empty_threshold	R/W	Think of FIFO as an empty threshold	01000
10-6	FIFO_full_threshold	R/W	Think FIFO is full threshold	10000
5-0	Synword_threshold	R/W	Consider the correct threshold of syncword, XX means wrong XX bit is also considered correct	000001

Table 11-18

RX_FIFO_RD_PTR Register 0x25 default: 0x0000

Bit	Name	R/W	Description	Default
15	RXFIFO_CLR_W_PTR	R/W	1: Empty RX FIFO to write a pointer	0
14	RX_FIFO_WR_PTR *[6]*	R/W	RX FIFO Write the highest bit of the pointer, when fifo_share_en=1 valid	0
13-8	RX_FIFO_WR_PTR *[5:0]*	R/W	RX FIFO Write down 6 bits	0
7	RXFIFO_CLR_R_PTR	R/W	1: Empty RX FIFO read pointer	0
6	RX_FIFO_RD_PTR*[6]*	R/W	RX FIFO Read the highest bit of the pointer,when fifo_share_en=1 valid	0
5-0	RX_FIFO_RD_PTR*[5:0]*	R/W	RX FIFO Read pointer low 6 bits	0H

Table 11-19

TX_FIFO_RD_PTR Register 0x26 default: 0x0000

Bit	Name	R/W	Description	Default
15	TXFIFO_CLR_W_PT	R/W	1: Empty TX FIFO to write a pointer	0

	R			
14	TX_FIFO_WR_PTR[6]	R/W	TX FIFO Write the highest bit of the pointer, when fifo_share_en=1 valid	0
13-8	TX_FIFO_WR_PTR[5:0]	R/W	TX FIFO Write down 6 bits	0
7	TXFIFO_CLR_R_PTR	R/W	1: Empty RX FIFO read pointer	0
6	TX_FIFO_RD_PTR[6]	R/W	TX FIFO Read the highest bit of the pointer,when fifo_share_en=1 valid	0
5-0	TX_FIFO_RD_PTR[5:0]	R/W	TX FIFO Write down 6 bits	0H

Table 11-20

TX_FIFO_REG Register 0x27 default: 0x0000

Bit	Name	R/W	Description	Default
15-0	TX_FIFO_REG	R/W	MCU write FIFO Data interface	0000H

Table 11-21

RX_FIFO_REG Register 0x28 default: 0x0000

Bit	Name	R/W	Description	Default
15-0	RX_FIFO_REG	R/W	MCU read FIFO Data interface	0000H

Table 11-22

Twelve. Register default values and optimization

The chip has 42 registers, and after the reset, all registers are the default values, as shown in table 12 1. When working normally, you only need to optimize the values of a few registers, as shown in Table 12, 2

Register default

Address	reset value	Address	reset value
0x00	0x0030	0x15	Read only
0x01	0x2077	0x16	Read only
0x02	0x3080	0x17	0x0000
0x03	0X5800	0x18	0x6FE1

0x04	0x4A00	0x19	0x1300
0x05	0x7126	0x1a	0x07F7
0x06	0x1988	0x1b	0x1800
0x07	0x7311	0x1c	0x4008
0x08	0x1659	0x1d	空
0x09	0x007B	0x1e	0x7FF4
0x0a	0x2433	0x1f	0x0101
0x0b	0x837F	0x20	0x0202
0x0c	0x3E11	0x21	0x0303
Ox0d	0x6000	0x22	0x0404
0x0e	0x4c00	0x23	0x8001
0x0f	0x6609	0x24	0x4401
0x10	0x5F8F	0x25	0x0000
0x11	Read only	0x26	0x0000
0x12	Read only	0x27	0x0000
0x13	Read only	0x28	0x0000
0x14	Read only	0x29	0x0000

Table 12-1

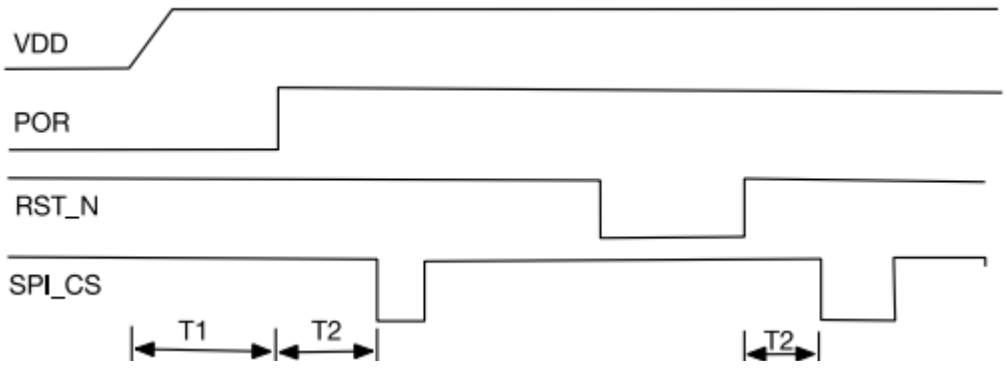
Register optimization

Address	Opt value
0x0a	0x2053
0x03	0x5810

Table 12-2

Thirteen. Attention

1、Power and register initialization data



Picture 13-1

1.Chip internal integration (POR) (if only internal reset, RST N feet only need to be raised or suspended), T1 time for power reset time, about 0.5ms

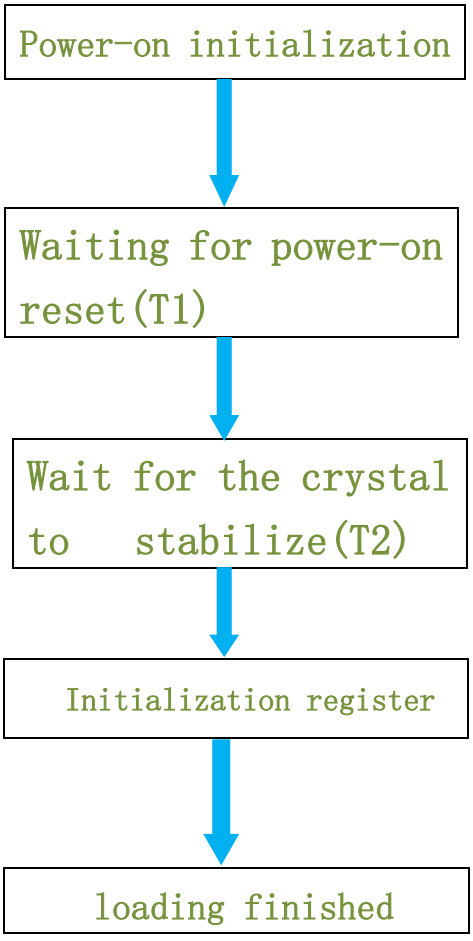
2. T2 is the crystal oscillator stabilization time, about 10ms, and then the register is initialized by the MCU

3. After the register is initialized, the chip can start transmitting or receiving data

4.In addition to internal automatic reset, there are two other ways to reset the chip：

a、 RST_N Pin reset： RST_N Reset the chip for low time

b、 Software reset: first write 0x1e[0] register as' 1 ', enabling software reset function, and '1' to write '1' on 0x01[7] to complete the reset operation. Using internal POR and software reset functions, RST N pins can be saved to save MCU resources, while RST N can be suspended or up to VDD33.



Picture 13-2

2、Enter sleep mode and wake up

When the SPI CS pulls high, and the MCU writes register 0x01 [15], the chip enters the sleep mode, and the current <1uA, the value of the register in the sleep mode can be maintained. When SPI CS is low, the chip automatically wakes up into IDLE state. The MCU will pull the SPI CS for a period (wait for crystal stability, about 1.5ms), and then write the SPI data.

3、Packet format

Air packet format

Preamble: 1~8 bytes,Can be set up.

SYNC: 16/32/48/64 bits, Can be set up.

Trailer: 4~18 bits, Can be set up..

Payload: TX/RX data. There are 4 data types:

Raw data

8bit/10bitlinecode

Manchester

Interleave with FEC option

CRC: 16-bit CRC is optional.

4、FIFO length

The default is 64 bytes, receive and send share, and can be set up to use 32 bytes to set 0x23[15] to 0, which USES 32 bytes each

5、clean FIFO hand

The read-write pointer that receives FIFO and sends FIFO can be removed by writing '1' at 0x25, 0x26 corresponding register。When the packet is received, the read pointer indicates how much bytes data is in FIFO. When the receiver receives SYNC, the receiving FIFO writes the pointer automatically 0. When the emitter sends out the data, a FIFO reading pointer automatically clears 0.

6、data packet payload length

Two ways to determine TX/RX package length. When register 0x01[2]= 1, the internal state of the state can detect the package length according to the payload first byte data. If you want to send 8 bytes, the first byte should write 8 and the total word length is 9 bytes.

When register 0x01[2]= 0, the first byte data has no special significance. The packet length will be determined by when the TX FIFO is empty or when the TX EN is cleared, see the table below.

0x01[2] pack_length_en	0x01[1] fw_term_tx	
0	0	When TX EN= 0, terminate the launch. When RX EN= 0, it terminates.
	1	When FIFO is empty, automatically terminates the launch When RX EN= 0, it terminates。
1	x	The first byte of playload shows the length of the packet , 0 to 64 bytes . When all data has been sent , the transmission terminates automatically

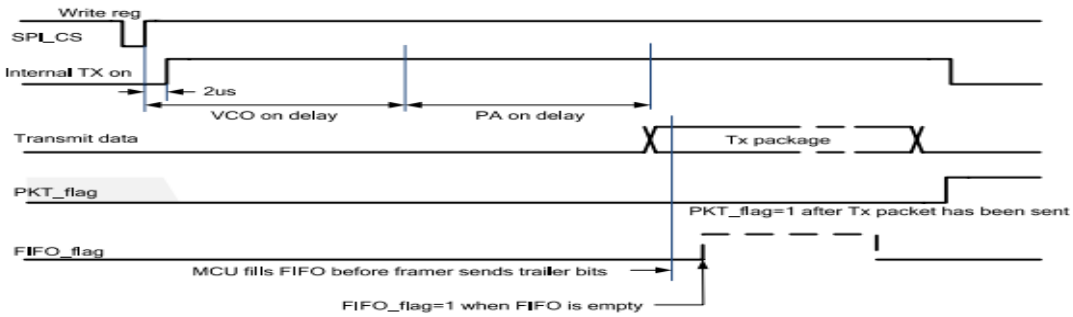
Table 13-1

7、The state machine determines the length of the package

When register 0x01[2]= 1, the first byte of payload indicates the package length, and the maximum length is 64 bytes

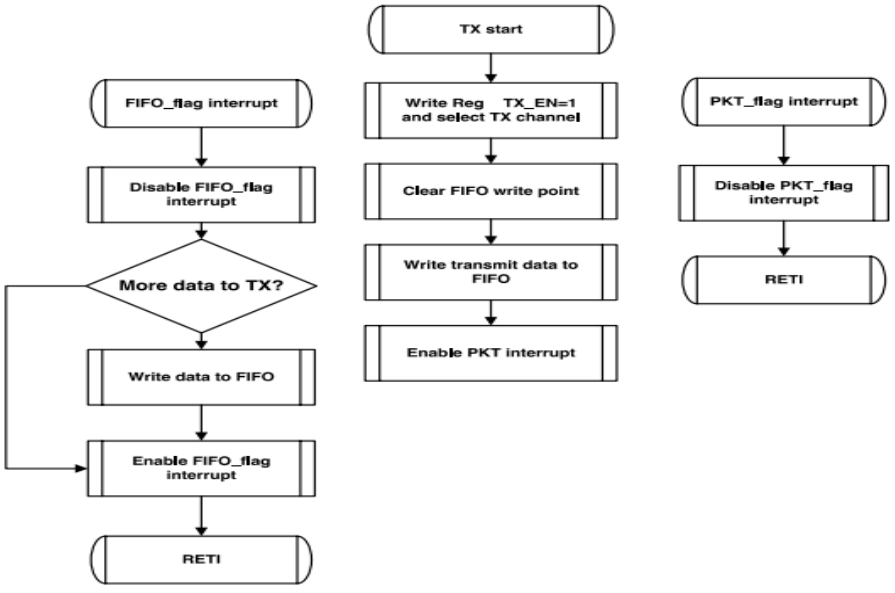
1、Launch timing

Below shows TX time series: when MCU writes register 0x00[15] to '1', and write register 0x00[6:0] to set up the transmitting channel, the chip will automatically generate the package according to the payload. MCU needs to write the launch data before launching the trailer. College if the packet length more than the length of the FIFO, MCU need to write a FIFO data many times. FIFO flag (reg0x12[13]) indicates whether FIFO is empty.



Picture 13-3

TX Timing diagram



Picture 13-4

MCU sending data packet flow chart FIFO and PKT flags are used as interrupt signals of MCU

In the above flow chart, you can send the state machine first, then send data to send FIFO, which can improve MCU efficiency, but ensure that all data is written before the packet is sent. If the time required to write is very long, you should write all the data before starting the sending state.

//////////////// Launch process example：

The initialization register, which is the register value that needs to be optimized

write reg[0x02] = 0x4060;

write reg[0x03] = 0x5810;

write reg[0x05] = 0x7fa6;

write reg[0x0A] = 0x2053;

write reg[0x0D] = 0x6003;

write reg[0x0F] = 0x661d;

write reg[0x1A] = 0x00f7;

write reg[0x01] = 0x207f;

write reg[0x0B] = 0x857f;

2, Clear and send FIFO

write reg[0x26] = 0x8080;

3, Write data to the FIFO（For example, you send data： 0x05 0x01 0x02 0x03 0x04 0x05, The first byte represents the length）

write reg[0x27] = 0x0501;

write reg[0x27] = 0x0203;

write reg[0x27] = 0x0405;

4, Start the send to enable, and set the channel

write reg[0x00] = 0x80XX;//Low 7 is channel number

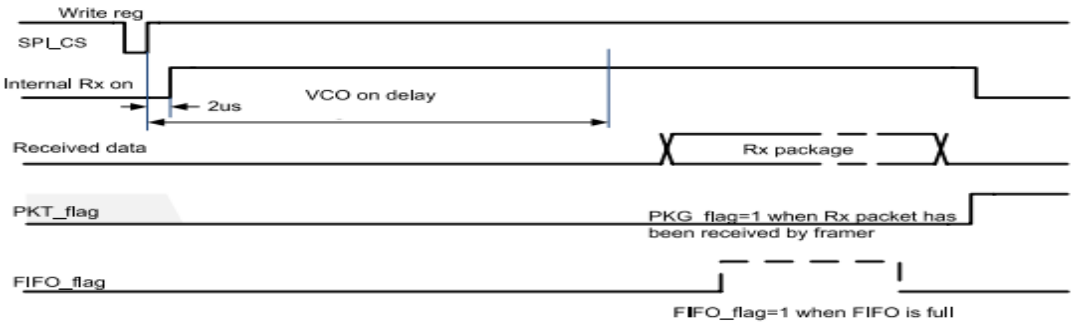
5，Wait for the PKT flag to be high, indicating that the delivery is complete

2、Receive sequence

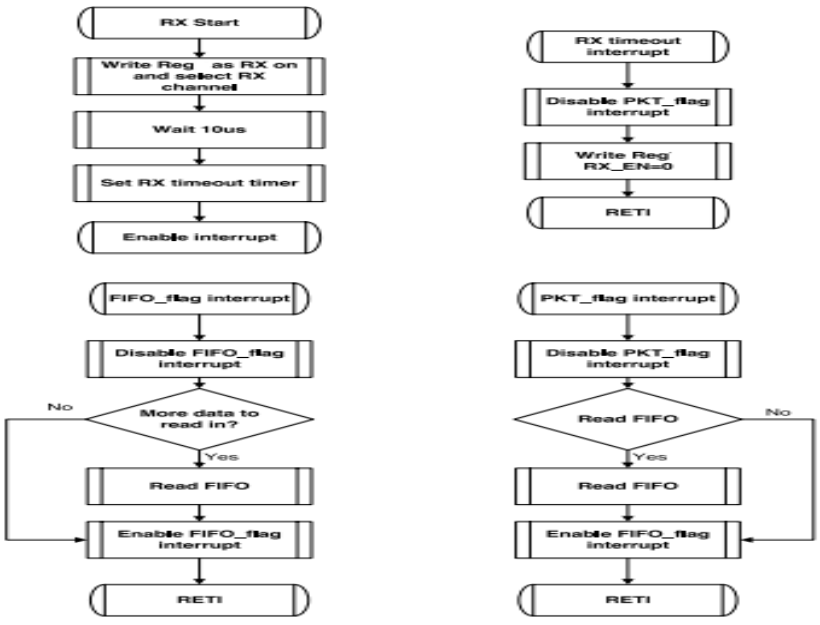
The RX reception sequence is shown below. When MCU writes register 0x00[14] to 1 and selects a good receiver channel, the chip will open RX and wait for the correct syncword. When the correct syncword is received, the chip will automatically start processing the packets. When the packet is processed, the state machine will enter IDLE.

When received packets longer than 63 bytes, FIFO flag will work, meaning that the MCU must read data from FIFO.

In weak signals, multipath and long distance, you may not receive the correct syncword. To avoid a crash, MCU needs to do a timer. In most applications, packets are received within a certain time window, and if the system is not received, the timer returns to normal mode.



RX sequence chart



Picture 13-6

Example of receiving process：

1,The initialization register, which is the register value that needs to be optimized

write reg[0x02] = 0x4026;

write reg[0x03] = 0x5810;

write reg[0x05] = 0x7fa6;

write reg[0x0A] = 0x3453;

write reg[0x0D] = 0x6003;

write reg[0x0F] = 0x661d;

write reg[0x1A] = 0x00f7;

write reg[0x18] = 0x6ffd;

write reg[0x27] = 0x1800;

write reg[0x01] = 0x207f;

write reg[0x0B] = 0x857f;

2, Empty the receiving FIFO

write reg[0x25] = 0x8080;

4,Start receive enable, and set channel

write reg[0x00] = 0x40XX; //Low 7 is channel number

5，Wait for the PKT flag to be high, indicating that it receives a frame of data, and starts to read the data from FIFO, and the first byte read is the data length

read reg[0x28]

readreg[0x28], 。。。。。。。

3、Automatic reply and automatic retransmission

The function can be configured with registers：

Write register 0x01[3] = 1 to enable auto-ack function。

Write register 0x0b [11:8], set the number of resend, the default value is 3, that is, after the first

failure, resend twice.

Write register 0x0b[5:0], setting time, waiting for an ACK default is 0 x3f, each step is 16 us, a total of approximately 1 ms, said if the received an ACK packet waiting time of 1 ms and retransmission times no will to send packets to the maximum.

Can make and don't make corresponding functions can be AUTO - ACK PKT FLAG up time is different: after the launch party receives an ACK packet or not yet received an ACK packet retransmission times has the biggest, then pull up PKT FLAG, exit the launching state, MCU in PKT FLAG raising, readable registers 0 x16 [7], if 1 receives an ACK packet. The receiver sends out an ACK packet after receiving the data packet, then exits the receiving state and raises the PKT_FLAG signal. The time of ACK packet is about 150us, which is determined by the length of preamble and syncword.

4、CRC16 verification

This function is enabled by default。

Write register 0x01[13] to turn on or off CRC functions。

When CRC is turned on but the AUTO - ACK function is not turned on , the chip reception state is not affected by the CRC state , but the register has a CRC error status bit . After the PKT _ flag is pulled up , the MCU can read 0x16 × 15 bits to determine if the CRC is correct to determine whether the frame data needs to be read .

If the CRC is on and the AUTO - ACK function is turned on , the chip will automatically determine if the CRC is correct , and if the receiver PKT _ FLAG is pulled up , the packet is received and the CRC is correct .

8、The application layer determines the package length

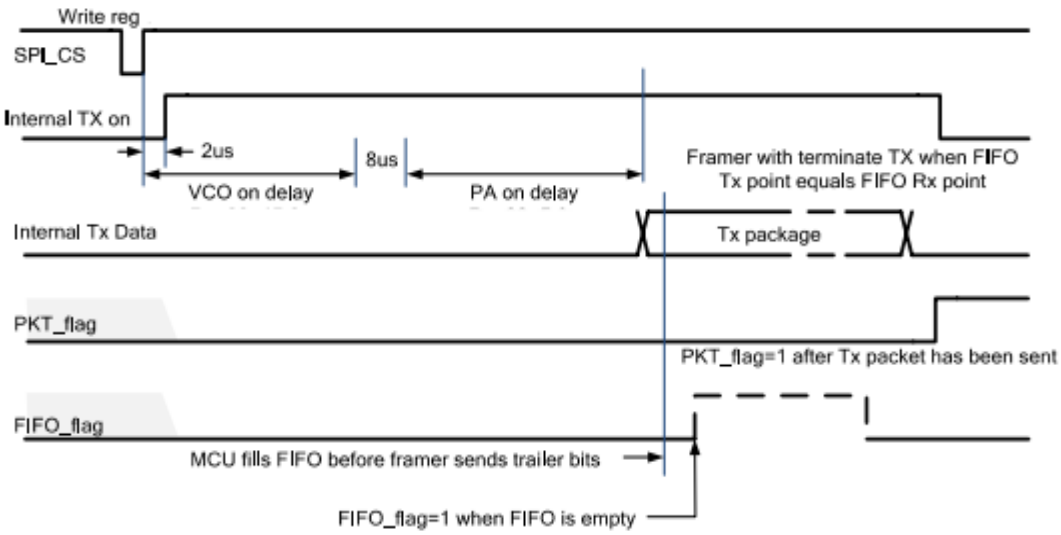
When register 0x01[2]= 0, the payload first byte has no special meaning, and the package

length is determined by the state of register 0x01 [1].

1、fw_term_tx=1

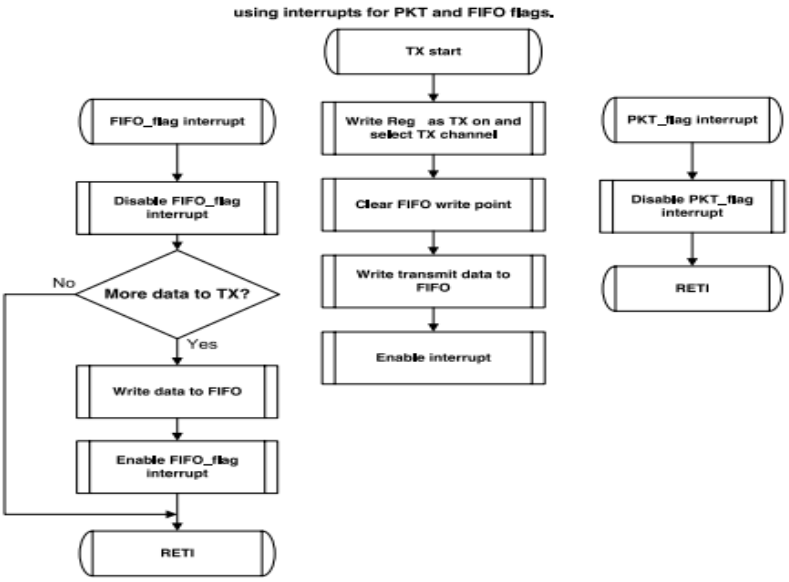
When register 0 x01 [1] = 1, when the firing data, the system will send FIFO write pointer and read pointer, if the MCU to stop sending FIFO data written, chips will eventually detected when the FIFO is empty, and then automatically exit status.

The sequence diagram is as follows：



Picture 13-5

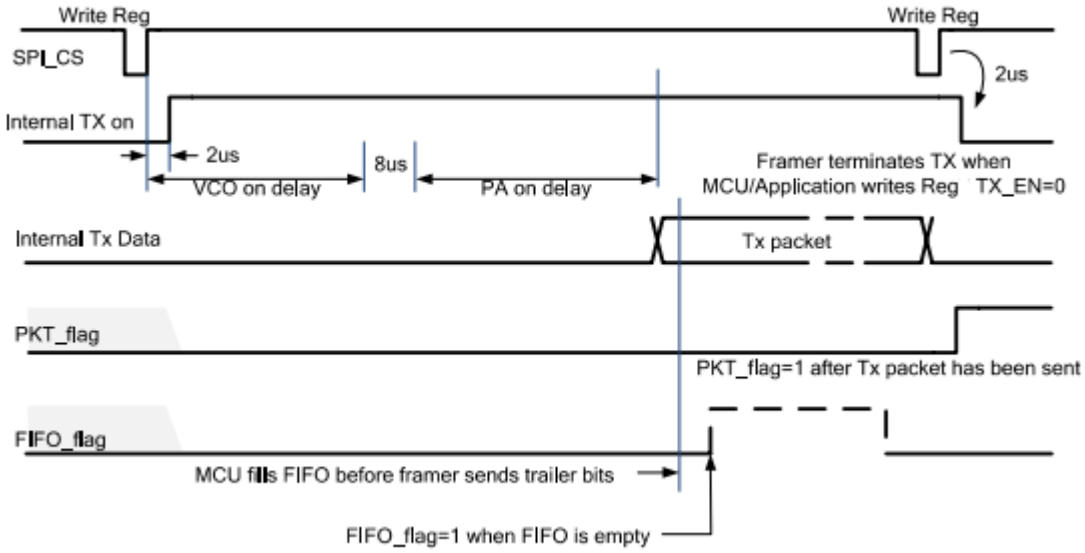
Note: when register 0x01[1]=1, do not allow FIFO to be empty or overfull, the FIFO full/empty THRESHOLD can be set by the register FIFO THRESHOLD, and the optimal value is determined by the SPI speed and the MCU reading and writing FIFO speed.



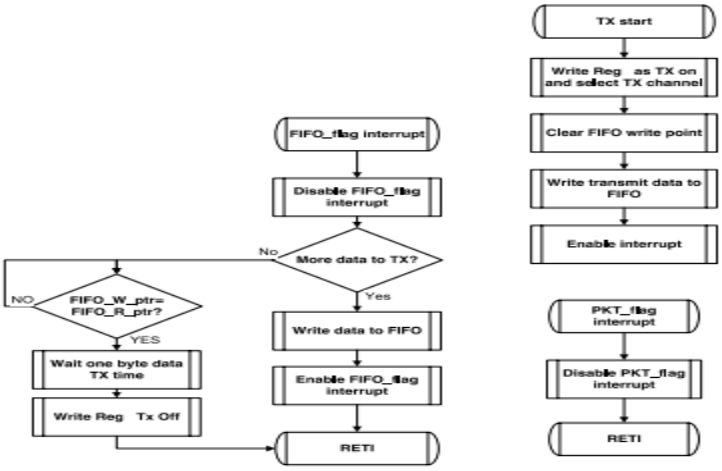
Picture 13-6

2、fw_term_tx=0(TX)

When register 0x01[2:1]=2 'b00, the system only stops firing when the register 0x00[15] tx en=0.



Picture 13-7

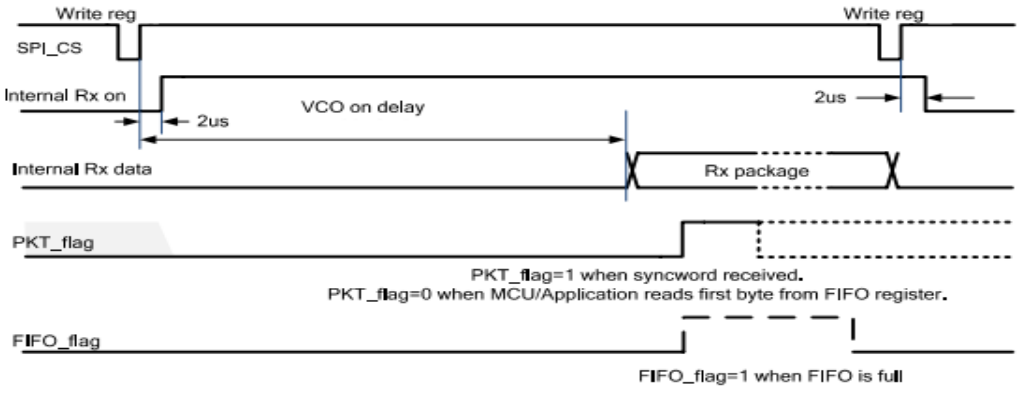


Picture 13-8

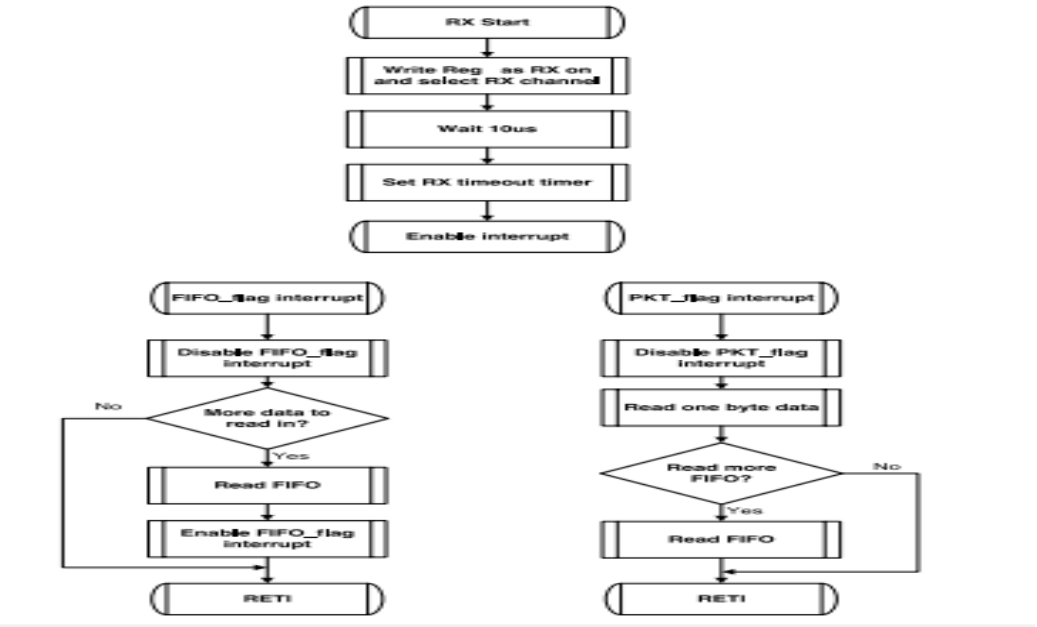
3、fw_term_tx=0 (RX)

When Reg0x01[2]= 0, the chip will start receiving the package at Reg0x00[14] when it is written as 1 (RX EN= 1), and the chip will automatically set the RX to the fixed channel. After waiting for some time to stabilize the internal clock and the RX circuit, the chip began to look for syncword in the received signal, and once found, it would pull the PKT FLAG and write the received data to FIFO. The PKT FLAG will always be high until the MCU reads the data in FIFO. When the MCU reads the data, the PKT FLAG will pull down until the next TX/RX cycle.

When Reg0x01[2:1]= 'b00 or' b01, the Reg0x00[14] must be written to 0 to exit the RX state.



Picture 13-9



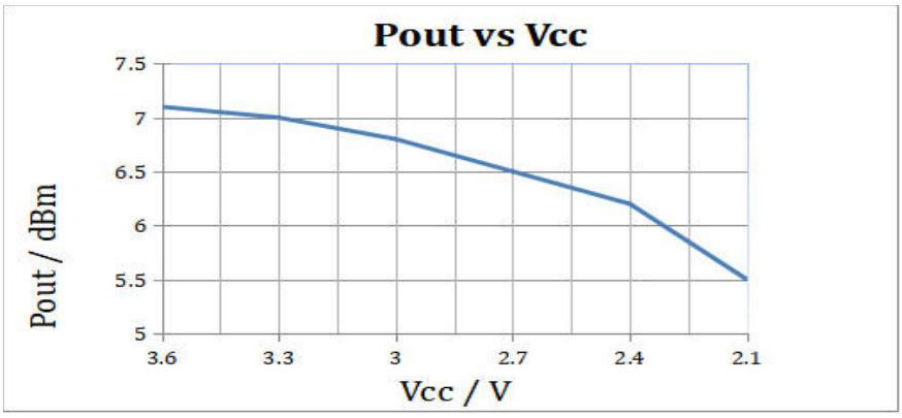
Picture 13-10

4、 PA Output power setting

. The output power of PA can be set by register reg0x02. The maximum output power can reach +8dBm, and the minimum can reach -24dBm. The following table lists some power configurations (if you need other power configurations, please contact the company's technical staff)

Reg0x02	Pout （dBm）	Ivcc （mA）
0x4060	7	34
0x4061	6	30
0x4065	3	23
0x4067	1	20
0x2020	0	16
0x2061	-2	15
0x2064	-5	13
0x2066	-7	12
0x2068	-10	11.6
0x306A	-13	11
0x307A	-16	9
0x306F	-24	8

The change of the power supply voltage will cause the output power to also change, so you need to pay attention to it in practical application. The following is the corresponding relationship between output power and power supply voltage:



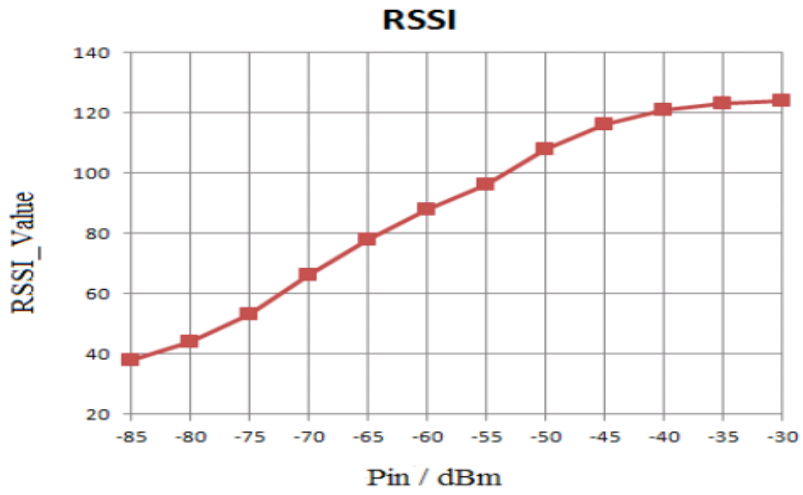
5、RSSI

Support RSSI detection function, in RX state, can read real-time RSSI directly through reg0x11[15:8]

(1)、Set the chip to the RX state；

(2)、The reg0x1c[15] was first written as 1, and the RSSI was closed to eliminate the remaining RSSI values. Then, the reg0x1c[15] is then written as 0, and the RSSI detection function is opened. After waiting for 60us, the current RSSI value can be read through reg0x11 [15:8].

The following figure is the measured performance of the chip RSSI detection function：



Picture 13-11

Forteen、FAQ

1、How to troubleshoot the SPI/I2C interface

a、First check whether the power supply of the chip is normal, whether the VDD33 foot has voltage (3.3 V) input, and the RF VDD foot has 1.8V or so voltage output;

b、Check the vibration of the chip. The default is IDLE state after the power is reset on the chip, and the crystal is switched on, and the power consumption is about 0.6 mA.XI and XO leg voltage by the multimeter at this time should be around 0.9 V, with an oscilloscope probe on the XOUT feet should be able to see 12 MHZ sine wave (if the oscilloscope probe capacitance is too large, low impedance vibration may cause crystals，The probe is recommended to be hit on the X10 slot）；

c、When the program runs, check whether there is a signal on the digital interface；

d、If the above conditions are normal, the time order of the interface is fine, and you should be able to read and write the register normally。

2、 There are several main types of chips

There are four main types of chips:

1、 IDLE state：When the chip is on (reset) the default is IDLE state, when the crystal is switched on, and the power consumption is about 0.6mA；

2、 RX state：Write register reg0x00=0x40XX (XX represents the channel number) to enter the RX state；

3、 TX state：Write register reg0x00=0x80XX (XX represents the channel number) to enter the TX state;

4、 Sleep state：Keep the SPI CS high and write reg0x01[15] as "1" to enter the sleep state, At this time, the power consumption of the chip is about 1uA. In the sleep state, the value of the register can still be maintained.

3、How to verify TX function and how to test PA output power

a、The chip is reset and the optimized value is written to the corresponding register according to the instructions (see table 10.2).；

b、Write register reg0x01= 0x2070, and write register reg0x00=0x8030 startup TX, and use the spectrometer to measure the signal output of 2.45ghz on the ANT feet (and other channel Numbers can be set for testing).。

c、Changing the value of register reg0x02 can adjust the size of PA output power；

4、Typical transceiver flow

(1)、Sending process:

a、The initialization register, which is the register value that needs to be optimized

write reg[0x02] = 0x4060;

write reg[0x03] = 0x5810;

write reg[0x05] = 0x7fa6;

write reg[0x0A] = 0x2053;

write reg[0x0D] = 0x6003;

write reg[0x0F] = 0x661d;

write reg[0x1A] = 0x00f7;

write reg[0x01] = 0x207f;

write reg[0x0B] = 0x857f;

b、Clear to send FIFO

write reg[0x26] = 0x8080

c、Write data to FIFO, such as the data sent： 0x05 0x01 0x02 0x03 0x04 0x05（The first byte represents length, the last five bytes are data, and the total length is 6 bytes.

write reg[0x27] = 0x0501;

write reg[0x27] = 0x0203;

write reg[0x27] = 0x0405;

d、Start sending enable and set the channel at the same time

write reg[0x00] = 0x80XX; // Low 7 is channel number

e、wait pkt _flag for highly，Indicates the completion of the transmission

(2)、Receiving process:

a、The initialization register, which is the register value that needs to be optimized

write reg[0x02] = 0x4026;

write reg[0x03] = 0x5810;

write reg[0x05] = 0x7fa6;

write reg[0x0A] = 0x3453;

write reg[0x0D] = 0x6003;

write reg[0x0F] = 0x661d;

write reg[0x1A] = 0x00f7;

write reg[0x18] = 0x6ffd;

write reg[0x27] = 0x1800;

write reg[0x01] = 0x207f;

write reg[0x0B] = 0x857f;

b、Empty the receiving FIFO

write reg[0x25] = 0x8080;

c、Start the receive enabled, and set the channel number

write reg[0x00] = 0x40XX; //Low 7 is channel number

d、Waiting PKT flag is high, said receives a frame data, this time can be read by reg0x16 [15] to judge the CRC is correct (reg0x16 [15] = 0 means CRC is correct, if CRC error, the bit will be set to "1", but once again into the receiving reg0x16 [15] will automatically reset), if the CRC is correct, that received the correct data, the MCU can read the required data from the receive FIFO, read the first byte of data length.

read reg[0x28]

read reg[0x28]

。。。。。。。

Note: under the condition of CRC open but without an AUTO_ACK is open (chip reset after the default state), in the process of receiving PKT_flag raising is not affected by CRC is PKT_flag raising cannot guarantee received packets must be correct, under certain conditions, even without the sender sends data, the receiver receives the noise or interference can be just and synchronization code matching thus raising PKT flag. Therefore, the PKT flag pulls high but if the CRC is incorrect, it should be re-entered into the receiving process (clear FIFO, enabling it to receive...).

5、 PKT_FALG How does the state change

After the TX is started, the PKT FLAG will automatically pull down, the PKT FLAG will be raised after the data is sent, and then the PKT FLAG will remain high until the TX or RX is started again. Under the default configuration, start the RX after PKT FLAG will automatically pull down, and then the chip will always search syncword, once received the correct syncword, chips will continue to receive, deal with subsequent packets, packets, such as receiving, after the completion of PKT FLAG high and maintain high level until once again to start the TX and RX.

6、 SYNCWORD How to set up

In the receiving state, the chip will continue to receive and process the subsequent packets only after receiving the correct syncword, so the setting of syncword has some effect on the reception performance. Through reg0x03[12:11] can set the length of the syncword, [and] can be set by reg0x1f ~ reg0x22 syncword concrete data, through reg0x24[5:0] can set the number of fault-tolerant bit syncword syncword (if set to 1, received wrong 1 bit also will receive a follow-up data). If syncword is long and fault-tolerant, it might be syncwoIt is possible that the data from the sending end is missed because of the error of syncword. If the syncword is set very short, the fault tolerance is set high, and the received noise or interference is easy to match with syncword and the data is wrong. Therefore, the setting of syncword should be determined according to the specific application environment. In general, the length is set to 48bit, and the fault tolerance of 1bit is better.

7、How to use auto-ack and resend

Write register 0x01[3] = 1 to enable auto-ack function. Write register 0x0b [11:8], set the number of resend, the default value is 3 times. After open the function, the receiving party after receiving data automatically returns an ACK signal to the sender, the sender after sending the data

will be automatically entered into a state of receiving, waiting for the receiver returns an ACK signal, if in a certain period of time (the time by0x0b[5:0] set, the default value is 0 x3f, about 1 ms) did not receive an ACK signal, then again send it again until it receives an ACK signal data or resend to reach maximum. The above process is automatically completed within the chip, without the need MCU intervention.

If the sender to open the function of auto - ack and resend, but the receiver is not open, the sender can't always get ack signals, after waiting for a certain period of time are sure to resend the same data again until reach maximum repetitions. This setting can be used as a hardware retransmission function.

Open auto - ack and retransmission, PKT FLAG raising time and didn't open the function of raising time is different: the sender signal or resend it receives an ack number will reach the maximum when PKT FLAG raising and exit the delivery status, PKT FLAG high register can be read after 0 x16 [7], if the "1" signal an ACK is received. The receiving party pulls the PKT FLAG and exits the receiving state after receiving the packet and automatically returning the ACK signal.

In case of low speed requirements, it is recommended to open the FEC function to improve performance. Turn on FEC13 or FEC23 by writing the register reg0x03[5:4]. FEC13 has better performance than FEC23, but the efficiency is also lower. It takes longer to send and receive the same data.

8、How does the state enter sleep, how to wake up, and how long does it take to wake up

Keep the SPI CS high and write reg0x01[15] as "1" to enter the sleep state. The SPI CS can wake up from the sleep state for a period of time to enter the IDLE state. The awakening time is mainly determined by the vibration and stability of the crystal, generally around 2ms.

9、How to prevent FIFO overflow

In sending or receiving data packets, in order to prevent spillage, FIFO can be set up by reg0x24 register the corresponding threshold, more than the threshold, the chip will give instructions, the indicator can be reg0x12 [13] FLAG (FIFO) to read.

10、Instructions for improving the working reliability of the chip

In order to improve the reliability of the chip and the product yield, the following improvements are recommended: 1. The optimized value of the 0x0a register is configured as 0x2403;

2. Before each start of sending and receiving, register 0x07 as 0x3f11 and then as 0x7f11 to ensure that the VCO works in the best band every time it receives or sends.

Example:

write reg[0x07] = 0x3f11; write reg[0x07] = 0x7f11;

write reg[0x00] = 0x80XX(TX) or write reg[0x00] = 0x40XX(RX) [XX is the channel number]

Fifteen、About IC ID with FCC ID

English:

"ThisdevicecomplieswithIndustryCanadalicence-exemptRSSstandard(s).Operationissubjectto thefollowingtwoconditions:(1)thisdevicemaynotcauseinterference,and(2)thisdevicemustacceptan yinterference,includinginterferencethatmaycauseundesiredoperationofthedevice.

French:

"LeprésentappareilestconformeauxCNRd'IndustrieCanadaapplicablesauxappareilsradioexem ptsdelicence.L'exploitationestautoriséeauxdeuxconditionssuivantes:(1)l'appareilnedoitpasproduir

edebrouillage,et(2)l'utilisateurdel'appareildoitacceptertoutbrouillageradioélectriquesubi,mêmesil

ebrouillageestsusceptibled'encompromettrelefonctionnement."

FCC STATEMENT :
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
This device may not cause harmful interference, and
This device must accept any interference received, including interference that may cause undesired operation.
Warning: Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
Reorient or relocate the receiving antenna.
Increase the separation between the equipment and receiver.
Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
Consult the dealer or an experienced radio/TV technician for help.

FCC Radiation Exposure Statement:
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.
This equipment should be installed and operated with minimum distance 5cm between the radiator & your body.

Sixteen、Manufacturer related information

Name：Jiangsu Jingweite Electronic Co. LTD

Address: Building 12, Lianfa industrial park, No.199, Tongyuan Rosad, Industrial park, Suzhou ,

Jiangsu province

Tel：0512-68566030

Web：http://www.js-jwt.com

requirement instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

2.2List of applicable FCC rules
FCC Part 15 Subpart C 15.249 & 15.207 & 15.209

2.3 Specific operational use conditions
This device is intended only for OEM integrators under the following conditions: The module must be installed in the host equipment such that 5 cm is maintained between the antenna and users, and the transmitter module may not be co-located with any other transmitter or antenna. The module shall be only used with the PCB antennas that has been originally tested and certified with this module. As long as 3 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).
Validity of using the module certification:
In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization for this module in combination with the host equipment is no longer considered valid and the FCC ID of the module cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.
2.4Limited module procedures .
The product is an unrestricted module.

2.5 Trace antenna designs

Not applicable. The module has its own antenna, and doesn't need a trace antenna etc.

2.6RF exposure considerations

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 5cm between the radiator & your body. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

2.7Antennas

Antenna Type: PCB Antenna Antenna Gain(Peak):1.96 dBi

2.8 Label and compliance information

Host product manufacturers need to provide a physical or e-label stating

"Contains FCC ID: 2AZLUJRF201103-1" with their finished product.

List of applicable FCC rules： FCC Part15 Subpart C, Section 15.247
2.9Information on test modes and additional testing requirements
To investigate the maximum EMI emission characteristics generates from EUT, the test system was pre-scanning tested base on the consideration of following EUT operation mode or test configuration mode which possible have effect on EMI emission level. Each of these EUT operation mode(s) or test configuration mode(s) mentioned above was evaluated respectively.
RADIATED EMISSION TEST (BELOW 1GHz):
Pre-Scan has been conducted to determine the worst-case mode from all possible combinations between available modulations, data rates, XYZ axis and antenna ports (if EUT with antenna diversity architecture).
For the test results, only the worst case was shown in test report.
RADIATED EMISSION TEST (ABOVE 1GHz):
Pre-Scan has been conducted to determine the worst-case mode from all possible combinations between available modulations, data rates, XYZ axis and antenna ports (if EUT with antenna diversity architecture).
2.10Additional testing Part15SubpartB disclaimer
The grantee should include a statement that the modular transmitter is only FCC authorized forthe specific rule parts (FCC Part 15.247&15.207&15.209..)transmitter rules)listedonthegrant， and that the host productmanufacturer is responsible for compliance to any other FCC rules that apply to the host notcovered by the modular transmitter grant of certification .If the grantee markets their product asbeing Part 15SubpartBcompliant(when it also contains unintentional - radiator digital circuit y)， then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed .
Federal Communication Commission Statement (FCC, U.S.)

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- **Reorient or relocate the receiving antenna.**
- **Increase the separation between the equipment and receiver.**
- **Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.**
- **Consult the dealer or an experienced radio/TV technician for help.**

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
FCC Caution:
Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.