VTech Communications LTD.

R&D Department

VTBM-A01 BT MODULE

Bluetooth® 5.0 Stereo Audio Module

Features:

- Complete, Fully Certified, Embedded 2.4GHz Bluetooth®Version5.0 Module
- Bluetooth Classic (BDR/EDR)
- Firmware can be field upgradable via SPI
- Compact surface mount module: 30 x 17 x 3mm³(cover changed)
- Castellated surface mount pads for easy and reliable host PCB mounting
- Perfect for Portable Battery Operated Devices
- Audio-In / Out

Operational:

- Operating voltage: 3.2V to 5.0V
- Temperature range: －40C to 85°C
- Simple, SPI interface
- Integrated crystal, internal voltage regulator, and matching circuitry
- Multiple I/O pins for control and status

RF/Analog:

- Frequency: 2.402 to 2.480 GHz
- Receive Sensitivity: －90 dBm (type) BDR receiver sensitivity
- Power Output: class 1 / +9dBm max.
- Connection Distance: >10m (free space and no interference)

Integrated power control regulation:

Audio processor：

- Dual I²S outputs

Supported sample rates of 8, 11.025,16, 22.05, 32,44.1, and 48kHz (DAC only)

- I²S input, SPDIF input (uncompressed PCM only) Stereo codec with 1 microphone input , stereo audio DAC
- USB audio
- Stereo audio ADC with line input, stereo audio DAC
- Support SCMS-T

Auxiliary features:

- Crystal oscillator with built-in digital trimming

Physical interfaces:

UART interface

- USB 2.0 (full-speed) interface, including
- USB charger detection
- 4-bit SPI flash memory interface
- SPI interface for debug and programming
- I²C master support
- Up to 14 general-purpose PIOs
- 3 LED drivers with PWM flasher independent of MCU

- 2 high-efficiency switch-mode regulators with 1.8 V and 1.35 V outputs direct from battery supply
- 3.3 V linear regulator for USB supply
- Low-voltage linear regulator for internal digital circuits
- Low-voltage linear regulator for internal analog circuits
- Power-on-reset detects low supply voltage
- Power management for ultralow power mode

Bluetooth features:

- Bluetooth v5.0 specification support
- A2DP v1.3.1
- AVRCP v1.6
- HFP v1.7
- QTIL's proximity pairing and QTIL's proximity connection

Battery charger:

- Lithium ion / Lithium polymer battery charger
- Charger supports 4.20 V and 4.35 V cells
- Instant-on function automatically selects the power supply between battery and USB, which enables operation even if the battery is fully discharged
- Fast charging support
  - Up to 200 mA with no external components
  - Up to 500 mA with external pass transistor
- Supports USB charger detection
- Support for thermistor protection of battery pack

Audio features:

- SBC, and AAC audio codecs
- Configurable Signal Detection to trigger events
- 1 bank of up to 10-stage Speaker Parametric EQ
- 6 banks of up to 5-stage User Parametric EQ for music enhancement
- Qualcomm®meloD™ Expansion audio processing: 3D stereo widening
- Compander to compress or expand the dynamic range of the audio
- Post Mastering to improve DAC fidelity
- Dual I²S outputs with crossover

1 Device overview

The stereo module VTBM-A01 BT Module provides a complete 2.4GHz Bluetooth system, based on Qualcomm 3008 chip which is a single-chip radio and baseband IC for Bluetooth,2.4GHz systems including basic rate, EDR. The chip integrates Bluetooth 5.0 radio transceiver.

Figure 1-1 shows the application block diagram.

Figure 1-1: Block Diagram:

The following depicts an example of VTBM-A01 BT Module operates as an independent system or connected to an MCU.

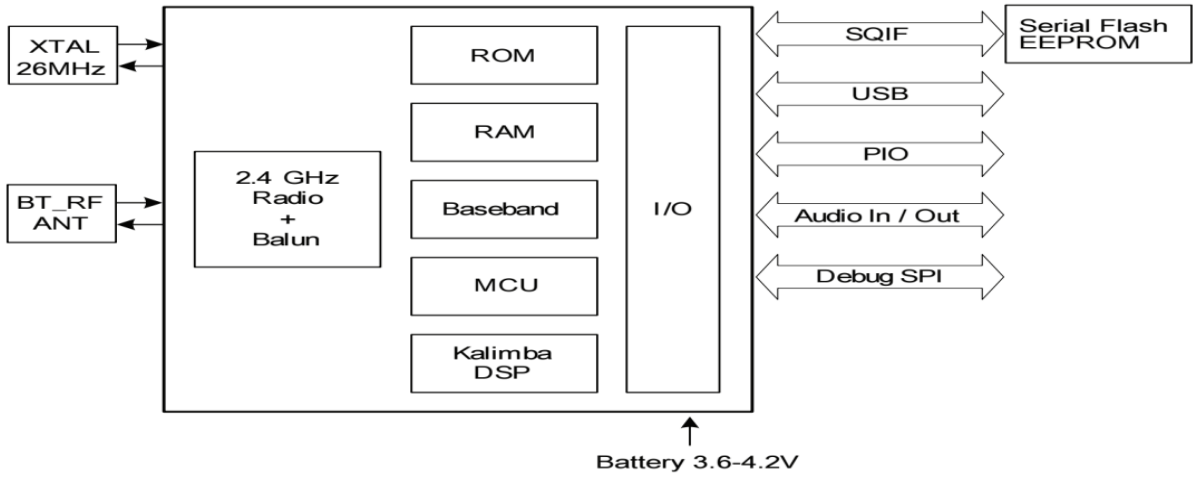


Figure 1-1

1.1 Interface description

VTBM-A01 pin diagram is shown in Figure 1-2. The pin descriptions are shown in Table 1-1

FIGURE 1-2: VTBM-A01 PIN DIAGRAM

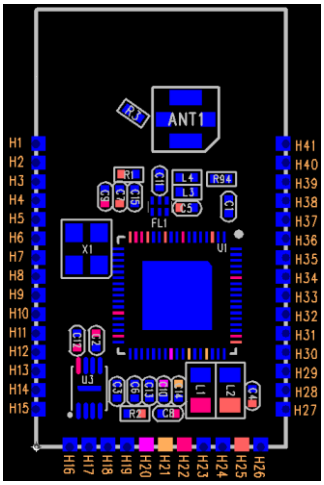


Figure 1-2

TABLE 1-1: VTBM-A01 **PIN DESCRIPTION**

PIN NO.	Pin TYP	Pin Name	Description
H1	P	GND	GND
H2	O	SPK_RN	Speaker output negative, right
H3	O	SPK_RP	Speaker output positive, right
H4	I	MIC_BN	Line input negative, channel B
H5	I	MIC_BP	Line input positive, channel B
H6	O	SPK_LN	Speaker output negative, left
H7	O	SPK_LP	Speaker output positive, left
H8	AIO	AIO[0]	Analog programmable input line 0.
H9	I/O	PIO[4]/I2S1_WS/SPI_CS#	Programmable input/output line 4./SPI_CS#/I2S1_WS
H10	I/O	PIO[16]/UART_RTS#	Programmable input/output line 16./UART_RTS
H11	I/O	PIO[3]/I2S1_SD_OUT/SPI_MISO	Programmable input/output line 3./SPI_MISO/I2S1_SD_OUT
H12	SPI_MOSI	SPI_MOSI	SPI_MOSI: Debug SPI data input
H13	I/O	PIO[17]/UART_CTS#	Programmable input/output line 17./UART_CTS
H14	I/O	PIO[5]/I2S1_SCK_SPI_CLK	Programmable input/output line 5./SPI_CLK/I2S1_SCK
H15	P	GND	GND
H16	I	RST	Reset if low. Pull low for minimum 5 ms to cause a reset.
H17	O	LED[1]	Open-drain output
H18	O	LED[0]	Open-drain output
H19	P	VREGENABLE	Regulator enable and multifunction button. A high input (tolerant to VBAT voltages) enables the on-chip regulators, which can then be latched on internally and the button used as a multifunction input.
H20	P	VCHG	Charger input.
H21	P	VBAT	Battery positive terminal.
H22	P	SMPS_1.8V	1.8V switch-mode power regulator output
H23	P	CHG_EXT	External battery charger transistor base control when using external charger boost. Otherwise leave unconnected
H24	I	VBAT_SENSE	Battery charger sense input.
H25	P	SMPS_1.35V	1.35V switch-mode power regulator output
H26	P	GND	GND
H27	P	GND	GND
H28	USB_N	USB_N	USB data minus
H29	USB_P	USB_P	USB data plus
H30	I/O	PIO[7]/I2S2_WS	Programmable input/output line 7./I2S2_WS
H31	I/O	PIO[9]/I2S2_SCK/UART_CTS#	Programmable input/output line 9./UART_CTS
H32	I/O	PIO[0]/UART_RX	Programmable input/output line 0./UART_RX
H33	I/O	PIO[1]/UART_TX	Programmable input/output line 1./UART_TX
H34	I/O	PIO[8]/I2S2_SD_IN/UART_RTS#	Programmable input/output line 8./UART_RTS
H35	I/O	PIO[6]/I2S2_SD_OUT	Programmable input/output line 6./I2S2_SD_OUT
H36	I/O	PIO[21]	Programmable input/output line 21.

H37	I/O	PIO[18]	Programmable input/output line 18.
H38	O	LED[2]	Open-drain output
H39	I	MIC_AN	Line or microphone input negative, channel A
H40	I	MIC_AP	Line or microphone input positive, channel A
H41	I	MIC_BIAS	Microphone bias

- I: input pin
- O: Output pin
- I/O: Input/Output pin
- P: Power pin

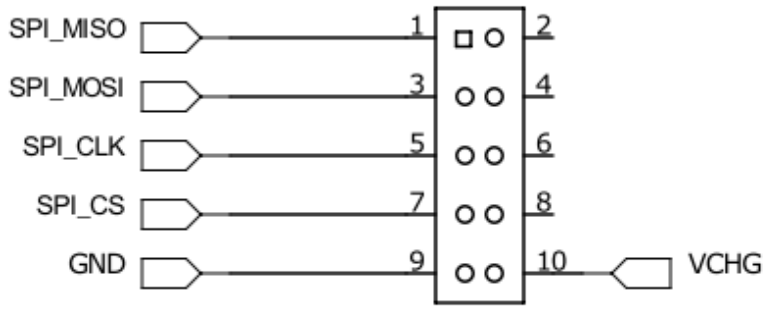


FIGURE 1-3:External Programming Header Connections

Configuration and firmware programming modes are entered according to the system configuration I/O pins as shown in the figure above.

2 Bluetooth modem

The Bluetooth modem includes the following components:

- RF ports
- RF receiver
- RF transmitter
- Bluetooth radio synthesizer
- Baseband

2.1 RF ports (BT-RF)

VTBM-A01 BT Module contains a balun that combines the balanced outputs of the PA on transmit and produces the balanced input signals for the LNA required on receive.

2.2 RF receiver

The receiver features a near-zero IF architecture that enables the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input enables the receiver to operate close to GSM and WCDMA cellular phone transmitters without being desensitized. A digital FSK discriminator means that no discriminator tank is needed and its

excellent performance in the presence of noise enables VTBM-A01 BT Module to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

2.3 RF transmitter

2.3.1 IQ modulator

The transmitter features a direct IQ modulator to minimize frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

2.3.2 Power amplifier

The internal PA output power is software controlled and configured through a PS Key. The internal PA on the VTBM-A01 BT Module has a maximum output power that enables it to operate as an up to Class 1 Bluetooth radio without requiring an external RF PA.

2.3 Bluetooth radio synthesizer

The Bluetooth radio synthesizer is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators, or loop filter. The synthesizer is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v5.0 specification.

2.4 Baseband

The baseband handles the digital functions of the Bluetooth modem, for example the Burst Mode Controller and Physical Layer Hardware Engine.

3.0 Clock generation

3.1 Crystal calibration

Crystal calibration uses a single measurement of RF output frequency and can be performed quickly as part of the product final test. Typically, a TXSTART radio command is sent and then a measurement of the output RF frequency is read. From this process, the calibration factor to correct actual offset from the intended frequency can be calculated. This offset value is stored in PSKEY_ANA_FTRIM_OFFSET. VTBM-A01 BT Module then compensates for the initial frequency offset of the crystal.

The value in PSKEY_ANA_FTRIM_OFFSET is a 16-bit two's complement signed integer that specifies the fractional part of the ratio between the true crystal frequency, factual, and the value set in PSKEY_ANA_FREQ, $f_{nominal}$.

PSKEY_ANA_FTRIM_OFFSET = (factual / fnominal – 1) ×2^20

For more information on TXSTART radio test, see the Blue Test User Guide.

4 Serial Quad I/O Flash

The VTBM-A01 BT Module uses external serial flash ICs for storage of:

- Device-specific data
- Application
- Libraries
- Voice prompt files
- Proprietary data

The VTBM-A01 BT Module supports a 8MB 4‑bit I/O flash.

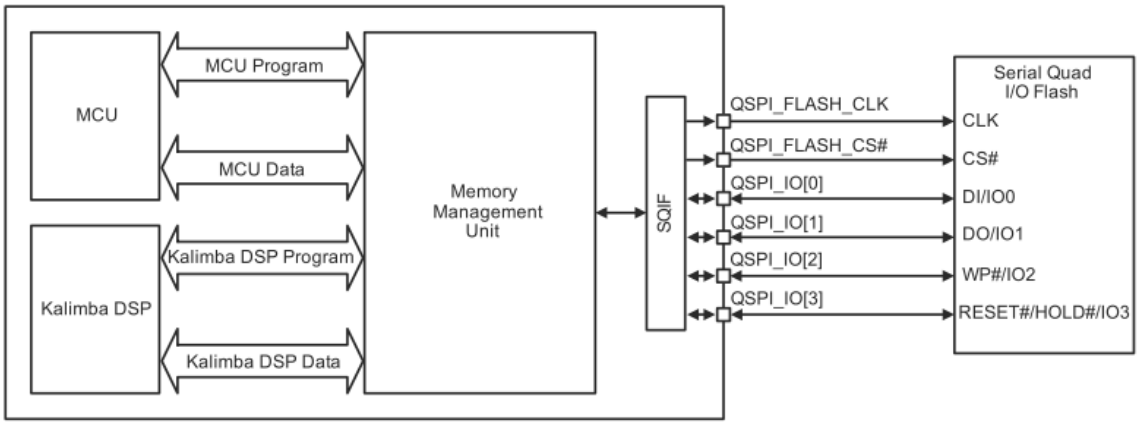


Figure 4-1 Typical connection between the QCC3008 QFN and a serial flash IC

5 Serial interfaces

5.1 USB interface

VTBM-A01 BT Module has a full-speed (12 Mbps) USB interface for communicating with other compatible digital devices. The USB interface on VTBM-A01 BT Module acts as a USB peripheral, responding to requests from a master host controller.

VTBM-A01 BT Module contains internal USB termination resistors and requires no external resistors.

VTBM-A01 BT Module supports the Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification), supports USB standard charger detection, and fully supports the USB Battery Charging Specification v1.2.

5.2 UART interface

VTBM-A01 BT Module has a UART serial interface that provides a simple mechanism for communicating with other serial devices using the RS232 protocol, including for test and debug. The UART interface is multiplexed with PIOs and other functions, and hardware flow control is optional.

Table 5-1 PS Keys for UART/PIO multiplexing

PS Key	PIO location option

PSKEY_UART_RX_PIO	PIO[0]
PSKEY_UART_TX_PIO	PIO[1]
PSKEY_UART_RTS_PIO	PIO[8] (default) or PIO[16]
PSKEY_UART_CTS_PIO	PIO[9] (default) or PIO[17]

Figure 5-1 shows the 4 signals that implement the UART function.

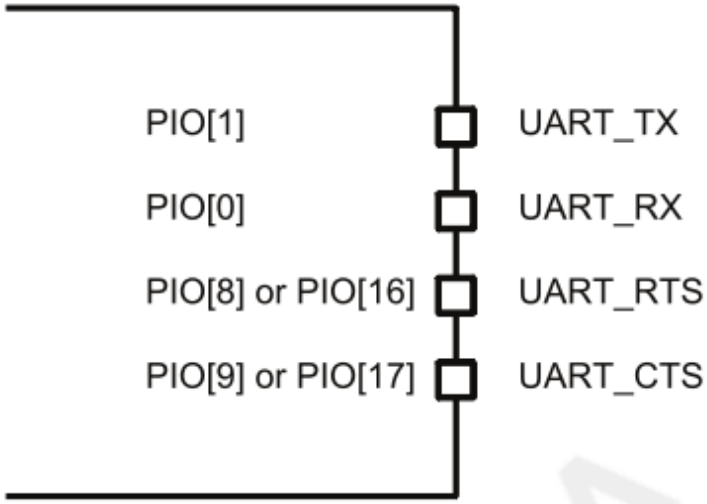


Figure 5-1 Universal asynchronous receiver

When VTBM-A01 BT Module is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. The remaining 2 signals, UART_CTS and UART_RTS, implement optional RS232 hardware flow control where both are active low indicators.

UART configuration parameters, such as baud rate and packet format, are set via using the VTBM-A01 BT Module firmware.

NOTE To communicate with the UART at its maximum data rate using a standard PC, the PC requires an accelerated serial port adapter card.The use of UART and USB are mutually exclusive.

Table 5-2 Possible UART settings

Parameter		**Possible values**
Baud rate	Minimum	1200 baud (≤ 2% Error)
		9600 baud (≤ 1% Error)
	Maximum	4 M baud (≤ 1% Error)
Flow control		RTS/CTS or None

Parity	None, Odd or Even
Number of stop bits	1 or 2
Bits per byte	8

Table 5-3 lists common baud rates and their associated error values for PSKEY_UART_BITRATE. To set the UART baud rate, load PSKEY_UART_BITRATE with the number of bits per second.

Table 5-3 Standard baud rates

Baud rate	PS Key value (bits per second)	Error
1200	1200	1.73%
2400	2400	1.73%
4800	4800	1.73%
9600	9600	-0.82%
19200	19200	0.45%
38400	38400	-0.18%
57600	57600	0.03%
76800	76800	0.14%
115200	115200	0.03%
230400	230400	0.03%
460800	460800	-0.02%
921600	921600	0.00%
1382400	1382400	-0.01%
1843200	1843200	0.00%
2764800	2764800	0.00%
3686400	3686400	0.00%

5.3 SPI interface

VTBM-A01 BT Module provides a debug SPI interface for programming, configuring, and debugging the VTBM-A01 BT Module.

Access to this interface is required in production. Ensure the 4 SPI signals are brought out to either test points or a header. Use the SPI interface. QTIL provides development and production tools to communicate over the SPI from a PC, although a level translator circuit is often required. All are available from QTIL.

5.4 I²C interface

The VTBM-A01 BT Module supports an I²C interface for I/O port expansion. The default assignment of the I²C interface onto the PIOs on the VTBM-A01 BT Module is:

- PIO [0] is the I²C interface SCL line (AMP_I2C_SCL)
- PIO [0] is the I²C interface SCL line (AMP_I2C_SCL)

Alternatively, the I²C interface can be assigned to two PIOs from PIO [9:0] using PSKEY_I2C_SCL_PIO and PSKEY_I2C_SDA_PIO.

NOTE The I²C interface requires external pull-up resistors. Ensure that external pull-up resistors are suitably sized for the I²C interface speed and PCB track capacitance.

6 Interfaces

6.1 Programmable I/O ports (PIO)

VTBM-A01 BT Module provides up to 14 lines of programmable bidirectional I/O, PIO[0:9,16:18,21].

Table 6-1 Alternative PIO functions

PIO	Function				
	Debug SPI	UART	I²C	I²S	SPDIF
PIO[0]	-	UART_RX	AMP_I2C_SCL(default)	-	-
PIO[1]	-	UART_TX	AMP_I2C_SDA(default)	-	-
PIO[2]	SPI_MOSI	-	Alternate I²Cfunction	I2S1_SD_IN	SPDIF_IN
PIO[3]	SPI_MISO	-	Alternate I²Cfunction	I2S1_SD_OUT	-
PIO[4]	SPI_CS#	-	Alternate I²Cfunction	I2S1_WS	-
PIO[5]	SPI_CLK	-	Alternate I²Cfunction	I2S1_SCK	-
PIO[6]	-	-	Alternate I²Cfunction	I2S2_SD_OUT	-
PIO[7]	-	-	Alternate I²Cfunction	I2S2_WS	-
PIO[8]	-	UART_RTS	Alternate I²Cfunction	I2S2_SD_IN: I2S2 synchronous data input	-
PIO[9]	-	UART_CTS	Alternate I²Cfunction	2S2_SD_IN	
PIO[16]	-	UART_RTS	-	-	-
PIO[17]	-	UART_CTS	-	-	-
PIO[18]	-	-	-	-	-
PIO[21]	-	-	-	-	-

6.2 Analog I/O ports (AIO)

VTBM-A01 BT Module has one general-purpose analog interface pin, AIO [0]. Typically, this pin connects to a thermistor for battery pack temperature measurements during charging.

6.3 LED drivers

VTBM-A01 BT Module includes a 3-pad PWM LED driver for driving RGB LEDs for producing a wide range of colors. All LEDs are controlled by application.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.

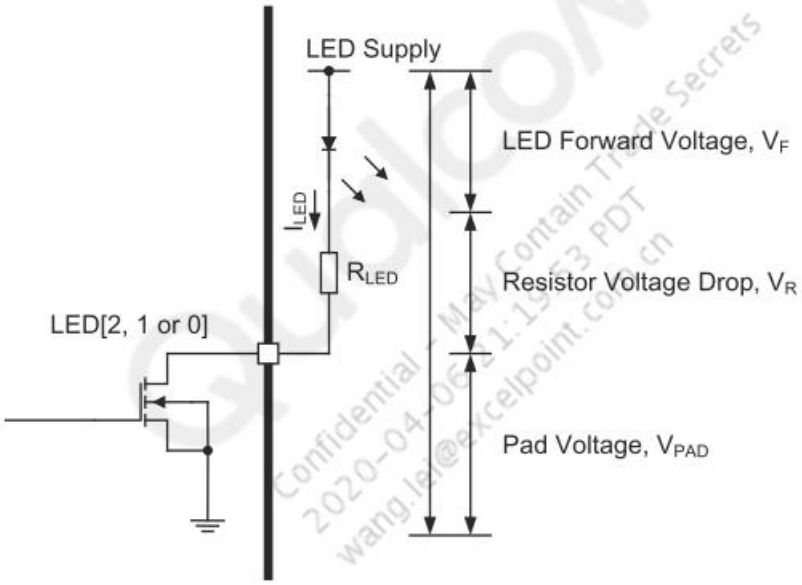


Figure 6-1 LED equivalent circuit

From Figure 6-1 it is possible to derive Equation 6-1 to calculate ILED. If a known value of current is required through the LED to give a specific luminous intensity, then the value of RLED is calculated.

I_{LED} =(VDD-V_F)/(R_{LED}+R_{PAD})

NOTE The supply domain for LED [2:0], must remain powered for LED functions to operate.

7 Audio interface

The audio interface circuit consists of the following components:

- Dual analog audio inputs
- Dual analog audio outputs
- 1 digital microphone input
- 2 configurable I²S interfaces
- Configurable SPDIF input interface

Figure 7-1 shows the functional blocks of the audio interface. The codec supports stereo/dual-mono playback and recording of audio signals at multiple sample rates with a 16-bit resolution. The ADC and the DAC of the codec each contain two independent high-quality channels. Each ADC or DAC channel runs at its own

independent sample rate.

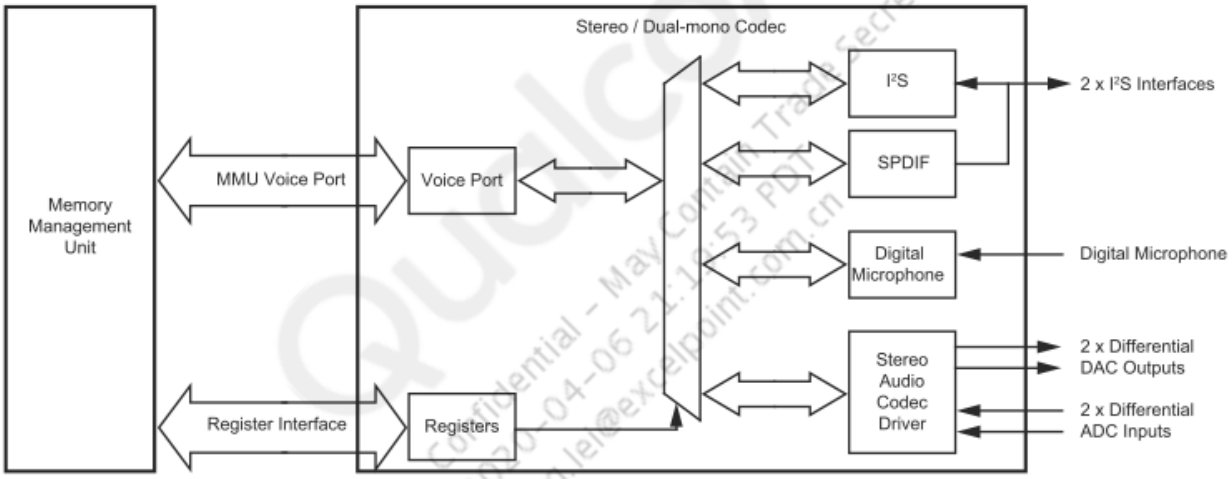


Figure 7-1 VTBM-01 BT Module audio interface

7.1 Audio input and output

The audio input circuitry consists of 2 independent 16-bit high-quality ADC channels:

- Programmable as either stereo or dual-mono inputs.
- 1 input programmable as either microphone or line input, the other as line input only.
- Each channel can be connected as either single-ended or fully differential.
- Each channel has an analog and digital programmable gain stage.

The audio output circuitry consists of a dual differential class A-B output stage.

NOTE VTBM-A01 BT module is designed for a differential audio output. If a single-ended audio output is required, use an external differential to single-ended converter.

7.2 Audio codec interface

The interface has the following features:

- Stereo and mono analog input for voice band and audio band
- Stereo and mono analog output for voice band and audio band

NOTE To avoid any confusion regarding stereo operation, this data sheet explicitly states which is the left and right channel for audio output. Regarding audio input, software, and any registers, channel 0 or channel A

represents the left channel and channel 1 or channel B represents the right channel.

7.2.1 Audio codec block diagram

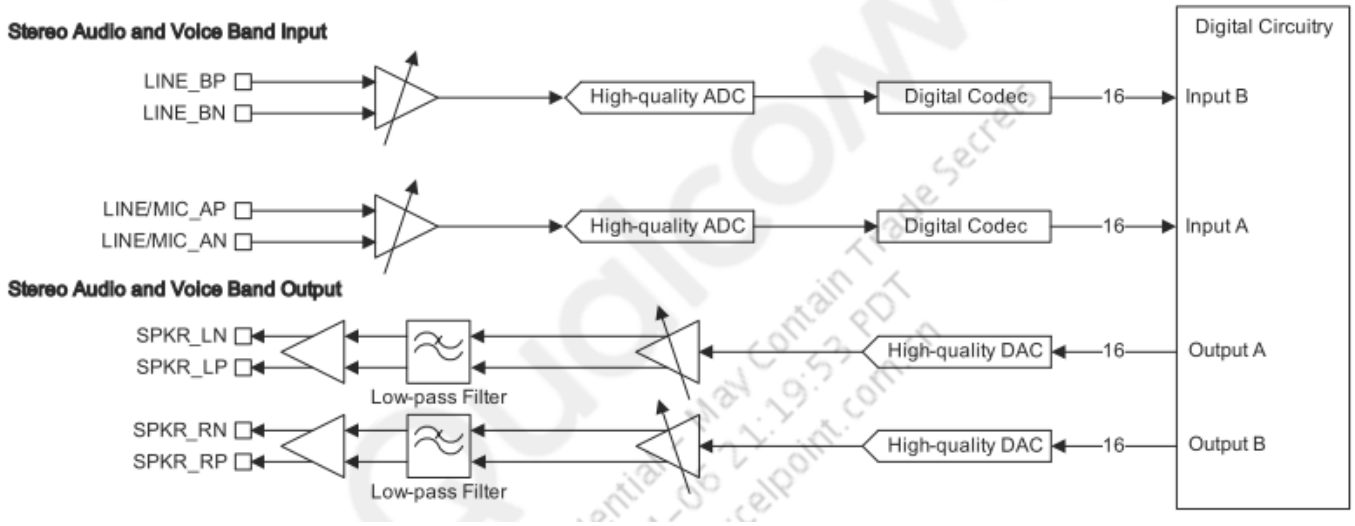


Figure 7-2 Audio codec input and output stages

The VTBM-A01 BT Module audio codec uses a fully differential architecture in the analog signal path. This architecture results in low common-mode-noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a dual power supply, VDD_AUDIO for the audio circuits and VDD_AUDIO_DRV for the audio driver circuits.

7.2.2 ADC

The VTBM-A01 BT Module consists of two high-quality ADCs:

- Each ADC has a second-order Sigma-Delta converter.
- Each ADC is a separate channel with identical functionality.
- Each channel has an analog and a digital gain stage.

7.2.2.1 ADC sample rate selection

Each ADC supports the following predefined sample rates:

- 8 kHz
- 11.025 kHz

- 16 kHz
- 22.050 kHz
- 24 kHz
- 32 kHz
- 44.1 kHz
- 48 kHz

7.2.2.2 ADC audio input gain

The VTBM-A01 BT Module audio input gain consists of the following components:

- An analog gain stage based on a pre-amplifier and an analog gain amplifier
- A digital gain stage

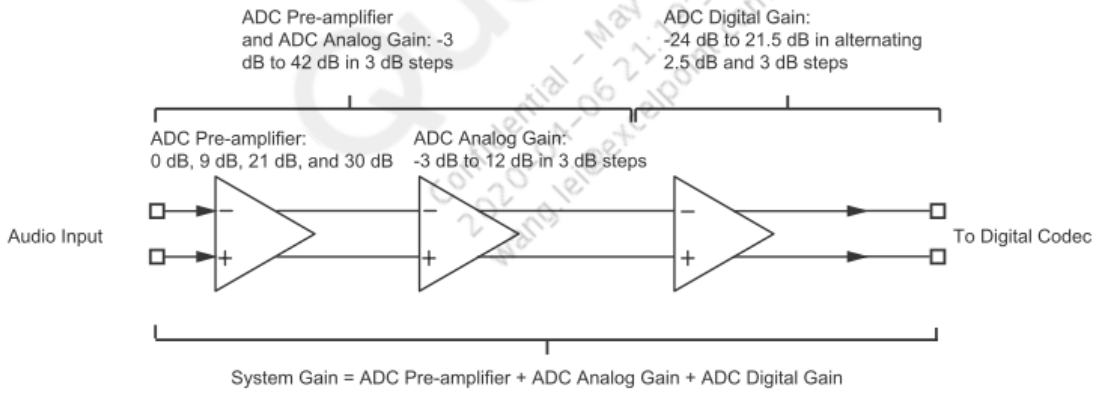


Figure 7-3 Audio input gain

7.2.2.3 ADC pre-amplifier and analog/digital gain

The gain of the ADC inputs can be configured in the range of -27 dB to 63.5 dB steps, making it suitable for line and microphone input levels. 0 dB is 1600 mV pk-pk input.

The ADC input impedance is nominal 6 kΩ except when 0 dB pre-amplifier gain is selected when it becomes 12 kΩ.

If the input pre-amplifier is disabled, the input impedance varies between 6 kΩ and 34 kΩ, depending on gain selection. In normal operation, the input pre-amplifier is enabled.

Calls connected by the VM stream automatically select the distribution of gain within the ADC for best performance. Alternatively, the individual gain stages can be set.

7.2.2.4 ADC digital gain

Table 7-1 lists how the ADC digital gain selection values map to digital gain settings.

Digital gain selection value	ADC digital gain setting (dB)	Digital gain selection value	ADC digital gain setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

7.2.2.5 ADC digital IIR filte

The ADC contains 2 integrated anti-aliasing filters:

- A long IIR filter suitable for music (> 44.1 kHz).
- G.722 filter . This is a digital IIR filter that improves the stop-band attenuation required for G.722 compliance. This filter is the best selection for 8 kHz/16 kHz/voice.

7.2.3 DAC

The DAC consists of two high-quality DACs

- Each DAC has a fourth-order Sigma-Delta converter.
- Each DAC is a separate channel with identical functionality.
- Each channel has an analog and a digital gain stage.

7.2.3.1 DAC sample rate selectio

Each DAC supports the following sample rates:

- 8 kHz
- 11.025 kHz
- 16 kHz
- 22.050 kHz

- 32 kHz
- 40 kHz
- 44.1 kHz
- 48 kHz

7.2.3.2 DAC gain

The DAC outputs have two gain stages, a digital stage followed by an analog stage. The digital gain varies between -24 dB and 21.5 dB and the analog gain between -21 dB and 0 dB, giving a total range of -45 dB to 21.5 dB.

Calls connected by the VM stream automatically select the distribution of gain within the DAC for best performance. Alternatively, the individual gain stages can be set.

Table 7-2 DAC digital gain selection

Digital gain selection value	ADC digital gain setting (dB)	Digital gain selection value	ADC digital gain setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 7-3 DAC analog gain selection

Analog gain selection value	**DAC analog gain setting (dB)**	**Analog gain selection value**	**DAC analog gain setting (dB)**
7	0	3	-12
6	-3	2	-15
5	-6	1	-18
4	-9	0	-21

7.2.3.3 DAC digital FIR filte

The DAC contains an integrated digital FIR filter with the following modes:

- A default long FIR filter for best performance at ≥ 44.1 kHz.
- A short FIR to reduce latency.
- A narrow FIR (a sharp roll-off at Nyquist) for G.722 compliance. Best for 8 kHz/16 kHz.

7.2.4 Microphone bias generator

VTBM-A01 BT Module contains an independent low-noise microphone bias generator. The microphone bias generator is recommended for biasing electret condensor microphones.

Figure 7-4 shows a typical biasing circuit for electret condenser microphones.

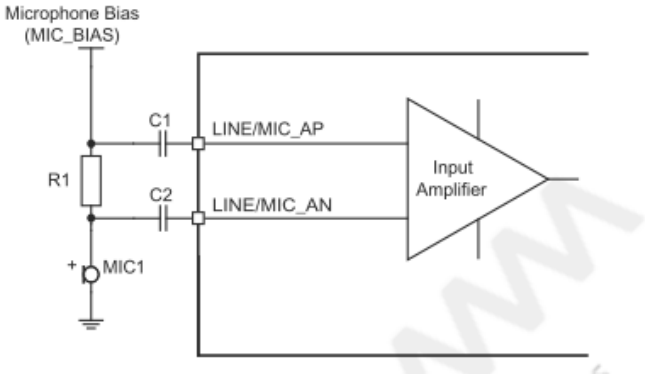


Figure 7-4 Microphone biasing

The microphone bias generator provides a selectable output voltage of 1.8 V or 2.6 V nominal and derives its power from VBAT or VOUT_3V3. No output capacitor is required.

The bias resistor R1 should match the microphone load impedance, and typically is 2.2 kΩ. C1 and C2 are typically 100/150 nF to give a bass roll-off to limit wind noise on the microphone.

The mic bias generator has a maximum drop out of 300 mV, if VBAT drops below (selected output voltage – drop out voltage), the output voltage will fall below specification. The generator will continue to operate but noise performance will be impaired.

7.2.5 Line input

Figure 7-5 and Figure 7-6 show 2 circuits for line input operation and show connections for either differential or single-ended inputs.

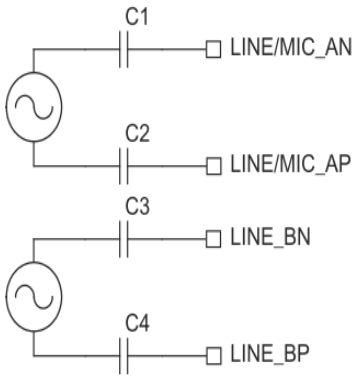


Figure 7-5 Differential input

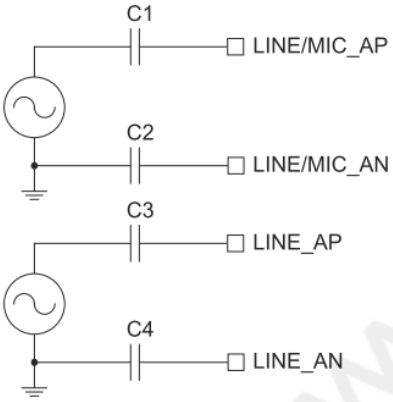


Figure 7-6 Single-ended input

7.2.6 Output stage

The output stage digital circuitry converts the signal from 16 bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analog output circuitry.

The analog output circuit comprises a DAC, a buffer with gain-setting, a low pass filter, and a class AB output stage amplifier.

Figure 7-7 shows that the output is available as a differential signal between SPKR_LN and SPKR_LP for the left channel, and between SPKR_RN and SPKR_RP for the right channel.

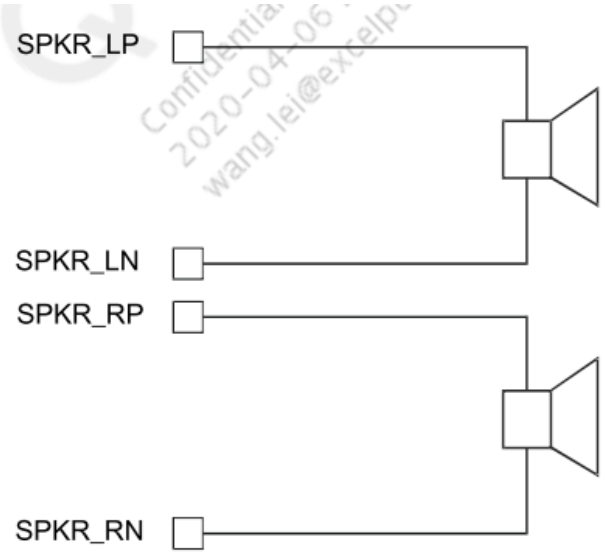


Figure 7-7 Speaker output

7.2.7 Mono operation

Mono operation is a single-channel operation of the stereo codec. The left channel represents the single mono channel for audio in and audio out. In mono operation, the right channel is the auxiliary mono channel for dual-mono channel operation. In single channel mono operation, disable the other channel to reduce power consumption.

7.2.8 Sidetone

In some applications, it is necessary to implement sidetone. This sidetone function applies configurable gain to the microphone signal and feeds it into the DAC stream. The sidetone routing selects the version of the microphone signal from before or after the digital gain in the ADC interface and adds it to the output signal before or after the digital gain of the DAC interface, see Figure 7-8.

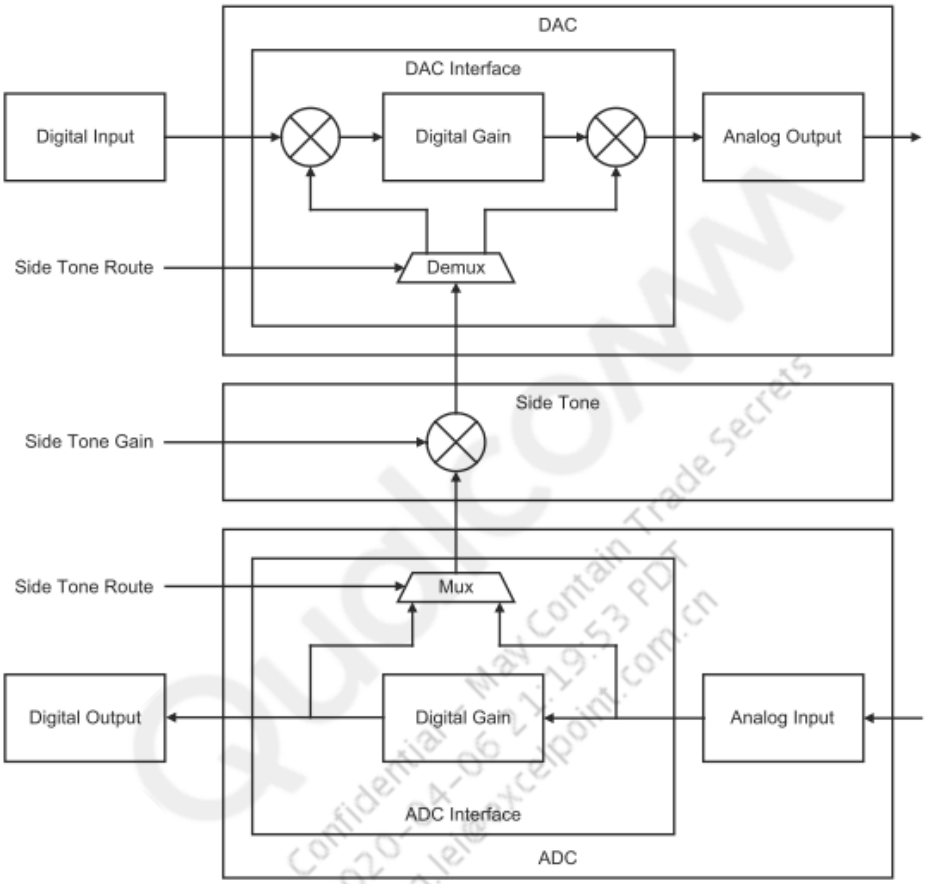


Figure 7-8 Sidetone

The ADC provides simple gain to the sidetone data. The gain values range from -32.6 dB to 12.0 dB in alternating steps of 2.5 dB and 3.5 dB, see Table 7-4.

Table 7-4 Sidetone gain

Value	Sidetone gain	Value	Sidetone gain
0	-32.6 dB	8	-8.5 dB
1	-30.1 dB	9	-6.0 dB
2	-26.6 dB	10	-2.5 dB
3	-24.1 dB	11	0 dB
4	-20.6 dB	12	3.5 dB
5	-18.1 dB	13	6.0 dB

6	-14.5 dB	14	9.5 dB
7	-12.0 dB	15	12.0 dB

7.3 I²S1 and I²S2 interface

VTBM-A01 BT Module supports I²S input and output via its two industry-standard I²S digital audio interfaces, left-justified or right-justified.

NOTE In this section, terms are defined as follows:

- I²S refers to the I²S1 and I²S2 interfaces.
- SD_IN refers to I2S1_SD_IN or I2S2_SD_IN.
- SD_OUT refers to I2S1_SD_OUT or I2S2_SD_OUT
- WS refers to I2S1_WS or I2S2_WS.
- SCK refers to I2S1_SCK or I2S2_SCK.

VTBM-A01 BT Module also supports several alternative PCM data formats.

I²S pin	PCM function
I2Sn_SD_IN	PCM_IN
I2Sn_SD_OUT	PCM_OUT
I2Sn_WS	PCM_SYNC
I2Sn_SCK	PCM_CLK

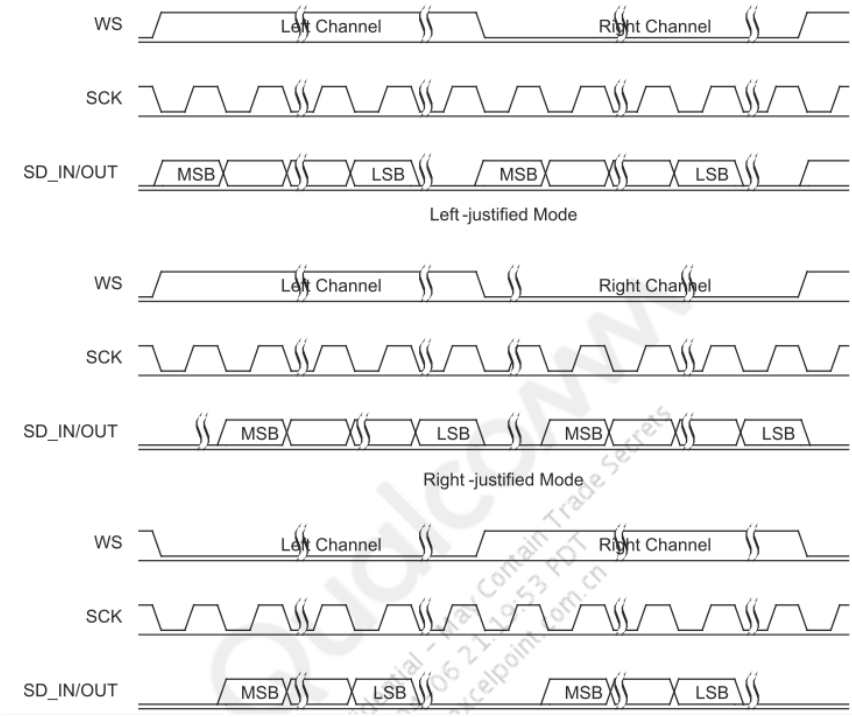


Figure 7-9 Digital audio interface modes

Table 7-5 Digital audio interface slave timing

Symbol	Parameter	Min	Typ	Max	Unit
–	SCK Frequency	–	–	6.2	MHz
–	WS Frequency	–	–	96	kHz
tch	SCK high time	80	–	–	ns
tcl	SCK low time	80	–	–	ns

Table 7-6 I²S slave mode timing

Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
tssu	WS valid to SCK high set-up time	20	–	–	ns
tsh	SCK high to WS invalid hold time	2.5	–	–	ns
topd	SCK low to SD_OUT invalid delay time	–	–	20	ns

Table 7-7 I²S slave mode timing (cont.)

Symbol	Parameter	Min	Typ	Max	Unit
tisu	SD_IN valid to SCK high set-up time	20	–	–	ns
tih	SCK high to SD_IN invalid hold time	2.5	–	–	ns

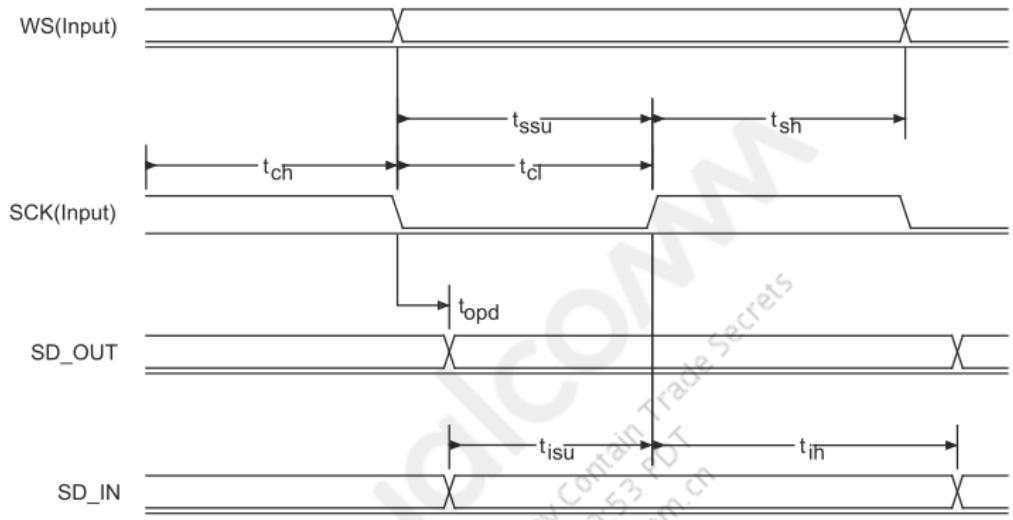


Figure 7-10 Digital audio interface slave timing

Table 7-8 Digital audio interface master timing

Symbol	Parameter	Min	Typ	Max	Unit
–	SCK Frequency	–	–	6.2	ns
–	WS Frequency	–	–	96	ns

Table 7-9 I²S master mode timing parameters, WS and SCK as outputs

Symbol	Parameter	Min	Typ	Max	Unit
tspd	SCK low to WS valid delay time	–	–	39.27	ns
topd	SCK low to WS valid delay time	–	–	18.44	ns

Table 7-10 I²S master mode timing parameters, WS and SCK as outputs (cont.)

Symbol	Parameter	Min	Typ	Max	Unit
tisu	SD_IN valid to SCK high set up time	18.44	–	–	ns
tih	SCK high to SD_IN invalid hold time	0	–	–	ns

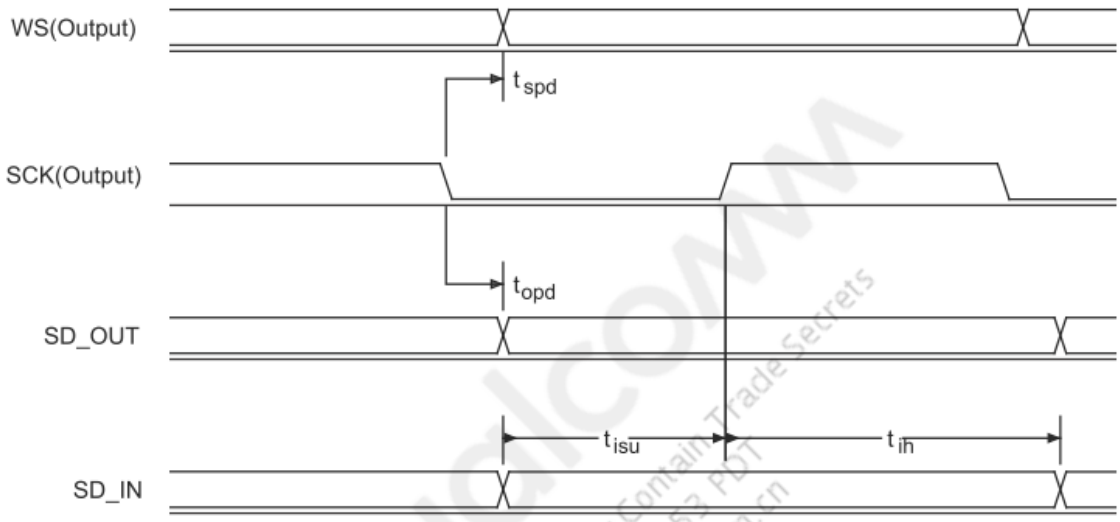


Figure 7-11 Digital audio interface master timing

8 Power control

8.1 Switch-mode regulators

For greater power efficiency, the VTBM-A01 BT Module contains 2 switch-mode regulators:

- One to generate a 1.8 V supply rail with an output current of 185 mA.
- One to generate a 1.35 V supply rail with an output current of 160 mA.
- Combining the 2 switch-mode regulators in parallel generates a single 1.8 V supply rail with an output current of 340 mA.

8.2 Reset, RST#

VTBM-A01 BT Module is reset from several sources:

- RST# pin
- Power-on reset
- USB charger attach reset
- Software configured watchdog timer

The RST# pin is an active low reset. Assert the reset signal for a period > 5 ms to ensure a full reset.At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are set to tristate.

NOTE Reset can also be triggered by a UART break symbol if:

- Host interface is any UART transport

And

- PSKEY_HOSTIO_UART_RESET_TIMEOUT is set to a value more than 1000 A reboot function is also available under software control.

9 Battery charger

The battery charger hardware is controlled by the on-chip application. The battery charger has 5 modes:

- Disabled
- Trickle charge
- Fast charge
- Standby: fully charged or float charge
- Error: charging input voltage, VCHG, is too low

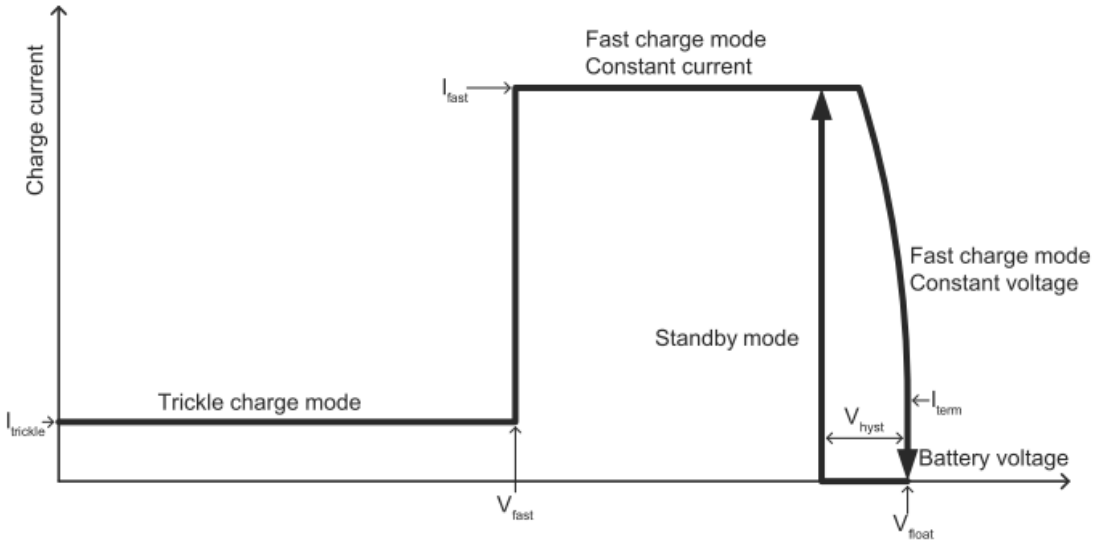
Transitions between the trickle charge, fast charge and standby modes are triggered by changes in battery voltageand charger current.

Table 10-1 Battery charger operating modes determined by battery voltage and charger current

Mode	Battery charger enabled	VBAT_SENSE
Disabled	No	X
Trickle charge	Yes	> 0 and < V_{fast}
Fast charge	Yes	> V_{fast} and < V_{float}
Standby	Yes	I_{term} and > (V_{float} - V_{hyst})
Error	Yes	> (VCHG - 50mV)

I_{term} is approximately 10% of I_{fast} for a given I_{fast} setting

Figure 9-1 shows the mode-to-mode transition voltages.



9.1 External mode

The external mode is for charging higher capacity batteries using an external pass device. The current is controlled by sinking a varying current into the CHG_EXT pin, and the current is determined by measuring the voltage drop across a resistor, Rsense, connected in series with the external pass device. The voltage drop is determined by looking at the difference between the VBAT_SENSE and VBAT pins. The charger regulates the current drawn from CHG_EXT pin to maintain nominal voltage drop of 200 mV across Rsense. The value of the external series resistor determines the charger current. This current can be trimmed with a PS Key.

Figure 9-2 shows R1 (220 mΩ) and C1 (4.7 µF) form a RC snubber that is required to maintain stability across all battery ESRs. The battery ESR must be < 1.0 Ω.

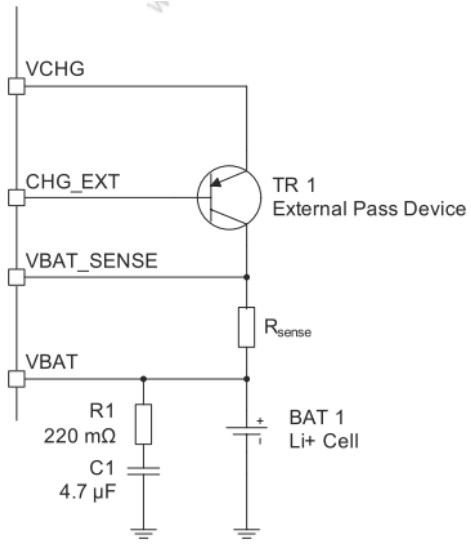


Figure 9-2 Battery charger external mode typical configuration

10 Electrical characteristic

10.1 Absolute maximum rating

Rating		Min	Max	Unit
Storage temperature		-40	105	℃
Supply voltage				
5 V (USB VBUS)	VCHG	-0.40	6.50	V
3.3V	VDD_USB	-0.40	3.60	V
Battery	LED[2:0]	-0.40	4.40	V
	SMP_VBAT	-0.40	4.40	V
	VBAT_SENSE	-0.40	4.40	V
	VREGENABLE	-0.40	4.40	V
PIO	PIO	-0.40	3.60	V

NOTE Voltage must not exceed 3.6 V on any I/O.

10.2 Recommended operating condition

Rating		Min	Typ	Max	Unit
Operating temperature range		-40	20	85	℃
5 V (USB VBUS)	VCHG, 4.20 V float setting	4.75 / 3.10	5.00	6.50	V
	VCHG, 4.35 V float setting	4.90 / 3.10	5.00	6.50	V
3.3 V	VDD_USB	3.10	3.30	3.60	V
Battery	LED[2:0]	–	3.70	4.40	V
	SMP_VBAT	2.50	3.70	4.40	V
	VBAT_SENSE	0	3.70	4.40	V
	VREGENABLE	0	3.70	4.40	V
PIO	PIO	1.70	1.80	3.60	V

10.3 Input/Output terminal characteristic

For all I/O terminal characteristics:

- Current drawn into a pin is defined as positive.
- Current supplied out of a pin is defined as negative.

10.3.1 LED driver pads

LED driver pads		Min	Typ	Max	Unit
Current, I_{PAD}	High impedance state	–	–	5	µA
	Current sink state	–	–	10	mA
LED pad voltage, V_{PAD}	I_{PAD} = 10 mA	–	–	0.55	V
V_{OL} output logic level low		–	0	–	V
V_{OH} output logic level high		–	0.8	–	V
V_{IL} input logic level low		–	0	–	V
V_{IH} input logic level high		–	0.8	–	V

NOTE LED output port is open-drain and requires a pull-up

10.4 Battery charger

Battery charger	Min	Typ	Max	Unit
Input voltage, VCHG, 4.20 V float setting	4.75/3.10	5.00	6.50	V
Input voltage, VCHG, 4.35 V float setting	4.90/3.10	5.00	6.,50	V

NOTE Reduced specification if VCHG - VBAT < 0.55 V. Full specification > 4.75 V.
Reduced specification if VCHG - VBAT < 0.55 V. Full specification > 4.90 V.

Trickle charge mode	Min	Typ	Max	Unit
Charge current Itrickle, as percentage of fast charge current	8	10	12	%
V_{fast} rising threshold	-	2.9	-	V

V_{fast} rising threshold trim step size	-	0.1	-	V
V_{fast} falling threshold	-	2.8	-	V

Fast charge mode		Min	Typ	Max	Unit
Charge current during constant current mode, I_{fast}	Maximum charge setting (VCHG - VBAT > 0.55 V)	194	200	206	mA
	Minimum charge setting (VCHG - VBAT > 0.55 V)	-	10	-	mA
Reduced headroom charge current, as a percentage of I_{fast}	(VCHG - VBAT < 0.55 V)	50-	-	100	%
Charge current step size		-	10	-	mA
Vfloat threshold, 4.20 V		4.16	4.20	4.24	V
Vfloat threshold, 4.35 V		4.31	4.35	4.39	V
Charge termination current I_{term}, as percentage of I_{fast}		7	10	20	%

Standby mode	Min	Typ	Max	Unit
Voltage hysteresis on VBAT, Vhyst	100	–	150	mV

Error charge mode	Min	Typ	Max	Unit
Headroom error falling threshold	–	50	–	mV

NOTE Headroom = VCHG – VBAT

External charge mode	Min	Typ	Max	Unit
Fast charge current, I_{fast}	200	–	500	mA
Control current into CHG_EXT	0	–	20	mA

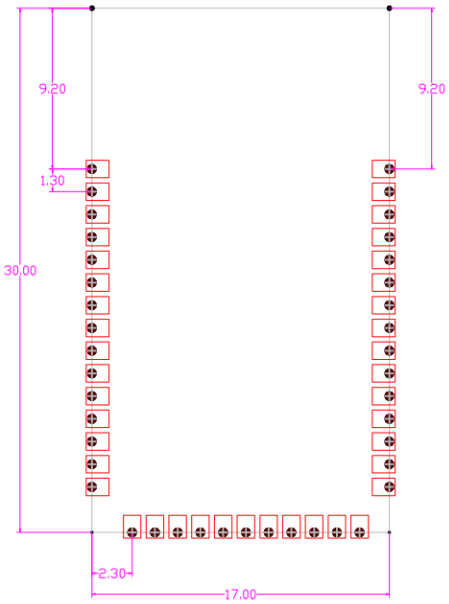
Voltage on CHG_EXT	0	–	6.50	V
External pass device h_{fe}	–	50	–	–
Sense voltage, between VBAT_SENSE and VBAT at maximum current	195	200	205	mV

NOTE In the external mode, the battery charger meets all the previous charger electrical characteristics and the additional or superseded electrical characteristics are listed in this table.

10.5 System current consumption

System Status	Typ.	Max.	Unit
System Off Mode	300	500	uA
Standby Mode	6.5	8	mA
Linked Mode	15	17	mA

11 Physical outline (unit mm)

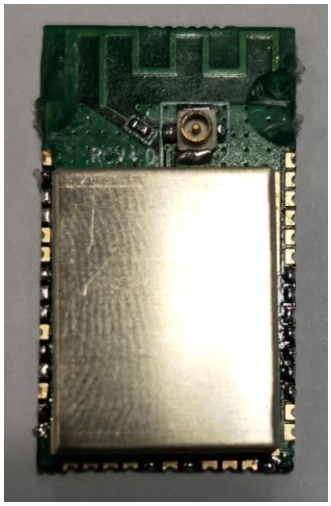


Top View

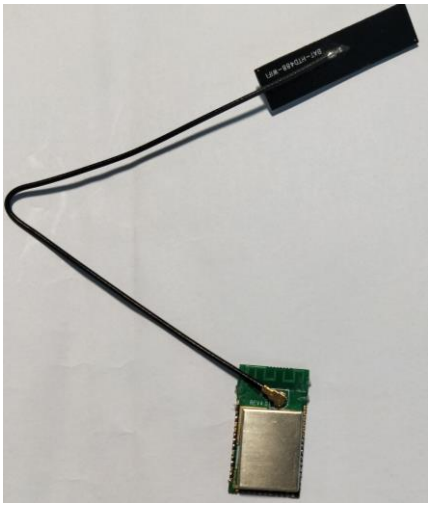
Side View

12 Module photo

Top View (PCB Ant Version)



Top View (External Ant Version)



13 Recommended Reflow Profile