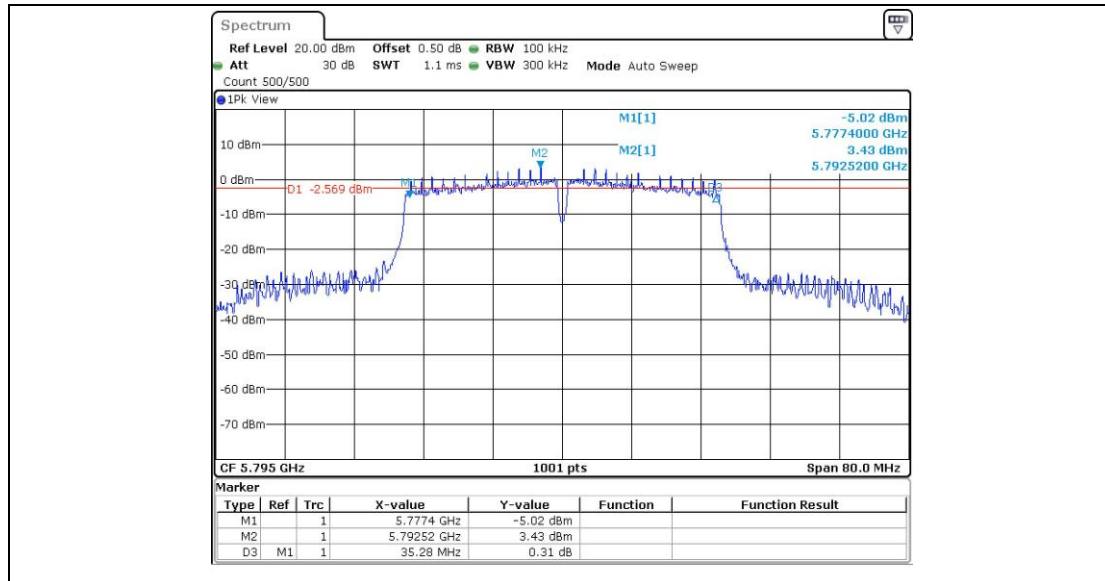
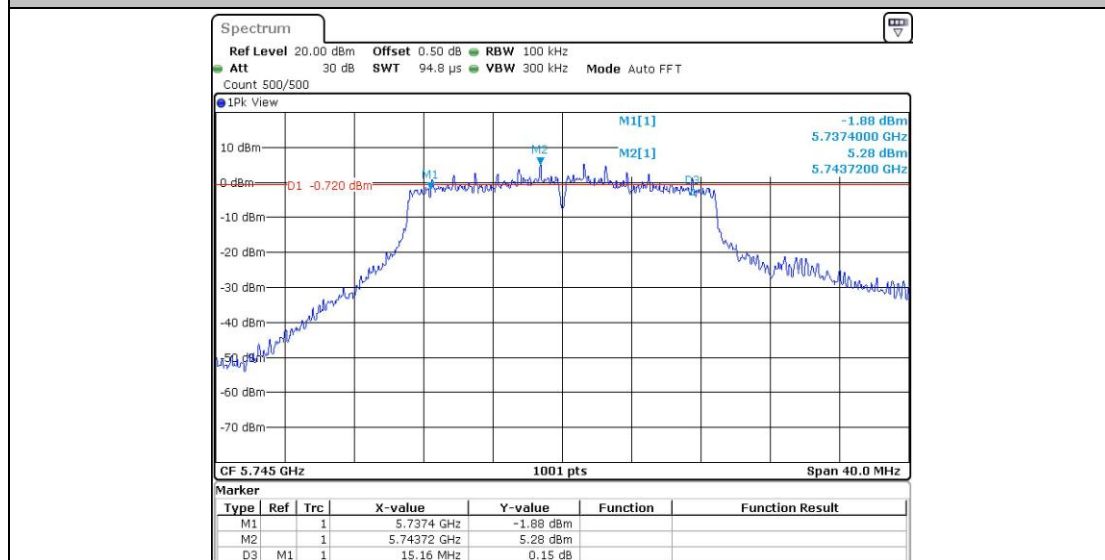
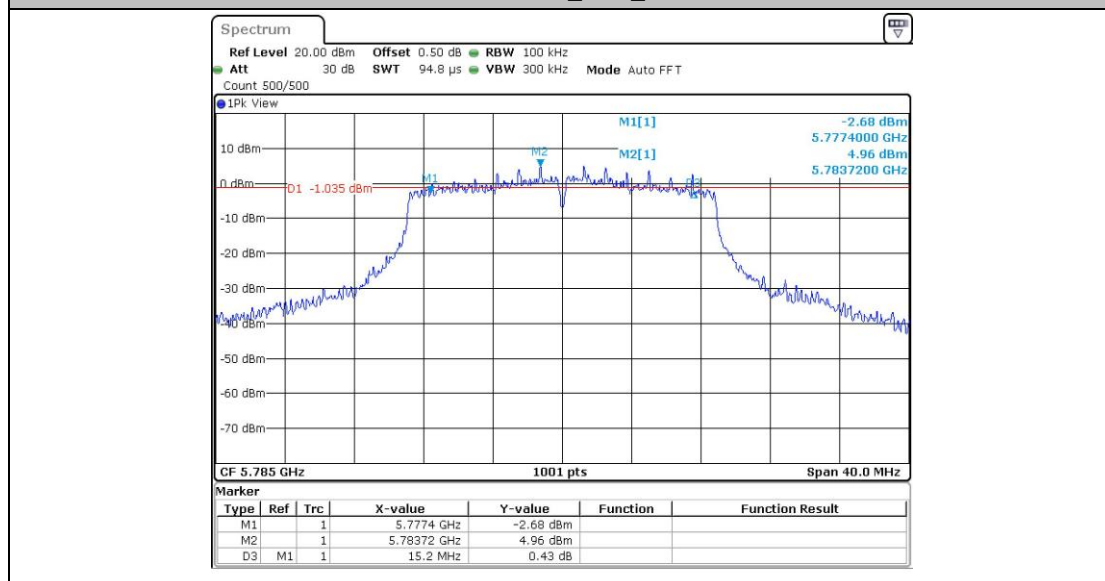




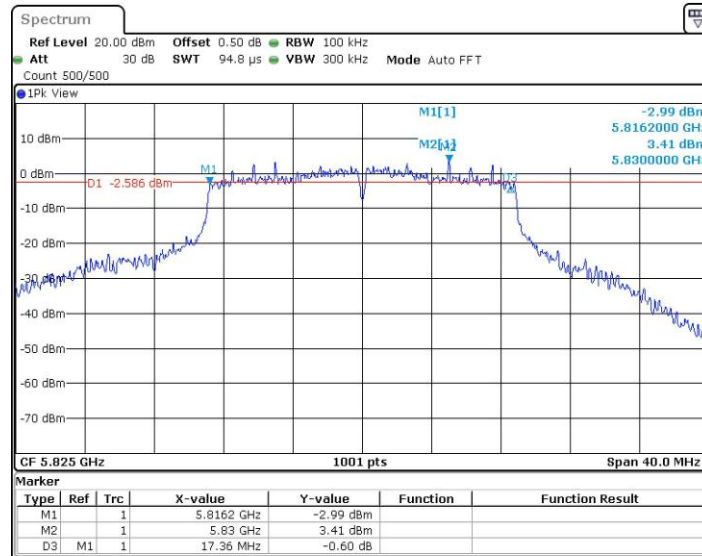
11N40SISO_Ant1_5795



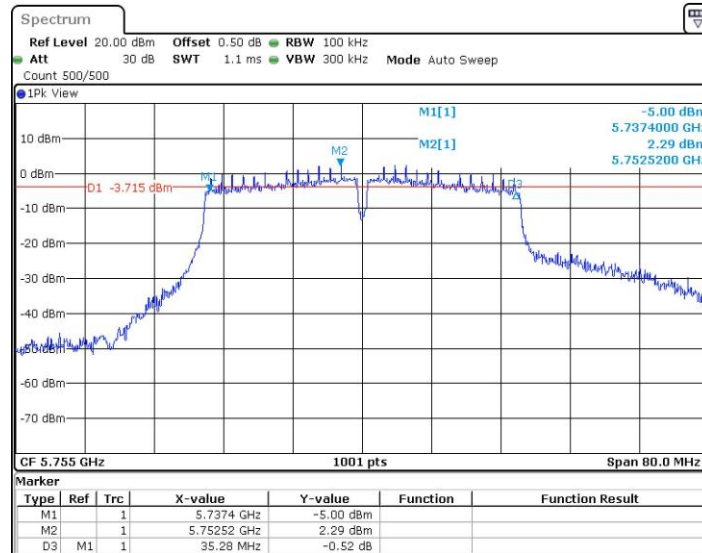
11AC20SISO_Ant1_5745



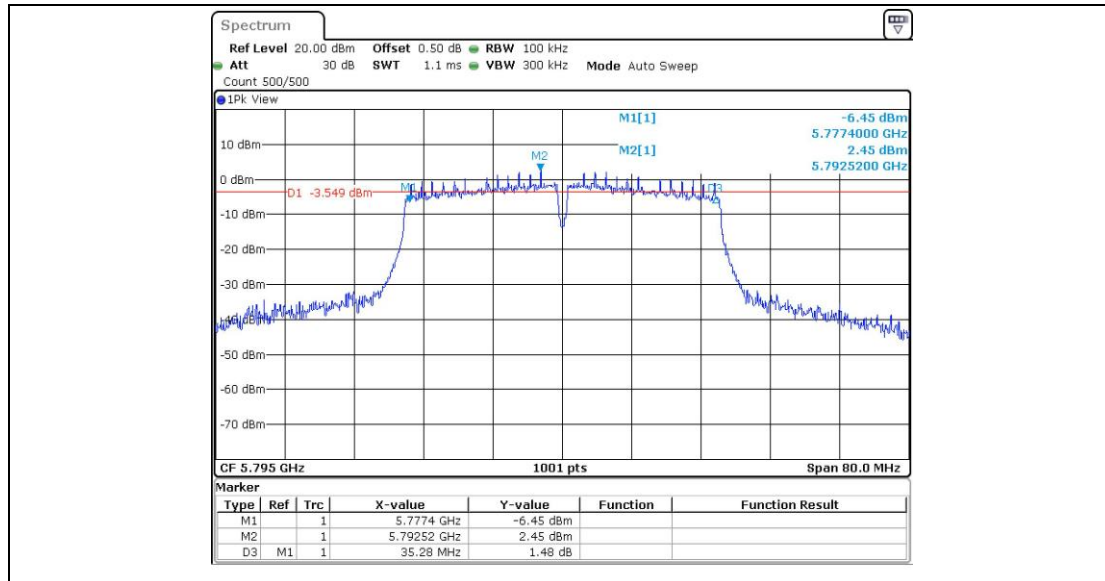
11AC20SISO_Ant1_5785



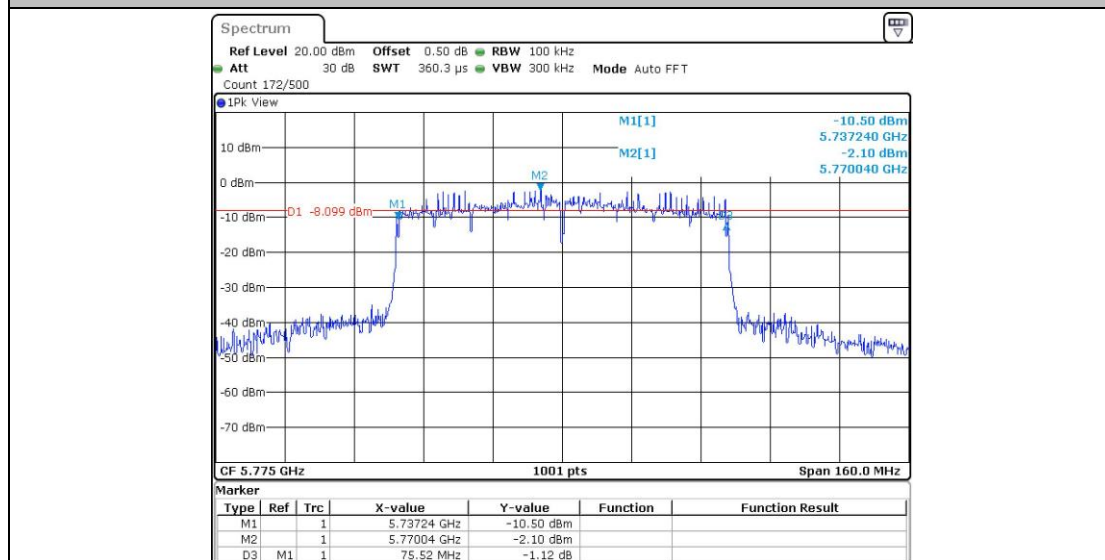
11AC20SISO_Ant1_5825



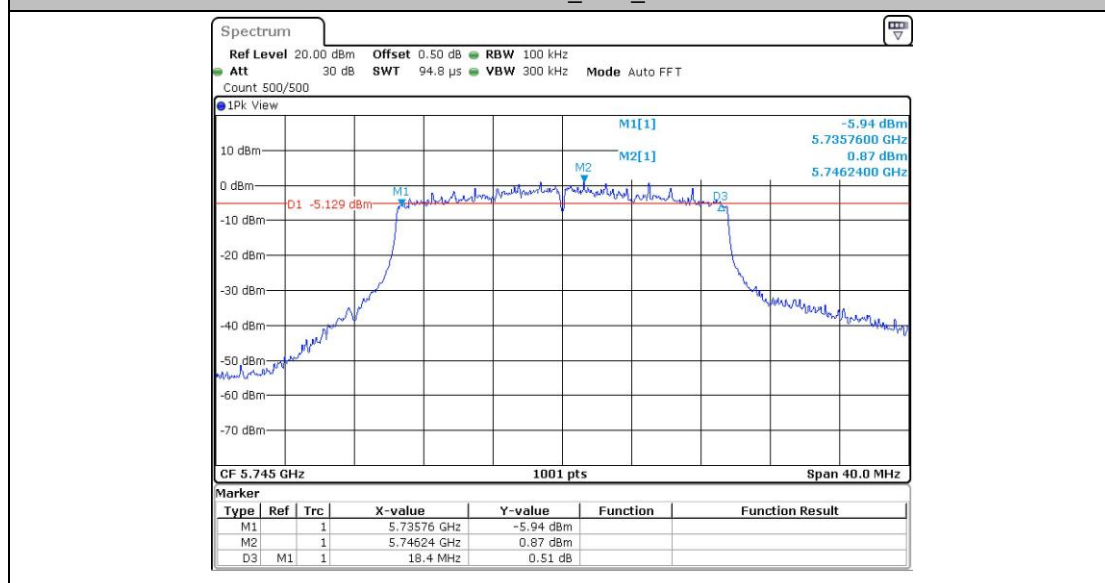
11AC40SISO_Ant1_5755



11AC40SISO_Ant1_5795



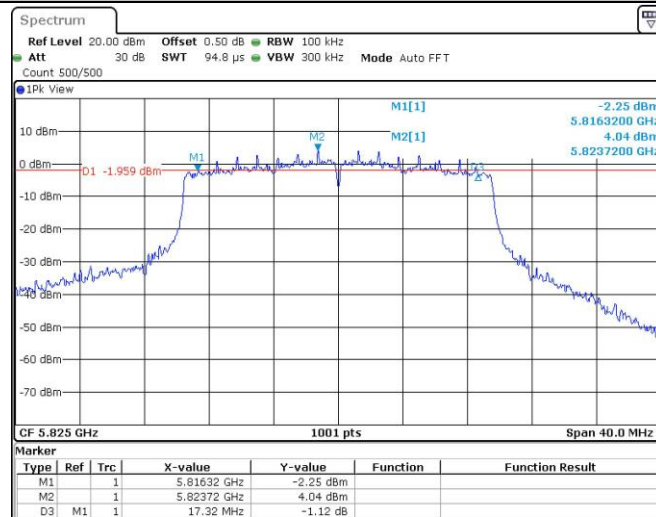
11AC80SISO_Ant1_5775



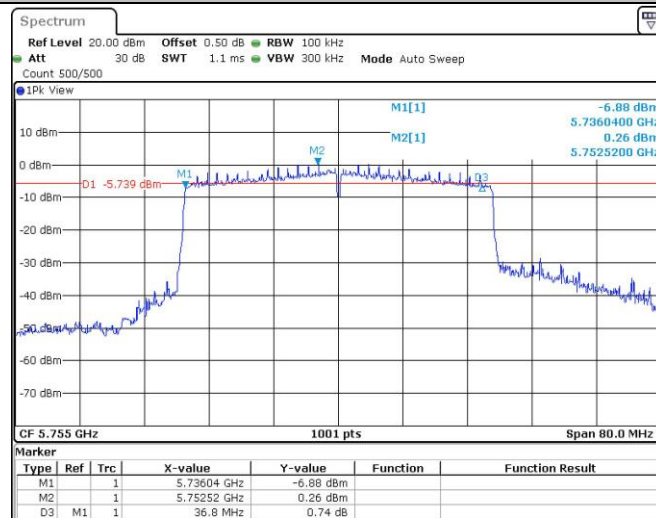
11AX20SISO_Ant1_5745



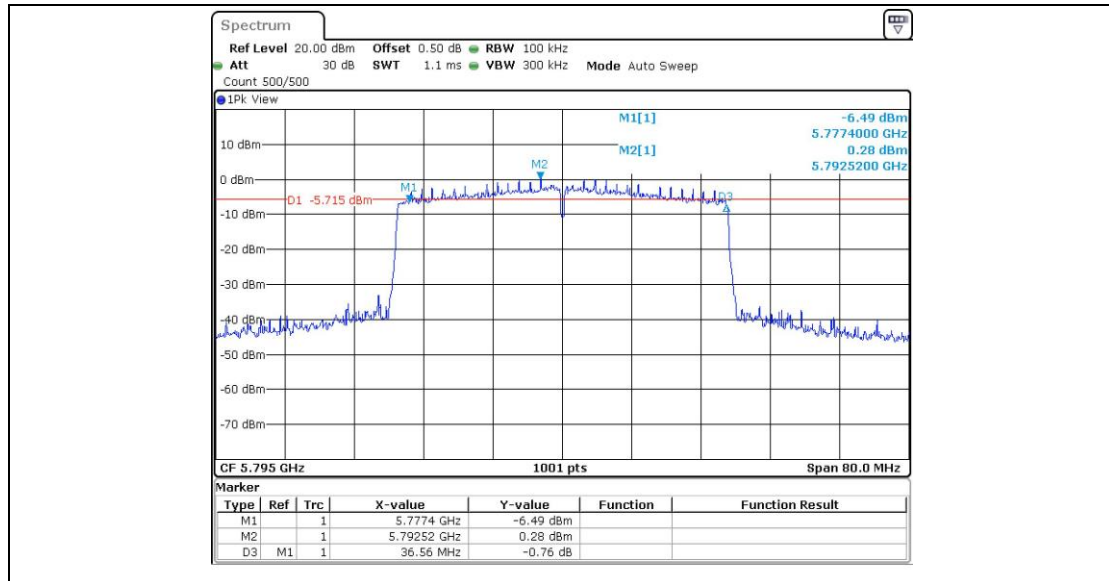
11AX20SISO_Ant1_5785



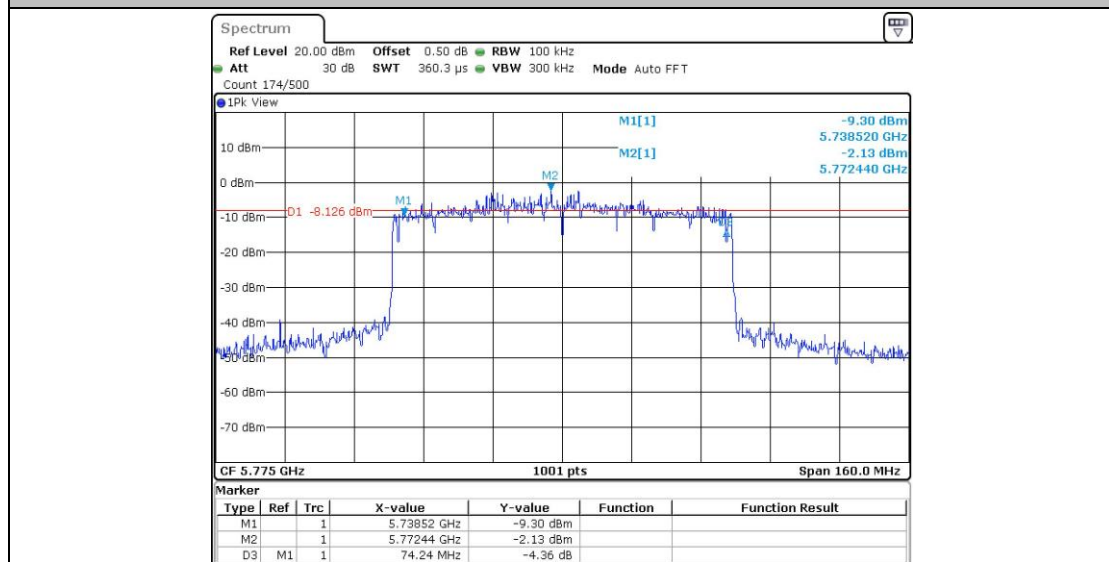
11AX20SISO_Ant1_5825



11AX40SISO_Ant1_5755



11AX40SISO_Ant1_5795



11AX80SISO_Ant1_5775

Appendix B1: Maximum conducted output power

Test Result

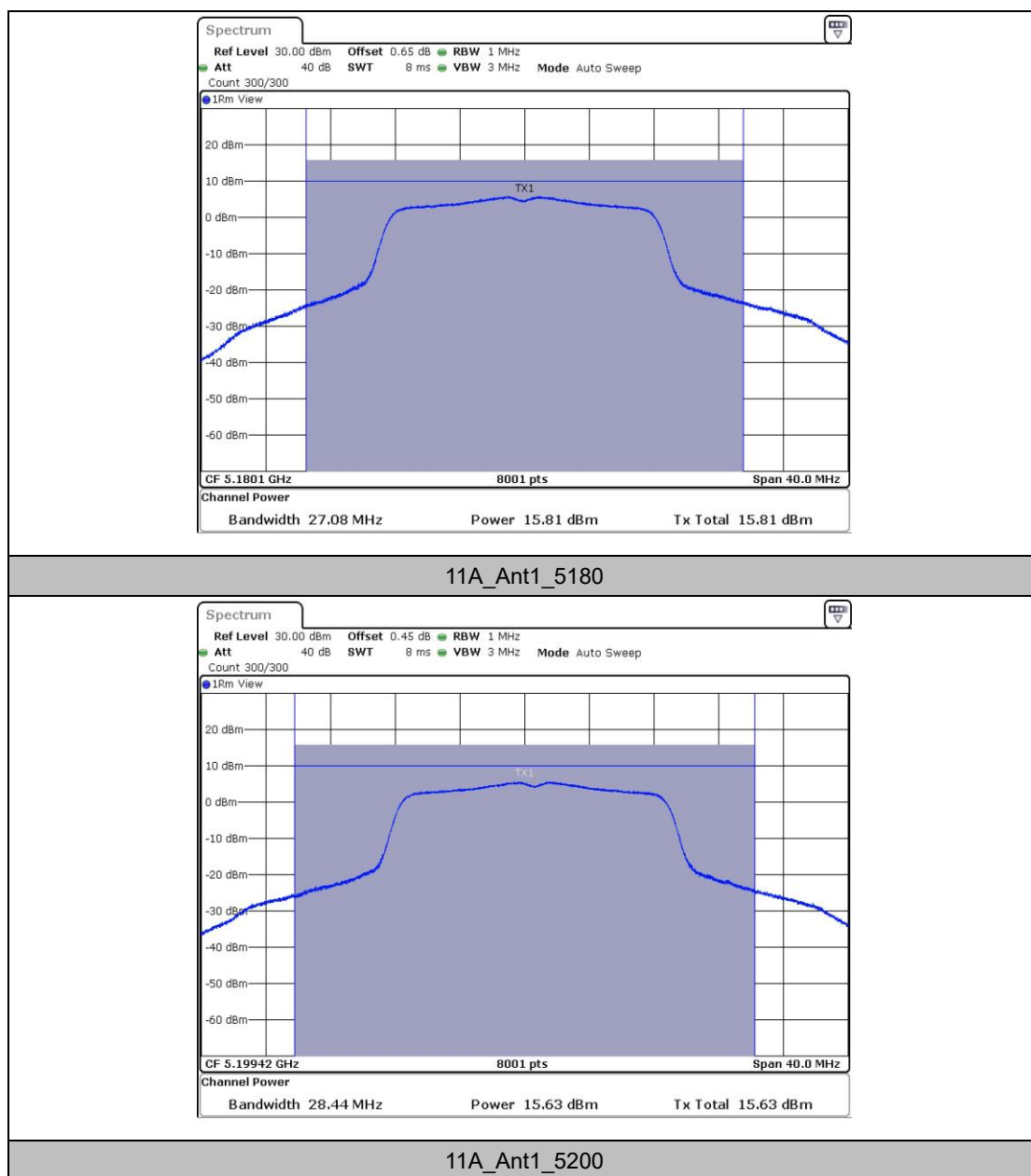
TestMode	Antenna	Channel	Result	Limit	Verdict
11A	Ant1	5180	15.81	<=23.98	PASS
		5200	15.63	<=23.98	PASS
		5240	16.10	<=23.98	PASS
		5260	15.08	<=23.98	PASS
		5280	15.23	<=23.98	PASS
		5320	14.96	<=23.98	PASS
		5500	15.65	<=23.98	PASS
		5580	15.68	<=23.98	PASS
		5700	15.34	<=23.98	PASS
		5745	15.54	<=30	PASS
		5785	15.73	<=30	PASS
		5825	15.37	<=30	PASS
11N20SISO	Ant1	5180	15.93	<=23.98	PASS
		5200	15.89	<=23.98	PASS
		5240	16.02	<=23.98	PASS
		5260	16.16	<=23.98	PASS
		5280	16.20	<=23.98	PASS
		5320	16.05	<=23.98	PASS
		5500	15.66	<=23.98	PASS
		5580	15.62	<=23.98	PASS
		5700	15.29	<=23.98	PASS
		5745	15.51	<=30	PASS
		5785	15.69	<=30	PASS
		5825	15.32	<=30	PASS
11N40SISO	Ant1	5190	15.93	<=23.98	PASS
		5230	15.94	<=23.98	PASS
		5270	16.02	<=23.98	PASS
		5310	16.00	<=23.98	PASS
		5510	16.74	<=23.98	PASS
		5550	16.77	<=23.98	PASS
		5670	16.32	<=23.98	PASS
		5755	16.33	<=30	PASS
		5795	16.73	<=30	PASS
11AC20SISO	Ant1	5180	15.79	<=23.98	PASS
		5200	15.79	<=23.98	PASS
		5240	16.06	<=23.98	PASS

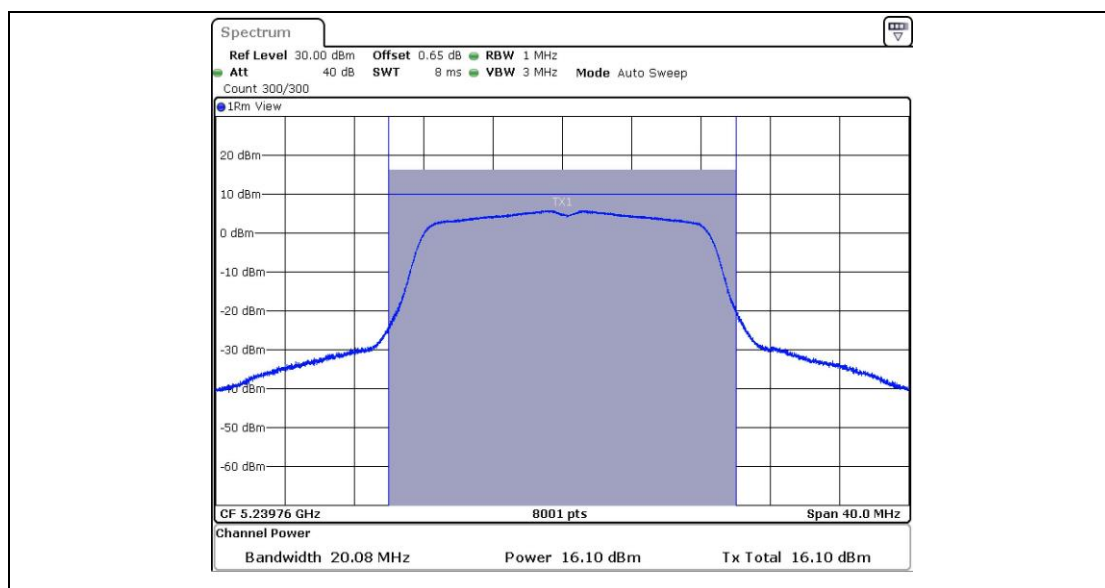
		5260	16.08	<=23.98	PASS
		5280	16.17	<=23.98	PASS
		5320	16.01	<=23.98	PASS
		5500	15.64	<=23.98	PASS
		5580	15.70	<=23.98	PASS
		5700	15.31	<=23.98	PASS
		5745	15.48	<=30	PASS
		5785	15.69	<=30	PASS
		5825	15.31	<=30	PASS
11AC40SISO	Ant1	5190	14.80	<=23.98	PASS
		5230	14.96	<=23.98	PASS
		5270	15.04	<=23.98	PASS
		5310	14.92	<=23.98	PASS
		5510	15.66	<=23.98	PASS
		5550	15.63	<=23.98	PASS
		5670	15.14	<=23.98	PASS
		5755	15.37	<=30	PASS
		5795	15.52	<=30	PASS
11AC80SISO	Ant1	5210	15.65	<=23.98	PASS
		5290	15.69	<=23.98	PASS
		5530	15.44	<=23.98	PASS
		5775	15.33	<=30	PASS
11AC160SISO	Ant1	5250	14.09	<=23.98	PASS
		5570	13.55	<=23.98	PASS
11AX20SISO	Ant1	5180	13.14	<=23.98	PASS
		5200	13.15	<=23.98	PASS
		5240	13.24	<=23.98	PASS
		5260	13.32	<=23.98	PASS
		5280	13.35	<=23.98	PASS
		5320	13.31	<=23.98	PASS
		5500	12.77	<=23.98	PASS
		5580	12.61	<=23.98	PASS
		5700	12.47	<=23.98	PASS
		5745	14.88	<=30	PASS
		5785	14.90	<=30	PASS
		5825	14.72	<=30	PASS
11AX40SISO	Ant1	5190	14.23	<=23.98	PASS
		5230	14.18	<=23.98	PASS
		5270	14.28	<=23.98	PASS
		5310	14.27	<=23.98	PASS
		5510	13.83	<=23.98	PASS
		5550	13.88	<=23.98	PASS
		5670	13.39	<=23.98	PASS

		5755	13.63	<=30	PASS
		5795	13.64	<=30	PASS
11AX80SISO	Ant1	5210	15.01	<=23.98	PASS
		5290	15.27	<=23.98	PASS
		5530	14.78	<=23.98	PASS
		5775	14.55	<=30	PASS
11AX160SISO	Ant1	5250	13.38	<=23.98	PASS
		5570	12.64	<=23.98	PASS

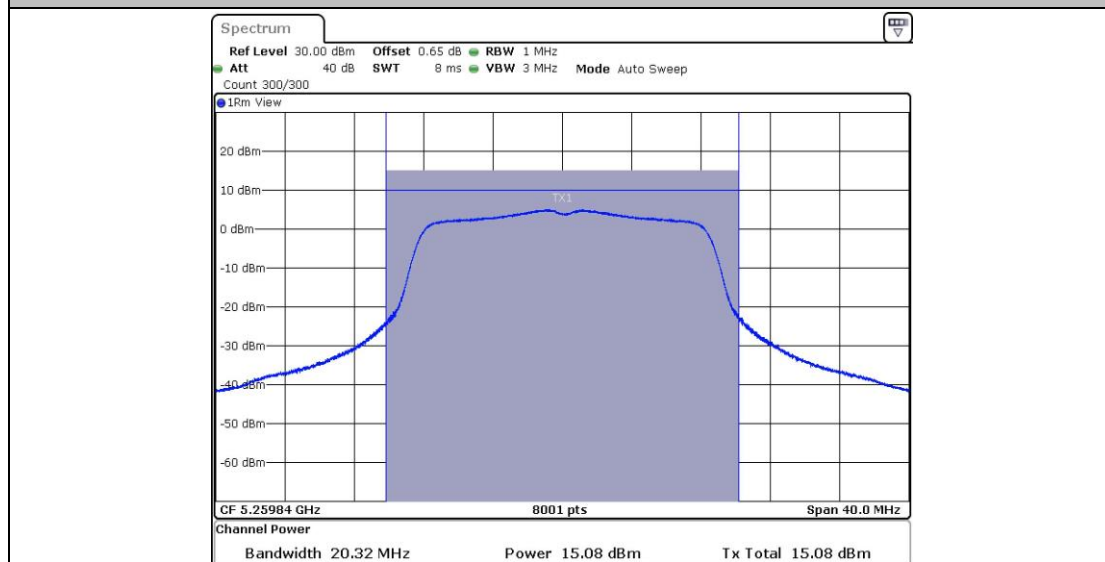
Note: The Duty Cycle Factor is compensated in the graph.

Test Graphs

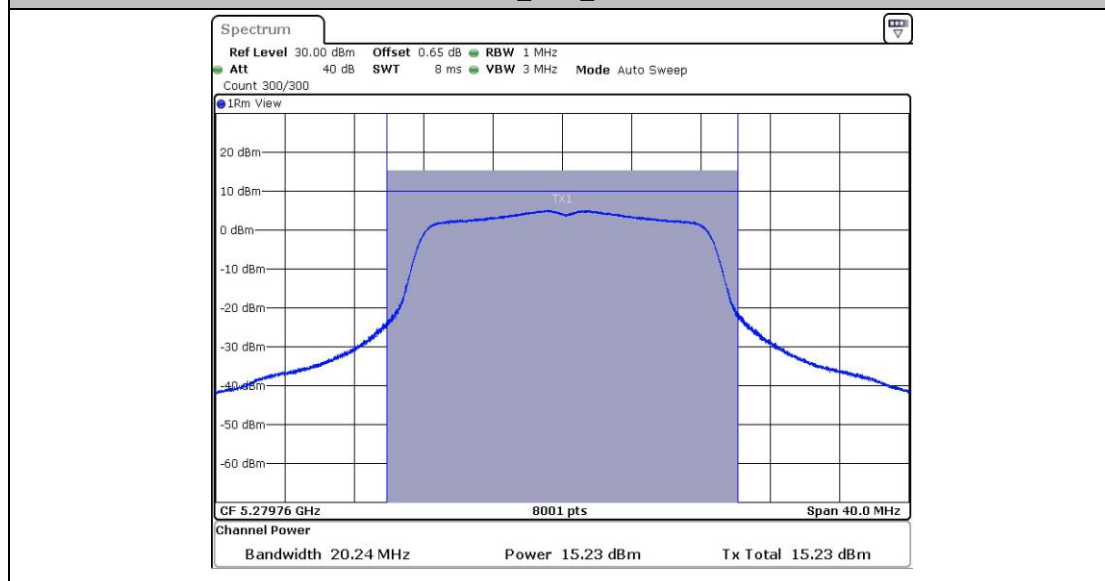


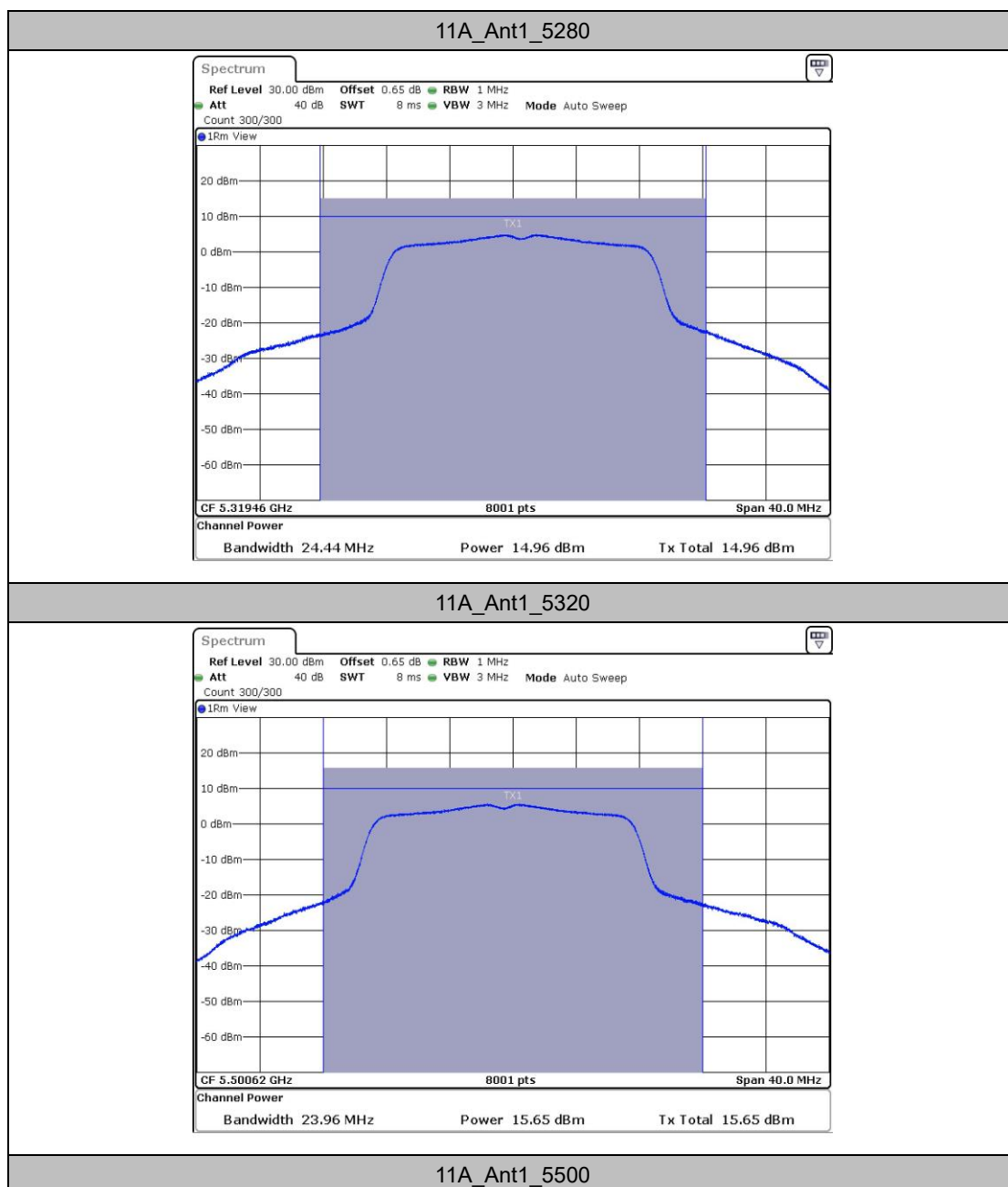


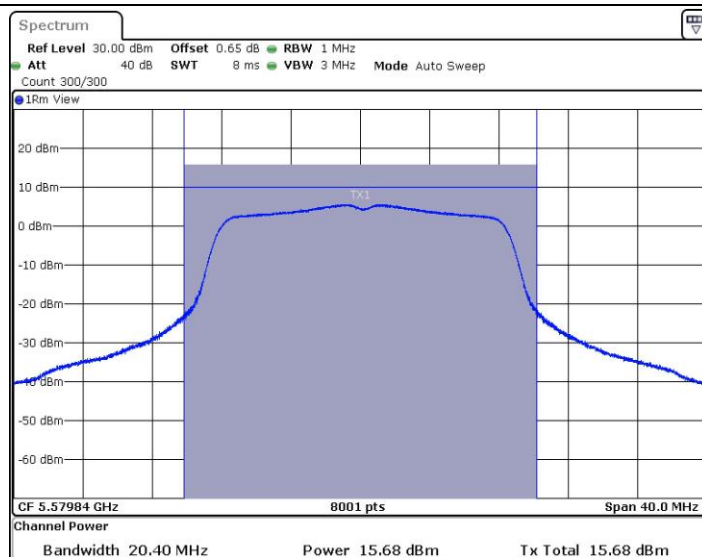
11A_Ant1_5240



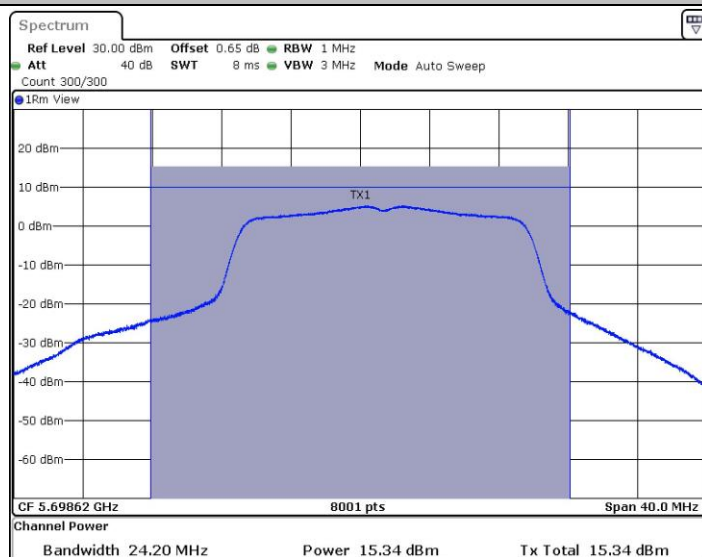
11A_Ant1_5260



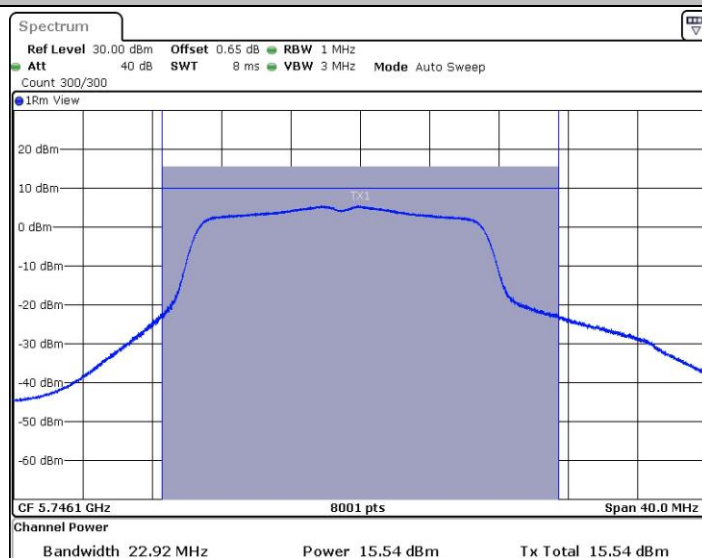


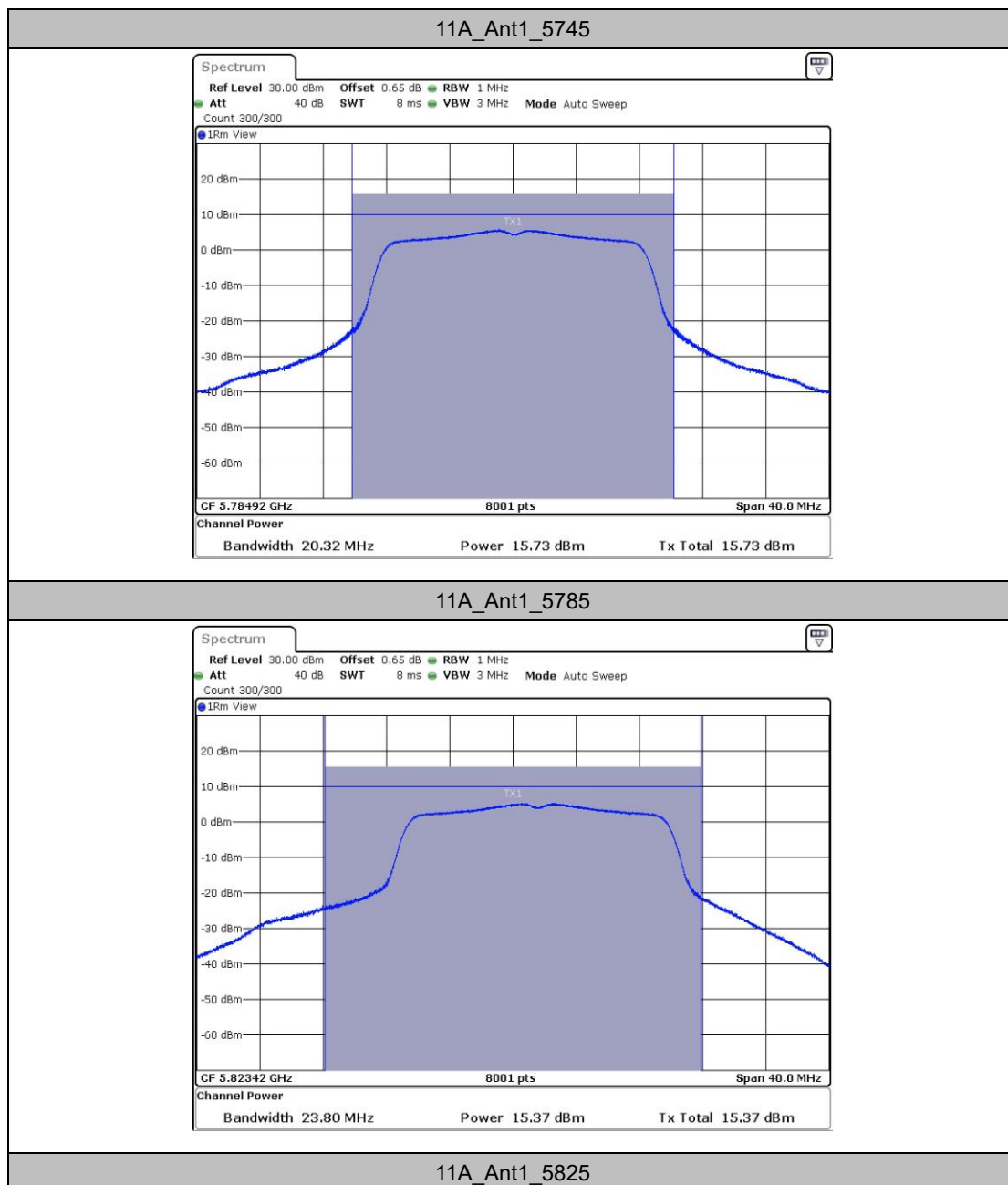


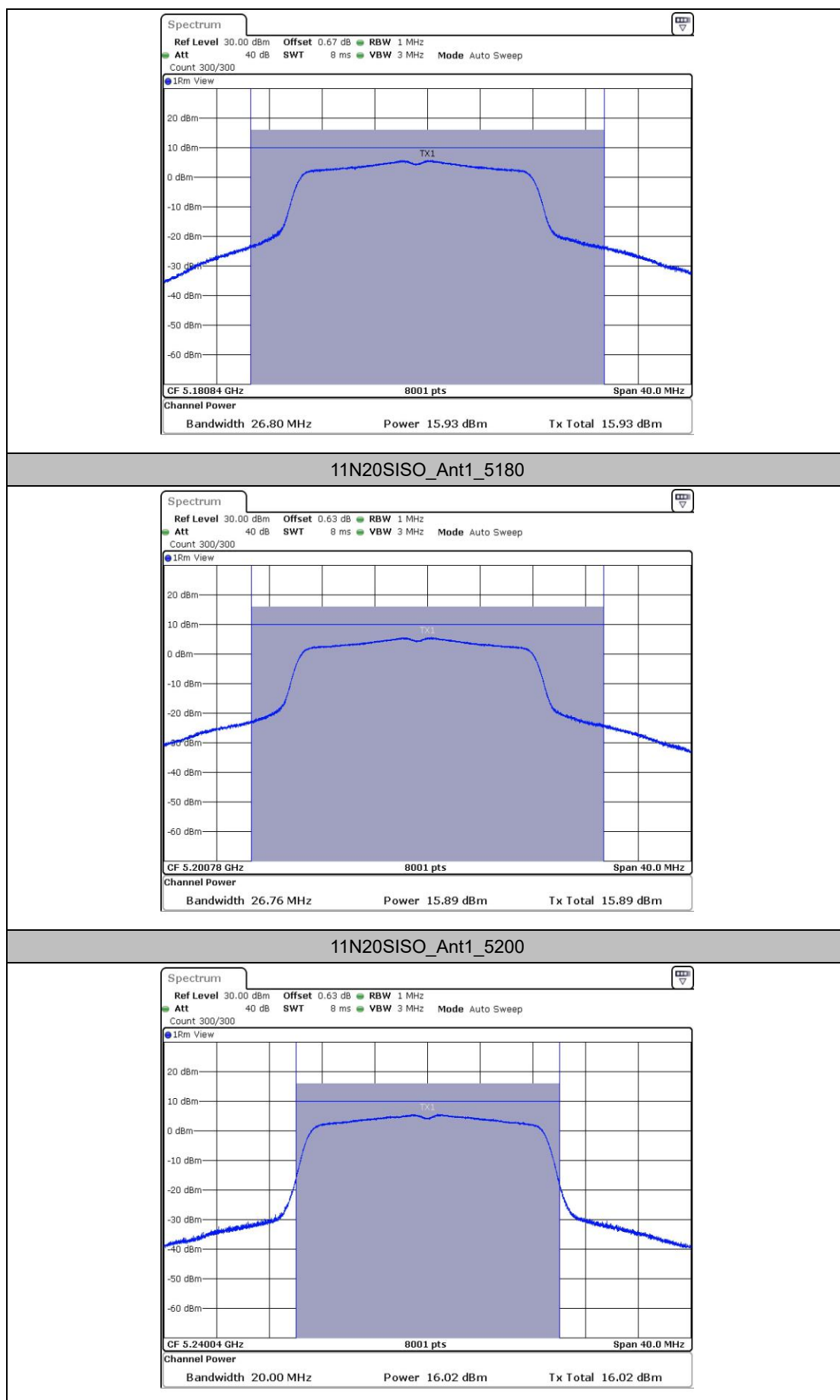
11A_Ant1_5580

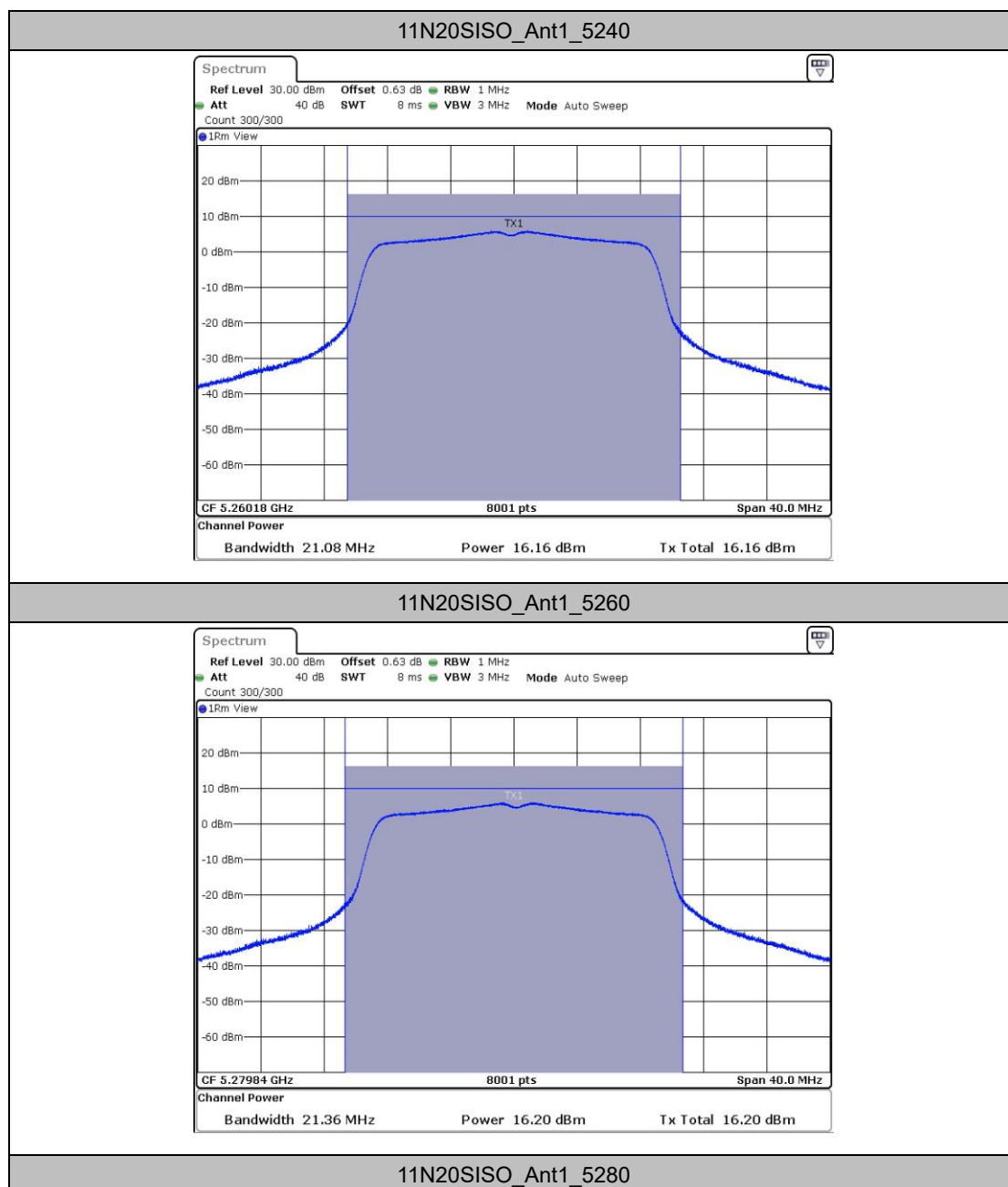


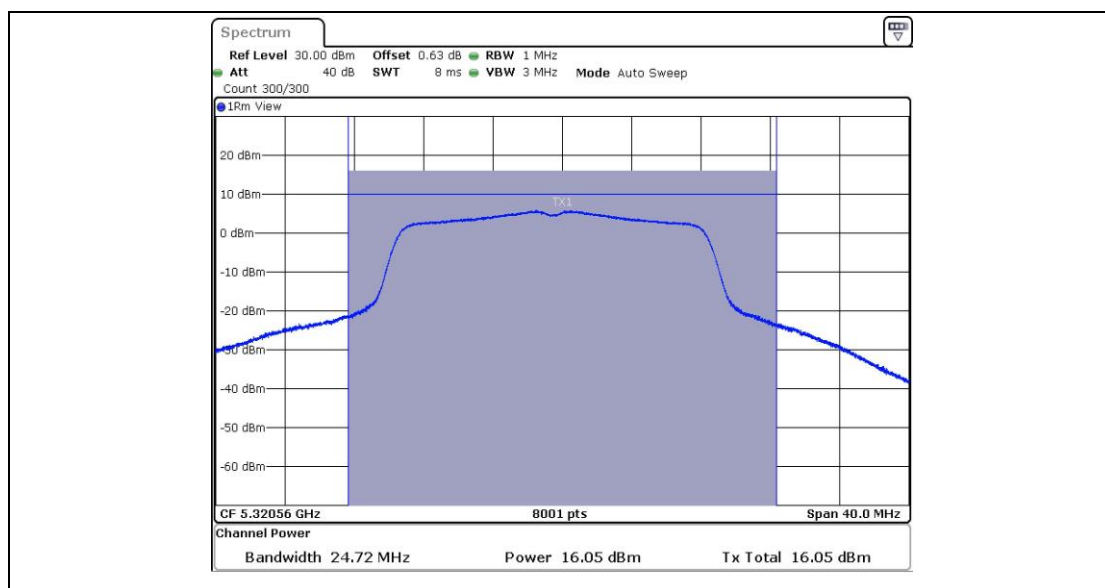
11A_Ant1_5700



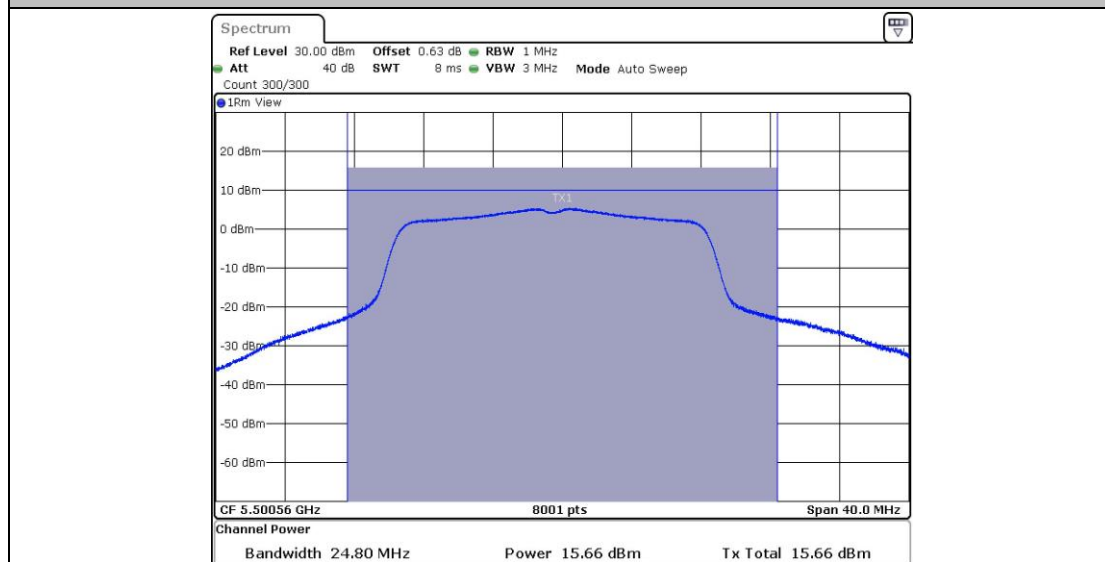




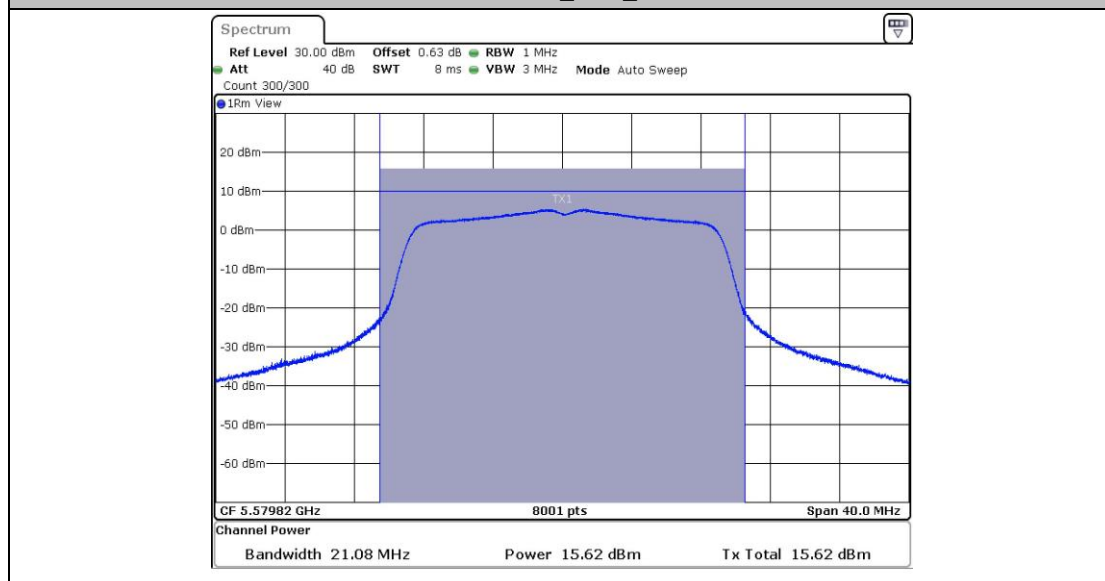


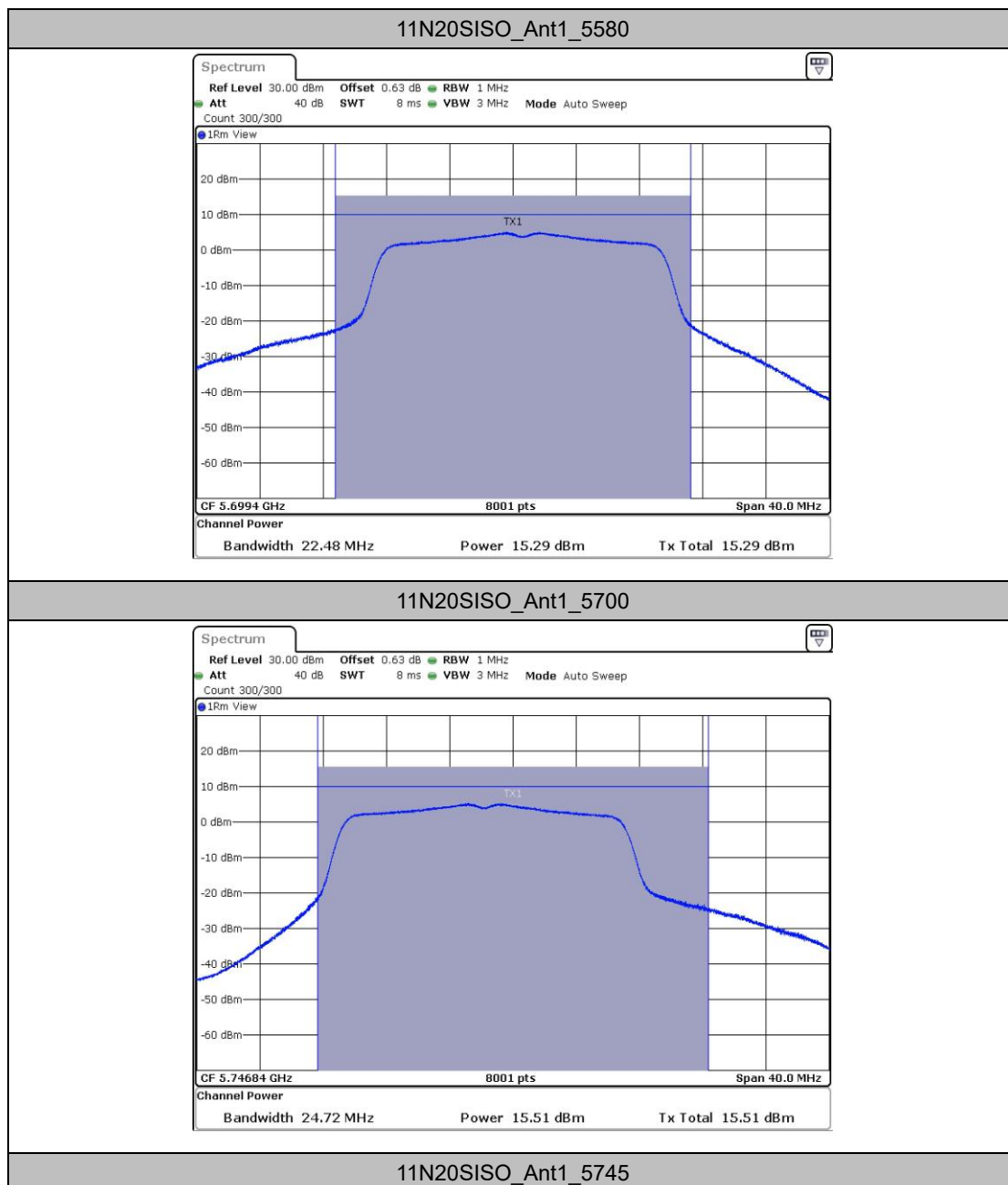


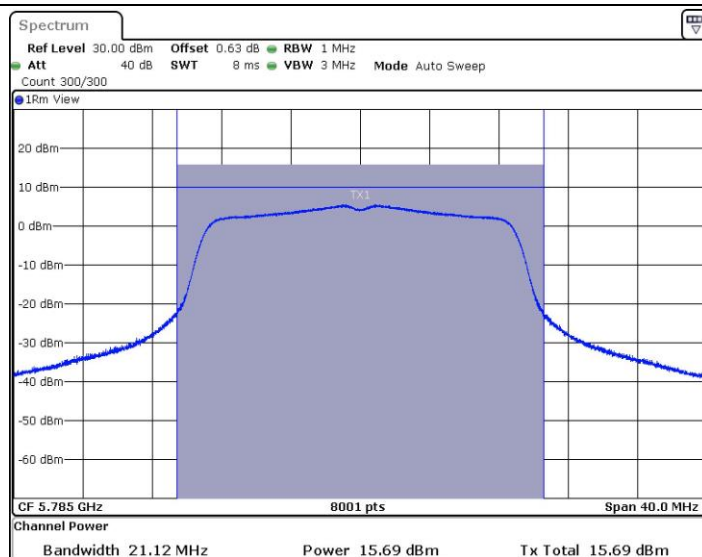
11N20SISO_Ant1_5320



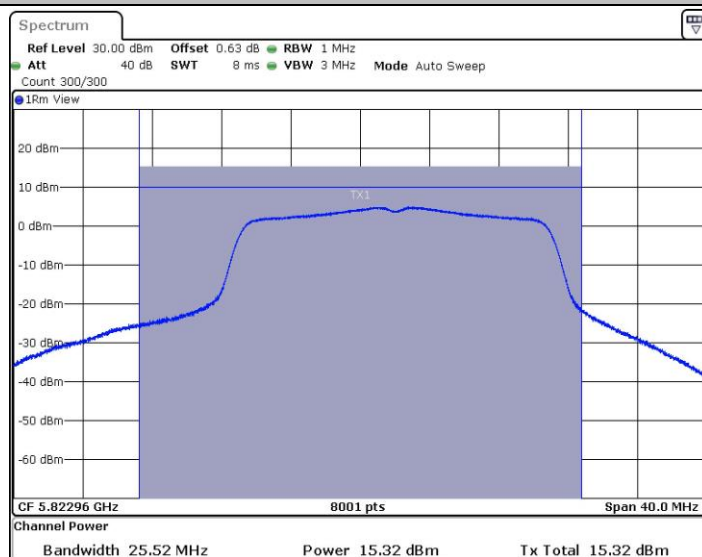
11N20SISO_Ant1_5500



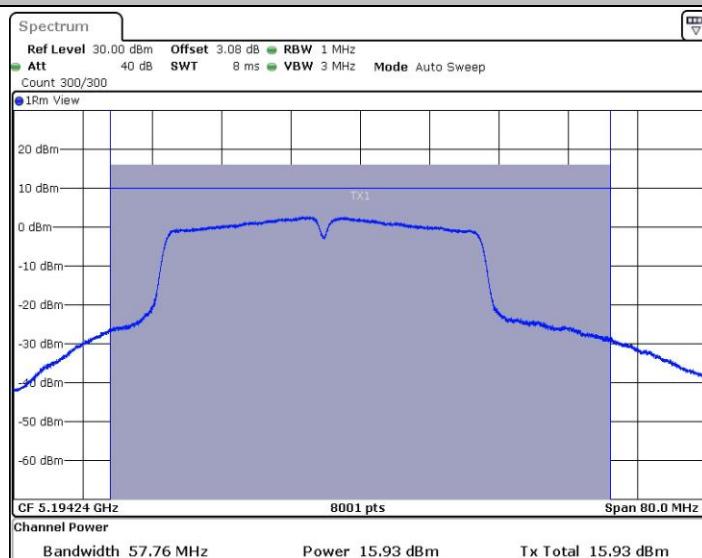


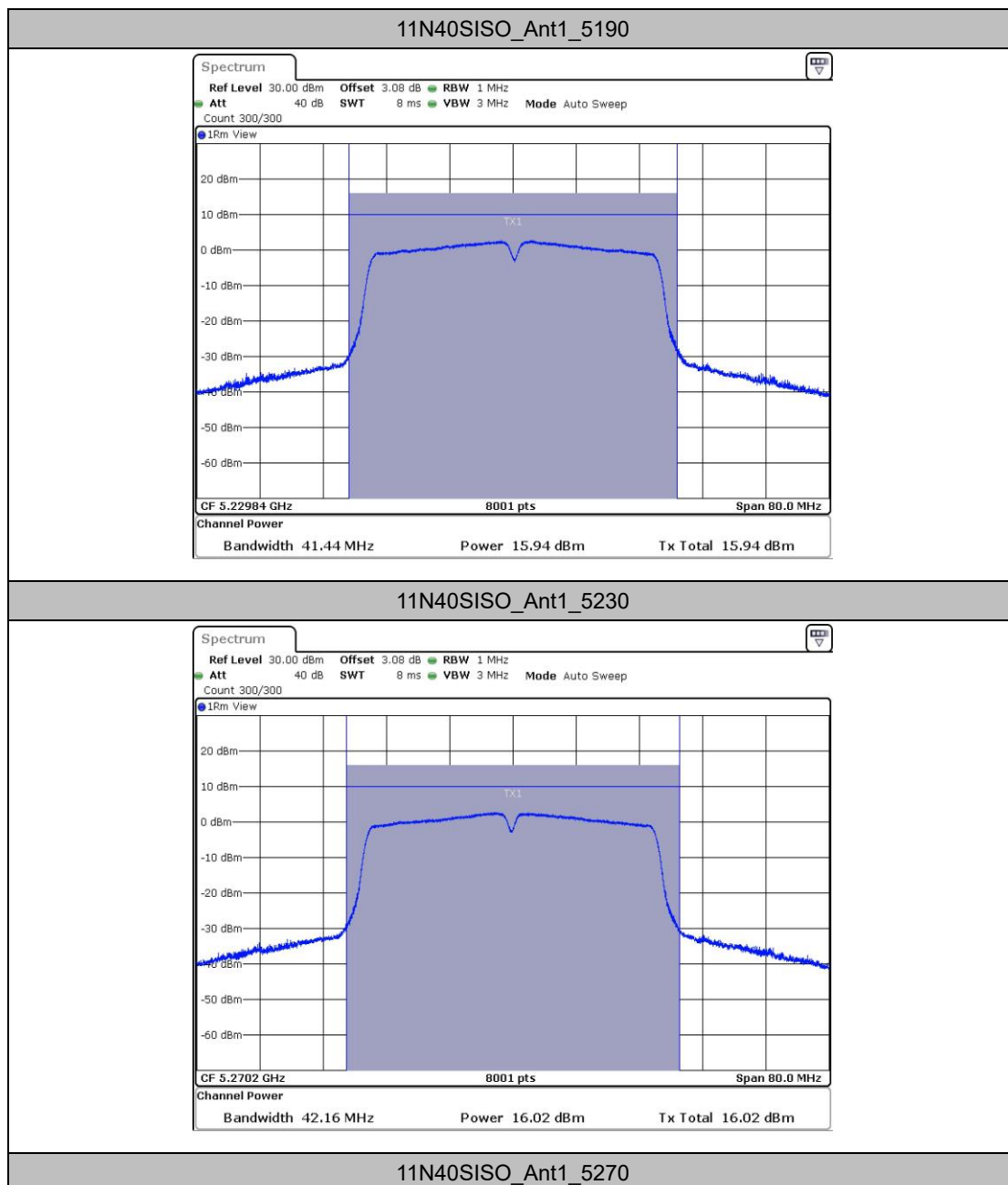


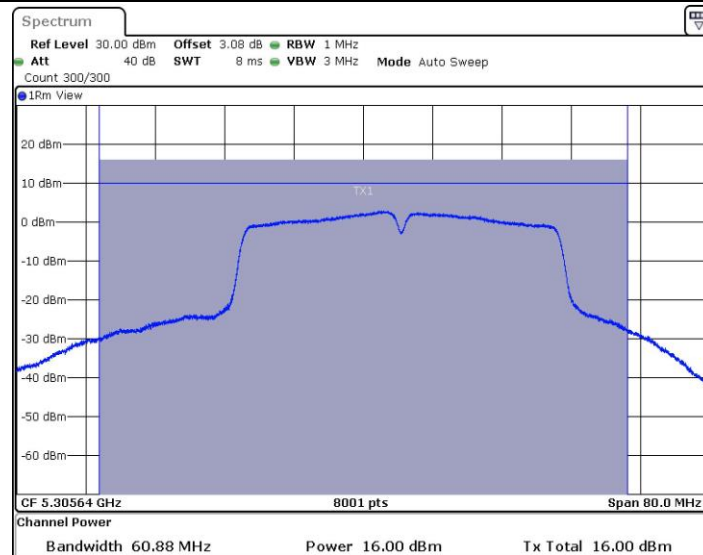
11N20SISO_Ant1_5785



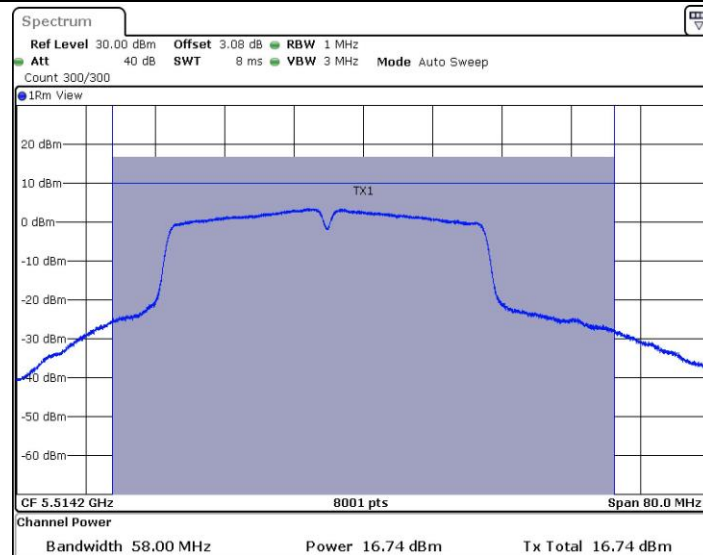
11N20SISO_Ant1_5825



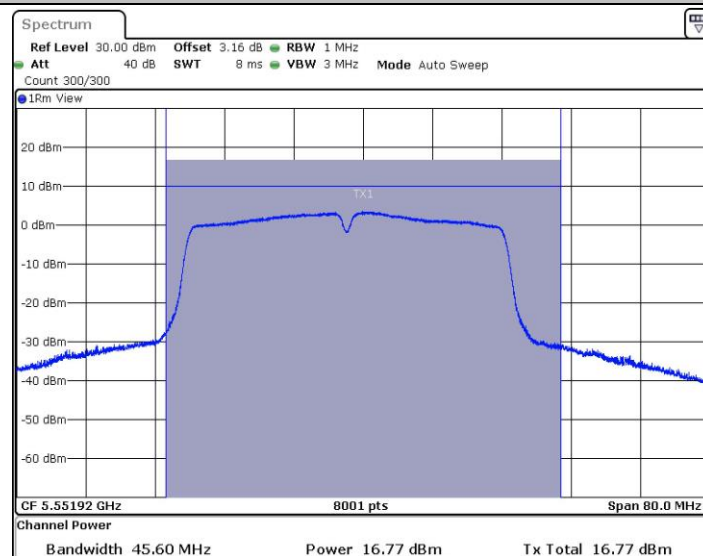


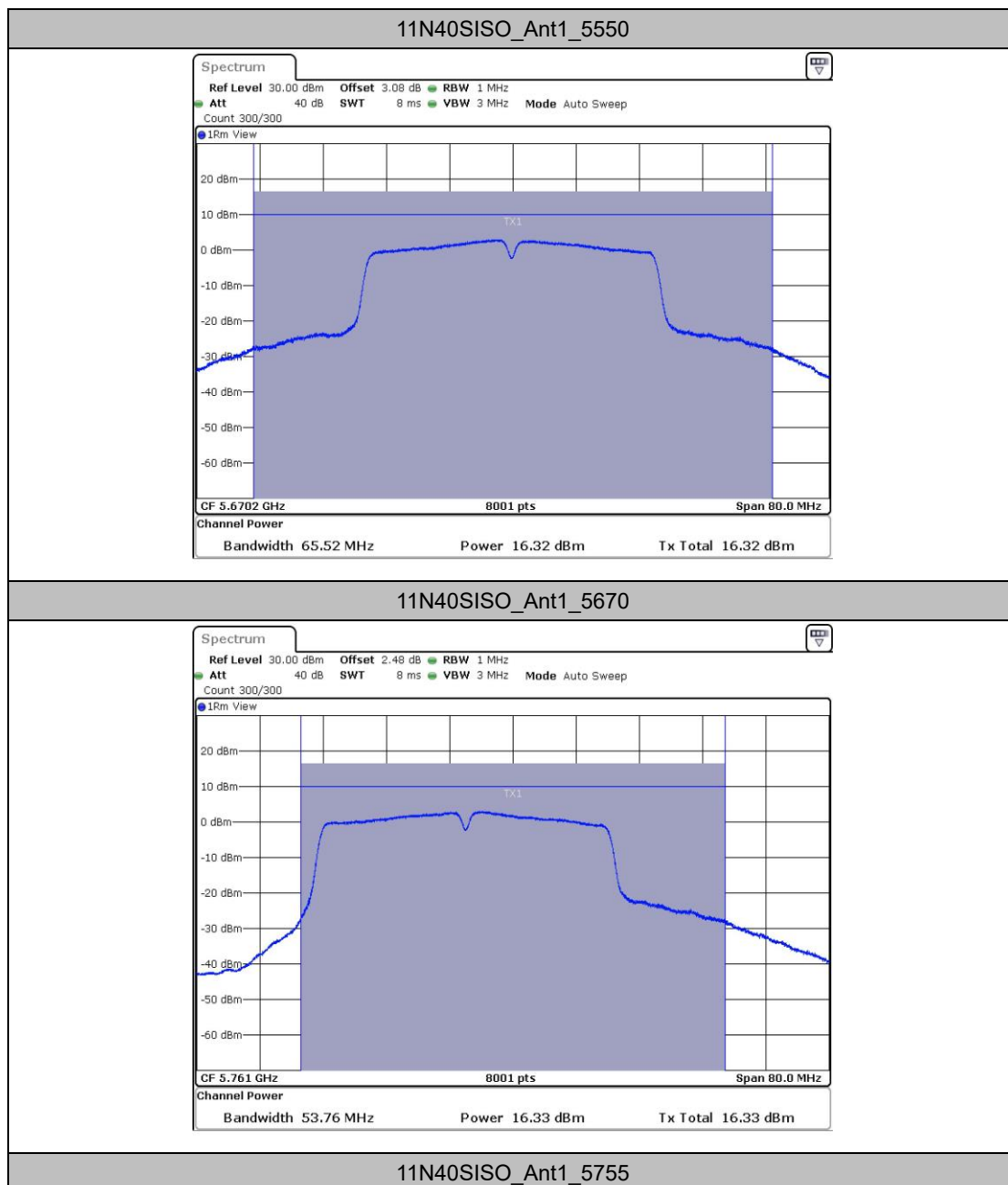


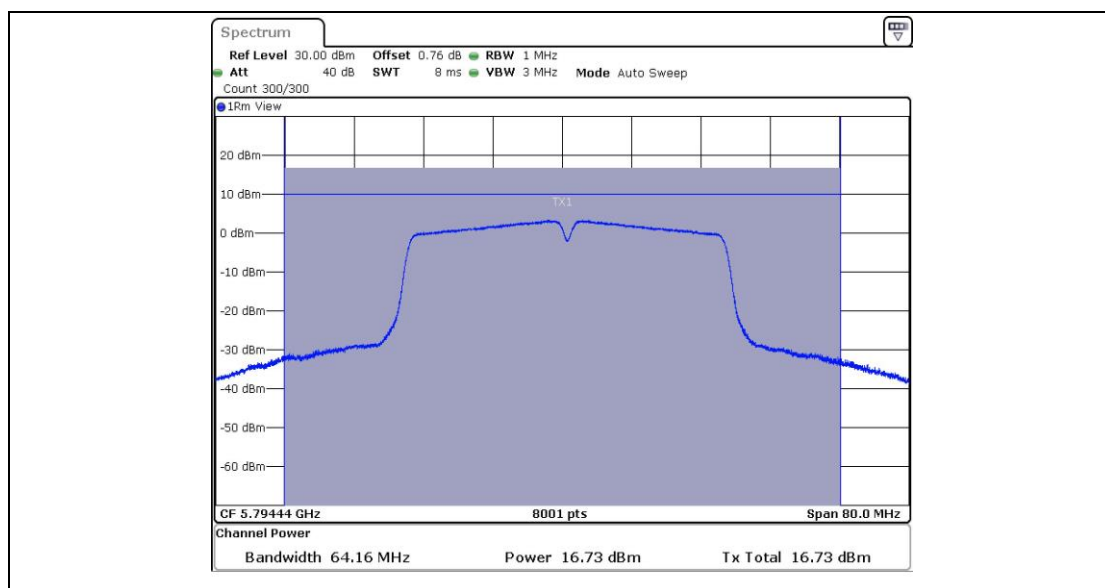
11N40SISO_Ant1_5310



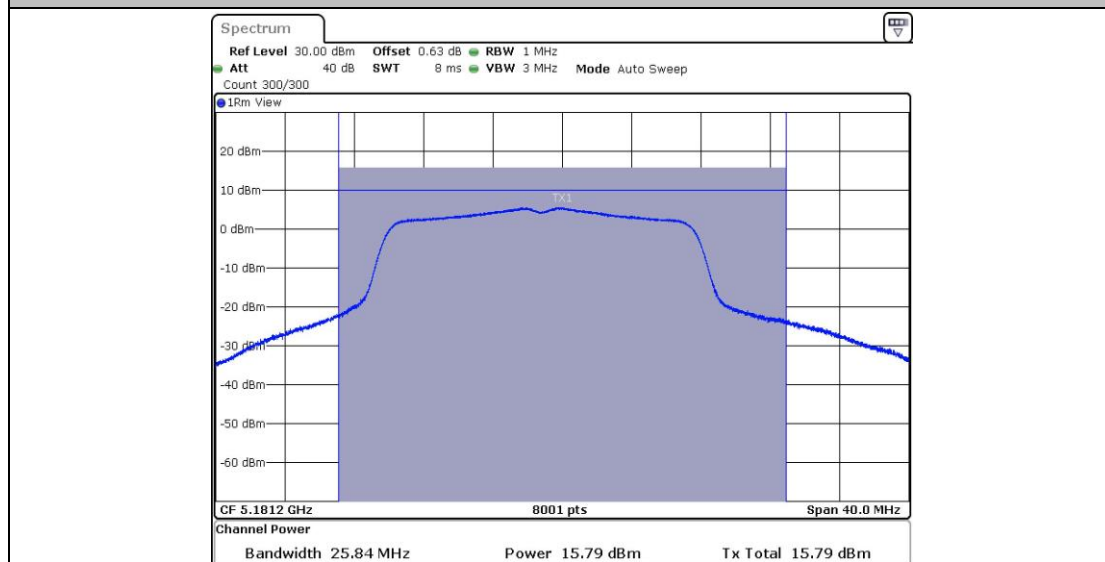
11N40SISO_Ant1_5510



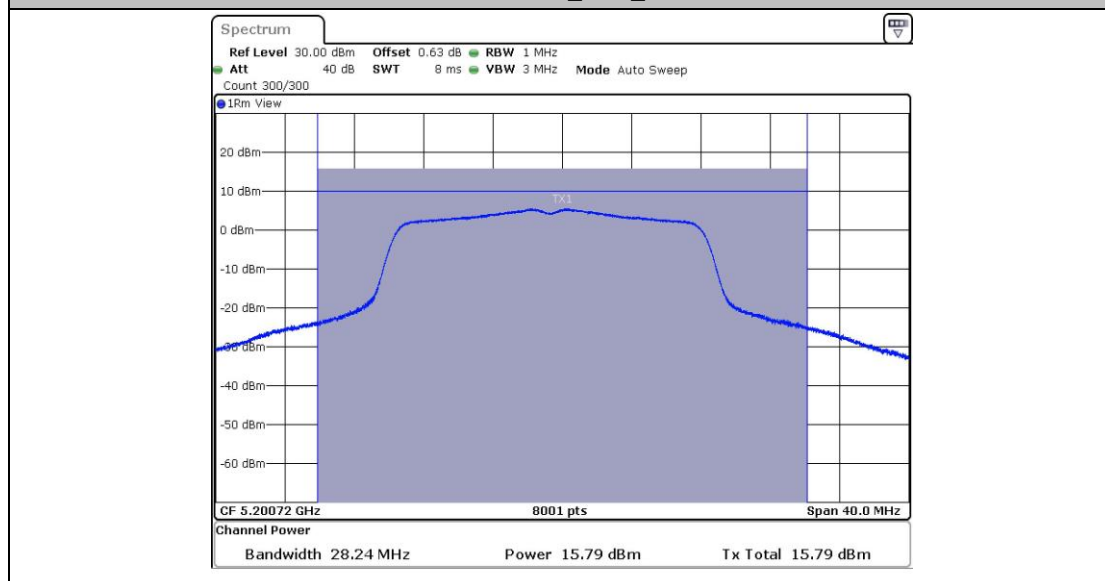


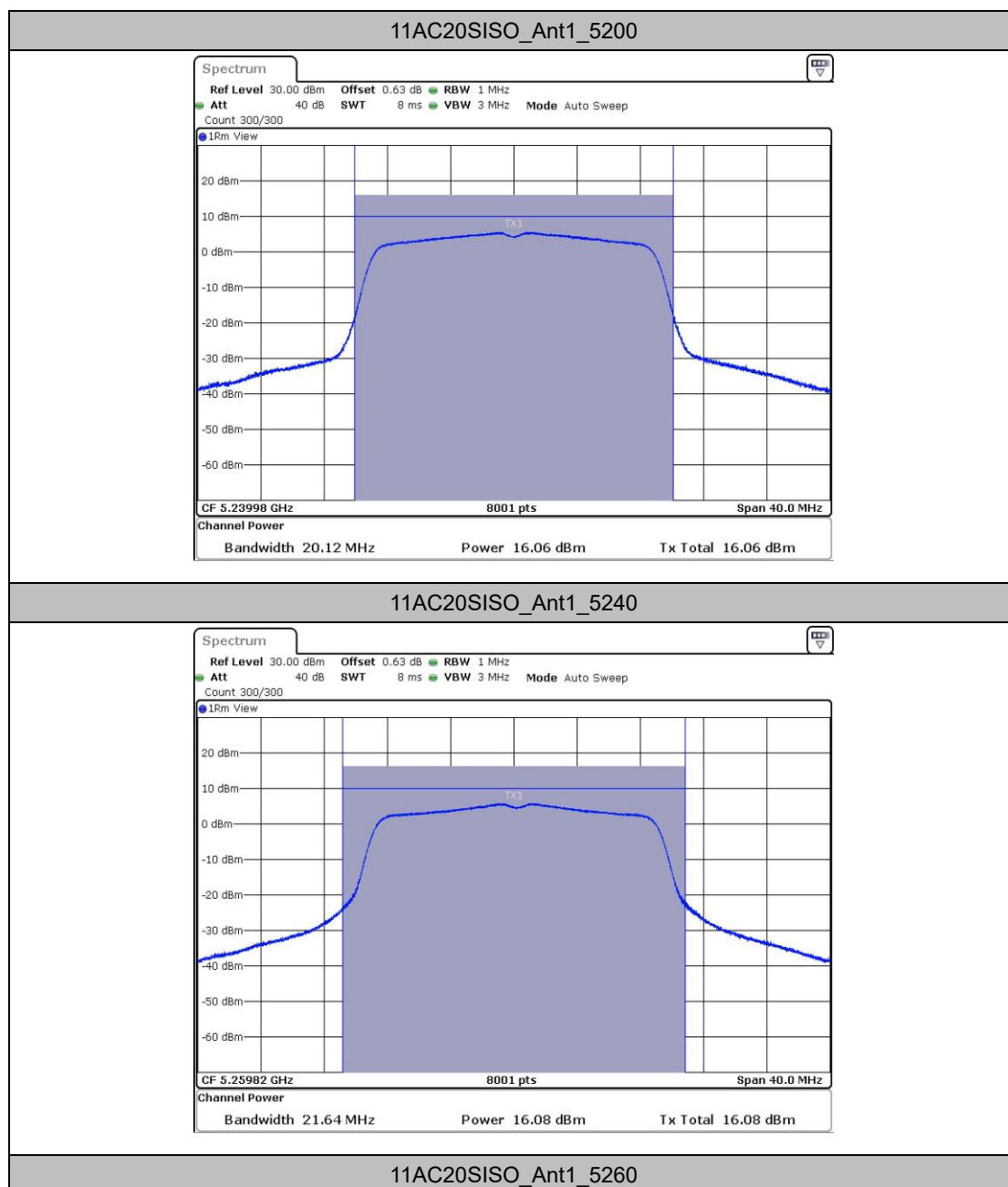


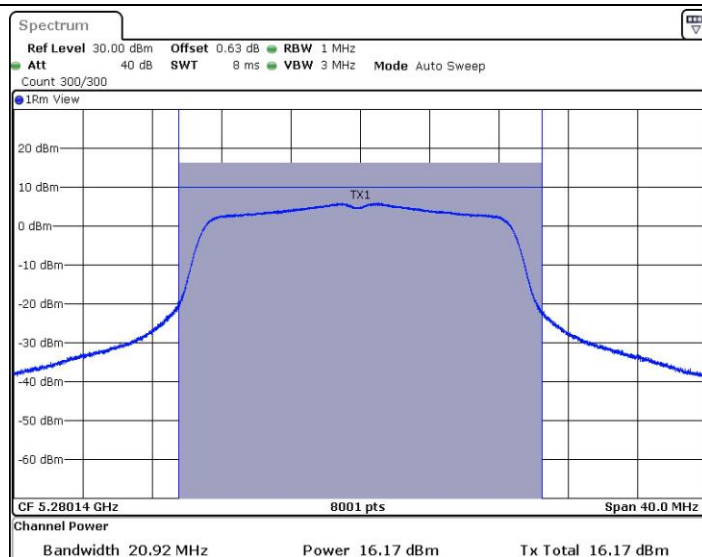
11N40SISO_Ant1_5795



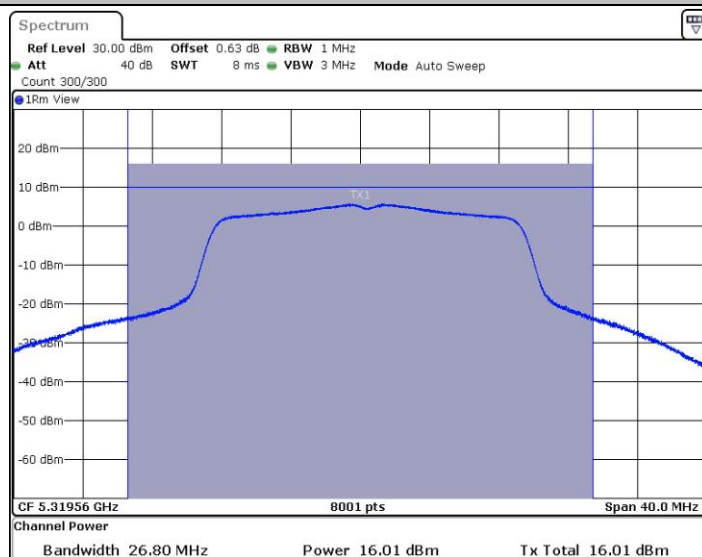
11AC20SISO_Ant1_5180



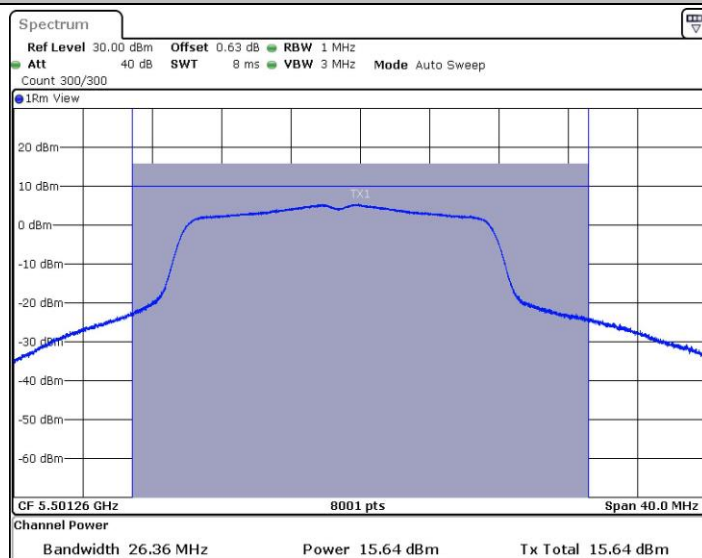


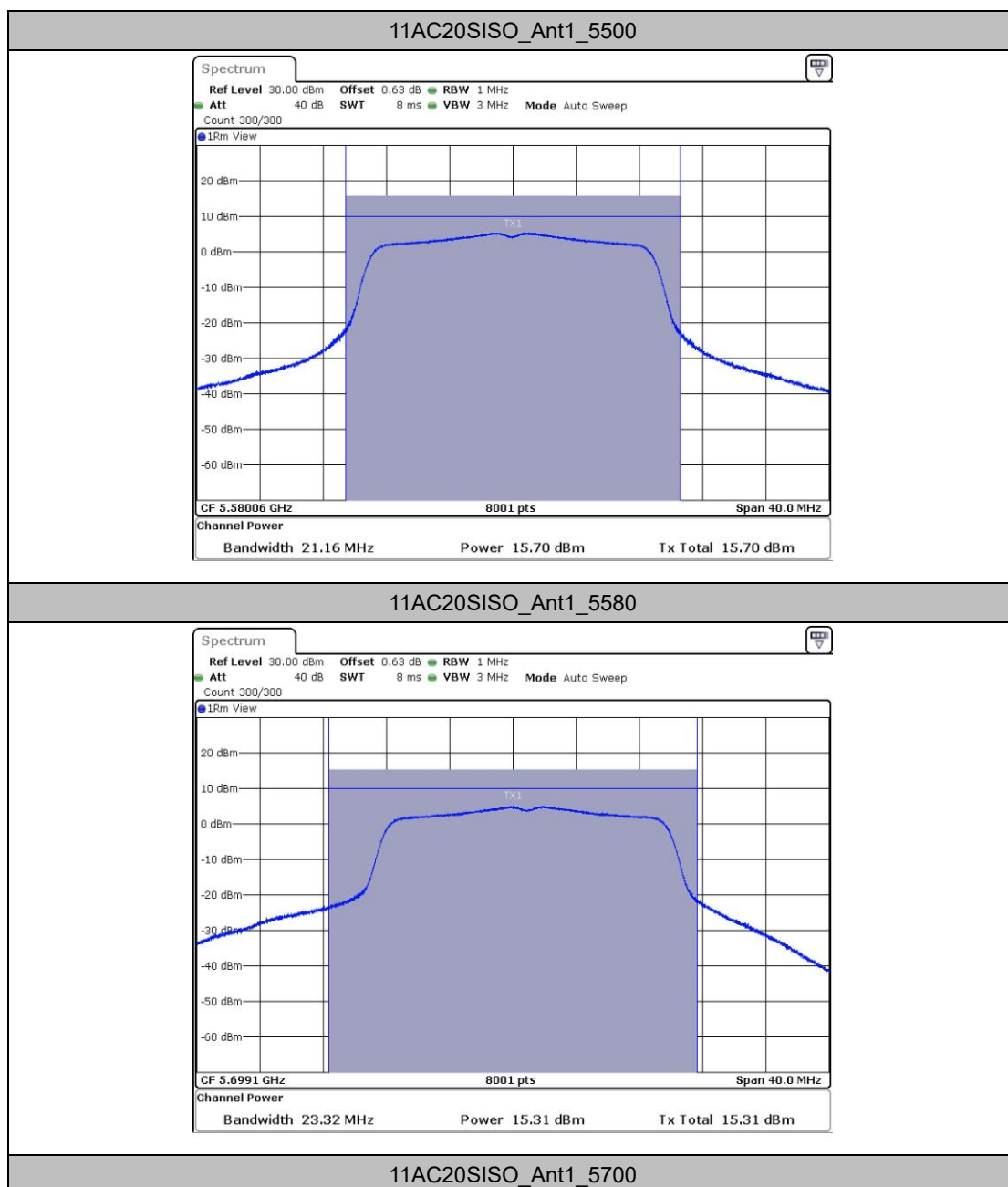


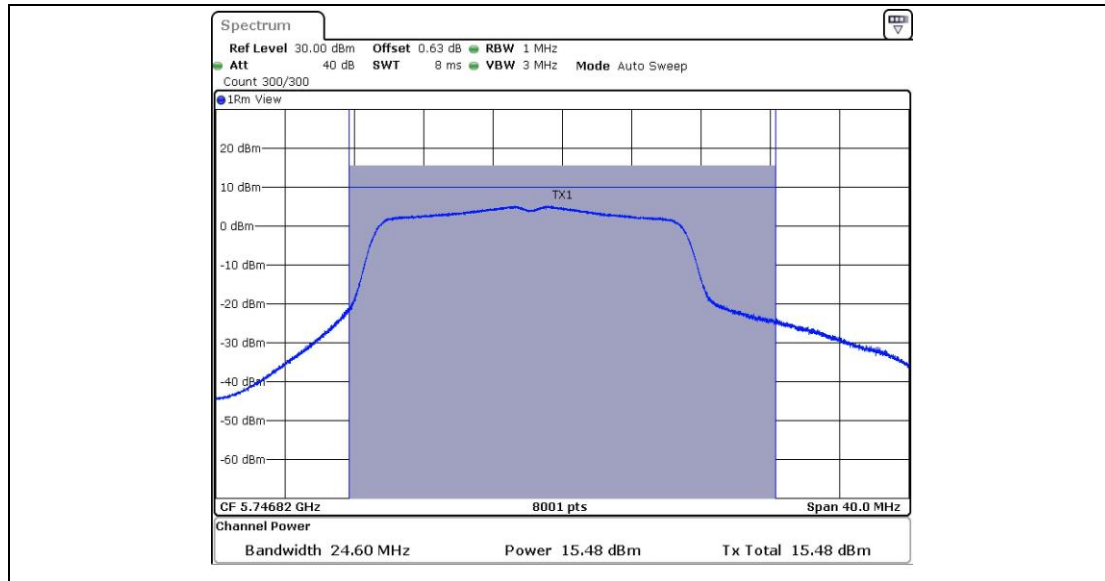
11AC20SISO_Ant1_5280



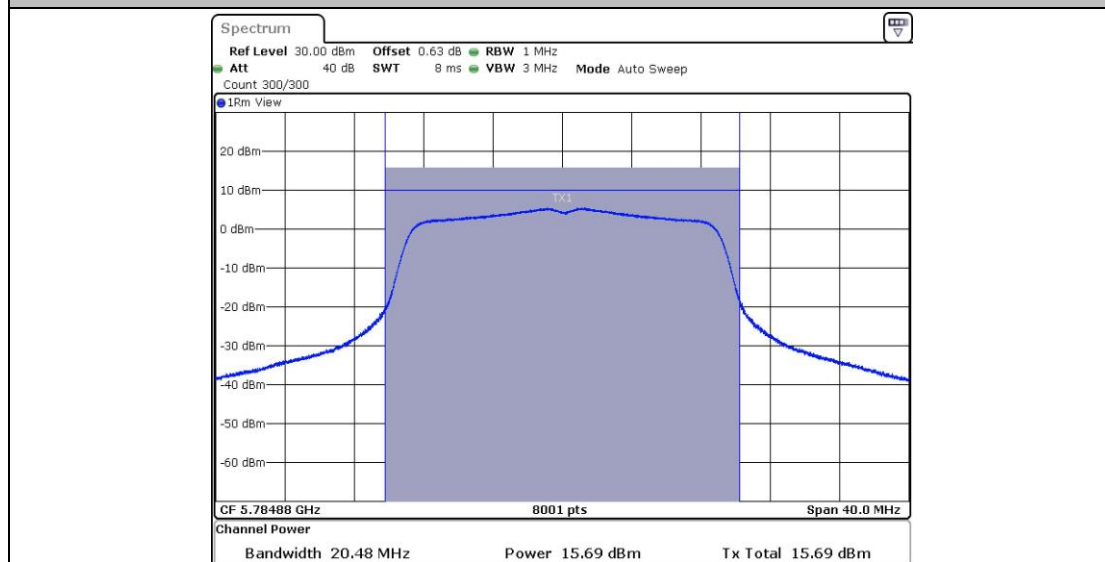
11AC20SISO_Ant1_5320



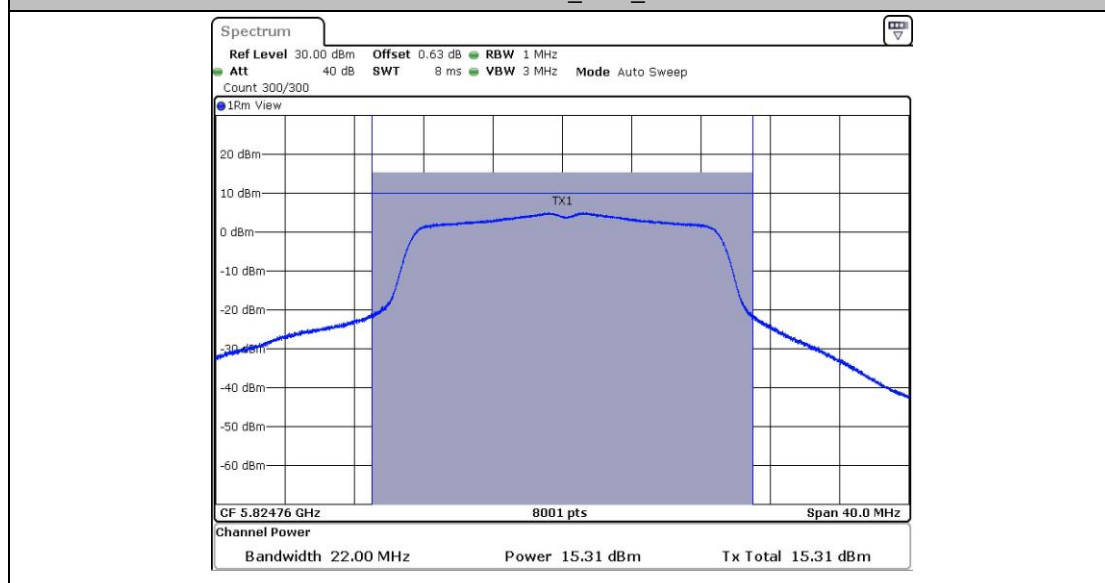


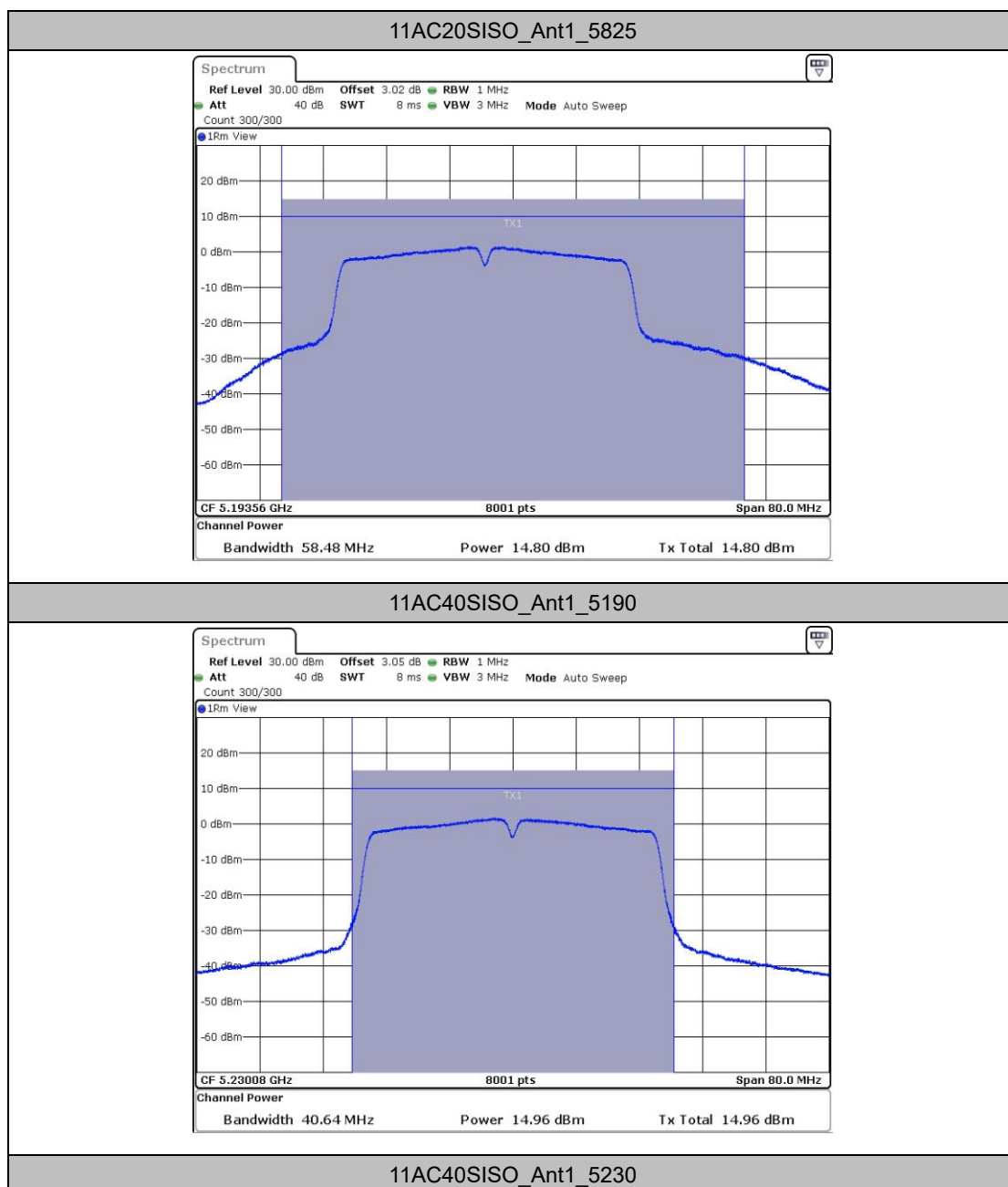


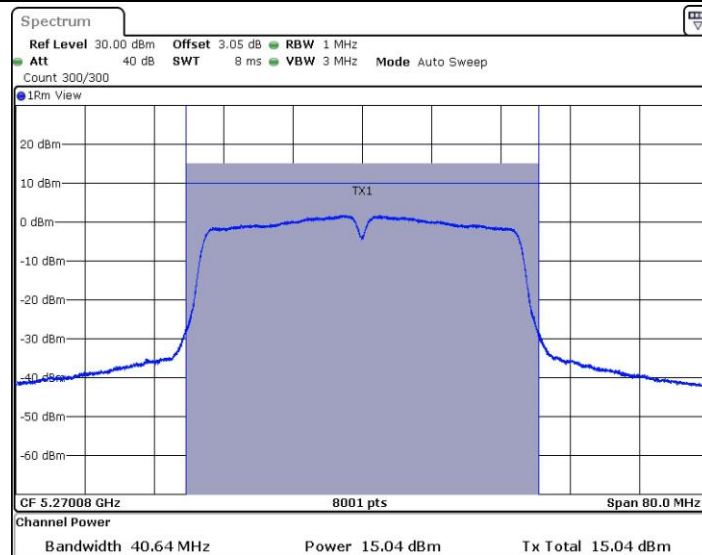
11AC20SISO_Ant1_5745



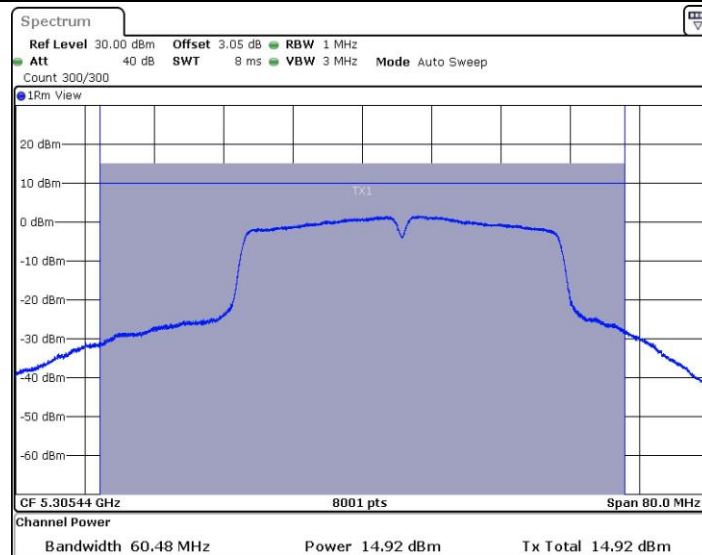
11AC20SISO_Ant1_5785



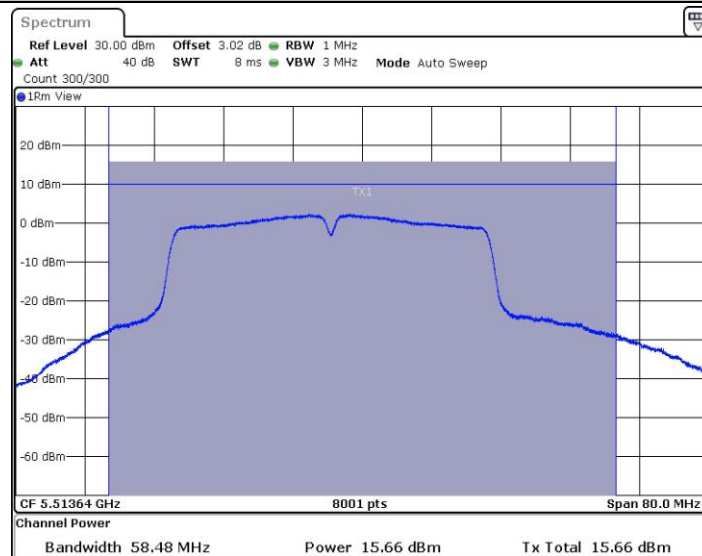


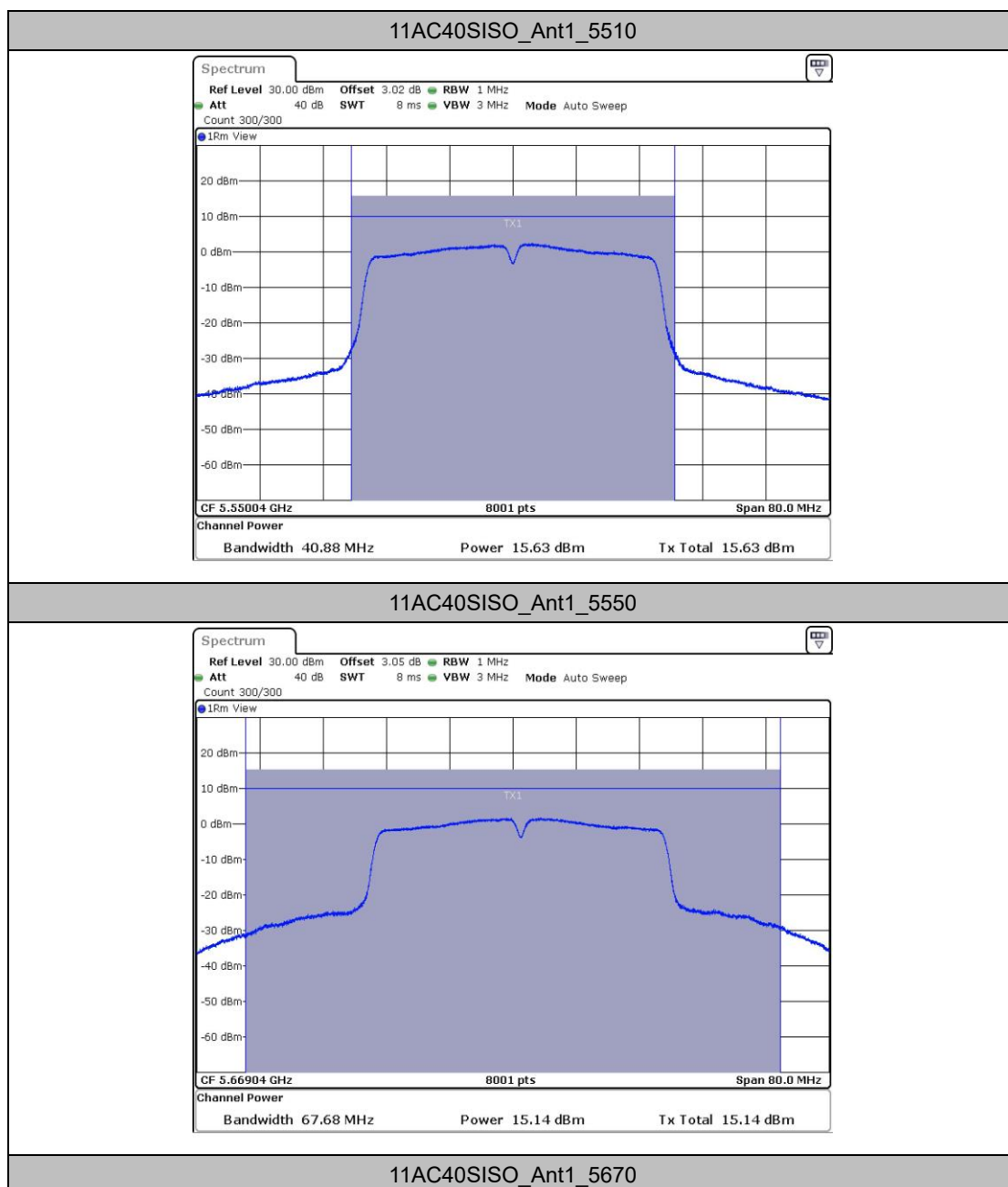


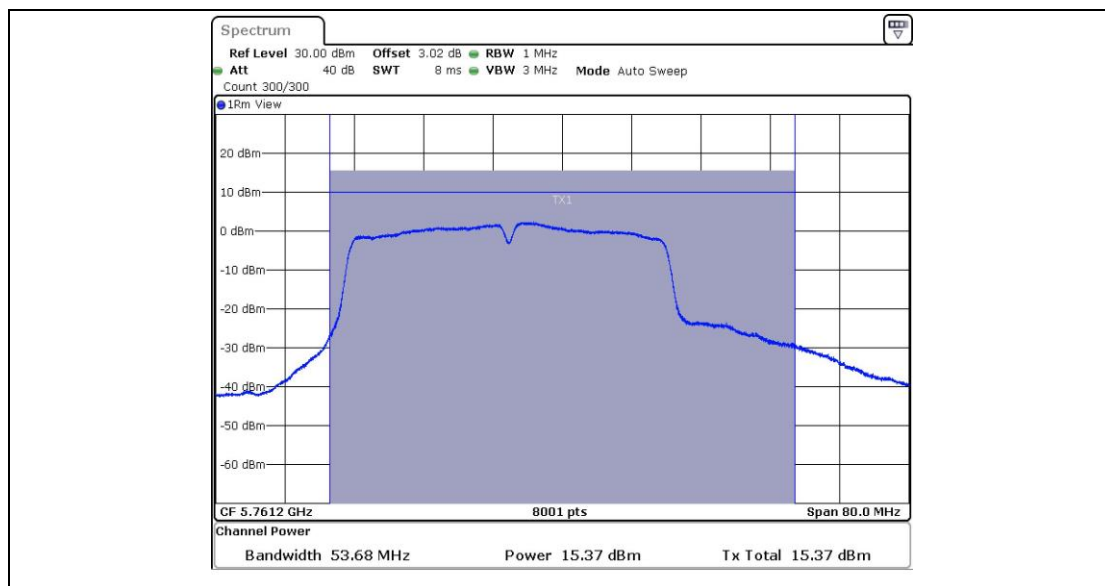
11AC40SISO_Ant1_5270



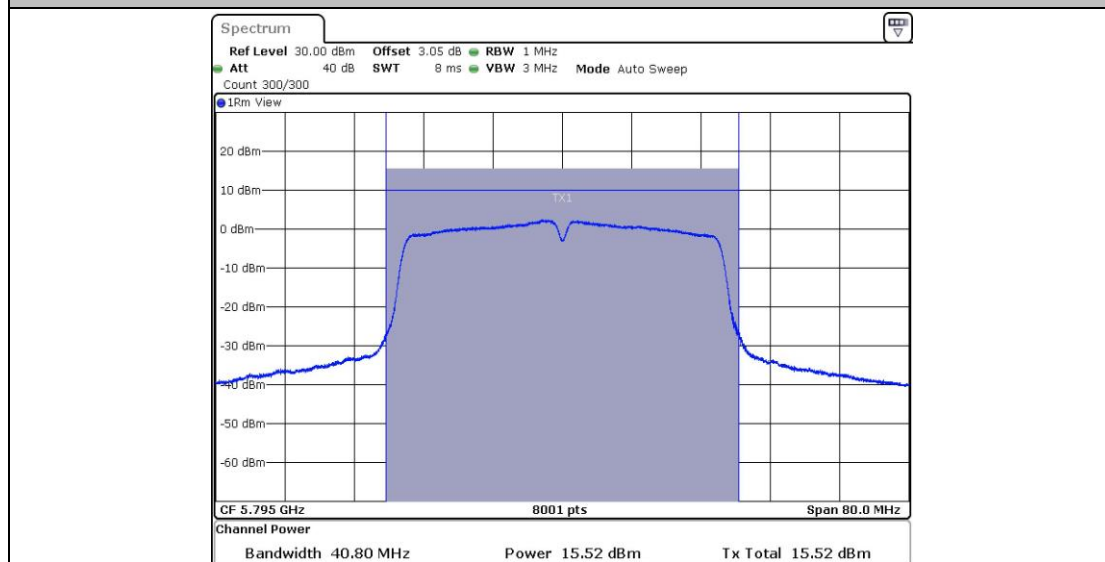
11AC40SISO_Ant1_5310



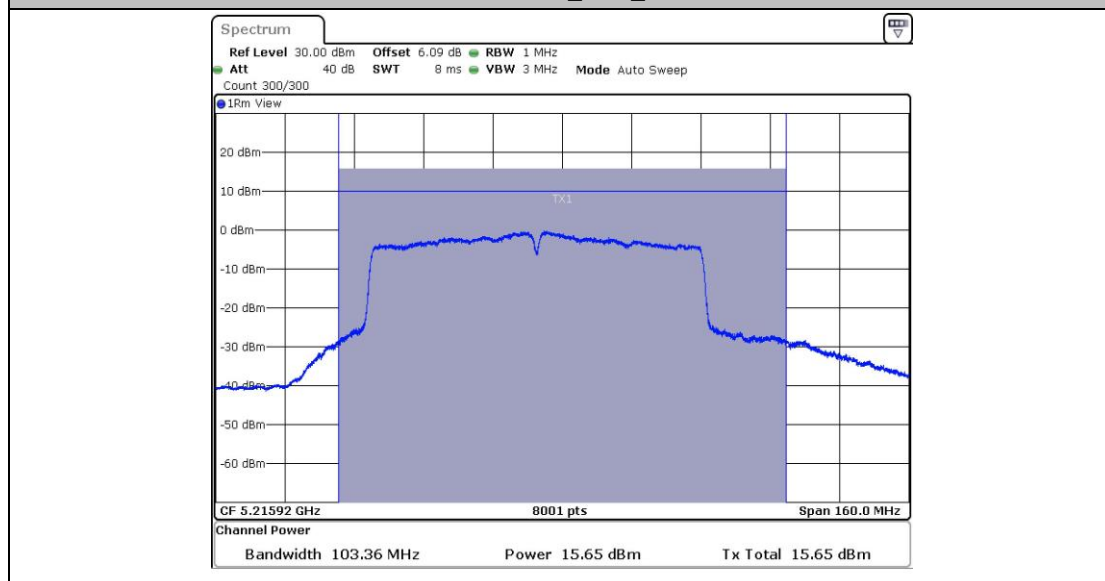


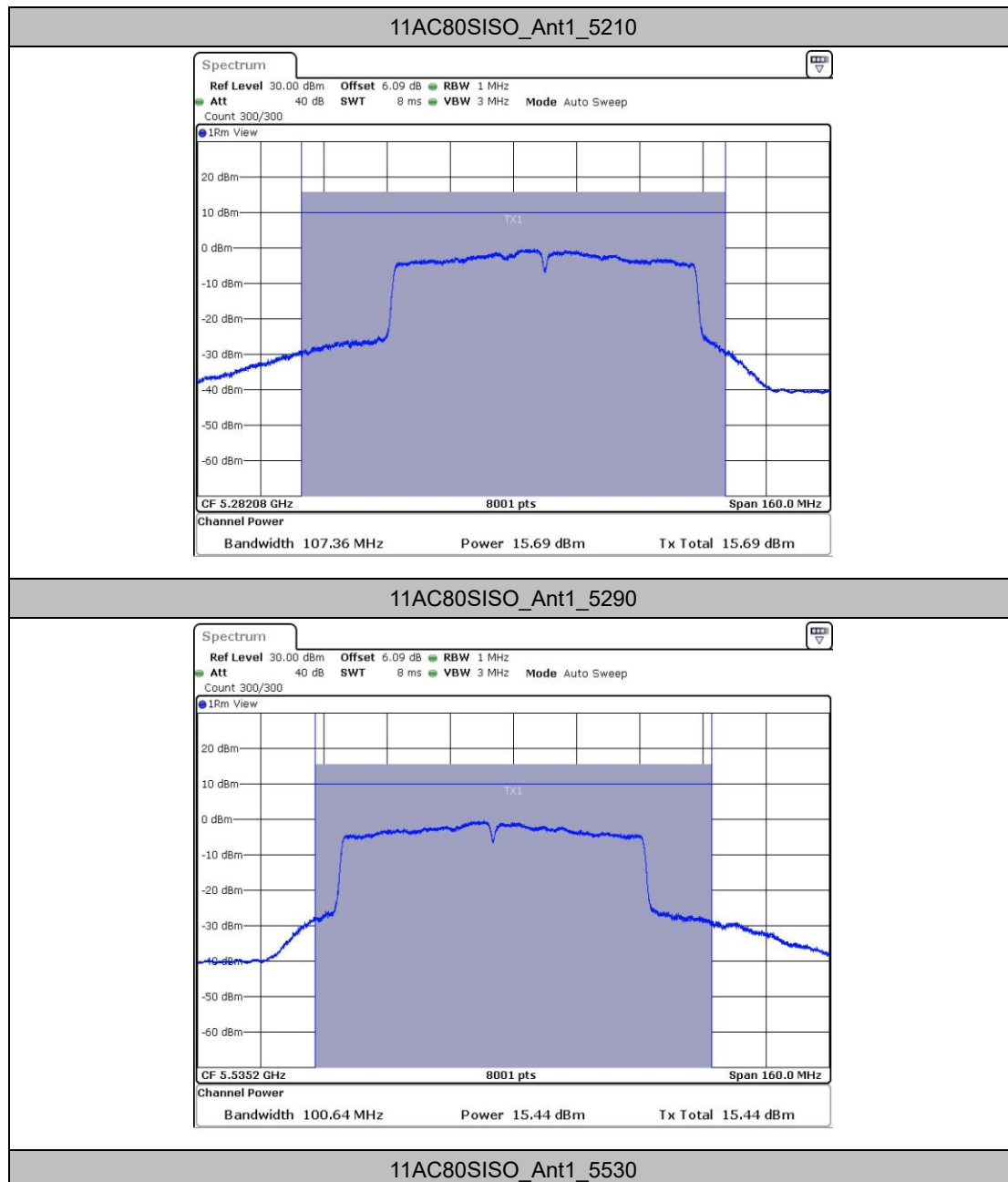


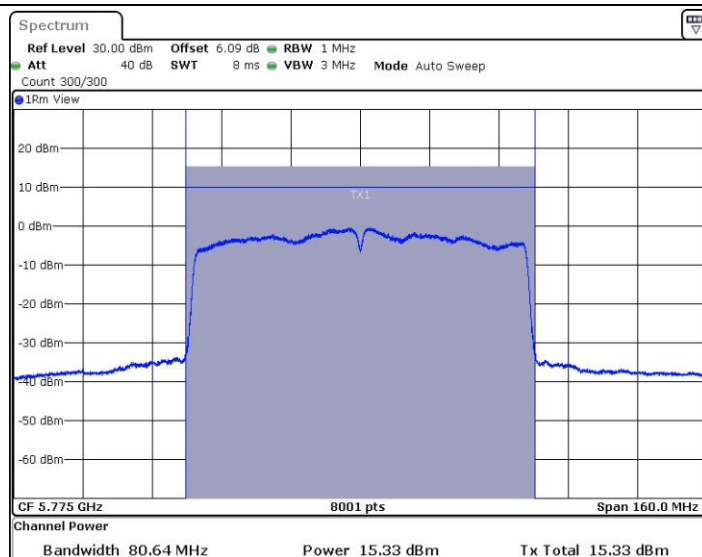
11AC40SISO_Ant1_5755



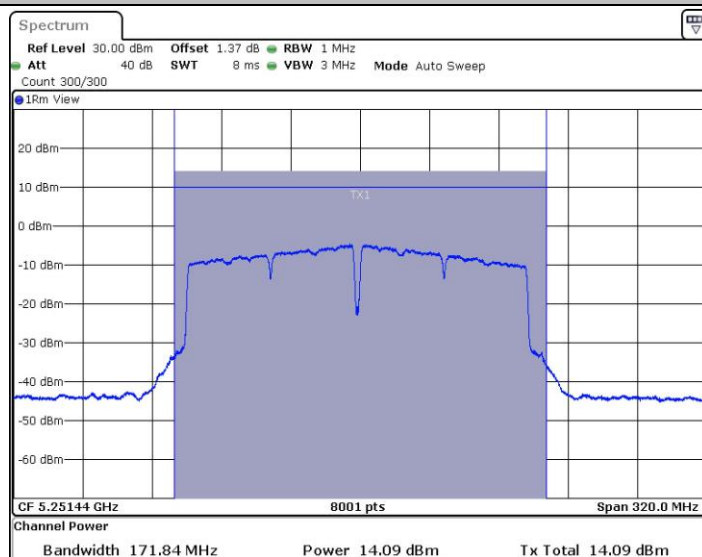
11AC40SISO_Ant1_5795



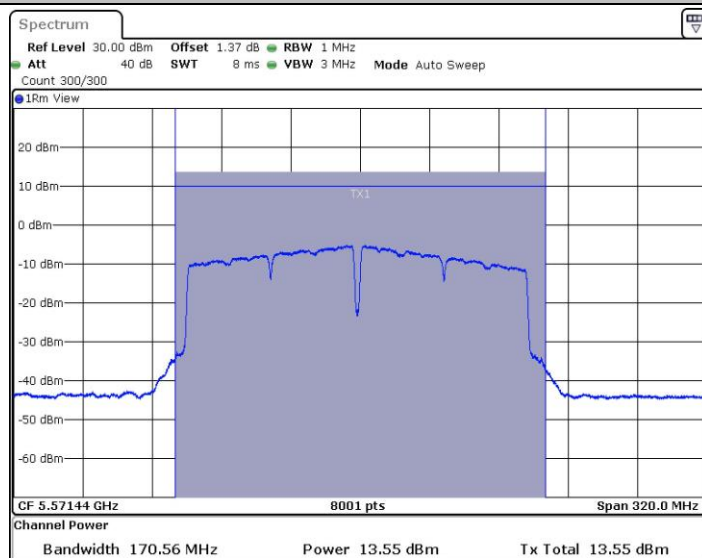


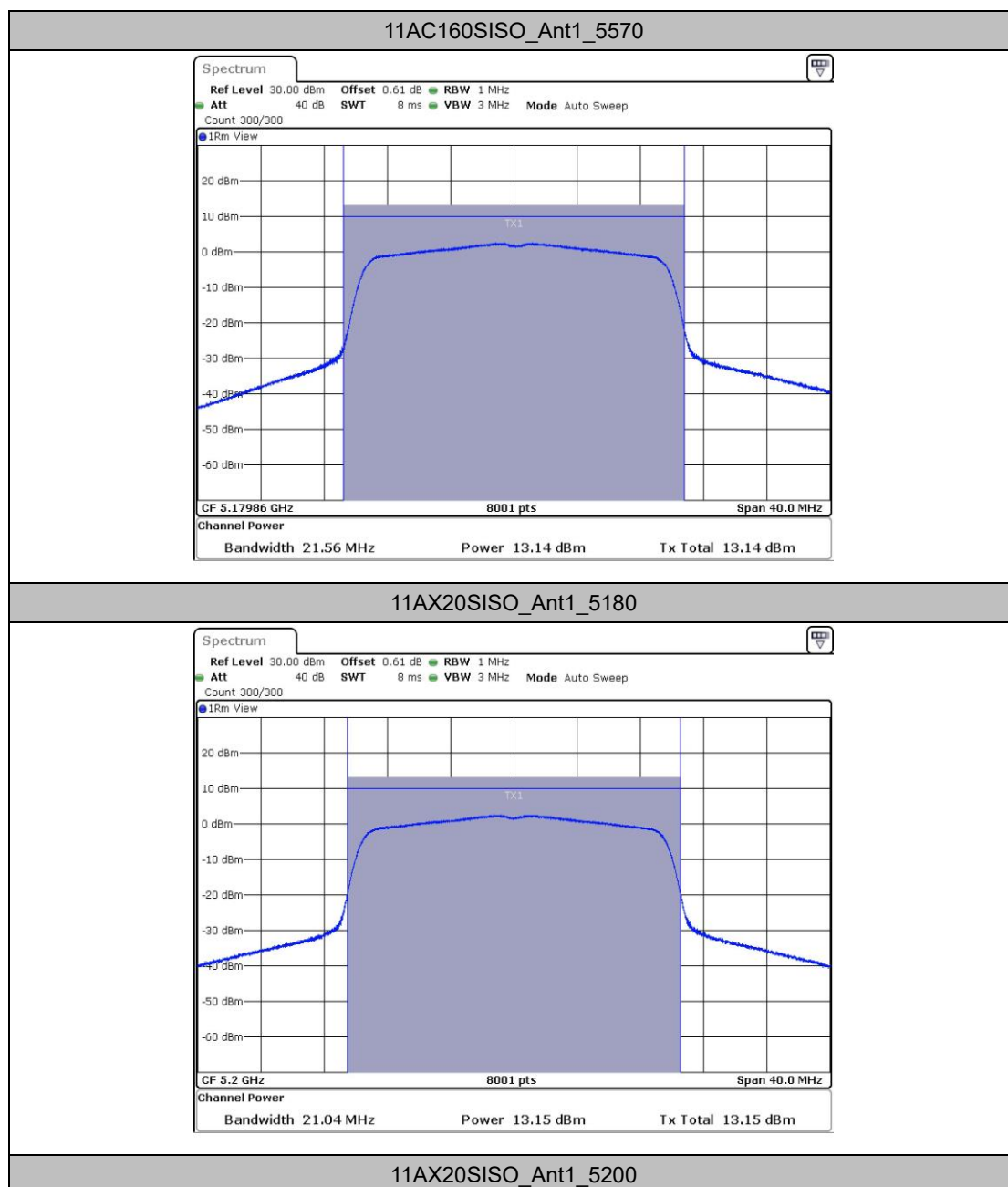


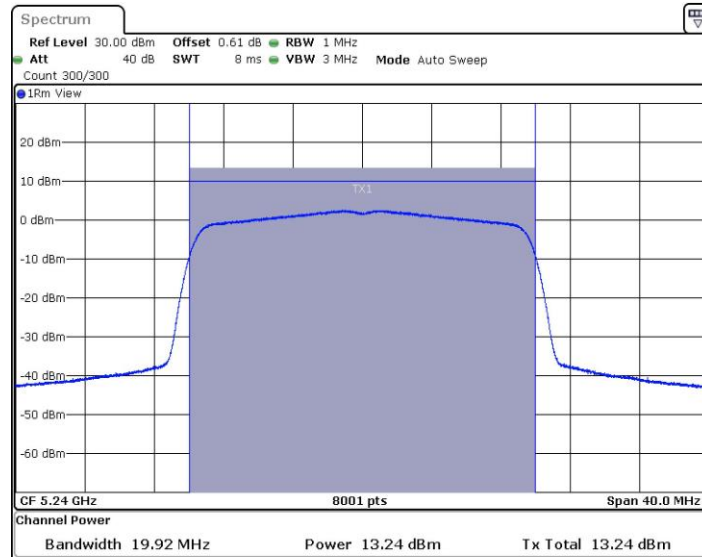
11AC80SISO_Ant1_5775



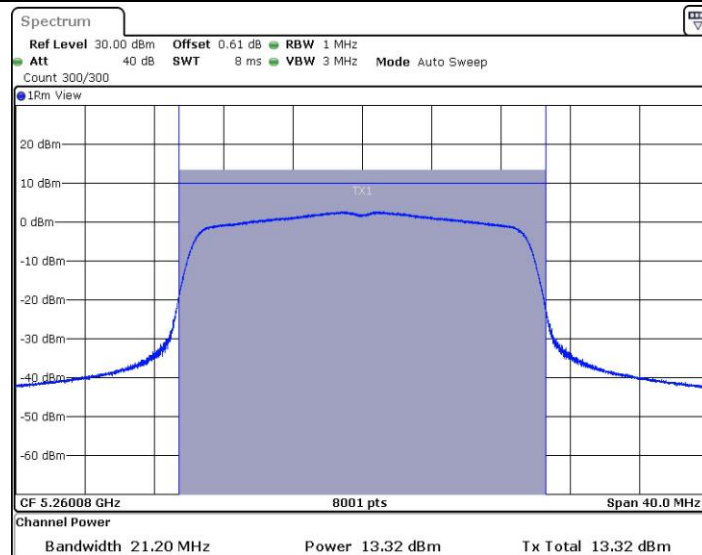
11AC160SISO_Ant1_5250



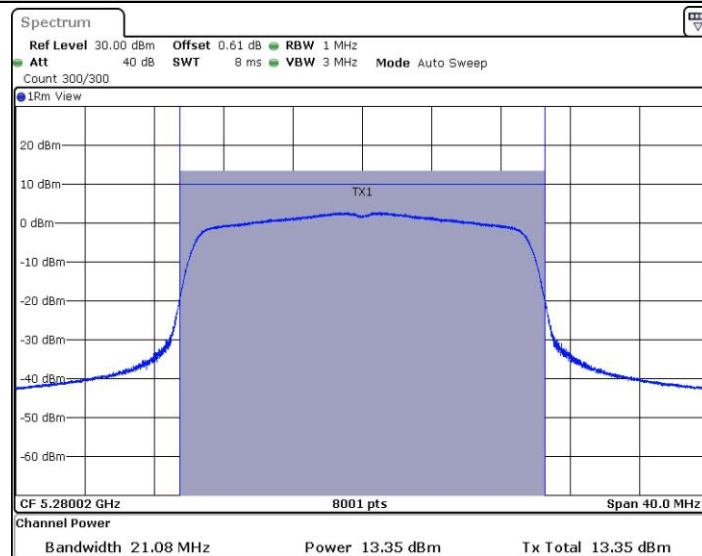


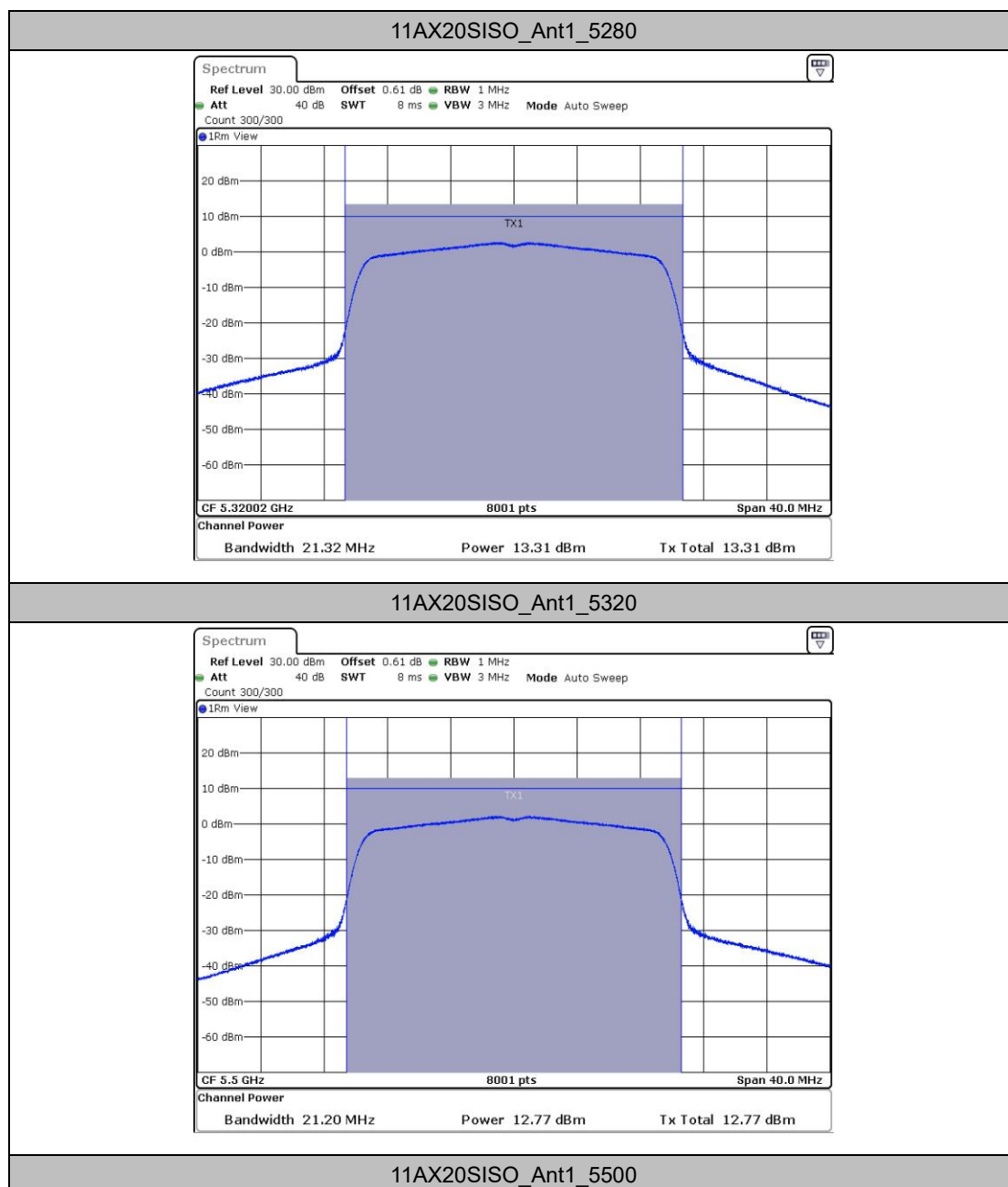


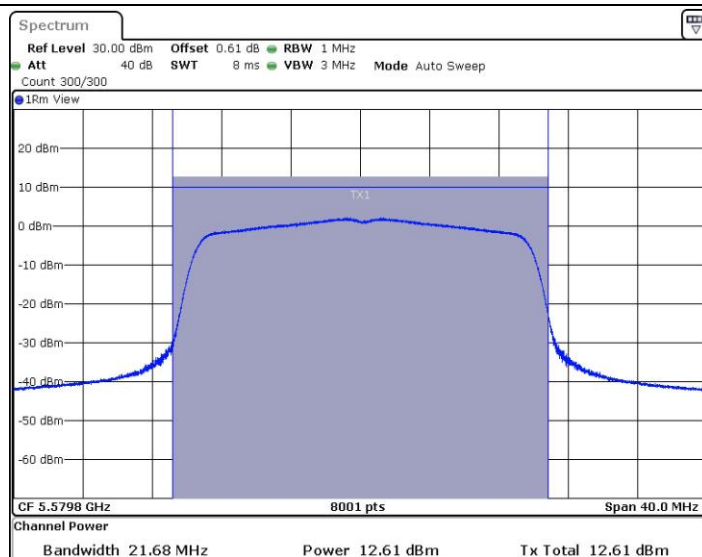
11AX20SISO_Ant1_5240



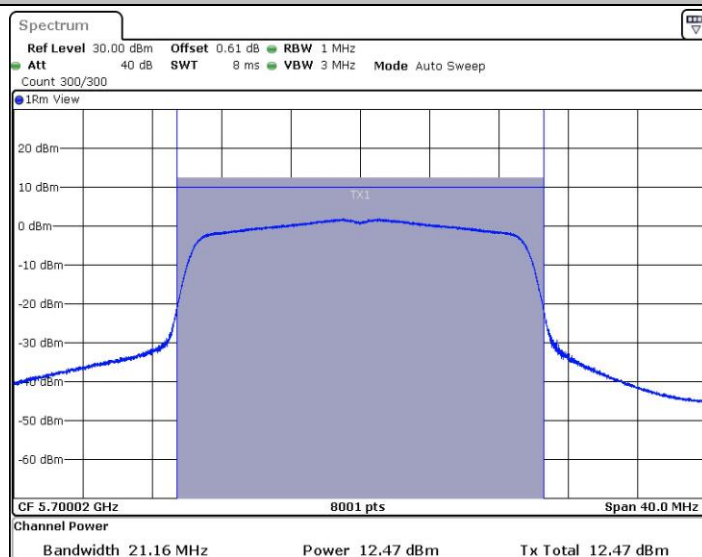
11AX20SISO_Ant1_5260



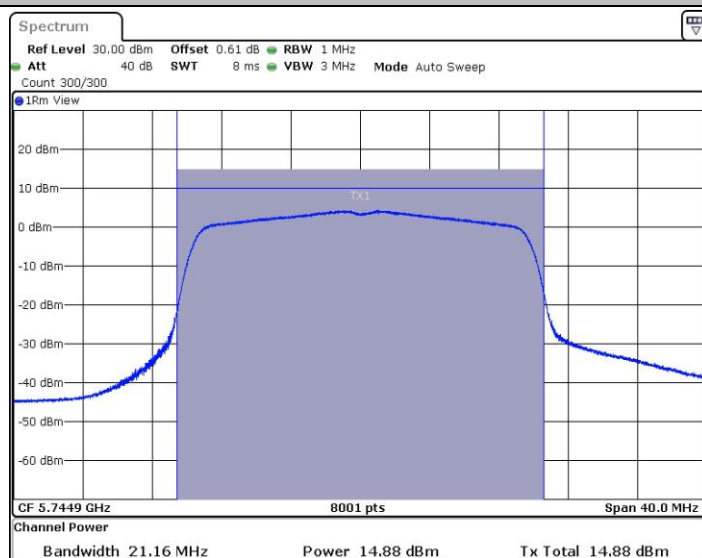


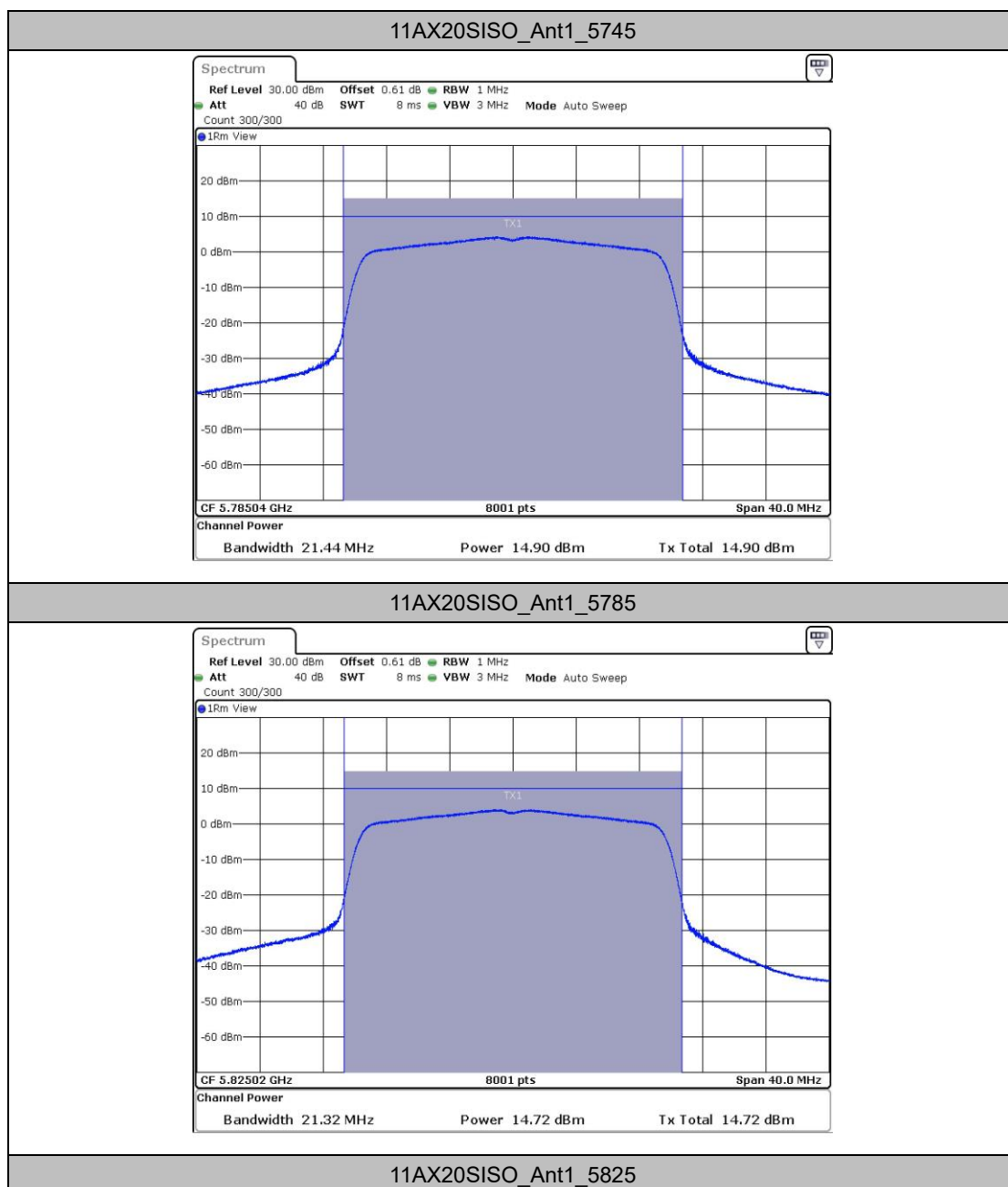


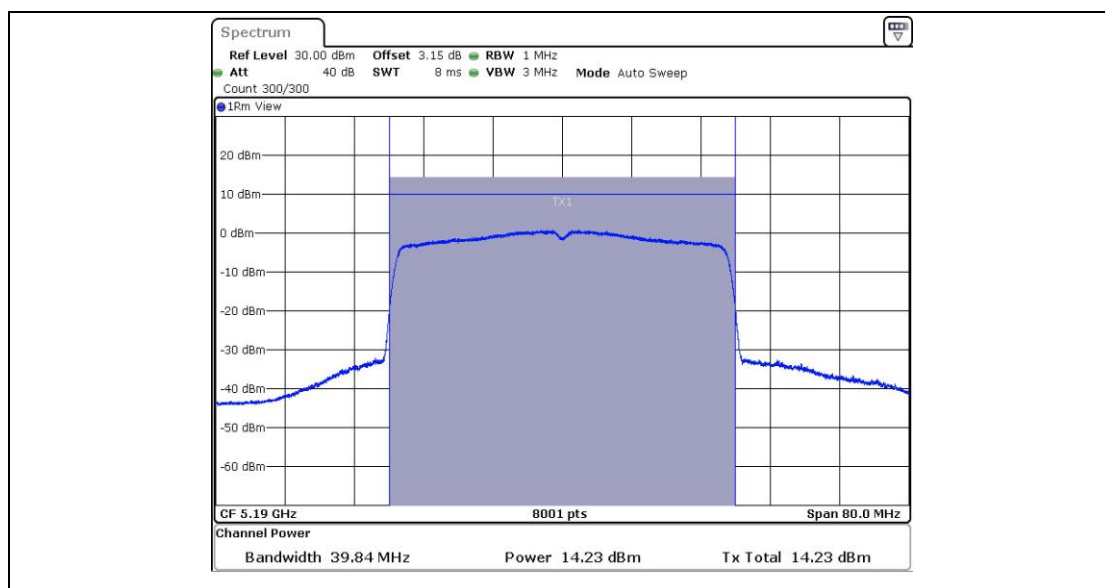
11AX20SISO_Ant1_5580



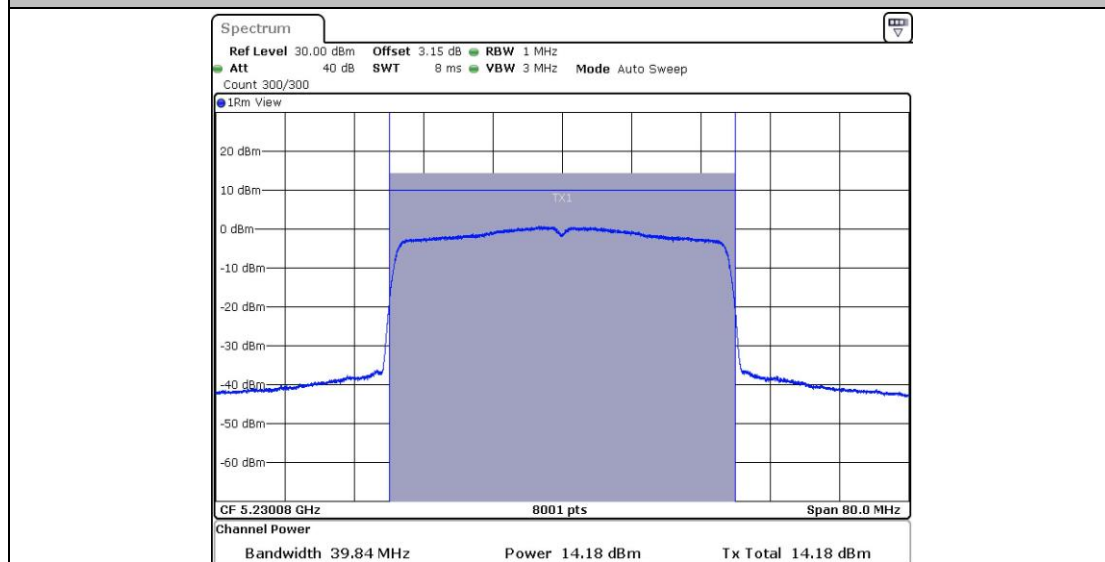
11AX20SISO_Ant1_5700



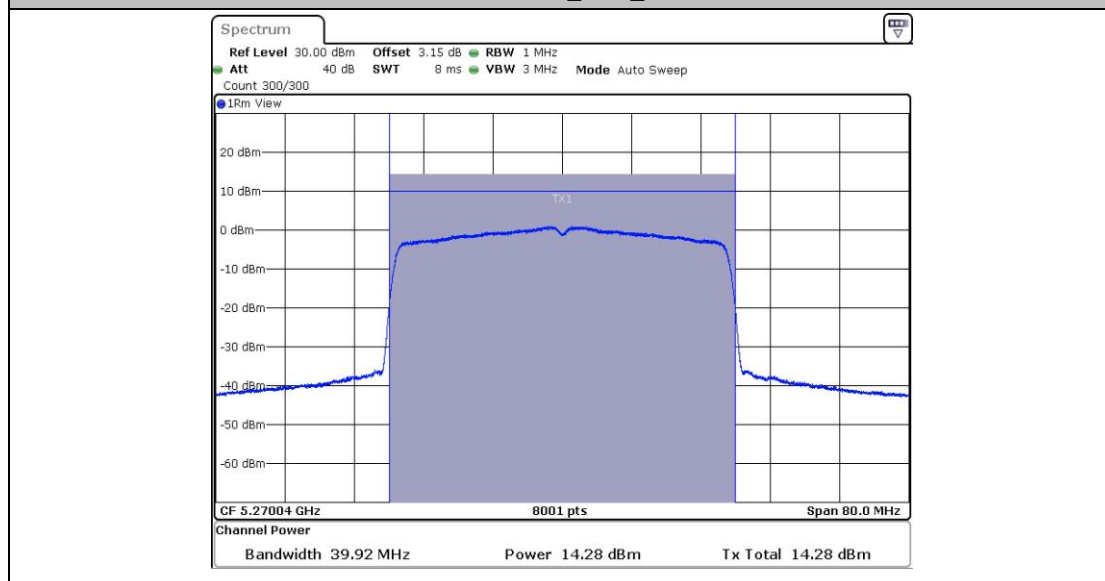


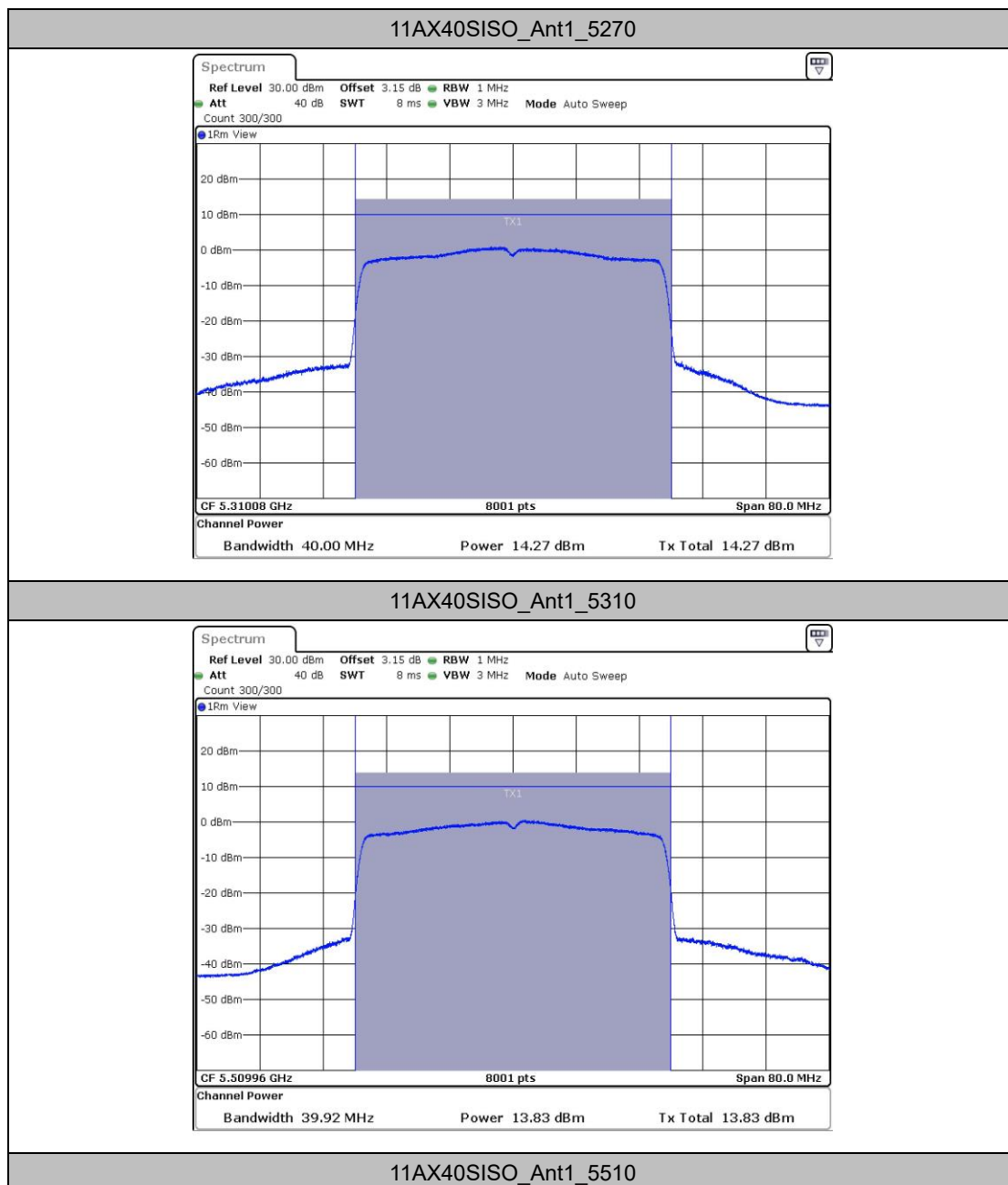


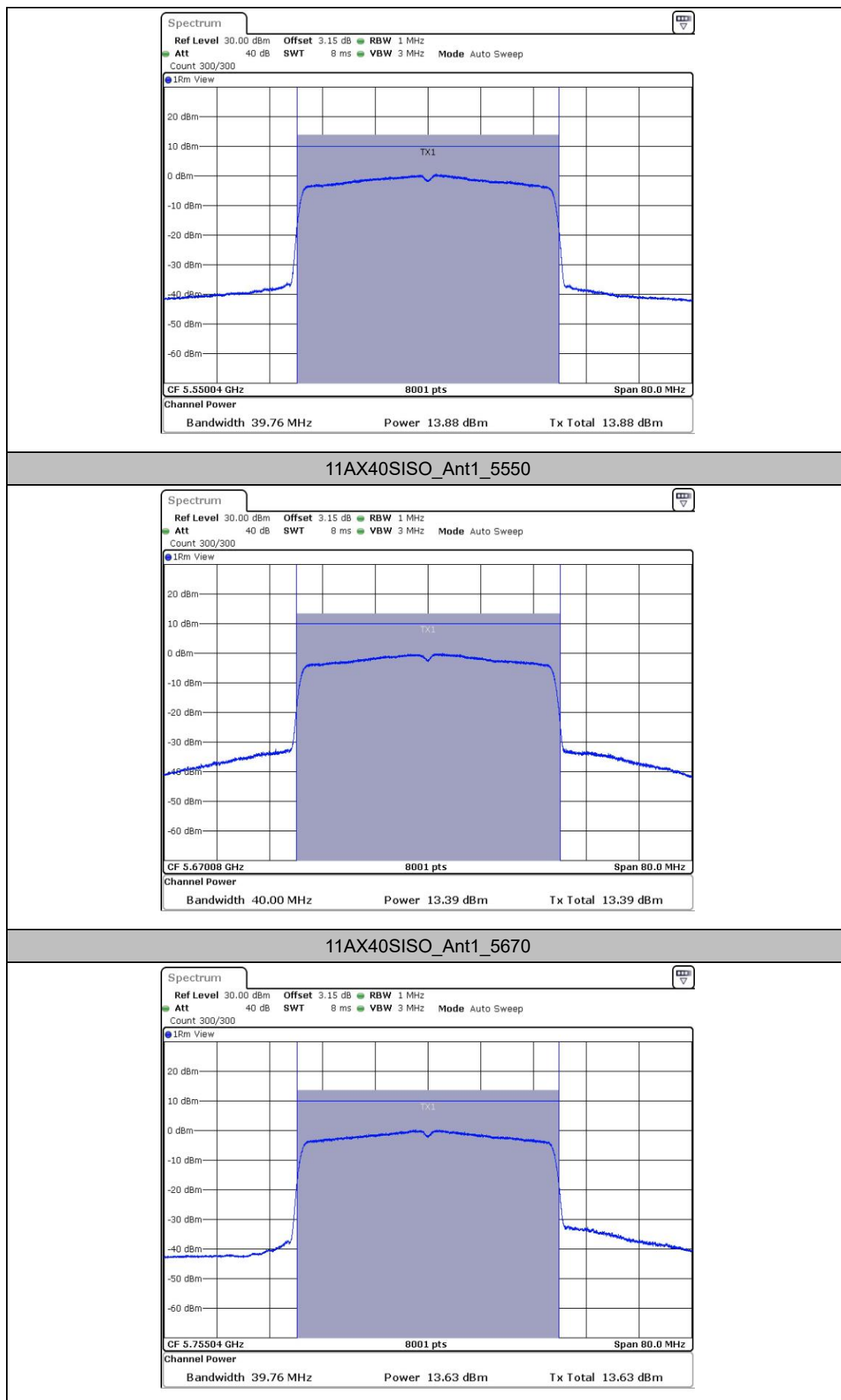
11AX40SISO_Ant1_5190

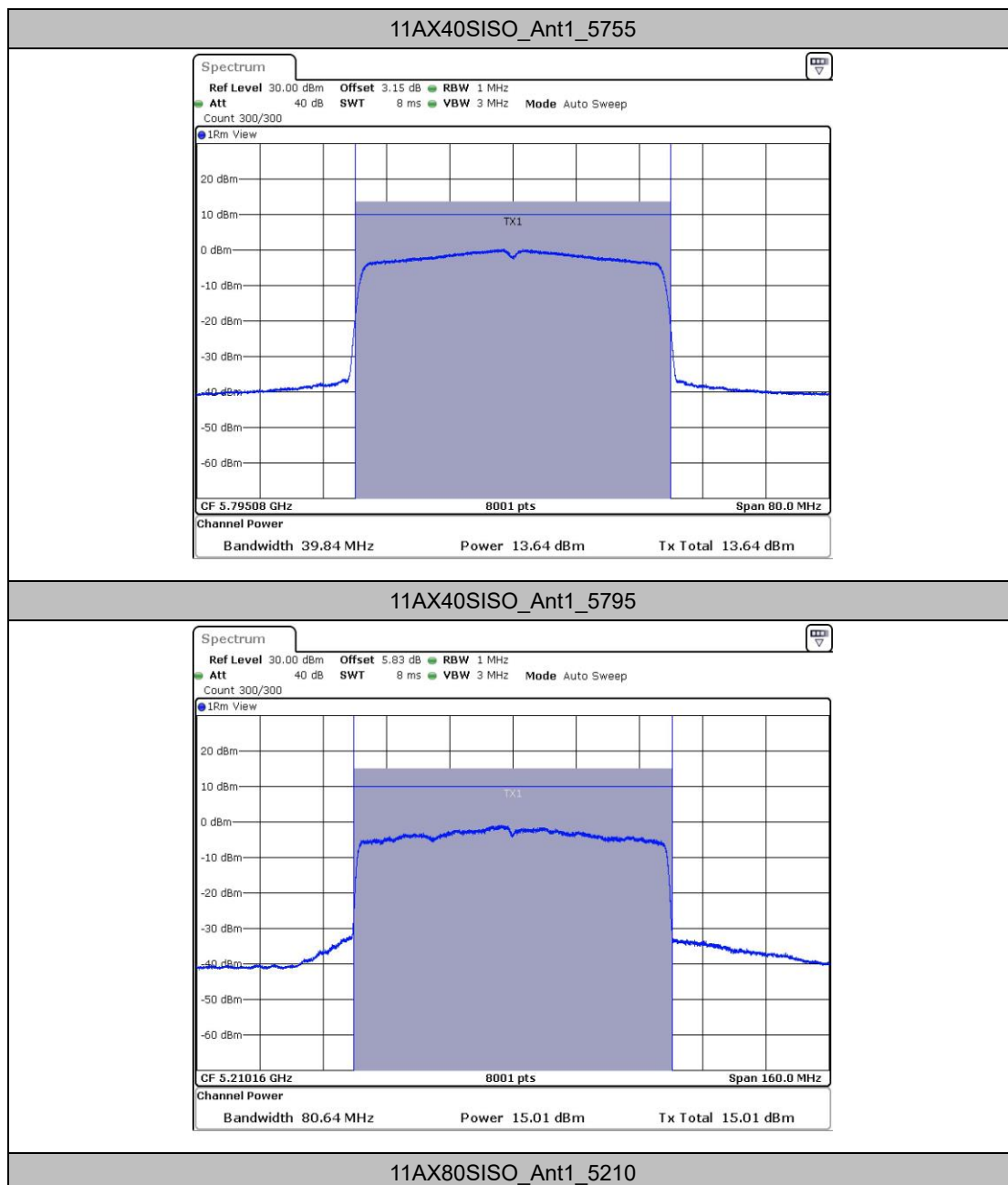


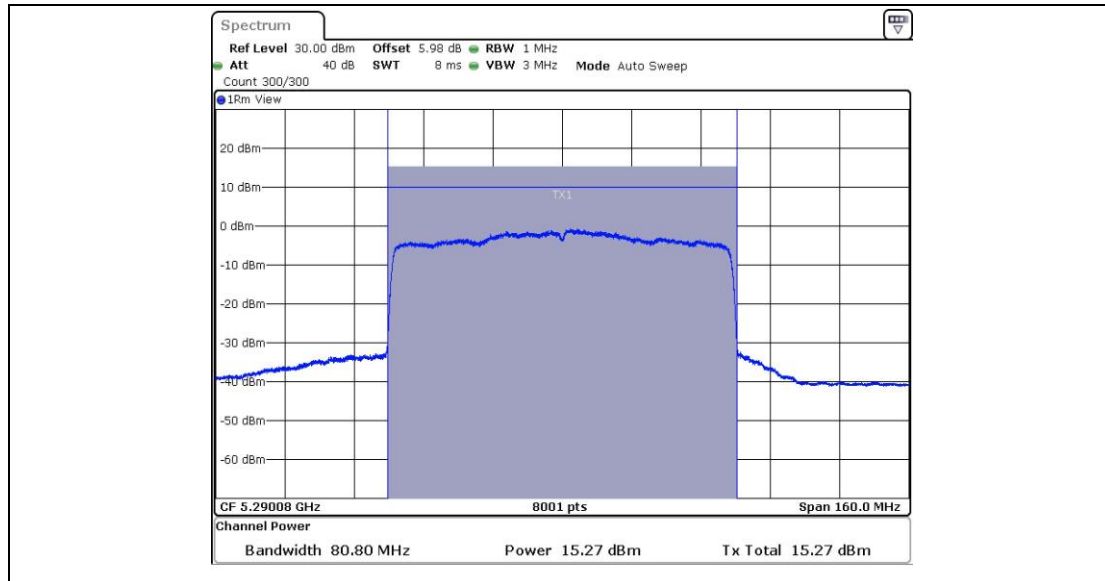
11AX40SISO_Ant1_5230



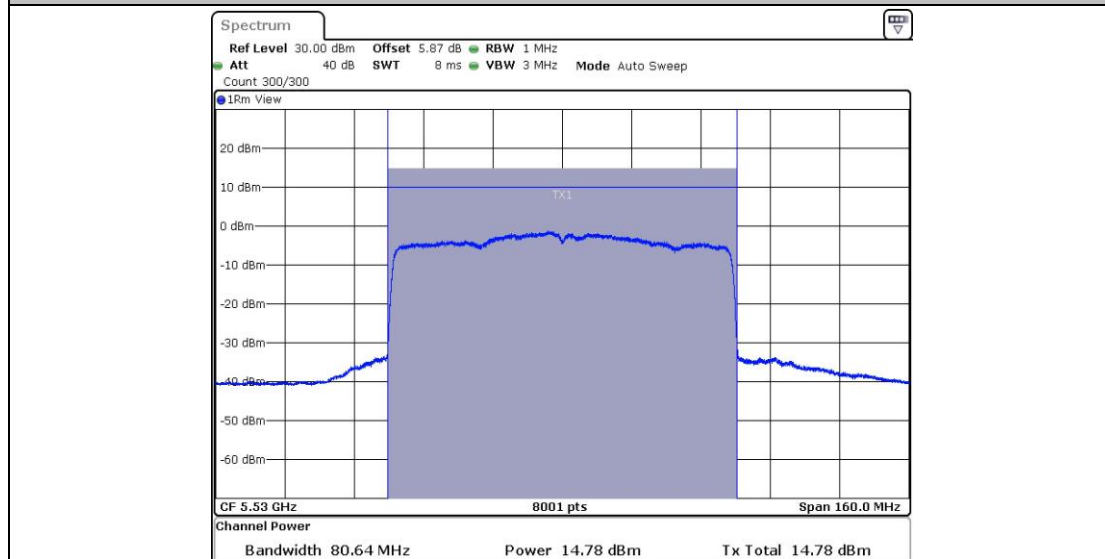




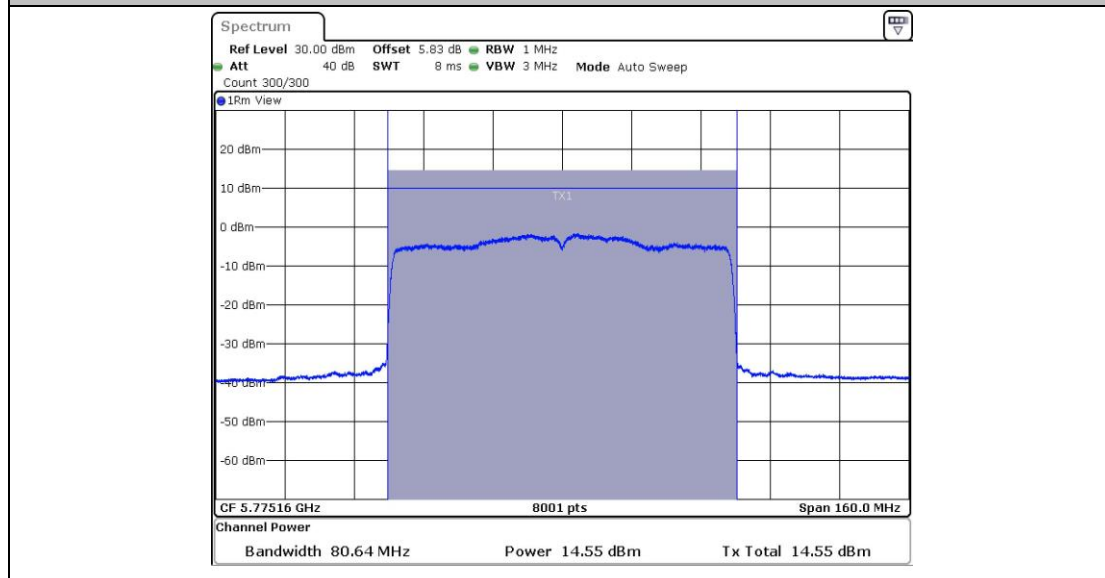


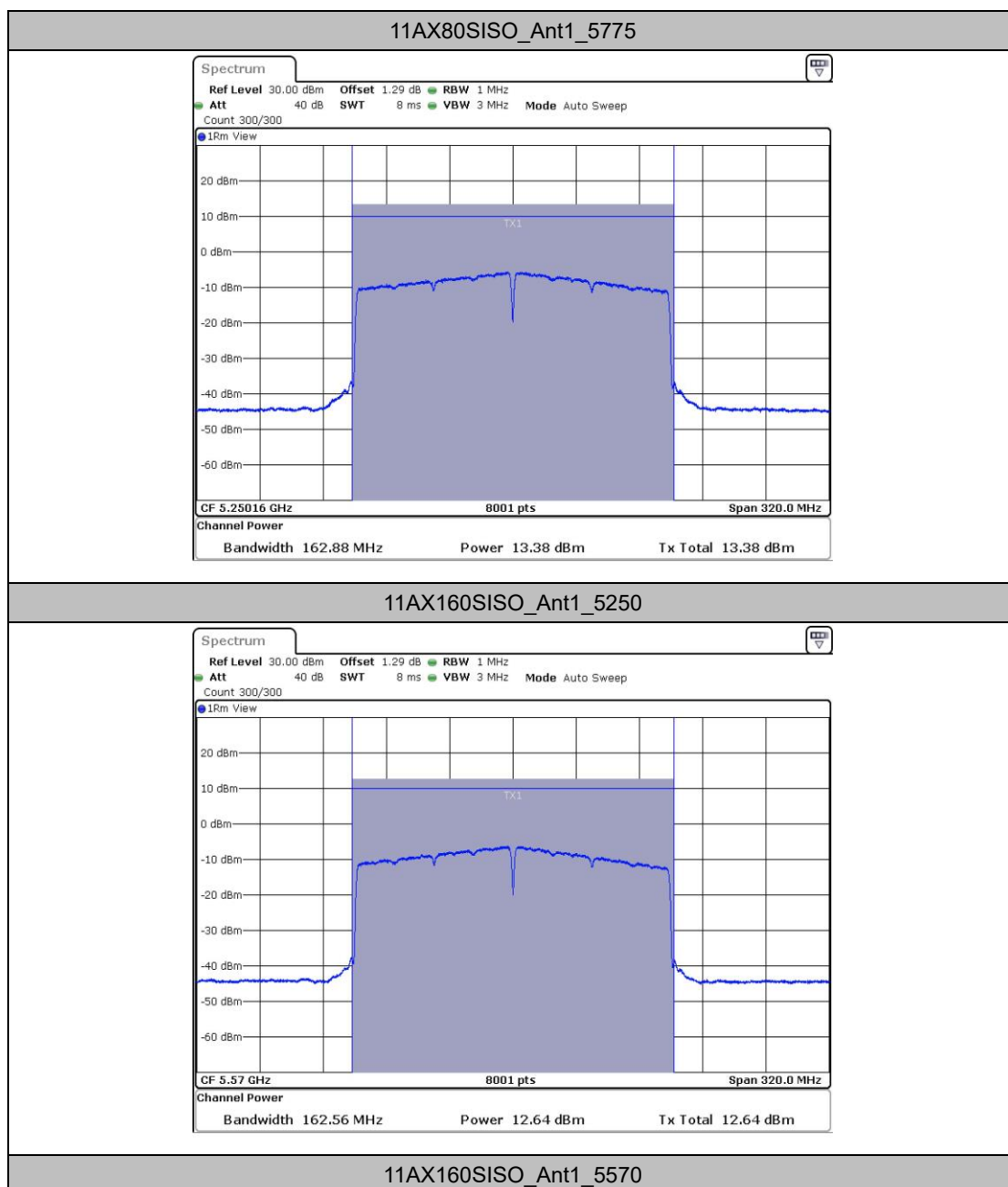


11AX80SISO_Ant1_5290



11AX80SISO_Ant1_5530





Appendix B2: Maximum EIRP

Test Result

TestMode	Antenna	Channel	Result	Limit	Verdict
11A	Ant1	5180	16.61	<=36	PASS
		5200	16.63	<=36	PASS
		5240	16.90	<=36	PASS
		5260	15.88	<=30	PASS
		5280	16.03	<=30	PASS
		5320	15.76	<=30	PASS
		5500	16.65	<=30	PASS
		5580	16.68	<=30	PASS
		5700	16.14	<=30	PASS
		5745	16.34	<=36	PASS
		5785	16.53	<=36	PASS
		5825	16.17	<=36	PASS
11N20SISO	Ant1	5180	16.73	<=36	PASS
		5200	16.69	<=36	PASS
		5240	16.82	<=36	PASS
		5260	16.96	<=30	PASS
		5280	17.00	<=30	PASS
		5320	16.85	<=30	PASS
		5500	16.46	<=30	PASS
		5580	16.42	<=30	PASS
		5700	16.09	<=30	PASS
		5745	16.81	<=36	PASS
		5785	16.49	<=36	PASS
		5825	16.12	<=36	PASS
11N40SISO	Ant1	5190	16.73	<=36	PASS
		5230	16.74	<=36	PASS
		5270	16.82	<=30	PASS
		5310	16.80	<=30	PASS
		5510	17.54	<=30	PASS
		5550	17.57	<=30	PASS
		5670	17.12	<=30	PASS
		5755	17.13	<=36	PASS
		5795	17.53	<=36	PASS
11AC20SISO	Ant1	5180	16.59	<=36	PASS
		5200	16.59	<=36	PASS
		5240	16.86	<=36	PASS
		5260	16.88	<=30	PASS
		5280	16.97	<=30	PASS

		5320	16.81	<=30	PASS
		5500	16.44	<=30	PASS
		5580	16.50	<=30	PASS
		5700	16.11	<=30	PASS
		5745	16.28	<=36	PASS
		5785	16.49	<=36	PASS
		5825	16.11	<=36	PASS
11AC40SISO	Ant1	5190	15.60	<=36	PASS
		5230	15.76	<=36	PASS
		5270	15.84	<=30	PASS
		5310	15.72	<=30	PASS
		5510	16.46	<=30	PASS
		5550	16.43	<=30	PASS
		5670	15.94	<=30	PASS
		5755	16.17	<=36	PASS
		5795	16.32	<=36	PASS
11AC80SISO	Ant1	5210	16.45	<=36	PASS
		5290	16.49	<=30	PASS
		5530	16.24	<=30	PASS
		5775	16.13	<=36	PASS
11AC160SISO	Ant1	5250	14.89	<=30	PASS
		5570	14.35	<=30	PASS
11AX20SISO	Ant1	5180	12.92	<=36	PASS
		5200	18.99	<=36	PASS
		5240	12.96	<=36	PASS
		5260	18.29	<=30	PASS
		5280	12.11	<=30	PASS
		5320	18.19	<=30	PASS
		5500	12.91	<=30	PASS
		5580	18.99	<=30	PASS
		5700	12.13	<=30	PASS
		5745	23.49	<=36	PASS
		5785	17.61	<=36	PASS
		5825	24.29	<=36	PASS
11AX40SISO	Ant1	5190	15.03	<=36	PASS
		5230	14.98	<=36	PASS
		5270	15.08	<=30	PASS
		5310	15.07	<=30	PASS
		5510	14.63	<=30	PASS
		5550	14.68	<=30	PASS
		5670	14.19	<=30	PASS
		5755	14.43	<=36	PASS
		5795	14.44	<=36	PASS

11AX80SISO	Ant1	5210	15.81	<=36	PASS
		5290	16.07	<=30	PASS
		5530	15.58	<=30	PASS
		5775	15.35	<=36	PASS
11AX160SISO	Ant1	5250	14.18	<=30	PASS
		5570	13.44	<=30	PASS

Note: The Duty Cycle Factor is compensated in the graph.

Appendix C: Maximum power spectral density

Test Result

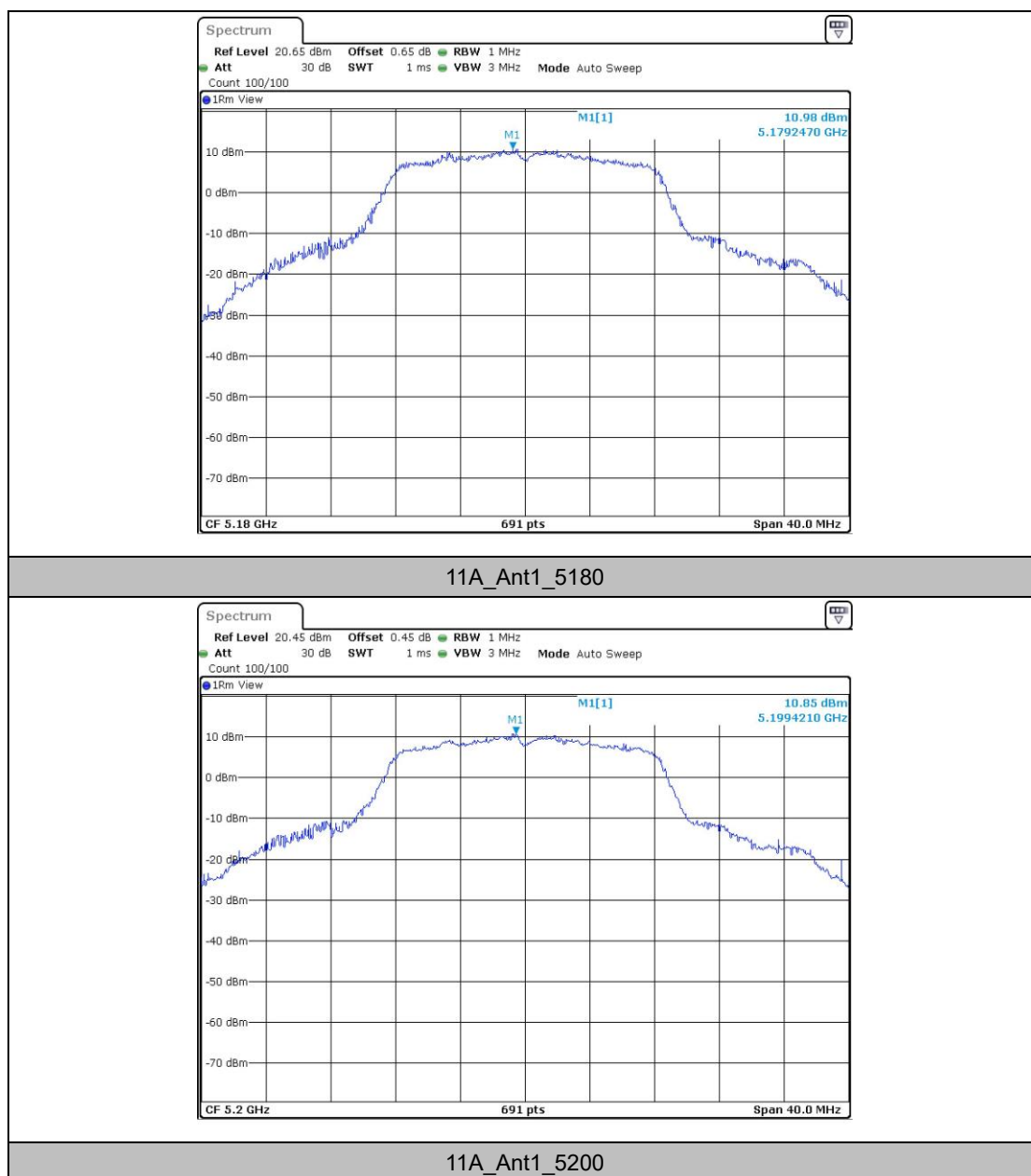
TestMode	Antenna	Channel	Result	Limit	Verdict
11A	Ant1	5180	10.98	<=11	PASS
		5200	10.85	<=11	PASS
		5240	10.59	<=11	PASS
		5260	9.83	<=11	PASS
		5280	10.29	<=11	PASS
		5320	10.37	<=11	PASS
		5500	10.98	<=11	PASS
		5580	10.91	<=11	PASS
		5700	10.52	<=11	PASS
		5745	9.3	<=30	PASS
		5785	9.57	<=30	PASS
		5825	9.48	<=30	PASS
11N20SISO	Ant1	5180	10.47	<=11	PASS
		5200	10.36	<=11	PASS
		5240	10.19	<=11	PASS
		5260	10.65	<=11	PASS
		5280	10.68	<=11	PASS
		5320	10.62	<=11	PASS
		5500	10.49	<=11	PASS
		5580	10.3	<=11	PASS
		5700	10.03	<=11	PASS
		5745	9.09	<=30	PASS
		5785	8.87	<=30	PASS
		5825	8.63	<=30	PASS
11N40SISO	Ant1	5190	10.03	<=11	PASS
		5230	9.46	<=11	PASS
		5270	9.98	<=11	PASS
		5310	9.99	<=11	PASS
		5510	10.25	<=11	PASS
		5550	10.61	<=11	PASS

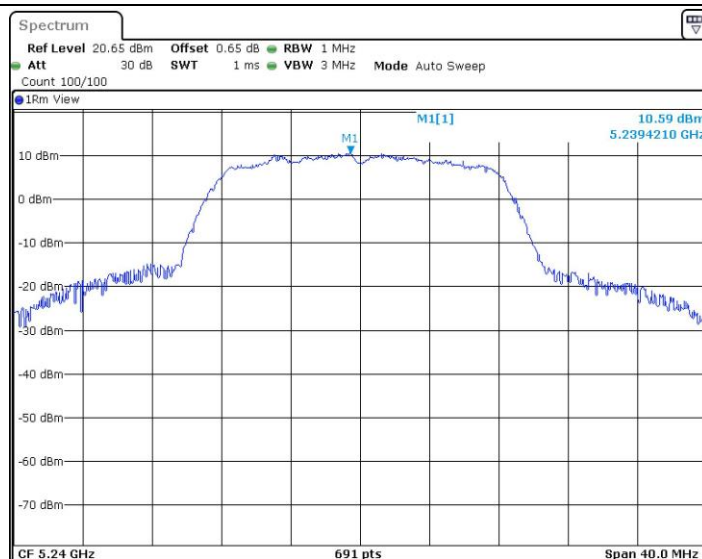
		5670	10.02	<=11	PASS
		5755	8.14	<=30	PASS
		5795	6.45	<=30	PASS
11AC20SISO	Ant1	5180	10.5	<=11	PASS
		5200	10.47	<=11	PASS
		5240	10.3	<=11	PASS
		5260	10.8	<=11	PASS
		5280	10.62	<=11	PASS
		5320	10.71	<=11	PASS
		5500	10.14	<=11	PASS
		5580	10.26	<=11	PASS
		5700	10.22	<=11	PASS
		5745	8.96	<=30	PASS
		5785	8.87	<=30	PASS
		5825	8.76	<=30	PASS
11AC40SISO	Ant1	5190	8.67	<=11	PASS
		5230	8.5	<=11	PASS
		5270	8.81	<=11	PASS
		5310	8.4	<=11	PASS
		5510	9.61	<=11	PASS
		5550	9.62	<=11	PASS
		5670	9.61	<=11	PASS
		5755	7.95	<=30	PASS
		5795	7.68	<=30	PASS
11AC80SISO	Ant1	5210	9.01	<=11	PASS
		5290	10.02	<=11	PASS
		5530	9.59	<=11	PASS
		5775	7.95	<=30	PASS
11AC160SISO	Ant1	5250	0.24	<=11	PASS
		5570	-0.21	<=11	PASS
11AX20SISO	Ant1	5180	10.26	<=11	PASS
		5200	10.8	<=11	PASS
		5240	9.76	<=11	PASS
		5260	10.52	<=11	PASS
		5280	10.6	<=11	PASS
		5320	10	<=11	PASS
		5500	9.57	<=11	PASS
		5580	9.66	<=11	PASS
		5700	9.79	<=11	PASS
		5745	9.95	<=30	PASS
		5785	9.55	<=30	PASS
		5825	9.83	<=30	PASS
11AX40SISO	Ant1	5190	10.11	<=11	PASS

		5230	10.71	<=11	PASS
		5270	10.76	<=11	PASS
		5310	10.32	<=11	PASS
		5510	10.88	<=11	PASS
		5550	9.53	<=11	PASS
		5670	10.16	<=11	PASS
		5755	8.38	<=30	PASS
		5795	7.56	<=30	PASS
11AX80SISO	Ant1	5210	9.61	<=11	PASS
		5290	10.8	<=11	PASS
		5530	9.83	<=11	PASS
		5775	7.98	<=30	PASS
11AX160SISO	Ant1	5250	0.91	<=11	PASS
		5570	1.19	<=11	PASS

Note: The Duty Cycle Factor is compensated in the graph.

Test Graphs





11A_Ant1_5240



11A_Ant1_5260

