LT102V2 Shielding Strategy

Introduction

This document illustrates the shielding strategy adopted for the LT102V2 device.

According to https://transition.fcc.gov/oet/ea/presentations/files/oct16/23-Equipment-Authorization-Modular-Devices-101216-JS.pdf , the shield is required to "prevent (near field) coupling between the RF circuitry and any y wires or circuits (traces) on the host. "

In the LT102V2, the shield is realized by the conductive silicon layer which is on top of the RF circuit. In detail the WLCSP technology is exploited to "embed" the active devices of the RF section in between board ground and the above-mentioned conductive layer. As demonstrated by means of full 3D EM Simulations, we demonstrate that the shielding of LT102V2 makes the requirement of an extra shielding redundant and useless.

WLCSP Technology

WLCSP technology is a "package-less" where "under-bumps" (UBM, Under Bump Metallization) are used to solder the chip to the PCB

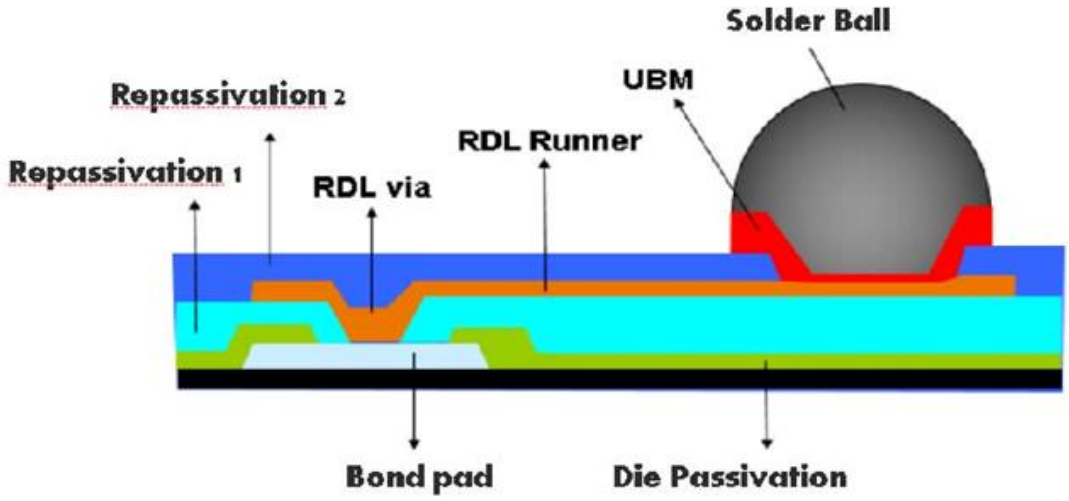

Figure 1 Cross Section of a WLCSP Integrated Circuit

1. Therefore, w.r.t. normal packaging techniques, the chip is actually flipped. This means that silicon substrate is "far" from the host board while silicon metal layers are close to the PCB and its ground plane.
2. This is the opposite w.r.t. normal packaging where silicon substrate is close to the PCB while on-chip metal layers are

When mounted on top of a Printed Circuit Board, the resulting stack-up is as follows.

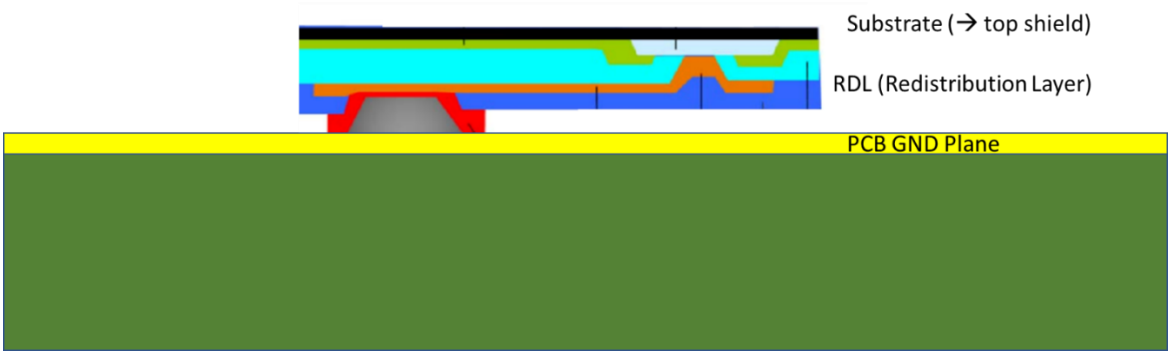

Figure 2 WLCSP Integrated Circuit Mounted on top of a PCB

Normal Packaging

While a normal package is depicted below

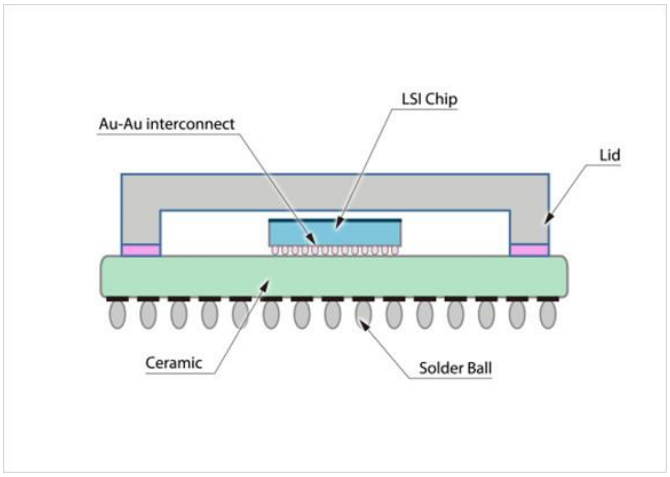

Figure 3 Normal IC Packaging

In “normal” packaging the silicon layer is in-between the active devices (transistors, inductors etc.) which are part of the Integrated Circuit.

As a result, they “lie” on top of the circuit: In normal packaging, no shielding is therefore available in this case.

Substrate as conductive layer

In LT102V2, all integrated devices which are part of the RF circuit are in between PCB ground and the substrate which contains few undoped areas (all integrated devices require a solid connection either to ground or power supply and this is realized by highly conductive doped areas).

In LT102V2 we exploit the WLCSP “flip-chip”, along with substrate doping to act as a shield.

While undoped silicon is a poor conductor (making it a poor shield), CMOS processes uses two different doping options (NDIFF, PDIFF) which make the silicon substrate a very good conductor.

For reference, the silicon process used for the LT102V2 front-end shows the following parameters (approx.):

Undoped silicon	1e-3 S/m
PDIFF	7e6 S/m
NDIFF	11e3 S/m

Sides

With respect of the "sides" of the devices, the RF integrated circuit is 0.7mm thick. Operating at maximum 8.5GHz frequency (wavelength=35.3mm), this corresponds to an aperture = 0.0198 λ.

Demonstration of the shielding properties

The effectiveness of the shielding strategy is demonstrated by means of EM Simulations. Given the requirement of preventing near-field interactions, the electric/magnetic field is evaluated with "near-field" sensors placed all over the integrated circuit. No far-field sensor is considered as all spurious radiation properties have been already verified in the anechoic chamber (see attached test reports).

To allow for a feasible EM model (i.e. a simulation with all the geometries inside the IC would be undoable given the size of the resulting mesh) we have modeled a resonating LC tank whose resonating frequency is @7.8GHz, inside the operating bandwidth of the device. The LC resonating tank is selected to maximize currents and magnetic fields, in order to highlight the effectiveness of the shielding.

Simulations are done by means of Keysight EmPRO 2022 (*Cyndaquil*). Simulation type: FEM. Conductor modeled as surface impedances. Solver SDS with mixed 1^{st} / 2^{nd} order basis. Adaptive meshing with max error on S-Params = 0.03 is enforced.

Near-fields are extracted at chip surfaces. To demonstrate the effectiveness of the shielding strategy, in the following tests are performed:

1. "Floating Chip": no shield is provided either at top / bottom level;
2. "Normal Packaging": LC tank is on top of the PCB-Substrate-BEOL (BackEnd Of Line);
3. "LT102V2: LC tank is in-between substrate and PCB ground;
4. Shield: the LC tank is shielded by a commercial shield

The 3D EM models are reported in the next pictures.

Description of the EM (electromagnetics models) and simulations

The 3D model of the LC tank is reported in the next picture.

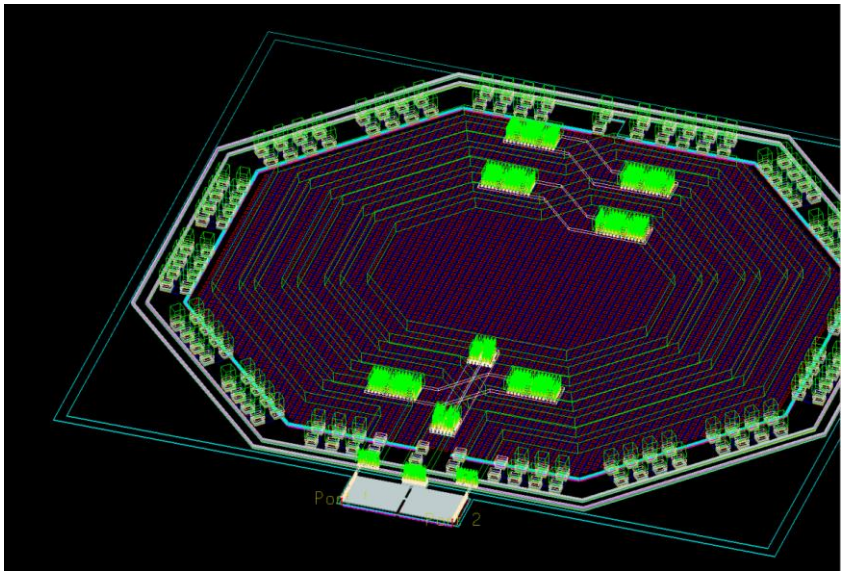

Figure 4 Detail on the active RF circuit

Physical details of the substrate and of metal interconnections are extracted by the foundry PDK (Process Development Kit).

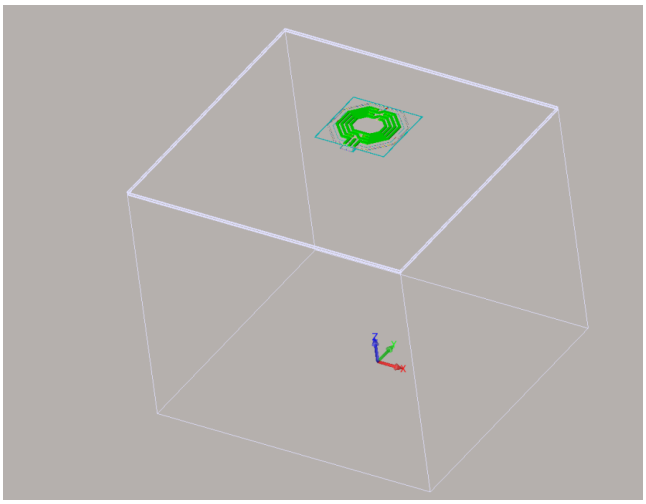

Figure 5 EM Model for the “floating chip”

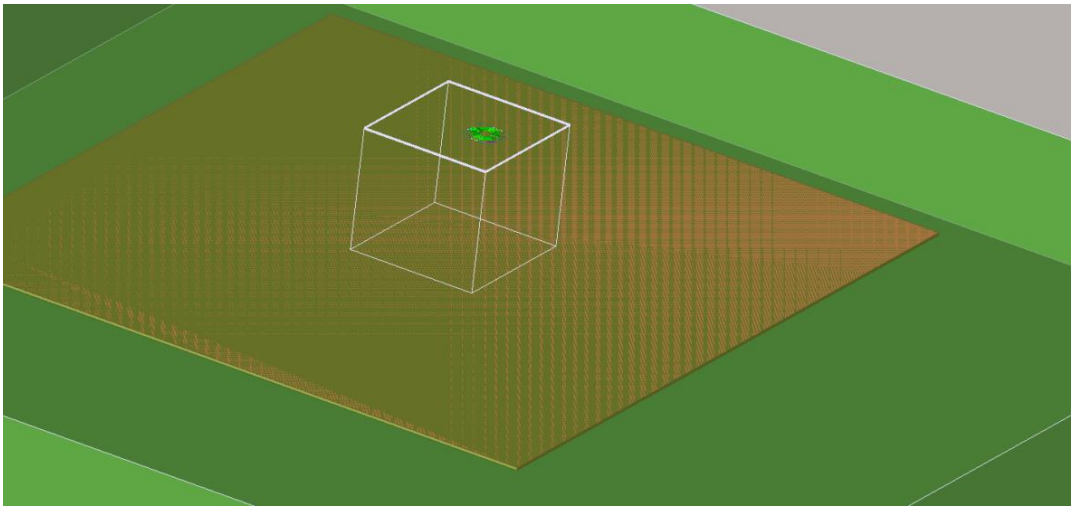

Figure 6 EM Model for the active Circuit in the "normal packaging scheme"

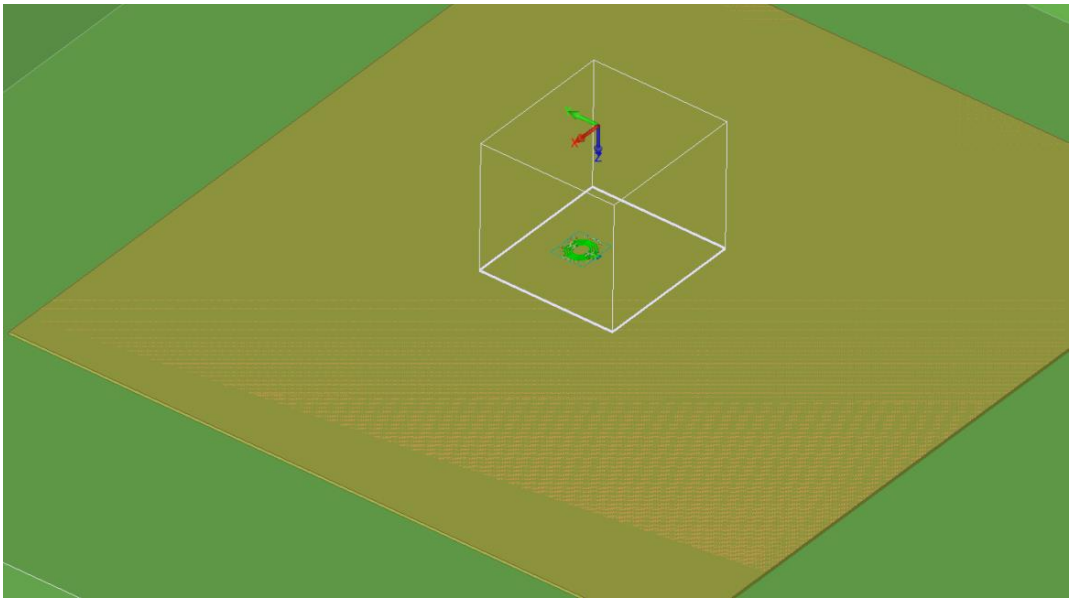

Figure 7 EM Model for the active Circuit in the LT102V2

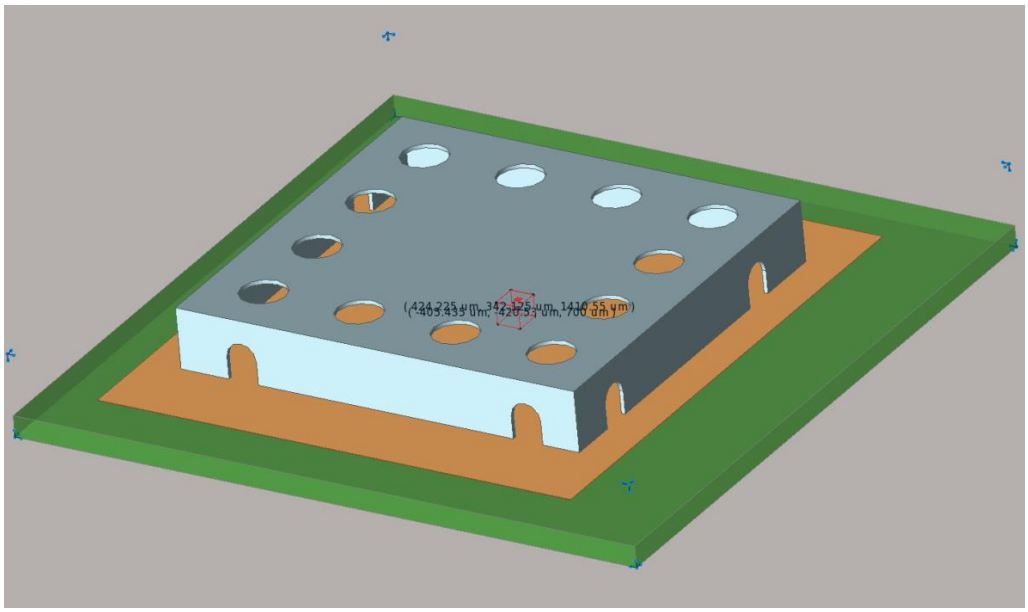

Figure 8 EM Model for the normal package + shield

Results: Fields on Surfaces

Case 1.: Floating Chip

Surface currents are shown in the next pictures.

Top Face

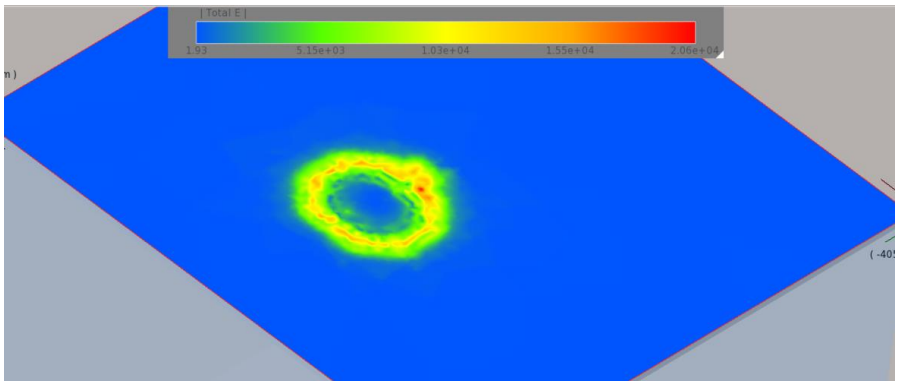

Figure 9 Surface E-Field Magnitude at top of the chip (BEOL side) for the unshielded case

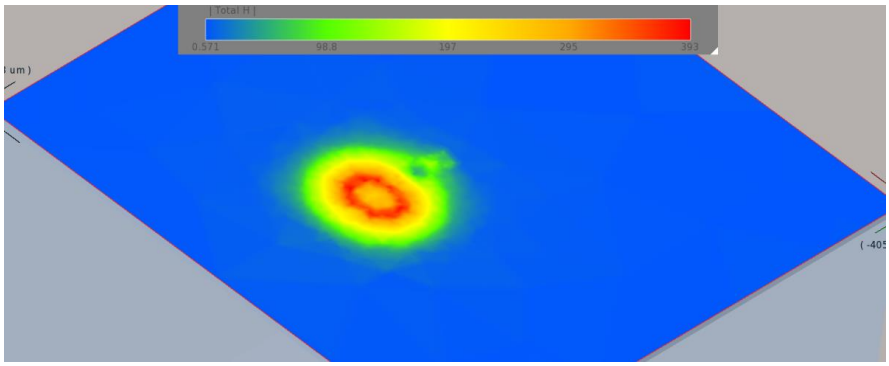

Figure 10 Surface H-Field Magnitude at top passivation layer for the unshielded case

Sides

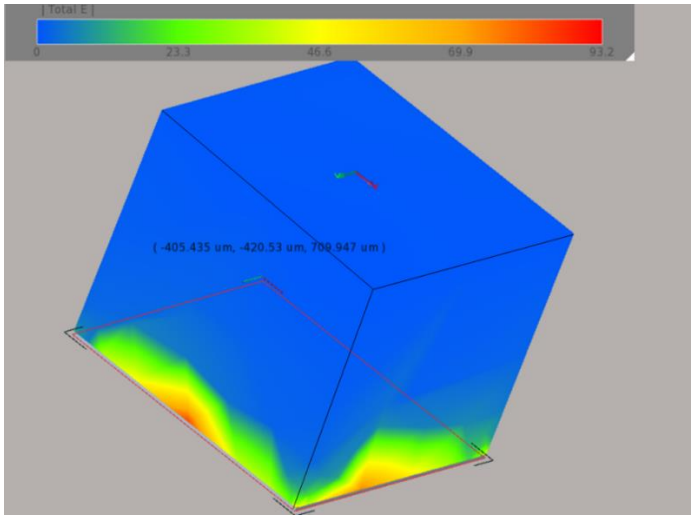

Figure 11 Surface E-Field Magnitude at chip sides for the unshielded case

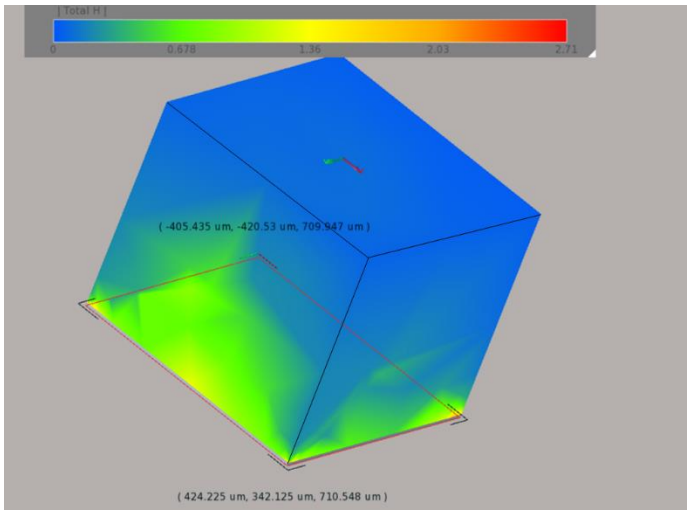

Figure 12 Surface H-Field Magnitude at chip sides for the unshielded case

Case 2: Normal Packaging

Top Face

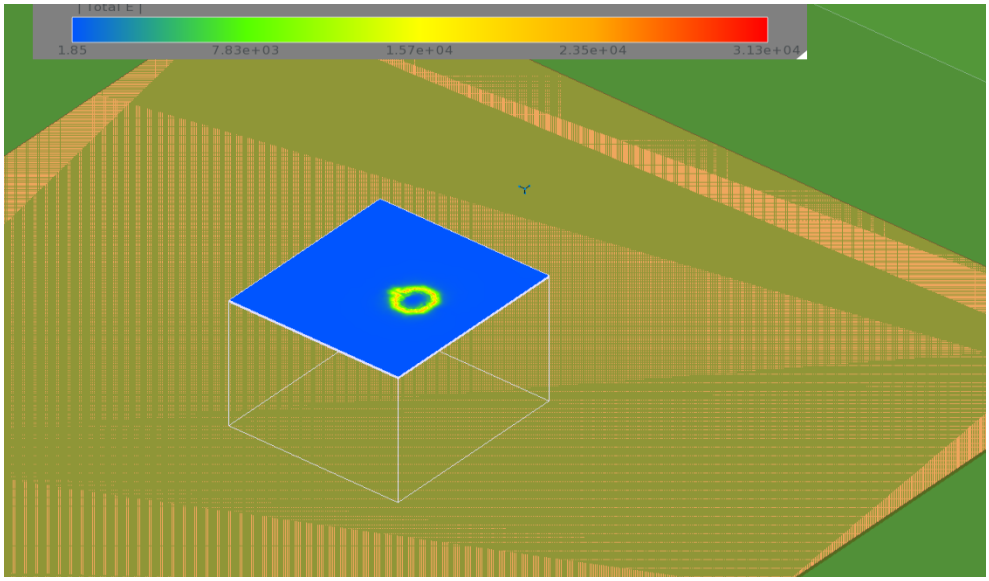

Figure 13 Surface E-Field Magnitude at top of the chip for normal packaging

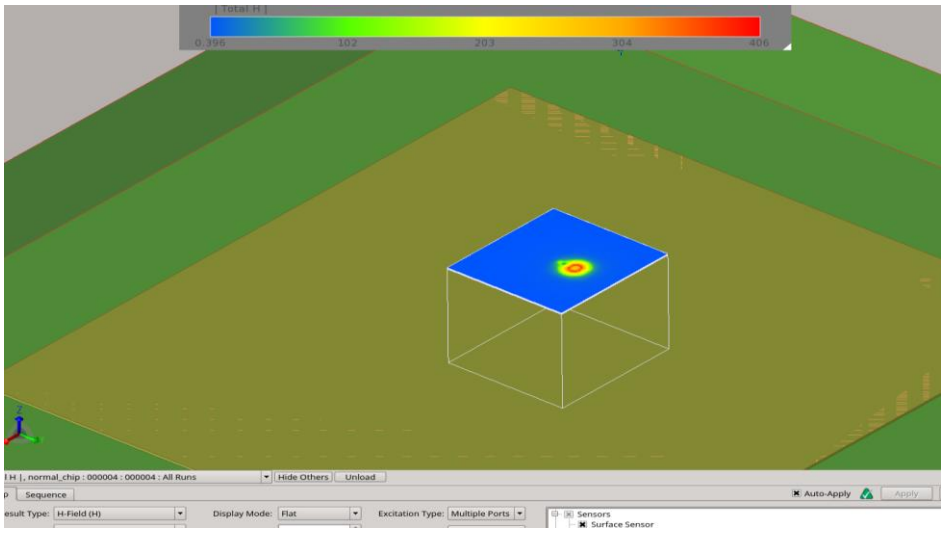

Figure 14 Surface H-Field Magnitude at top of the chip for normal packaging

Sides

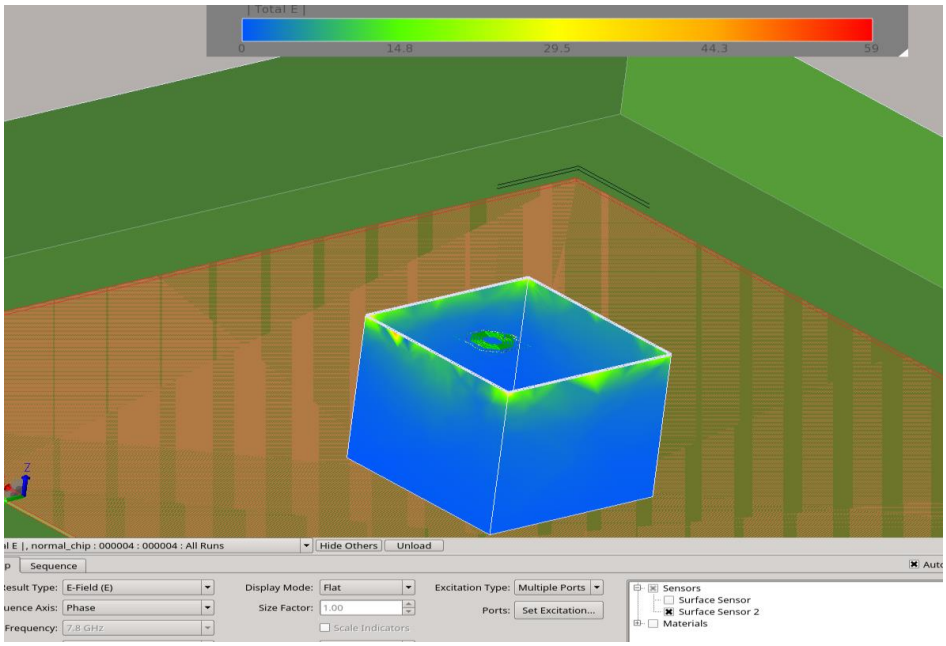

Figure 15 Surface E-Field Magnitude at chip sides for normal packaging

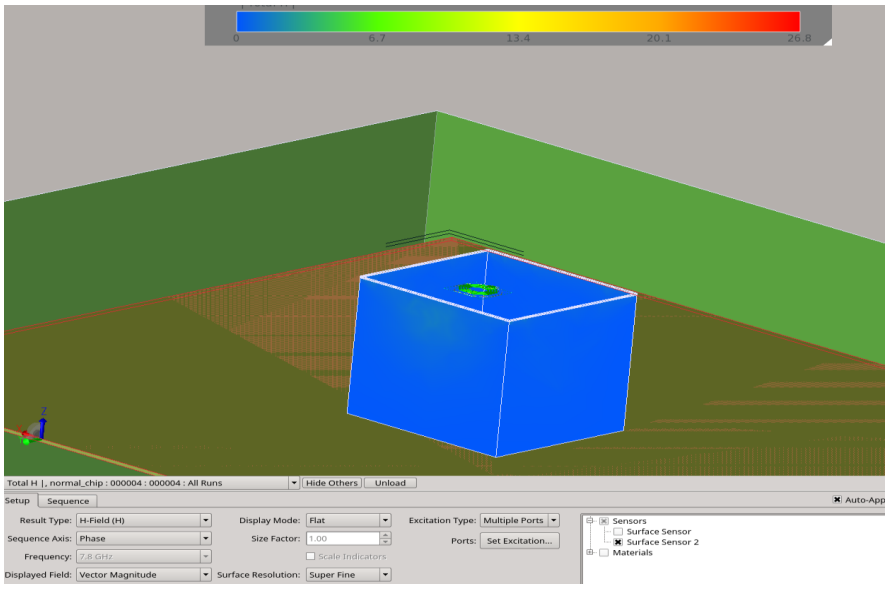

Figure 16 Side H-Field Magnitude at chip side for normal packaging

Case 3: LT102V2

The LT102V2 active RF circuit is modeled as in Figure 7: the flipped chip is mounted over the PCB. Underneath the RF circuit the Groud plane is modeled as a 1/2oz (17um thick) copper shield.

Top Face

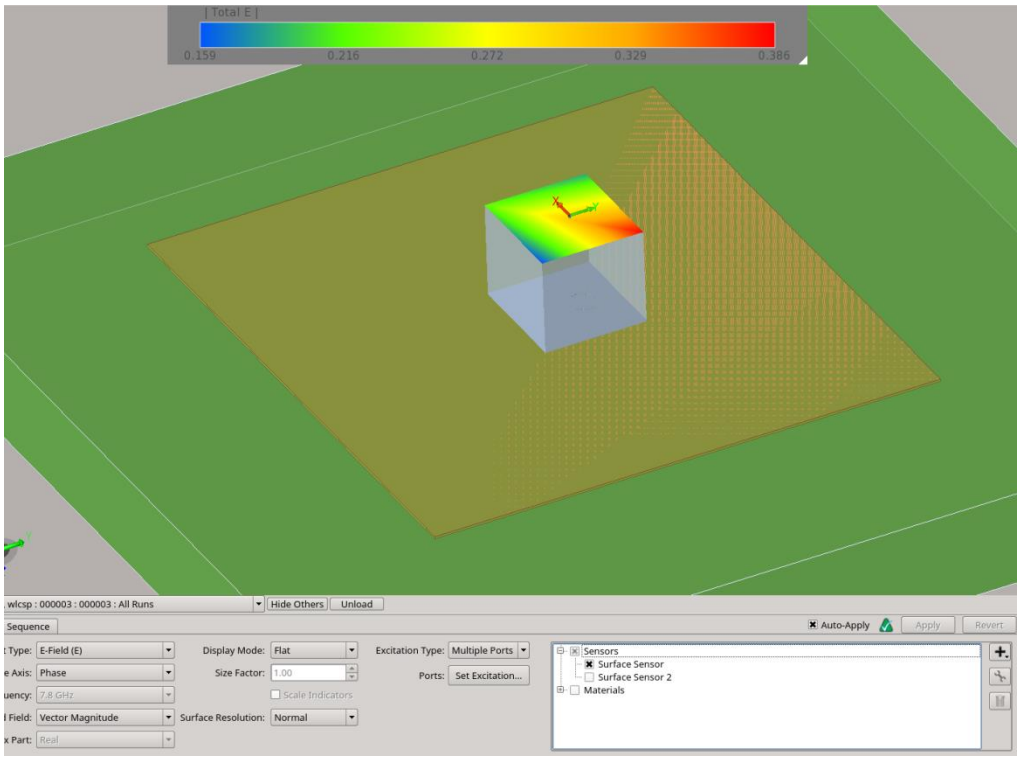

Figure 17 Surface E-Field Magnitude at top of the chip for the LT102V2

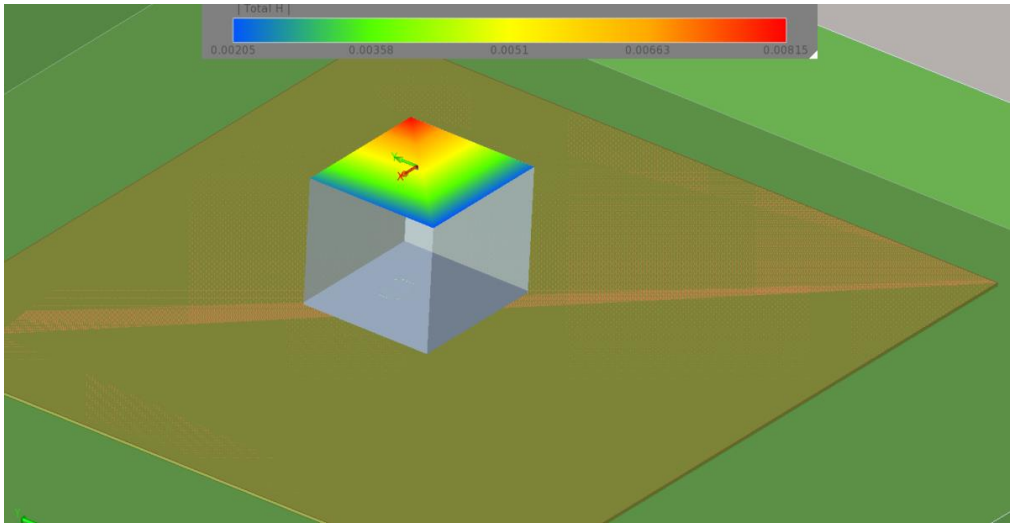

Figure 18 Surface H-Field Magnitude at top of the chip (BEOL side) for the LT102V2

Sides

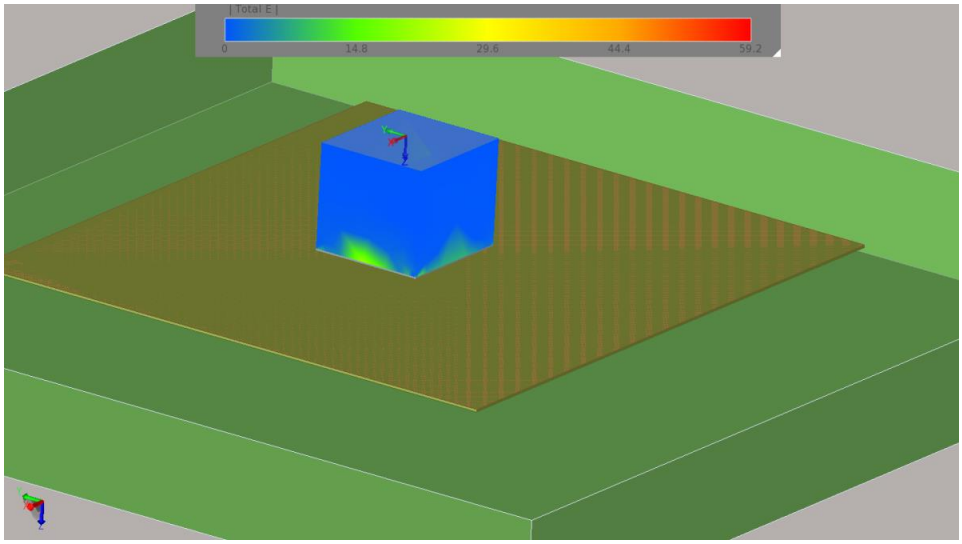

Figure 19 Surface E-Field Magnitude at sides of the chip (BEOL side) for the LT102V2 shielding

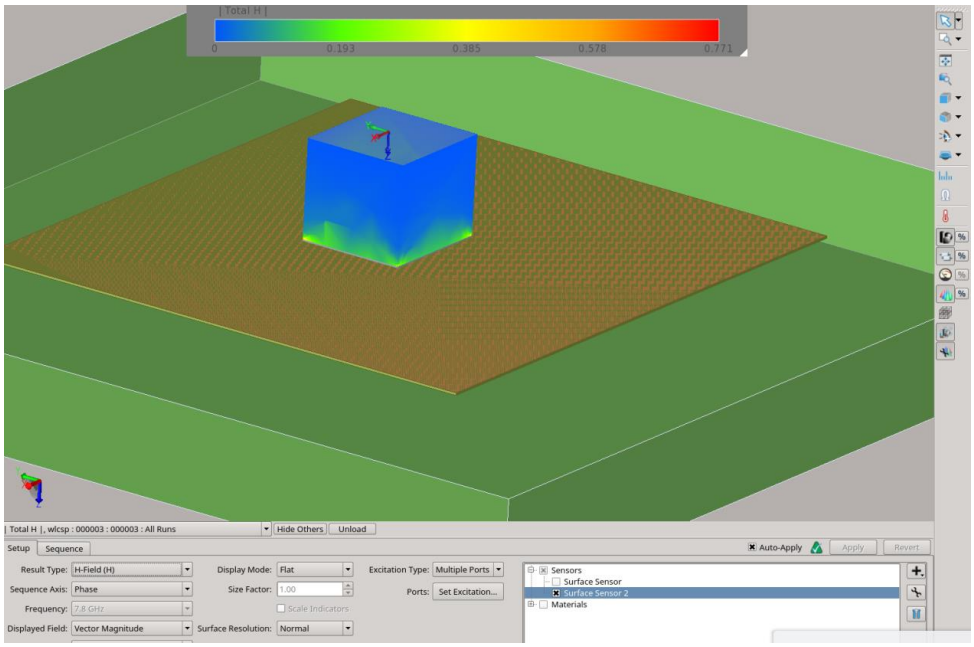

Figure 20 Surface H-Field Magnitude at sides of the chip (BEOL side) for the LT102V2 shielding

Summary

We consider mainly the fields at the top surface of the RF circuitry since this is the face that will get closer to any potential mating device. The comparison is made considering the “normal packaging” as the reference case

Test Case	Maximum E-Field (magnitude)	E-Field relative value	Maximum H-Field (magnitude)	H-Field relative value
Floating Chip	2.06e4 V/m	-3.6dB	393 A/m	-0.28dB
Normal Packaging	3.13e4 V/m	0dB	406 A/m	0dB
LT102V2	0.386 V/m	-98dB	0.00815 A/m	-93dB

Comparison with Shield

The shielding properties of the LT102V2 have been compared to a real shield. The model adopted is the Laird-BMI-S-201-F shield. In the results the peak values for each field have been selected. To have a fair comparison the field is sampled @ 2mm away from the PCB top plane (i.e. at the same height of the shield therefore assuming the same distance of a potential EMI receiver).

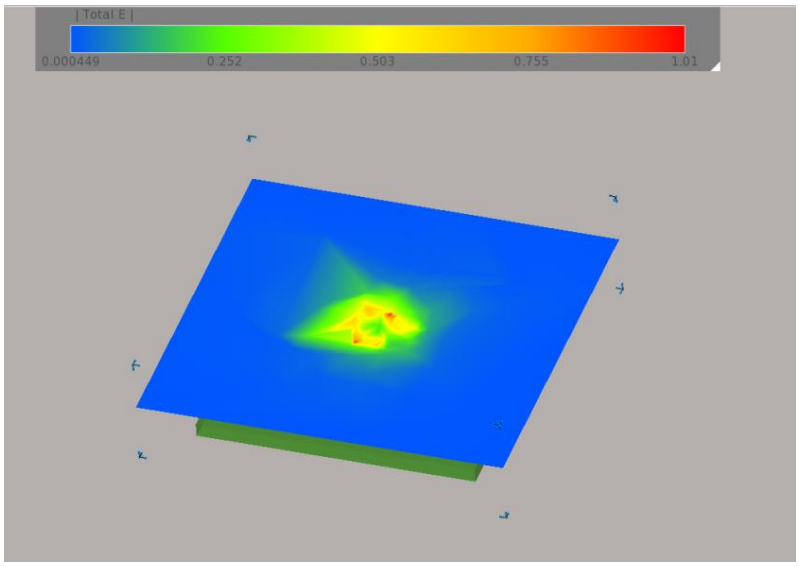

Figure 21 E-Field @ 2mm away from normal package (unshielded)

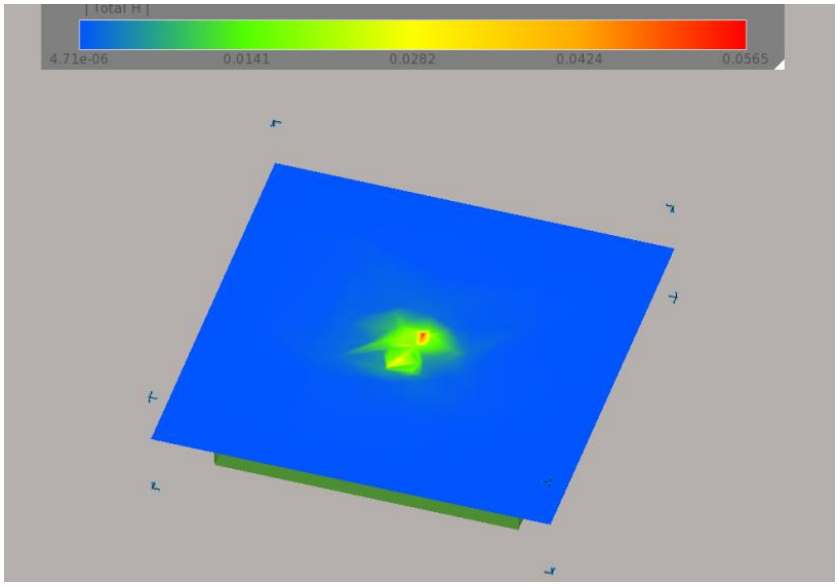

Figure 22 H-Field @ 2mm away from normal package (unshielded)

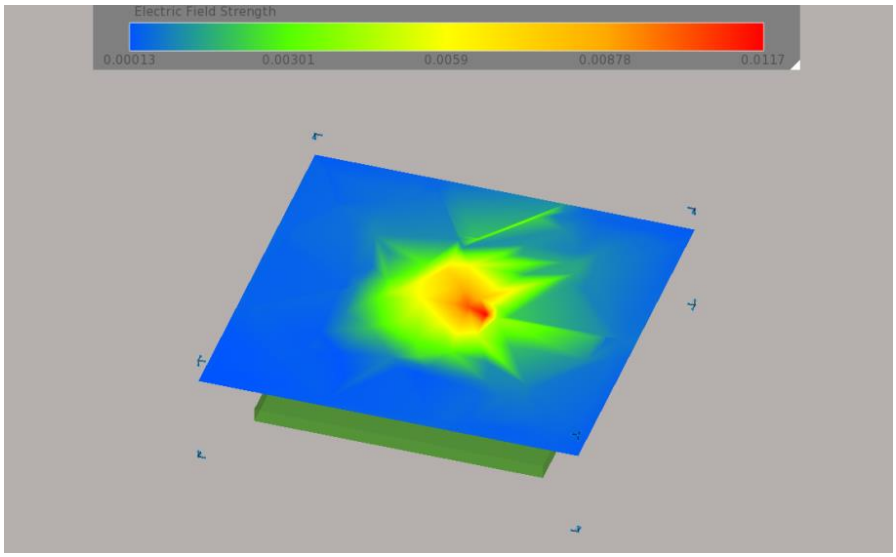

Figure 23 E-Field @ 2mm away from PCB (LT102V2)

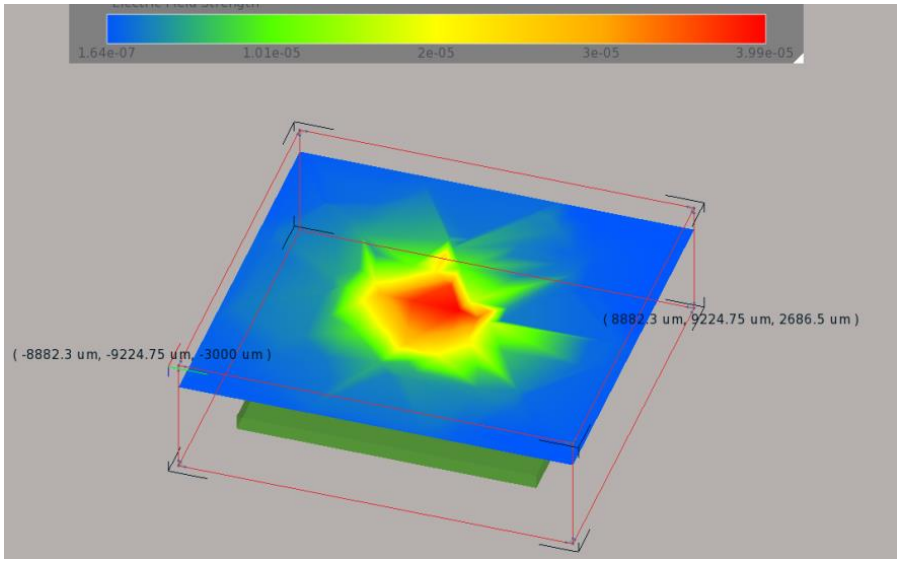

Figure 24 H-Field @ 2mm away from PCB (LT102V2)

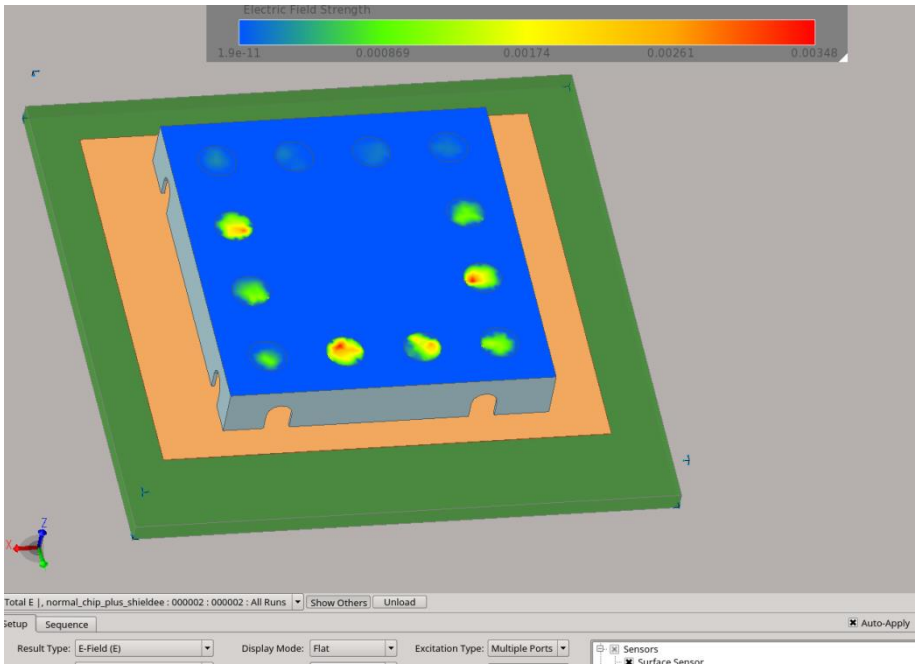

Figure 25 E-Field @ shield interface

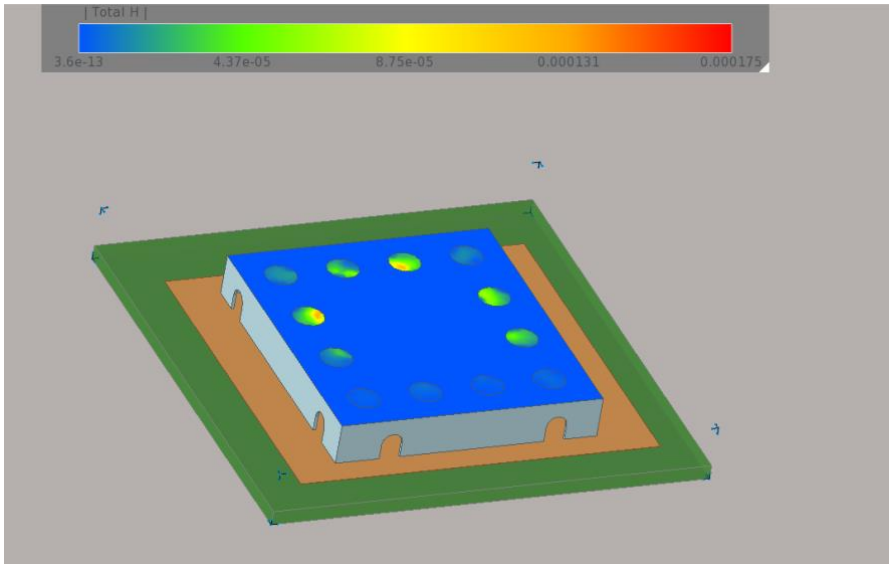

Figure 26 H-Field @ shield interface

Summary

We consider the fields at the same distance to the PCB containing the RF circuitry. The comparison is made considering the “normal packaging” as the reference case

Test Case	Maximum E-Field (magnitude)	E-Field relative value	Maximum H-Field (magnitude)	H-Field relative value
Normal Packaging-unshielded	1.01 V/m	0dB	0.0565 A/m	0dB
LT102V2	0.0117V/m	-38.7dB	3.99e-5A/m	-63dB
Normal package + Laird-BMI-S-201-F	0.00357V/m	-49dB	0.000175A/m	-50dB

Conclusions

In LT102V2 we exploit silicon substrate / doping as an effective shield. The shielding properties of the WLCSP package exhibits shielding performances on-par with a commercial shield.