H353 WiFi/BLE Module

Product Specification

802.11b/g/n/ax 1T1R WiFi/BLE Module

(Q353233N1100)

Version Ver1.0

History

Document Release	Date	Modification	Initials	Approved
Version V1.0	2025/02/05			

Overview

Q353233N1100 is a highly integrated 2.4GHz low-power SoC WiFi and BLE Combo chip that integrates IEEE 802.11b/g/n/ax baseband and RF circuits. The RF circuit includes power amplifier PA, low-noise amplifier LNA, RF BALUN, TX/RX Switch, and power management modules; Supports 20MHz/40MHz bandwidth and provides a maximum physical layer rate of 150Mbps.

Q353233N1100 WiFi baseband supports Orthogonal Frequency Division Multiple Access (OFDMA) technology, Orthogonal Frequency Division Multiplexing (OFDM) technology, and is backward compatible with Direct Sequence Spread Spectrum (DSSS) and Complementary Code Keying (CCK) technology. It supports various data rates of IEEE 802.11b/g/n protocol and MCS0-MCS9 rates of IEEE 802.11ax protocol.

Q353233N1100 supports BLE 1MHz/2MHz bandwidth, BLE 4.0/4.1/4.2/5.0/5.1/5.2/5.3 protocols, BLE Mesh function, and a maximum air interface rate of 2Mbps.Q353233N1100 integrates a dual core high-performance 32-bit microprocessor, hardware security engine, and rich peripheral interfaces, including SDIO, SPI, QSPI, UART, I2C, I2S, PWM, GPIO, and multi-channel ADC; The chip has built-in SRAM and Flash, which can run independently and support running programs on Flash. Q353233N1100 supports OpenHarmony and third-party components, and provides an open and easy-to-use development and debugging environment. Q353233N1100 is suitable for IoT intelligent terminal fields such as smart door locks, smart doorbells, battery cameras, etc

Main specifications

WiFi

- 1X1 2.4GHz frequency band
- PHY supports IEEE 802.11b/g/n/ax
  MAC supports IEEE 802.11d/e/i/k/v/r/w
- Supports 802.11n 20MHz/40MHz bandwidth, supports 802.11ax 20MHz bandwidth
- Maximum supported speed: 150Mbps@HT40 MCS7，114.7Mbps@HE20 MCS9
- Built in PA and LNA, integrated TX/RX Switch, Balun, etc
- Supports both STA and SoftAP forms, with a maximum support of 4 STAs when used as SoftAP
- Support A-MPDU A-MSDU
- Support QoS to meet the quality of service requirements of different businesses
- Support WPA/WPA2/WPA3 personal, WPS2.0
- Support RF self calibration scheme
- Support STBC and LDPC
- Power supply voltage input range: VBAT=3.3V, VDDIO power supply voltage supports 1.8V and 3.3V
- Low power consumption:

  Ultra Deep Sleep mode: 16 uA @ 3.3V

  DTIM10: 98uA@3.3V

*Test conditions: The ambient temperature is 25 ℃, the RX reception time is 1mS, and the chip is powered by Buck and tested under shielded environmental conditions.

Bluetooth

- Bluetooth Low Energy（BLE）
- Supports speeds of 125Kbps, 500Kbps, 1Mbps, and 2Mbps
- Supports Class 1 Class 2
- Supports maximum power of 14dBm and BLE Mesh
- Support BLE Mesh
- Supports BLE 4.0/4.1/4.2/5.0/5.1/5.2/5.3 CPU subsystem

CPU subsystem

- High performance 32-bit microprocessor with a maximum operating frequency of 120MHz
- Embedded SRAM 576KB ROM 352KB
- Embedded 4MB Flash
- Embedded 2KB eFuse

peripheral interface

- 1 SPI interface, 1 QSPI interface, 2 I2C interfaces, 1 I2S interface, 3 UART interfaces, 1 SDIO 2.0 interface, 28 GPIO interfaces, 8 ADC inputs, 8 PWM inputs, external 32K clock (note: the above interfaces are implemented through multiplexing)

Other information

- Working temperature:- 40℃～ 85℃

Main features of the solution

Stable and reliable communication capability

- Support reliable communication algorithms such as TPC, automatic rate, and weak interference immunity in complex environments

Flexible networking capability

- Support BLE Mesh networking
- Supports Wi Fi and BLE networking methods

Comprehensive network support

- Support IPv4/IPv6 network functionality
- Supports DHCPv4/DHCP v6 Client/Server
- Support DNS Client functionality
- Support mDNS function
- Support CoAP/MQTT/HTTP/JSON basic components

Powerful security engine

- Hardware implementation of AES128/256 encryption and decryption algorithm
- Hardware implementation of HASH-SHA256 and HMAC-SHA256 algorithms
- Hardware implementation of RSA and ECC signature verification algorithms
- Hardware implementation of true random number generation, meeting FIPS140-2 random testing standards
- Hardware supports TLS/DTLS acceleration
- Hardware supports national encryption algorithms SM2, SM3, SM4
- Internally integrated EFUSE, supporting secure storage, secure boot, and hardware ID
- Internally integrated MPU feature, supporting memory isolation feature

Open Operating System

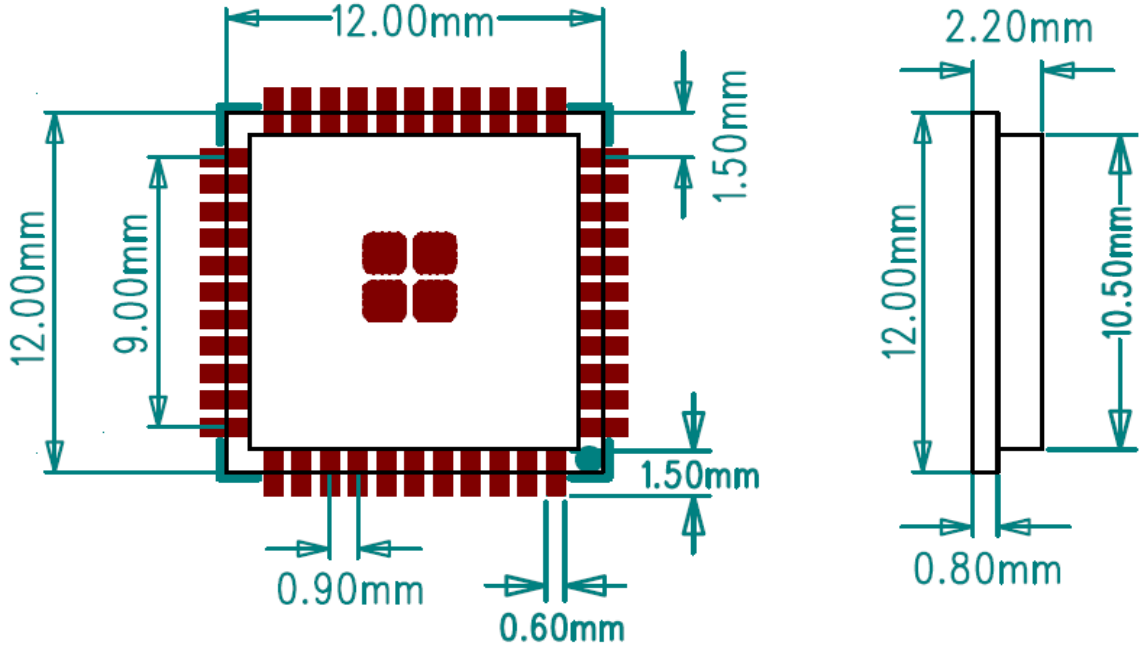
- Supports operating systems such as OpenHarmony and FreeRTOS, providing an open, efficient, and secure system development and runtime environment
- Provide flexible protocol support and scalability
- Provide multi-level development interfaces: operating system adaptation interface and system diagnostic interface, link layer interface, network layer interface

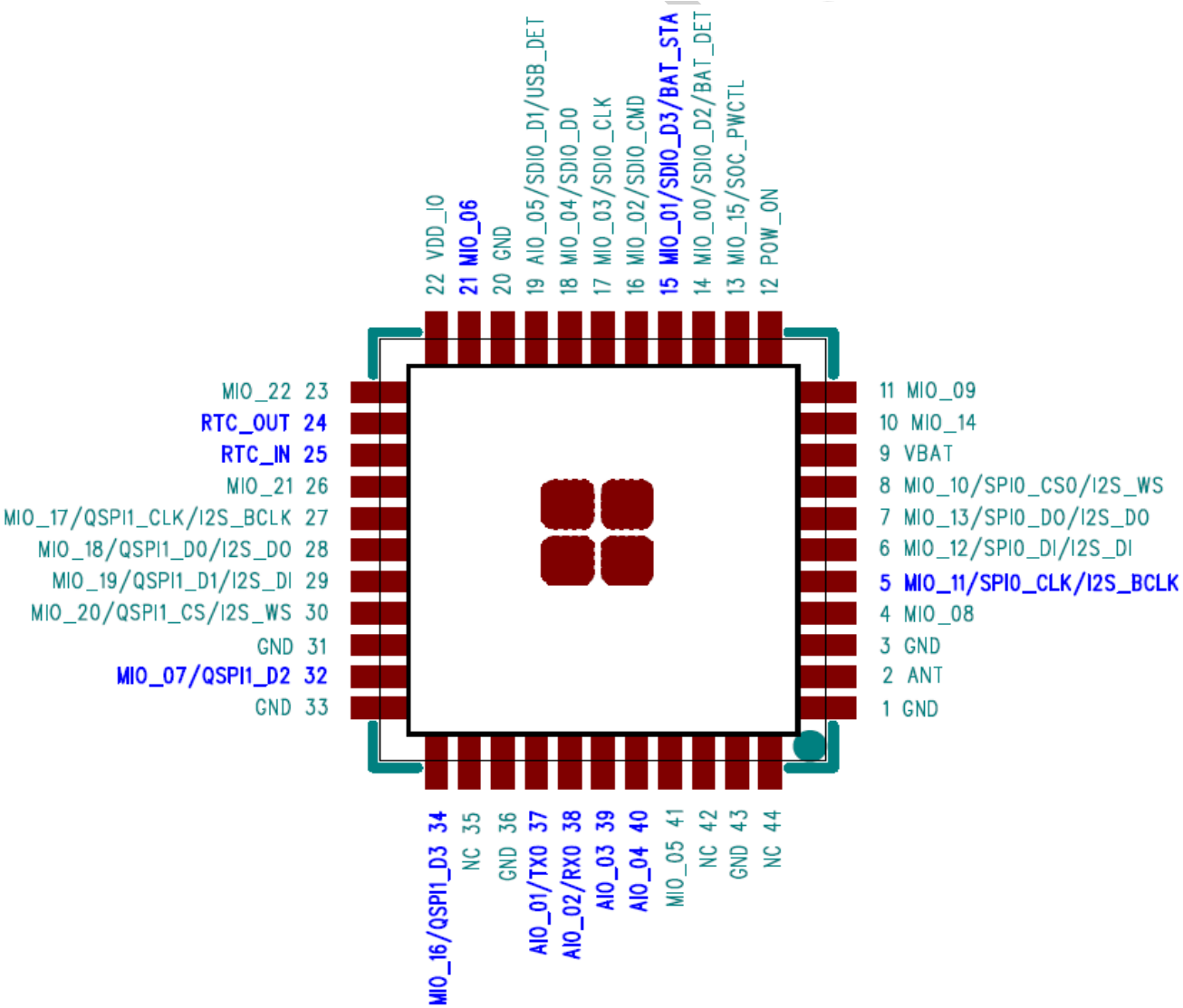
Complete product solutions

- Support integration with mainstream control chips and provide dual machine communication components

MODULE SIZE (Units: mm) (Dimensional tolerance ± 10%)

Note: The height with shielding cover is 2.2 ± 0.2mm, and the overall height of the module without shielding cover is 1.8 ± 0.2mm.





Module pin definition

The following (3) red pins are hardware configuration pins that cannot be pulled, and the module cannot be at a high level when powered on.
The following (5) blue pins can be configured as edge and level triggered wake-up in Udsleep mode. Deep sleep cannot output high and low levels.
The following (5) blue pins can be configured as edge and level triggered wake-up in Udsleep mode. Deep sleep can output high and low levels.

Pin	Function	Type	Voltage	Description
1	GND	GND	-	GND pin
2	ANT	O_{RF}	-	WiFi/BLE RF input and output
3	GND	GND	-	GND pin
4	MIO_08	I/O	VDDIO	MIO_08
5	MIO_11,（Udsleep）	I/O	VDDIO	MIO_11/SPI0_CLK/I2S_BCLK
6	MIO_12	I/O	VDDIO	MIO_12/SPI0_DI/I2S_DI,
7	MIO_13/SDIO_INT	I/O	VDDIO	MIO_13/SPI0_DO/I2S_DO
8	MIO_10	I/O	VDDIO	MIO_10/SPI0_CS0/I2S_WS
9	VBAT	I_{PMU}	3.3V	VABT power input
10	MIO_14	I/O	VDDIO	MIO_14
11	MIO_09	I/O	VDDIO	MIO_09
12	RESET	I_{ANA}	VDDIO	Chip reset pin (low level reset)
13	MIO_15/SOC_PWCTL	I/O	VDDIO	SOC_PWCTL master SoC power control pin
14	MIO_00/SDIO_D2	I/O	VDDIO	MIO_00/SDIO_D2/BAT_DET
15	MIO_01/SDIO_D3,（Udsleep）	I/O	VDDIO	MIO_01/SDIO_D3/BAT_STA
16	MIO_02/SDIO_CMD	I/O	VDDIO	SDIO Command In
17	MIO_03/SDIO_CLK	I	VDDIO	SDIO CLK
18	MIO_04/SDIO_D0	I/O	VDDIO	SDIO Data0, single-wire SDIO data line pin
19	AIO_05/SDIO_D1,（Udsleep）	I/O	VDDIO	USB_DET, USB insertion detection
20	GND	GND	-	GND pin
21	MIO_06,（Udsleep）	I/O	VDDIO	MIO_06
22	VDDIO	I_{PMU}	VDDIO	IO power supply, all IO level select pins, supports 1.8V and 3.3V
23	MIO_22	I/O	VDDIO	MIO_22
24	RTC_OUT	O	-	Module external 32.768KHz crystal
25	RTC_IN	I	-	Module external 32.768KHz crystal or single-ended 32.768KHz signal input.
26	MIO_21	I/O	VDDIO	MIO_21
27	MIO_17/QSPI1_CLK/I2S_BCLK	I/O	VDDIO	MIO_17/QSPI1_CLK/I2S_BCLK
28	MIO_18/QSPI1_D0/I2S_DO	I/O	VDDIO	MIO_18/QSPI1_D0/I2S_DO
29	MIO_19/QSPI1_D1/I2S_DI	I/O	VDDIO	MIO_19/QSPI1_D1/I2S_DI
30	MIO_20/QSPI1_CS/I2S_WS	I/O	VDDIO	MIO_20/QSPI1_CS/I2S_WS
31	GND	GND	-	GND pin
32	MIO_07/QSPI1_D2,（Udsleep）	I/O	VDDIO	MIO_07/QSPI1_D2
33	GND	GND	-	GND pin
34	MIO_16/QSPI1_D3,（Udsleep）	I/O	VDDIO	MIO_16/QSPI1_D3
35	NC	NC	-	NC Pin, Overhang Handling
36	GND	GND	-	GND pin
37	AIO_01/TX0,（Udsleep）	I/O	VDDIO	UART0_TX, burn-in and general-purpose control pin
38	AIO_02/RX0,（Udsleep）	I/O	VDDIO	UART0_RX, burn-in and general-purpose control pins
39	AIO_03,（Udsleep）	I/O	VDDIO	AIO_03
40	AIO_04,（Udsleep）	I/O	VDDIO	AIO_04
41	MIO_05	I/O	VDDIO	MIO_05
42	NC	NC	-	NC Pin, Overhang Handling
43	GND	GND	-	GND pin
44	NC	NC	-	NC Pin, Overhang Handling

GPIO multiplexed pin

The GPIO (General Purpose Input/Output) pins are shown in the table below. Note: The reuse signal 0 is the default function after the power-on reset is completed.

Module Pin	Chip Pin	Pin Name	Typology	Drive (mA)	Voltage (V)	Descriptive
14	31	MGPIO0	ISPU/O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO0 multiplexed signal 1：SDIO_D2 multiplexed signal 2-7 ：reservations Also multiplexed as an analog pin ADC_CH3
15	32	MGPIO1/ AGPIO06	ISPU/O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO1 multiplexed signal1：SDIO_D3 multiplexed signal 2-7 ：reservations
16	33	MGPIO2	ISPU/O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO2 multiplexed signal 1：SDIO_CMD multiplexed signal 2：SPI0_DI multiplexed signal 3~7：reservations
17	34	MGPIO3	ISPU/O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO3 multiplexed signal 1：SDIO_CLK multiplexed signal 2：SPI0_CLK multiplexed signal 3~7：reservations
18	35	MGPIO4	ISPU/O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO4 multiplexed signal 1：SDIO_D0 multiplexed signal 2：SPI0_DO multiplexed signal 3~7：reservations
19	36	AGPIO5	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：AGPIO5 multiplexed signal 1：SDIO_D1 multiplexed signal 2：SPI0_CS0 multiplexed signal 3~7：reservations
41	5	MGPIO5	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO5 multiplexed signal 1：UART_H1_TXD multiplexed signal 2~7：reservations Can be reused as analog pins CLK_XOUT_32M
21	28	MGPIO6/ AGPIO00	ISPU/O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO6 multiplexed signal 1：UART_H0_RTS multiplexed signal 2：SPI0_DI multiplexed signal 3：WB_GLP_SYNC_PULSE multiplexed signal 4~7：reservations Can be reused as analog pinsADC_CH7
32	52	MGPIO7/ AGPIO09	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO7 multiplexed signal 1：UART_H0_CTS multiplexed signal 2：SPI0_CS0 multiplexed signal 3：QSPI1_D2 multiplexed signal 4：reservations multiplexed signal 5：reservations multiplexed signal 6：ANT_SEL2 multiplexed signal 7：reservations
4	26	MGPIO8	ISPU/O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO8 multiplexed signal 1：UART_H0_TXD multiplexed signal 2：SPI0_CLK multiplexed signal 3：I2C1_SCL multiplexed signal 4~7：reservations Can be reused as analog pins ADC_CH5

Module Pin	Chip Pin	Pin Name	Typology	Drive (mA)	Voltage (V)	Descriptive
11	27	MGPIO9	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO9 multiplexed signal 1：UART_H0_RXD multiplexed signal 2：SPI0_DO multiplexed signal 3：I2C1_SDA multiplexed signal 4~7 :reservations Multiplexable as analog tube ADC_CH6
8	21	MGPIO10	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO10 multiplexed signal 1：SPI0_CS0 multiplexed signal 2：UART_H1_CTS multiplexed signal 3：reservations multiplexed signal 4：PWM0P multiplexed signal 5：I2S_WS multiplexed signal 6：ANT_SEL3 multiplexed signal 7：reservations
5	22	MGPIO11/ AGPIO07	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO11 multiplexed signal 1：SPI0_CLK multiplexed signal 2：UART_H1_RTS multiplexed signal 3：reservations multiplexed signal 4：PWM0N multiplexed signal 5：I2S_BCLK multiplexed signal 6~7：reservations
6	23	MGPIO12	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO12 multiplexed signal 1：SPI0_DI multiplexed signal 2：UART_H1_TXD multiplexed signal 3：reservations multiplexed signal 4：reservations multiplexed signal 5：I2S_DI multiplexed signal 6：ANT_SEL4 multiplexed signal 7：reservations
7	24	MGPIO13	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO13 multiplexed signal 1：SPI0_DO multiplexed signal 2：UART_H1_RXD multiplexed signal 3：I2C0_SCL multiplexed signal 4：reservations multiplexed signal 5：I2S_DO multiplexed signal 6~7：reservations
10	25	MGPIO14	ISPU/O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO14 multiplexed signal 1：SPWM1N multiplexed signal 2：I2C0_SDA multiplexed signal 3：WB_GLP_SYNC_PULSE multiplexed signal 4：BT_ACTIVE multiplexed signal 5：UART_H0_CTS multiplexed signal 6：reservations multiplexed signal 7：reservations
13	30	MGPIO15	ISPU/O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO15 multiplexed signal 1：SPWM1P multiplexed signal 2：BT_STATUS multiplexed signal 3：UART_H1_RTS multiplexed signal 4：reservations multiplexed signal 5：reservations multiplexed signal 6：reservations multiplexed signal 7：reservations

Module Pin	Chip Pin	Pin Name	Typology	Drive (mA)	Voltage (V)	Descriptive
34	47	MGPIO16/ AGPIO08	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO16 multiplexed signal 1：QSPI1_D3 multiplexed signal 2：PWM3N multiplexed signal 3~7：
27	48	MGPIO17	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO17 multiplexed signal 1：QSPI1_CLK multiplexed signal 2：UART_H0_TXD multiplexed signal 3：I2S_BCLK multiplexed signal 4：reservations multiplexed signal 5：BT_ACTIVE multiplexed signal 6~7：reservations
28	49	MGPIO18	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO18 multiplexed signal 1：QSPI1_D0 multiplexed signal 2：UART_H0_RXD multiplexed signal 3：I2S_DO multiplexed signal 4：WB_GLP_SYC_PULSE multiplexed signal 5：BT_STATUS multiplexed signal 6~7：reservations
29	50	MGPIO19	ISPU/O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO19 multiplexed signal 1：QSPI1_D1 multiplexed signal 2：PWM2P multiplexed signal 3：I2S_DI multiplexed signal 4：reservations multiplexed signal 5：BT_FREQ multiplexed signal 6~7：
30	51	MGPIO20	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO20 multiplexed signal 1：QSPI1_CS multiplexed signal 2：PWM2N multiplexed signal 3：I2S_WS multiplexed signal 4：reservations multiplexed signal 5：WLAN_ACTIVE multiplexed signal 6~7：reservations
26	46	MGPIO21	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO21 multiplexed signal 1：PWM0P multiplexed signal 2：UART_H0_RTS multiplexed signal 3：I2C0_SCL multiplexed signal 4：WB_GLP_SYNC_PULSE multiplexed signal 5：BT_STATUS multiplexed signal 6~7：reservations
23	43	MGPIO22	ISPU/O	configurable	3.3/ 1.8	multiplexed signal 0：MGPIO22 multiplexed signal 1：PWM3P multiplexed signal 2：UART_H1_CTS multiplexed signal 3：I2C0_SDA multiplexed signal 4：reservations multiplexed signal 5：WLAN_ACTIVE multiplexed signal 6：ANT_SEL5 multiplexed signal 7：reservations Can be reused as analog pins ADC_CH4

Module Pin	Chip Pin	Pin Name	Typology	Drive (mA)	Voltage (V)	Descriptive
37	1	AGPIO1	ISPU/O	configurable	3.3/ 1.8	multiplexed signal 0：AGPIO1 multiplexed signal 1：UART_L0_TXD multiplexed signal 2~7：reservations Can be reused as analog pins ADC_CH0
38	2	AGPIO2	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：AGPIO2 multiplexed signal 1：UART_L0_RXD multiplexed signal 2：PWM0P multiplexed signal 3~7：reservations
39	3	AGPIO3	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：AGPIO3 multiplexed signal 1：I2C1_SCL multiplexed signal 2：PWM0N multiplexed signal 3~7：reservations Can be reused as analog pins ADC_CH1
40	4	AGPIO4	ISPU/ O	configurable	3.3/ 1.8	multiplexed signal 0：AGPIO4 multiplexed signal 1：I2C1_SDA multiplexed signal 2：UART_H1_RXD multiplexed signal 3~7：reservations Can be reused as analog pins ADC_CH2
25	45	RTC_IN	ISPU/O	configurable	3.3/ 1.8	
24	44	RTC_OUT	ISPU/ O	configurable	3.3/ 1.8	
12		RST_N	ISPU/O	configurable	3.3/ 1.8	Global reset signal

Pin I/O Type Description: ISPU/O = Bidirectional, input pull-up with Schmitt trigger.

Recommperating Conditions

Parameter	Min	Typ	Max	Unit
VBAT & VDDIO = 3.3V	3.16	3.30	3.46	V
VDDIO = 1.8V	1.71	1.80	1.89	V
VBAT+VDDIO=3.3V Working Current	-	350	500	mA
VDDIO=3.3 or 1.8V Working Current	-	50	150	mA
Operation Temperature	-20		70	℃

current consumption Specifications

Parameter	Test Item	TX Power	Current	Unit
WiFi TX	11b, CCK,1Mbps	19dBm	430	mA
	11b, CCK,11Mbps	19dBm	420	mA
	11g, OFDM, 6Mbps	19dBm	320	mA
	11g, OFDM, 54Mbps	19dBm	200	mA
	11n,HT20, MCS0	19dBm	310	mA
	11n,HT20, MCS7	18dBm	200	mA
	11ax,HE20, MCS0	20dBm	320	mA
	11ax,HE20, MCS9	16dBm	180	mA
	11n,HT40, MCS0	19dBm	310	mA
	11n,HT40, MCS7	18dBm	180	mA
	WiFi Stop TX	0dBm	25	mA
WiFi RX	-	-	45	mA
	WiFi Stop RX		25	mA
BT TX	BLE,1M,	14dBm	90	mA
	BLE,2M	14dBm	65	mA
	BLE Stop TX	0dBm	20	mA
BT RX	-	-	25	mA
	BLE Stop RX		20	

RF Characteristics

WiFi 2.4G launch indicators

Parameter	Test Item	Typical Value
Output Power	11b, 1Mbps	17±2dBm,EVM<-20dB
	11b,11Mbps	17±2dBm,EVM<-18dB
	11g , 6Mbps	17±2dBm,EVM<-20dB
	11g , 54Mbps	17±2dBm,EVM<-28dB
	11n, HT20 MCS0	17±2dBm,EVM<-20dB
	11n, HT20 MCS7	17±2dBm,EVM<-29dB
	11ax ,HT20 MSC0	18±2dBm,EVM<-22dB
	11ax ,HT20 MSC9	18±2dBm,EVM<-34dB
	Test Item	**Typical Value**
	11n, HT40 MCS0	18±2dB,EVM<-20dB
	11n, HT40 MCS7	18±2dB,EVM<-29dB

WLAN Receiver Characteristic

Parameters	Test Item	CH3	CH7	CH11	Unit
Receive Sensitivity	11b, 1M , <-76dBm@8%PER	-98	-98	-98	dBm
	11b, 11M ,<-76dBm@8%PER	-90	-90	-90	dBm
	11g, 6M , <-82dBm@10%PER	-95	-95	-95	dBm
	11g, 54M , <-65dBm@10%PER	-76	-76	-76	dBm
	11n, HT20 MCS0, <-82dBm@10%PER	-94	-94	-94	dBm
	11n, HT20 MCS7, <-64dBm@10%PER	-74	-74	-74	dBm
	11ax, HE20 MCS0, <-82dBm@10%PER	-94	-94	-94	dBm
	11ax, HE20 MCS9, <-57dBm@10%PER	-68	-68	-68	dBm
	Test Item	**CH3**	**CH7**	**CH11**	**Unit**
	11n, HT40 MCS0,<-79dBm@10%PER	-91	-91	-91	dBm
	11n, HT40 MCS7,<-61dBm@10%PER	-71	-71	-71	dBm

BLE TX Performance

Parameter	Test Item	Typical Value
Output power	1M	12±2dB
Output power	2M	12±2dB

Note: There is no commission certification requirement, compared to the typical value of the maximum power, there is a 4dB power reduction for the 2402M and 2478M channels and a 10dB power reduction for the 2480M channel.

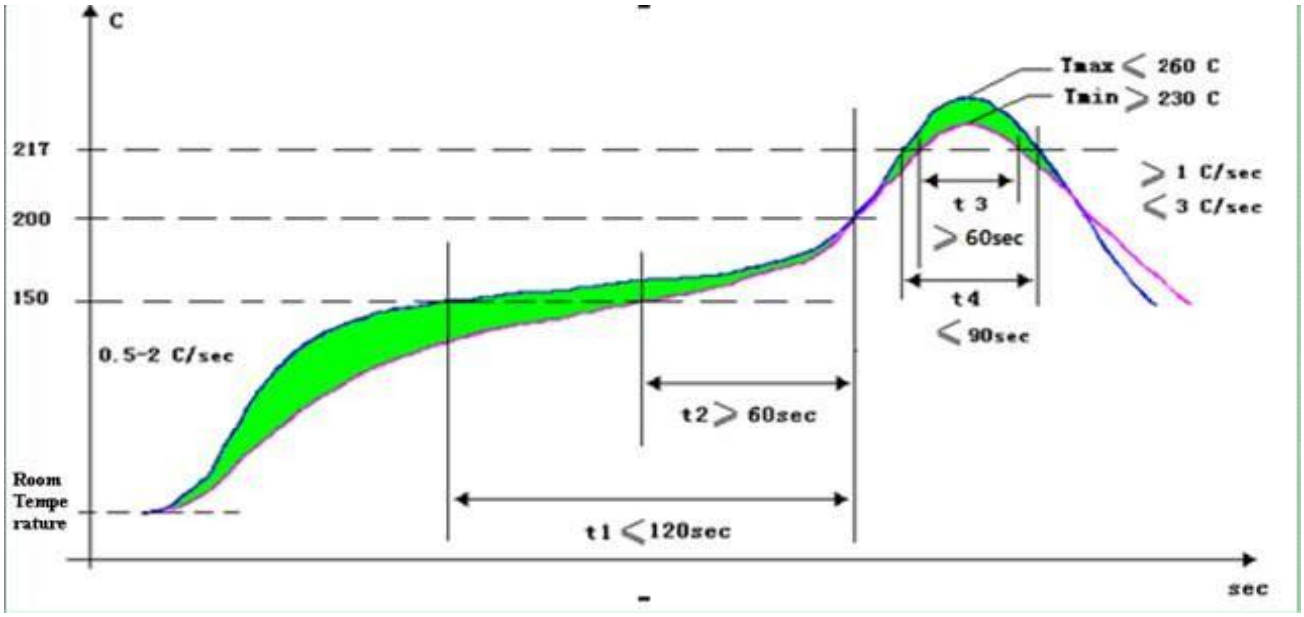
BLE RX Performance

Parameter	Test Item	Typical Value	Channel			Unit
			CH1	CH19	CH39	
Sensitivity >30% packaet	1M	<-96	-98	-98	-98	dBm
Sensitivity >30% packaet	2M	<-93	-95	-95	-95	dBm

Order Information

Module	Part number	Description
H353	H353_NS	H353 WiFi/BLE Module without Shield
H353	H353_WS	H353 WiFi/BLE Module with Shield

- **Lead-free reflow process parameter requirements**
  The lead-free reflow soldering process profile is shown below.



- The lead-free reflow process parameters are shown in the table below.

shore	timing	heating	Peak temperature	cooling rate
warm-up area（40～150℃）	60～150s	≤2.0℃/s	-	-
equal temperature zone（150～200℃）	60～120s	＜1.0℃/s	-	-
reflux zone（＞217℃）	60～90s	-	230-260℃	-
cooling zone（Tmax～180℃）	-	-	-	1.0℃/s≤Slope≤4.0℃/s

Description:

- Preheating zone: the temperature is from 40℃ to 150℃, the temperature increase rate is controlled at about 2℃/s, the time of this temperature zone is 60-150s.
- average temperature zone: temperature from 150 ℃ to 200 ℃, stable and slow warming, the temperature rise rate of less than 1 ℃ / s, and the time control in the region of 60 ~ 120s (Note: the region must be slowly heated, otherwise it is easy to lead to poor welding).
- reflux zone: temperature from 217°C to Tmax ~ 217°C, the time of the whole interval is controlled at 60-90s.
- Cooling zone: temperature from Tmax～180℃, the maximum temperature drop rate cannot exceed 4℃/s.
- Temperature increase from room temperature 25°C to 250°C should not take more than 6 minutes.
- The reflow profile is only a recommendation, the client needs to adjust it according to the actual production situation.

The reflow time is targeted at 60 to 90s, and the reflow time can be relaxed to 120s for some veneer boards with large heat capacitance that cannot meet the time requirement.

Refer to IPC/JEDEC J-STD-020D for package temperature resistance standard, and refer to JEP 140 for package temperature measurement method.

IPC/JEDEC J-STD-020D standard, encapsulation body temperature measurement method in accordance with JEP 140 standard requirements:

The temperature resistance standards for lead-free device packages in IPC/JEDEC 020D are shown in the table below.

Table IPC/JEDEC 020D Temperature Resistance Criteria for Lead-Free Device Packages

Package Thickness	Volume mm3 <350	Volume mm3 350~2000	Volume mm3 >2000
＜1.6mm	260℃	260℃	260℃
1.6mm～2.5mm	260℃	250℃	245℃
＞2.5mm	250℃	245℃	245℃

Device solder ends (balls, pins) and external heat sinks are not accounted for in the volume calculations.

Reflow Soldering Process Profile Measurement Methods:

JEP140 Recommendations: For smaller thickness devices, measure the package temperature by directly placing a thermocouple on the surface of the device, and for larger thickness devices, drill and bury a thermocouple in the surface of the device for measurement. Due to the requirement of quantifying the thickness of the device, it is recommended that all the thermocouples are drilled and embedded on the surface of the package (except for particularly thin devices, which cannot be drilled)

FCC Statement

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user' s authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursua nt to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful inte rference in a residential installation. This equipment generates uses and can radiate radio frequency energy a nd, if not installed and used in accordance with the instructions, may cause harmful interference to radio com munications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turn ing the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help important announcement

Important Note:

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator and your body.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Country Code selection feature to be disabled for products marketed to the US/Canada.

This device is intended only for OEM integrators under the following conditions:

1. The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2. The transmitter module may not be co-located with any other transmitter or antenna,
3. For all products market in US, OEM has to limit the operation channels in CH1 to CH11 for 2.4G band by supplied firmware programming tool. OEM shall not supply any tool or info to the end-user regarding to Regulatory Domain change. (if modular only test Channel 1-11)

As long as the three conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Important Note:

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

The final end product must be labeled in a visible area with the following"

Contains FCC ID: **2AXX8-H353-NS** "

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01r01

2.2 List of applicable FCC rules

CFR 47 FCC PART 15 SUBPART C has been investigated. It is applicable to the modular transmitter

2.3 Specific operational use conditions

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in a host, host manufacturer have to consult with module manufacturer for the installation method in end system.

2.4 Limited module procedures

Not applicable

2.5 Trace antenna designs

Not applicable

2.6 RF exposure considerations

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

2.7 Antennas

This radio transmitter **FCC ID:2AXX8-H353-NS** has been approved by Federal Communications Commission to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Antenna No.	Model No. of antenna:	Type of antenna:	Gain of the antenna (Max.)		Frequency range:
			Antenna 1	Antenna 2	
Bluetooth	/	External Antenna	4.55	/	2402-2480MHz
2.4G Wi-Fi	/	External Antenna	4.55	/	2412-2462MHz

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following" Contains **FCC ID:2AXX8-H353-NS**".

2.9 Information on test modes and additional testing requirements

Host manufacturer is strongly recommended to confirm compliance with FCC requirements for the transmitter when the module is installed in the host.

2.10 Additional testing, Part 15 Subpart B disclaimer

Host manufacturer is responsible for compliance of the host system with module installed with all other applicable requirements for the system such as Part 15 B.

2.11 Note EMI Considerations

Host manufacture is recommended to use D04 Module Integration Guide recommending as "best practice" RF design engineering testing and evaluation in case non-linear interactions generate additional non-compliant limits due to module placement to host components or properties.

2.12 How to make changes

This module is stand-alone modular. If the end product will involve the Multiple simultaneously transmitting condition or different operational conditions for a stand-alone modular transmitter in a host, host manufacturer have to consult with module manufacturer for the installation method in end system. According to the KDB 996369 D02 Q&A Q12, that a host manufacture only needs to do an evaluation (i.e., no C2PC required when no emission exceeds the limit of any individual device (including unintentional radiators) as a composite. The host manufacturer must fix any failure.