QPG6095

Zigbee/Thread/BLE Smart Home
Communications Controller

Data Sheet

1 Product Overview

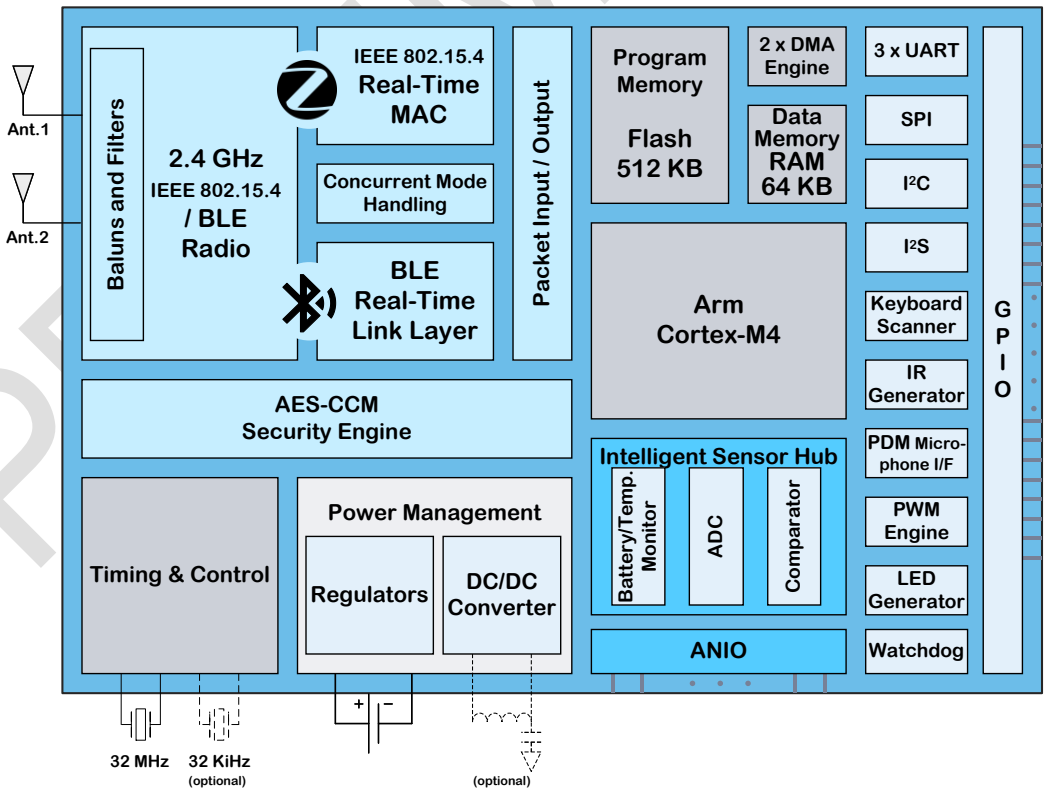
The QPG6095 Zigbee/Thread/BLE Smart Home Communications Controller provides a fully integrated solution for ultra-low power wireless communications for Smart Home sentroller devices such as thermostats, motion sensors, smart plugs, key pads and door/window sensors. It is compliant with the IEEE Standard 802.15.4 for Zigbee and Thread, and the Bluetooth Core Specification version 5.0 for Bluetooth Smart, providing robust spread spectrum data communication with a highly secure encrypted and authenticated data flow. For IEEE 802.15.4 communications, antenna diversity offers additional robustness in a crowded 2.4 GHz environment.

The QPG6095 features a radio transceiver, integrated real-time IEEE 802.15.4 Medium Access Control and Bluetooth Low Energy (BLE) controller, integrated Arm® Cortex®-M4 microprocessor, RAM and Flash memory, security engine, event scheduler, and an extensive set of peripherals including analog signal monitors and comparators. The QPG6095's integrated RF baluns and filters reduce the product's RF design complexity enabling very low cost single layer applications using simple PCB antennas requiring no shielding and a minimum number of external components. The Flash memory allows for software upgrade over the air.

The QPG6095 is capable of running the full stack and applications for Zigbee 3.0, Thread and Bluetooth Smart devices. Integrated multi-stack, multi-protocol support enables stacks to operate concurrently, and on different channels, enabling innovative new applications combining Zigbee, Thread and Bluetooth Smart in one product.

Advanced power management features ensure that power consumption is minimized in active as well as in standby states, enabling maintenance free and very small form factor products. For lower power consumption, the integrated DC/DC Buck converter can be used together with a few external components. Alternatively, the internal regulator can be used instead of the integrated DC/DC converter, to minimize the bill of material.

2 Functional Block Diagram



3 Key Features

Radio
- ✓ 2.4-GHz RF Transceiver compliant with:
  IEEE 802.15.4 and
  Bluetooth Smart
- ✓ Excellent receiver sensitivity
- ✓ IEEE 802.15.4 Preamble based Antenna Diversity, increasing the range significantly
- ✓ IEEE 802.15.4 Packet-in-Packet resynchronization
- ✓ In 1 dB steps programmable transmitter output power, stable over voltage and temperature, up to 10 dBm
- ✓ Integrated baluns and RF filters limit the number of external components
- ✓ Support for external LNA and/or PA
- ✓ Targeting compliance with worldwide RF regulations: ETSI EN 300 328 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T-66 (Japan)

Real-Time Medium Access Control
- ✓ IEEE 802.15.4-compliant MAC
- ✓ CSMA/CA
- ✓ Automatic ACK handling and Retransmissions
- ✓ Address recognition and packet filtering

Real-Time BLE Controller
- ✓ Bluetooth 5.0 compliant LE Controller
- ✓ Supports high data rate of 2 Mbit/s
- ✓ Maximum PDU payload size of 240 bytes.
- ✓ Full connection utilization guarantee

Multi-Protocol / Multi-Channel Support
- ✓ Concurrent IEEE 802.15.4 and BLE Communications
- ✓ Multiple protocol stacks operating concurrently
- ✓ Simultaneous listening on 3 different channels with antenna diversity
- ✓ Up to 3 PANs

Security
- ✓ CCM and CCM* encryption and authentication with 128-bit keys

Integrated Microcontroller
- ✓ Arm Cortex-M4 processor with DSP functionality
- ✓ Up to 64 MHz clock speed

Memory
- ✓ 64 Kbyte Low Leakage Retention RAM
- ✓ 512 Kbyte Flash Program memory
- ✓ Two DMA Engines

Peripherals and Interfaces
- ✓ Up to 30 Programmable GPIO lines
- ✓ Up to 6 Analog input lines
- ✓ Keyboard Scanner
- ✓ IR generator for dual-mode operation
- ✓ High drive sink on GPIO18 for IR
- ✓ SPI Master and Slave interfaces
- ✓ I^2C Master and Slave interfaces
- ✓ Three UART interfaces
- ✓ I^2S Master interface for digital audio devices
- ✓ PDM Microphone Interface
- ✓ PWM Engine (16-bit PWM) for 6 outputs
- ✓ LED Generator (8-bit PWM) with fading support for 4 signaling LEDs
- ✓ 10/12-bit ADC to monitor the ANIO pins, the power supply level and the temperature
- ✓ Low power comparator

Power Management
- ✓ Operating voltage range: 1.8 ... 3.6V
- ✓ Integrated Regulators
- ✓ Integrated DC/DC Buck Converter
- ✓ Low power standby modes:
  Using internal RC oscillator: 1 µA
  Using 32 MHz crystal oscillator: 760 µA
  Using 32 KiHz crystal oscillator: 1.2 µA
- ✓ Data and state retention in all standby modes

Dimensions and Layout
- ✓ QFN40 6x6 mm package
- ✓ Supports direct interfacing with printed antennas
- ✓ No RF shielding required

Environmental Aspects
- ✓ RoHS compliant

4 Ordering Information

Table 1: Ordering and Packing Information

Part Number	Chip Package	Flash	RAM	Packing	Unit Quantity (number of chips)	Box Dimensions
QPG6095TR13	QFN40	512 KB	64 KB	13” Tape and Reel	3000	37 x 35 x 8 cm

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5 Functional Description

5.1 2.4 GHz Radio

The QPG6095 radio transceiver provides all the functionality for the Physical layer (PHY) for both the IEEE 802.15.4 and the Bluetooth communications.

The QPG6095 is able to listen simultaneously on three different IEEE 802.15.4 channels while antenna diversity is enabled.

This section describes the generic features; following sections describe the specific features for IEEE 802.15.4 and Bluetooth.

5.1.1 RF Ports with Integrated Baluns and Filters

The QPG6095 has two antenna ports with integrated baluns and RF filters. The antenna ports output is 50 Ω single ended. Optionally the outputs can be combined to one 200 Ω differential output.

5.1.2 Radio Configurations

The QPG6095 supports several different radio configurations. It can be configured to use a different receive and transmit antenna, or for IEEE 802.15.4 communications it can use antenna diversity (see section 5.2.2). It can also use an external LNA and/or PA with TX antenna diversity switch to increase the link budget (contact Qorvo Support for supported FEM types). A few sample configurations are depicted below, but others are also possible.

Sample Configuration 1 (Figure 1):

- Single ended 50 Ω antenna
- Using antenna 1 (RF1 pin) for both RX and TX
- Antenna diversity disabled

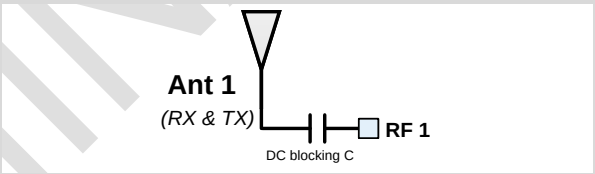


Figure 1: Single Antenna

Sample Configuration 2 (Figure 2):

- 2 Single ended 50 Ω antennas
- TX on same antenna as was selected best by RX
- Antenna diversity enabled (for IEEE 802.15.4)

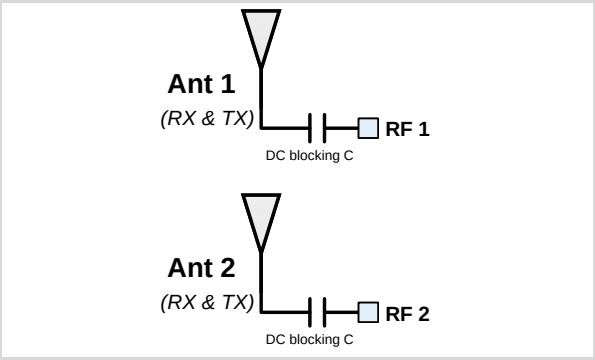


Figure 2: Two Antennas

Sample Configuration 3 (Figure 3):

- Symmetrical antenna
- Antenna diversity disabled

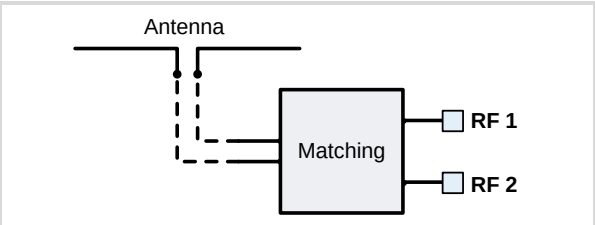


Figure 3: Symmetrical Antenna

5.1.3 RSSI

The PHY's RSSI circuitry measures the received signal energy level and this value is converted to dBm values in the Hardware Abstraction Layer (HAL). See Receiver Characteristics (6.4 below) for the range and accuracy.

5.1.4 Transmit Power Control

The transmitter output power is configured by software, in steps of 1 dB.

5.2 IEEE 802.15.4 Communications

5.2.1 2.4 GHz IEEE 802.15.4 Transceiver

The QPG6095 radio is compliant with the IEEE 802.15.4 standard as required for supporting Zigbee and Thread.

The QPG6095 supports all the IEEE Standard 802.15.4 defined channels in the 2.4 GHz ISM license-free frequency band (channels 11 .. 26).

The channel number (k) and center frequency (F_c) relate as follows: $\boldsymbol{F_c = 2405 + 5(k - 11)}$ *in MHz*

5.2.2 Antenna Diversity

Preamble based antenna diversity enables the PHY to choose the optimal antenna for every individual packet, and increases the performance of the receiver in environments that are dominated by multipath fading effects and interference situations. In receive mode the PHY selects the antenna based on the best signal quality (signal-to-noise/interference ratio).

For typical indoor usage in an environment with 50 ns delay-spread and 2 MHz signal bandwidth using the Rayleigh fading model, antenna diversity with 2 antennas results in a ~8 dB improved link budget (at a 1% outage probability) compared to no antenna diversity. This translates into 70% more reliable range (using a log-distance breakpoint model[1] with path loss coefficients g1=2 (free space propagation) and g2=3.5 above the breakpoint at 10 m).

Unless configured otherwise, the QPG6095 will use the same antenna for transmission as the one that was used for the reception of the last packet.

[1] Refer to "T.S. Rappaport, Wireless Communications – Principles & Practice, Prentice Hall, 1996" for this model.

5.2.3 Clear Channel Assessment (CCA)

The PHY can perform a clear channel assessment (CCA) to avoid collisions. The IEEE 802.15.4 standard defines 3 CCA methods; the QPG6095 supports:

Energy Detect : The medium is considered busy when the measured energy in the selected channel is above a certain threshold. This CCA threshold is programmable.

5.2.4 Packet-in-Packet Resynchronization

If the QPG6095 is receiving a packet from one node and is interrupted by the reception of another stronger packet from another node, the receiver will resynchronize to the latter and continue to receive and process this packet. This allows one packet (the strongest) to be received where otherwise both packets would have been lost. Packet-in-Packet collisions can occur in situations when neighbor network packets are received at a low level and in hidden node situations where not all nodes can see each other.

5.2.5 Real-Time Medium Access Control (MAC)

The QPG6095 implements all Zigbee and Thread-required MAC features of the IEEE Standard 802.15.4. The MAC provides a packet-level service to the protocol stack, and handles packet transmissions and receptions autonomously, including:

- Performing CSMA/CA to avoid collisions when transmitting packets;
- Adding CRC and Sequence number;
- Acknowledgement handling for transmitted packets, including automatic retransmissions;
- Option to spread retransmissions over different channels to natively support RF4CE multi-channel acknowledged transmission schemes
- Address recognition and packet filtering on received packets, including CRC checking;
- Acknowledgement handling for received packets, including automatic acknowledge transmission.

5.2.6 Link Quality Indication

In addition to the RSSI, there is also a link quality indication (LQI) determined for each received IEEE 802.15.4 data packet, for use at the network and application layers.

5.3 Bluetooth Communications

The QPG6095 implements the Bluetooth low energy LE Controller functionality, including PHY, Link Layer and HCI according the Bluetooth Core Specification version 5.0* for Bluetooth Smart. When combined with a BLE Host Stack (see chapter 8), it supports all GATT-based profiles and services, and it can operate as a Broadcaster, Observer, Central and Peripheral device.

*Note: The QPG6095 is certified for BLE 5.0 with support for the 2 Mbit/s data rate; it does not support other optional BLE 5.0 features like the Long Range Coded PHY and Advertising Extensions.

5.3.1 2.4 GHz BLE PHY Layer

The QPG6095 implements the Bluetooth LE PHY layer, supporting all the (40) Bluetooth defined frequency channels in the 2.4 GHz ISM license-free frequency band.

The BLE Controller supports the normal data rate of 1 Mbit/s, as well as the high data rate of 2 Mbit/s.

5.3.2 Real-Time BLE Link Layer

The Real-Time Link Layer implements the real-time functions of the Bluetooth LE Link Layer (LL) protocol for the Advertising-, Scanning, Initiating and Connection States. Multi-state operation is supported: a multi-level priority mechanism ensures appropriate scheduling of Advertising, Scanning, Initiating and Connection-events.

In the Connection State, the Real-Time Link Layer maintains the LE Asynchronous Connection-oriented Logical (LE ACL) transport on master and/or slave connections, allowing transfer of control (LE-C) and user (LE-U) data. High-throughput applications are supported via a dedicated queue per (LE ACL) connection, thus ensuring efficient filling of Connection Events.

The maximal PDU size supported is 246 bytes (resulting in a PDU payload size of 240 bytes). Together with 4 bytes of access code and 3 bytes of CRC, this gives a total packet size, excluding preamble, of 253 bytes.

5.3.3 Full Connection Utilization Guarantee

The QPG6095 has been optimized for audio streaming over BLE with a full BLE connection utilization guarantee under high CPU load conditions. This implies that the system can fill the complete connection with BLE packets allowing to achieve the maximal bandwidth of the connection, even when the CPU is processing audio (decimation, equalizing, compressing), under a large variety of BLE connection configurations (normal data and high data rate, short and long connection intervals, short and long BLE packets).

5.4 Concurrent IEEE 802.15.4 / BLE Communications

The QPG6095 features state of the art support for concurrent IEEE 802.15.4 and BLE communications. It allows to interleave IEEE 802.15.4 traffic and BLE connections in a way adapted to the use case.

It supports two modes:

- A best effort mode, where the BLE controller will automatically free-up air time in the connection when IEEE 802.15.4 has data packets queued.
- A controlled BW mode, where the BLE controller will reserve a portion of the connection for IEEE 802.15.4 communication.

5.5 Security Engine

The QPG6095 is equipped with a low power Security Engine that can work independently from the PHY and MAC.

The Security Engine is capable of:

- CCM and CCM* encryption, decryption and authentication with 128, 192 and 256-bit keys
- AES encryption with 128, 192 and 256-bit keys

For IEEE 802.15.4 the 128-bit CCM* is used. For Bluetooth Smart the 128-bit CCM is used.

5.6 Packet Input Output (PIO)

The Packet Input Output (PIO) controls the exchange of primitives and packets between the microcontroller and the 802.15.4 Real-Time MAC, as well as the exchange of (LE-C and LE-U) packets between the microcontroller and the BLE Real-Time Link Layer. Information about a packet or other primitive parameters is stored in Packet Buffer Memory (PBM), a reserved region of the RAM that can hold information for up to 32 packets. The number of packets is software configurable; the application needs to make sure there are sufficient PBMs available to meet the requirements. These PBM entries are shared between the 802.15.4 MAC (RX & TX) and BLE (RX & TX) functions.

5.7 Memory Architecture

The QPG6095 contains:

64 Kbyte RAM : Low Leakage Random Access Memory (RAM), for packet buffering and run-time data. This is split in:
50% is System RAM, accessible to the internal microcontroller and other functional blocks, and
50% is MCU RAM, accessible to the internal microcontroller only.

The contents of the RAM can be retained (or partially retained) during standby modes, but is cleared when a power-on-reset (POR) occurs.

512 Kbyte Flash : Flash memory, for program storage, calibration data and non-volatile storage of critical run-time data (e.g. pairing information and frame counters). The contents are retained under all circumstances (power-on-reset, standby).

DMA Engines : The QPG6095 has two integrated DMA Engines that relieve the microcontroller from transferring data internally between RAM and peripherals.

In addition, the QPG6095 is able to support external SPI Flash memory.

5.8 Internal Microcontroller

The internal microcontroller allows the QPG6095 to operate as a standalone system. It is a high performance 32-bit Arm Cortex-M4 processor with DSP functionality, optimized for low power consumption, performance and code size.

It runs at up to 64 MHz clock speed, and can execute code from Flash as well as from RAM, with zero wait states.

Table 2: Memory Access Speeds

Arm clock	MCU RAM access	System RAM access	Flash Memory access
16 MHz	16 MHz	16 MHz	16 MHz
32 MHz	32 MHz		32 MHz for linear code; 16 MHz worst case
64 MHz	64 MHz		

5.9 Peripherals

The QPG6095 features a set of peripherals, and allows configuration of the mapping between the IO signals needed by the peripherals and the available IO pins.

5.9.1 IO Pins

The QPG6095 features many IO pins that can be configured to predefined functional signals; see the Pin Assignments in chapter 9:

- 20 programmable General Purpose IO (GPIO) lines, plus
- 6 programmable Analog IO (ANIO) or GPIO lines (of which 2 input only), plus
- 2 pins for the optional 32 KiHz crystal IO can alternatively be used as GPIO (input only) lines, plus
- 2 pins for the optional DC/DC Converter can alternatively be used as GPIO lines.

The whole pin configuration with associated settings is retained when going to standby.

5.9.1.1 GPIO

The QPG6095 features programmable GPIO lines that are configured to predefined functional signals with following settings:

Pin pull-up/down settings : Except for GPIO36 and GPIO37, all GPIO pins can be individually weakly pulled up or weakly pulled down during active as well as standby states.
Unless specified otherwise, at power-up/reset all GPIO pins are default set in floating mode.

Drive strength : The drive strength of the GPIO output pins can be configured per group of 4 IO's (GPIO0 … GPIO3, GPIO4 … GPIO7, etc.; see also Table 33) to 4.5, 9, 13.5 or 18 mA.

High Drive Sink : On GPIO18 a high drive sink (MOSFET N-Type) can be enabled, suitable for e.g. driving a high-power IR LED circuit. Figure 4 shows an IR LED circuit with the high drive sink enabled. For comparison, Figure 5 shows an example without high drive sink.

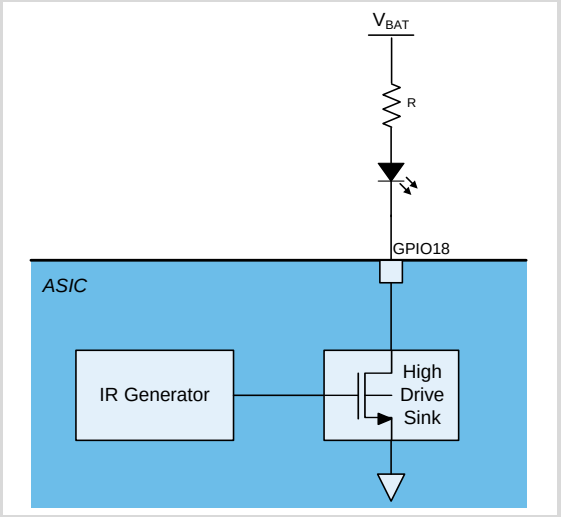


Figure 4: IR with High Drive Sink

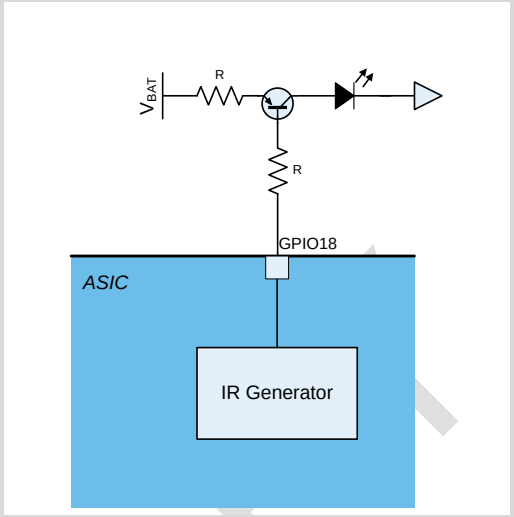


Figure 5: IR without High Drive Sink

Wake up: The IO pins GPIO0 through GPIO11, GPIO20 through GPIO26 and GPIO36 through GPIO39 can be configured as **wake-up** pin. Each of these can be configured to trigger a wake-up event on a rising edge, on a falling edge or on both edges seen on the pin.

5.9.1.2 ANIO

The QPG6095 features up to 6 ANIO lines for inputs to the ADC. ANIO0 and ANIO1 are the preferred ones as they are protected from potential interference by output signals. ANIO0 and ANIO1 can also be used for differential measurements.

5.9.2 UARTs

The QPG6095 contains two Universal Asynchronous Receiver and Transmitters (UARTs) for interfacing with additional peripheral devices, plus one for terminal logging during (software) development. The UARTs support:

- Full-duplex operation.
- Baud rates from 2400 Bd to 1 MBd.
- Serial frames with 5, 6, 7, 8 or 9 data bits and 1 or 2 stop bits, with framing error detection.
- Odd or even parity generation and checking.
- Buffer overflow detection.
- False start bit detection and digital low pass filter for robustness against noise.
- Separate interrupts on TX Complete, TX Data Register Empty and RX Complete.
- Configurable pin mappings; i.e. a RX pin and a TX pin can be made available on the QPG6095 pin-out.

5.9.3 SPI Master

The QPG6095 contains a Serial Peripheral Interface (SPI) for interfacing with additional peripheral devices. This SPI Master supports:

- Full-duplex synchronous transfers on three lines (MISO, MOSI, SCLK).
- Programmable clock polarity and phase, supports SPI mode 0, 1, 2 and 3.
- Programmable data order with MSb-first or LSb-first shifting.
- High speed clock generator supporting clock speeds up to 8 MHz.
- 4-bit to 16-bit transfer frame format selection.
- Three separate interrupts on TX Complete, TX Data Register Empty and RX Complete.

5.9.4 SPI Slave

The QPG6095 contains an SPI Slave interface. This SPI Slave supports:

- SPI mode 0
- SPI clock frequencies up to 16 MHz
- Limited to byte based operation

5.9.5 I²C Master

The QPG6095 contains a I²C (Inter-Integrated Circuit) Master interface, also referred to as Two-Wire Interface (TWI), for interfacing with additional peripheral devices. This I²C Master supports:

- Standard mode and Fast mode
- Short (7-bit) and long (10-bit) addresses
- General call address (0x00)
- Clock stretching

5.9.6 I²C Slave

The QPG6095 contains an I²C Slave interface. This I²C Slave supports:

- Standard mode and Fast mode
- Short (7-bit) and long (10-bit) addresses
- Configurable Slave Address
- General call address (0x00)

5.9.7 I²S Master

The QPG6095 contains a I²S (Inter-IC Sound) Master interface for interfacing with digital audio devices. This I²S Master supports:

- Full duplex transfers
- Configurable word length
- Left justified. Right justified mode can be emulated.
- Double buffered, DMA capable
- Clock frequency selectable from 62.5 kHz up to 8 MHz

5.9.8 Keyboard Scanner

The QPG6095 has an integrated 8x8 Keyboard Scanner with ultra-low power wake-up on key press, keyboard scan and de-bounce. The keyboard scan operation is triggered by a change on the IO (key press), as well as by a timed event (for de-bouncing). The keys are organized in a matrix. The mapping of the physical keys (row/column) to the application or profile-defined keys is software configurable. The maximum number of keyboard columns and rows depends on the number of other GPIO-devices enabled; see Table 33.

5.9.9 IR Generator

The QPG6095 has an InfraRed (IR) generator for multi-mode (RF and IR) operation and compatibility with legacy IR target devices. The IR generator supports a wide range of common IR protocols.

The IR generator supports multiple modulation modes:

- Pattern based: input is a pattern of 0's and 1's in RAM.
- Time based: input is a sequence of ON and OFF times.
- Event based: modulation is controlled by scheduled actions.

5.9.10 LED Generator

The QPG6095 supports up to 4 signaling LEDs, with configurable function and events. The LED generator supports:

- 8-bit Pulse-Width Modulation (PWM)
- Fade-in/Fade-out
- Duty cycling to adjust brightness and save power

5.9.11 PDM Microphone Interface

The QPG6095 contains a Pulse-Density Modulation (PDM) MEMS Microphone Interface, that supports:

- A Clock and Data pin for interfacing with a PDM MEMS microphone
- Optionally Capturing Data on the Rising and Falling Edge of the Clock for Stereo operations.
- Frequency of Clock signal: 2 MHz.
- HW CIC Decimation filter with programmable decimation factor (R=1…64) that converts 1-bit input samples to 16-bit output samples. HW CIC output can be connected to DMA, to allow this processing chain to be extended with further decimation, equalization, volume control and compression using the Cortex M4 DSP routines.

5.9.12 PWM Engine

The QPG6095 contains a Pulse-Width Modulation (PWM) engine, for e.g. the backlight of a display or for a speaker output, that supports:

- 16-bits real-time timer. (Note that the Event Scheduler contains a timer with a much longer time base; see section 5.10 below)
- 16-bit PWM
- Configuration of the modulation parameters
- Support for 6 PWM outputs.

5.9.12.1 Timestamping

The PWM Engine features the option to take a timestamp whenever a selected input pin changes state. This can typically be used for IR learning purposes.

- Support for 4 timestamp inputs.
- Input pin selection separate from PWM outputs.
- Hysteresis capable preprocessing.

5.9.13 Watchdog

The QPG6095 contains a Watchdog timer that serves to detect and resolve software failures and to trigger an interrupt, an internal microcontroller reset or a system reset when the timer reaches a certain timeout value. Timeout values are software configurable: 16-bit values in 16 µs resolution.

5.9.14 Intelligent Sensor Hub

The QPG6095 supports an Intelligent Sensor Hub mode for ultra-short measurement cycles for battery operated sensors, ensuring minimal battery usage for these measurements. Upon wake up from standby mode (see also section 5.10 below) measurements and calculations can be performed running on the internal system clock to determine quickly whether the system should be fully woken up (e.g. for radio transmission, requiring the 32 MHz crystal oscillator) or can go back to standby. This whole cycle is intended to take less than 100 µs.

Through software configuration, all analog input channels (ANIO, see section 5.9.1) can be connected to the ADC and to the Comparator. The battery and temperature monitor signals can also be connected to the ADC.

5.9.14.1 ADC

The QPG6095 has an integrated ADC module that can be used to monitor external analog signals via the ANIO pins (see section 5.9.1.2) as well as the power supply level and temperature.

- ANIO0 and ANIO1 can be used for differential measurements.
- The ADC runs on 4 MHz clock speed. A total of 16 cycles are needed to obtain a conversion result.

Table 23 in section 6.11 provides the ADC's accuracy and other characteristics.

5.9.14.2 Battery / Temperature Monitor

The ADC can be configured by software to monitor the power supply level and/or temperature internally; no external components are required. The power supply level and temperature are measured separate from the ANIO pins.

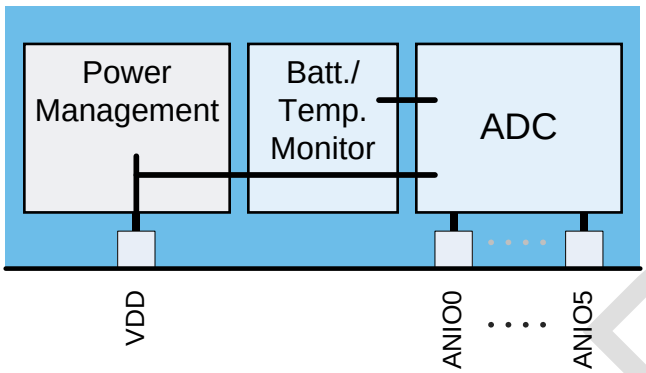


Figure 6: Battery / Temperature Monitor

5.9.14.3 Comparator

The QPG6095 features a low power comparator that can be used to trigger events to wake up the chip and/or trigger an action. The low power analog comparator can be connected to analog input(s). It supports 4 slots, allowing for time multiplexed measurements on different channels and with different threshold configurations. The comparator can be configured to combine such measurements to 'windowed' events (i.e. value is between 2 configurable levels).

5.9.15 Clock Output

The QPG6095 can provide a clock to peripheral devices (CLK_OUT). The clock frequency is derived from the 32 MHz crystal oscillator system clock. It can be configured for:

- 1, 2, 4, or 8 MHz clock with 50% duty cycle
- 16 MHz pulse blanked clock.

5.10 Timing and Control

The QPG6095 is designed to work in an environment where low power consumption is very important. To achieve the low power consumption in between receive and transmission cycles, the QPG6095 can be put in a standby (or sleep) state.

Following are the reasons for the QPG6095 to wake up:

- An event is detected on one of the IO lines (falling edge or rising edge).
- The voltage of an analog IO goes over or under a configurable threshold.
- It is time for a scheduled action.

The QPG6095 features a highly accurate and adaptive timing engine. The time base spans up to 30 minutes with a 1 µs resolution, and can be maintained during the standby modes. It can be used to autonomously and periodically schedule actions listed below in a just-in-time manner, improving the overall energy consumption of the system:

- Transmission of a packet from a TX queue.
- Enabling/disabling the receiver.
- Triggering a keyboard scan
- Switch on/off IR modulation
- Trigger ADC measurement cycle
- Trigger analog measurements
- Interrupt and wake up the microcontroller.

5.10.1 Oscillator Settings

The QPG6095 includes the following oscillators:

32 MHz crystal oscillator, based on the required external 32 MHz crystal. This is used as main system clock and reference frequency to obtain the desired RF performance.

Internal system clock. This internal clock generator is used for fast start-up and initial processing. Its frequency is close to 32 MHz but its frequency accuracy is insufficient for RF performance. It can also be used for the Intelligent Sensor Hub, enabling minimum wake-up time to perform analog measurements.

32 kHz RC oscillator. This can be used for less accurate timing during standby. Also, if more accurate timing during standby is needed, this can be achieved by regularly waking up the device to calibrate the 32 kHz RC oscillator based on the 32 MHz crystal oscillator.

Optional **32 KiHz crystal oscillator**, based on the optional external 32 KiHz crystal. This oscillator can be used to optimize the power consumption if more accurate timing during standby is needed, as it allows to avoid the regular wake up cycles to calibrate the 32 kHz RC oscillator. This can be a relevant power optimization in use cases where the device spends a significant amount of its operation in standby with highly accurate timing requirements.

5.10.2 Standby Modes

The QPG6095 supports the following standby modes (see section 6.3 Table 6 for the power consumption):

XT Standby mode : A low power mode that requires no reconfiguration (partial or full state retention). The time base for the Event Scheduler is delivered by the 32 MHz crystal oscillator.

RC Standby mode : A low power mode that requires no reconfiguration (partial or full state retention). The time base for the Event Scheduler is delivered by the internal 32 kHz RC oscillator.

32KiHz Standby mode : An optional low power mode that requires no reconfiguration (partial or full state retention). The time base for the Event Scheduler is delivered by the oscillator based on the optional 32 KiHz crystal.

In all standby modes, the QPG6095 can be programmed to also be woken up by an external event.

5.11 Power Management

The QPG6095 has an integrated power management system which includes a Buck DC/DC Convertor and a Global Low Dropout Regulator (GLDO). This generates an internal 1.8 V power supply by using either the DC/DC Converter or the GLDO. The chip always powers up using the Global LDO where after the DC/DC Converter can be enabled or disabled by the application program. When the DC/DC Converter is enabled, the GLDO is turned off and the power consumption of the chip can be reduced by up to 33% (assuming Max TX power and VDD = 3 V).

The internal 1.8 V power rail is used to supply separate local LDO regulators feeding RF/analog and digital blocks. The local LDOs used to supply RF/analog blocks are specially designed to have high power supply rejection ratio (PSRR) to suppress the supply ripples generated in DC/DC mode.

5.11.1 DC/DC Converter

The QPG6095 has an integrated Buck-type DC/DC Converter that can be enabled to reduce the power consumption of the chip. The DC/DC converter uses two low-cost off-chip components as shown in Figure 7 below; see Table 27 for the required values. It converts the battery supply voltage to a lower voltage used to supply the local LDOs for RF/analog and digital blocks. Ripple on the internal power supply generated by the DC/DC is filtered by the local LDOs to provide a clean supply to the RF/analog blocks.

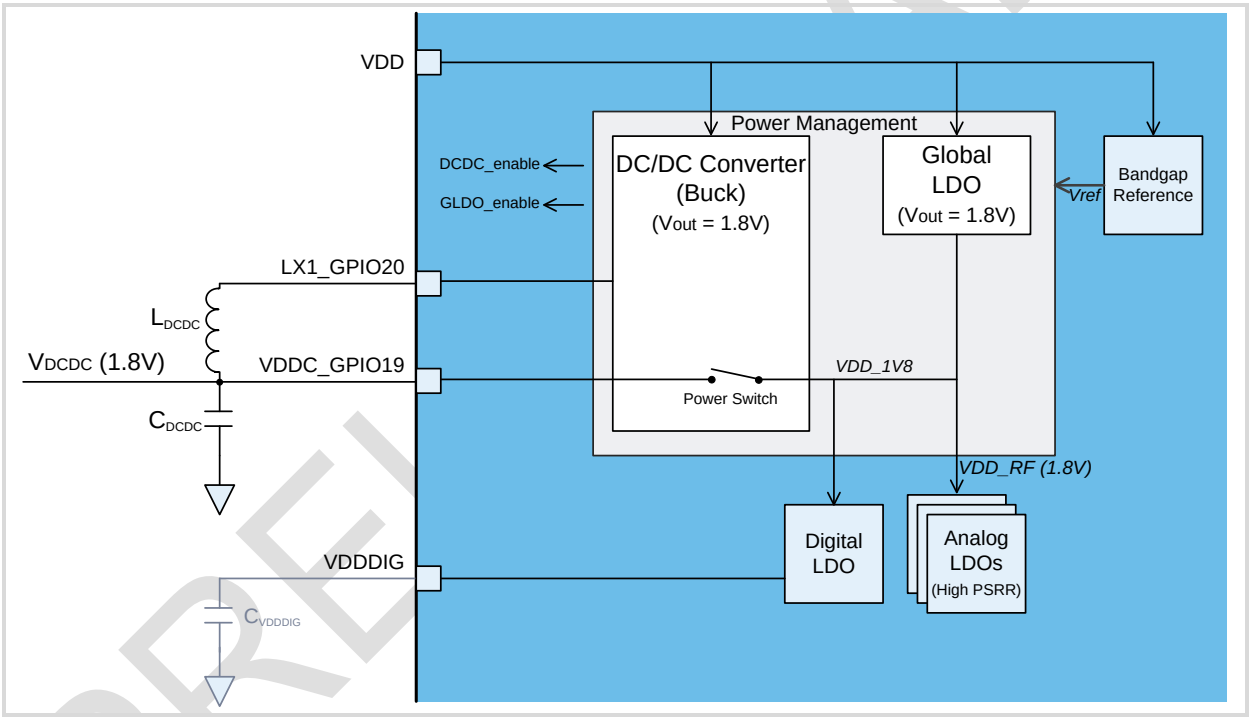


Figure 7: DC/DC Converter

The QPG6095 offers full flexibility to the application program to enable or disable the DC/DC Converter after the chip is powered up and out of standby mode. During standby mode, the DC/DC Converter is disabled to save power. In this mode, the power switch is turned off and the external capacitor retains its charge to allow fast wake up from standby mode.

If an application does not make use of the DC/DC Converter, the two external components are not required to be placed. In this case, the Global LDO is used to generate the internal power supply and the two pins of the DC/DC Converter can also be configured to be used as GPIOs (GPIO19 and GPIO20).

5.11.2 Low Voltage Behavior

The QPG6095 contains following features that can be combined to implement the desired low voltage behavior:

VDD Brown-out Interrupt : Interrupt that can be software configured to trigger when VDD drops below the VDD Brown-out threshold while being active. This interrupt can be used to trigger the software to disable the radio and go into standby mode. A higher value gives the application more time for state cleanup.

The VDD Brown-out threshold is software configurable: 1.80, 1.85, 1.90 or 1.95 V; default value is 1.80 V.

VMT : Voltage Minimum Threshold (VMT) that can be software configured, under which the chip will not wake up from standby mode.

VMT range = 1.6 ... 3.1 V (default value is 1.6 V).
VMT crossing detection time is 125 µs.

Cut-Off : A VDD threshold under which all functions are disabled and current consumption is strictly limited.

Cut-Off threshold = 1.6 V (fixed).
Cut-Off crossing detection time is 125 µs.

Power On Reset voltage level at which the chip will start up:

Maximum = 1.8 V.

6 Electrical Characteristics

The QPG6095 characteristics are determined in the circuit shown in Figure 8 below:

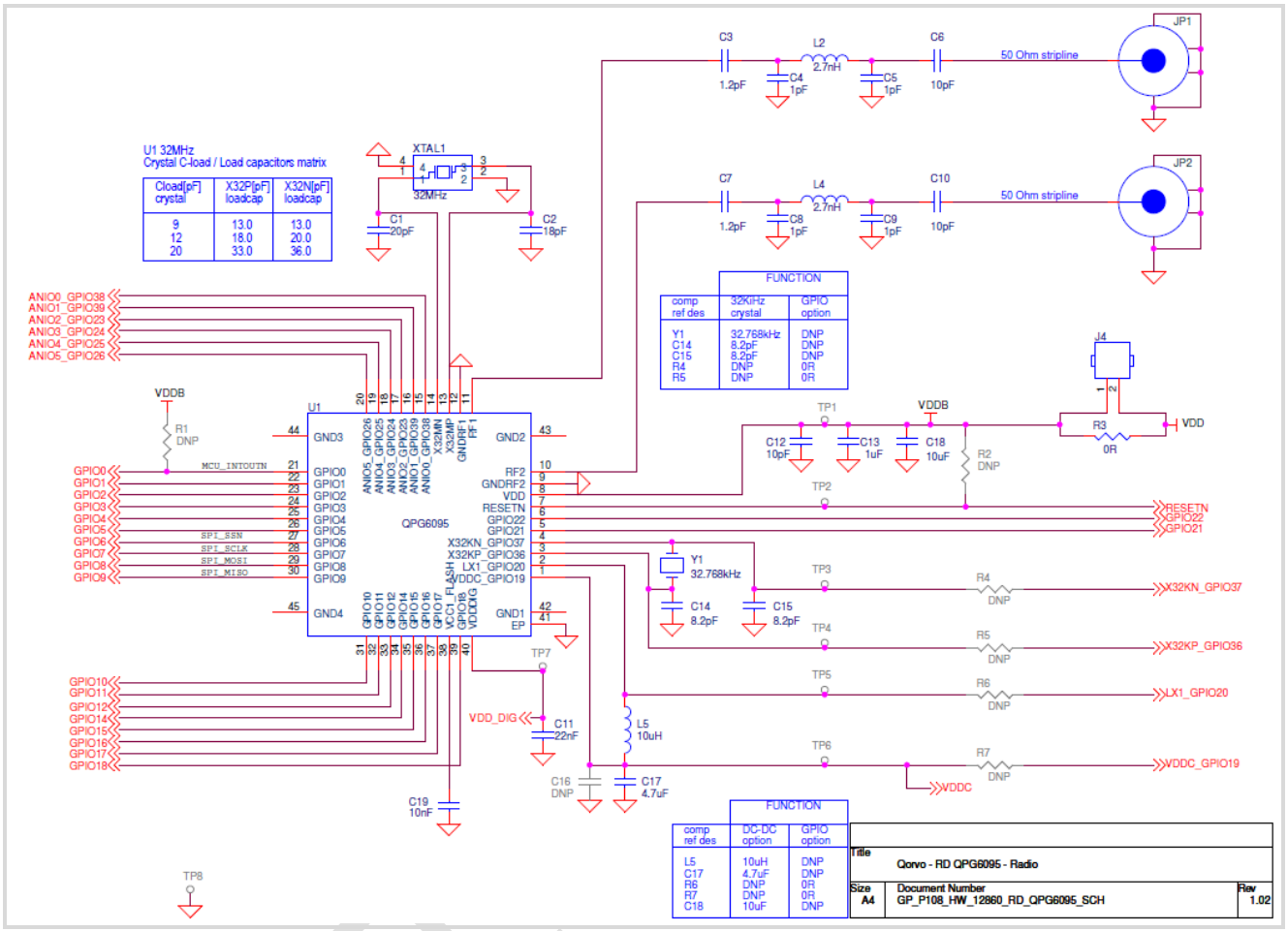


Figure 8: Parameter Evaluation Circuit

Some component values depend on the application of the DC/DC Converter:

Table 3: DC/DC Converter Components

Component Reference	With DC/DC Converter	Without DC/DC Converter
L5	10 µH	DNP
C17	4.7 µF	DNP
R6	DNP	0 Ω
C18	10 µF	DNP

- Current consumption values for transmit and receive are specified with and without the DC/DC Converter enabled.
- Transmit as well as receive behavior is measured in accordance with the IEEE 802.15.4 specification and the Bluetooth Test Specification (RF-PHY.TS.4.2.1).
- All parameters are measured at VDD = 3.0 V and T_A = 25 °C, unless otherwise specified.
- IEEE 802.15.4 channel rejection is measured with the QPG6095 reference design system as interferer.

6.1 Absolute Maximum Ratings

Table 4: Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
VDD	Supply Input Voltage		-0.3 to +3.6	V
All Digital pins (see Table 32)	Digital IO Voltage		-0.3 to VDD+0.3 (Max = +3.6)	V
ANIO0…ANIO5 pins	Analog IO Voltage		-0.3 to +3.6	V
All other Analog pins (see Table 32)	Analog IO Voltage		-0.3 to +1.32	V
VDDDIG	Decoupling Voltage		-0.3 to +1.32	V
VCC1_FLASH	Decoupling Voltage		-0.3 to +1.95	V
RF1, RF2	RF IO Voltage		-0.3 to +3.6	V
P_{MAX}	Input RF level		+10	dBm
T_J	Junction Temperature		+125	°C
T_{stg}	Storage Temperature		-50 to +150	°C
T_{sol}	Reflow Soldering Temperature		+260	°C
	ESD HBM (AEC - Q100-002 Human Body Model)	non-RF pins:	2000	V
		RF pins:	1250	
	ESD CDM (AEC - Q100-011 Charged Device Model)	non-RF pins:	750	V
		RF pins:	750	

6.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
VDD	Power Supply Voltage			1.8	3.3	3.6	V
T_A	Ambient Temperature			-40	+25	+105	°C
F_{ref}	Reference Crystal Oscillation Frequency				32		MHz
V_{IL}	Input Low Voltage for all GPIO lines	Logical value (functional)	VDD = 1.8 V			0.6	V
			VDD = 3.3 V			1.1	
			VDD = 3.6 V			1.3	
		Analogue value (prevents leakage current)				0.25	V
V_{IH}	Input High Voltage for all GPIO lines	Logical value (functional)	VDD = 1.8 V	0.9			V
			VDD = 3.3 V	1.8			
			VDD = 3.6 V	2.0			
		Analogue value (prevents leakage current)		VDD – 0.25			V

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{OL}	Output Low Voltage for all GPIO lines (For GPIO18 with high drive sink, refer to section 6.15)	VDD	Drive Strength(*)	I_{OL}(**)				
		1.8 V	4.5 mA	4.5 mA		0.4	0.6	V
			9 mA	9 mA		0.4	0.6	
			13.5 mA	13.5 mA		0.5	0.6	
			18 mA	18 mA		0.5	0.6	
		3.3 V	4.5 mA	4.5 mA		0.20	0.35	V
			9 mA	9 mA		0.20	0.35	
			13.5 mA	13.5 mA		0.25	0.40	
			18 mA	18 mA		0.25	0.40	
		3.6 V	4.5 mA	4.5 mA		0.20	0.35	V
			9 mA	9 mA		0.20	0.35	
			13.5 mA	13.5 mA		0.25	0.40	
			18 mA	18 mA		0.25	0.40	
V_{OH}	Output High Voltage for all GPIO lines	VDD	Drive Strength(*)	I_{OH}(**)				
		1.8 V	4.5 mA	-4.5 mA	1.1	1.3		V
			9 mA	-9 mA	1.1	1.3		
			13.5 mA	-13.5 mA	1.0	1.2		
			18 mA	-18 mA	1.0	1.2		
		3.3 V	4.5 mA	-4.5 mA	2.8	3.1		V
			9 mA	-9 mA	2.8	3.1		
			13.5 mA	-13.5 mA	2.7	3.0		
			18 mA	-18 mA	2.7	3.0		
		3.6 V	4.5 mA	-4.5 mA	3.1	3.4		V
			9 mA	-9 mA	3.1	3.4		
			13.5 mA	-13.5 mA	3.0	3.3		
			18 mA	-18 mA	3.0	3.3		
notes:	* Refer to section 5.9.1.1 for applicability. ** I_{OL} / I_{OH} : positive value: pin is sinking current; negative value: pin is sourcing current.							
I_{OH}	Total sourced current for all GPIO output lines combined (excluding the high drive of GPIO18)						100	mA
T_{INT}	Pulse width for GPIO interrupts				250			ns

6.3 Current Consumption

Table 6: Current Consumption - Common

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{idle}	Idle Modes	Arm asleep		1.5		mA
	(Current consumption in the 'Arm running' modes depends on the user program. Given numbers are max currents for reference program used.) (typical XTAL 32 MHz running)	Arm running from RAM @ 16 MHz		2.4		
		@ 32 MHz		3.0		
		@ 64 MHz		5.0		
		Arm running from Flash @ 16 MHz		3.8		
		@ 32 MHz		5.0		
$I_{standby}$	Standby Modes	RC Standby mode; 8 KB RAM retained		1.1		µA
		16 KB RAM retained		1.3		
		32 KB RAM retained		1.6		
		64 KB RAM retained		2.1		
		32 KiHz Standby mode; 8 KB RAM retained		1.2		
		16 KB RAM retained		1.4		
		32 KB RAM retained		1.7		
		64 KB RAM retained		2.2		
	(Current consumption depends on crystal specification and load capacitance, see section 6.9 below)	XT Standby mode		760		
	Current increase by activated comparator (measurement frequency dependent)	Measurement frequency = 32 kHz		0.3		
I_{reset}	Reset Mode			50		µA

Table 7: Current Consumption - IEEE 802.15.4

Symbol	Parameter	Conditions		Min	Typ	Max*	Unit
I_{active}	Active Modes (Operating in IEEE 802.15.4 channel 20)	DC/DC enabled VDD = 3.6 V V_{DCDC} = 1.8 V	RX, single antenna		3.5	3.7	mA
			RX, single channel, with antenna diversity		4.4	4.6	
			RX, multi-channel, with antenna diversity		6.7	7.0	
			TX @ 0 dBm		8.7	9.5	
			TX @ max power		22	22.5	
		DC/DC enabled VDD = 3.0 V V_{DCDC} = 1.8 V	RX, single antenna		4.0	4.2	
			RX, single channel, with antenna diversity		5.1	5.3	
			RX, multi-channel, with antenna diversity		7.8	8.2	
			TX @ 0 dBm		10.2	11.8	
			TX @ max power		26	27	
		DC/DC disabled	RX, single antenna		5.7	6.0	
			RX, single channel, with antenna diversity		7.4	7.6	
			RX, multi-channel, with antenna diversity		11.5	11.8	
			TX @ 0 dBm		15.2	17.6	
			TX @ max power		38	39	

***** Max is defined over process and voltage at 25 ˚C.

Table 8: Current Consumption - BLE

Symbol	Parameter	Conditions		Min	Typ	Max*	Unit
I_{active}	Active Modes	DC/DC enabled VDD = 3.6 V V_{DCDC} = 1.8 V	RX		7.1	7.5	mA
			TX @ 0 dBm		8.7	9.5	
			TX @ max power		22	22.5	
		DC/DC enabled VDD = 3.0 V V_{DCDC} = 1.8 V	RX		8.3	8.8	
			TX @ 0 dBm		10.2	11.8	
			TX @ max power		26	27	
		DC/DC disabled	RX		12.3	12.8	
			TX @ 0 dBm		15.2	17.6	
			TX @ max power		38	39	

***** Max is defined over process and voltage at 25 ˚C.

6.4 Receiver Characteristics

Table 9: Receiver Characteristics - Common

Parameter	Conditions	Min	Typ	Max	Unit
RSSI range (assuming the HAL is used, see sections 5.1.3 and 8.1)	5 dB accuracy	-95		-50	dBm
	Resolution:		1		dB
LO leakage	2.4 GHz			-47	dBm
	4.8 GHz			-47	

Table 10: Receiver Characteristics - IEEE 802.15.4

Parameter	Conditions	Min	Typ	Max	Unit
RF channels	Programmable in 5 MHz steps as defined by IEEE 802.15.4	2405		2480	MHz
Bit rate			250		kbit/s
Chip rate			2.0		Mchip/s
Receiver sensitivity	as defined in IEEE 802.15.4 (Measured in IEEE 802.15.4 channel 20)				dBm
	Single channel listening		-100	-99	
	Multi-channel listening (signal at both antenna ports)		-99	-98	
	Max is defined over process and voltage at 25 ˚C				
	Antenna Diversity Gain (refer to section 5.2.2 for the channel model)		8		dB
RX carrier frequency offset range	Sensitivity loss < 1 dB	-160		+220	kHz
Maximum receive level	1% PER as defined in IEEE 802.15.4		10		dBm
IIP3	RX mode		-9		dBm
P-1dB RF front-end	RX mode		-19		dBm
Co-Channel rejection	Packet in Packet collision		-12		dB
	Non IEEE 802.15.4 Interference (noise)				dB
	single antenna		-5.3		
	with antenna diversity		-4.8		
Adjacent channel rejection	as defined in IEEE 802.15.4. IEEE 802.15.4 interferer, +/- 5 MHz		32		dB
Alternate adjacent channel rejection	as defined in IEEE 802.15.4. IEEE 802.15.4 interferer, +/- 10 MHz		48		dB
Far away channel rejection	wanted signal at -82 dBm. IEEE 802.15.4 interferer, +/- 15 MHz		62		dB
Wi-Fi IEEE 802.11n rejection	wanted signal at -82 dBm; Wi-Fi centered at +12 MHz / -13 MHz or higher offset frequency		25		dB
Bluetooth rejection (fixed carrier, rejection of FSK modulated signal with frequency deviation +/- 160 kHz, BT=0.5)	wanted signal at -82 dBm, Bluetooth carrier at:				dB
	+/-4 MHz		30		
	+/-6 MHz		52		

Parameter	Conditions	Min	Typ	Max	Unit
Blocking / desensitization (e.g. mobile phone signal rejection)	(Measured according to ETSI EN 300 440-1 V1.6.1; 2010-08).				
	-100 MHz from lower band edge		-11		dBm
	-40 MHz from lower band edge		-13		
	-20 MHz from lower band edge		-14		
	+20 MHz from upper band edge		-14		
	+40 MHz from upper band edge		-12		
	+100 MHz from upper band edge		-10		

Table 11: Receiver Characteristics - BLE

Parameter	Conditions	Min	Typ	Max	Unit
RF channels	Channel spacing in 2 MHz steps	2402		2480	MHz
Frequency error tolerance		-250		250	kHz
Bit rate			1		Mbit/s
Extended Bit rate			2		Mbit/s
Symbol rate			1		Msymbol/s
Extended Symbol rate			2		Msymbol/s
Data rate error tolerance		-500		+500	ppm
Receiver sensitivity	* (TP/RCV-LE/CA/BV-01-C, TP/RCV-LE/CA/BV-02-C); BER = 10^{-3} (Measured in BLE channel 0 = 2402 MHz)		-96	-94	dBm
	Note: Sensitivity in BLE channels 6, 13, 21 and 29 can be:			-91	
Receiver saturation	* (TP/RCV-LE/CA/BV-06-C); BER = 10^{-3}		10		dBm
Co-Channel rejection	Wanted signal at -67 dBm, modulated interferer in channel, BER = 10^{-3}		-9		dB
Selectivity	* (TP/RCV-LE/CA/BV-03-C); Wanted signal at -67 dBm, BER = 10^{-3}, modulated interferer at:				
	-5 MHz or more		56		dB
	-4 MHz		52		
	-3 MHz		48		
	-2 MHz		37		
	-1 MHz		9		
	+1 MHz		7		
	+2 MHz		32		
	+3 MHz = image frequency -1 MHz		36		
	+4 MHz = image frequency		25		
	+5 MHz or more = image frequency +1 MHz		41		
Out-of-band blocking	* (TP/RCV-LE/CA/BV-04-C);				
	30 ... 2000 MHz		2.7		dBm
	2003 ... 2399 MHz		-4.8		
	2484 ... 2997 MHz		-2.5		
	3000 MHz ... 12.75 GHz		3.0		

Parameter	Conditions	Min	Typ	Max	Unit
Intermodulation	* (TP/RCV-LE/CA/BV-05-C); Wanted signal at 2402 MHz, at -64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level.		-28		

Note: * As defined in Bluetooth Test Specification RF-PHY.TS.4.2.1, and for 1 Mbit/s bit rate.

6.5 Transmitter Characteristics

Table 12: Transmitter Characteristics - Common

Parameter	Conditions	Min	Typ	Max	Unit
Maximum TX output power			10		dBm
Minimum TX output power	Active TX		-24		dBm
TX output power variation	Over temperature range		3	4	dB
TX Harmonics	Conducted measurement at 0 dBm output power (1 MHz resolution bandwidth, average power and modulated carrier)			-42	dBm
TX out of band emissions	Measured at 0 dBm output power, modulated signal, on all IEEE 802.15.4 and BLE channels. (1 MHz resolution bandwidth, average power)				dBm
	< 2390 MHz			-42	
	> 2483.5 MHz			-42	

Table 13: Transmitter Characteristics - IEEE 802.15.4

Parameter	Conditions	Min	Typ	Max	Unit
RF channels	Programmable in 5 MHz steps as defined by IEEE 802.15.4	2405		2480	MHz
Bit rate			250		kbit/s
Chip rate			2.0		Mchip/s
EVM			14	22	%

Table 14: Transmitter Characteristics - BLE

Parameter	Conditions	Min	Typ	Max	Unit
RF channels	Channel spacing in 2 MHz steps	2402		2480	MHz
Bit rate			1		Mbit/s
Extended Bit rate			2		Mbit/s
Symbol rate			1		Msymbol/s
Extended Symbol rate			2		Msymbol/s
In-band emissions	* (TP/TRM-LE/CA/BV-03-C, TP/TRM-LE/CA/BV-04-C)				
	+/-2 MHz		-35	-20	dBm
	+/-(3+n) MHz (n=0,1,2…)		-38	-30	
Frequency deviation	* (TP/TRM-LE/CA/BV-05-C)				
	$\Delta f1_{avg}$	225		275	kHz
	$\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8			

Note: * As defined in Bluetooth Test Specification RF-PHY.TS.4.2.1, and for 1 Mbit/s bit rate.

6.6 Digital Timing Characteristics

Table 15: SPI Slave Timing Characteristics

Symbol	Parameter	Reference (Figure 9)	Min	Typ	Max	Unit
F_{SCLK}	SCLK frequency	t1	0		16	MHz
	SCLK duty cycle clock			50		%
	MOSI setup time	t2	20			ns
	MOSI hold time	t3	20			ns
	SCLK low to MISO valid time	t4			31.25	ns
	SSn setup time	t5	31.25			ns
	SSn high to MISO tri-state	t6			31.25	ns

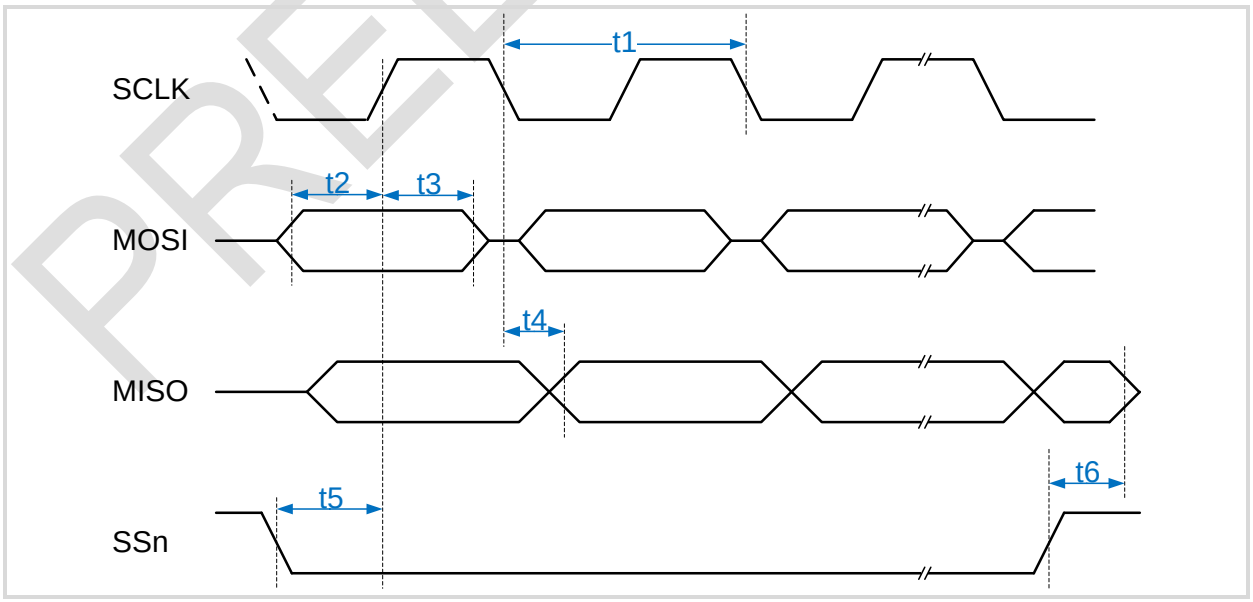


Figure 9: SPI Slave Signaling Timing Diagram

Table 16: I²C Timing Characteristics

Symbol	Parameter	Reference (Figure 10)	Standard Mode		Fast Mode		Unit
			Min	Max	Min	Max	
F_{SCL}	SCL frequency	t1		100		400	kHz
t_{HIGH}	Clock High Time	t2	4		0.6		µs
t_{LOW}	Clock Low Time	t3	4.7		1.3		µs
$t_{SU;STA}$	START condition setup time	t4	4		0.6		µs
$t_{HD;STA}$	START condition hold time	t5	4.7		0.6		µs
$t_{HD;DAT}$	Data hold time	t6	0		0		µs
$t_{SU;DAT}$	Data setup time	t7	0.25		0.1		µs
$t_{SU;STO}$	STOP condition setup time	t8	4		0.6		µs
t_{BUF}	Bus free time between a STOP and a START condition	t9	4.7		1.3		µs

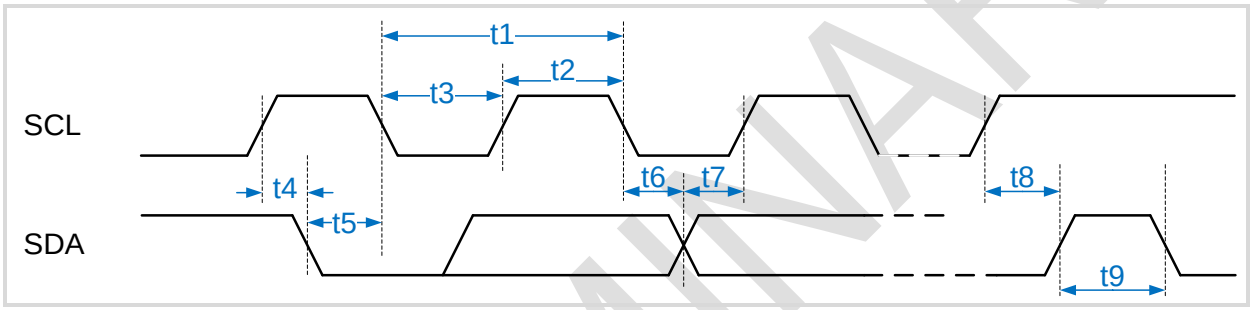


Figure 10: I²C Signaling Timing Diagram

6.7 Reset, Wake up and Standby Timing Characteristics

Table 17: Reset, Wake up and Standby Timings

Application use cases	Remarks	Min	Typ	Max	Unit
Power on detect	See Figure 11 below.		0.8	20	ms
From Power on detect, until Program starts running (*) (**)	See Figure 11 below.		520		µs
External Reset, until Program starts running (*) (**)	See Figure 12 below.		520		µs
RESETN pulse width	See Figure 12 below. The RESETN is asynchronous. A practical minimum is 10 ns.				
Go to RC Standby mode, from application command (*)	8 KB RAM retained		120		µs
Go to XT Standby mode, from application command				1	µs
Go to 32KiHz Standby mode, from application command	Value is dominated by the startup time of the 32 KiHz crystal oscillator (see section 6.9.2). Typically, this can go up to 500 ms.		150		ms
Wake up from RC or 32KiHz Standby mode, until Program starts running (*) (**)	8 KB RAM retained; other RAM not re-initialized.		180		µs
Wake up from XT Standby mode, until Program starts running (*)				1	µs
Note * : The Program is responsible for backup/restore of operational data as required by the application. The time required for this is not included in the values specified above.	backup: restore:		40 40		µs
Note ** : To enable RF reception or transmission, the 32 MHz crystal oscillator has to be started:					
Prepare for RX/TX, when 32 MHz crystal oscillator is not yet running	See Figure 11 and Figure 12 below. Value is dominated by the startup time of the 32 MHz crystal oscillator (see section 6.9.1)		2		ms

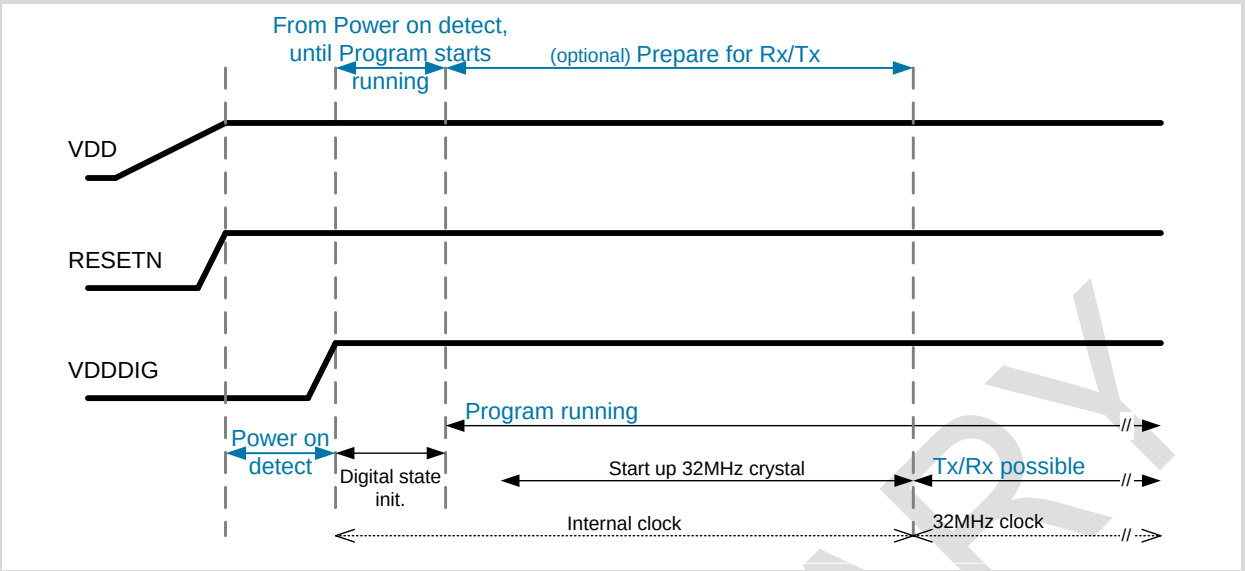


Figure 11: Power On Timing (not to scale)

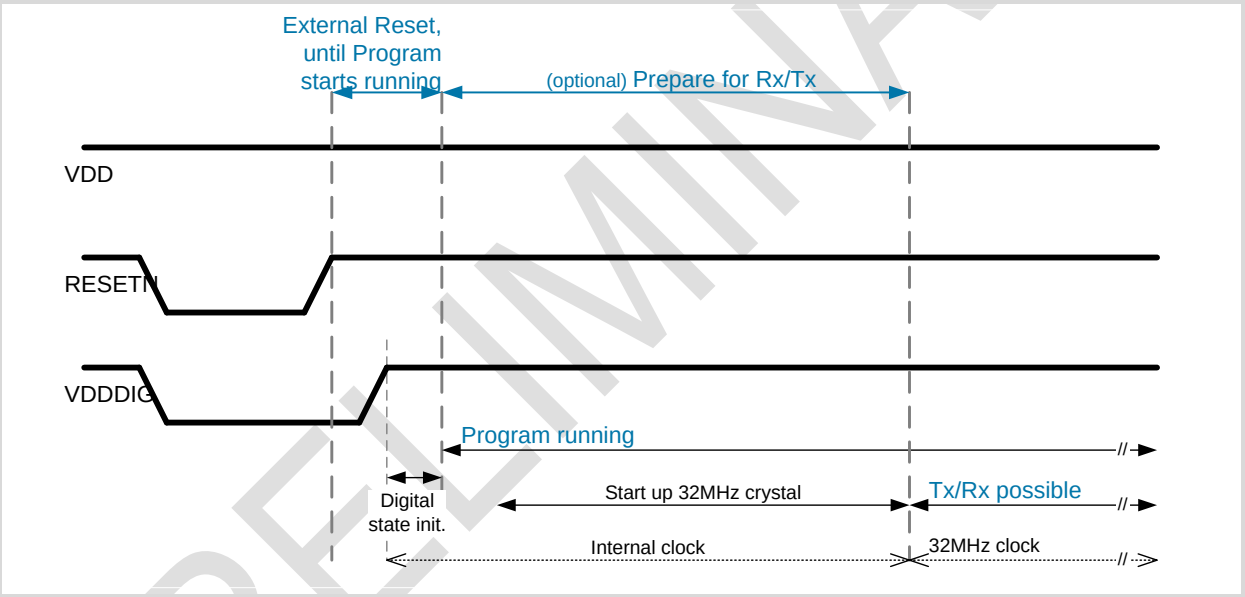


Figure 12: External Reset Timing (not to scale)

6.8 Flash Memory Characteristics

Table 18: Flash Memory Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Retention period	105°C	10			year
	Number of ERASE cycles		100k			
	VDD for programming	Zero source resistance	1.8		3.6	V
	Sector size			512		byte
T_{WR}	Write time (256 bytes)	Physical operations, so excluding software overhead and transmission times			2	ms
T_{PE}	Sector Erase time		2		2.5	
T_{BE}	Bulk Erase time		8		10	
I_{WR}	Write current	Average delta current		4		mA
I_{PE}	Sector Erase current			4		
I_{BE}	Bulk Erase current			4		

6.9 Crystal Oscillator Specifications

6.9.1 The 32 MHz Crystal Oscillator

The 32 MHz crystal oscillator is an AGC controlled oscillator that provides a high gain at start-up, to assure fast start-up times, and low gain when running, to minimize current consumption. It generates the system clock for the QPG6095 and can also be used as time base generation.

Some QPG6095 characteristics are crystal dependent. For reliable operation and to meet the specified standby current and startup time the crystal should comply with the Qorvo Procurement Specifications for the crystal. These Specifications are available from Qorvo upon request; see Table 19 below. Qorvo can also provide service to evaluate other crystals.

Table 19: 32 MHz Crystal Specifications

Package	Size	Type	Procurement Specification
Thru-Hole or SMD	Metal can	HC-49S 2 leads	GP_P007_PS_06541
SMD	3.2 x 2.5 mm	4 pads SMD	GP_P007_PS_06542
SMD	2.5 x 2.0 mm	4 pads SMD	GP_P007_PS_06544
SMD	2.0 x 1.6 mm	4 pads SMD	GP_P007_PS_06543

Figure 13 shows the typical configuration of the oscillator. The values of the external load capacitors (CL) are crystal type dependent.

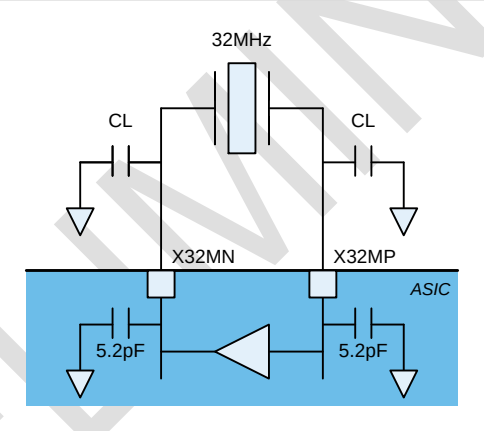


Figure 13: Typical 32 MHz Crystal Configuration

6.9.2 The 32 KiHz Crystal Oscillator (optional)

The 32.768 kHz (in short: 32 KiHz) crystal oscillator is optional and can be used for ultra-low power time base generation for the Event Scheduler with high accuracy. This high accuracy is required for BLE long standby timing. A side effect of this low power consumption is that the start-up time of the 32 KiHz oscillator is very dependent on the crystal and the capacitive load on the X32K oscillator pins. Within the operational temperature range, the 32 KiHz oscillator will always start within one second (At 25°C the start-up time is less than 0.5 s). The application must make sure that the QPG6095 does not enter the 32 KiHz standby mode before the 32 KiHz oscillator is stable.
For reliable operation and to meet the specified characteristics the crystal should comply with the Qorvo Procurement Specifications; see Table 20. These Specifications are available from Qorvo upon request. Qorvo can also provide service to evaluate other crystals.

Figure 14 shows the typical configuration of the oscillator. The values of the external load capacitors (CL) are crystal type dependent as specified in Table 20.

Table 20: 32 KiHz Crystal Specifications

Procurement Specification	Load Capacitance Value (CL)
GP_P004_PS_03122	8.2 pF
GP_P008_PS_13494 (Version 2.00 or higher)	8.2 pF

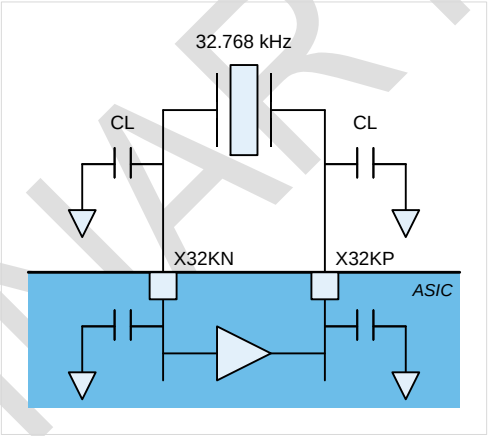


Figure 14: Typical 32 KiHz Crystal Configuration

6.9.2.1 The 32 KiHz Crystal Oscillator for Devices Subject to Mechanical Shock

32 KiHz Crystals may be susceptible to mechanical shock, causing disturbance to the 32 KiHz crystal oscillator that may introduce time base errors. This susceptibility to mechanical shock depends on the usage and mechanical design of the product, and on the package of the crystal. Whether the oscillator disturbance causes operational errors is application dependent: how long and how well does the product need to stay synchronized with the target device in 32 KiHz standby mode.

For devices subject to mechanical shock, Qorvo recommends a 32 KiHz crystal oscillator configuration with higher amplitude; see Table 21 and Figure 15:

Table 21: 32 KiHz Crystal Specifications for Devices Subject to Mechanical Shock

Procurement Specification	Load Capacitance Value (CL)	Pull-Up (R)
GP_P008_PS_13779	15 pF	15 MΩ

Note: This configuration increases the current consumption in 32 KiHz Standby Mode, as specified in section 6.3, by 0.2 µA.

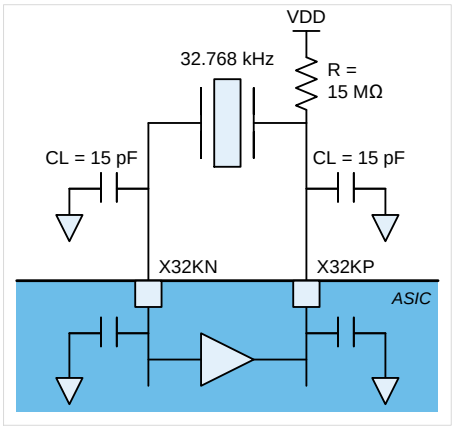


Figure 15: 32 KiHz Crystal Configuration for Devices Subject to Mechanical Shock

6.10 Internal Pull-up / Pull-down Characteristics

Table 22: Internal Pull-up / Pull-down Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Internal pull-up resistance	VDD=3.3V, T_A=25ºC		41		kΩ
	Internal pull-down resistance	VDD=3.3V, T_A=25ºC		42		kΩ

6.11 ADC Characteristics

Table 23: ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Resolution	Sample rate up to 250 000 sample/s		10		bits
		Integration factor 16, sample rate up to 15 625 sample/s		12		bits
V_{IN}	Measurement range	At the ANIO pin	0		3.6	
	Note: The ADC contains a scaler, which allows several measurement ranges.					
	Channel switching time	(The ADC uses 16 clock cycles for a conversion)		4		µs
	Conversion time			4		µs
	Offset	Calibrated; gain=1x, single ended		2.4		mV
	Gain error	Calibrated; gain=1x, single ended		3		LSb
	Reference variation (over temperature)			10		LSb
	Note: The reference (=2x bandgap voltage) variation will also translate to a gain error.					
INL	Integral Nonlinearity	Single ended, Scaler gain=1x		2		LSb
		Differential measurement		1		
DNL	Differential Nonlinearity	Differential measurement		> -1		LSb

6.12 Battery / Temperature Monitor Characteristics

Table 24: Battery / Temperature Monitor Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Battery level range		1.8		3.6	V
	Resolution of battery level measurement	At 3.6V		10		mV
	Accuracy of battery level measurement	Typ at 3.6V. Max over process, voltage and temperature.		25	60	mV
	temperature measurement range		-40		+105	°C
	Resolution of temperature measurement			1.4		°C
	Accuracy of temperature measurement	Range -5 ... +40°C		3		°C
		Ranges -40 ... -5°C and +40 ... +105°C		5		

6.13 Comparator Characteristics

Table 25: Comparator Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Resolution			VDD/64		V
	Threshold level error				1	LSb
	Increase of current consumption in Standby Mode	Measurement frequency = 32 kHz		0.3		µA

6.14 DC/DC Converter Characteristics

Table 26: DC/DC Converter Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BATT_BUCK}	Battery voltage in BUCK mode		2.2	3.0	3.6	V
	Note: For efficiency reasons, it is advised to disable the DC/DC Converter when the input voltage gets below the Minimum.					
VDDC	Output voltage		1.65	1.8	1.9	V
V_{ripple}	Ripple in output voltage				5	mV
$T_{startup}$	Startup time	Cold start		350	500	µs
	Efficiency			85		%

Table 27: DC/DC Converter External Components Requirements

Symbol	Component	Requirement	Min	Typ	Max	Unit
L_DCDC	DCDC inductor	Inductance		10		µH
		Characterization has been done with the following part: Manufacturer: TDK Part Number: MLZ2012M100WT000				
C_DCDC	DCDC capacitor	Capacitance		4.7		µF

6.15 GPIO18 High Drive Sink Characteristics

Table 28: High Drive Sink Characteristics

Symbol	Parameter	Remarks	Min	Typ	Max	Unit
I_{MAX}	Current handling	Advised max current, going beyond may reduce lifetime and might cause failure or increased leakage			600	mA
I_{OFF}	Off / leakage current	Leakage current when driver is not sinking current		0.1	0.5	µA
R_{ON}	On resistance	Equivalent resistance when driver is sinking current		0.75	1.0	Ω
T_{RISE}	Rise time of the current	Time to reach 90% of the target end voltage. Measured with VDD = 3.6 V and external load resistor of 5 Ω (leading to a 600 mA current when active)		20	50	ns
V_{OL}	Output Low Voltage	At 600 mA continuous current				
		VDD = 2.2 V		0.65	0.75	
		VDD = 3.3 V		0.50	0.55	V
		VDD = 3.6 V		0.45	0.55	

7 Application Circuit

Qorvo provides reference designs for typical applications, suitable for systems targeting compliance with EN 300 328 and EN 300 440 class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (Japan). Please contact Qorvo Support.

8 Application Programming Information

Arm Programming Information:

Available from Arm:

- Generic User Guide, Cortex™-M4 Devices (document DUI 0553A), http://infocenter.arm.com/help/topic/com.arm.doc.dui0553a/DUI0553A_cortex_m4_dgug.pdf.

Available from Qorvo:

- Software Development Kit, including amongst others:
  - QPG6095 User Manual, describing the various peripherals and interfaces.
  - API Manuals for the various Qorvo-provided software layers.
  - Programming Guides for selected functions and features.
  - Sample applications.

Development System:

A development system for the development of QPG6095 software is available from Qorvo upon request.

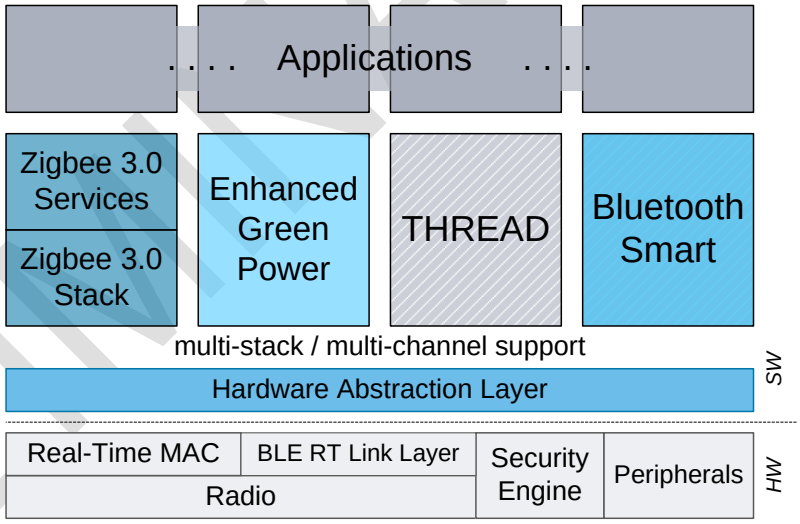
8.1 Multi-Protocol Support

The QPG6095 can run the full stack and applications for

- Zigbee 3.0,
  - including Green Power,
- Thread and
- Bluetooth Smart devices.

Integrated multi-stack, multi-protocol support enables stacks to operate concurrently, and on different channels.

The Hardware Abstraction Layer (HAL) provides an easy-to-use interface abstracting all features of the chip.



9 Flash Programming and Configuration

The Flash program and configuration memory is not programmed when the chips are shipped by Qorvo. To enable the functionality, the Flash must be programmed through a dedicated programming protocol. Please contact Qorvo Support for details of available programming solutions.

9.1 SPI Programming Interface

The primary programming interface for (production) programming of the Flash memory is the SPI Slave interface (section 5.9.4). For this the signals shown in Table 29 shall be made available for the Program Port.

Table 29: Mapping Signals to Program Port (SPI)

QPG6095	Program Port	Notes
EP	GND	Ground
VDD	VCC_DUT	The recommended supply voltage is: **3.3 V**
RESETN	RESETn	The reset signal
GPIO6	PROG_SSn	Slave select signal
GPIO7	PROG_SCLK	Clock provided by the Programmer
GPIO8	PROG_MOSI	Data from Programmer to device
GPIO9	PROG_MISO	Data from device to Programmer
ANIO5_GPIO26	PROG_ENn	Low (stable) enables programming mode at startup/reset. Should be kept low at least until the first SPI access in programming mode. The time between Power On / Reset and the first SPI access must be at least 10 ms. If no command has been received within 4 s, the chip will enter normal application mode.

Following characteristics apply to the SPI programming interface:

- maximum SCLK frequency: **2 MHz**
- minimum SSn high time: **2 µs**
- minimum last SCLK to SSn high time: **2 µs**

9.2 UART Programming Interface

The Flash memory can also be programmed via the UART interface (section 5.9.2). This is a lower performance interface meant for use during development; not for production.
For this the signals shown in Table 30 shall be made available for the Program Port.

Table 30: Mapping Signals to Program Port (UART)

QPG6095	Program Port	Notes
EP	GND	Ground
VDD	VCC_DUT	The recommended supply voltage is: **3.3 V**
RESETN	RESETn	The reset signal
GPIO10	UART_TX	Data from device to Programmer
GPIO11	UART_RX	Data from Programmer to device
ANIO5_GPIO26	PROG_ENn	Low (stable) enables programming mode at startup/reset. Should be kept low at least until the first UART access in programming mode. The time between Power On / Reset and the first UART access must be at least 10 ms. If no command has been received within 4 s, the chip will enter normal application mode.

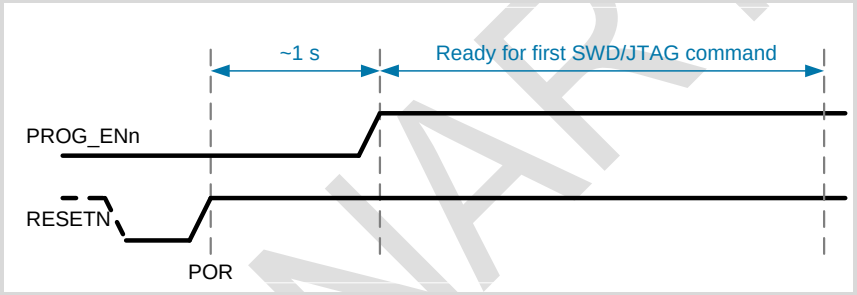
Following characteristics apply to the UART programming interface:

- Default baud rate: **57600** Bd (the baud rate can be changed via the programming protocol after initial setup)
- 1 start bit, 8 data bits, 1 stop bit, no parity

10 Debug Mode

During startup/reset the QPG6095 can be triggered to come up in debug mode. The SWD/JTAG signals shown in Table 31 will then be available.

Table 31: Debug Mode Signals

QPG6095	SWD/JTAC	Notes
GPIO6	SWIO/TMS_b	
GPIO7	SWCLK/TCK_b	
GPIO8	TDI_b	
GPIO9	SWV/TDO_b	
ANIO5_GPIO26	PROG_ENn	Low for about 1 s after Power On / Reset, then high, enables debug mode.  **Figure 16: Entering Debug Mode** While PROG_ENn is asserted low, no transaction should be started on SPI or UART (otherwise programming mode will be entered; see chapter 9). The QPG6095 will be ready for the first SWD/JTAG command for a period of 32 s. If then no command has been received, the chip will enter normal application mode.

11 Device Information

11.1 QFN40 Package

11.1.1 QFN40 Pin Assignments

Figure 17 below shows the pin connections top view, and Table 32 lists the pin assignments. Table 33 provides GPIO assignment options for various functions. For the software configuration options of the GPIO pins, please refer to section 5.9.1. Unless specified otherwise, at power-up/reset all GPIO pins are default set in floating mode.

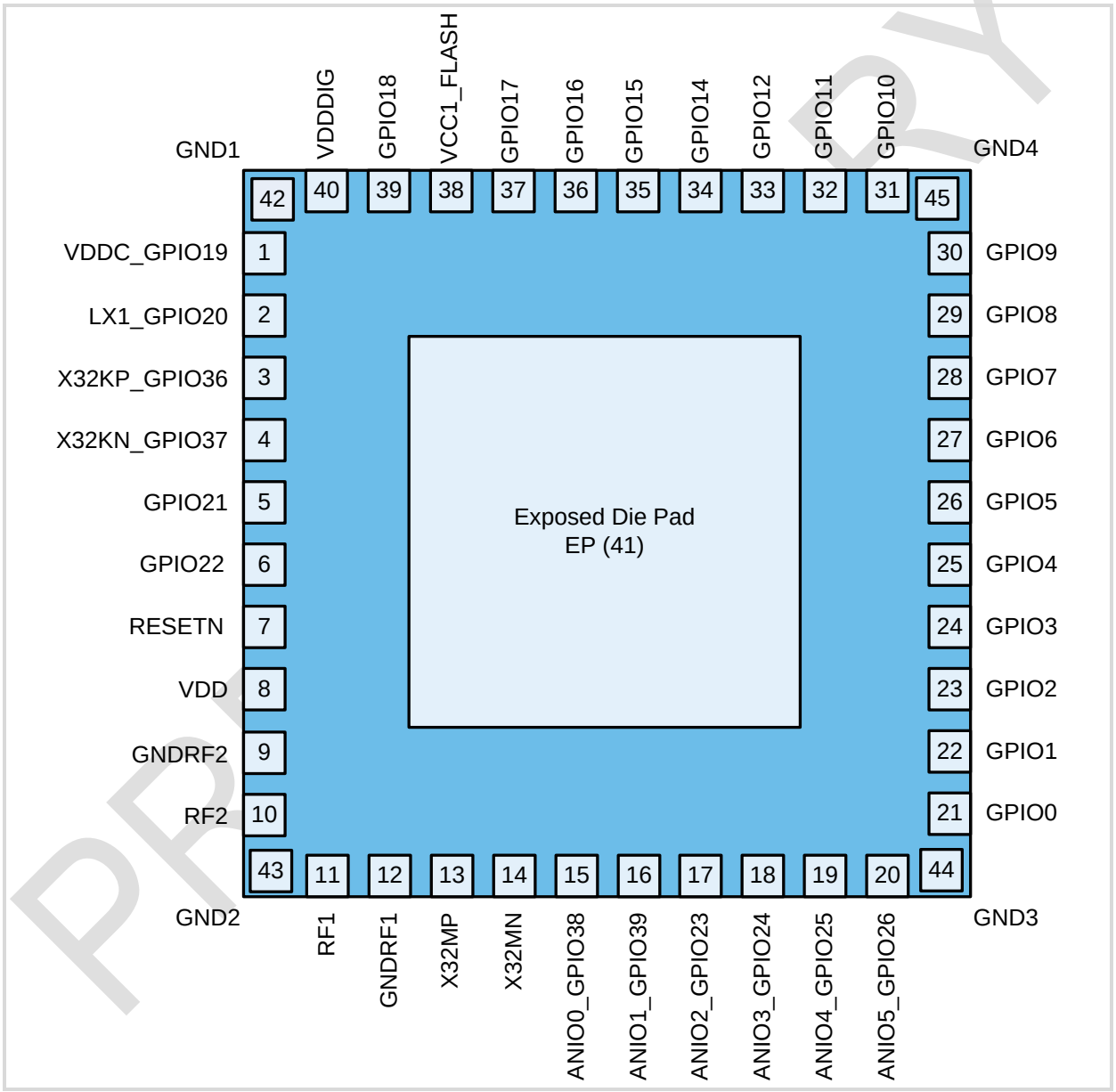


Figure 17: Pin Connections (QFN40) – Top View

Table 32: Pin Assignments (QFN40)

Pin #	Name	Type	Description	Notes
1	VDDC_GPIO19	Power or Digital	Optional DC-DC converter output, or Configurable GPIO	For DC-DC Converter configuration see sections 5.11.1 and 6.14.
2	LX1_GPIO20	Power or Digital	Optional DC-DC converter output, or Configurable GPIO	
3	X32KP_GPIO36	Analog or Digital	Optional 32 KiHz reference crystal input, or Configurable GPIO (input only)	Both pins should either be used for the 32 KiHz reference crystal or defined as GPIO. If a pin is not used, it must be connected to the exposed die pad (GND) and/or software should disable the input buffer, to prevent leakage current. If defined as GPIO, apply external pull up or pull down to avoid floating input.
4	X32KN_GPIO37	Analog or Digital	Optional 32 KiHz reference crystal output, or Configurable GPIO (input only)	
5	GPIO21	Digital	Configurable GPIO	See erratum (section 12.2).
6	GPIO22	Digital	Configurable GPIO	
7	RESETN	Digital	Active-low reset circuit	Internally pulled up, so no external pull up is required. This pin shall be available for optional Flash programming, see chapter 9.
8	VDD	Power	Power supply input	
9	GNDRF2	RF	RF ground return path RF2	Must be connected to the exposed die pad (GND).
10	RF2	RF	RF port for antenna 2	In all cases the RF pins should be isolated from ground or VDD. A DC path between RF1 and RF2 is only permitted when used in differential mode.
11	RF1	RF	RF port for antenna 1	
12	GNDRF1	RF	RF ground return path RF1	Must be connected to the exposed die pad (GND).
13	X32MP	Analog	32 MHz reference crystal input	The QPG6095 does not support an external clock.
14	X32MN	Analog	32 MHz reference crystal output	
15	ANIO0_GPIO38	Analog or Digital	Preferred ADC input, or Configurable GPIO (input only).	ANIO pins that are not used, are recommended to be connected to the exposed die pad (GND).
16	ANIO1_GPIO39	Analog or Digital	Preferred ADC input, or Configurable GPIO (input only)	
17	ANIO2_GPIO23	Analog or Digital	Optional ADC input, or Configurable GPIO	
18	ANIO3_GPIO24	Analog or Digital	Optional ADC input, or Configurable GPIO	
19	ANIO4_GPIO25	Analog or Digital	Optional ADC input, or Configurable GPIO	
20	ANIO5_GPIO26	Analog or Digital	Optional ADC input, or Configurable GPIO	This pin shall be available for optional Flash programming, see chapter 9. At start-up/reset, the QPG6095 bootloader enables a temporary weak internal pull-up to prevent the QPG6095 entering programming mode in normal operation.
21	GPIO0	Digital	Configurable GPIO	
22	GPIO1	Digital	Configurable GPIO	
23	GPIO2	Digital	Configurable GPIO	
24	GPIO3	Digital	Configurable GPIO	

Pin #	Name	Type	Description	Notes
25	GPIO4	Digital	Configurable GPIO	
26	GPIO5	Digital	Configurable GPIO	
27	GPIO6	Digital	Configurable GPIO	These pins shall be available for optional Flash programming via SPI, see chapter 9.
28	GPIO7	Digital	Configurable GPIO	
29	GPIO8	Digital	Configurable GPIO	
30	GPIO9	Digital	Configurable GPIO	
31	GPIO10	Digital	Configurable GPIO	These pins shall be available for optional Flash programming via UART, see chapter 9.
32	GPIO11	Digital	Configurable GPIO	
33	GPIO12	Digital	Configurable GPIO	
34	GPIO14	Digital	Configurable GPIO	
35	GPIO15	Digital	Configurable GPIO	
36	GPIO16	Digital	Configurable GPIO	
37	GPIO17	Digital	Configurable GPIO	
38	VCC1_FLASH	Power	Decoupling of Flash memory	Decoupling to ground. This pin requires a 10 nF decoupling capacitor to ground.
39	GPIO18	Digital	Configurable GPIO	Up to 600 mA output drive strength, suitable for e.g. driving an IR LED circuit.
40	VDDDIG	Power	Power supply output for decoupling	Decoupling to ground. This pin requires a 22 nF decoupling capacitor to ground.
Die pad (41)	EP	Ground	Exposed die pad; analog chip ground	RF ground (GND)
(42)	GND1	Ground	\ Additional ground connections, internally connected to the die pad via the lead frame. /	Available for easier ground routing, e.g. on single layer designs.
(43)	GND2	Ground		
(44)	GND3	Ground		
(45)	GND4	Ground		

For the software configuration options of the GPIO pins, please refer to section 5.9.1. Unless specified otherwise, at power-up/reset all GPIO pins are default set in floating mode.

Table 33: GPIO Assignment Options (QFN40)

Pin #	Pin Name	Wake Up	Drive Strength group	Keyboard Scan (column = input, row = output)	SPI Master	SPI Slave	I²C Master	I²C Slave	I²S Master	UART Debug	UART Func 1	UART Func 2	IR	PWM	Time-stamp	PDM (Voice)	LED	SWD / JTAG	Clock Output	RF Front End
21	GPIO0	WKUP	0..3	Kbd Column 0_a	MISO_a [1]	SSn_a	SDA_a [2]	SDA_a [2]	SDI_a		TX_a	TX_a		PWM0_a	Tstmp0_a		LED0_a			MODE3_c
22	GPIO1	WKUP		Kbd Column 1_a	SSn_a	MISO_a	SCL_a [2]	SCL_a [2]	WS_a	TX_a	RX_a	RX_a		PWM1_a	Tstmp1_a		LED1_a			MODE2_c
23	GPIO2	WKUP		Kbd Column 2_ab	SCLK_a	MOSI_a	SDA_b [2]	SDA_b [2]	SCK_a	RX_a		TX_b	OUT_a	PWM2_a	Tstmp2_a	DATA_a	LED2_a			MODE1_c
24	GPIO3	WKUP		Kbd Column 3_ab	MOSI_a	SCLK_a	SCL_b [2]	SCL_b [2]	SDO_a			RX_b		PWM3_a	Tstmp3_a	CLK_a	LED3_a			ANTSW_c
25	GPIO4	WKUP	4..7	Kbd Column 4_a	MISO_f [1]	SSn_f			SDI_f					PWM0_b	Tstmp0_b		LED0_b			ANTSWn_c
26	GPIO5	WKUP		Kbd Column 5_a	SSn_f	MISO_f			WS_f	TX_f				PWM1_b	Tstmp1_b		LED1_b			MODE0_c
27	GPIO6	WKUP		Kbd Column 6_a	MOSI_f	SSn_b			SDO_f					PWM4_a				SWIO / TMS_b		
28	GPIO7	WKUP		Kbd Column 7_a		SCLK_b	SCL_c [2]	SCL_c [2]						PWM5_a			LED1_g	SWCLK / TCK_b		
29	GPIO8	WKUP	8..11	Kbd Row 0_a		MOSI_b	SDA_c [2]	SDA_c [2]		RX_b	TX_b			PWM4_b			LED2_b	TDI_b		
30	GPIO9	WKUP		Kbd Row 1_a		MISO_b				TX_b	RX_b			PWM5_b			LED3_b	SWV / TDO_b		
31	GPIO10	WKUP		Kbd Row 2_ab		SSn_c					TX_c		OUT_b	PWM0_c	Tstmp0_c	DATA_b	LED0_c		CLK_OUT	ANTSWn_a
32	GPIO11	WKUP		Kbd Row 3_ab		SCLK_c					RX_c	RX_c		PWM1_c	Tstmp1_c	CLK_b	LED1_c			MODE3_a
33	GPIO12		12..15	Kbd Row 4_a		MOSI_c				RX_c		TX_c		PWM2_c	Tstmp2_c		LED2_c			
34	GPIO14			Kbd Row 6_ab	SCLK_b	MOSI_d			SCK_b	RX_d	TX_d	TX_d		PWM0_d	Tstmp0_d		LED0_d			MODE2_a
35	GPIO15			Kbd Row 7_ab	MOSI_b	MISO_d			SDO_b	TX_d	RX_d			PWM1_d	Tstmp1_d		LED1_d			MODE1_a

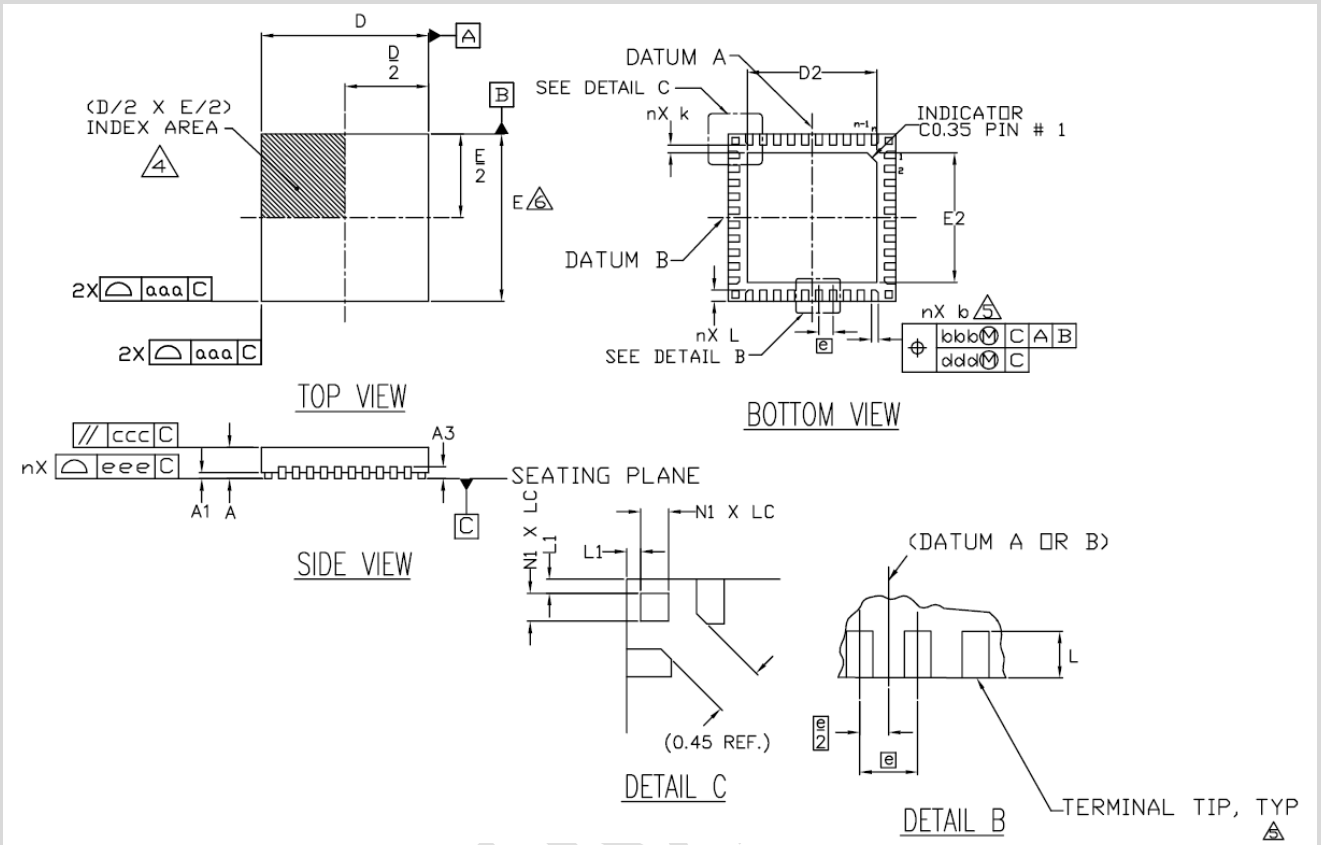
[1] SPI MISO signal may require external pull down to prevent floating input signal, depending on the behavior of the slave device (e.g. during sleep state, or when not selected).
[2] I²C bus signals (SCL, SDA) require external pull up.

Pin #	Pin Name	Wake Up	Drive Strength group	Keyboard Scan (column = input, row = output)	SPI Master	SPI Slave	I²C Master	I²C Slave	I²S Master	UART Debug	UART Func 1	UART Func 2	IR	PWM	Time-stamp	PDM (Voice)	LED	SWD / JTAG	Clock Output	RF Front End
36	GPIO16		16..19	Kbd Row 4_b	MISO_b [1]	SSn_d			SDI_b					PWM2_d	Tstmp2_d	DATA_c	LED2_d			MODE0_a
37	GPIO17			Kbd Row 5_b	SSn_b	SCLK_d			WS_b				OUT_c	PWM3_d	Tstmp3_d	CLK_c	LED3_d			ANTSW_a
39	GPIO18				SCLK_f				SCK_f				OUT_e [3]	PWM4_c	Tstmp3_f		LED0_g			ANTSW_d
1	GPIO19	WKUP		Kbd Row 0_b	SCLK_e		SCL_d [2]	SCL_d [2]	SCK_e					PWM5_c	Tstmp0_e	DATA_d	LED2_e			ANTSWn_d
2	GPIO20	WKUP	20..23	Kbd Row 1_b	MOSI_e		SDA_d [2]	SDA_d [2]	SDO_e		TX_g			PWM0_e	Tstmp1_e	CLK_d	LED3_e			
5	GPIO21	WKUP			MISO_e [1]		SCL_f [2]	SCL_f [2]	SDI_e		TX_e		OUT_f	PWM4_e	Tstmp0_g		LED0_e			
6	GPIO22	WKUP			SSn_e		SDA_f [2]	SDA_f [2]	WS_e		RX_e			PWM5_e	Tstmp1_g		LED1_e			
17	GPIO23	WKUP			MISO_d [1]	MOSI_e	SDA_e [2]	SDA_e [2]	SDI_d	RX_e		TX_f		PWM2_f	Tstmp2_g	CLK_f	LED0_f			MODE2_b
18	GPIO24	WKUP			SSn_d	SCLK_e	SCL_e [2]	SCL_e [2]	WS_d			RX_f		PWM3_f	Tstmp3_g	DATA_f	LED1_f			MODE1_b
19	GPIO25	WKUP	24..27	Kbd Column 4_b	SCLK_c	SSn_e	SDA_g [2]	SDA_g [2]	SCK_c		RX_f	TX_e		PWM4_f	Tstmp2_f	CLK_e	LED2_f			MODE0_b
20	GPIO26	WKUP		Kbd Column 5_b	MOSI_c	MISO_e	SCL_g [2]	SCL_g [2]	SDO_c	TX_e	TX_f		OUT_g	PWM5_f			LED3_f			ANTSW_b
3	GPIO36	WKUP	36..39 (input only)								RX_g				Tstmp2_e	DATA_g				
4	GPIO37	WKUP													Tstmp3_e					
15	GPIO38	WKUP		Kbd Column 6_b		MOSI_f				RX_f					Tstmp0_f					
16	GPIO39	WKUP		Kbd Column 7_b	MISO_c [1]	SCLK_f			SDI_c			RX_e			Tstmp1_f	DATA_e				

Note: Although the signals are grouped in sets (_a, _b, etc.), they can be mapped individually.

[3] OUT_e is generally preferred for IR due to the increased drive strength possibility of GPIO18 (see section 5.9.1).

11.1.2 QFN40 Package Drawings



REF	Min.	Nom.	Max.	Unit
A	0.80	0.90	1.00	mm
A1	0.00	0.02	0.05	mm
A3		0.20 REF.		mm
b	0.18	0.25	0.30	mm
D, E	5.925	6.00	6.075	mm
D2, E2	4.55	4.65	4.75	mm
e		0.50 BSC.		mm
k	0.20			mm
L	0.35	0.40	0.45	mm
L1	0.075	0.125	0.175	mm
LC	0.20	0.25	0.30	mm
n		40		
N1		4		

Tolerances of form and position	
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08
fff	0.10

Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. n is the total number of pins.
3. nD is the number of pins on each side.
4. The pin #1 identifier and pin numbering conform to JEDEC publication 95 SPP-002.
5. Dimension b applies to the metallized pin and is measured between 0.25 mm and 0.30 mm from pin tip.

Figure 18: QFN40 Package Drawings and Dimensions

11.1.3 QFN40 Package Information

Figure 19: Information on the QFN40 Package

11.1.4 QFN40 Thermal Resistance

Table 34: QFN40 Thermal Resistance

Symbol	Parameter	Conditions	QFN40 value	Unit
Theta JA ($R_{\theta JA}$)	Thermal resistance from junction to ambient	JEDEC 2S2P (4L) board as per JESD 51-7	33.3	K/W
Theta JC ($R_{\theta JC}$)	Thermal resistance from junction to case, at the exposed die pad	JEDEC 1S0P (2L) board as per JESD 51-3	16.7	K/W

11.2 Moisture/Reflow Sensitivity

Table 35: Moisture/Reflow Sensitivity

Symbol	Parameter	Conditions	Value	Unit
	Soldering Process		Pb-free	
T_c	Peak reflow temperature		260	°C
MSL	Moisture Sensitivity Level		3	
	The Moisture/Reflow Sensitivity is classified according to: IPC/JEDEC J-STD-020D.1 (March 2008) Joint Industry Standard; Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.			

11.3 RoHS Compliance

Table 36: RoHS Compliance

Symbol	Attribute	Compliant
RoHS	Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment; Directives 2011/65/EU and 2015/863/EU.	✓
Pb	Lead Free	✓
	Halogen Free (Chlorine, Bromine)	✓
	Antimony Free	✓
	TBBP-A ($C_{15}H_{12}Br_4O_2$) Free	✓
	PFOS Free	✓
	SVHC Free	✓

12 Errata

12.1 Internal Microcontroller

The Arm Cortex-M4 processor can experience a spurious 'busfault' exception, when an interrupt is triggered while a memory access is pending due to memory bus contention. The probability of this is very low, but increases with the interrupt rate. These specific circumstances allow a robust solution that will not impact performance or debugging options. All following steps must be used (these are part of the default Qorvo deliverables and reference layers):

- The exception handler MUST ignore busfaults that are IMPRECISE only, and there is a pending interrupt. The Qorvo software releases contain a small wrapper function around the busfault_handler to do this.
- The busfault exception MUST be enabled at the highest priority ('0').
- Interrupts and e.g. SysTick exception MUST run at a lower priority, if enabled. By default, the Qorvo releases set all interrupts to priority '2'.
- The system stack MUST be in MCU RAM if the Arm processor frequency is 32 MHz or higher.

12.2 GPIO Pin 5

Pin 5 (GPIO21) has some susceptibility to latch-up at ambient temperatures > 55 °C. Non-destructive latch-up can be triggered on this pin with a transient condition in which voltage on pin 5 is higher than VDD + 1 V and current running into the pin is > 70 mA (both typical conditions).

During this latch-up state:

- No decrease in function or performance has been observed
- The device consumes an additional current of 25 … 30 mA (typical)

The chip will exit the latch-up state under following conditions:

- Power-On-Reset condition
- Going to RC or 32KiHz Standby Mode
- Ambient temperature drops below 55 °C (typical)

Recommendation for the application:

- For remote control applications (normally asleep, limited temperature range): no special recommendation.
- For always on, high-temperature applications: it is recommended to keep pin 5 (GPIO21) connected to GND if the absolute maximum rating of VDD + 0.3 V cannot be guaranteed at all times.

12.3 GPIO State in VDD Cut-off Standby State

When VDD drops below the Cut-Off threshold, the chip enters a forced standby state and all GPIOs switch to input. However, GPIO20, GPIO21 and GPIO22 are not guaranteed to switch to input if they were configured as output at the time the cut-off condition was triggered.

Recommendation for the application:

- If any of these 3 GPIOs are used as output, the VDD Brown-out detect (BOD) handler (or other similar mechanism) **should** switch them to input to ensure they are in input state when the VDD Cut-Off condition occurs, as is implemented in the default BOD handler provided by Qorvo.

12.4 Spurious External Event

A spurious 'external event' interrupt may be triggered in the following case:

- A timer event is triggered that wakes up the device from RC Standby Mode or 32KiHz Standby Mode, AND
- a GPIO with wake-up capability (WKUP) has been configured to trigger on 'falling edge' (using internal or external pull-up)

This issue will never lead to spurious wake-ups, i.e. the issue is triggered as part of the wake-up resulting from the timer event. The spurious external event can be safely ignored in the external event handler in this case; examples: keyboard scan returns no change since previous scan, or external wake-up line is not low on wake-

up. In practice, since the external event has no specific GPIO information, external event handlers incorporate the robustness against this spurious event by default. Processing overhead of the spurious event will be negligible.

Abbreviations

ACL	Asynchronous Connection Logical transport
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AES	Advanced Encryption Standard
AGC	Automatic Gain Control
ANIO	Analog Input/Output
API	Application Program(ming) Interface
ARIB	(Japan) Association of Radio Industries and Businesses
ASME	American Society of Mechanical Engineers
BLE	Bluetooth Low Energy
CCA	Clear Channel Assessment
CCM	Counter with CBC-MAC (ciphering), where CBC-MAC = cipher block chaining message authentication code
CCM*	extension of CCM
CDM	(ESD) Charged Device Model
CSMA/CA	Carrier Sense Multiple Access with Collision Avoidance
DNL	Differential Nonlinearity
ESD	Electrostatic Discharge
ETSI	European Telecommunication Standardization Institute
EVM	Error Vector Magnitude
FCC	(US) Federal Communications Commission
FEM	Front-End module
GATT	Generic Attribute Protocol
GND	Ground
GPIO	General Purpose Input / Output
HAL	Hardware Abstraction Layer
HBM	(ESD) Human Body Model
HCI	Host Controller Interface
HID	Human Interface Device
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
INL	Integral Nonlinearity
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
IIP3	Third Order Input Intercept Point
IO	Input/Output
IR	InfraRed
ISM	Industrial, Scientific, and Medical (license-free frequency band)
LDO	Low Drop-Out voltage regulator
LE	(Bluetooth) Low Energy
LED	Light Emitting Diode
LFSR	linear feedback shift register
LL	(Bluetooth) Link Layer
LNA	Low-noise amplifier
LQI	Link Quality Indication
LSb	Least-Significant bit
MAC	Medium Access Control layer
MCU	MicroController Unit
MEMS	Micro-Electro-Mechanical Systems
MOQ	Minimum Order Quantity
MOSFET	metal–oxide–semiconductor field-effect transistor
MSb	Most-Significant bit
PA	Power Amplifier
PCB	Printed Circuit Board
PDM	Pulse-Density Modulation
PER	Packet Error Rate
PHY	Physical layer
POR	Power On Reset
PSRR	Power Supply Rejection Ratio
PWM	Pulse-Width Modulation
QFN	Quad Flat No leads (package)
RAM	Random-Access Memory
RC	resistor–capacitor (circuit)
RF	Radio Frequency
RF4CE	Radio Frequency for Consumer Electronics
RSSI	Received Signal Strength Indication
RoHS	Restriction of Hazardous Substances (Directive)
ROM	Read-Only Memory
RX	Receive
SPI	Serial Peripheral Interface
TWI	Two-Wire Interface
TX	Transmit
UART	Universal Asynchronous Receiver and Transmitter
VDD	Voltage Drain Drain (i.e. Positive voltage supply)
VMT	Voltage Minimum Threshold

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Document History

Version	Date	Section	Changes
0.14	6 Jul 2017	All	ADVANCE INFO release.
0.15	7 Aug 2017	All	Updated Arm trademarks marking.
		6.2	Corrected VDD condition for VOL and VOH.
		6.9.2	Added another option for the 32 KiHz crystal.
0.16	30 Nov 2017	All	Spelling: Zigbee without capital B.
		6.9.2	Added recommendation for devices subject to mechanical shock.
		11.1.1	Correction: GPIO18 max drive = 600 mA.
0.17	15 Mar 2018		PRELIMINARY release.
		1, 3, 5.3	BLE 5.0
		2	Updated block diagram.
		4	Updated ordering info.
		5.9.1.1, 11.1.1	No pull-up/down on GPIO36 and GPIO37.
		5.9.11, 5.9.14.1, 6.11	Updated clock.
		6	Updated Parameter Evaluation Circuit.
		6.2, 6.8	Updated temperature range.
		6.3	Added numbers for other RAM retention levels.
		6.3, 6.13	Added comparator characteristics.
		6.3, 6.5, 6.14	Updated; removed TBDs.
		11.1.1	Table 33 updated; GPIO36 and GPIO37 can be WKUP.