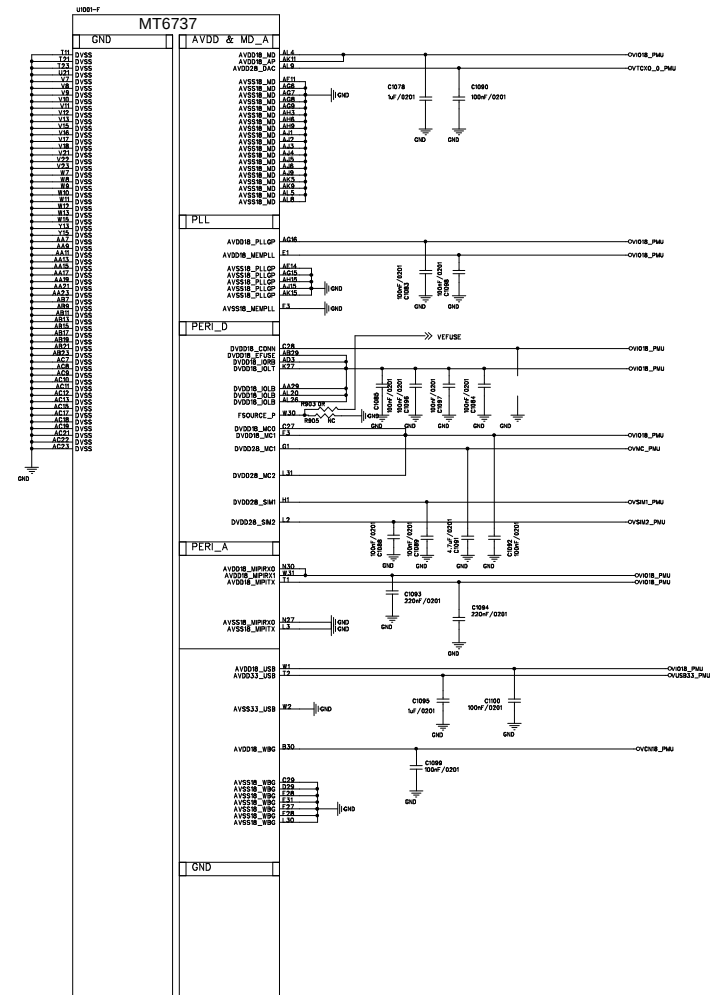
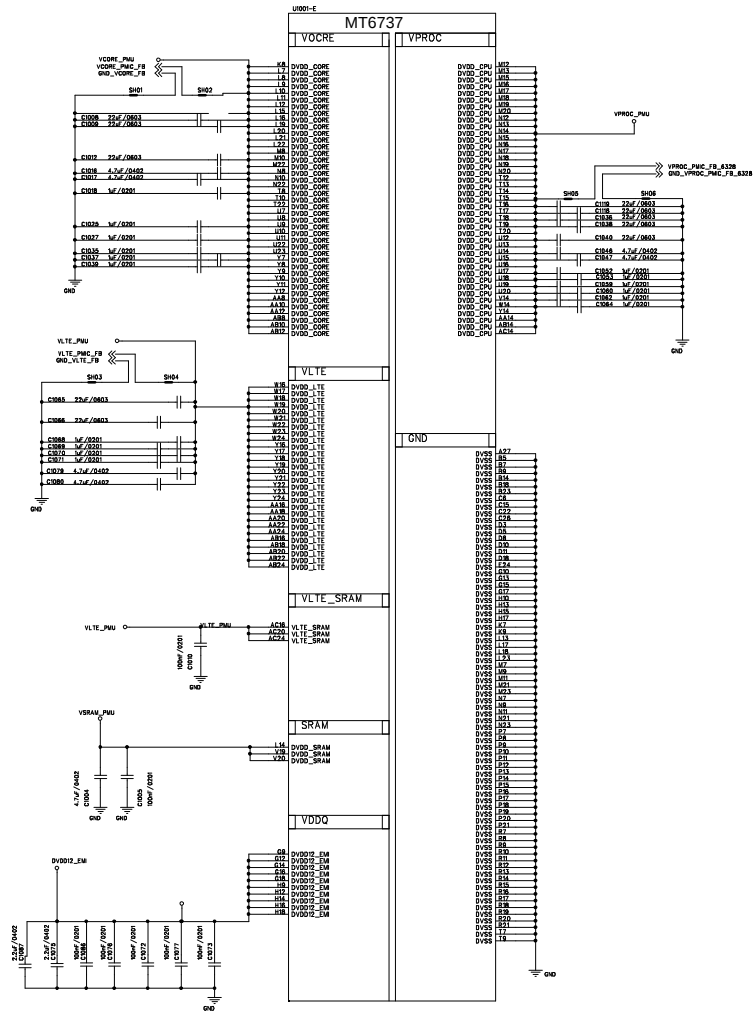
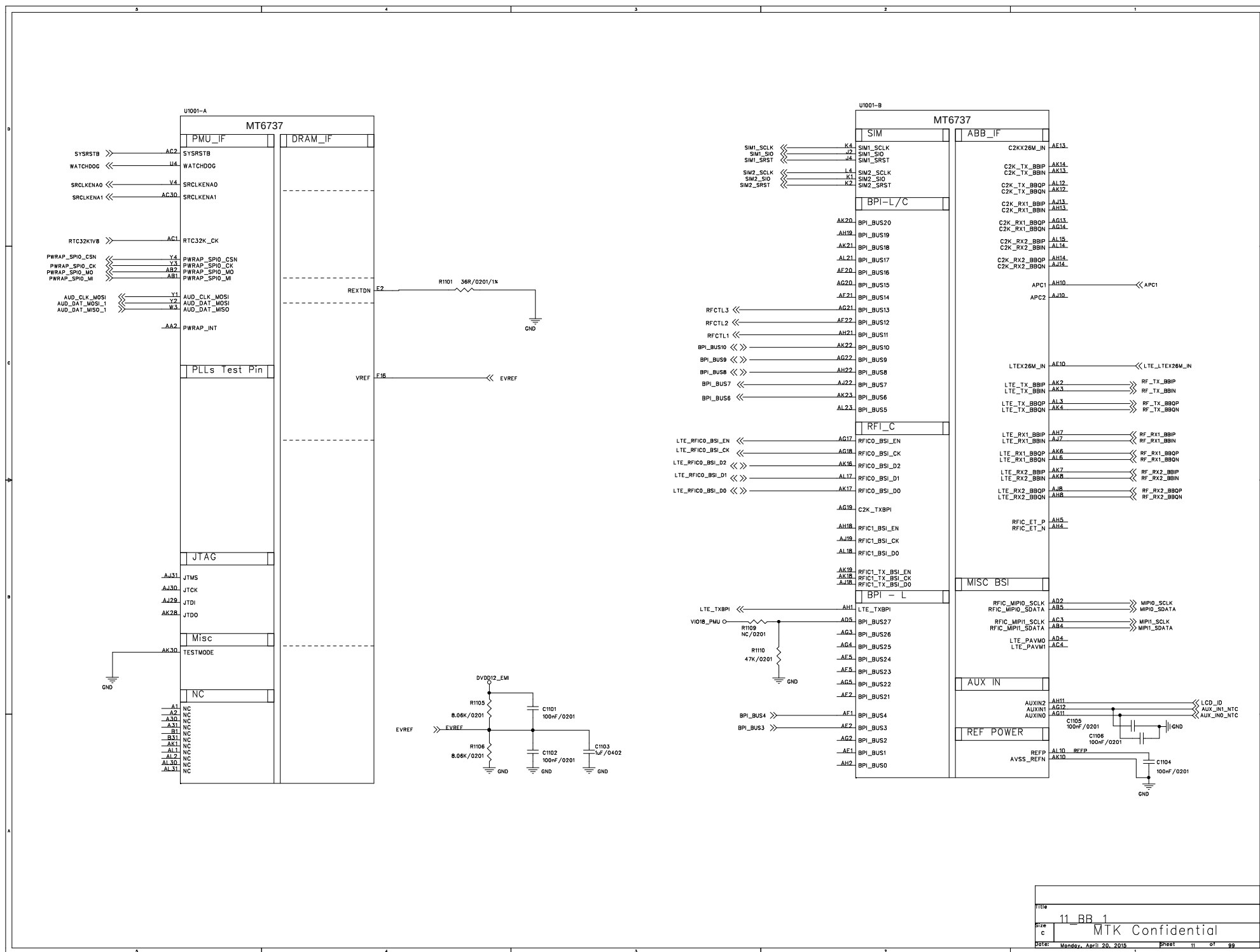
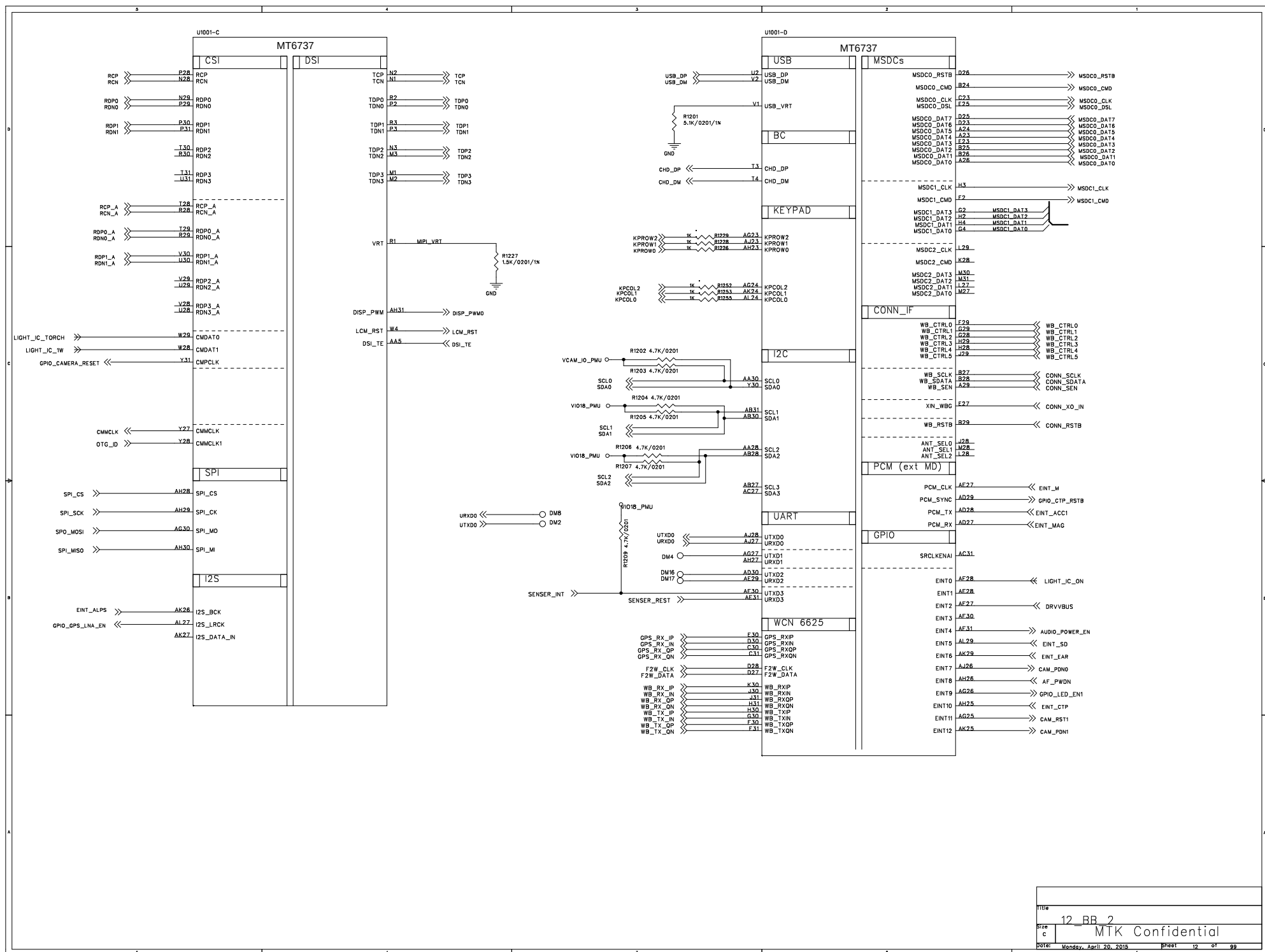
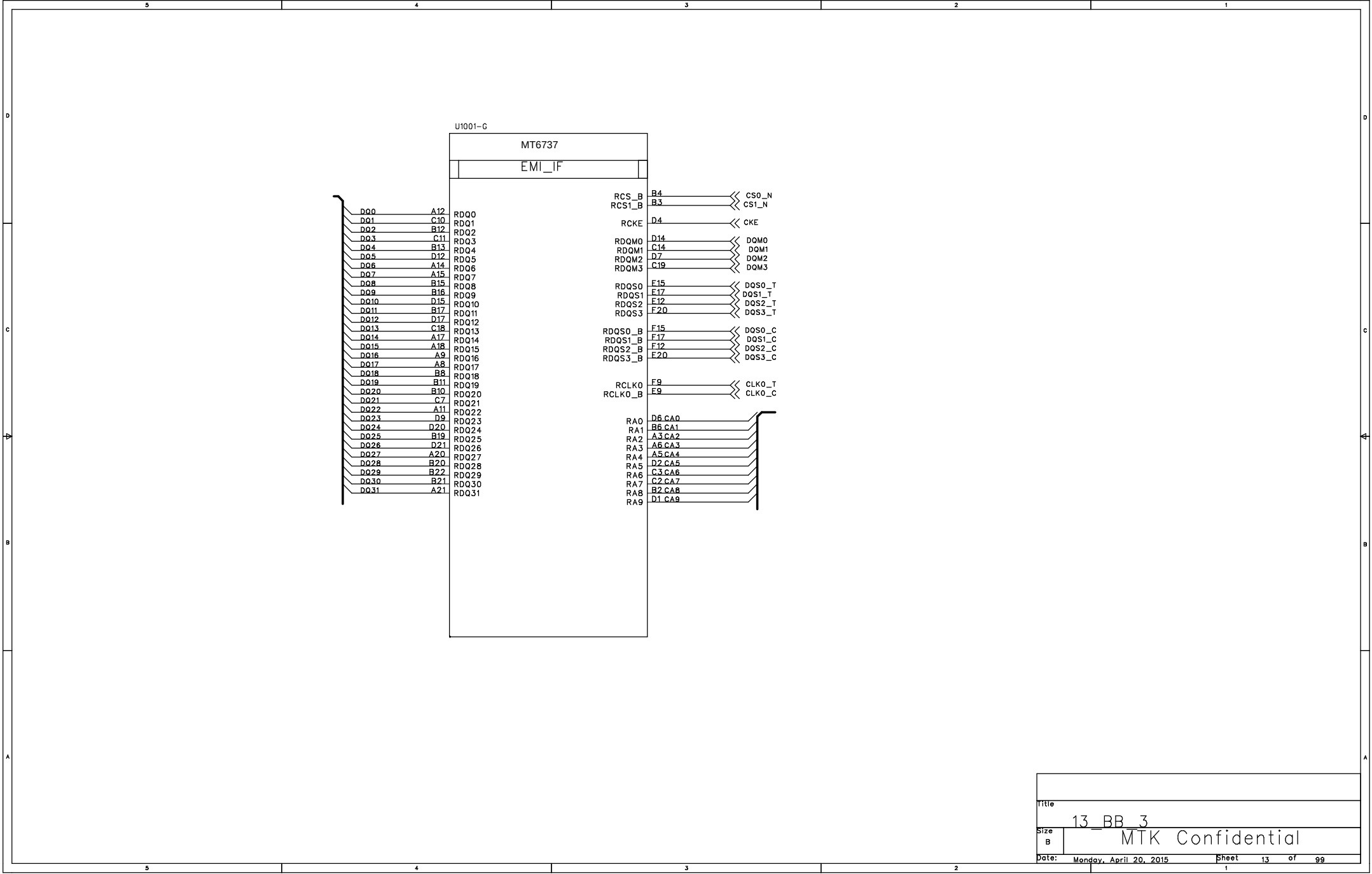




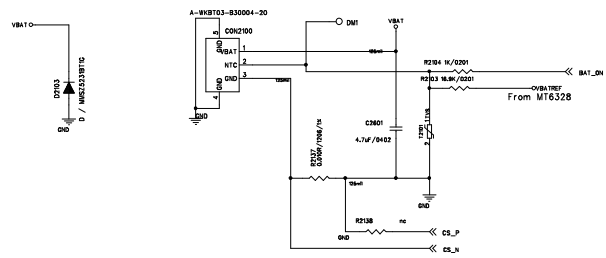


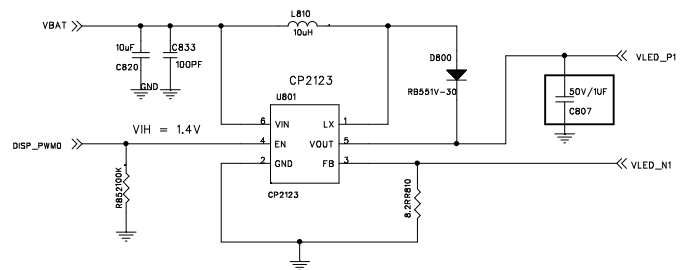


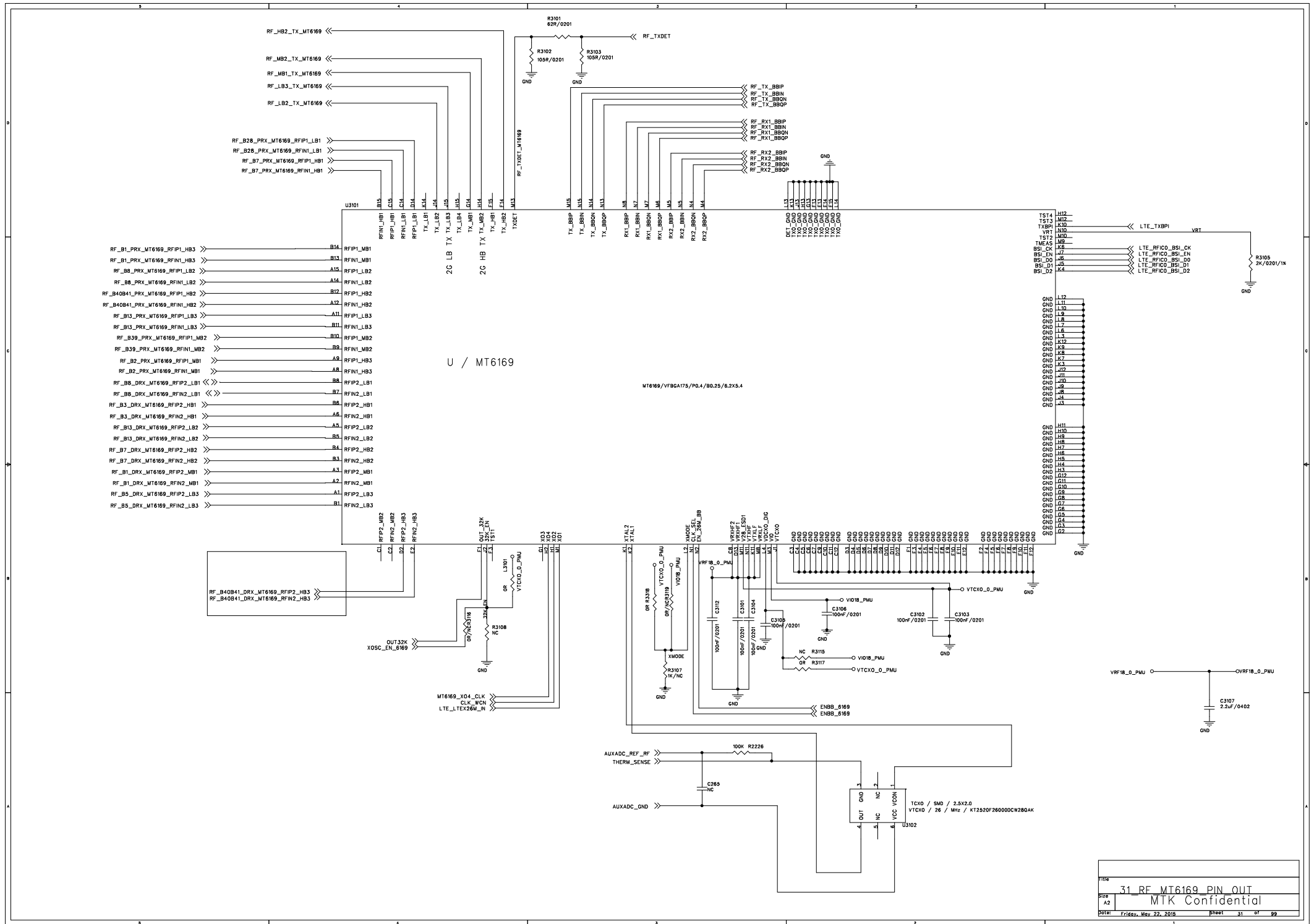


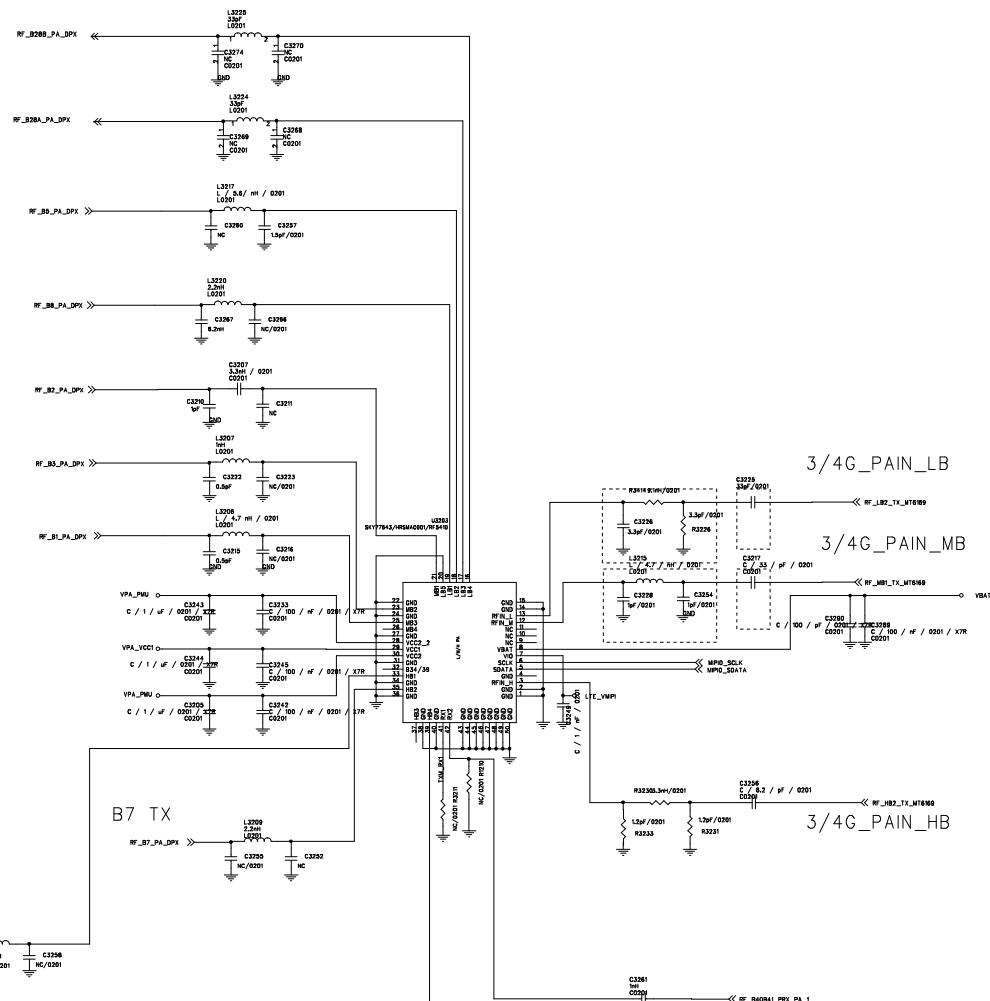
BATTERY CONNECTOR

Pulse Charger



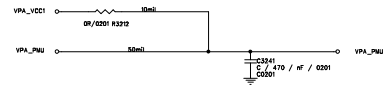




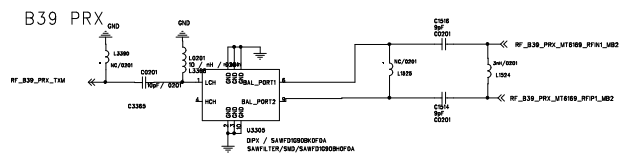
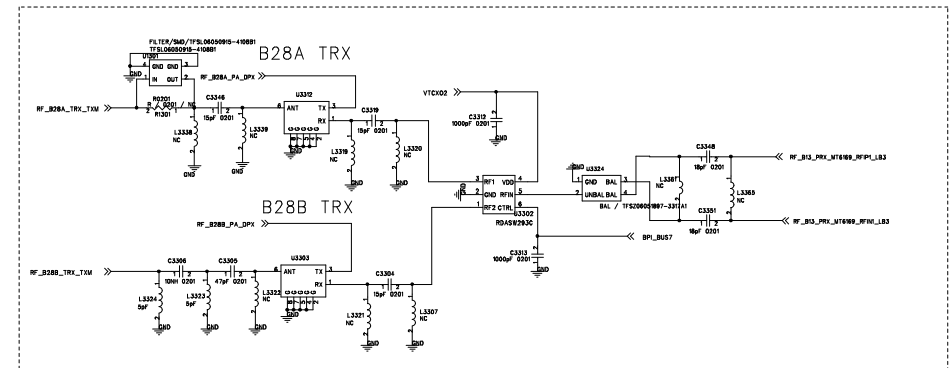
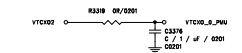


Power Net Connection

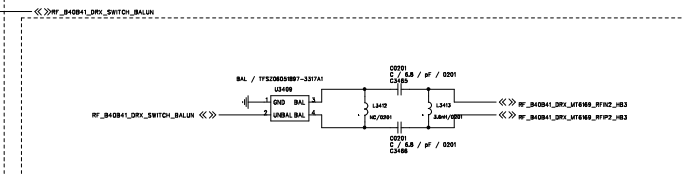
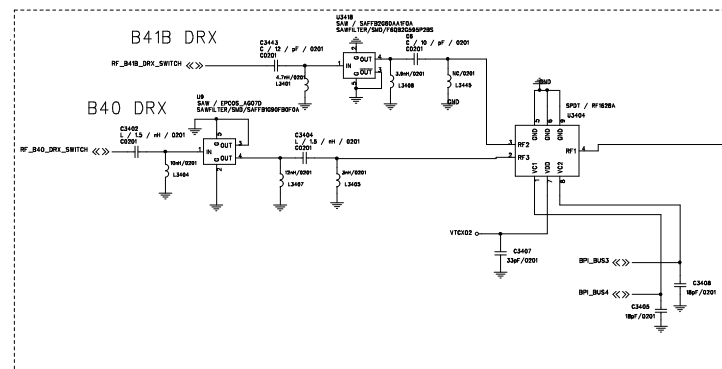
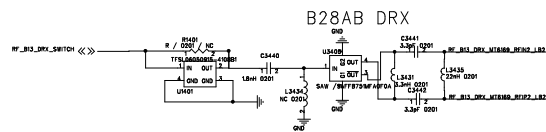
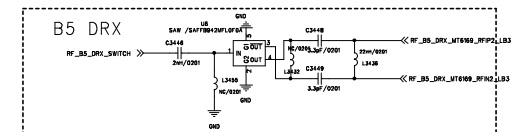
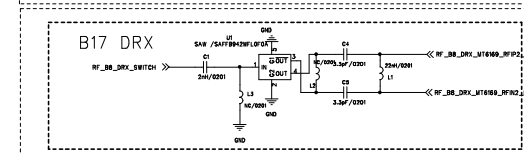
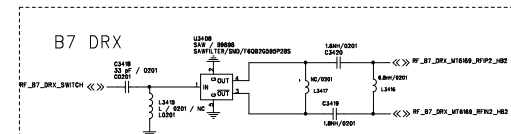
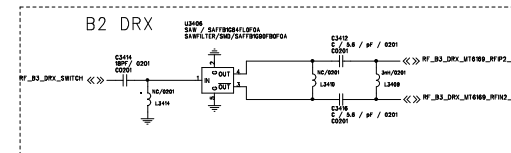
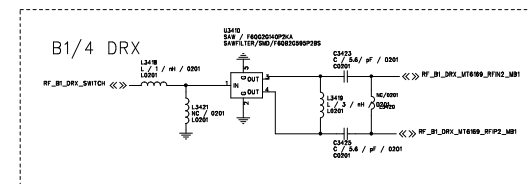
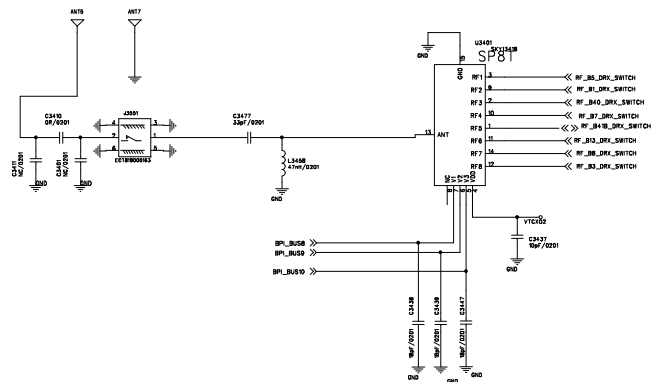
VPA_VCC1 and VPA PMU need to be connected after Cap



VPA_VCC1 and VPA PMU need to be connected after Cap



DRX ANT: 1805-2690MHz

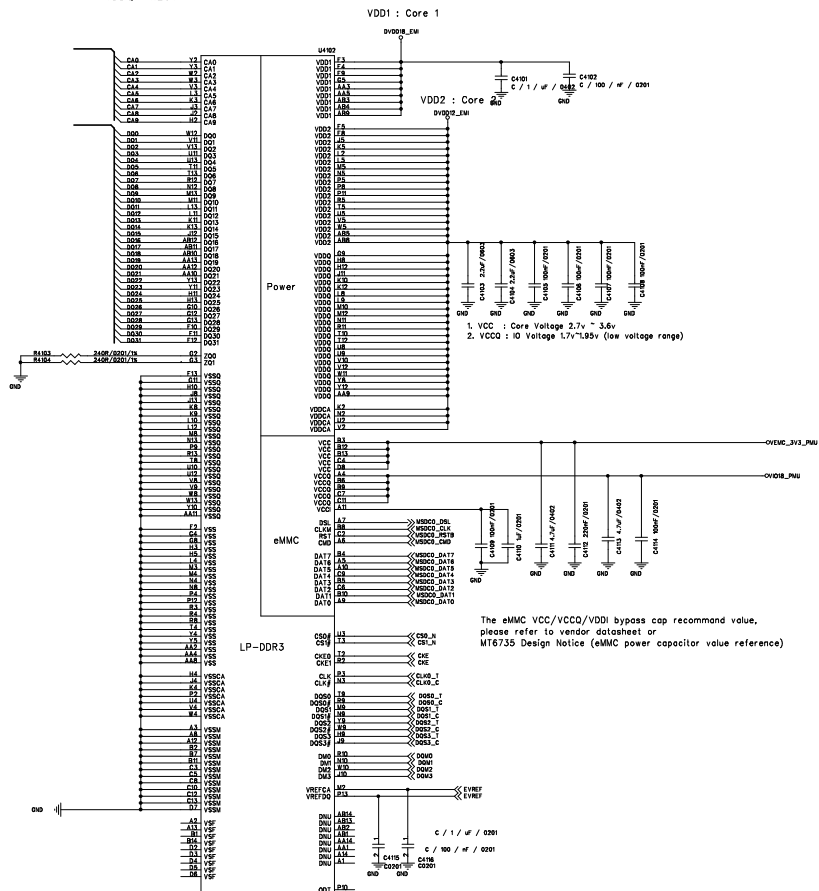


Connect to AP			
DQ[0..31]	DQ[0..31]		
CA[0..9]	CA[0..9]		
CS0_N	CS0_N		
CS1_N	CS1_N		
CKE	CKE		
DM0	DM0		
DM1	DM1		
DM2	DM2		
DM3	DM3		
DQS0_C	DQS0_C		
DQS1_C	DQS1_C		
DQS2_C	DQS2_C		
DQS3_C	DQS3_C		
DQS0_T	DQS0_T		
DQS1_T	DQS1_T		
DQS2_T	DQS2_T		
DQS3_T	DQS3_T		
CLK0_T	CLK0_T		
CLK0_C	CLK0_C		
VREF_CA	VREF_CA		
VREF_DQ	VREF_DQ		
MSDC0_RSTB	MSDC0_RSTB		
MSDC0_CMD	MSDC0_CMD		
MSDC0_CLK	MSDC0_CLK		
MSDC0_DSL	MSDC0_DSL		
MSDC0_DAT0	MSDC0_DAT0		
MSDC0_DAT1	MSDC0_DAT1		
MSDC0_DAT2	MSDC0_DAT2		
MSDC0_DAT3	MSDC0_DAT3		
MSDC0_DAT4	MSDC0_DAT4		
MSDC0_DAT5	MSDC0_DAT5		
MSDC0_DAT6	MSDC0_DAT6		
MSDC0_DAT7	MSDC0_DAT7		
Power I/F			
VIO1B_PMU	VIO1B_PMU		
VEMC_3V3_PMU	VEMC_3V3_PMU		
DVDD12_EMI	DVDD12_EMI		

eMMC+LPDDR3
221 Ball, 0.5mm pitch

VDD1=1.8V
VDD2=1.20V
VDDCA=1.2V
VDDQ= 1.20V

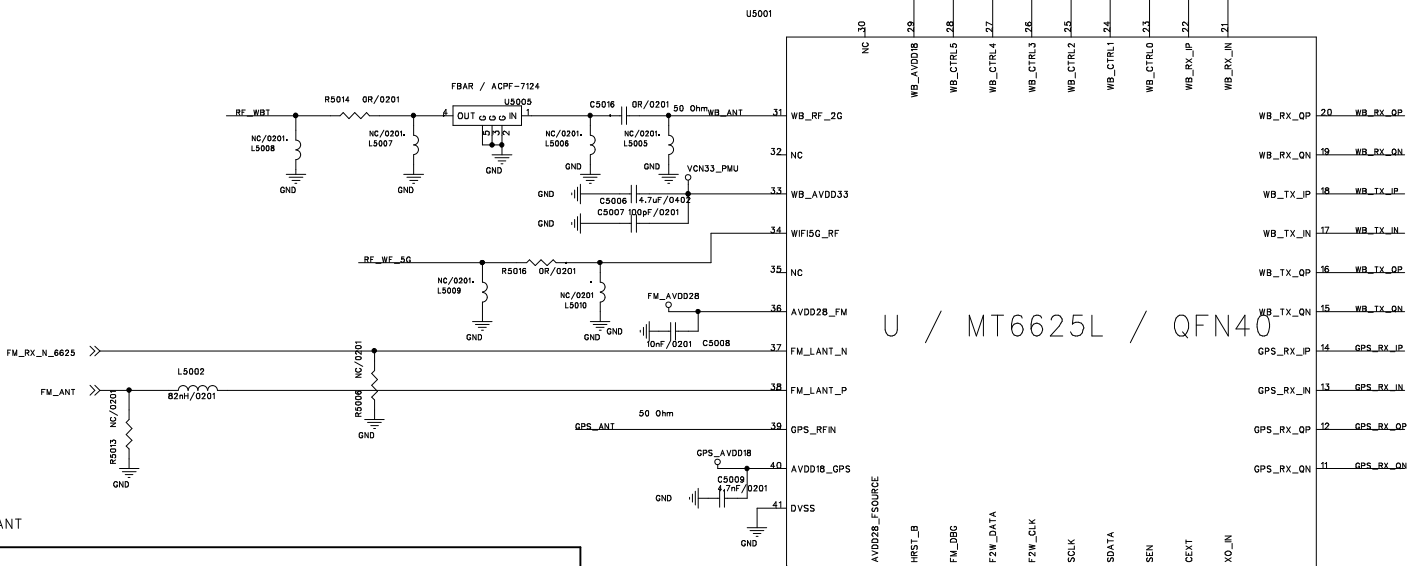
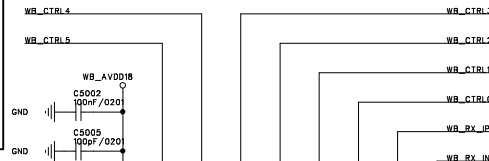
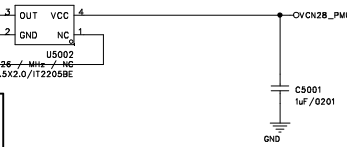
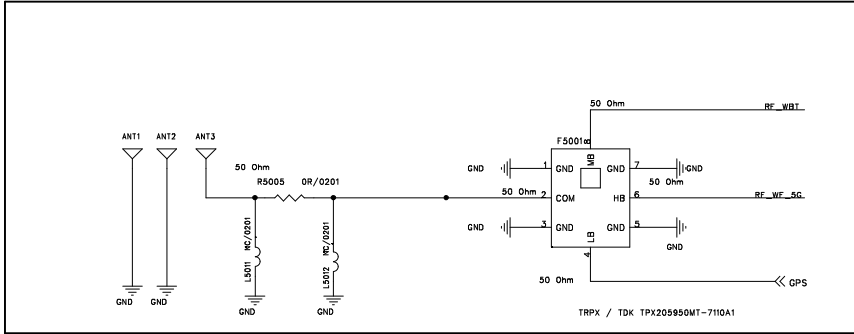
8GB eMMC + 8Gb LPDDR3
Hynix/H9TQ64A8GTMCUR-KUM



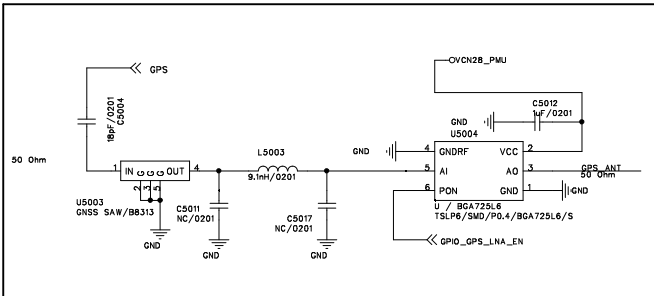
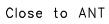
FB0A221/PLA/90.27/1.919/BAUB000 / H9TQ64A8GTMCUR-KUM

Reserve Keep out region from L1 to Main GND layer

Close to Antenna



U / MT6625L / QFN4C^W



WB_CTRL0	<<	WB_CTRL0
WB_CTRL1	<<	WB_CTRL1
WB_CTRL2	<<	WB_CTRL2
WB_CTRL3	<<	WB_CTRL3
WB_CTRL4	<<	WB_CTRL4
WB_CTRL5	<<	WB_CTRL5
CONN_SCLK	<<	CONN_SCLK
CONN_SDATA	<<	CONN_SDATA
CONN_SEN	<<	CONN_SEN
CONN_RSTB	<<	CONN_RSTB

```

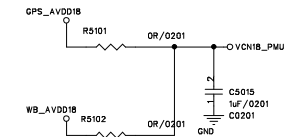
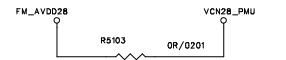
GPS_RX_IP      << GPS_RX_IP
GPS_RX_IN      << GPS_RX_IN
GPS_RX_QP      << GPS_RX_QP
GPS_RX_ON      << GPS_RX_ON

F2W_CLK        << F2W_CLK
F2W_DATA       << F2W_DATA

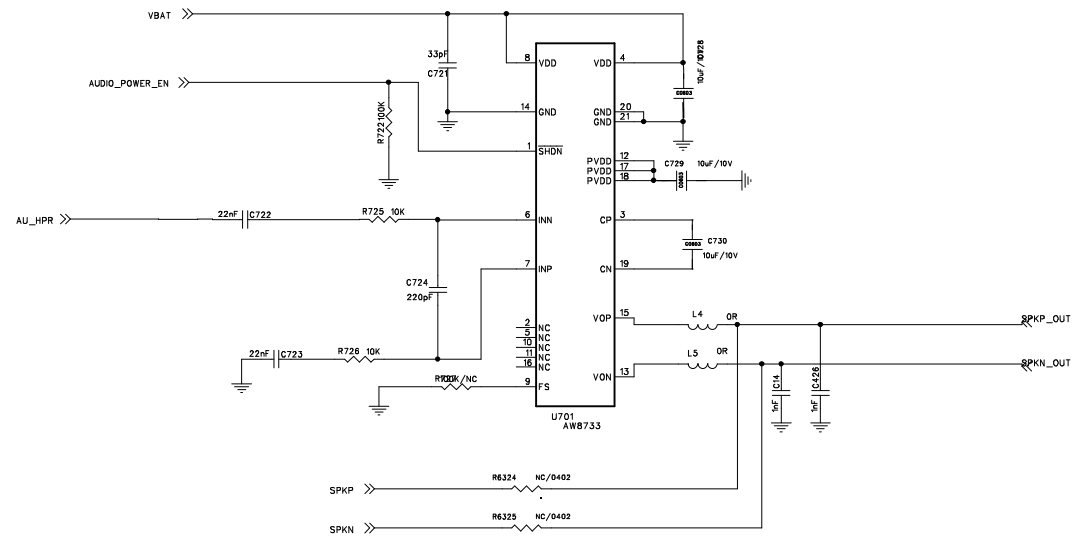
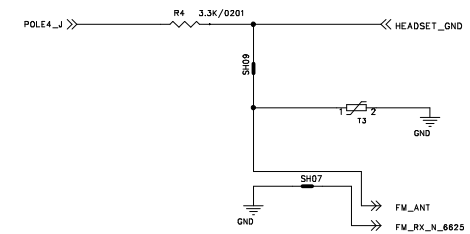
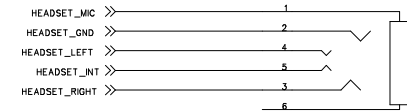
WB_RX_IP       << WB_RX_IP
WB_RX_IN       << WB_RX_IN
WB_RX_QP       << WB_RX_QP
WB_RX_ON       << WB_RX_ON
WB_TX_IP       << WB_TX_IP
WB_TX_IN       << WB_TX_IN
WB_TX_QP       << WB_TX_QP
WB_TX_ON       << WB_TX_ON

CONN_XD_IN     << CONN_XD_IN

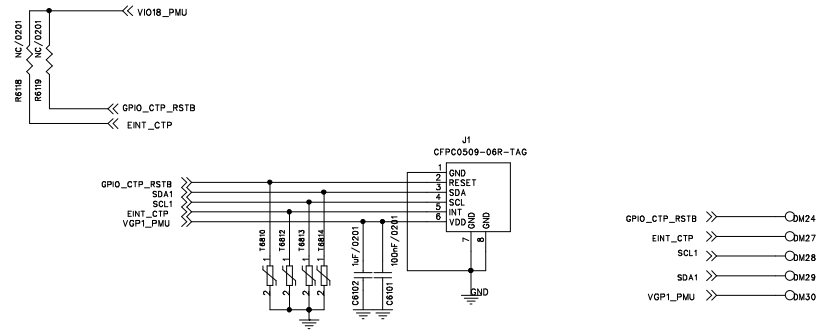
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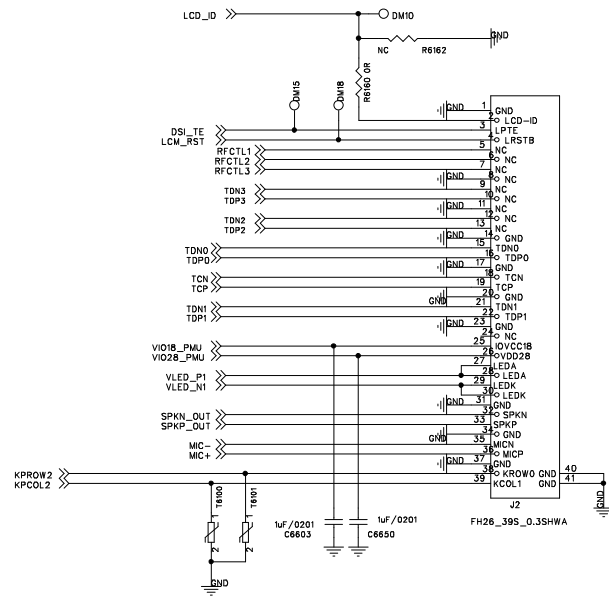
TK:reference design R5102=R5101=NC?

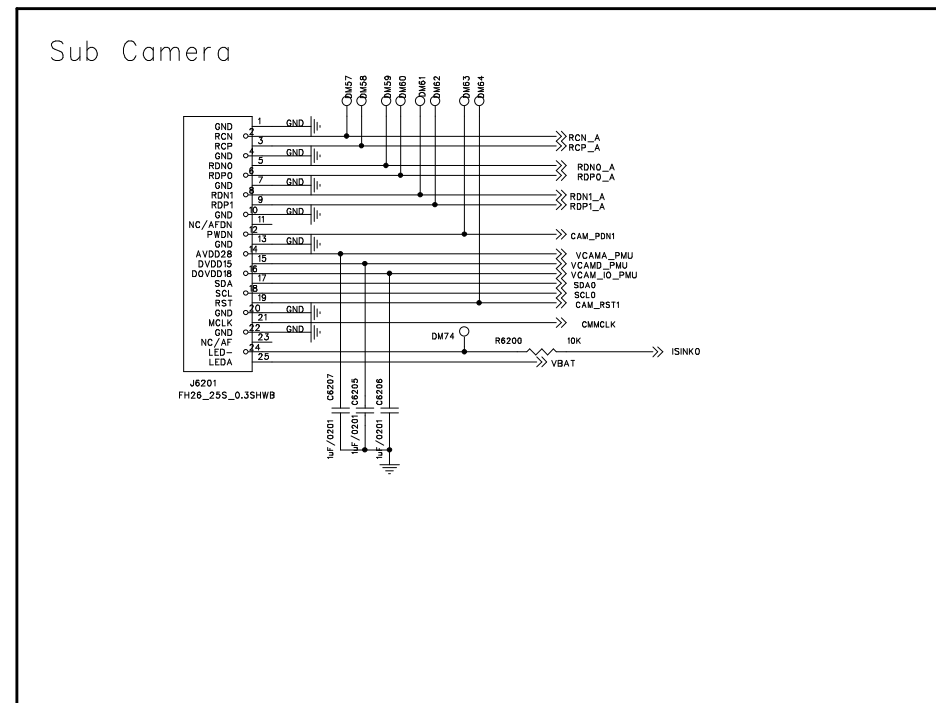
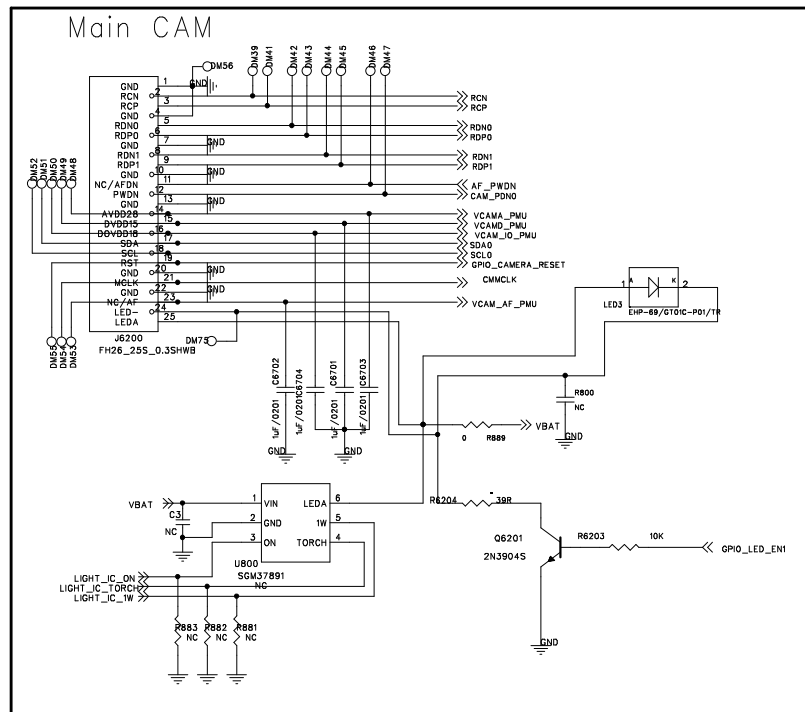


CTP Connector



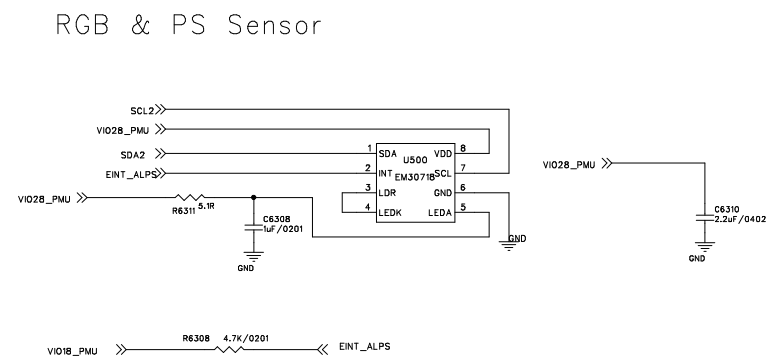
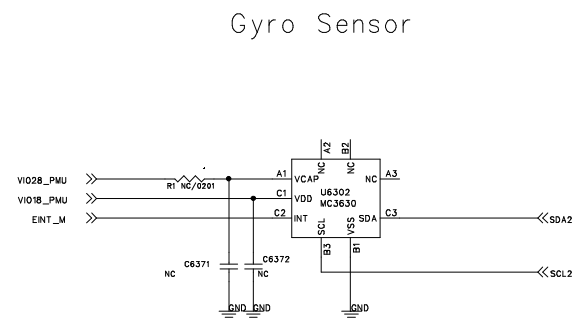
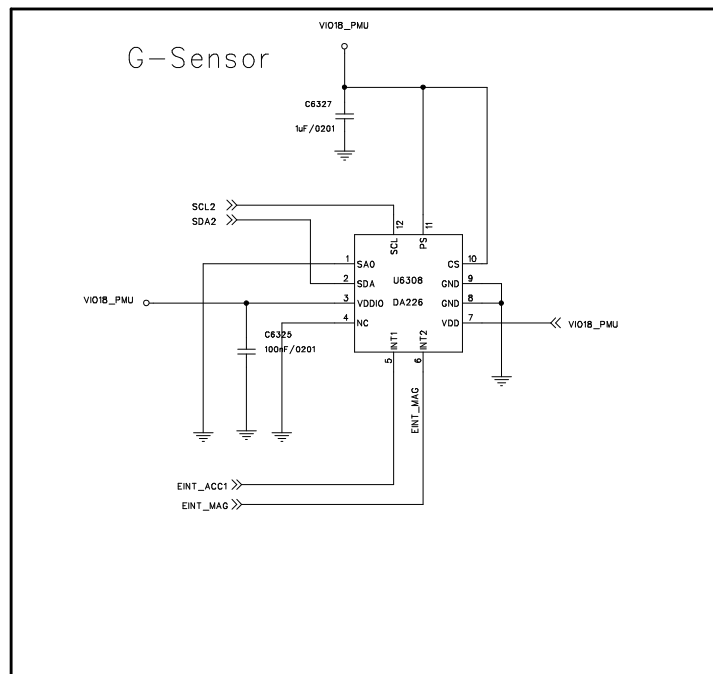
Main LCM





Schematic design notice of "62_PERI_CAMERA" page.

Note 62-1: If your project needs PIP function, please refer to MT6735 design notice for the connection of MCLK / I2C / AVDD & DVDD

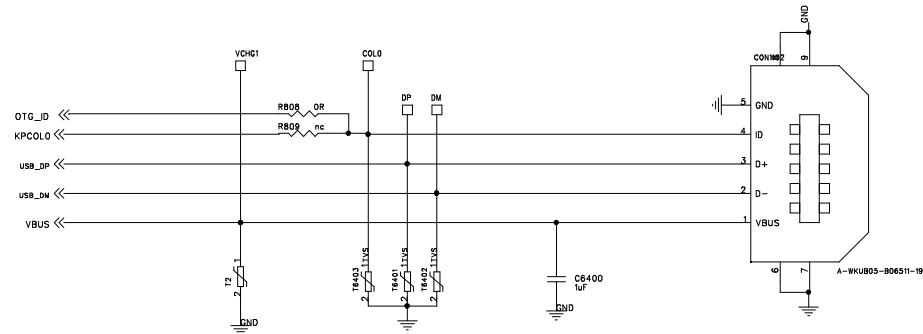


Thermistor / To sense board level temperature



USB HS IF

If mini-A connector insert => CID < 0V => Low
 If mini-B connector insert => CID > 1.2V => High
 IDPULLUP pin is replaced by 1.2V power source.



OTG POWER

