

Everestek

5GHz Module (MD)

Data Sheet

Everestek Inc.

Version: 0.1

Subject to change without further notice.

2022/05/06

INDEX

1. Features.....	3
2. Application	3
3. Electrical Specifications	4
4. I2S Format	5
5. I2C Timing.....	6
6. Module Pin Definition	7
7. Federal Communication Commission Interference Statement	9
8. Revision History	10

1. Features

The MD is a module based on dual Everestek ETK52, providing uncompressed or compressed audio applications operating in the 5.8/5.2 GHz bands.

The wireless audio link support lots of application, like subwoofer, stereo, headphone, headset, microphone, and comes with additional features such as data encryption, pairing functionality, bi-directional data messages, enhanced RF interference detection, and automatic frequency allocation.

Brief features include:

- Radio Frequency: 5.8/5.2 GHz unlicensed bands**
- Link Distance: up to 10 ~ 40 meters depends on application**
- Advanced RF Selection Algorithm**
- Small RF Foot Print**
- Best Coexistence with Wi-Fi/Bluetooth**
- Highly Integrated SoC: RF/PA/CPU/Flash Embedded**
- Wide-Band Antenna on Module**
- Short RBOM List**
- RF Modulation: FSK**
- Digital I2S (master or slave) Audio Interface, 16/24bit , 32/44.1/48/96KHz Sampling Rate**
- Low Power Consumption**
- Supply Voltage: 2.7~3.6V**
- Support I2C master/slave mode and UART**
- Compliant with EMC Regulations (FCC/CE)**

2. Application

- Wireless HIFI Mono**
- Wireless HIFI Stereo**
- Wireless 2.1CH with Advanced Audio Quality**

3. Electrical Specifications

RF Specification

Item	Min	Typ	Max	Unit	Note
RF Carrier Frequency	5725	—	5850	MHz	For 5.8G
	5135		5260		For 5.2G
-20dB bandwidth	—	2	—	MHz	
Output Power		7		dBm	
RF Sensitivity	—	-81		dBm	

Operation Condition

Item	Min	Typ	Max	Unit	Note
VDD	2.7	3.3	3.6	V	Power Supply Voltage
Operating Temperature	-5	25	60	°C	Ambient temperature

Electrical Specification (MCU+RF)

Item	Min	Typ	Max	Unit	Note
Transmitter current		160		mA	Output power 7dBm, two chip in operation
		80		mA	Output power 7dBm, one chip in operation
Receiver current		120		mA	Output power 7dBm, two chip in operation
		60		mA	Output power 7dBm, one chip in operation
RF idle with ARM @33MHz		40		mA	RF idle, two chip in operation
		24		mA	RF idle, one chip in operation
sleep mode		8		mA	Crystal enable, timer or interrupt wake up system

Note: power consumption is different depends on application.

Digital interface

Item	Min	Typ	Max	Unit	Note
VIH	0.7VDD		VDD+0.2	V	Input High Threshold
VIL	VSS		0.3VDD	V	Input Low Threshold
VOH	VDD-0.3		VDD	V	Output High Threshold
VOL	0		0.3	V	Output Low Threshold

4. I2S Format

ETK52 I2S data in and data out share the same LRCK and BCK pins. ETK52 can work in master mode and slave mode. The audio sampling rate can be 32/44.1/48K.

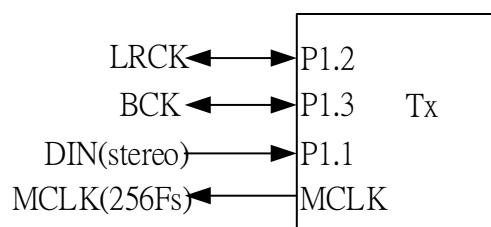
In master mode, ETK52 will generate I2S_MCLK/LRCK/BCK for external audio codec. In slave mode, ETK52 will receive external LRCK/BCK signal.

ETK52 has a digital controlled PLL, so the clock jitter noise will not be a problem in Rx.

During operate in slave mode, ETK52 will tracking external audio clock to make Tx and Rx work in the same frequency.

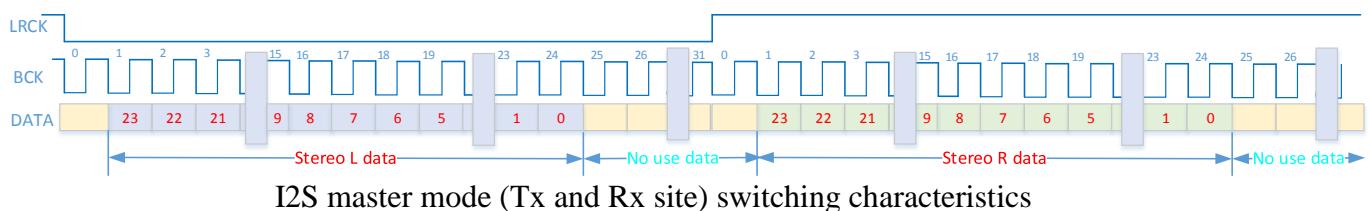
Mono channel data can feed through left channel (Lch) or right channel (Rch).

If 2(stereo) or 1(mono) channel application, Tx I2S signal connection as followed,



Note: if module is operated in I2S slave mode, module don't need MCLK signal. Only need BCK, LRCK, DIN signals.

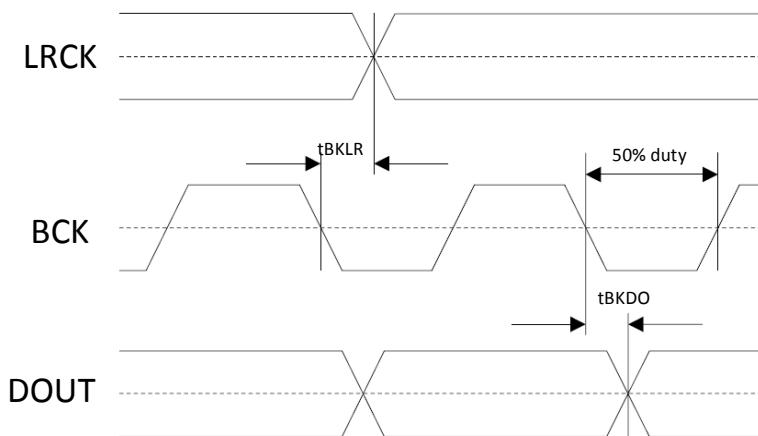
ETK52 work in 64 Fs mode. This means total 64 BCK pulse in one LRCK cycle. The I2S signal as the chart followed,



Symbol	Min	Typ	Max	Unit
MCLK		256fs		Hz
BCK		64fs		Hz
Duty (MCLK, BCK)		50		%

Symbol	Min	Typ	Max	Unit	Note
tBKLR	-1		+1	ns	
tBKDO (Rx only)	-1		+1	ns	BCK falling edge to DOUT transient

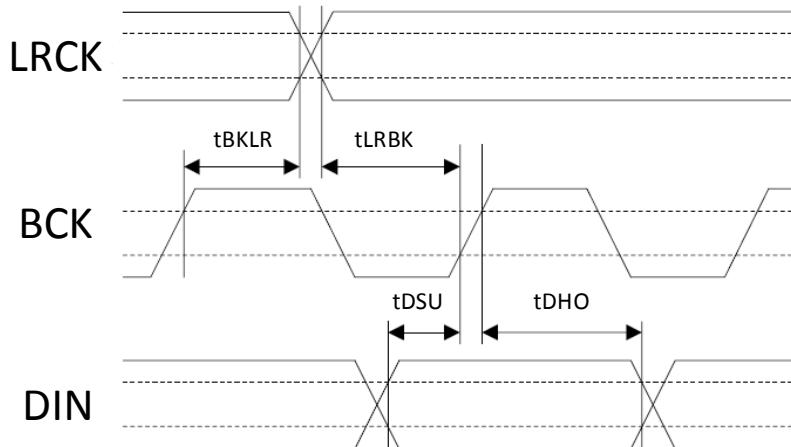
Note: DIN setup time and hold time timing in master mode is same as slave mode.



I2S slave mode (Tx site) switching characteristics

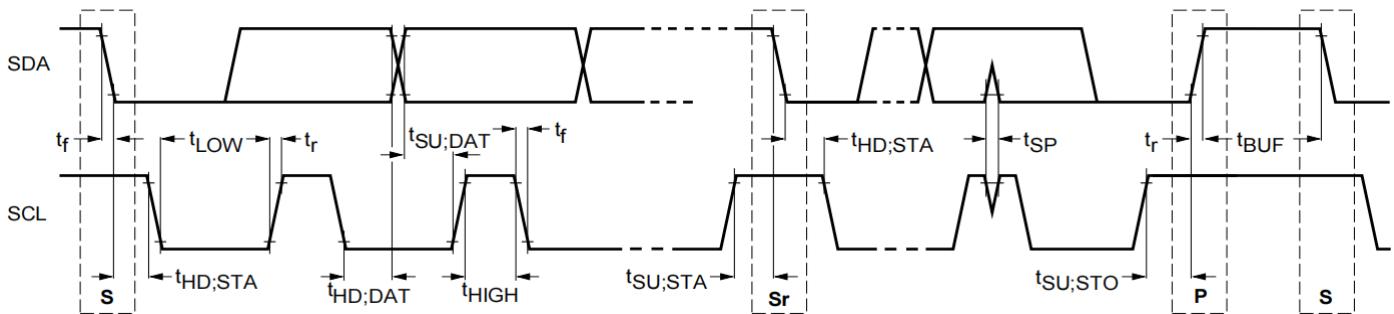
Symbol	Min	Typ	Max	Unit
BCK		64fs		Hz

Symbol	Min	Typ	Max	Unit	Note
tBKLR	10			ns	BCK rising to LRCK edge
tLRBK	10			ns	LRCK edge to BCK rising
tDSU	20			ns	DIN setup time
tDHO	20			ns	DIN hold time



Second I2S data input please refer to manual “2.1_Second_I2S_AppNote v1.0 for client.pdf”.

5. I2C Timing



Parameter	Symbol	Min	Max	unit
SCL clock frequency	F _{SCL}		200	KHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	t _{HD;STA}	4		us
LOW period of the SCL clock	t _{LOW}	2.2		us
HIGH period of the SCL clock	t _{HIGH}	2.2		us
Set-up time for a repeated START condition	t _{SU;STA}	4		us
Data hold time:	t _{HD;DAT}	0		us
Data set-up time	t _{SU;DAT}	100		ns
Rise time of both SDA and SCL signals	t _r		500	ns
Fall time of both SDA and SCL signals	t _f		300	ns
Set-up time for STOP condition	t _{SU;STO}	4		us
Bus free time between a STOP and START condition	T _{BUF}	10		us

Please also refer to "Everestek_I2C_200KHz_and_USB_HID_descrition.pdf" for detail.

6. Module Pin Definition

Note:

XXXX-**A**: means this GPIO is connect to A-chip.

XXXX-**B**: means this GPIO is connect to B-chip.

XXXX-**dual**: means this GPIO is connect to both A-chip and B-chip.

Pin	Name	I/O	Function Definition
1	VDD	P	VDD (2.7V~3.6V)
2	DGND	P	System ground
3	MCLK-A	O	For audio codec system clock(12.288MHz or 11.2896MHz)
4	DGND	P	System ground
5	D-_A	A	USB D-
6	DGND	P	System ground
7	D+_A	A	USB D+
8	DGND	P	System ground

9	P0.7_CS-A	I/O, C	GPIO and SPI SCK for SPI in programming internal flash mode
10	P2.0_DOUT1-A	I/O	I2S Data out (spare) or GPIO
11	P2.7-A	I/O	GPIO
12	P1.5_I2S_DataIn2-A	I/O	GPIO or 2nd I2S data input for subwoofer
13	P0.6_SCK-A	I/O, C	General I/O and SPI SCK for SPI in programming internal flash mode
14	P1.5-B	I/O	GPIO
15	P0.5_MISO-A	I/O, C	General I/O and SPI MISO for SPI in programming internal flash mode
16	FLASH_PROG	C	Program mode select, active high, default pull low For programming internal flash memory Please leave this pin float for normal operation.
17	P0.4_MOSI-A	I/O, C	General I/O and SPI MOSI for SPI in programming internal flash mode
18	P0.0_SCL-dual	I/O	General I/O, I2C clock
19	P0.1_SDA-dual	I/O	General I/O, I2C data
20	P2.0_DOUT1-B	I/O	I2S Data out (spare) or GPIO
21	P1.6-A	I/O	GPIO
22	P1.2_I2S_LRCK-dual	I/O	I2S LRCK(input for I2S slave, output for I2S master)
23	P2.7_PWM-B	I/O	GPIO or PWM
24	P1.3_I2S_BCK-dual	I/O	I2S BCK(input for I2S slave, output for I2S master)
25	P1.1_I2S_DIN-A	I/O	I2S Data in(from audio codec, or from ADC I2S DATA out)
26	P1.0_I2S_DOUT-A	I/O	I2S Data out(to audio codec, or to DAC I2S DATA in)
27	P1.1_I2S_DIN-B	I/O	I2S Data in(from audio codec, or from ADC I2S DATA out)
28	P1.0_I2S_DOUT-B	I/O	I2S Data out(to audio codec, or to DAC I2S DATA in)
29	P3.2-A	I/O	General I/O
30	P3.2-B	I/O	General I/O
31	P0.6_SCK-B	I/O, C	General I/O and SPI SCK for programming internal flash mode
32	P0.7_CS-B	I/O, C	General I/O and SPI chip select for programming internal flash mode
33	P0.4_MOSI-B	I/O, C	General I/O and SPI MOSI for programming internal flash mode
34	P0.5_MISO-B	I/O, C	General I/O and SPI MISO for programming internal flash mode

7. Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This device is restricted for indoor use.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

IMPORTANT NOTE:

This module is intended for OEM integrator. This module is only FCC authorized for the specific rule parts listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Additional testing and certification may be necessary when multiple modules are used.

USERS MANUAL OF THE END PRODUCT:

In the users manual of the end product, the end user has to be informed to keep at least **20cm** separation with the antenna while this end product is installed and operated. The end user has to be informed that the FCC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied.

The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:

The final end product must be labeled in a visible area with the following " Contains TX FCC ID: 2AWBQ-EWMD ".

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

Antenna Information

Ant.	Antenna Type	Gain (dBi)
1	PCB	2
2	PCB	2

8. Revision History

Revision	Descriptions	Date
0.1	Draft	2022/05/06