RM-240

IEEE802.15.4 compliant 2.4GHz Real-time communication module

Data Sheet

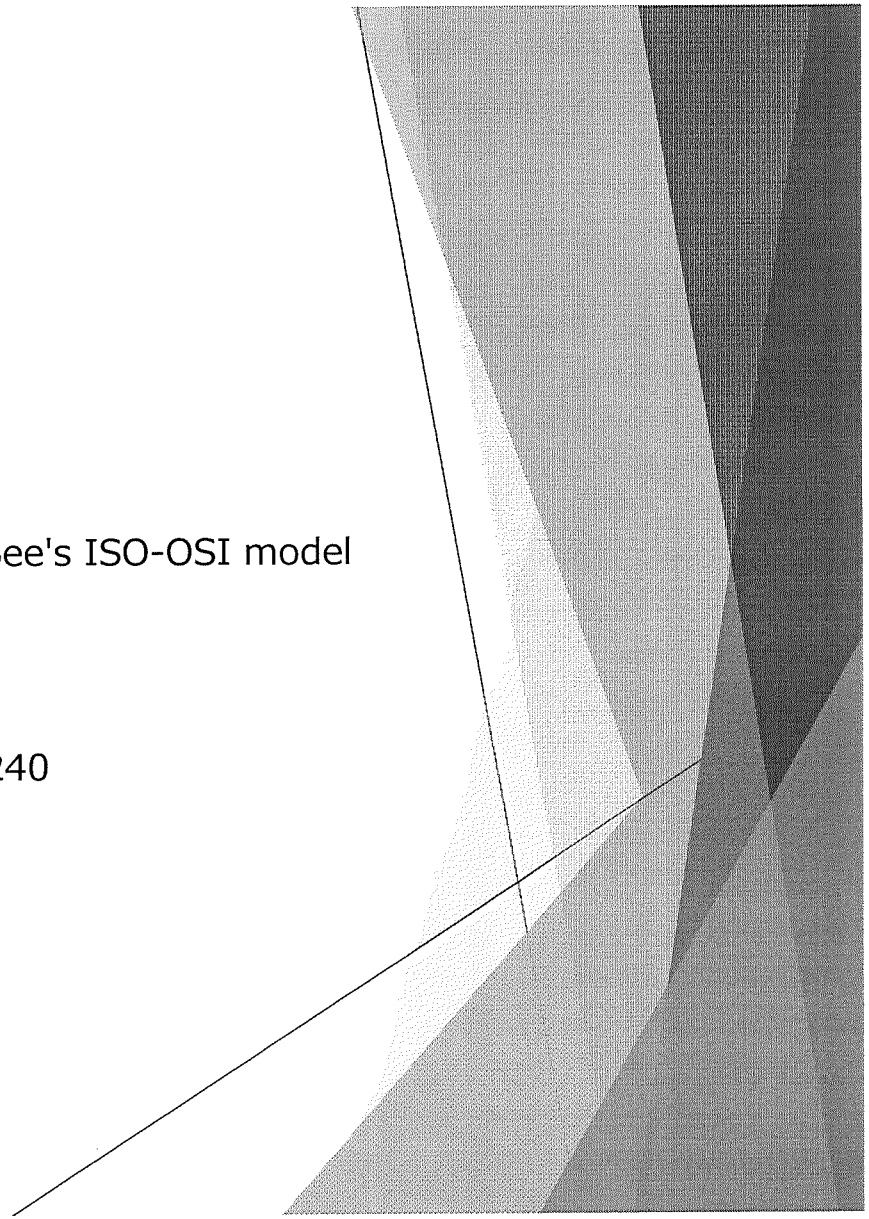
RF LINK

Table of contents

1. Introduction

2. RM-240 Hardware specifications
    2.1 Basic specifications
    2.2 PIN Sequence
3. RM-240 Firmware specifications
    3.1 Comparison between OSI basic model and ZigBee's ISO-OSI model
    3.2 Memory map

4.RM-240 Radio characteristics
    4.1 Radio characteristics
    4.2 Precautions when creating a substrate for RM-240



1. Introduction

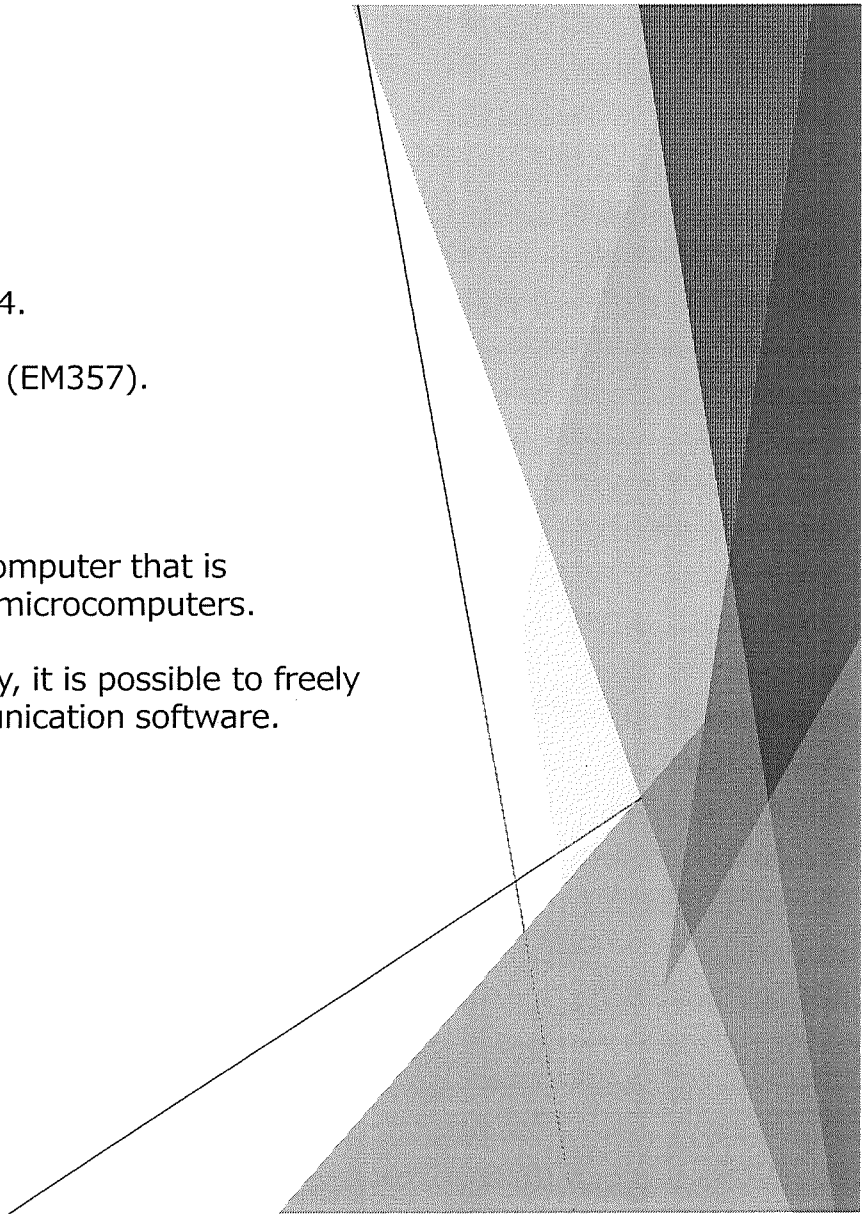
RM-240 is a 2.4GHz band wireless module compliant with IEEE802.15.4.

Chip antenna type wireless module with built-in SiliconLabs 32-bit CPU (EM357).
The smallest size in the world is realized.

(CPU:ARM Cortex M3)

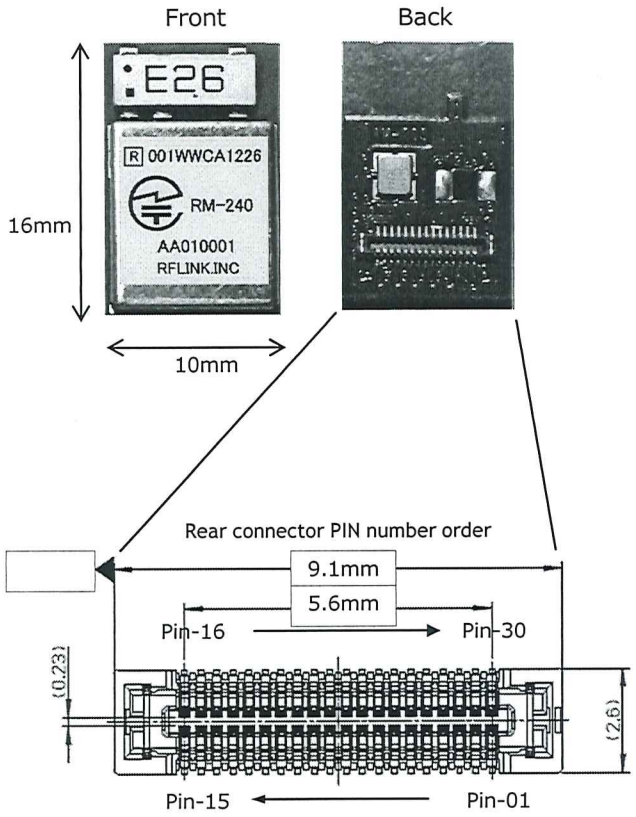
In addition to RF devices, the RM-240 uses a wireless one-chip microcomputer that is equipped with various peripherals that are necessary for general RISC microcomputers.

Therefore, by purchasing the development kit provided by our company, it is possible to freely develop and modify based on the source code of the MAC layer communication software.



2.RM-240 Hardware specifications

2.1 Basic specifications



No	Item	Content
01	Maximum transmission output	+7dBm
02	Receive sensitivity	-98dBm
03	Wireless standard	IEEE802.15.4 compliant
04	Modulation method	DSSS/O-QPSK
05	CH number	16ch
06	power consumption	TX:40mA RX:29mA Sleep time 0.8μA or less
07	weight	0.8g or less
08	External dimensions	16.0mm(H)×10mm(W)×3.1mm(D)
09	transfer speed	250Kbps
10	Communication distance	About 120m (Line-of-sight distance)
11	Core processor	EM357 (ARM CoretexM3)
12	Built-in memory	FlashROM 128KB SRAM 12KB
13	Power-supply voltage	2.1V～3.6V
14	External interface	GPIO(24PIN) / ADC(12bit×6ch) / SPI(1ch) / I2C(1ch) / UART(1ch) ※The number of GPIO PINs varies depending on the usage of internal peripherals.
15	Operating temperature	-25℃～+75℃
16	Rear connector	Molex 502430-3010 (PCB side socket : 502426-3010)
17	Environment	RoHS compliant
18	Radio Act (in japan)	TELEC construction design certification acquired (001WWCA1226)

2.RM-240 Product Specifications

2.2 PIN Sequence listing (1/3)

PIN	記号	I/O	内容
01	PA3	I/O	Digital I/O
	SC2 n SSEL	I	SPI slave select of Serial Controller 2
	TRACECLK	O	Synchronous CPU trace clock
	TIM2_CH2	O	Timer 2 channel 2 output
		I	Timer 2 channel 2 input.
02	PA4	I/O	Digital I/O
	ADC4	I	ADC Input 4
	PTI_EN	O	Frame signal of Packet Trace Interface
	TRACEDATA2	O	Synchronous CPU trace data bit 2
03	PA5	I/O	Digital I/O
	ADC5	I	ADC Input 5
	PTI_DATA	O	Data signal of Packet Trace Interface
	nBOOTMODE	I	Embedded serial bootloader activation
	TRACEDATA3	O	Synchronous CPU trace data bit 3
04	PA2	I/O	Digital I/O
	TIM2_CH4	O	Timer 2 channel 4 output
		I	Timer 2 channel 4 input.
	SC2SCL	I/O	TWI clock of Serial Controller 2
	SC2SCLK	O	SPI master clock of Serial Controller 2
		I	SPI slave clock of Serial Controller 2
05	PA6	I/O	Digital I/O
	TIM1_CH3	O	Timer 1 channel 3 output
		I	Timer 1 channel 3 output

PIN	記号	I/O	内容
06			NC
07	PB1	I/O	Digital I/O
	SC1MISO	O	SPI slave data out of Serial Controller 1
	SC1MOSI	O	SPI master data out of SerialController1
	SC1SDA	I/O	TWI data of Serial Controller 1
	SC1TXD	O	UART transmit data of Serial Controller 1
	TIM2_CH1	O	Timer 2 channel 1 output
		I	Timer 2 channel 1 input
08	PB2	I/O	Digital I/O
	SC1MISO	I	SPI master data in of Serial Controller 1
	SC1MOSI	I	SPI slave data in of Serial Controller 1
	SC1SCL	I/O	TWI clock of Serial Controller 1
	SC1RXD	I	UART receive data of Serial Controller 1
	TIM2_CH2	O	Timer 2 channel 2 output
		I	Timer 2 channel 2 input
09	SWCLK	I/O	Serial Wire clock I/O with debugger
	JTCK	I	JTAG clock input from debugger
10	PC2	I/O	Digital I/O
	JTDO	O	JTAG data out to debugger
	SWO	O	Serial Wire Output asynchronous trace output to debugger

2.RM-240 Hardware specifications

2.2 PIN Sequence listing (2/3)

PIN	記号	I/O	内容
11	PC3	I/O	Digital I/O
	JTD1	I	JTAG data in from debugger
12	PC4	I/O	Digital I/O
	JTMS	I	JTAG mode select from debugger
	SWDIO	I/O	Serial Wire bidirectional data
13	PB0	I/O	Digital I/O
	VREF	O	ADC reference output.
	VREF	I	ADC reference input.
	IRQA	I	External interrupt source A.
	TRACECLK	O	Synchronous CPU trace clock
	TIM1CLK	I	Timer 1 external clock input.
	TIM1CLK	I	Timer 2 external clock mask input.
14	VDD_PADS		Pads supply (2.1-3.6 V)
15	VDD_PADS		Pads supply (2.1-3.6 V)

PIN	記号	I/O	内容
16	PC0	I/O	Digital I/O
	JRST	I	JTAG reset input from debugger
	IRQD	I	Default external interrupt source D
	TRACEDATA1	O	Synchronous CPU trace data bit 1
17	PC1	I/O	Digital I/O
	ADC3	I	ADC Input 3
	SWO	O	Serial Wire Output output to debugger
	TRACEDATA0	O	Synchronous CPU trace data bit 0
18	PB7	I/O	Digital I/O
	ADC2	I	ADC Input 2
	IRQC	I	Default external interrupt source C
	TIM1_CH2	O	Timer 1 channel 2 output
		I	Timer 1 channel 2 input
19	PB6	I/O	Digital I/O
	ADC1	I	ADC Input 1
	IRQB	I	External interrupt source B
	TIM1_CH1	O	Timer 1 channel 1 output
		I	Timer 1 channel 1 input
20	PB5	I/O	Digital I/O
	ADC0	I	ADC Input 0
	TIM2CLK	I	Timer 2 external clock input
	TIM1MSK	I	Timer 2 external clock mask input

2.RM-240 Hardware specifications

2.2 PIN Sequence listing (3/3)

PIN	記号	I/O	内容
21			NC
22	PC5	I/O	Digital I/O
	TX_ACTIVE	O	Logic-level control for ext Rx/Tx switch.
23	nRESET	I	Active low chip reset
24	GND		Ground
25	GND		Ground
26	PA1	I/O	Digital I/O
	TIM2_CH3	O	Timer 2 channel 3 output
		I	Timer 2 channel 3 input
	SC2SDA	I/O	TWI data of Serial Controller 2
	SC2MISO	O	SPI slave data out of Serial Controller 2
		I	SPI master data in of Serial Controller 2
27	PA7	I/O	Digital I/O
	TIM1_CH4	O	Timer 1 Channel 4 output
		I	Timer 1 Channel 4 input
	REG_EN	I	External regulator open drain output

PIN	記号	I/O	内容
28	PB3	I/O	Digital I/O
	TIM2_CH3	O	Timer 2 channel 3 output
		I	Timer 2 channel 3 input
	UART_CTS	I	UART CTS Serial Controller 1
	SC1SCLK	O	SPI master clock of Serial Controller 1
		I	SPI slave clock of Serial Controller 1
29	PB4	I/O	Digital I/O
	TIM2_CH4	O	Timer 2 channel 4 output
		I	Timer 2 channel 4 input
	UART_RTS	O	UART RTS Serial Controller 1
	SC1nSSEL	I	SPI slave select of Serial Controller 1
30	PA0	I/O	Digital I/O
	TIM2_CH1	O	Timer 2 channel 1 output
		I	Timer 2 channel 1 input
	SC2MOSI	O	SPI master data out of Serial Controller 2
		I	SPI slave data in of Serial Controller 2

3.RM-240 Firmware specifications

3.1 Comparison between OSI basic model and ZigBee's ISO-OSI model

Compared to the standard OSI model in Figure 1, the ZigBee OSI model is configured in Figure 2, and the proprietary MAC communication stack is configured in Figure 3.
The following three types of software can be used with the RM-240.
It can be used according to the customer's application.

- ZigBee-PRO stack — The Software part necessary for standard ZigBee communication
- SimpleMAC stack — The communication software part directly connected to the MAC layer
- RF4CE profile stack — This software part conforms to the remote control profile.

Figure 1 OSI basic model

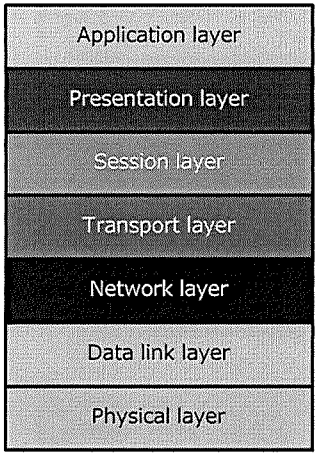


Figure 2 ZigBee basic model

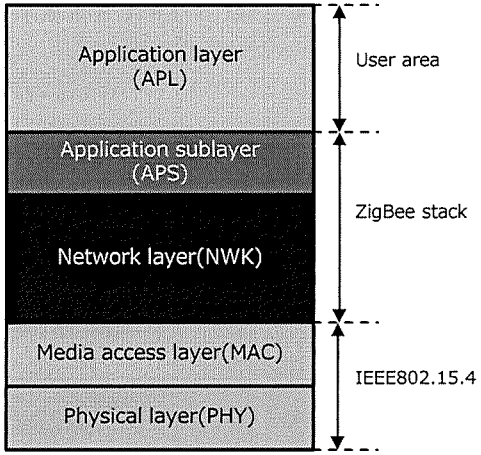
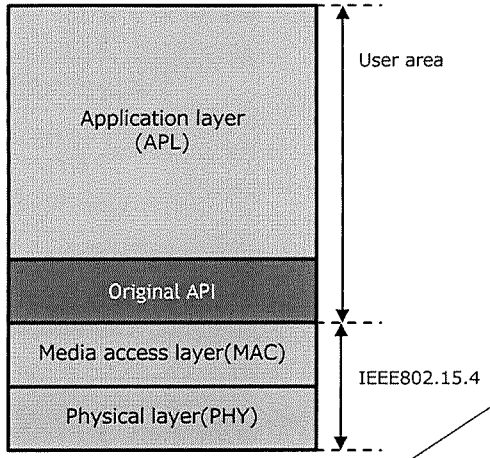


Figure 3 MAC layer communication model

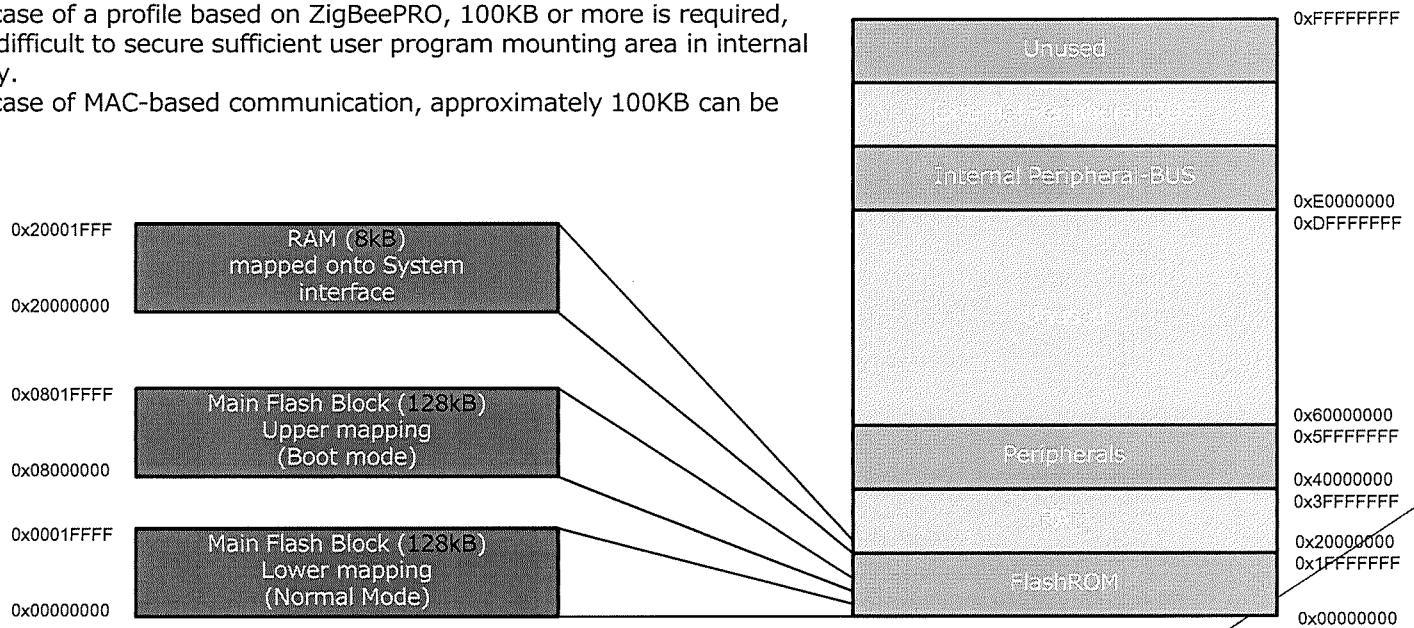


3.RM-240 Firmware specifications

3.2 RM-240　memory map

RM-240 is equipped with EM357 from Silicon Lapse.
For detailed processor specifications, download the data sheet from our website.

The required memory size varies depending on the installed profile.
In the case of a profile based on ZigBeePRO, 100KB or more is required, so it is difficult to secure sufficient user program mounting area in internal memory.
In the case of MAC-based communication, approximately 100KB can be used.



4.RM-240 Radio characteristics

4.1 Radio characteristics

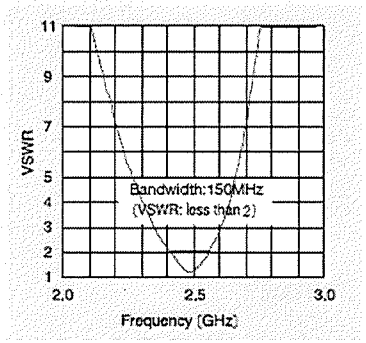
RM-240 has a chip antenna manufactured by Taiyo Yuden Co., Ltd.

Model number : AH083F245001

For details on the radio characteristics of RM-240, refer to the Taiyo Yuden website.

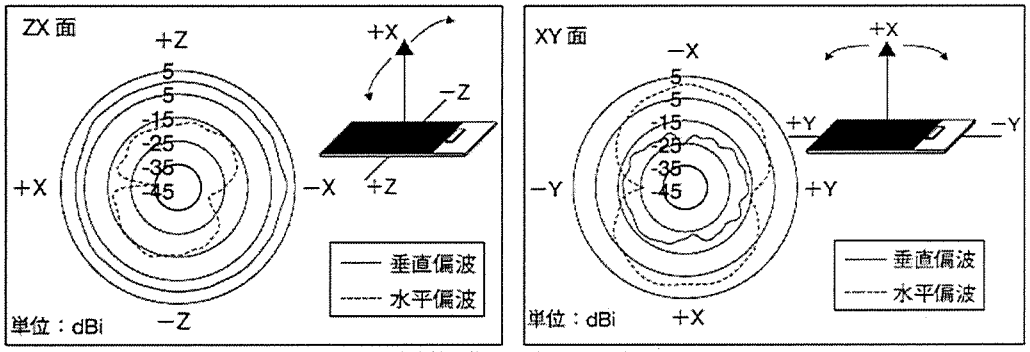
http://www.yuden.co.jp/jp/product/pdf/chipantenna01_j.pdf

●AH 083F245001



VSWR特性の代表例

Typical example of
VSWR characteristics



指向性の代表例（@2.45GHz）

unit

Typical example of
directivity

vertically polarized wave
horizontally polarized wave

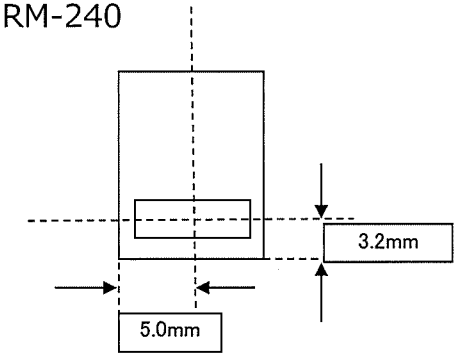
4.RM-240 Radio characteristics

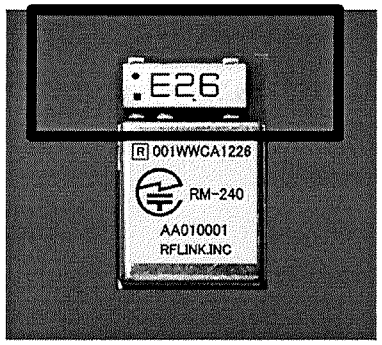
4.2 Precautions when creating a substrate for RM-240

◆User side board socket position

The socket is made by Molex 502426-3010.
(Dimensions are the center position of the socket)

* It is recommended to put silk printing around the outside of RM-240.





◆Customer development board

◆Pattern prohibited area

A 2.4Ghz band chip antenna is mounted on top of the RM-240. Since the antenna characteristics will be affected, avoid mounting the pattern, GND, and front / rear parts on the red frame as much as possible.

◆For installation of RM-240

When mounting RM-240 on the board, fix the back surface and the board with double-sided rubber tape if necessary.

In particular, when mounting products that are subject to vibration or shock, consider a stronger fixing method.

低功率電波幅射性電機管理辦法

第十二條

經型式認證合格之低功率射頻電機，非經許可，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。

第十四條

低功率射頻電機之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。

前項合法通信，指依電信法規定作業之無線電通信。低功率射頻電機須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

FCC Warning

1. This device complies with part 15 of the fcc rules. Operationis subject to the following two conditions: (1) this device maynot cause harmful interference, and (2) this device mustaccept any interference received, including interference thatmay cause undesired operation.
2. NOTE: the grantee is not responsible for any changes or modifications not expressly approved by the party responsible for compliance. Such modifications could void the user's authority to operate the equipment.
3. Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

   —Reorient or relocate the receiving antenna.

   —Increase the separation between the equipment and receiver.

   —Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

   —Consult the dealer or an experienced radio/TV technician for help.

RF warning statement:Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC rules. Operation is subject to the followin two conditions:

(1)This device may not cause harmful interference, and

(2)This device must accept any interference received including interference that may cuased undersired operation.

Information for the Integrators:

1)Antenna Type: Chip Antenna, Gain: 1.8dBi

2)The modular transmitter is used for FCC part 15C listed on the FCC grant. The final host product manufacturer is responsible to ensure the host product undergoes FCC part 15B compliance testing with the modular transmitter installed.

3)Please see the full Grant Equipment document for other restriction.

4)The final end product must be labeled in a visible area with following " Contain FCC ID: 2AVOZ-CETOPZWTW"

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