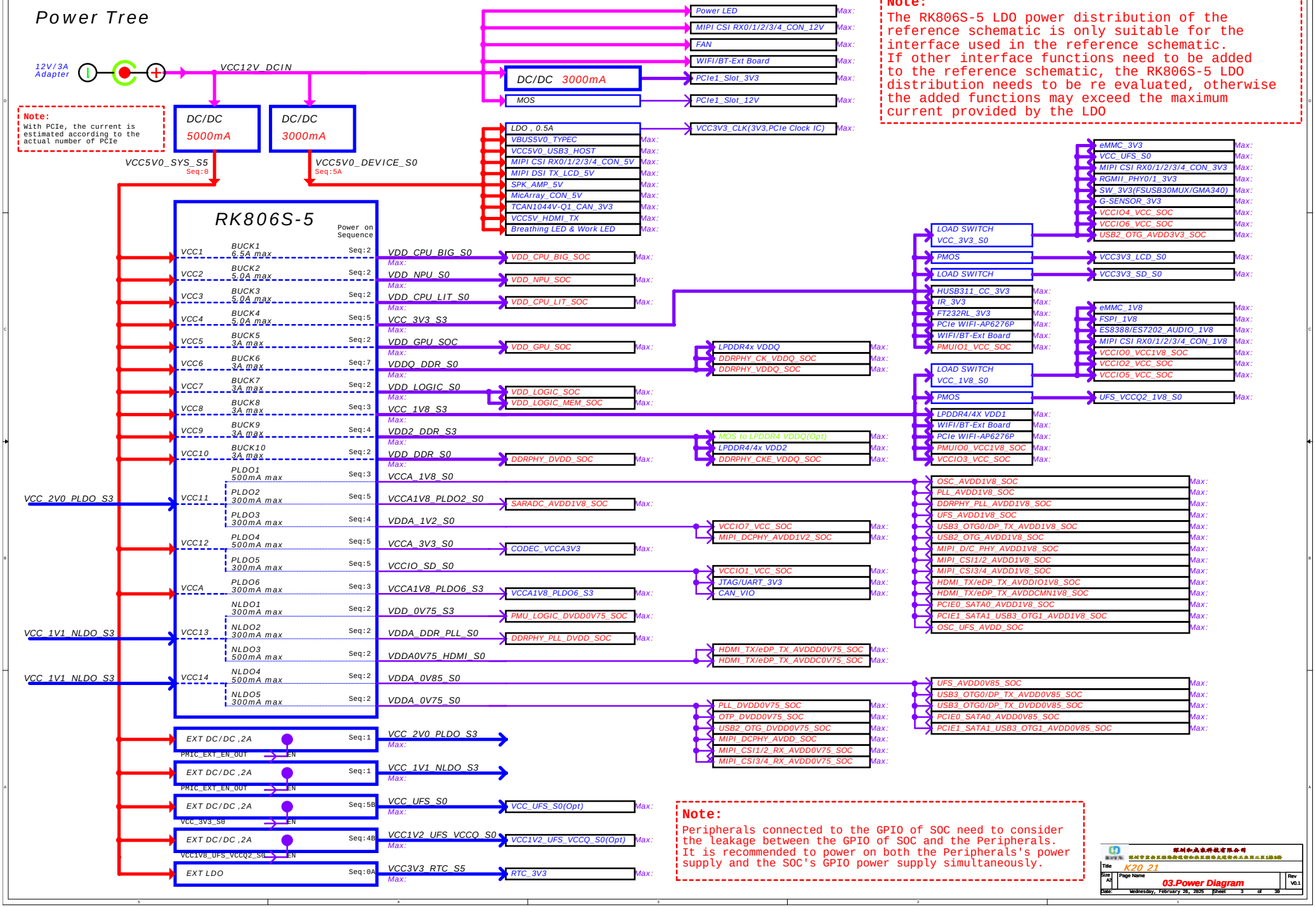
Power Tree

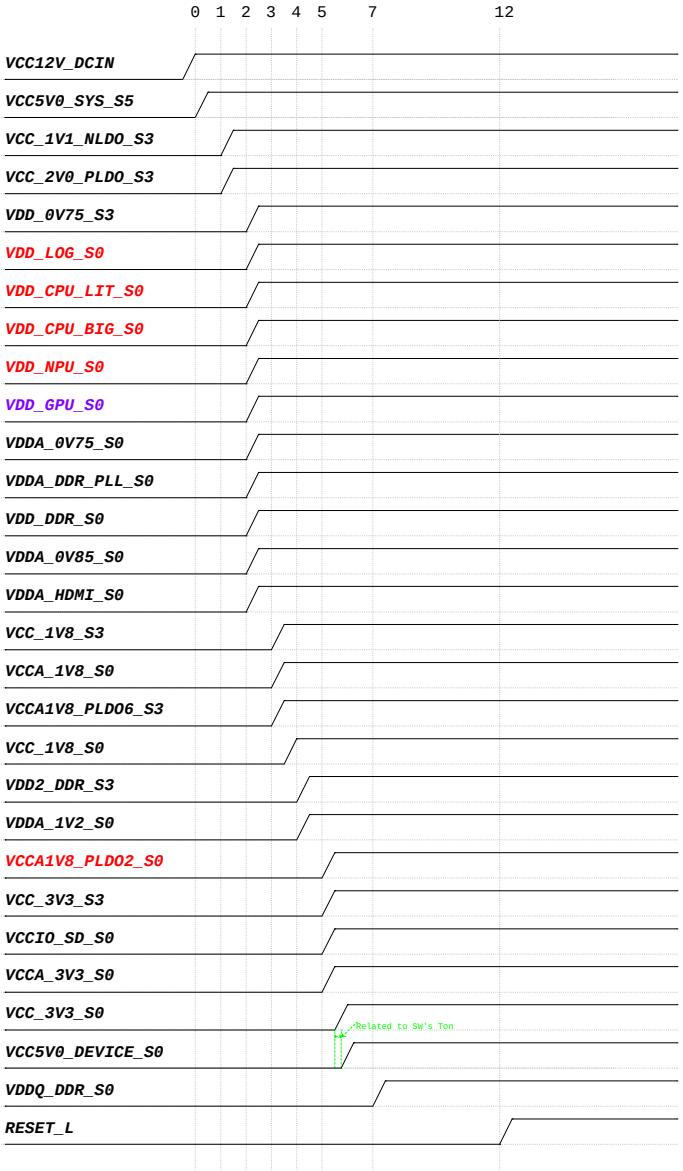


Note:
The RK806S-5 LDO power distribution of the reference schematic is only suitable for the interface used in the reference schematic. If other interface functions need to be added to the reference schematic, the RK806S-5 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

Note:
Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

Title	K20_21	
Size A2	Page Name 03.Power Diagram	Rev V0.1
Date: Wednesday, February 26, 2025	Sheet 3 of 30	

Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC5V0_SYS_S5	RK806_BUCK1	6.5A	VDD_CPU_BIG_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK2	5A	VDD_NPU_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK3	5A	VDD_CPU_LIT_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK4	5A	VCC_3V3_S3	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK5	3A	VDD_GPU_S0	Slot:2	ADJ FB=0.5V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK6	3A	VDDQ_DDR_S0	Slot:7	ADJ FB=0.5V	ON	0.61V-LP4/4x 0.51V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK7	3A	VDD_LOGIC_S0 VDD_LOGIC_MEM_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK8	3A	VCC_1V8_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK9	3A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	1.1V-LP4/4x 1.05V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK10	3A	VDD_DDR_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_PLDO2_S0	Slot:5	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO4	0.5A	VCCA_3V3_S0	Slot:5	3.0V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD_S0	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA0V75_HDMI_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETn								
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_2V0_PLDO_S3	Slot:1	2.1V	ON	2.0V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	5A	VCC5V0_SYS_S5	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_DEVICE_S0	Slot:5A	5.2V	ON	5.2V	TBD	TBD
VCC_3V3_S3	SWITCH	2A	VCC_3V3_S0	Slot:5A	3.3V	ON	3.3V	TBD	TBD
VCC_1V8_S3	SWITCH	2A	VCC_1V8_S0	Slot:3A	1.8V	ON	1.8V	TBD	TBD

Note:
The power suffix S0, S3 or S5 means:
S5: Keep power on during power down
S3: Keep power on during sleeping
S0: Power off during sleeping

Note:
Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

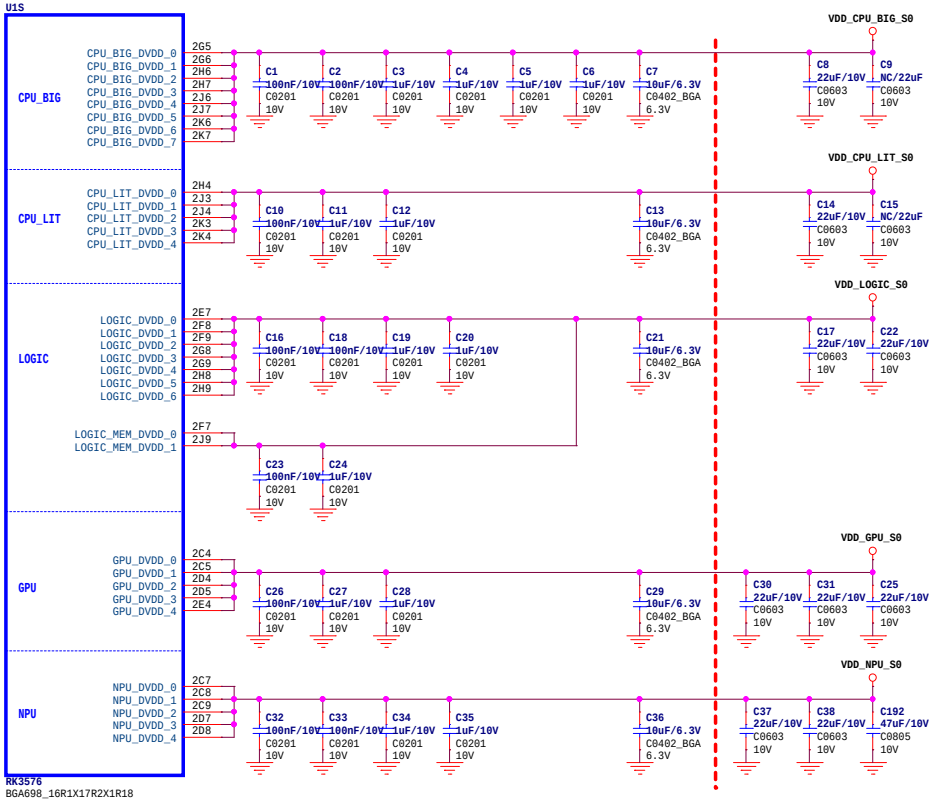
IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO0	Pin 2K11	1.8V Only	PMUIO0_VCC1V8	VCC_1V8	1.8V
PMUIO1	Pin 1U20	1.8V or 3.3V	PMUIO1_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO0	Pin 1J20	1.8V Only	VCCIO0_VCC1V8	VCC_1V8	1.8V
VCCIO1	Pin 2A8	1.8V or 3.3V	VCCIO1_VCC	VCC_1V8 VCC_3V3	1.8V/3.3V
VCCIO2	Pin 2A2	1.8V or 3.3V	VCCIO2_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO3	Pin 2B10	1.8V or 3.3V	VCCIO3_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO4	Pin 2A7	1.8V or 3.3V	VCCIO4_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO5	Pin 2A4/2A5	1.8V or 3.3V	VCCIO5_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO6	Pin 2N3	1.8V or 3.3V	VCCIO6_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO7	Pin 2M3	1.2V or 1.8V	VCCIO7_VCC	VCC_1V2 VCC_1V8	1.2V

IO Type	Operating Voltage
1.8V Only	VCCIO*_VCC1V8=1.8V
1.2V or 1.8V	VCCIO*_VCC=1.2V or 1.8V
1.8V or 3.3V	VCCIO*_VCC=1.8V or 3.3V

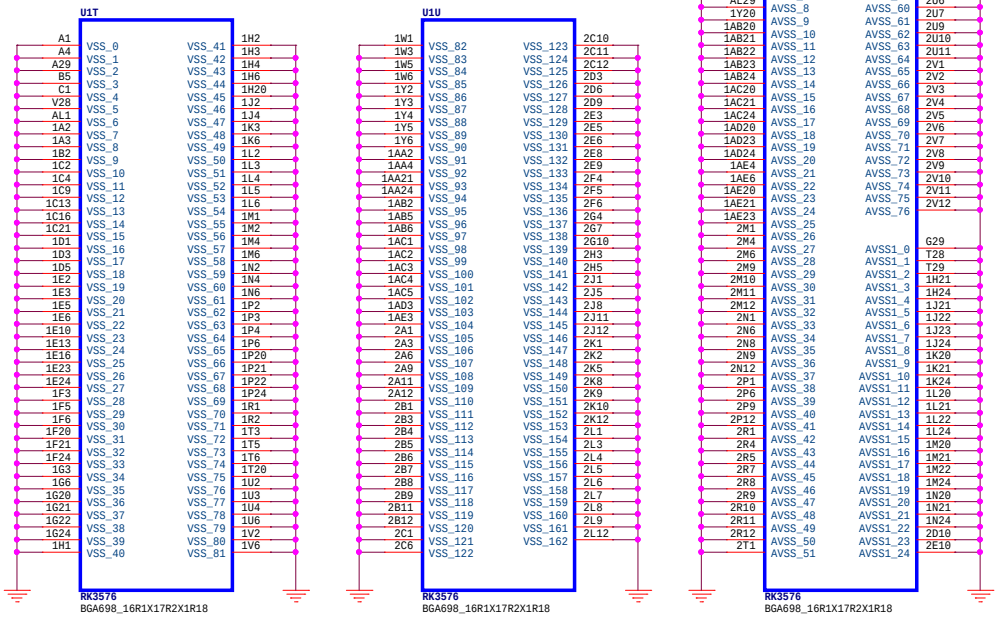
深圳和威东科技有限公司
深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼
Title K20_21
Size A3 | Page Name 04.Power Sequence and Map | Rev V0.1
Date: Wednesday, February 26, 2025 | Sheet 4 of 30

RK3576_S (Power)



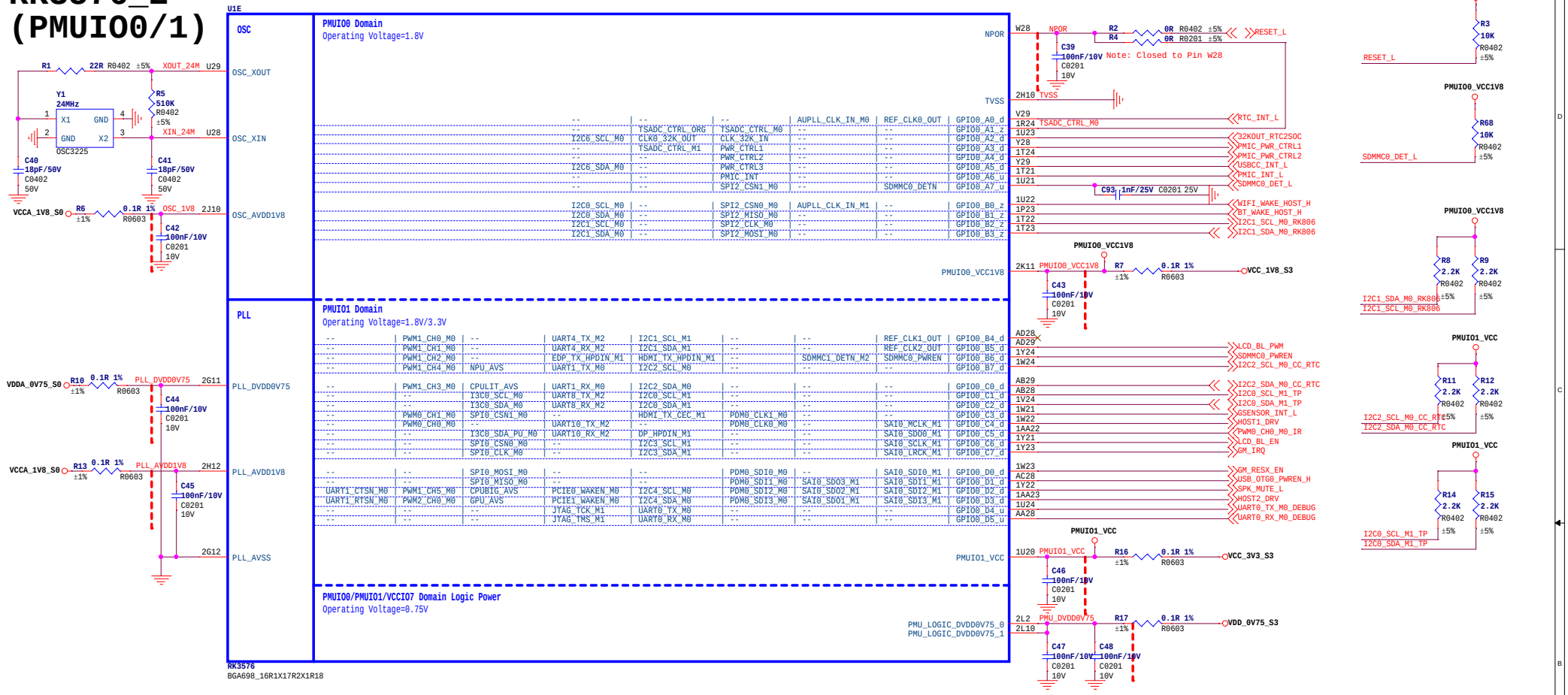
Note:
Caps of between dashed red lines and U1
should be placed under the U1 package.
Other caps should be placed close to the U1 package

RK3576_T/U/V (GND)

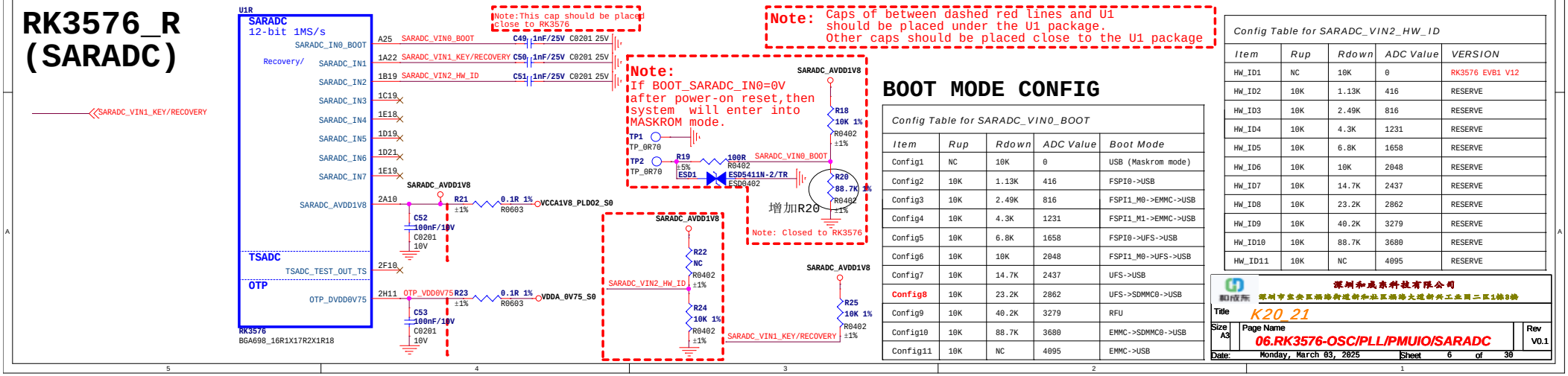


深圳市宝安区福海街道新和社区福海大道新共工业园二区1栋3楼	深圳和成东科技有限公司
Title	K20_21
Size A3	Page Name 05.RK3576-Power/GND
Rev	V0.1
Date: Wednesday, February 26, 2025	Sheet 5 of 30

RK3576_E (PMUIO0/1)



RK3576_R (SARADC)



BOOT MODE CONFIG

Config Table for SARADC_VIN0_BOOT

Item	Rup	Rdown	ADC Value	Boot Mode
Config1	NC	10K	0	USB (Maskrom mode)
Config2	10K	1.13K	416	FSPI0->USB
Config3	10K	2.49K	816	FSPI1_M0->EMMC->USB
Config4	10K	4.3K	1231	FSPI1_M1->EMMC->USB
Config5	10K	6.8K	1658	FSPI0->UFS->USB
Config6	10K	10K	2048	FSPI1_M0->UFS->USB
Config7	10K	14.7K	2437	UFS->USB
Config8	10K	23.2K	2862	UFS->SDMMC0->USB
Config9	10K	40.2K	3279	RFU
Config10	10K	88.7K	3680	EMMC->SDMMC0->USB
Config11	10K	NC	4095	EMMC->USB

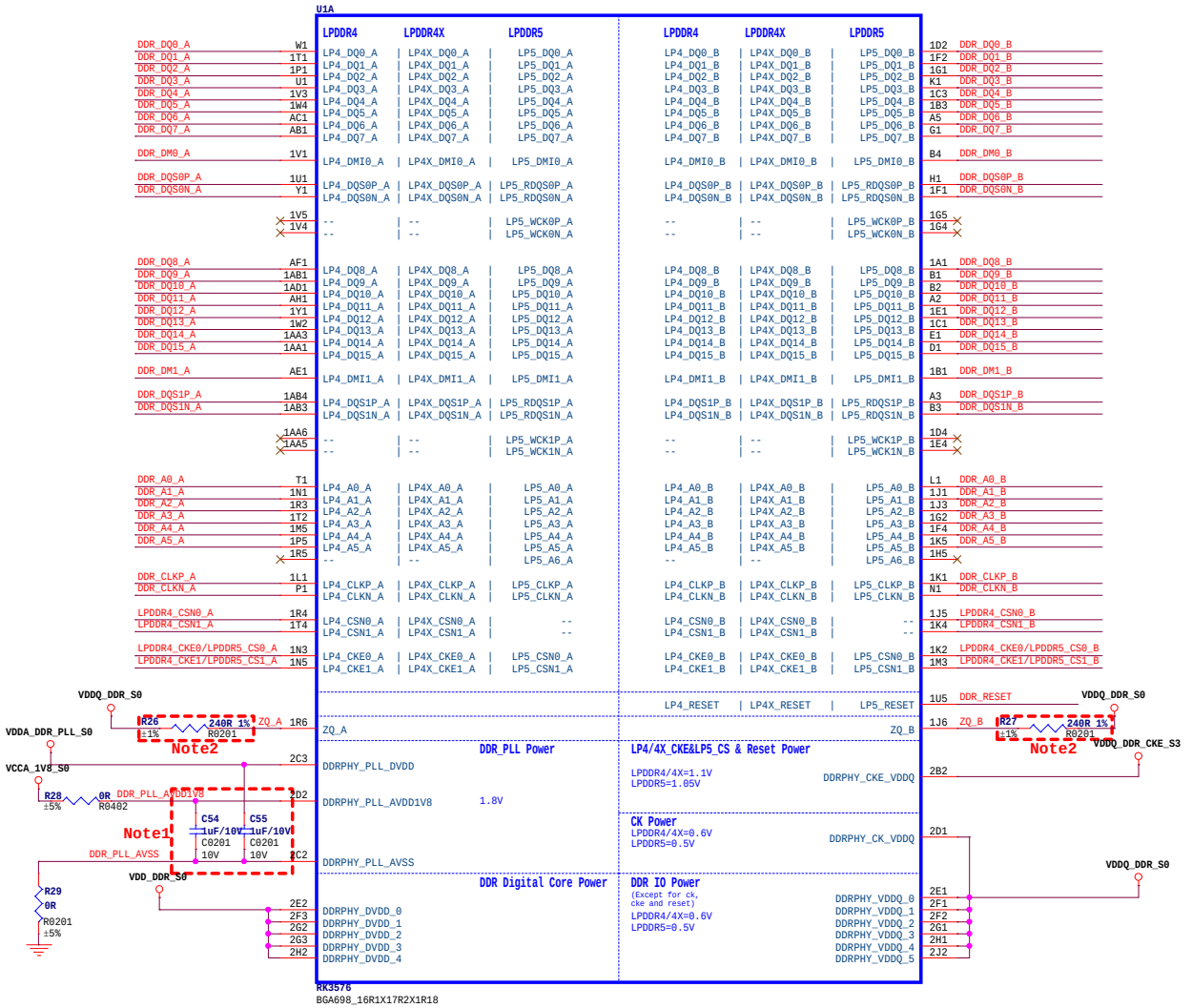
Config Table for SARADC_VIN2_HW_ID

Item	Rup	Rdown	ADC Value	VERSION
HW_ID1	NC	10K	0	RK3576 EVB1 V12
HW_ID2	10K	1.13K	416	RESERVE
HW_ID3	10K	2.49K	816	RESERVE
HW_ID4	10K	4.3K	1231	RESERVE
HW_ID5	10K	6.8K	1658	RESERVE
HW_ID6	10K	10K	2048	RESERVE
HW_ID7	10K	14.7K	2437	RESERVE
HW_ID8	10K	23.2K	2862	RESERVE
HW_ID9	10K	40.2K	3279	RESERVE
HW_ID10	10K	88.7K	3680	RESERVE
HW_ID11	10K	NC	4095	RESERVE

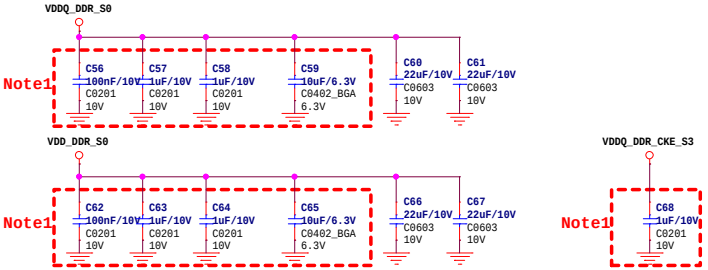
深圳和成系科技有限公司
深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼

Title	K20_21		
Size A3	Page Name	06.RK3576-OSC/PLL/PMUIO/SARADC	Rev V0.1
Date: Monday, March 03, 2025	Sheet 6 of 30		

RK3576_A(DDRPHY)



DDR FILTER



Note:
(1) Power Sequence: VDD-VDDQ_CKE-VDDQ
(2) Hold power of DDRPHY_CKE_VDDQ during retention times.

Note1:
Caps in the red line dotted box should be placed under the U1 package

Note2:
Resistors in the red line dotted box should be placed under the U1 package

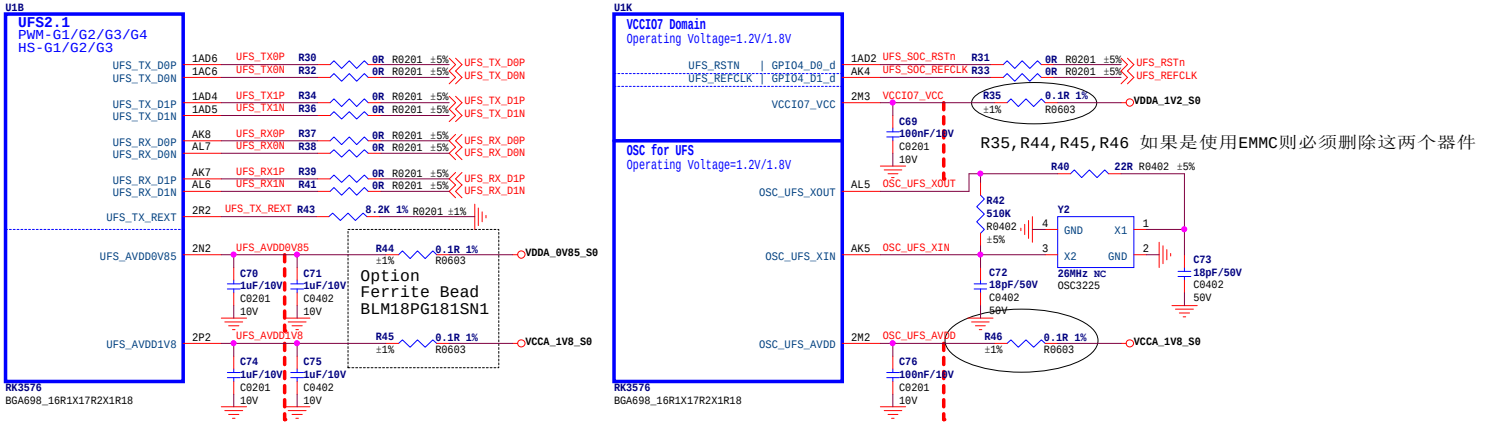
LPDDR4 Signal

DDR_DQ0_A → LPDDR4_DQ0_A
DDR_DQ1_A → LPDDR4_DQ1_A
DDR_DQ2_A → LPDDR4_DQ2_A
DDR_DQ3_A → LPDDR4_DQ3_A
DDR_DQ4_A → LPDDR4_DQ4_A
DDR_DQ5_A → LPDDR4_DQ5_A
DDR_DQ6_A → LPDDR4_DQ6_A
DDR_DQ7_A → LPDDR4_DQ7_A
DDR_DQS0P_A → LPDDR4_DQS0P_A
DDR_DQS0N_A → LPDDR4_DQS0N_A
DDR_DM0_A → LPDDR4_DMI0_A
DDR_DQ8_A → LPDDR4_DQ8_A
DDR_DQ9_A → LPDDR4_DQ9_A
DDR_DQ10_A → LPDDR4_DQ10_A
DDR_DQ11_A → LPDDR4_DQ11_A
DDR_DQ12_A → LPDDR4_DQ12_A
DDR_DQ13_A → LPDDR4_DQ13_A
DDR_DQ14_A → LPDDR4_DQ14_A
DDR_DQ15_A → LPDDR4_DQ15_A
DDR_DQS1P_A → LPDDR4_DQS1P_A
DDR_DQS1N_A → LPDDR4_DQS1N_A
DDR_DM1_A → LPDDR4_DMI1_A
DDR_A0_A → LPDDR4_A0_A
DDR_A1_A → LPDDR4_A1_A
DDR_A2_A → LPDDR4_A2_A
DDR_A3_A → LPDDR4_A3_A
DDR_A4_A → LPDDR4_A4_A
DDR_A5_A → LPDDR4_A5_A
DDR_CLKP_A → LPDDR4_CLKP_A
DDR_CLKN_A → LPDDR4_CLKN_A
DDR_DQ0_B → LPDDR4_DQ0_B
DDR_DQ1_B → LPDDR4_DQ1_B
DDR_DQ2_B → LPDDR4_DQ2_B
DDR_DQ3_B → LPDDR4_DQ3_B
DDR_DQ4_B → LPDDR4_DQ4_B
DDR_DQ5_B → LPDDR4_DQ5_B
DDR_DQ6_B → LPDDR4_DQ6_B
DDR_DQ7_B → LPDDR4_DQ7_B
DDR_DQS0P_B → LPDDR4_DQS0P_B
DDR_DQS0N_B → LPDDR4_DQS0N_B
DDR_DM0_B → LPDDR4_DMI0_B
DDR_DQ8_B → LPDDR4_DQ8_B
DDR_DQ9_B → LPDDR4_DQ9_B
DDR_DQ10_B → LPDDR4_DQ10_B
DDR_DQ11_B → LPDDR4_DQ11_B
DDR_DQ12_B → LPDDR4_DQ12_B
DDR_DQ13_B → LPDDR4_DQ13_B
DDR_DQ14_B → LPDDR4_DQ14_B
DDR_DQ15_B → LPDDR4_DQ15_B
DDR_DQS1P_B → LPDDR4_DQS1P_B
DDR_DQS1N_B → LPDDR4_DQS1N_B
DDR_DM1_B → LPDDR4_DMI1_B
DDR_A0_B → LPDDR4_A0_B
DDR_A1_B → LPDDR4_A1_B
DDR_A2_B → LPDDR4_A2_B
DDR_A3_B → LPDDR4_A3_B
DDR_A4_B → LPDDR4_A4_B
DDR_A5_B → LPDDR4_A5_B
DDR_CLKP_B → LPDDR4_CLKP_B
DDR_CLKN_B → LPDDR4_CLKN_B
LPDDR4_CKE0/LPDDR5_CS0_A → LPDDR4_CKE0_A
LPDDR4_CKE1/LPDDR5_CS1_A → LPDDR4_CKE1_A
LPDDR4_CKE0/LPDDR5_CS0_B → LPDDR4_CKE0_B
LPDDR4_CKE1/LPDDR5_CS1_B → LPDDR4_CKE1_B
DDR_RESET → LPDDR4_RESET
LPDDR4_CSN0_A → LPDDR4_CSN0_A
LPDDR4_CSN1_A → LPDDR4_CSN1_A
LPDDR4_CSN0_B → LPDDR4_CSN0_B
LPDDR4_CSN1_B → LPDDR4_CSN1_B

深圳和成荣科技有限公司
深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼

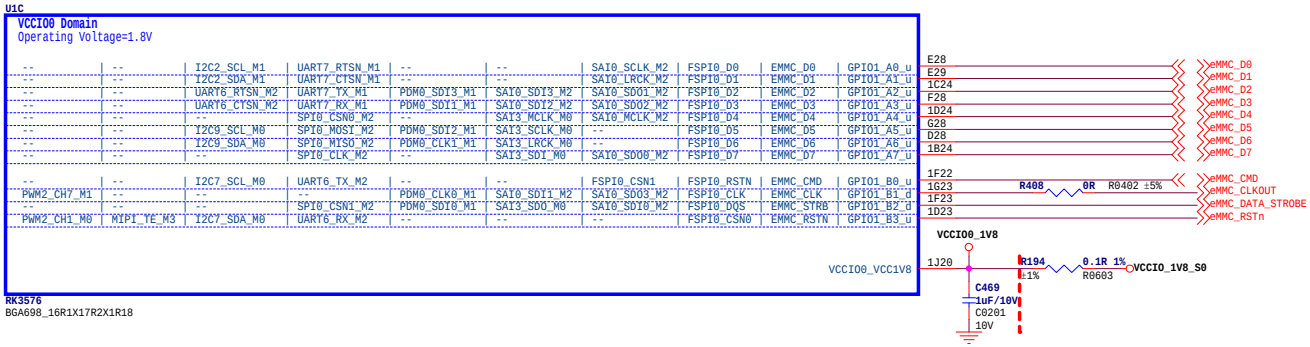
Title	K20_21		
Size A3	Page Name 07.RK3576-DDR PHY		Rev V0.1
Date: Wednesday, February 26, 2025	Sheet 7	of 30	

RK3576_B (UFS2.1)

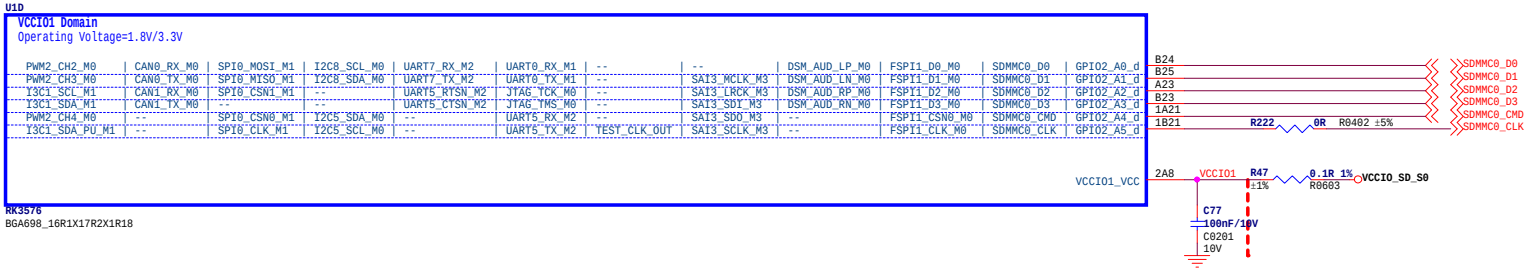


R35,R44,R45,R46 如果是使用EMMC则必须删除这两个器件

RK3576_C (VCCIO0)



RK3576_D (VCCIO1)



Note:
Caps of between dashed red lines and U1 should be placed under the U1 package. Other caps should be placed close to the U1 package

深圳和成永科技有限公司
深圳市宝安区福海街道新和社区福海大道创兴工业园二区1栋3楼

Title	K20_21		
Size A3	Page Name	08.RK3576-eMMC/UFS/SD	Rev V0.1
Date: Tuesday, March 04, 2025	Sheet 8 of 30		

RK3576_L (USB3/DP)

U1L

USB3 OTG0/DP1.4 Alt
USB:USB3.2 Gen1x1 OTG0
DP :RBR/HBR/HBR2/HBR3

--	DP_TX_AUXP
--	DP_TX_AUXN
USB3_OTG0_SSRX1P	DP_TX_D0P
USB3_OTG0_SSRX1N	DP_TX_D0N
USB3_OTG0_SSTX1P	DP_TX_D1P
USB3_OTG0_SSTX1N	DP_TX_D1N
USB3_OTG0_SSRX2P	DP_TX_D2P
USB3_OTG0_SSRX2N	DP_TX_D2N
USB3_OTG0_SSTX2P	DP_TX_D3P
USB3_OTG0_SSTX2N	DP_TX_D3N
USB3_OTG0_REXT	DP_TX_REXT
USB3_OTG0_DP_TX_AVDD0V85	
USB3_OTG0_DP_TX_DVDD0V85	
USB3_OTG0_DP_TX_AVDD1V8	

RK3576
BGA698_16R1X17R2X1R18

Support:
Type-C With Displayport Alternate Mode

2T2 2T3 DP_TX_AUXP DP_TX_AUXN
AK10 AL10 DP_TX_D0P DP_TX_D0N
AL11 AK11 DP_TX_D1P DP_TX_D1N
AK12 AL12 DP_TX_D2P DP_TX_D2N
AL13 AK13 DP_TX_D3P DP_TX_D3N

2T7 USB3_OTG0_DP_TX_REXT R48 8.2K 1% R0201 ±1%

2M5 2N5 USB3_OTG0/DP_TX_AVDD0V85 R49 ±1% 0.1R 1% R0603 VDDA_0V85_S0
C78 1uF/10V C0201 10V
C79 1uF/10V C0402 10V

2N4 USB3_OTG0/DP_TX_AVDD1V8 R50 ±1% 0.1R 1% R0603 VCCA_1V8_S0
C80 1uF/10V C0201 10V
C81 1uF/10V C0402 10V

Note:
Caps of between dashed red lines and U1 should be placed under the U1 package. Other caps should be placed close to the U1 package

RK3576_M (USB2)

U1M

USB2 OTG0
OTG/HOST/DEVICE
HS/FS/LS
Download Port

USB2_OTG0_DP	
USB2_OTG0_DM	
USB2_OTG0_ID	
USB2_OTG0_VBUSDET	
USB2_OTG0_REXT	

USB2 OTG1
OTG/HOST/DEVICE
HS/FS/LS

USB2_OTG1_DP	
USB2_OTG1_DM	
USB2_OTG1_ID	
USB2_OTG1_VBUSDET	
USB2_OTG1_REXT	
USB2_OTG_DVDD0V75	
USB2_OTG_AVDD1V8	
USB2_OTG_AVDD3V3	

RK3576
BGA698_16R1X17R2X1R18

40K 40K

AK9 AL9 USB2_OTG0_DP USB2_OTG0_DM

2R6 USB2_OTG0_ID TP3 TP_0R70

2P3 USB2_OTG0_VBUSDET
C82 100nF/10V C0201 10V

2R3 USB2_OTG0_REXT R51 200R 1% R0201 ±1%

2T4 2T5 USB2_HOST1_DP USB2_HOST1_DM

2T9 USB2_OTG1_ID TP4 TP_0R70

2T10 USB2_OTG1_VBUSDET
C83 NC/100nF C0201 10V
R52 ±5% NC/10K R0402
R55 NC/20K R0402 ±5%
VCC_3V3_S0
Option: For test

2U8 USB2_OTG1_REXT R53 200R 1% R0201 ±1%

2P5 USB2_OTG_DVDD0V75 R54 ±1% 0.1R 1% R0603 VDDA_0V75_S0
C84 100nF/10V C0201 10V

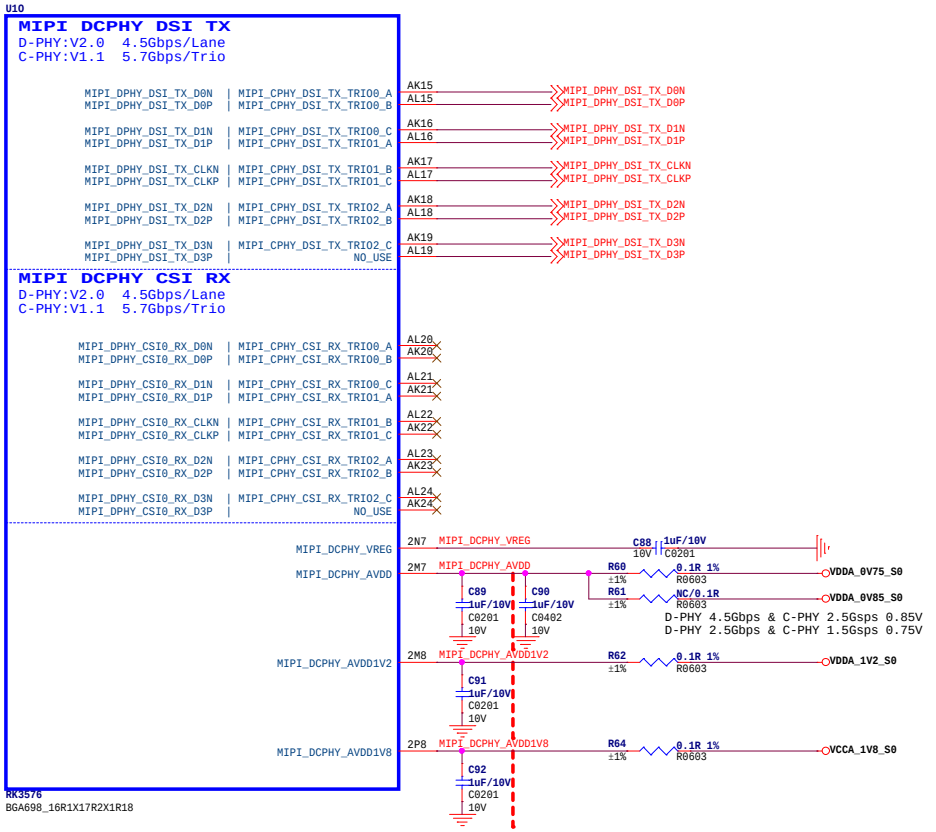
2P4 USB2_OTG_AVDD1V8 R56 ±1% 0.1R 1% R0603 VCCA_1V8_S0
C85 100nF/10V C0201 10V
C86 NC/1uF C0402 10V

2P7 USB2_OTG_AVDD3V3 R57 ±1% 0.1R 1% R0603 VCC_3V3_S0
C87 100nF/10V C0201 10V

深圳和成东科技有限公司
深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼

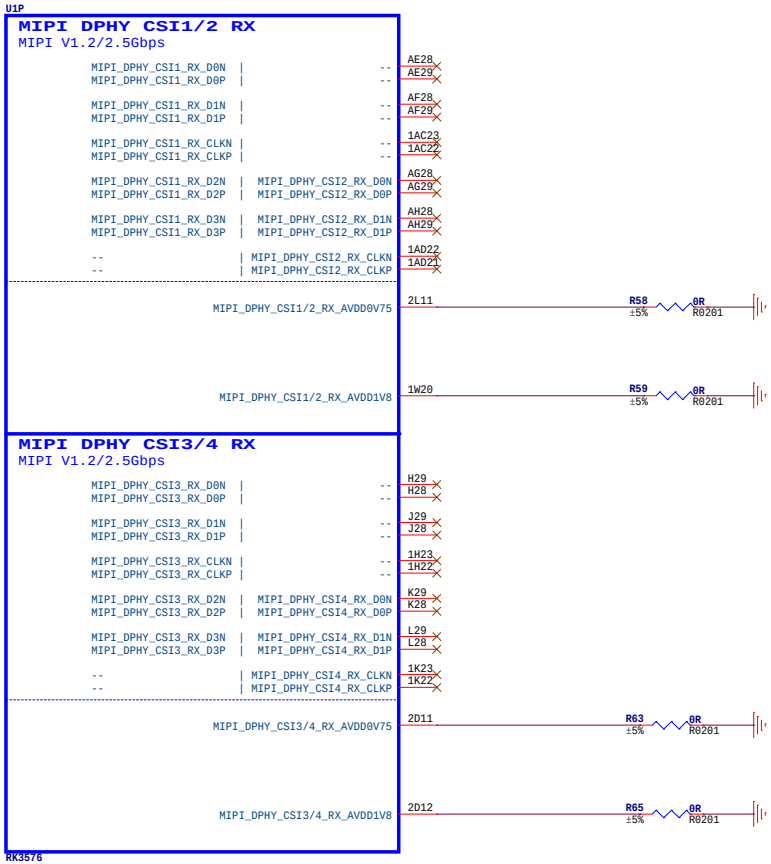
Title	K20_21	
Size A4	Page Name 09.RK3576-TypeC/USB	Rev V0.1
Date: Monday, March 03, 2025	Sheet 9 of 30	

RK3576_O(MIPI DCPHY)



Note:
Caps of between dashed red lines and U1 should be placed under the U1 package. Other caps should be placed close to the U1 package

RK3576_P(MIPI DPHY CSI RX)



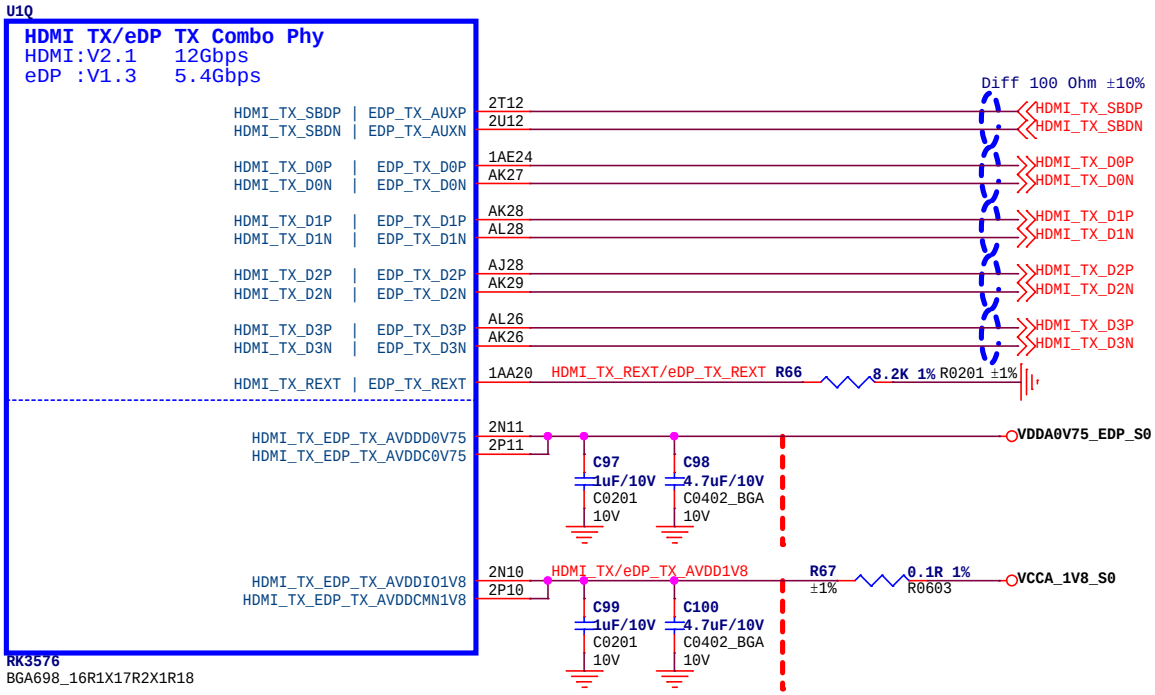
Note:
Caps of between dashed red lines and U1 should be placed under the U1 package. Other caps should be placed close to the U1 package

深圳和盛东科技有限公司
深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼

Title	K20_21	
Size A3	Page Name 10.RK3576-MIPI DSI/CSI	Rev V0.1
Date: Wednesday, February 26, 2025	Sheet 10 of 30	

RK3576_Q(HDMI/eDP)

Note:
HDMI 2.1 supports up to 4Kx2K@120Hz

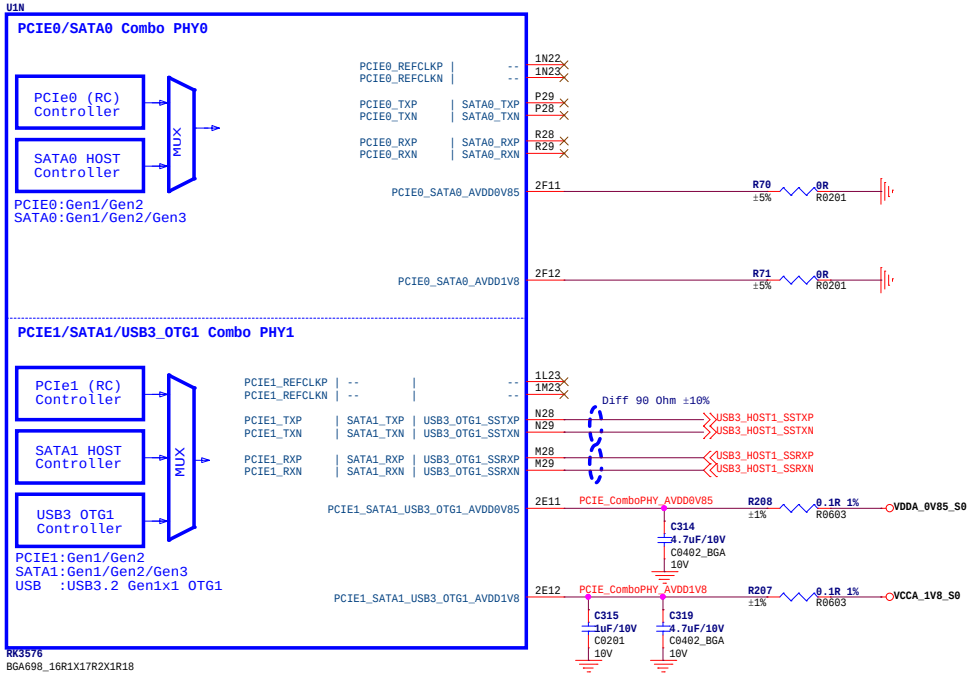


Note:
Caps of between dashed red lines and U1 should be placed under the U1 package. Other caps should be placed close to the U1 package

深圳和成东科技有限公司
深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼

Title	K20_21		
Size A4	Page Name	11.RK3576-HDMI/eDP	Rev V0.1
Date: Wednesday, February 26, 2025	Sheet 11 of 30		

RK3576_N(PCIe/SATA/USB3)



Note:
Caps of between dashed red lines and U1 should be placed under the U1 package. Other caps should be placed close to the U1 package

深圳和成系科技有限公司
深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼

Title	K20_21	
Size A3	Page Name 12.RK3576-PCIe/SATA/USB3	Rev V0.1
Date: Saturday, March 01, 2025	Sheet 12 of 30	

RK3576_F(VCCIO2)

U1F

VCCIO2 Domain

Operating Voltage=1.8V/3.3V

PWM2_CH5_M0	--	--	--	--	--	AUPLL_CLK_IN_M2	SAI4_MCLK_M0	SAI1_MCLK_M0	GPIO4_A2_d
PWM2_CH4_M1	PCIE1_WAKEN_M2	I2C2_SCL_M2	UART5_RTSN_M1	SPI3_CSN0_M2	FLEXBUS1_CSN_M4	--	--	SAI1_SCLK_M0	GPIO4_A3_d
CAN0_TX_M2	--	I2C4_SCL_M1	UART6_TX_M0	SPI3_MOSI_M2	FLEXBUS0_D13_M1	PDM1_SDI3_M1	SAI4_SCLK_M0	--	GPIO4_A4_d
--	PCIE1_CLKREQN_M2	I2C2_SDA_M2	UART5_CTSN_M1	SPI4_CSN1_M2	FLEXBUS1_D12_M1	--	--	SAI1_LRCK_M0	GPIO4_A5_d
CAN0_RX_M2	--	I2C4_SDA_M1	UART6_RX_M0	SPI3_MISO_M2	FLEXBUS0_D14_M1	PDM1_CLK0_M1	SAI4_LRCK_M0	--	GPIO4_A6_d
PWM2_CH6_M0	--	--	--	SPI3_CLK_M2	--	--	SAI4_SDI_M0	SAI1_SDO0_M0	GPIO4_A7_d
--	UART2_RTSN_M1	UART6_RTSN_M0	UART5_TX_M1	SPI4_CLK_M2	FLEXBUS1_D13_M1	PDM1_CLK1_M1	SAI1_SDI3_M0	SAI1_SDO1_M0	GPIO4_B0_d
--	UART2_CTSN_M1	UART6_CTSN_M0	UART5_RX_M1	SPI4_MOSI_M2	FLEXBUS1_D14_M1	PDM1_SDI2_M1	SAI1_SDI2_M0	SAI1_SDO2_M0	GPIO4_B1_d
--	--	MIPI_TE_M0	--	SPI4_MISO_M2	FLEXBUS1_D15_M1	PDM1_SDI1_M1	SAI1_SDI1_M0	SAI1_SDO3_M0	GPIO4_B2_d
PWM2_CH7_M0	--	--	SPI3_CSN1_M2	SPI4_CSN0_M2	--	PDM1_SDI0_M1	SAI4_SDO_M0	SAI1_SDI0_M0	GPIO4_B3_d
CAN1_RX_M2	PCIE0_WAKEN_M2	I2C3_SDA_M0	UART2_RX_M1	--	FLEXBUS0_CSN_M4	--	--	SPDIF_RX0_M0	GPIO4_B4_d
CAN1_TX_M2	PCIE0_CLKREQN_M2	I2C3_SCL_M0	UART2_TX_M1	--	FLEXBUS0_D15_M1	--	--	SPDIF_TX0_M0	GPIO4_B5_d

RK3576

BGA698_16R1X17R2X1R18

1D6 SAI1_MCLK_M0
1C6 SAI1_SCLK_M0
1C5
1B6 SAI1_LRCK_M0
1B5
A7 SAI1_SDO0_M0
1A5
B7
B6
1A6
B8
1A4 I2C3_SDA_M0_Audio / I2C3_SCL_M0_Audio

VCCIO2

VCCIO2_VCC 2A2 — R72 ±1% 0.1R 1% R0603 — VCCIO_AUDIO

C103 100nF/10V C0201 10V

VCCIO2

R416 2.2K R0402 ±5%
R417 2.2K R0402 ±5%

I2C3_SDA_M0_Audio
I2C3_SCL_M0_Audio

RK3576_G(VCCIO3)

U1G

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH0_M1	PCIE1_CLKREQN_M1	SPI1_CLK_M0	I2C9_SDA_M1	--	--	--	SAI3_SCLK_M1	--	SDMMC1_D0_M0	ETH1_RXD2_M1	GPIO1_B4_d
PWM1_CH1_M1	PCIE1_WAKEN_M1	SPI1_MOSI_M0	I2C9_SCL_M1	--	--	--	SAI3_LRCK_M1	--	SDMMC1_D1_M0	ETH1_RXD3_M1	GPIO1_B5_d
--	PCIE0_CLKREQN_M1	SPI1_MISO_M0	--	UART3_CTSN_M2	--	--	SAI3_SDO_M1	--	SDMMC1_D2_M0	ETH1_RXCLK_M1	GPIO1_B6_d
--	PCIE0_WAKEN_M1	SPI1_CSN0_M0	--	UART3_RTSN_M2	--	--	SAI3_SDI_M1	--	SDMMC1_D3_M0	ETH1_TXD2_M1	GPIO1_B7_d
PWM0_CH0_M1	--	SPI1_CSN1_M0	--	UART3_TX_M2	--	PDM0_SDI2_M2	--	--	SDMMC1_CMD_M0	ETH1_TXD3_M1	GPIO1_C0_d
--	--	--	--	UART3_RX_M2	--	PDM0_CLK0_M2	SAI3_MCLK_M1	--	SDMMC1_CLK_M0	ETH1_TXCLK_M1	GPIO1_C1_d
PWM1_CH2_M1	--	SPI2_CSN1_M1	I2C6_SCL_M1	UART4_RTSN_M1	--	--	FSPI1_CSN1_M1	FSPI1_RSTN_M1	SDMMC1_PWREN_M0	ETH1_PPSCLK_M1	GPIO1_C2_u
--	--	SPI2_CSN0_M1	I2C6_SDA_M1	UART4_CTSN_M1	--	--	--	FSPI1_CSN0_M1	SDMMC1_DETN_M0	ETH1_PPSTRIG_M1	GPIO1_C3_u
--	PCIE0_BUTTONRSTN	SPI2_MOSI_M1	UART2_RTSN_M0	UART4_TX_M1	--	--	--	FSPI1_D0_M1	--	ETH1_TXD0_M1	GPIO1_C4_d
--	PCIE1_BUTTONRSTN	SPI2_MISO_M1	UART2_CTSN_M0	UART4_RX_M1	--	--	--	FSPI1_D1_M1	--	ETH1_TXD1_M1	GPIO1_C5_d
--	SATA_CPPOD	--	I2C8_SCL_M1	UART2_TX_M0	--	PDM0_SDI0_M2	--	FSPI1_D2_M1	--	ETH1_TXCTL_M1	GPIO1_C6_d
--	SATA_CPDET	--	I2C8_SDA_M1	UART2_RX_M0	--	PDM0_SDI1_M2	--	FSPI1_D3_M1	--	ETH1_RXD0_M1	GPIO1_C7_d
--	--	--	--	UART10_TX_M1	--	--	SAI2_SDO_M0	FSPI1_D4_M1	--	ETH1_RXD1_M1	GPIO1_D0_d
--	--	--	I3C0_SDA_PU_M1	UART10_RX_M1	--	--	SAI2_SCLK_M0	FSPI1_D5_M1	--	ETH1_RXCTL_M1	GPIO1_D1_d
PWM1_CH3_M1	--	--	I3C0_SCL_M1	--	--	--	SAI2_LRCK_M0	FSPI1_D6_M1	--	ETH1_MDC_M1	GPIO1_D2_d
PWM1_CH4_M1	--	--	I3C0_SDA_M1	--	--	--	SAI2_SDI_M0	FSPI1_D7_M1	--	ETH1_MDIO_M1	GPIO1_D3_d
--	--	--	I2C5_SCL_M1	UART10_RTSN_M1	SPDIF_RX1_M2	PDM0_SDI3_M2	SAI2_MCLK_M0	FSPI1_DQS_M1	--	ETH1_MCLK_M1	GPIO1_D4_d
CLK1_32K_OUT	SATA_MPSW1T	SPI2_CLK_M1	I2C5_SDA_M1	UART10_CTSN_M1	SPDIF_TX1_M2	PDM0_CLK1_M2	--	FSPI1_CLK_M1	--	ETH_CLK1_25M_OUT_M1	GPIO1_D5_d

RK3576

BGA698_16R1X17R2X1R18

A28 SDMMC1_D0_M0
B27 SDMMC1_D1_M0
1A23 SDMMC1_D2_M0
A27 SDMMC1_D3_M0
B26 SDMMC1_CMD_M0
1B22 R415 0R R0402 ±5% SDMMC1_CLK_M0
B29 UART4_RTSN_M1
1C23 UART4_CTSN_M1
1B23 UART4_TX_M1
B28 UART4_RX_M1
A26 WIFI_REG_ON_H
1C22 BT_REG_ON_H
C29
1D22
1A24
C28
1E21 HOST_WAKE_BT_H
1E22

For BT

VCCIO3

VCCIO3_VCC 2B10 — R73 ±1% 0.1R 1% R0603 — VCCIO_WL

C104 100nF/10V C0201 10V

Note:
Caps of between dashed red lines and U1 should be placed under the U1 package. Other caps should be placed close to the U1 package

RK3576_J(VCCIO6)

U1J

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH5_M1	UART11_TX_M2	SPI4_CSN1_M0	I2C7_SCL_M3	PCIE1_WAKEN_M3	HDMI_TX_CEC_M0	--	SAI4_MCLK_M2	DSM_AUD_LP_M1	GPIO4_C0_d
PWM0_CH1_M1	UART11_RX_M2	EDP_TX_HPDIN_M0	I2C7_SDA_M3	PCIE1_CLKREQN_M3	HDMI_TX_HPDIN_M0	--	--	DSM_AUD_LN_M1	GPIO4_C1_d
PWM2_CH0_M1	UART9_TX_M2	CAN0_TX_M1	I2C2_SCL_M3	--	HDMI_TX_SCL	--	--	DSM_AUD_RP_M1	GPIO4_C2_d
PWM2_CH1_M1	UART9_RX_M2	CAN0_RX_M1	I2C2_SDA_M3	--	HDMI_TX_SDA	--	--	DSM_AUD_RN_M1	GPIO4_C3_d
PWM2_CH6_M1	UART8_TX_M3	SPI4_CSN0_M0	I2C3_SCL_M3	DP_HPDIN_M0	--	--	SAI4_LRCK_M2	ISP_PRELIGHT_TRIG_M1	GPIO4_C4_d
PWM2_CH5_M1	UART8_RX_M3	SPI4_MOSI_M0	I2C3_SDA_M3	SATA1_ACTLED_M1	PCIE0_WAKEN_M3	VP0_SYNC_OUT	SAI4_SDO_M2	ISP_FLASH_TRIGOUT_M1	GPIO4_C5_d
PWM2_CH2_M1	CAN1_TX_M1	SPI4_MISO_M0	I2C6_SCL_M3	SATA0_ACTLED_M1	PCIE0_CLKREQN_M3	VP1_SYNC_OUT	SAI4_SDI_M2	--	GPIO4_C6_d
PWM2_CH3_M1	CAN1_RX_M1	SPI4_CLK_M0	I2C6_SDA_M3	--	--	VP2_SYNC_OUT	SAI4_SCLK_M2	--	GPIO4_C7_d

RK3576

BGA698_16R1X17R2X1R18

AK3 HDMI_TX_CEC_M0
AK2 HDMI_TX_HPDIN_M0
AL2 HDMI_TX_SCL
1AE2 HDMI_TX_SDA
AL3 DP_HPDIN
AK1 DP_PWREN
1AE1 I2C6_SCL_M3_TP
AJ1 I2C6_SDA_M3_TP

VCCIO6

VCCIO6_VCC 2N3 — R74 ±1% 0.1R 1% R0603 — VCC_3V3_S3

C105 100nF/10V C0201 10V

VCCIO6

R75 2.2K R0402 ±5%
R76 2.2K R0402 ±5%

I2C6_SCL_M3_TP
I2C6_SDA_M3_TP

深圳和成东科技有限公司

深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼

Title	K20_21		
Size A3	Page Name	13.RK3576-GPIO VCCIO2/3/6	Rev V0.1
Date: Wednesday, February 26, 2025	Sheet 13 of 30		

RK3576_H(VCCIO4)

U1H

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

--	--	I2C4_SCL_M2	SPI4_CSN1_M3	UART8_TX_M1	--	SAI0_SDO0_M0	ETH0_RXD0_M1	SDMMC1_D0_M1	VI_CIF_D15	GPIO2_A6_d
--	--	I2C4_SDA_M2	--	UART8_RX_M1	--	SAI0_SDO1_M0	ETH0_TXCTL_M1	SDMMC1_D1_M1	VI_CIF_D14	GPIO2_A7_d
--	--	--	--	UART1_TX_M1	PDM0_SDI3_M3	SAI0_SDI0_M0	ETH0_TXD1_M1	SDMMC1_D2_M1	VI_CIF_D13	GPIO2_B0_d
--	--	--	--	UART1_RX_M1	PDM0_SDI2_M3	SAI0_SDI1_M0	ETH0_TXD0_M1	SDMMC1_D3_M1	VI_CIF_D12	GPIO2_B1_d
--	--	PCIE0_CLKREQN_M0	SPI4_CSN0_M3	UART1_CTSN_M1	PDM0_SDI1_M3	SAI0_SDI2_M0	ETH0_TXD3_M1	SDMMC1_CMD_M1	VI_CIF_D11	GPIO2_B2_d
--	--	PCIE1_CLKREQN_M0	SPI4_CLK_M3	UART1_RTSN_M1	PDM0_CLK1_M3	SAI0_SDO2_M0	ETH0_TXCLK_M1	SDMMC1_CLK_M1	VI_CIF_D10	GPIO2_B3_d
--	SATA0_ACTLED_M0	--	SPI4_MOSI_M3	UART7_CTSN_M0	PDM0_SDI0_M3	SAI0_SDI3_M0	ETH0_TXD2_M1	SDMMC1_PWREN_M1	VI_CIF_D9	GPIO2_B4_d
--	SATA1_ACTLED_M0	--	SPI4_MISO_M3	UART7_RTSN_M0	PDM0_CLK0_M3	SAI0_MCLK_M0	ETH0_RXCLK_M1	SDMMC1_DETN_M1	VI_CIF_D8	GPIO2_B5_d
--	--	I2C8_SCL_M2	UART8_RTSN_M1	UART7_TX_M0	--	SAI0_SCLK_M0	ETH0_RXD3_M1	ETH1_PTP_REFCLK_M1	VI_CIF_D7	GPIO2_B6_d
--	--	I2C8_SDA_M2	UART8_CTSN_M1	UART7_RX_M0	--	SAI0_LRCK_M0	ETH0_RXD2_M1	--	VI_CIF_D6	GPIO2_B7_d
PWM1_CH0_M2	--	--	--	UART9_RX_M0	PDM1_SDI1_M0	--	ETH0_PTP_REFCLK_M1	ETH1_RXD2_M0	VI_CIF_D5	GPIO2_C0_d
PWM1_CH1_M2	--	--	SPI1_CSN1_M1	UART9_TX_M0	PDM1_CLK1_M0	SAI2_MCLK_M1	ETH0_PPSCLK_M1	ETH1_RXD3_M0	VI_CIF_D4	GPIO2_C1_d
PWM1_CH2_M2	--	--	SPI1_MOSI_M1	UART11_CTSN_M1	PDM1_SDI2_M0	SAI2_SCLK_M1	ETH0_PPSTRIG_M1	ETH1_RXCLK_M0	VI_CIF_D3	GPIO2_C2_d
PWM0_CH0_M2	--	--	SPI1_MISO_M1	UART11_RTSN_M1	PDM1_SDI3_M0	SAI2_LRCK_M1	--	ETH1_TXD2_M0	VI_CIF_D2	GPIO2_C3_d
PWM1_CH3_M2	--	--	SPI1_CSN0_M1	UART11_TX_M1	PDM1_SDI0_M0	SAI2_SDO_M1	--	ETH1_TXD3_M0	VI_CIF_D1	GPIO2_C4_d
PWM1_CH4_M2	--	--	SPI1_CLK_M1	UART11_RX_M1	PDM1_CLK0_M0	SAI2_SDI_M1	--	ETH1_TXCLK_M0	VI_CIF_D0	GPIO2_C5_d
PWM1_CH5_M2	--	I2C5_SCL_M2	--	UART4_CTSN_M0	--	SAI4_SCLK_M3	--	ETH1_TXD0_M0	--	GPIO2_C6_d
PWM0_CH1_M2	--	I2C5_SDA_M2	--	UART4_RTSN_M0	--	SAI4_LRCK_M3	--	ETH1_TXD1_M0	--	GPIO2_C7_d
PWM2_CH0_M2	--	I2C6_SCL_M2	--	UART4_TX_M0	--	SAI4_SDI_M3	--	ETH1_TXCTL_M0	--	GPIO2_D0_d
PWM2_CH1_M2	--	I2C6_SDA_M2	--	UART4_RX_M0	--	SAI4_SDO_M3	--	ETH1_RXD0_M0	--	GPIO2_D1_d
PWM2_CH2_M2	I3C1_SCL_M0	--	--	UART6_TX_M1	--	SAI4_MCLK_M3	--	ETH1_RXD1_M0	CAM_CLK0_OUT_M1	GPIO2_D2_d
PWM2_CH3_M2	I3C1_SDA_M0	--	--	UART6_RX_M1	--	--	--	ETH1_RXCTL_M0	--	GPIO2_D3_d
PWM2_CH4_M2	--	I2C9_SDA_M2	--	UART6_RTSN_M1	--	--	--	ETH1_MDC_M0	ISP_PRELIGHT_TRIG_M0	GPIO2_D4_d
PWM2_CH5_M2	--	I2C9_SCL_M2	--	UART6_CTSN_M1	--	--	--	ETH1_MDIO_M0	ISP_FLASH_TRIGOUT_M0	GPIO2_D5_d
PWM2_CH6_M2	I3C1_SDA_PU_M0	--	--	UART9_RTSN_M0	SPDIF_RX0_M2	SAI3_MCLK_M2	ETH0_MCLK_M1	ETH_CLK1_25M_OUT_M0	CAM_CLK1_OUT_M1	GPIO2_D6_d
PWM2_CH7_M2	--	--	SPI3_CSN1_M0	UART9_CTSN_M0	SPDIF_TX0_M2	SAI0_SDO3_M0	ETH_CLK0_25M_OUT_M1	ETH1_MCLK_M0	CAM_CLK2_OUT_M1	GPIO2_D7_d
--	--	I2C7_SCL_M1	SPI3_CLK_M0	UART3_TX_M0	--	SAI3_SCLK_M2	ETH0_MDIO_M1	--	VI_CIF_HREF	GPIO3_A0_d
--	--	I2C7_SDA_M1	SPI3_MOSI_M0	UART3_RX_M0	--	SAI3_LRCK_M2	ETH0_MDC_M1	ETH1_PPSTRIG_M0	VI_CIF_VSYNC	GPIO3_A1_d
--	MIPI_TE_M1	CAN1_TX_M3	SPI3_MISO_M0	UART3_CTSN_M0	SPDIF_RX1_M1	SAI3_SDO_M2	ETH0_RXCTL_M1	ETH1_PPSCLK_M0	VI_CIF_CLKO	GPIO3_A2_d
--	--	CAN1_RX_M3	SPI3_CSN0_M0	UART3_RTSN_M0	SPDIF_TX1_M1	SAI3_SDI_M2	ETH0_RXD1_M1	ETH1_PTP_REFCLK_M0	VI_CIF_CLKI	GPIO3_A3_d

VCCIO4_VCC

RK3576

BGA698_16R1X17R2X1R18

B22 — DIAL_SWITCH_GPIO2_A6
B20 — DIAL_SWITCH_GPIO2_A7
B19 — HDMI_TX_ON_H
1A18 — SPK_CTL_L
1A17 — NFC_IRQ
1B16 — NFC_VEN
A19 — NFC_CHECK
1C18 — GMAC0_RSTn
A21 — DIAL_SWITCH_GPIO2_B6
B21 — DIAL_SWITCH_GPIO2_B7
A17 — NFC_DWL
1A15, 1D15, A15, 1A13, 1C15, 1A14, B15, B16, 1A16, B17, B18, 1B13, 1B15, 1D18, 1E15, 1D16, 1B18, 1A20, 1A19 — NC

VCCIO4
2A7
C106 NC/100nF C0201 10V
C107 1uF/10V C0201 10V
R85 ±1% 0.1R 1% R0603 — VCC_3V3_S0
R86 ±1% NC/0.1R R0603 — VCCIO_1V8_S0

RK3576_I(VCCIO5)

U1I

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM1_CH0_M3	--	SPI2_CLK_M2	UART1_CTSN_M2	FLEXBUS0_CSN_M0	--	FLEXBUS1_D11	DSMC_RDYN	SAI4_SDI_M1	ETH_CLK0_25M_OUT_M0	VO_EBC_SDSHR	VO_LCDC_D23	GPIO3_A4_d
PWM1_CH1_M3	--	SPI2_CSN1_M2	UART1_RTSN_M2	--	--	FLEXBUS0_D7	DSMC_DATA15	PDM1_SDI3_M2	ETH0_MDIO_M0	VO_EBC_GDSP	VO_LCDC_D22	GPIO3_A5_d
PWM1_CH2_M3	--	UART10_CTSN_M0	UART1_RX_M2	--	--	FLEXBUS0_D6	DSMC_DATA14	PDM1_SDI2_M2	ETH0_MDC_M0	VO_EBC_GDOE	VO_LCDC_D21	GPIO3_A6_d
--	--	UART10_RTSN_M0	UART1_TX_M2	--	--	FLEXBUS0_D5	DSMC_DATA13	PDM1_CLK1_M2	ETH0_RXCTL_M0	VO_EBC_VCOM	VO_LCDC_D20	GPIO3_A7_d
PWM0_CH0_M3	--	SPI2_MOSI_M2	UART10_RX_M0	--	--	FLEXBUS0_D8	DSMC_CSN1	SAI4_MCLK_M1	ETH0_MCLK_M0	VO_EBC_SDCE3	VO_LCDC_D19	GPIO3_B0_d
PWM1_CH3_M3	--	SPI4_CSN0_M1	UART10_TX_M0	--	--	FLEXBUS0_D4	DSMC_DATA12	PDM1_CLK0_M2	ETH0_RXD1_M0	VO_EBC_SDCE2	VO_LCDC_D18	GPIO3_B1_d
--	I2C8_SDA_M3	--	UART9_RX_M1	--	--	FLEXBUS0_D3	DSMC_DATA11	PDM1_SDI1_M2	ETH0_RXD0_M0	VO_EBC_SDCE1	VO_LCDC_D17	GPIO3_B2_d
--	I2C8_SCL_M3	--	UART9_TX_M1	--	--	FLEXBUS0_D2	DSMC_DATA10	PDM1_SDI0_M2	ETH0_TXCTL_M0	VO_EBC_SDCE0	VO_LCDC_D16	GPIO3_B3_d
PWM1_CH4_M3	--	--	UART9_RTSN_M1	--	--	FLEXBUS0_D1	DSMC_DATA9	SPDIF_RX1_M0	ETH0_TXD1_M0	VO_EBC_SDDO15	VO_LCDC_D15	GPIO3_B4_d
PWM1_CH5_M3	--	--	UART9_CTSN_M1	--	--	FLEXBUS0_D0	DSMC_DATA8	SPDIF_TX1_M0	ETH0_TXD0_M0	VO_EBC_SDDO14	VO_LCDC_D14	GPIO3_B5_d
PWM0_CH1_M3	--	SPI3_CSN0_M1	--	--	--	FLEXBUS0_CLK	DSMC_DQS1	--	ETH0_TXCLK_M0	VO_EBC_SDDO13	VO_LCDC_D13	GPIO3_B6_d
--	I2C4_SDA_M3	UART3_CTSN_M1	UART2_RX_M2	FLEXBUS1_CSN_M0	--	FLEXBUS1_D10	DSMC_DQS0	SAI1_SDI0_M1	ETH0_PPSTRIG_M0	VO_EBC_SDDO12	VO_LCDC_D12	GPIO3_B7_d
--	I2C4_SCL_M3	UART3_RTSN_M1	UART2_TX_M2	--	--	FLEXBUS1_D9	DSMC_DATA7	SAI1_SDO3_M1	ETH0_PPSCLK_M0	VO_EBC_SDDO11	VO_LCDC_D11	GPIO3_C0_d
CAN0_RX_M3	I2C5_SDA_M3	SPI2_MISO_M2	UART11_RX_M0	--	--	FLEXBUS1_D8	DSMC_DATA6	SAI1_SDO2_M1	ETH0_PTP_REFCLK_M0	VO_EBC_SDDO10	VO_LCDC_D10	GPIO3_C1_d
PWM2_CH0_M3	I2C9_SCL_M3	SPI4_MISO_M1	UART11_RTSN_M0	--	--	FLEXBUS1_D9	DSMC_INT1	SAI2_SCLK_M2	ETH0_TXD3_M0	VO_EBC_SDDO9	VO_LCDC_D9	GPIO3_C2_d
PWM2_CH1_M3	I2C9_SDA_M3	SPI4_MOSI_M1	UART11_CTSN_M0	FLEXBUS0_CSN_M2	--	FLEXBUS0_D10	DSMC_INT3	SAI2_LRCK_M2	ETH0_TXD2_M0	VO_EBC_SDDO8	VO_LCDC_D8	GPIO3_C3_d
CAN0_TX_M3	I2C5_SCL_M3	SPI2_CSN0_M2	UART11_TX_M0	--	--	FLEXBUS1_D7	DSMC_DATA5	SAI1_SDO1_M1	--	VO_EBC_SDDO7	VO_LCDC_D7	GPIO3_C4_d
PWM2_CH2_M3	--	SPI1_MISO_M2	UART8_RX_M0	--	--	FLEXBUS1_D6	DSMC_DATA4	SAI1_SDO0_M1	--	VO_EBC_SDDO6	VO_LCDC_D6	GPIO3_C5_d
--	--	SPI1_MOSI_M2	UART8_TX_M0	--	--	FLEXBUS1_D5	DSMC_DATA3	SAI1_LRCK_M1	--	VO_EBC_SDDO5	VO_LCDC_D5	GPIO3_C6_d
--	--	SPI1_CLK_M2	UART8_RTSN_M0	--	--	FLEXBUS1_D4	DSMC_DATA2	SAI1_SCLK_M1	--	VO_EBC_SDDO4	VO_LCDC_D4	GPIO3_C7_d
PWM2_CH3_M3	--	SPI1_CSN0_M2	UART8_CTSN_M0	--	--	FLEXBUS1_D3	DSMC_DATA1	SAI1_MCLK_M1	--	VO_EBC_SDDO3	VO_LCDC_D3	GPIO3_D0_d
--	I3C1_SDA_PU_M2	SPI4_CLK_M1	--	FLEXBUS1_CSN_M2	--	FLEXBUS0_D11	DSMC_CSN2	SAI2_MCLK_M2	ETH0_RXCLK_M0	VO_EBC_SDDO2	VO_LCDC_D2	GPIO3_D1_d
PWM2_CH4_M3	I3C1_SDA_M2	SPI4_CSN1_M1	UART2_RTSN_M2	FLEXBUS0_CSN_M3	FLEXBUS1_D15_M0	FLEXBUS0_D12	DSMC_CSN3	SAI2_SDI_M2	ETH0_RXD3_M0	VO_EBC_SDDO1	VO_LCDC_D1	GPIO3_D2_d
PWM2_CH5_M3	I3C1_SCL_M2	--	UART2_CTSN_M2	--	--	FLEXBUS1_D2	DSMC_CSN0	SAI2_SDO_M2	ETH0_RXD2_M0	VO_EBC_SDDO0	VO_LCDC_D0	GPIO3_D3_d
--	I2C3_SCL_M2	SPI3_CLK_M1	UART5_RX_M0	--	--	FLEXBUS1_D1	DSMC_DATA0	SAI1_SDI1_M1	--	VO_EBC_SDLE	VO_LCDC_DEN	GPIO3_D4_d
--	I2C3_SDA_M2	SPI3_MISO_M1	UART5_TX_M0	--	--	FLEXBUS1_D0	DSMC_CLKP	SAI1_SDI2_M1	--	VO_EBC_GDCLK	VO_LCDC_HSYNC	GPIO3_D5_d
PWM2_CH6_M3	--	SPI3_MOSI_M1	UART5_CTSN_M0	--	--	FLEXBUS1_CLK	DSMC_CLKN	SAI1_SDI3_M1	--	VO_EBC_SDCLK	VO_LCDC_VSYNC	GPIO3_D6_d
PWM2_CH7_M3	--	SPI3_CSN1_M1	UART5_RTSN_M0	FLEXBUS1_CSN_M1	FLEXBUS1_D12_M0	FLEXBUS0_D15_M0	DSMC_RESETN	SAI4_SCLK_M1	CAM_CLK0_OUT_M0	VO_EBC_SDOE	VO_LCDC_CLK	GPIO3_D7_d
MIPI_TE_M2	I2C7_SCL_M2	SPI1_CSN1_M2	UART3_TX_M1	FLEXBUS1_CSN_M3	FLEXBUS1_D14_M0	FLEXBUS0_D13_M0	DSMC_INT0	SAI4_LRCK_M1	CAM_CLK1_OUT_M0	SPDIF_RX0_M1	--	GPIO4_A0_d
--	I2C7_SDA_M2	--	UART3_RX_M1	FLEXBUS0_CSN_M1	FLEXBUS1_D13_M0	FLEXBUS0_D14_M0	DSMC_INT2	SAI4_SDO_M1	CAM_CLK2_OUT_M0	SPDIF_TX0_M1	VO_POST_EMPTY	GPIO4_A1_d

VCCIO5_VCC_0
VCCIO5_VCC_1

RK3576

BGA698_16R1X17R2X1R18

1D13 — ETH_CLK0_25M_OUT_M0
A9 — GMAC0_MDIO_M0
1A7 — GMAC0_MDC_M0
B13 — GMAC0_RXCTL_M0
B14 — GMAC0_RXD1_M0
1A11 — GMAC0_RXD0_M0
A13 — GMAC0_TXCTL_M0
A11 — GMAC0_TXD1_M0
B10 — GMAC0_TXD0_M0
1A9 — GMAC0_TXCLK_M0
B11
1D12
1E9
1B10
B9 — GMAC0_TXD3_M0
1A8 — GMAC0_TXD2_M0
1D9 — HUB_RST
1B9 — IRLED1_EN
1D7 — IRLED2_EN
1C7 — PWRON_LED_EN
1C12 — GMAC0_RXCLK_M0
1A12 — GMAC0_RXD3_M0
1A10 — GMAC0_RXD2_M0
B12
1E12
1D10
1C10
1E7
1B12
1B7

FB17 120R FB0402
R88 22R R0402 ±5%
R89 22R R0402 ±5%
R90 22R R0402 ±5%
R91 22R R0402 ±5%
R92 0R R0402 ±5%
R93 22R R0402 ±5%
R94 22R R0402 ±5%

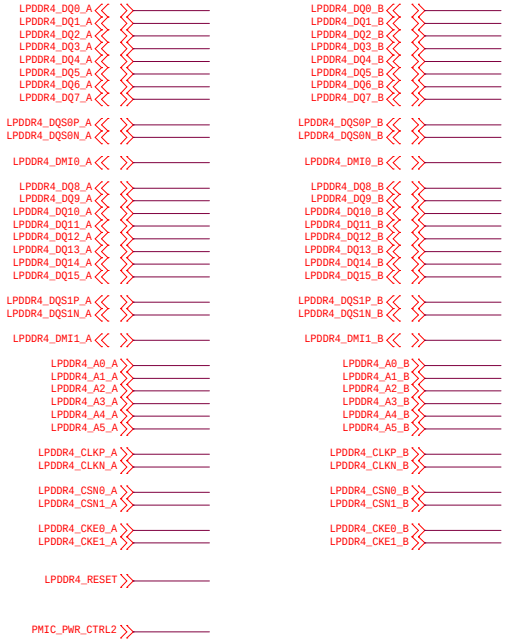
VCCIO5
2A4
2A5
C108 NC/100nF C0201 10V
C109 1uF/10V C0201 10V
R95 ±1% 0.1R 1% R0603 — VCC_3V3_S0
R96 ±1% NC/0.1R R0603 — VCCIO_1V8_S0

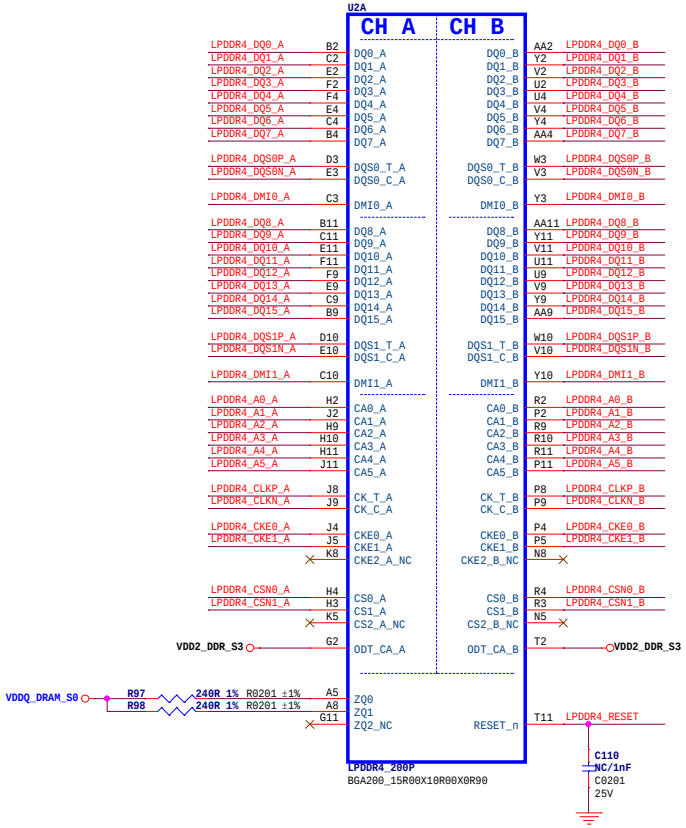
Note:
Caps of between dashed red lines and U1 should be placed under the U1 package. Other caps should be placed close to the U1 package

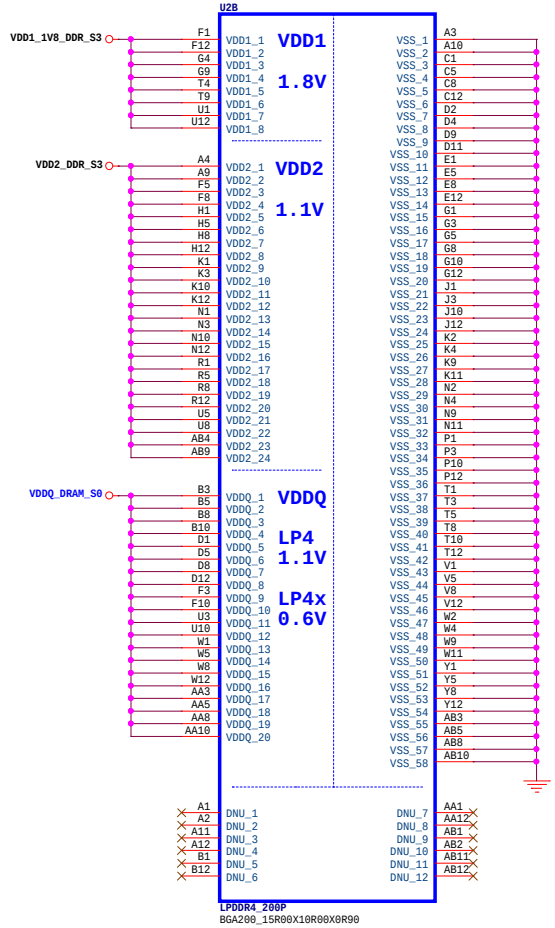
深圳和成永科技有限公司
深圳市宝安区福海街道新和社区福海大道创兴工业园二区1栋3楼

Title	K20_21		
Size A3	Page Name	14.RK3576-GPIO VCCIO4/5	Rev V0.1
Date: Friday, February 28, 2025	Sheet 14 of 30		

LPDDR4/4X







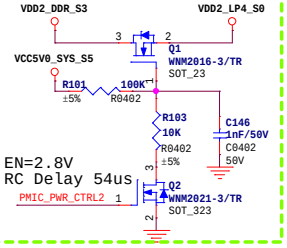
Note:

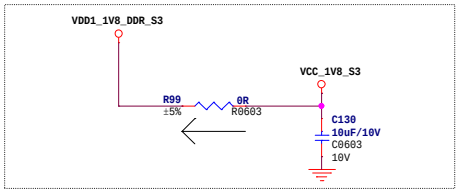
Sequence:VDD1-VDD2-VDDQ

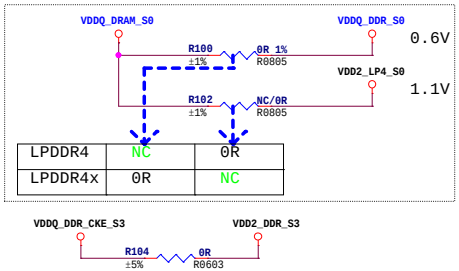
	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65

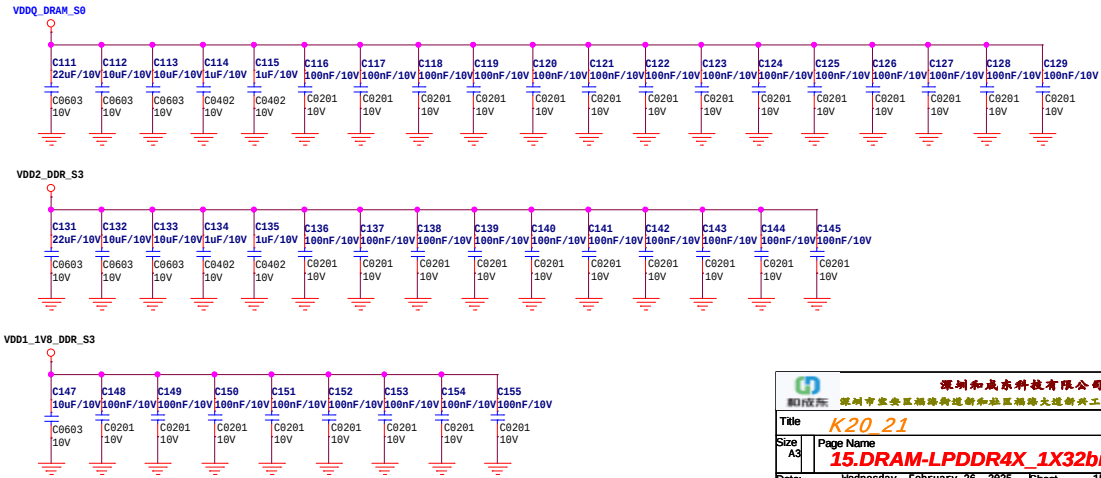
Option

Power down VDDQ during standby for LPDDR4







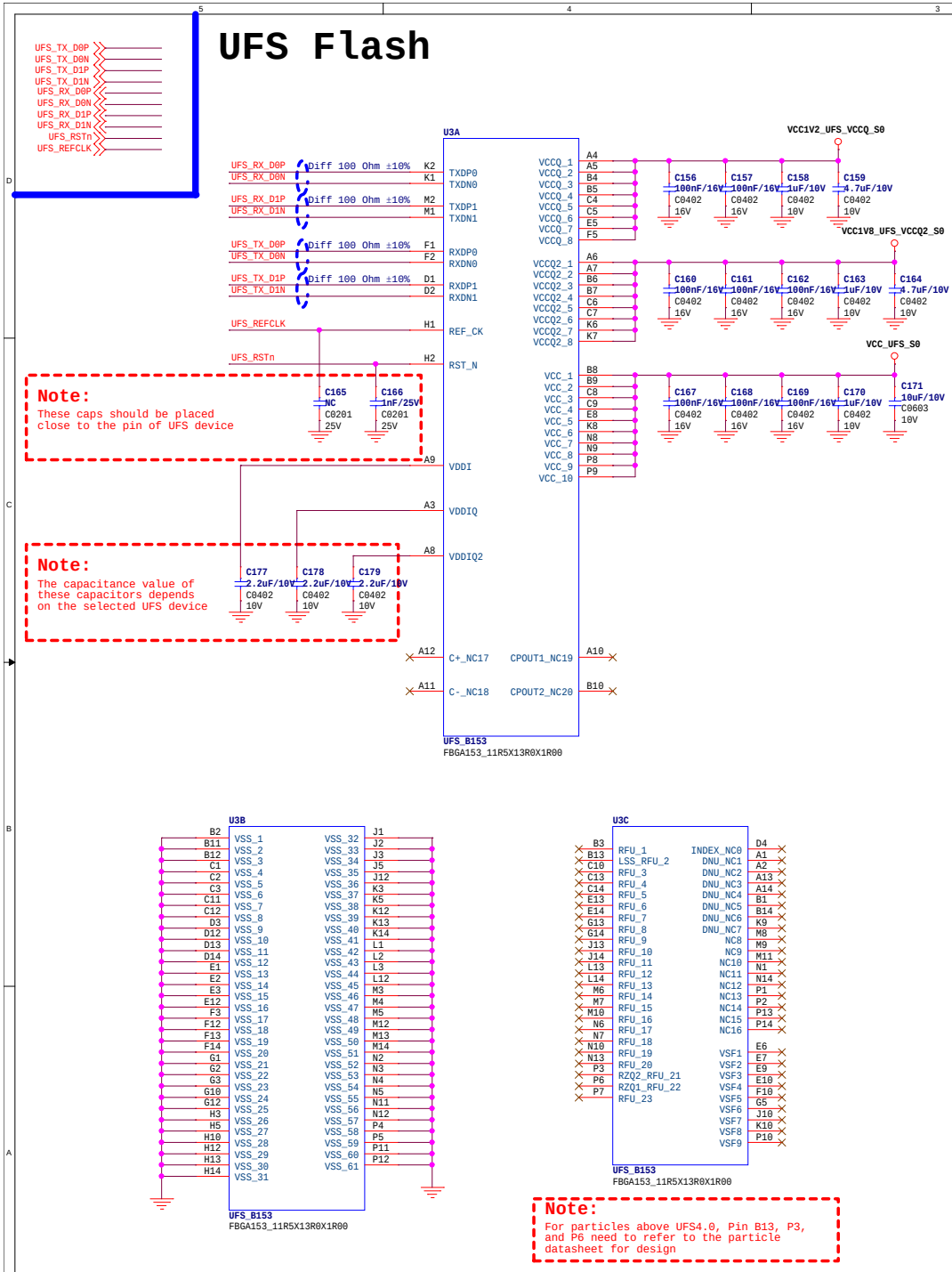


深圳和威东科技有限公司

深圳市宝安区福海街道和平社区福海大道创兴工业园二区1栋3楼

Title	K20_21		
Size A3	Page Name	15.DRAM-LPDDR4X_1X32bit_200P	Rev V0.1
Date:	Wednesday, February 26, 2025	Sheet 15 of 30	

UFS Flash



UFS POWER

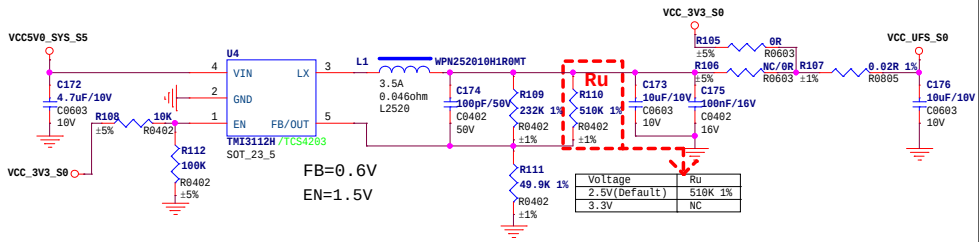
Supported Particles	VCCQ	VCCQ2	VCC
UFS2.0	1.2V	1.8V	3.3V
UFS2.1	No Connect	1.8V	3.3V
UFS2.2	No Connect	1.8V	3.3V
UFS3.0	1.2V	No Connect	2.5V/3.3V
UFS3.1	1.2V	No Connect	2.5V/3.3V

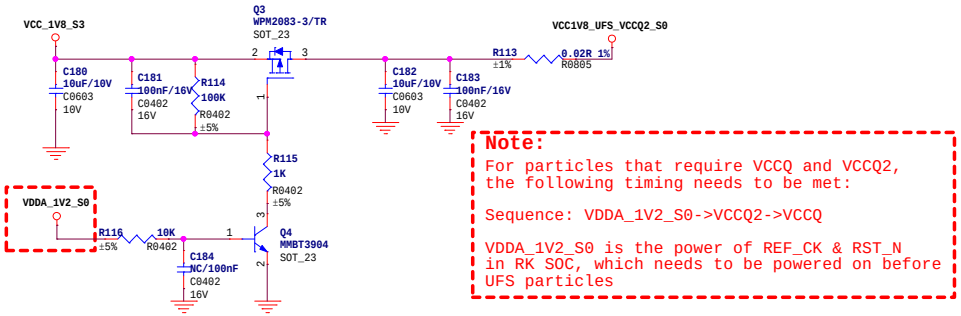
Default UFS device: UFS2.2

Do not support UFS4.0 Device!

Sequence:VCCQ2->VCCQ, VCC is independent

Note:
The power ball that is not used at the particle must be kept floating.

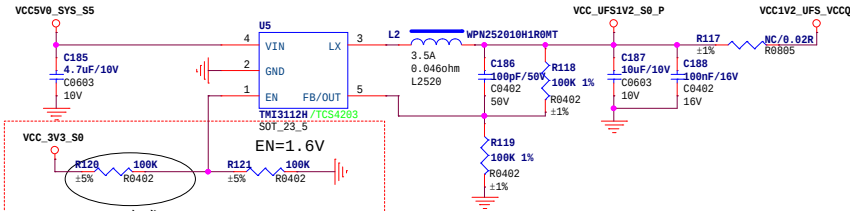




Note:
For particles that require VCCQ and VCCQ2, the following timing needs to be met:

Sequence: VDDA_1V2_S0->VCCQ2->VCCQ

VDDA_1V2_S0 is the power of REF_CK & RST_N in RK SOC, which needs to be powered on before UFS particles

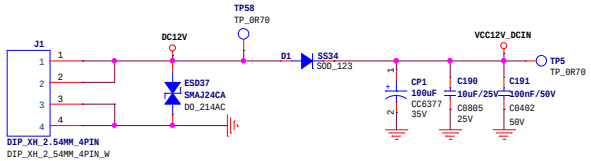


Note:
1. VCC_3V3_S0 is used to ensure the power supply timing of the UFS chip;
2. The resistance voltage division value needs to be designed based on the EN pin threshold of DCDC.

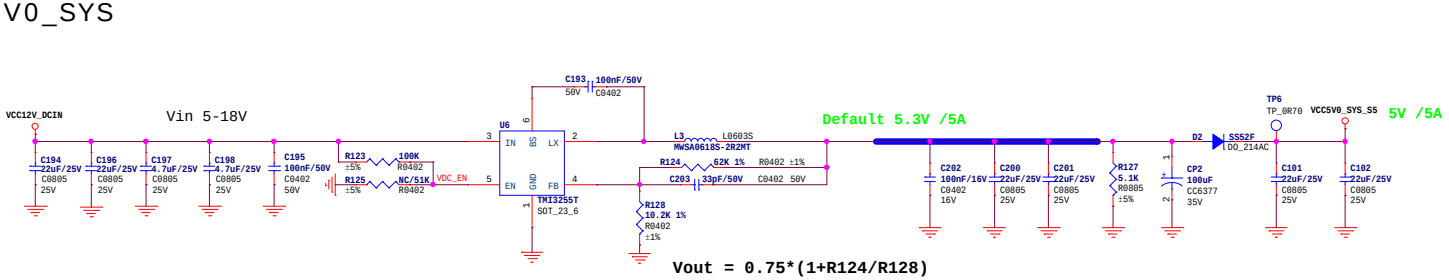
深圳和成东科技有限公司
深圳市宝安区福海街道和平社区福海大道创兴工业园二区1栋3楼

Title	K20_21		
Size A3	Page Name 16.Flash-UFS		Rev V0.1
Date: Wednesday, February 26, 2025	Sheet 16 of 30		

12V/3A DCIN

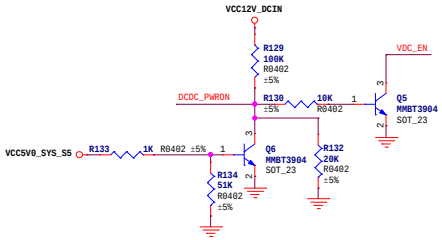


VCC5V0_SYS

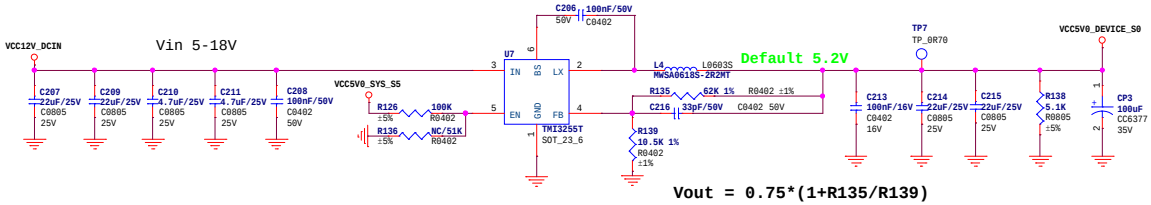


Vout = 0.75*(1+R124/R128)

DCDC_PWRON

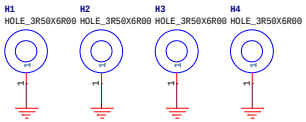


VCC5V0_DEVICE



Vout = 0.75*(1+R135/R139)

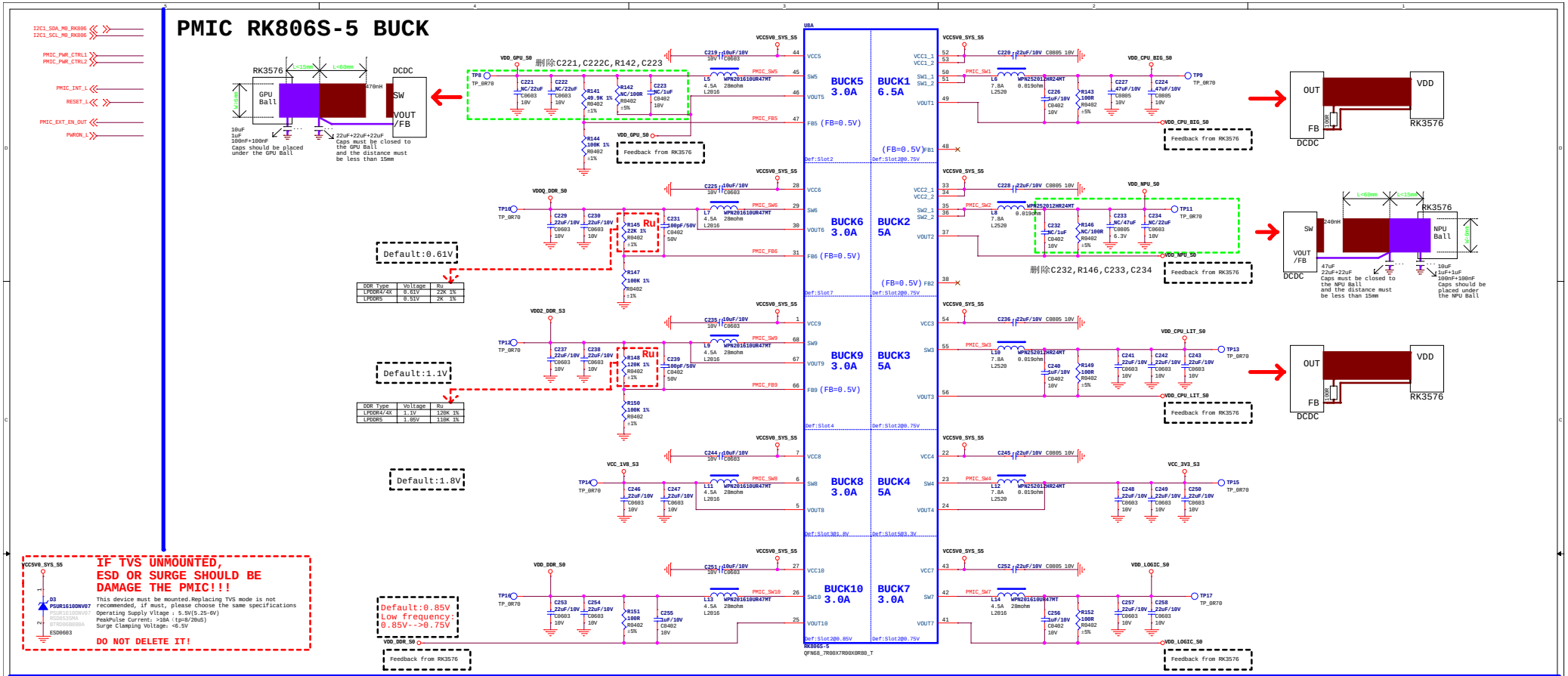
HOLE & MARKE



深圳和成泰科技有限公司

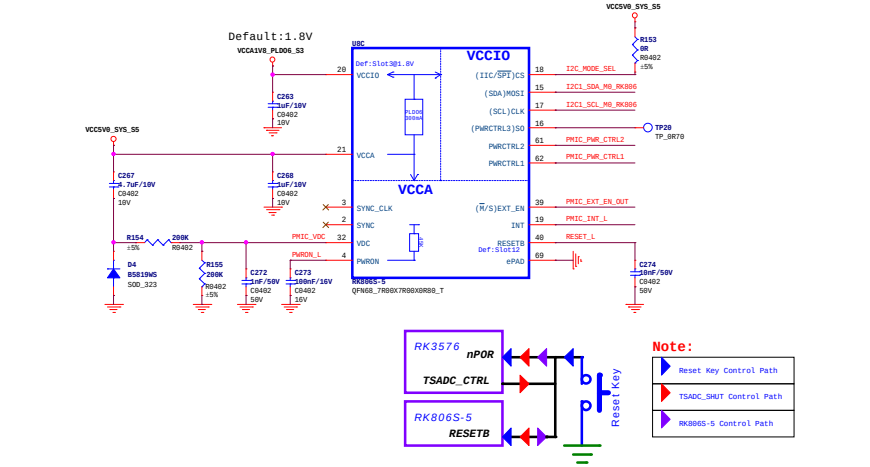
Title	K20_21		
Size: Custom	Page Name	17.Power_DC IN	Rev V0.1
Date: Thursday, February 27, 2025	Sheet 17 of 38		

PMIC RK806S-5 BUCK

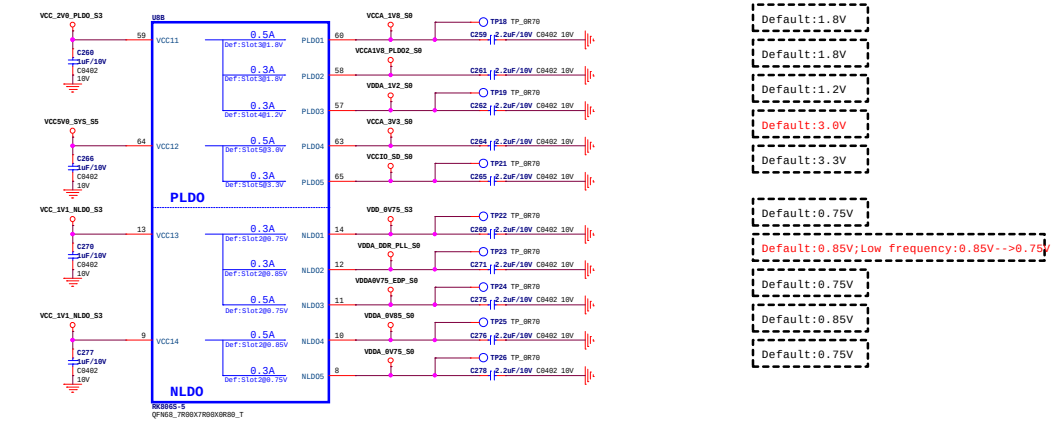


PMIC RK806S-5 Managerment

Note:
I2C Mode:CS(pin18) connected to VCCA(pin21);
SPI Mode(Def):CS(pin18) floating or connected to GND



PMIC RK806S-5 LDO



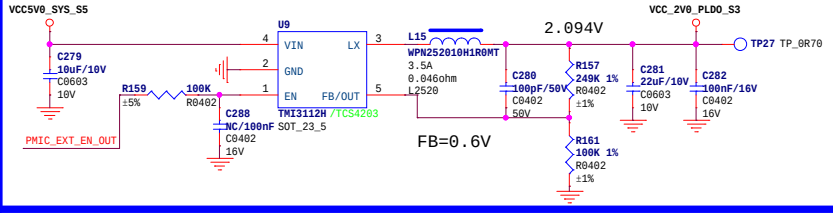
Default:1.8V
Default:1.8V
Default:1.2V
Default:3.0V
Default:3.3V
Default:0.75V
Default:0.85V;Low frequency:0.85V-->0.75V
Default:0.75V
Default:0.85V
Default:0.75V

Note: The RK806 LDO power distribution of the reference chematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

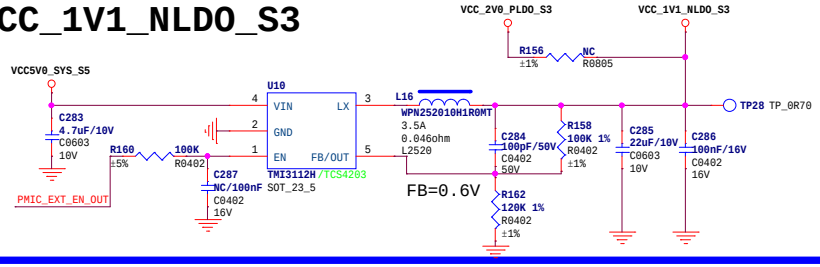
Title	K20_21		
Size A2	Page Name	18.Power-PMIC RK806S-5	Rev V0.1
Date:	Tuesday, March 04, 2025	Sheet 18 of 30	

I2C2_SCL_M0_CC_RTC
I2C2_SDA_M0_CC_RTC
RTC_INT_L
32KOUT_RTC2SOC
32KOUT_RTC2WIFI
PMIC_PWR_CTRL2
PMIC_EXT_EN_OUT

VCC_2V0_PLDO_S3

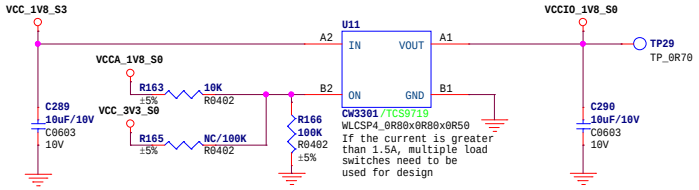


VCC_1V1_NLDO_S3



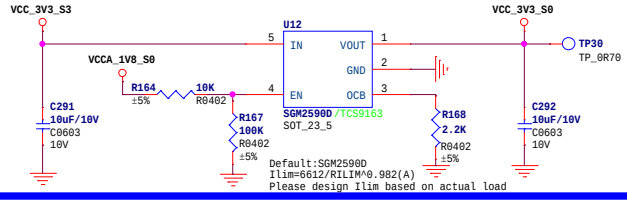
VCCIO_1V8_S0

Note: Need quick output discharge

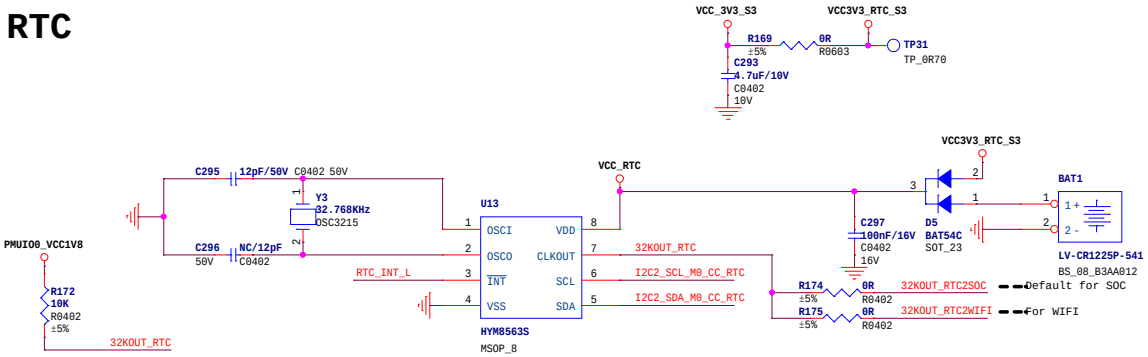


VCC_3V3_S0

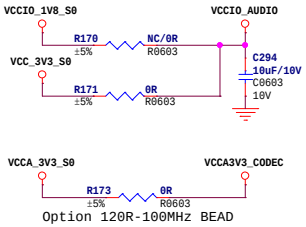
Note: Need quick output discharge



RTC

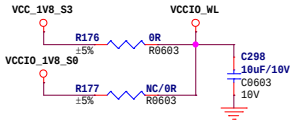


Audio Power



VDD_LOGIC_MEM EXT(Option for test)

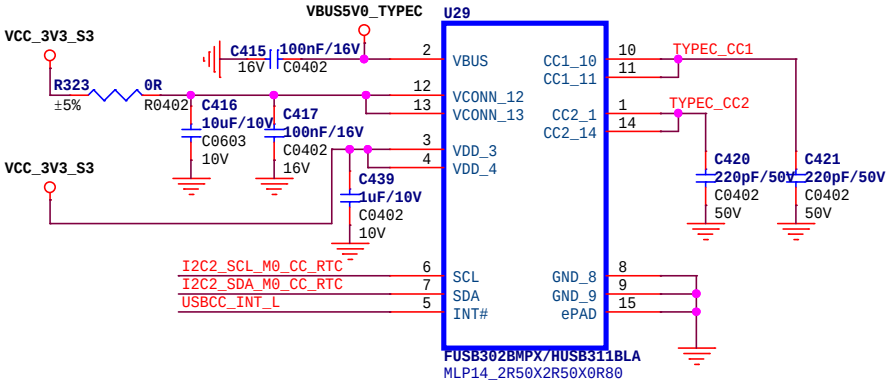
WIFI/BT Power



深圳和成永科技有限公司
深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼

Title	K20_21	
Size A3	Page Name 19.Power-Ext Discrete/RTC IC	Rev V0.1
Date: Wednesday, February 26, 2025	Sheet 19 of 30	

CC



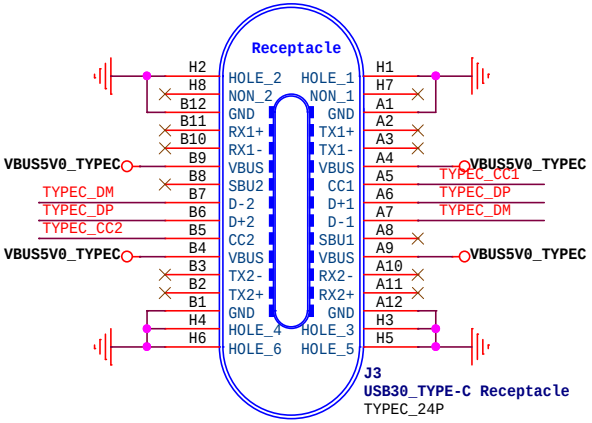
Note:

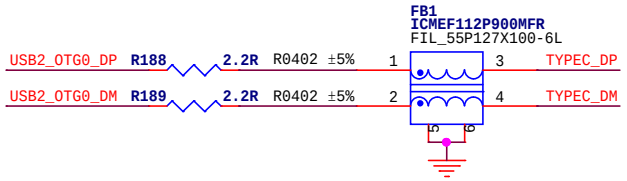
7bit address=0x22

VBUS of FUSB302BMPX: 4 to 21 TYP = 5V
VDD of FUSB302BMPX: 3 to 5.5 TYP = 3.3V
VCONN of FUSB302BMPX: 3 to 5.5

TYPEC

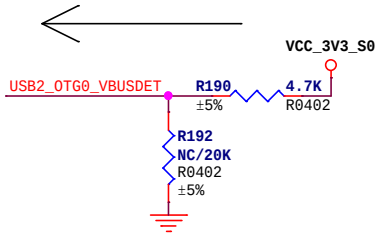
With Displayport Alternate Mode
This is also the firmware download interface



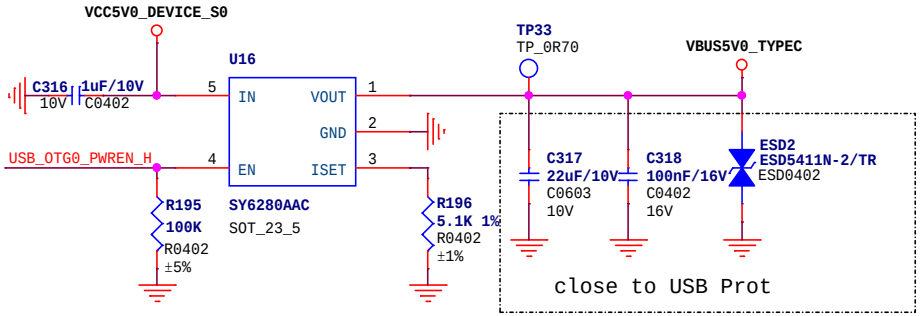


Note:

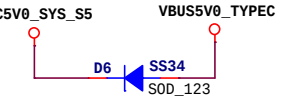
If common mode inductors are needed,
it is recommended to keep 2.2ohm in series
to improve the antistatic ability



USB POWER



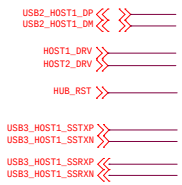
Download power supply



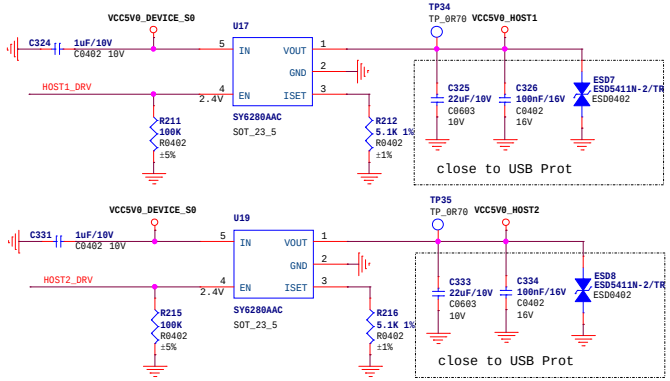
深圳和成东科技有限公司
深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼

Title	K20_21	
Size A4	Page Name 20.USB/TypeC Port	Rev V0.1
Date: Monday, March 03, 2025	Sheet 20 of 30	

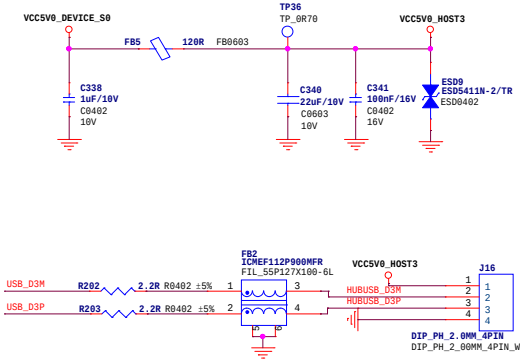
USB_HOST



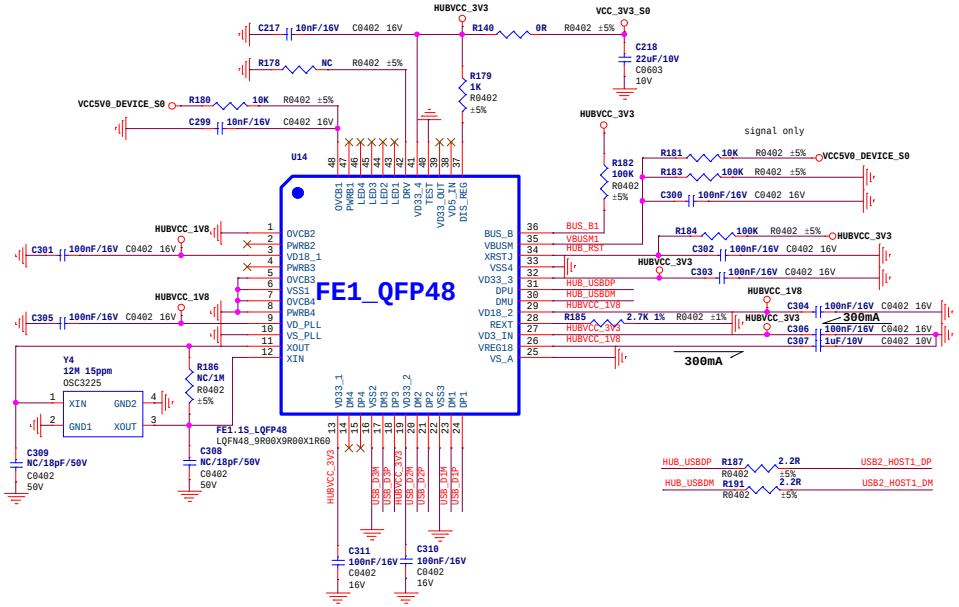
USB POWER



USB TP

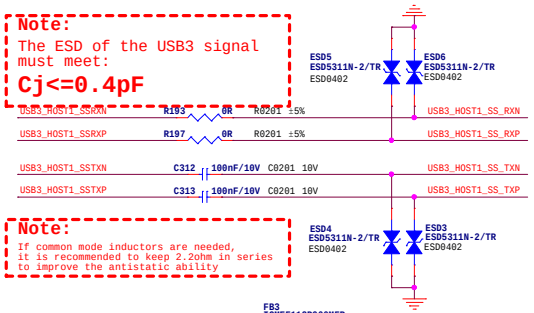


USB HUB

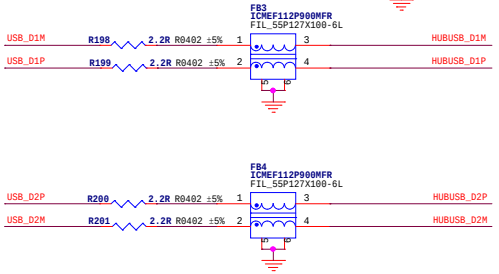


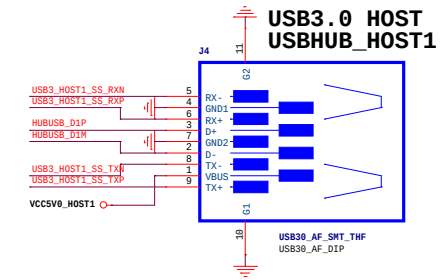
USB Port

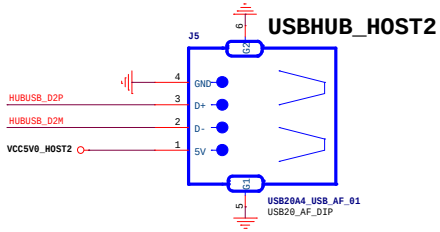
Note:
The ESD of the USB3 signal must meet:
Cj<=0.4pF



Note:
If common mode inductors are needed, it is recommended to keep 2.2ohm in series to improve the antistatic ability





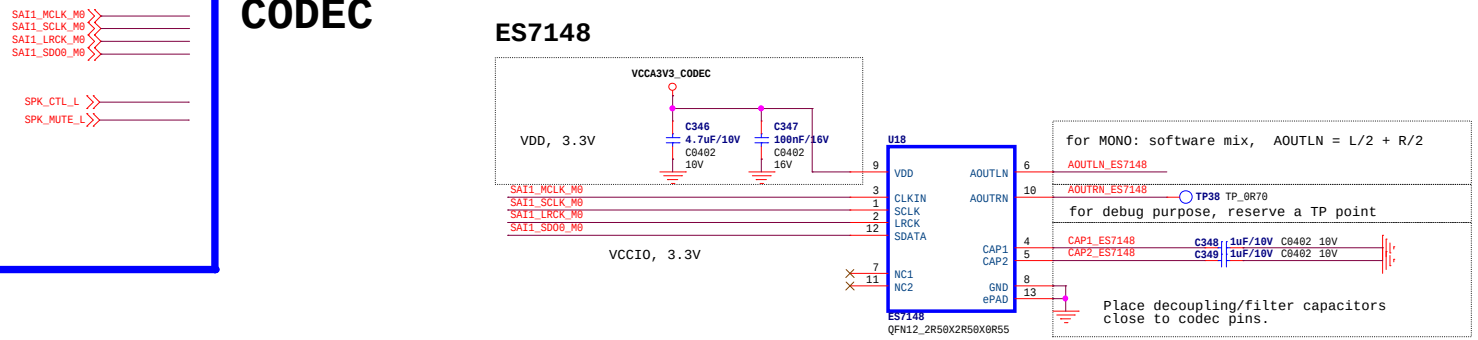


深圳和成永科技有限公司
深圳市宝安区福海街道和平社区福海大道研兴工业园二区1栋8楼

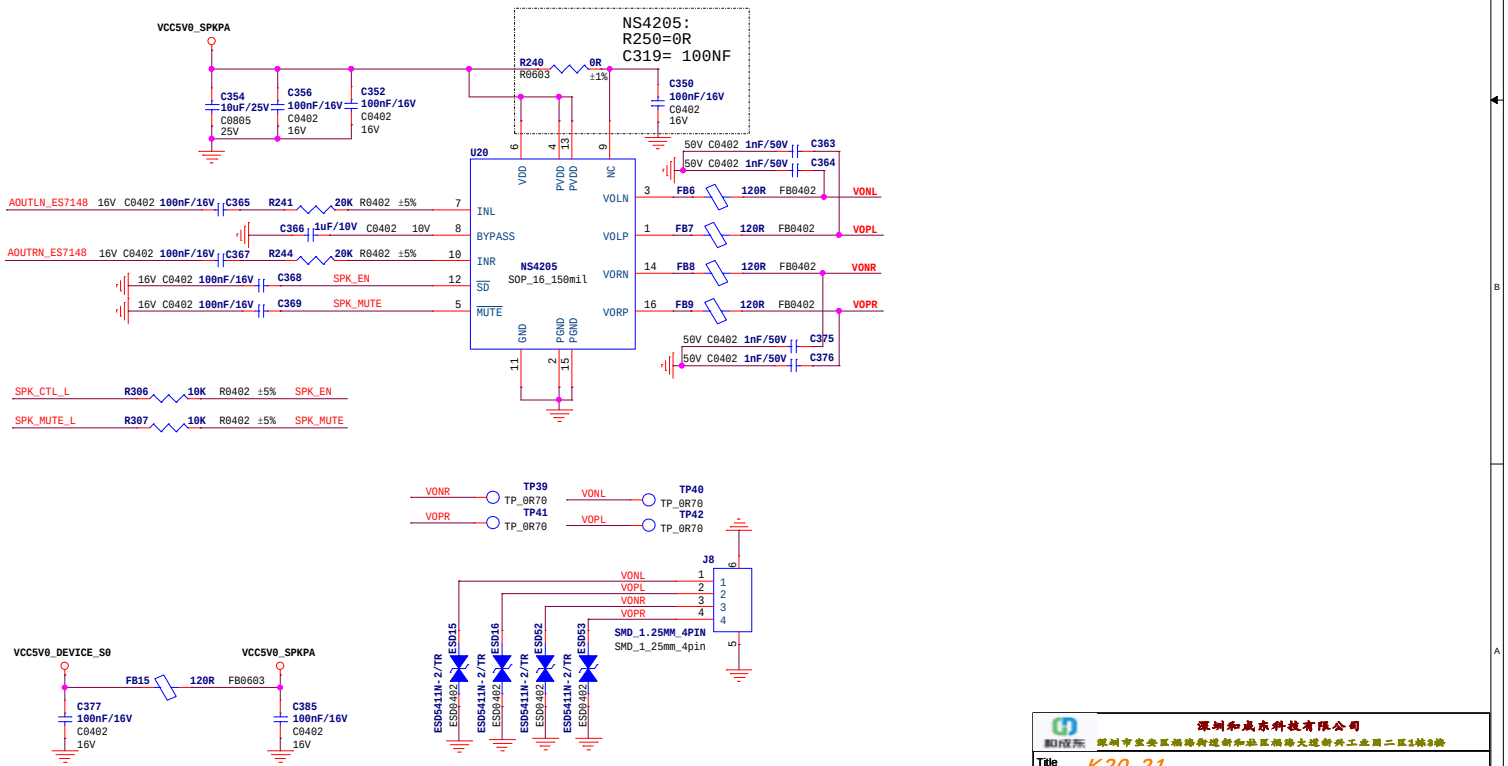
Title	K20_21	
Size: Custom	Page Name: 21.USB/USB HUB	Rev: V0.1
Date: Monday, March 03, 2025	Sheet 21 of 30	

CODEC

ES7148



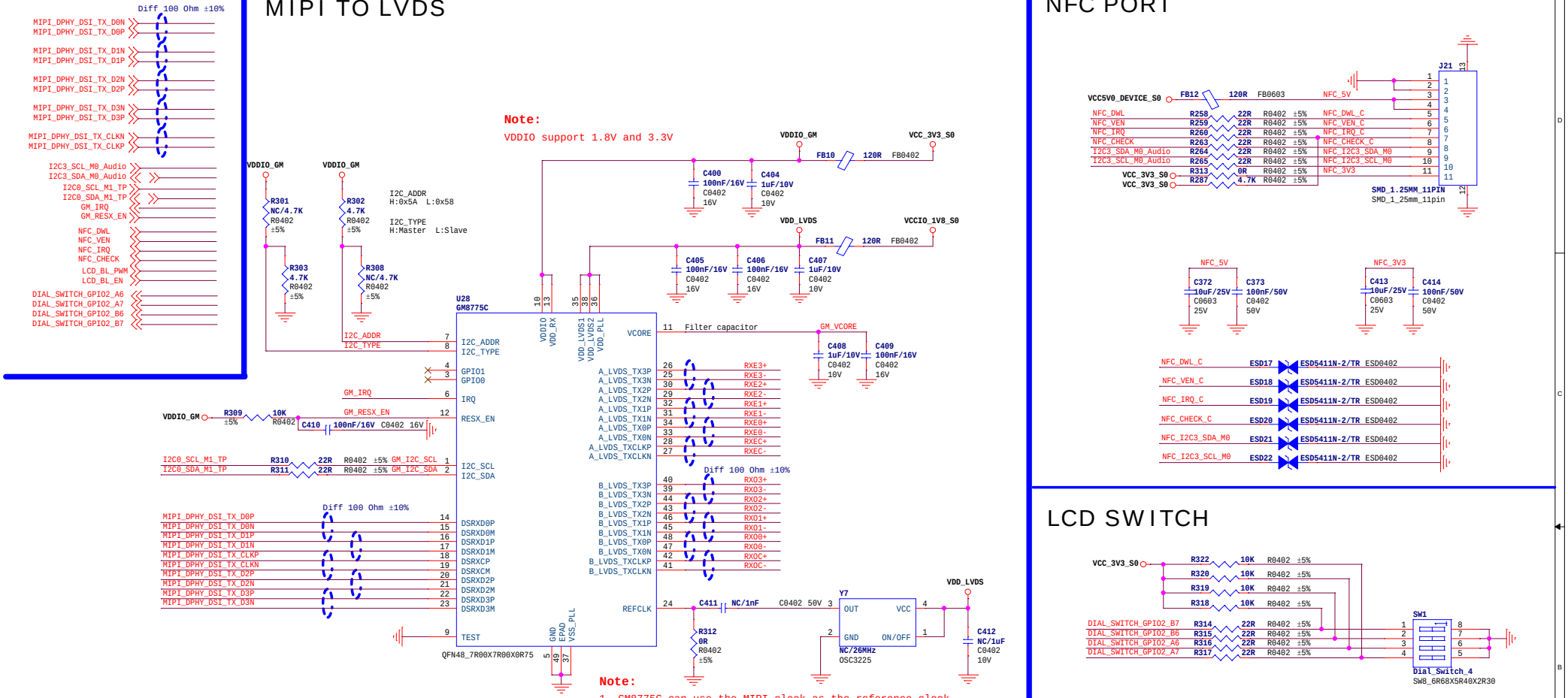
SPK



深圳和威东科技有限公司

Title	K20_21	
Size A3	Page Name 22.Audio-CODEC(ES8388)	Rev V0.1
Date: Friday, February 28, 2025	Sheet 22 of 30	

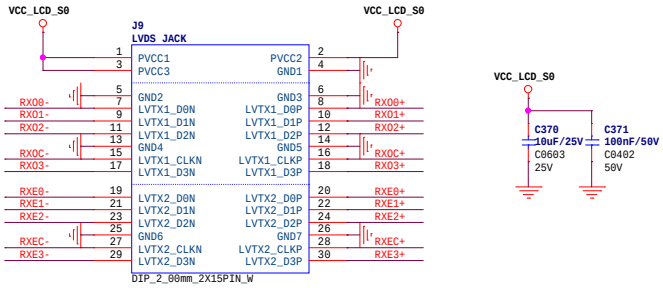
MIPI TO LVDS



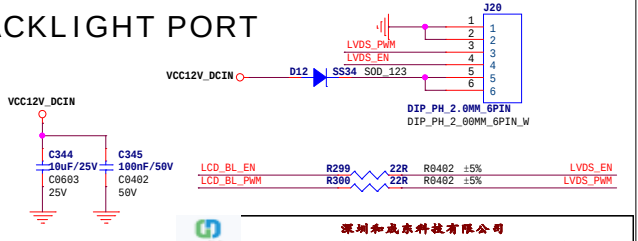
NFC PORT

LCD SWITCH

LVDS PORT



BACKLIGHT PORT

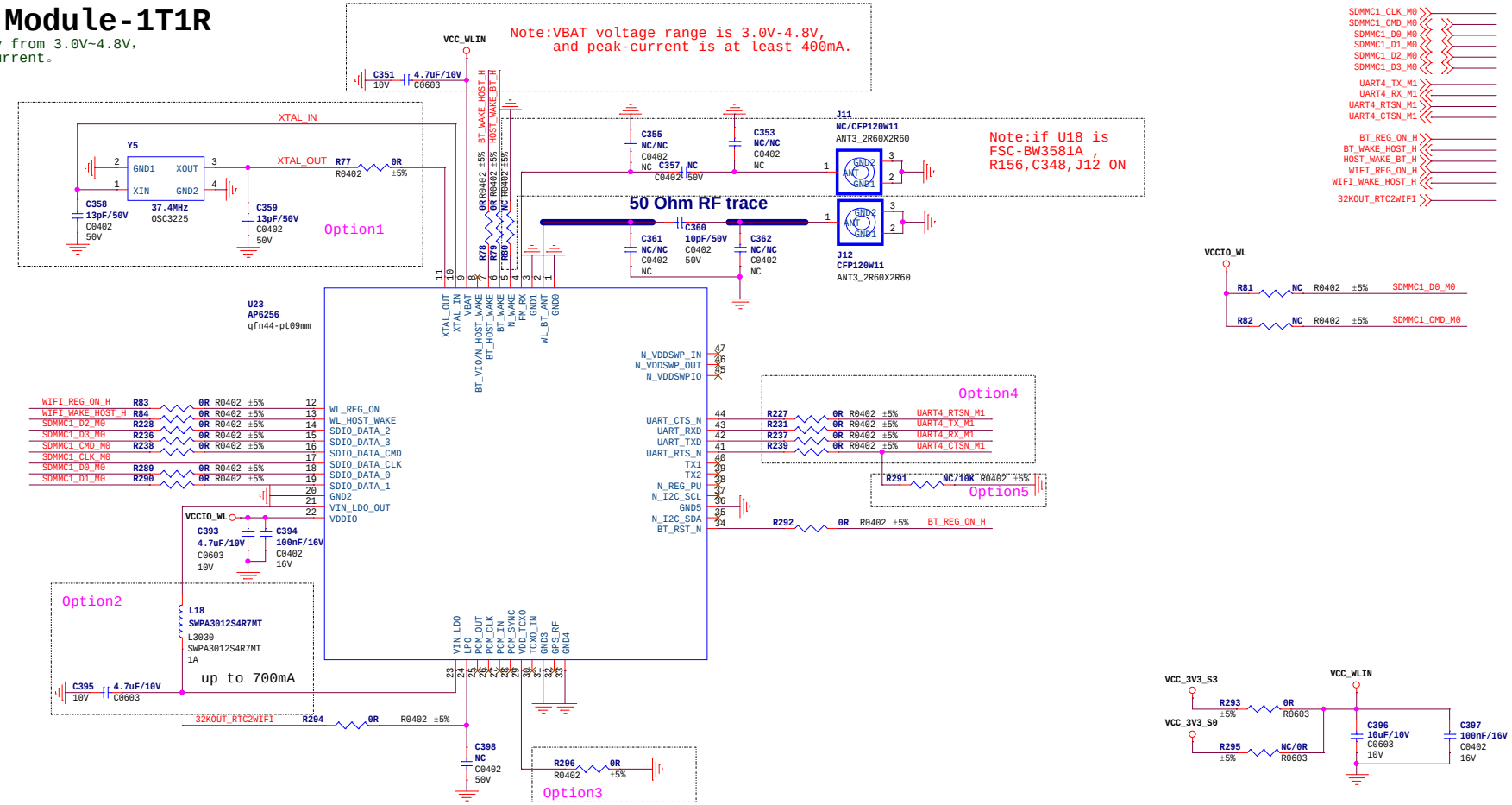


深圳和成系科技有限公司

Title	K20_21		
Size A3	Page Name	23.LCM_MIPI TO LVDS/NFC	Rev V0.1
Date: Saturday, March 01, 2025	Sheet 23 of 30		

WIFI/BT Module-1T1R

Note:VBAT supply from 3.0V~4.8V,
400mA of current。



Note:
Yes: option circuit be mounted
No: option circuit not be mounted

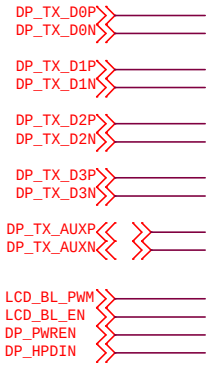
Note:
VCCIO_SDIO voltage is 1.8V

OPTION	WIFI				BT	Crystals	VCCIO_SDIO	OPTION1	OPTION2	OPTION3	OPTION4	OPTION5
	a	b/g/n	ac	5GHz								
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes	No
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.63V	Yes	Yes	No	Yes	No
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.62-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0	Yes	No
RTL8189FTV Module F89FTSM12-W3	No	Yes	No	No	No	Module Integrated	1.8-3.3V	No	No	No	No	No
RTL8723DS Module 6223A-SRD	No	Yes	No	No	4.2	Module Integrated	1.62-3.63V	No	No	No	Yes	Yes
QCA9377 Module 8223A-SR	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	Yes	No
RTL8821CS Module 6221A-SRC	Yes	Yes	Yes	Yes	4.2	Module Integrated	1.7-3.45V	No	No	No	Yes	No

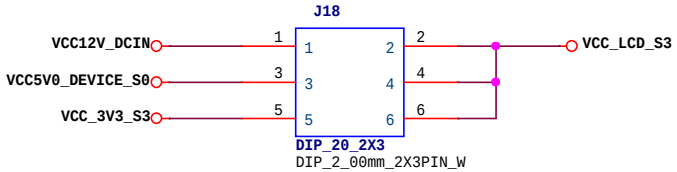
深圳和成系科技有限公司
深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼

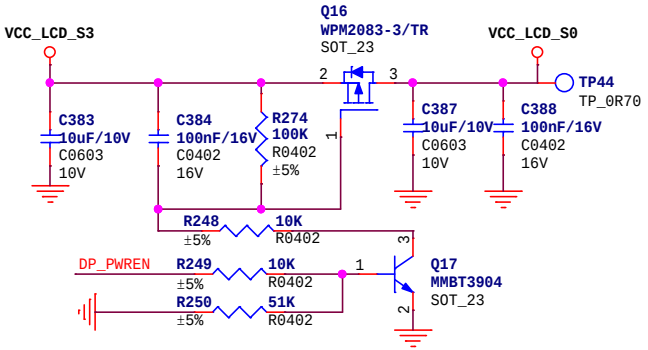
Title	K20_21	
Size A3	Page Name 25.WIFI/BT-SDIO_1T1R	Rev V0.1
Date: Tuesday, March 04, 2025	Sheet 23 of 27	

DP Panel

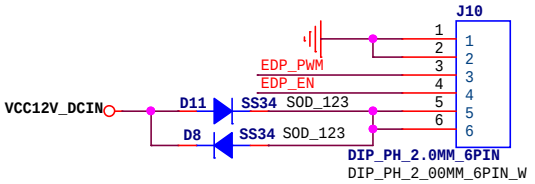


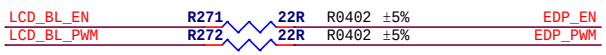
LCD POWER

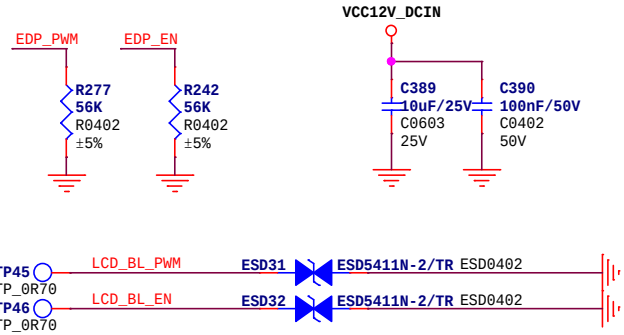




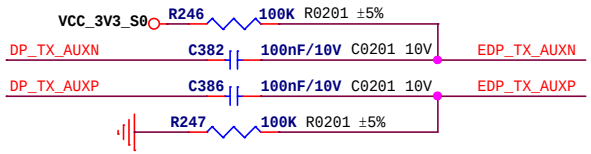
BACKLIGHT PORT

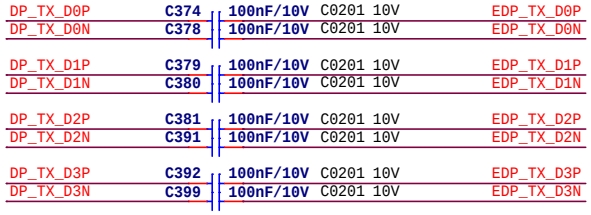


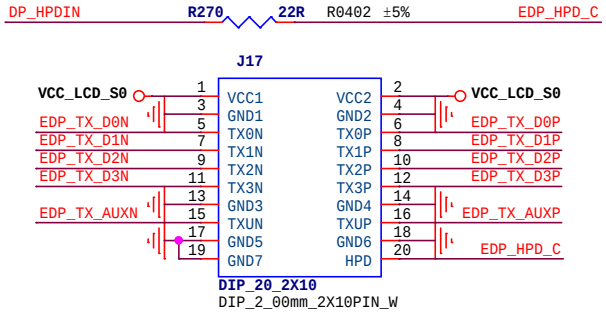


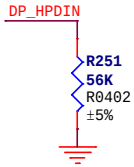


15.6''LCD









深圳和成东科技有限公司
深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼

Title	K20_21		
Size A4	Page Name 24.LCM_eDP		Rev V0.1
Date: Tuesday, March 04, 2025	Sheet 24 of 30		

RGMII0_M0

GMAC0_TXD0_M0
GMAC0_TXD1_M0
GMAC0_TXD2_M0
GMAC0_TXD3_M0
GMAC0_TXCTL_M0
GMAC0_TXCLK_M0

GMAC0_RXD0_M0
GMAC0_RXD1_M0
GMAC0_RXD2_M0
GMAC0_RXD3_M0
GMAC0_RXCTL_M0
GMAC0_RXCLK_M0

ETH_CLK0_25M_OUT_M0

GMAC0_MDC_M0
GMAC0_MDIO_M0
GMAC0_RSTn

Option1

PHY0_XTALOUT — X1 GND X2 — PHY0_XTALIN
Y6 NC/25MHz OSC3225
C418 NC/18pF C0402 50V
C419 NC/18pF C0402 50V

Option2

ETH_CLK0_25M_OUT_M0 — R321 NC R0402 ±5% — PHY0_XTALOUT
R305 0R R0402 ±5% — PHY0_XTALIN
R304 NC R0402 ±5% — PHY0_XTALIN

MAC -----> PHY

Clock mode	R321	R305	R304
RK631A	Yes	No	Yes
YT8531C	Yes	No	Yes
JL2101B	No	Yes	No

U26 H5007 SOIC24_15R10X10R00X4R00

PHY0_MDI0+ — ACM2012H_T05 — FIL0 SDCW2012-2-900TF — PHY1_MDI_0+ — TCT1 MCT1 — LAN1_MCT1
PHY0_MDI0- — PHY1_MDI_0- — TD1+ MX1+ — LAN1_A+
PHY0_MDI1+ — FIL1 — PHY1_MDI_1+ — TD1- MX1- — LAN1_A-
PHY0_MDI1- — FIL2 — PHY1_MDI_1- — TCT2 MCT2 — LAN1_MCT2
PHY0_MDI2+ — FIL3 — PHY1_MDI_2+ — TD2+ MX2+ — LAN1_B+
PHY0_MDI2- — PHY1_MDI_2- — TD2- MX2- — LAN1_B-
PHY0_MDI3+ — FIL4 — PHY1_MDI_3+ — TCT3 MCT3 — LAN1_MCT3
PHY0_MDI3- — PHY1_MDI_3- — TD3+ MX3+ — LAN1_C+
TD3- MX3- — LAN1_C-
TCT4 MCT4 — LAN1_MCT4
TD4+ MX4+ — LAN1_D+
TD4- MX4- — LAN1_D-

C189 10nF/50V C0402 50V
C199 10nF/50V C0402 50V
C204 10nF/50V C0402 50V
C205 10nF/50V C0402 50V

R87 75R R0603 ±5%
R122 75R ±5% R0603 ±5%
R131 75R ±5% R0603 ±5%
R137 75R ±5% R0603 ±5%

J14 RJ45-RJ-046-1-BK RJ45_RJ_046_1_BK

LAN1_A+ 1 — A+
LAN1_A- 2 — A-
LAN1_B+ 3 — B+
LAN1_C+ 4 — C+
LAN1_C- 5 — C-
LAN1_B- 6 — B-
LAN1_D+ 7 — D+
LAN1_D- 8 — D-
Tab up
GLED+ 9
GLED- 10
YLED+ 11
YLED- 12
G1 13
G2 14

R204 510R ±5% R0402 — ESD46 ESD5411N-2/TR ESD0402 — PHY0_LED2/CFG_LDO1
R205 510R ±5% R0402 — ESD47 ESD5411N-2/TR ESD0402 — PHY0_LED1/CFG_LDO0

C212 1000pF C1206 2KV

PHY1_MDI_3- ESD38 ESD5311N-2/TR ESD0402
PHY1_MDI_2- ESD40 ESD5311N-2/TR ESD0402
PHY1_MDI_1- ESD42 ESD5311N-2/TR ESD0402
PHY1_MDI_0- ESD44 ESD5311N-2/TR ESD0402
PHY1_MDI_3+ ESD39 ESD5311N-2/TR ESD0402
PHY1_MDI_2+ ESD41 ESD5311N-2/TR ESD0402
PHY1_MDI_1+ ESD43 ESD5311N-2/TR ESD0402
PHY1_MDI_0+ ESD45 ESD5311N-2/TR ESD0402

LAN1_MCT1 R267 0R R1206 ±5% — J19 1
LAN1_MCT2 R268 0R R1206 ±5% — 2
LAN1_MCT3 R297 0R R1206 ±5% — 3
LAN1_MCT4 R298 0R R1206 ±5% — 4

DIP_XH_2.54MM_4PIN
DIP_XH_2_54MM_4PIN_W

R206 1M R0603 ±5%
C321 1000pF C1206 2KV

R326 NC/4.7K R0402 ±5% — PHY0_LED0/CFG_EXT
R327 4.7K R0402 ±5% — VCC3V3_PHY0
R328 4.7K R0402 ±5% — PHY0_LED2/CFG_LDO1
R329 NC/4.7K R0402 ±5%
R330 4.7K R0402 ±5% — PHY0_LED1/CFG_LDO0

VCC_PHY0_IO Voltage Config

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	PHY0_LED2
External 3.3V (default)	1'b1	2'b00	String 510R to GND
External 1.8V	1'b1	2'b10	String 510R to VCC3V3_PHY
Internal 1.8V	1'b0	2'b10	String 510R to VCC3V3_PHY

R331 NC/4.7K R0402 ±5% — PHY0_RXD2/PLLOFF — R332 4.7K R0402 ±5% — VCCIO_PHY0

Pull-up to disable PLL @ ALDPS mode(Low power mode)

R333 NC/4.7K R0402 ±5% — PHY0_RXD0/RXDLY — R334 4.7K R0402 ±5% — VCCIO_PHY0

Pull-up for additional 2ns delay to RXC for data latching

R336 4.7K R0402 ±5% — PHY0_RXD1/TXDLY — R337 NC/4.7K R0402 ±5% — VCCIO_PHY0

Pull-up for additional 2ns delay to TXC for data latching

R341 NC/4.7K R0402 ±5% — PHY0_RXD3/PHYAD0 — R340 4.7K R0402 ±5% — VCCIO_PHY0
R343 4.7K R0402 ±5% — PHY0_RXCLK/PHYAD1
R344 4.7K R0402 ±5% — PHY0_RXDV/PHYAD2

PHY Address Config

PHY Address	PHYAD[2:0]
1 (default)	3'b001

VDD10_PHY0

PHY0_REG_OUT — L20 SWPA3015S2R2NT L3030 — C428 4.7uF/10V C0402 10V — C429 100nF/16V C0402 16V — Close to PIN30

C430 100nF/16V C0402 16V — Close to PIN21

C431 100nF/16V C0402 16V
C432 100nF/16V C0402 16V
C435 100nF/16V C0402 16V — Close to PIN3,8,38

VCCIO_1V8_S0 — R338 NC/0R R0402 ±5% — VCC_3V3_S0 — R342 0R R0402 ±5%
VCC_3V3_S0 — R345 0R R0402 ±5%

From system Power

VCCIO_PHY0 — C422 4.7uF/10V C0402 10V

C423 1uF/10V C0402 10V
C424 100nF/16V C0402 16V — Close to PIN28

VCC3V3_PHY0 — C425 4.7uF/10V C0402 10V

C426 100nF/16V C0402 16V
C427 100nF/16V C0402 16V — Close to PIN11,40

C433 4.7uF/10V C0402 10V
C434 100nF/16V C0402 16V — Close to PIN29

VDD10_PHY0

R335 2.49K 1% R0402 ±1%
PHY0_CLKOUT125 — TP43 TP_0R70
VCC3V3_PHY0
GMAC0_INT/PMEB — R339 4.7K R0402 ±5%

OD,pull up 3.3V
Connect to the GPIO in
SOC 3.3V power domain.

U27 RK631A QFN40_5R00X5R00X0R90_T

E_Pad
AVDD33 RSET AVDD10 XTAL_OUT/EXT_CLKIN XTAL_IN CLKOUT LED2/CFG_LDO1 LED1/CFG_LDO0 LED0/CFG_EXT INTB/PMEB
PHY0_XTALOUT PHY0_XTALIN PHY0_CLKOUT125 PHY0_LED2/CFG_LDO1 PHY0_LED1/CFG_LDO0 PHY0_LED0/CFG_EXT

PHY0_MDI0+ PHY0_MDI0- PHY0_MDI1+ PHY0_MDI1- PHY0_MDI2+ PHY0_MDI2- PHY0_MDI3+ PHY0_MDI3-
MDI[0]+ MDI[0]- AVDD10 MDI[1]+ MDI[1]- MDI[2]+ MDI[2]- AVDD10 MDI[3]+ MDI[3]-

REG_OUT DVDD33 DVDD_RG RXC/PHYAD1 RXCTL/PHYAD2 RXD0/RXDLY RXD1/TXDLY RXD2/PLLOFF RXD3/PHYAD0 DVDD10
PHY0_REG_OUT
PHY0_RXCLK/PHYAD1 PHY0_RXDV/PHYAD2 PHY0_RXD0/RXDLY PHY0_RXD1/TXDLY PHY0_RXD2/PLLOFF PHY0_RXD3/PHYAD0

AVDD33 PHYRSTB MDC MDIO TXD3 TXD2 TXD1 TXD0 TXCTL TXC
PHY0_RSTn GMAC0_MDC_M0 GMAC0_MDIO_M0 GMAC0_TXD3_M0 GMAC0_TXD2_M0 GMAC0_TXD1_M0 GMAC0_TXD0_M0 GMAC0_TXCTL_M0 GMAC0_TXCLK_M0

C436 NC/3.0pF 50V C0402

R252 1.8K R0402 ±5% — VCCIO_PHY0

PHYRSTB is 3.3V IO

GMAC0_RSTn — R347 0R R0402 ±5% — PHY0_RSTn
C437 100nF/16V C0402 16V — Close to PIN12

Close to PHY

PHY0_RXD0/RXDLY — R348 22R R0402 ±5% — GMAC0_RXD0_M0
PHY0_RXD1/TXDLY — R349 22R R0402 ±5% — GMAC0_RXD1_M0
PHY0_RXD2/PLLOFF — R350 22R R0402 ±5% — GMAC0_RXD2_M0
PHY0_RXD3/PHYAD0 — R351 22R R0402 ±5% — GMAC0_RXD3_M0
PHY0_RXCLK/PHYAD1 — R352 22R R0402 ±5% — GMAC0_RXCLK_M0 — C438 NC 50V C0402
PHY0_RXDV/PHYAD2 — R353 22R R0402 ±5% — GMAC0_RXCTL_M0

深圳和点科技有限公司
深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼

Title	K20_21		
Size A3	Page Name	26.Ethernet-GEPHY_RGMII0	Rev V0.1
Date: Thursday, February 27, 2025	Sheet 26 of 30		

HDMI 2.1 Support video output up to 4Kx2K@120Hz

Diff 100 Ohm ±10%

HDMI_TX_SBDP
HDMI_TX_SBDN
HDMI_TX_D0P
HDMI_TX_D0N
HDMI_TX_D1P
HDMI_TX_D1N
HDMI_TX_D2P
HDMI_TX_D2N
HDMI_TX_D3P
HDMI_TX_D3N
HDMI_TX_SDA
HDMI_TX_SCL
HDMI_TX_CEC_M0
HDMI_TX_HPDIN_M0
HDMI_TX_ON_H

Note:
Close to HDMI Connector

HDMI_TX_D0P	C320	220nF/10V	C0201 10V
HDMI_TX_D0N	C322	220nF/10V	C0201 10V
HDMI_TX_D1P	C323	220nF/10V	C0201 10V
HDMI_TX_D1N	C327	220nF/10V	C0201 10V
HDMI_TX_D2P	C328	220nF/10V	C0201 10V
HDMI_TX_D2N	C329	220nF/10V	C0201 10V
HDMI_TX_D3P	C330	220nF/10V	C0201 10V
HDMI_TX_D3N	C332	220nF/10V	C0201 10V

Diff 100 Ohm ±10%

Default

HDMI_TX0P
HDMI_TX0N
HDMI_TX1P
HDMI_TX1N
HDMI_TX2P
HDMI_TX2N
HDMI_TX3P
HDMI_TX3N

Note:
Close to HDMI Connector

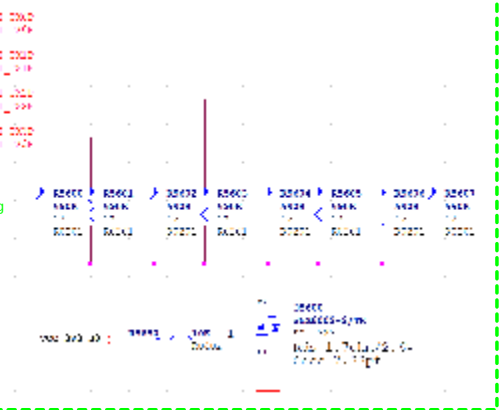
R223 590R 1% R0201 ±1%
R224 590R 1% R0201 ±1%
R225 590R 1% R0201 ±1%
R226 590R 1% R0201 ±1%
R229 590R 1% R0201 ±1%
R230 590R 1% R0201 ±1%
R232 590R 1% R0201 ±1%
R233 590R 1% R0201 ±1%

HDMI_TX_ON_H

Q7 WNM6002-3/TR SOT_323
Q8 WNM6002-3/TR SOT_323
Q9 WNM6002-3/TR SOT_323
Q10 WNM6002-3/TR SOT_323

Rds=1.7ohm/2.6V
Coss=7.33pf

Option:
When only supporting HDMI 2.0 mode, this simplified circuit can be used.



Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

Note:
The controller only support AC coupled link.
In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.

VCC5V0_DEVICE_S0
D7 B5819WS SOD_323
VCC5V_HDMI_TX

HDMI TX DDC

VCC5V0_DEVICE_S0
D10 B5819WS SOD_323
VCC_3V3_S0
R245 20K R0402 ±5%
R256 1.8K R0402 ±5%
Q12 WNM2021-3/TR SOT_323
HDMI_TX_SCL R257 ±5% 100R R0402
HDMI_TX_SCL_PORT

VCC_3V3_S0
R254 27K R0402 ±5%
R255 1.8K R0402 ±5%
Q18 WNM2021-3/TR SOT_323
HDMI_TX_SDA R282 100R R0402 ±5%
HDMI_TX_SDA_PORT

HDMI TX ARC

HDMI_TX_SBDP C339 1uF/10V C0402 10V HDMITX_SBDP
HDMI_TX_SBDN C335 1uF/10V C0402 10V HDMITX_HPDIN/HDMITX_SBDN

HDMI TX HPD

VCC_3V3_S0
R234 47K R0402 ±5%
R235 47K R0402 ±5%
HDMI_TX_HPDIN_M0
3.3V IO
Q11 WNM2021-3/TR SOT_323
Q14 WNM2021-3/TR SOT_323
R243 ±5% 1.2K R0402
R261 47K R0402 ±5%
HDMITX_HPDIN/HDMITX_SBDN
2.4-5.3V

HDMI TX CEC

VCC_3V3_S0 VCC5V0_DEVICE_S0
R253 27K R0402 ±5%
Q19 WNM2021-3/TR SOT_323
HDMI_TX_CEC_M0 R284 100R R0402 ±5%
HDMI_TX_CEC_PORT

Cj<=0.2pF

J7 HDMI_A HDMI_A_19PIN

ED1 ESD5344D SON10_2R50X1R00X0R50
ED2 ESD5344D SON10_2R50X1R00X0R50

HDMI_TX2P
HDMI_TX2N
HDMI_TX1P
HDMI_TX1N
HDMI_TX0P
HDMI_TX0N
HDMI_TX3P
HDMI_TX3N
HDMI_TX_CEC_PORT
HDMI_TX_SCL_PORT
HDMI_TX_SDA_PORT
HDMITX_HPDIN/HDMITX_SBDN
HDMITX_SBDP
VCC5V_HDMI_TX

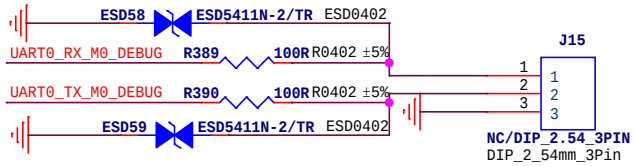
ESD5311N-2/TR ESD12 ESD0402
ESD5411N-2/TR ESD48 ESD0402
ESD5411N-2/TR ESD49 ESD0402
ESD5411N-2/TR ESD50 ESD0402
ESD5311N-2/TR ESD14 ESD0402

C337 1uF/10V C0402 10V

D2P D2_G D2N D1P D1_G D1N D0P D0_G D0N CLKP CLK_G CLKN CEC Utility SCL SDA GND +5V HPD
Type A

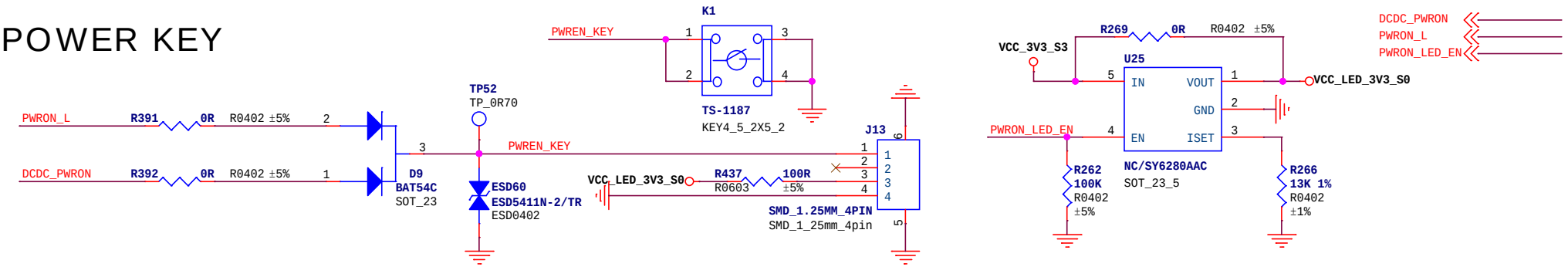
深圳和成东科技有限公司	
Title	K20_21
Size A3	Page Name 27.HDMI 2.1
Rev	V0.1
Date: Thursday, February 27, 2025	Sheet 27 of 30

UART DEBUG

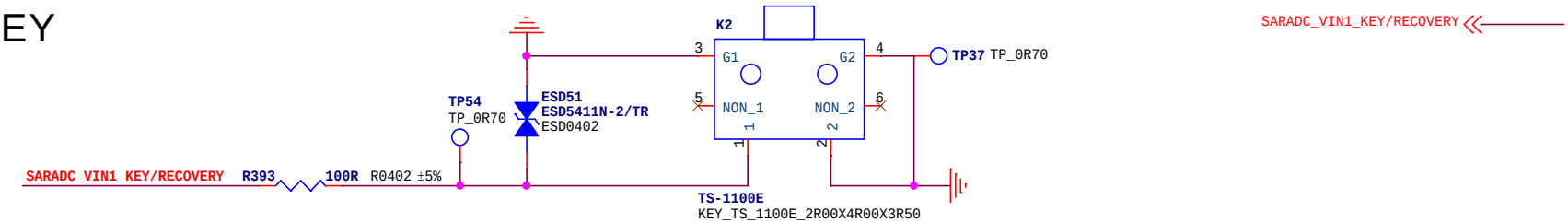


UART0_TX_M0_DEBUG
UART0_RX_M0_DEBUG

POWER KEY

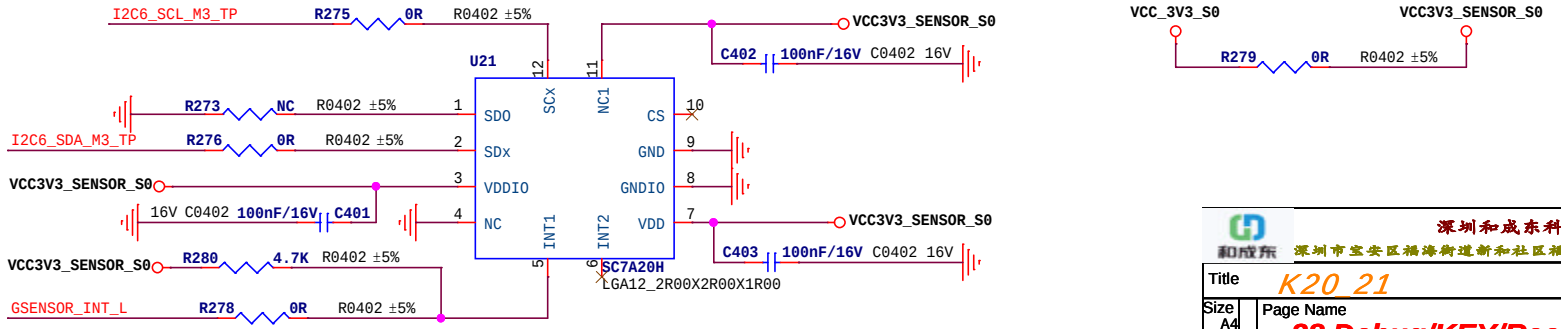


RECOVERY KEY



Gyroscope+G-sensor

I2C6_SCL_M3_TP
I2C6_SDA_M3_TP
GSENSOR_INT_L



深圳和成东科技有限公司
深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼

Title	K20_21	
Size A4	Page Name 28.Debug/KEY/Recovery/G-sensor	Rev V0.1
Date: Wednesday, February 26, 2025	Sheet 28 of 30	

TF CARD

SDMMC0_D0
SDMMC0_D1
SDMMC0_D2
SDMMC0_D3
SDMMC0_CMD
SDMMC0_CLK
SDMMC0_DET_L
SDMMC0_PWREN

VCC_3V3_S3
C94 1uF/10V C0402 10V
U15
IN VOUT GND EN ISET
SY6280AAC SOT_23_5
SDMMC0_PWREN 2.4V
R69 100K R0402 ±5%
R214 4.7K 1% R0402 ±1%
TP32 TP_0R70 VCC3V3_SD_S0
C95 22uF/10V C0603 10V
C96 100nF/16V C0402 16V
close to MicroSD Card

MicroSD Card

VCC3V3_SD_S0
SDMMC0_D2 R209 22R R0402 ±5%
SDMMC0_D3 R210 22R R0402 ±5%
SDMMC0_CMD R213 22R R0402 ±5%
SDMMC0_CLK
SDMMC0_D0 R217 22R R0402 ±5%
SDMMC0_D1 R218 22R R0402 ±5%
SDMMC0_DET_L R221 100R R0402 ±5%
ESD10 ESD11 ESD13 ESD33 ESD34 ESD35 ESD36
ESD5411N-2/TR ESD0402
ESD5311N-2/TR ESD0402
J2 TFP09-2-12B TF_card
DATA2 CD/DATA3 CMD VDD CLK VSS DATA0 DATA1 CD
G1 G2 G3 G4 NON_1 NON_2

IR Receiver

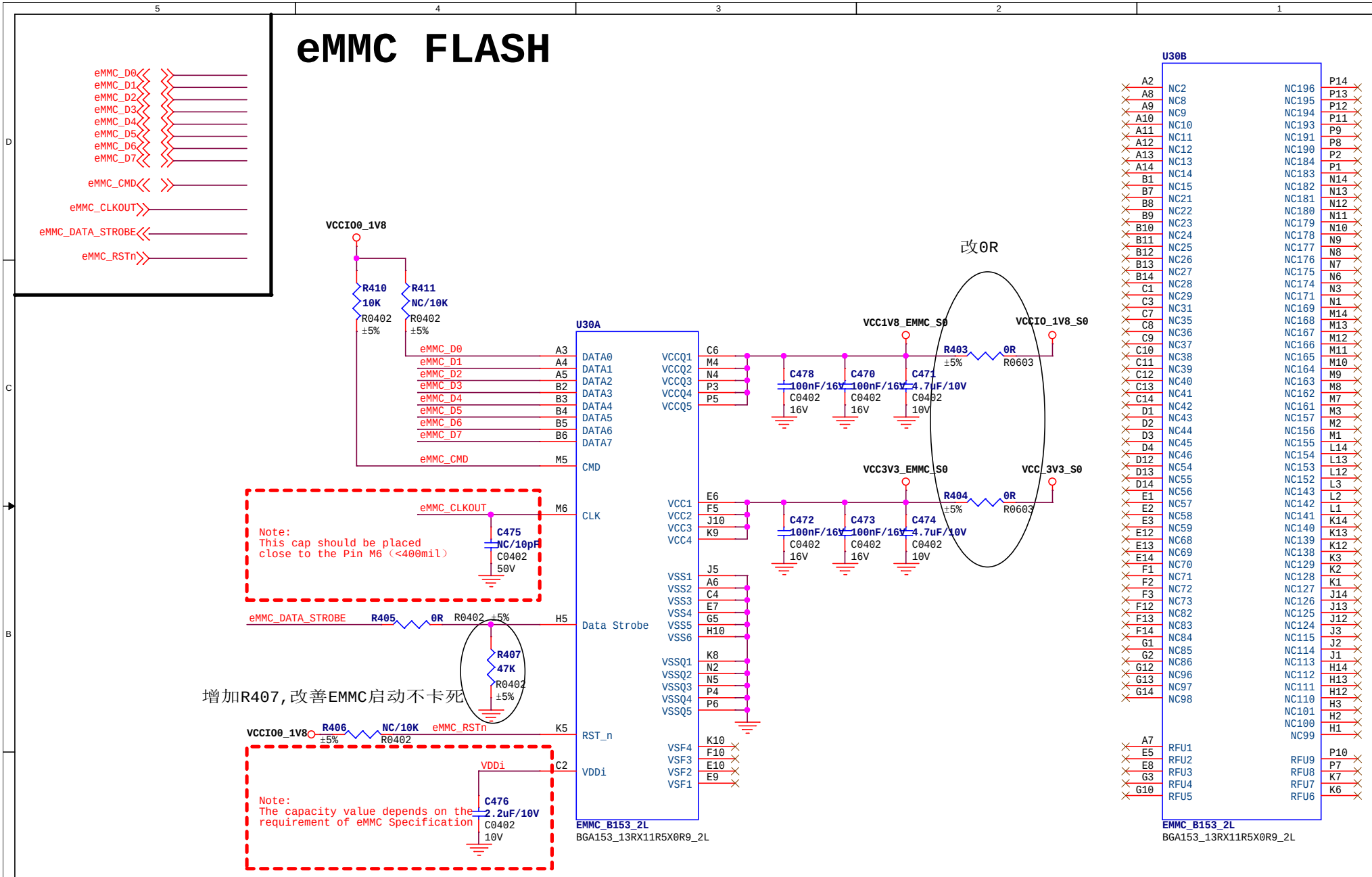
PWM0_CH0_M0_IR
IRLED1_EN
IRLED2_EN

VCC_3V3_S3
U22 U24
IN VOUT GND EN ISET
SY6280AAC SOT_23_5
R281 100K R0402 ±5%
R283 13K 1% R0402 ±1%
R286 100K R0402 ±5%
R288 13K 1% R0402 ±1%
C343 22uF/10V C0603 10V
C342 100nF/16V C0402 16V
R219 0R R0402 ±5%
J6 DIP_PH_2.0MM_5PIN DIP_PH_2_00MM_5PIN_W
R285 22R R0402 ±5%
R220 10K R0402 ±5%
C336 1nF/50V C0402 50V
3.3V
PWM0_CH0_M0_IR

深圳和成东科技有限公司
深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼

Title	K20_21		
Size A4	Page Name	29.TF CARD/IR Receiver	Rev V0.1
Date: Wednesday, February 26, 2025	Sheet 29 of 30		

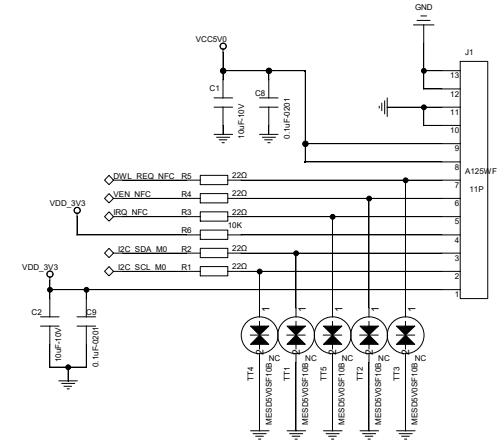
eMMC FLASH

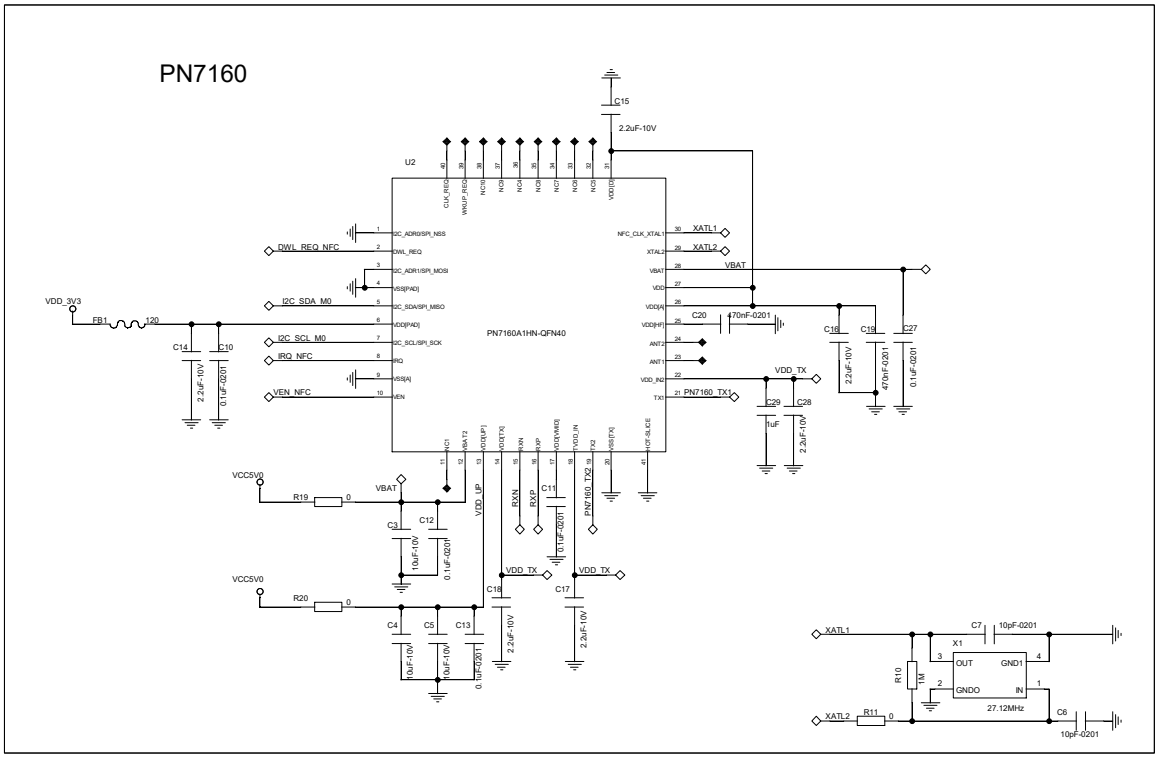


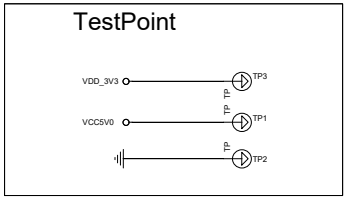
深圳和成东科技有限公司
深圳市宝安区福海街道新和社区福海大道新兴工业园二区1栋3楼

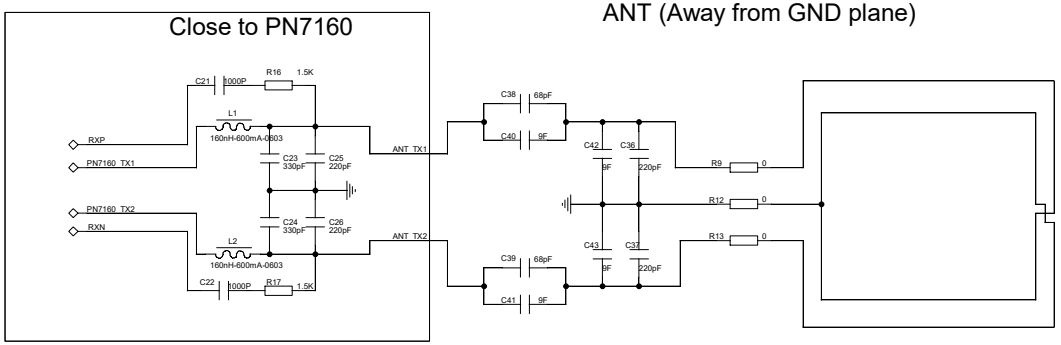
Title	K20_21	
Size A4	Page Name 30.Flash-eMMC	Rev V0.1
Date: Wednesday, February 26, 2025	Sheet 30 of 30	

NFC Module









APPROVALS		DATE	K320-NFC-V01
DRAWN	Liuying	2025/02/25	
CHECKED			
ISSUED			VER V01 SHEET 1/1

H=4ND; V=4LA