Electronic and Software Architecture and Design Document for: SPR RadStar 2.0 Continuous Radon Monitor

Revision 1

5/25/2018

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1 Introduction

1.1 Purpose

The purpose of this document is to specify the architecture and design details of both the electronics snd firmware for the RadStar 2.0 Main PCB.

1.2 Scope

The document is intended to provide a high level guidance (architecture) and specify details of the design that would otherwise not be obvious from review of the schematics or firmware source code.

1.3 Definitions, Acronyms, and Abbreviations

Term	Definition
AGM	Absorbed Glass Mat
BLE	Bluetooth Low Energy. A communications technology for two-way digital data transfer via radio. This technology is supported by many handheld communication devices.
CRM	Continuous Radon Monitor
FKV	Flash Key Value

1.4 References

2 Document Number	Document Name
SPR1804104-ers	RadStar2 Electrical Requirements Specification
SPR1804107-srs	RadStar2 Firmware Requirements

2.1 Overview

This document is intended to encompass the architecture and design for both the electronics and firmware of the main board for the RadStar 2.0. It is broken into four sections, Electronics Architecture, Electronics Design, Software Architecture, and Software Design.

In Electronics Architectures, the high level blocks are identified.

In Electronics Design, any detailed description of how or why a particular circuit is designed and any layout, assembly or other criteria that affect those design decisions.

In Firmware Architecture the major blocks of the design are identified.

In Firmware Design, details regarding critical features affecting implementation are specified.

3 System Overview

This document covers the Main PCB of the RadStar 2.0. It is connected to both a keypad/LEDs and Radon detection chamber that are not part of the design detail contained herein. The batteries are considered to be part of this overall design document.

4 Electronics Architecture Design

The electronics will be designed around an ST Microelectronics ARM based processor.

Peripherals for Temperature/Barometric Pressure, and Humidity will be selected to use SPI bus interfaces in order to minimize driver development.

A power management module will handle charging of the batteries, reporting of charge status to the processor, and power control via the external Power On/Off button. Power On/Off will be available as both processor control, and via a forced hold done of the power On/Off button.

Power input is expected to be via the USB interface connector. The design is expected to require well less than the 500 mA (5v) maximum of USB 2.0 to operate. However to accommodate a more rapid charge, the design will allow for USB 3 connection and the higher level of power available to that standard.

LED control is to be handled through GPIO off of the processor. This initial diagram depicts the LEDS as off board (part of the keypad assembly). This is one option that allows for a more streamlined assembly and lower mechanical design. Alternatively, these LEDs could be placed on the board, requiring more effort by the Spruce mechanical team to deal with case openings, light pipes, and alignments.

In Figure 1 is depicted the external interfaces to the board. Figure 2 depicts the expected modules on the RS2 main PCB.

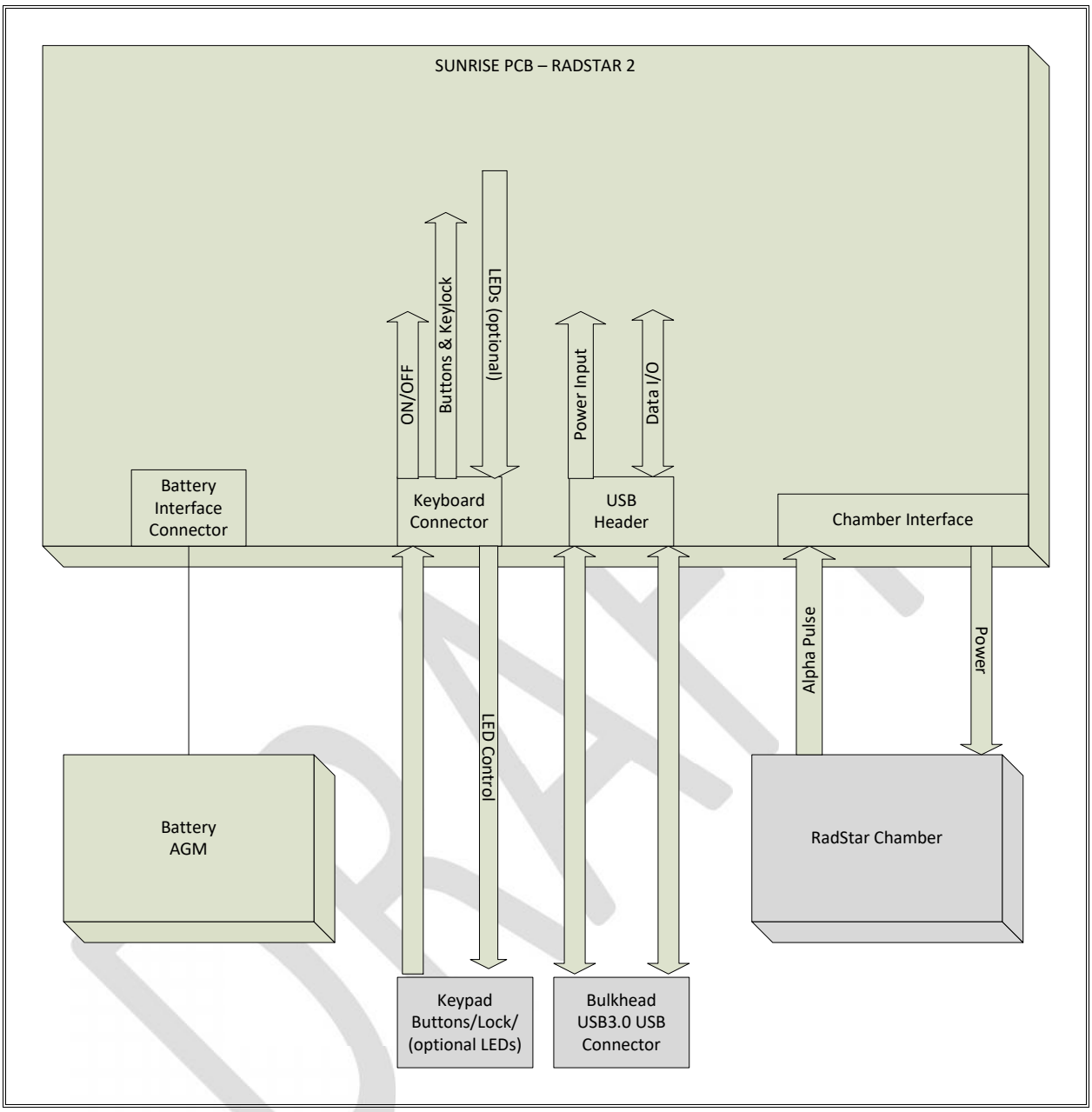

Figure 1 - RS2 Mainboard interconnects

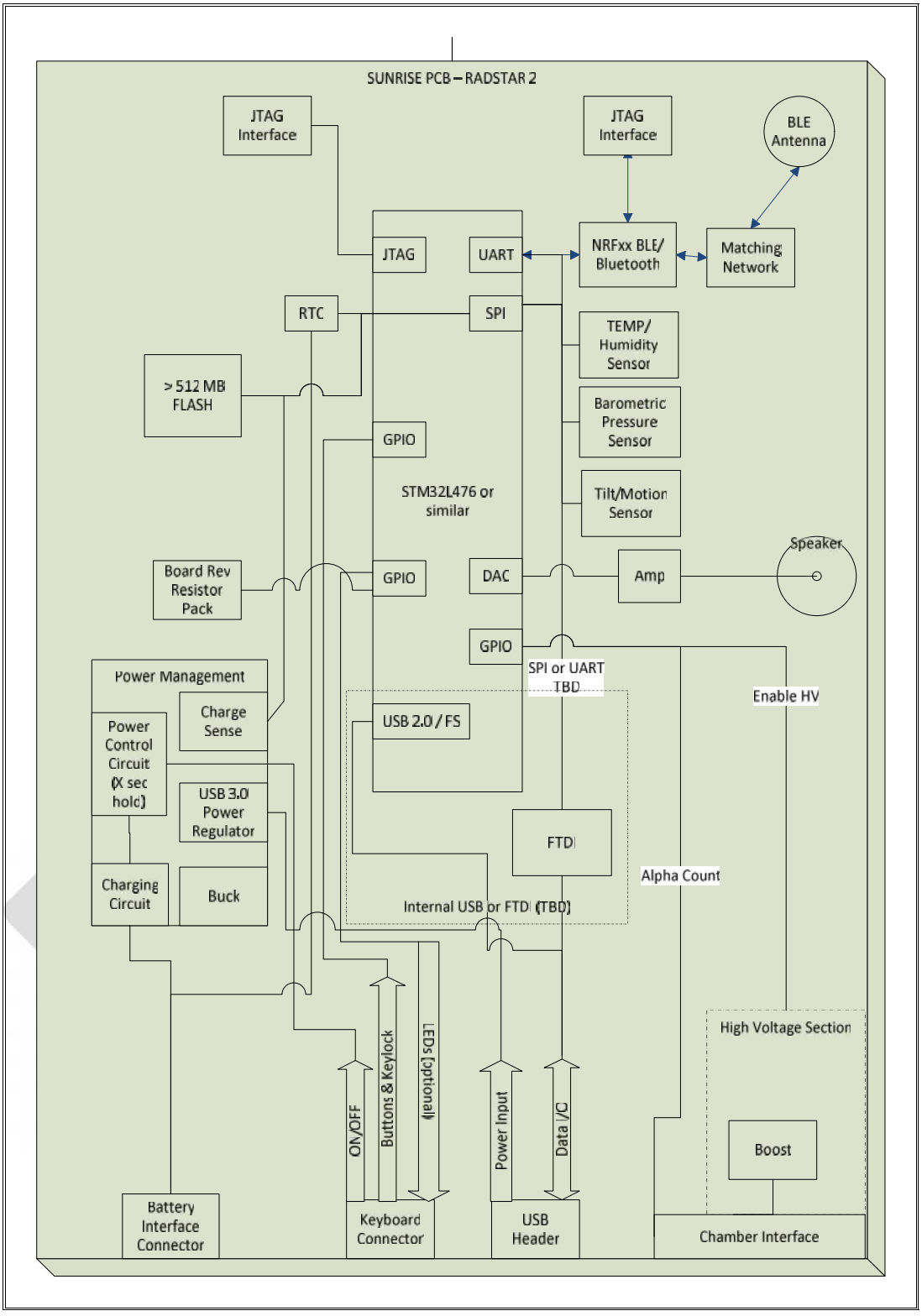

Figure 2 - RS2 Main Board Architecture

5 Electronic Detailed Design

Sunrise will draw upon our existing IP to efficiently create the schematic. Existing design blocks we are planning on using include:

- Nordic-based BLE design include matching network and antenna.
- STM32L476 design with an accelerometer for tilt and motion detection.
- Audio amplifier design.
- AGM charge controller.
- Various low-voltage power supplies.

The Chamber Interface shall include a high voltage supply. This will boost the battery voltage to TBD volts as required by the chamber. Good high voltage design practices (creepage and clearance, etc.) shall be used. This will impact board layout.

The USB 3.0 Power design will be based around off-the-shelf IC solution. The power negotiation is non-trivial, so using a pre-engineered solution is most efficient. Several manufactures offer USB power solutions.

6 Firmware Architecture Design

The firmware will consist of three layers, hardware access, data link, and the application. The diagram of Figure 3 depicts this.

At the top layer, no embedded operating system is to be employed. The main loop of the application in conjunction with timer interrupts will manage tasks needed to perform the functions of the RS2.

The design of the SWICD Data Link is intended to use data as directed from either the USB or BLE interface, thereby guaranteeing the same response through either interface and maintaining consistency in the application level protocols.

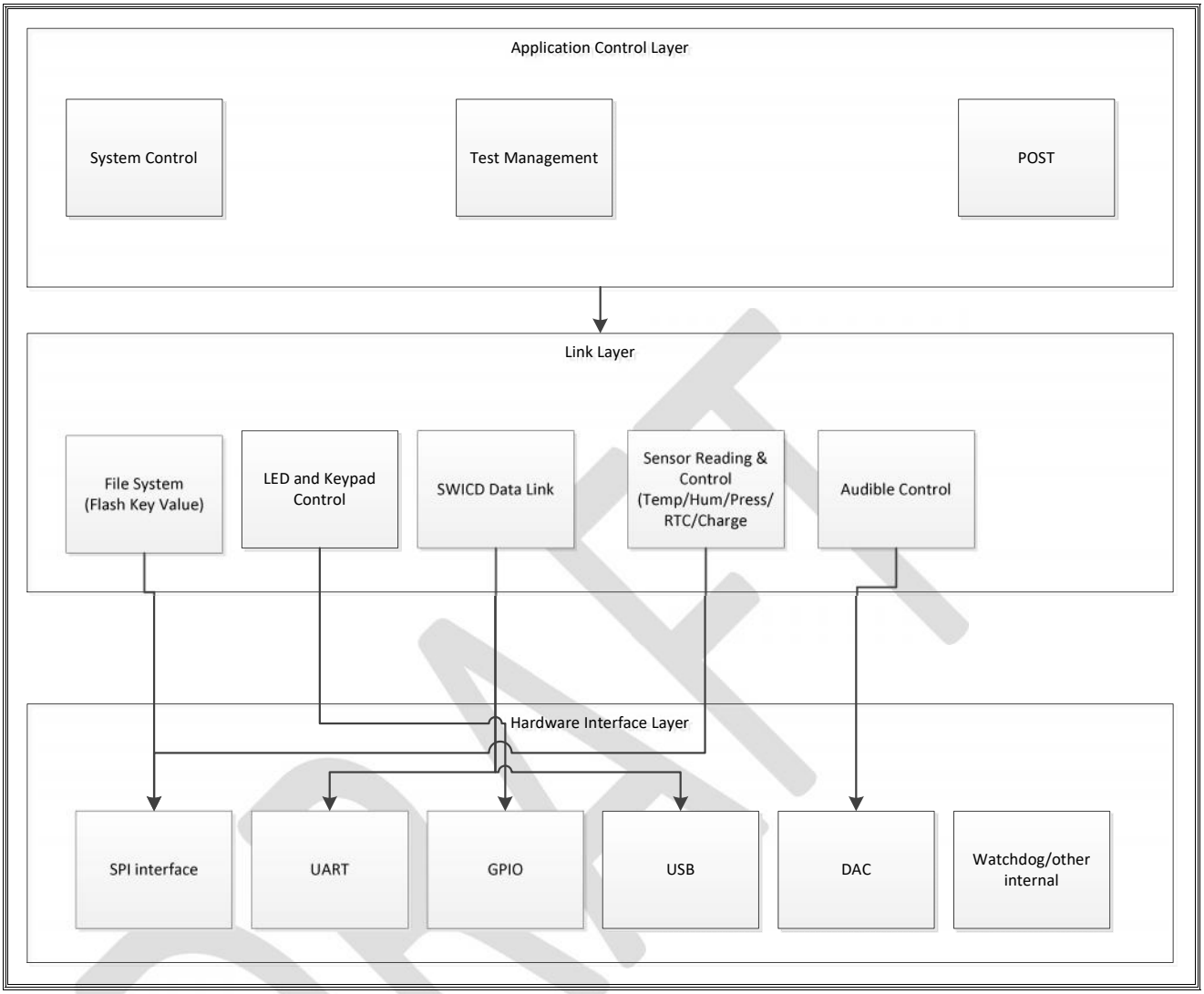

Figure 3 - Firmware Architecture Block Diagram

7 Firmware Detailed Design

7.1 Application Layer

The top layer application will provide overall control of tasks. It will provide initialization/power on self test (POST) and task scheduling for the operation of the RS2.

7.2 Link Layer

The following items detail relate to specific module components of the Link Layer of the firmware.

7.2.1 File System (Data Store)

The storage of data will be controlled through the Sunrise Flash Key Value (FKV) file management design. This design is a block based mechanism tailored for known size block writes to flash. It will be modified to support the underlying API read/writes for the Flash device of the HAL layer.

7.3 Hardware Interface Layer (HAL)

SPI devices

7.4 Data Design

This section explains how the information on your system transforms into data structures. Describe the data entities are stored, processed, and organized.

8 Revision History

Revision	Change Description	Author	Date
001	Initial Release		yyyy-mm-dd
002	<table><tr><td>IMPACTS:</td><td>Yes/No</td></tr><tr><td>Does this change impact other requirement documents?</td><td></td></tr><tr><td>Indicate a weakness in the QMS that should be addressed?</td><td></td></tr><tr><td>Does this change require training?</td><td></td></tr><tr><td>Impact test procedures?</td><td></td></tr><tr><td>Does this change require verification testing?</td><td></td></tr><tr><td>Impact the Hazard Analysis?</td><td></td></tr><tr><td>Impact the BOM?</td><td></td></tr><tr><td>Impact prototype parts inventory or ordering?</td><td></td></tr></table>		