Buffalo-B Product Specification

Product:	Buffalo / Bluetooth 4.2BLE module
Module name:	Buffalo-B
Version:	VER 1.2
Vendor:	Suzhou Pairlink Network Technology Co.,Ltd.
TEL:	
Address:	Room 117, No.55, Su hong xi Road, Suzhou Industrial
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Revision History

Data	Revision	Change Description
2017/04/17	1.0	Initial release
2017/06/02	1.1	Add 3.3.1 PCB-Antenna Characteristics
		1:Modify Bluetooth Core Version
		Add Note 1
		2:Modify Packing Information
2018/08/08	1.2	Add 9.3: Label Information

Note 1: ST released new Stack which is Bluetooth Core V4.2 in June 2018.Buffalo-B has upgraded. But this Stack didn't support the feature "LE Data Length Extension".

FEATURES

- Bluetooth specification compliant master, slave and multiple roles simultaneously, single-mode Bluetooth low energy system-on-chip
- Operating supply voltage: from 1.7 to 3.6V
- Integrated linear regulator and DC-DC step-down converter
- Operating temperature range: -40 °C to 105 °C
- High performance, ultra-low power Cortex-M0 32-bit based architecture core
- High performance, ultra-low power
 Cortex-M0 32-bit based architecture core
- Programmable 160 KB Flash
- 24 KB RAM with retention (two 12 KB banks)
- 1 x UART interface
- 1 x SPI interface
- 2 x I2C interface
- 15 GPIO
- 2 x multifunction timer
- 10-bit ADC
- Watchdog & RTC
- 2 x PWM source
- DMA controller

- PDM stream processor
- 16 or 32 MHz crystal oscillator
- 32 kHz crystal oscillator
- Battery voltage monitor and temperature sensor
- Up to +8 dBm available output power (at antenna connector)
- Excellent RF link budget (up to 96 dB)
- Accurate RSSI to allow power control
- 8.2 mA maximum TX current (@ 0 dBm, 3.0 V)
- Down to 3uA current consumption with active BLE stack (sleep mode)
- Package type:20.5*14.0*2.4mm FR4 PCB

APPLICATIONS

- Automotive product
- Watches
- Fitness, wellness and sports
- Consumer medical
- Remote control
- Home and industrial automation
- Assisted living
- Lighting

1. Functional Characteristics

Buffalo-B is a Soc module developed based on the Bluetooth 4.2 standards. the internal integration architecture Corrtex-M0 processor. It has the advantage of small volume, low power consumption, long distance transmission, strong anti-jamming capability, low cost. Specifically applied to bluetooth low power control area, and suitable for various occasions short distance wireless communication.

Buffalo-B integral compact, simplifies the design in hardware and institution for user. The module interface open completely to make the users has more flexible secondary development space.

Buffalo-B is a Bluetooth Low Energy module with 25 pads located around the perimeter. Primary component on the module is the ST_BlueNRG-1 which is a Bluetooth 4.2 compliant basic rate single-chip. The baseband and radio have been integrated into a single chip implemented in standard digital CMOS. Block diagram of the module is shown in Figure 1.

Buffalo-B Supported Pairlink BLE Mesh Protocol. Suitable for IOT systems.

Buffalo-B Supported Pairlink UART Protocol. Suitable all kinds of wireless system.

Pairlink provide APK/APP software product design and development at the same time.

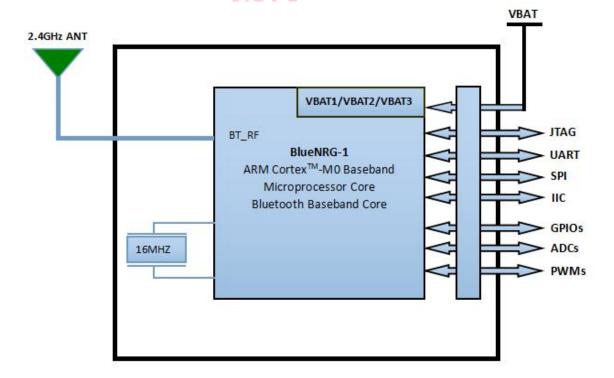


Figure 1:Block Diagram

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2. Module Interface Description

2.1. Pin Assignment and Pin Description

Buffalo-B Pin definition can refer to Figure 15.

Table 1: Module Pin Description

Pin Number	Pin Name	1/0	Alternate Function Description
10	VBAT	VBAT	Power Supply
3,6,16,25	GND	GND	Connect to Ground
11	RESET	I	System Reset
5	DIO7/BOOT	I/O	Bootloader Pin
1	XTALO	1	• 32kHz crystal
2	XTALI	I	• 32kHz crystal
4	DIO6	1/0	• GPIO: P6
7	DIO9	1/0	• GPIO: P9
8	DIO10	1/0	• GPIO: P10
9	DIO14	0	• GPIO: P14
12	ADC1	1 (• 10bit ADC input: ADC1
13	ADC2	W	• 10bit ADC input: ADC2
14	DIO13	0	GPIO: P13 OD structure
15	DIO12	0	• GPIO: P12 OD structure
17	DIO0	1/0	• GPIO: P0
18	DIO11_RX	1/0	• GPIO: P11 • UART_RX
19	DIO8_TX	1/0	• GPIO: P8 • UART_TX
20	DIO5	1/0	• GPIO: P5 • I2C2_DAT
21	DIO4	1/0	• GPIO: P4 • I2C2_CLK
22	DIO3	1/0	• GPIO: P3
		., 0	• SPI_IN • PWM1
23	DIO2	1/0	• GPIO: P2 • SPI_OUT • PWM0
	5.04		• GPIO: P1
24	DIO1	1/0	• SPI_CS

2.2. GPIO Description

2.2.1. GPIO Introduction

The Buffalo-B offers 15 GPIOs.

The programmable I/O pin can be configured for operating as:

- Programmable GPIOs
- Peripheral input or output line of standard communication interfaces
- 2 PWM sources (PWM0 and PWM1 independently configurable) and 4 PWM output pins (IO2, IO3, IO4 and IO5).
- 5 wakeup sources from standby and sleep mode
- Each I/O can generate an interrupt independently to the selected mode. Interrupts are generated depending on a level or edge

2.2.2. GPIO Functional Description

In the table below is reported the GPIO configuration table where at each IO pin is associated the related functions.

Pin name	GPIO 1	GPIO mode "000"		Mode serial1 '001"		Mode serial0 '100'		Microphone/ADC mode '101'		
name	Type	Signal	Туре	Signal	Туре	Signal	Туре	Signal		
100	1/0	GPIO 0	1	UART_CTS	1/0	SPI_CLK	-	, s		
101	1/0	GPIO 1	0	UART_RTS	1/0	SPI_CS1	E	PDM_DATA		
102	1/0	GPIO 2	0	PWM0	0	SPI_OUT	0	PDM_CLK		
IO3	1/0	GPIO 3	0	PWM1	1	SPI_IN	0	ADC_CLK		
104	1/0	GPIO 4	ı	UART_RXD	1/0	I2C2_CLK	0	PWM0		
105	1/0	GPIO 5	0	UART_TXD	I/O	I2C2_DAT	0	PWM1		
106	1/0	GPIO 6	0	UART_RTS	I/O	12C2_CLK	I	PDM_DATA		
107	I/O	GPIO 7	1	UART_CTS	1/0	I2C2_DAT	0	PDM_CLK		
108	1/0	GPIO 8	0	UART_TXD	1/0	SPI_CLK	Ę	PDM_DATA		
109	1/0	GPIO 9	1	SWCLK	1	SPI_IN	-	· ×		
1010	1/0	GPIO 10	4	SWDIO	0	SPI_OUT	853	5		
1011	1/0	GPIO 11	1	UART_RXD	1/0	SPI_CS1	1527	-		
1012	OD	GPIO 12	Ĩ	5	1/0	I ² C1_CLK) -	NT		
1013	OD	GPIO 13	1	UART_CTS	1/0	I ² C1_DAT	1127	-		
1014	I/O	GPIO 14	1/0	I2C1_CLK	1/0	SPI_CLK	0	ADC_DATA		

Table 2: IO Functional Map

2.2.3. GPIO Interrupts

Each IO in GPIO mode can be used as interrupt source from external signal. The trigger event is both edge and level sensitive according to configuration. All the configuration are reported in table below.

Table 3: GPIO Interrupts modes

CE	Interrupt mode						
Configuration	Falling edge	Rising edge	Both edges	Low level	High level		
IOIS	0	0	0	1	1		
IOIBE	0	0	1	NA	NA		
IOIEV	0	1	NA	0	1		

2.2.4. GPIO Characteristics

By default all the GPIO pins are configured as input with related pull-up or pull-down resistor enabled according to table below.

Table 4: GPIO Characteristics

Name	Туре	Buffer strength	Pull-up / pull-down availability	Reset state
100	I/O	2 / 4 mA	Pull-down	Input pull-down
IO1	I/O	2 / 4 mA	Pull-down	Input pull-down
102	I/O	2 / 4 mA	Pull-down	Input pull-down
IO3	I/O	2 / 4 mA	Pull-down	Input pull-down
IO4	I/O	2 / 4 mA	Pull-down	Input pull-down
105	I/O	2 / 4 mA	Pull-down	Input pull-down
IO6	I/O	2 / 4 mA	Pull-down	Input pull-down
DIO7	I/O	2 / 4 mA	Pull-down	Input pull-down
IO8	I/O	2 / 4 mA	Pull-down	Input pull-down
109	I/O	2 / 4 mA	Pull- up	Input pull-up
IO10	I/O	2 / 4 mA	Pull- up	Input pull-up
IO11	I/O	2 / 4 mA	Pull-up	Input pull-up
IO12	I/O	10 mA	No pull	Input
IO13	I/O	10 mA	No pull	Input
IO14	I/O	2 / 4 mA	Pull-down	Input pull-down

Table 12:IO Pull Values

Name	Description name	Min.	Тур.	Max.	Unit	
Digital inpu	ut and output when 1.8 V supply.					
RPD	Pull-down value	117	202	363	40	
RPU	Pull-up value	135	211	334	kΩ	

3. Module Specification

3.1. Electrical Characteristics

Table 5: Recommended Operating Conditions

Symbol	Parameter	Value	Unit
VBAT	Operating battery supply voltage	1.7 to +3.6	V
TA	Operating Ambient temperature range	-40 to +105	${\mathbb C}$
	Operating Ambient temperature range	-40 to +105	${\mathbb C}$
	For automotive grade level		~ 0.7

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to TA = 25 $^{\circ}$ C, VBAT = 3.0 V. All performance data are referred to a 50 $^{\circ}$ C PCB antenna.

Table 6: Electrical Characteristics

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Power co	nsumption whe	n DC-DC converter active				
		Reset		5		nΑ
		Standby		500		nA
		Sleep mode: 32 kHz XO ON (24 KB retention RAM)		0.9		
		Sleep mode: 32 kHZ RO ON (24 KB retention RAM)		2.1		μА
		Active mode: CPU, Flash and RAM on		1.9		mA
		RX		7.7		mA
I _{BAT}	Supply current	TX +8 dBm		15.1		
Current		TX +4 dBm		10.9		
		TX +2 dBm		9]	
		TX -2 dBm		8.3		A
		TX -5 dBm		7.7		mA
		TX -8 dBm		7.1		
		TX -11 dBm		6.8		
		TX -14 dBm		6.6		

3.2. Absolute Maximum Ratings

Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referred to GND.

Table 7: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
VBAT	DC voltage for Buffalo-B	-0.3 to +3.9	V
TSTG	Storage temperature range	-40 to +125	${\mathbb C}$
VESD-HBM	Electrostatic discharge voltage	±2.0	KV
Current	Current consumption @ 3.0V	0~20	mA

3.3. RF General Characteristics

Characteristics measured over recommended operating conditions unless otherwise specified. Typical value are referred to TA = 25 $^{\circ}$ C, VBAT =3.0 V. All performance data are referred to a 50 Ω PCB antenna.

Table 8: RF Transmitter Characteristics

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
MOD	Modulation scheme			GF	SK	X32
ВТ	Bandwidth-bit period product			0.5		
Mindex	Modulation index			0.5	2	
DR	Air data rate		(S	1		Mbps
PMAX	Maximum Output Power	At antenna connector		+8	+10	dBm
PRFC	Minimum Output Power		02	-15		dBm
PBW1M	6 dB Bandwidth for modulated carrier (1 Mbps)	Using resolution bandwidth of 100kHz	500			kHz
PRF1	1 st Adjacent channel transmit power 2 MHz	Using resolution bandwidth of 100 kHz and average detector		-35		dBm
PRF2	2 nd Adjacent channel transmit Power >3MHz	Using resolution bandwidth of 100 kHz and average detector		-40		dBm
ZLOAD	Optimum differential load	@ 2440 MHz		25.4 + j20.8°		Ω

Table 9: Buffalo-B RF Performance

Parameter	Channel	AVG Output	Frequency Accuracy	RX Sensitivity
		Power(dBm)	(KHz)	(PER<30.8 %)
Buffalo-B	CH 0(2402MHz)	-3.21	2401.734	-85dBm
(-2dBm)	CH 19(2440MHz)	-3.52	2439.734	-85dBm
	CH 39(2480MHz)	-3.80	2479.734	-84dBm
Buffalo-B	CH 0(2402MHz)	-0.79	2401.734	-85dBm
(0dBm)	CH 19(2440MHz)	-1.11	2439.734	-85dBm
V	CH 39(2480MHz)	-1.34	2479.734	-84dBm
Buffalo-B	CH 0(2402MHz)	7.64	2401.734	-85dBm
(8dBm)	CH 19(2440MHz)	7.77	2439.734	-85dBm
	CH 39(2480MHz)	7.74	2479.734	-84dBm

3.3.1. PCB-Antenna Characteristics

Figure 2: Antenna Characteristics

Frequency (Hz)	Efficiency	Gain (dBi)
2400000000	32%	-0.41
2410000000	29%	-0.92
2420000000	26%	-1.41
2430000000	25%	-1.46
2440000000	23%	-1.51
2450000000	22%	-1.73
2460000000	20%	-1.86
2470000000	20%	-1.74
2480000000	19%	-1.94

Radiation Pattern and Gain were dependent on measurement Buffalo-B PCB design.

Figure 3: E1 plane

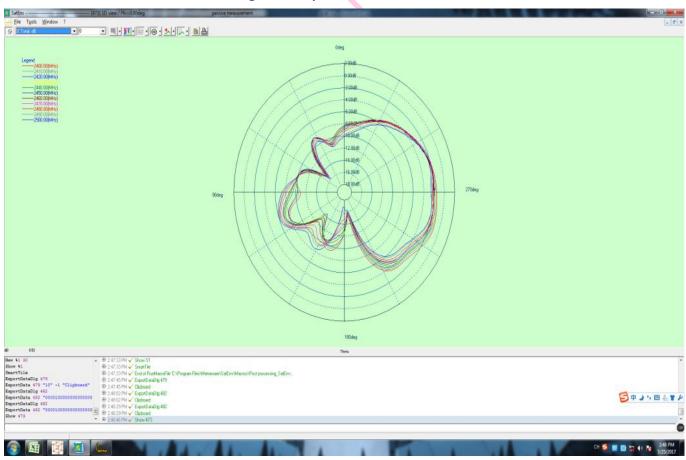


Figure 4: E2 Plane

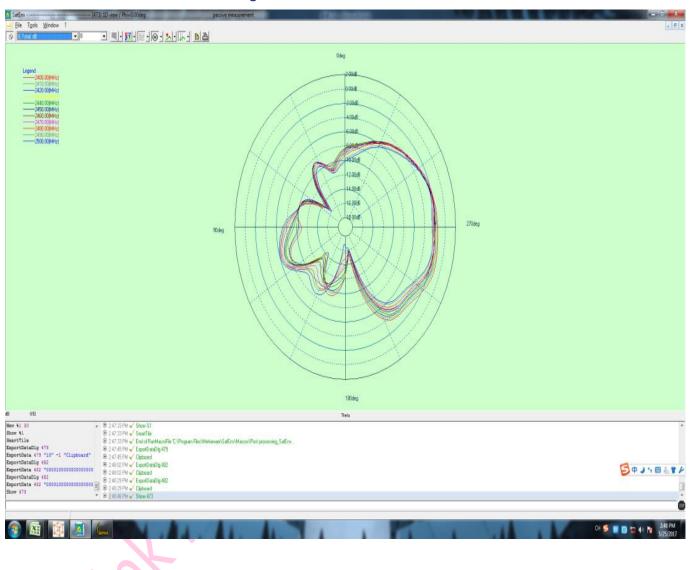


Figure 5: H Plane

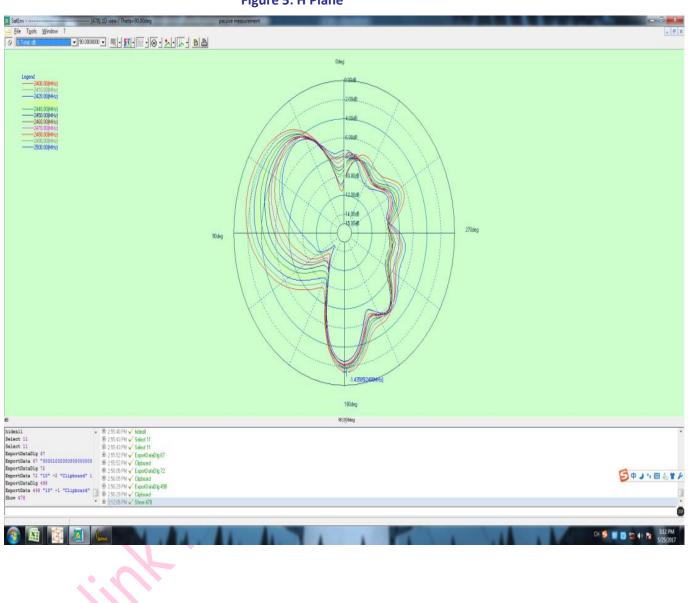
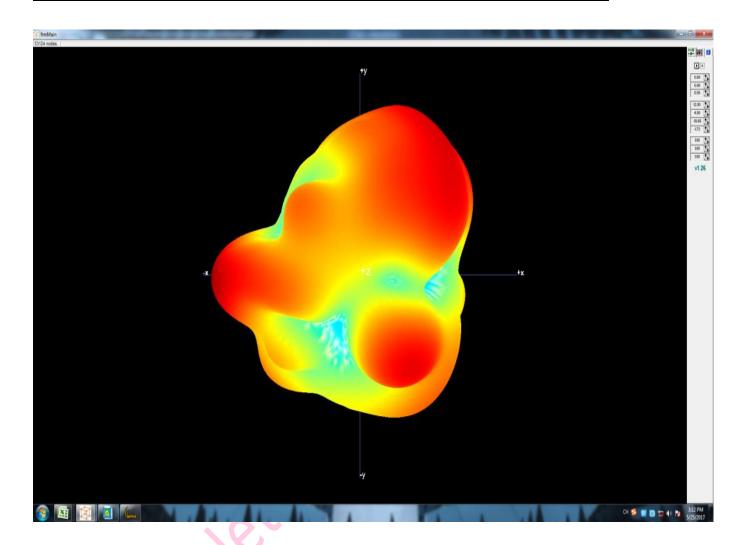


Figure 6: X-Y scheme



3.4. Power Management

The Buffalo-B integrates both a low dropout voltage regulator (LDO) and a step-down DC-DC converter to supply the internal Buffalo-B circuitry.

The Buffalo-B most efficient power management configuration is with DC-DC converter active where best power consumption is obtained without compromising performances. Nevertheless, a configuration based on LDO can also be used, if needed.

A simplified version of the state machine is shown below.

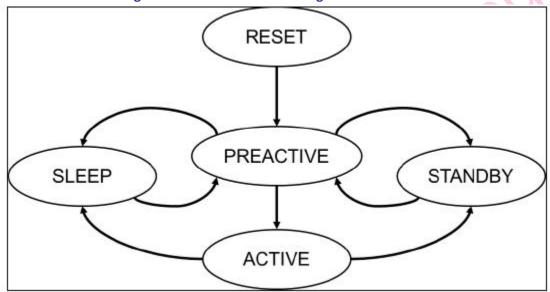


Figure 7: Buffalo-B Power Management State Machine

3.4.1. States Description

3.4.1.1 Preactive State

The preactive state is the default state after a POR event.

In this state:

- All the digital power supplies are stable.
- The high frequency clock runs on internal fast clock RC oscillator (16 MHz).
- The low frequency clock runs on internal RC oscillator (32.768 kHz).

3.4.1.2 Active State

In this state:

The high frequency runs on the accurate clock (16 MHz \pm 50 ppm) provided by the external XO. The internal fast clock RO oscillator is switched off.

3.4.1.3 Standby State

In this state:

Only the digital power supplies necessary to keep the RAM in retention are used.

The wake-up from this low power state is driven by the following sources:

- IO9
- IO10
- IO11
- IO12
- IO13

If they have been programmed as wake-up source in the system controller registers.

3.4.1.4 Sleep State

In this state:

Only the digital power supplies necessary to keep the RAM in retention are used.

The low frequency oscillator is switched on.

The wake-up from this low power state is driven by the following sources:

- 109
- IO10
- IO11
- IO12
- IO13

If they have been programmed as wake-up source in the system controller registers and from the internal timers of the BLE radio.

3.5. Buffalo-B Power-On Sequence

Buffalo-B is provided with an automatic Power-On Reset (POR) circuit which is designed to generate a RESETN active (low) level for a time TRESET after the VBAT reaches the Reset Release Threshold voltage VRRT, as shown in Figure 3.

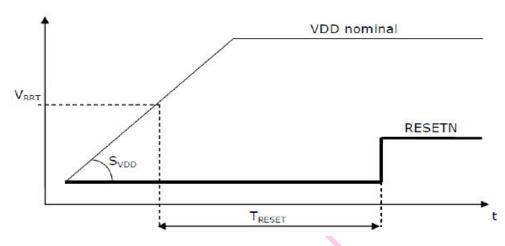


Figure 8: Power-On Sequence

The parameters VRRT and TRESET are fixed by design in order to guarantee a reliable reset procedure of the state machine. Typical and extreme values are reported in Table 10.

Comment Min Symbol Parameter Тур Max Unit Reset Startup Threshold Voltage V_{RRT} 0.5 SVDD Power-on VDD Slope Successfully tested VDD slope region 1.0 V/ms TRESET Reset Pulse Width 0.5

Table 10: Reset Characteristics

3.5.1. Buffalo-B Transition Time

Figure 9:Buffalo-B Transition Time

		•		
Blue	NRG-1 Transition	Times		
Transition	Maximum Time	Condition	(*):	
	1.5 ms	32 kHz not available	- temperature 26 °C	
Reset-active (*)	7 ms	32 kHz RO	- power supply 3.3V - these measurements depend from the HS and	
	94 ms	32 kHz XO		
			LS crystal used on the board, these are worst	
	0.52 ms	32 kHz not available	case.	
Standby-active (*)	6.2 ms	32 kHz RO		
	93 ms	32 kHz XO		
Sleep-active (*)	0.52 ms			
Antius DV	125 µs	Channel change		
Active-RX	61 µs	No channel change		
Active-TX	131 μs	Channel change		
ACLIVE-1X	67 μs	No channel change		
RX-TX or TX-RX	150 μs			

3.6. Reset Management

Figure 5: "Reset and Wakeup Generation" shows the general principle of reset. Releasing the Reset pin puts the chip out of shutdown state. The wakeup logic is powered and receives the POR. Each time the wake-up controller decides to exit sleep or standby modes, it will generate a reset for the core logic. The core logic can also be reset by:

- Watchdog
- Reset request from the processor (system reset)
- LOCKUP state of the Cortex-M0.

The SWD logic is reset by the POR. It is important to highlight that reset pin actually power down chip, so it is not possible to perform debug access with system under reset.

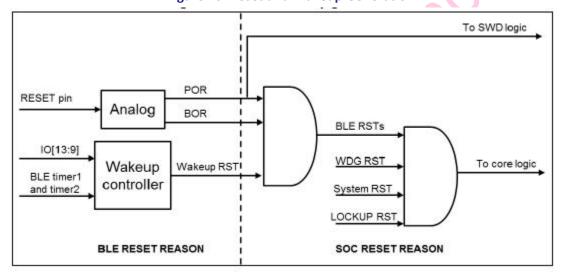


Figure 10: Reset and Wakeup Generation

4. Functional Details

4.2. ADC

4.1.1. Introduction

The Buffalo-B integrates a 10-bit Analog-to-Digital Converter (ADC) for sampling an external signal.

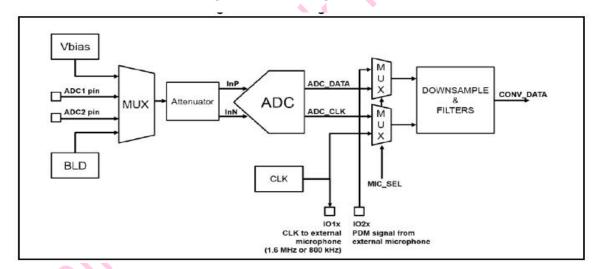
Main features are:

- Sampling frequency 1 MHz
- One channel in single ended or differential input through the pins ADC1 and ADC2
- Battery level conversion
- The conversion are either continuous or single step acquisition
- An integrated digital filter is used to process a PDM data stream from a MEMS microphone

4.1.2. Functional Overview

The Figure 6 below shows a top diagram of the ADC.

Figure 11: Block Diagram of ADC



Several channels are available for conversion, the CHSEL selects the channel according to Table 11

Table 11: ADC Channels

CHSEL	Channels description
0	All switch open. No input
1	Single ended through ADC2 pin. InP = Vbias (internal), InN = ADC2 pin
2	Single ended through ADC1 pin. InP = ADC1 pin, InN = Vbias (internal)
3	Differential ADC1 pin – ADC2 pin. InP = ADC1 pin, InN = ADC2 pin
5	Battery level detector. InN = BLD, InP = 0.6 V (internal)
6	Short. InP = InN = 0.6 V (internal)

The conversion can be single (CONT = 0) or continuous (CONT = 1). In continuous mode, the conversion runs with a preprogrammed sampling rate, while in single step mode the ADC performs a conversion and then stops.

The output data rate depends on DECIM_RATE according to the table below.

Table 12: ADC data rate

DECIM	Output data rate[Ksample/s]
0(2000)	5
1(100)	10
2(64)	15.625
3(32)	31.25

4.1.2.1. ADC Start Conversion

The ADC both analog and digital sub-system are switched on by setting ADCON and SWSTART. The conversion operation consists of four phases.

- 1. The wake-up phase lasts 5 us, is present at the beginning of a single acquisition, with the goal to let the analog system to settle before to start the acquisition.
- 2. If the CALEN is set, a calibration phase is performed. It permits to compensate the offset in the analog part. The conversion status is tracked by SR status register. At the beginning of the conversion the BUSY bit is set and masks any attempt to change CONF, up to the end of the conversion. At end of this conversion, the ENDCAL flag is generated and the OFFSET register is written with the converted offset voltage.
- 3. The acquisition phase is regulated by a timeout depending on the resolution. In this phase, digital filter chain processes the data coming from ADC.

4.1.2.2 ADC Offset

The ADC can correct automatically the offset and the gain error.

To enable the automatic offset correction the CALEN and the OFFSET_UPDATE must be set. The result of the last calibration is stored in the OFFSET register.

The correction of the offset can be also done manually, for example by making a conversion of the internal channel InP = InN = 0.6 V and after that, writing the result of conversion in the OFFSET register.

4.2. UART

4.2.1. Introduction

The Buffalo-B integrates a universal asynchronous receiver/transmitter that support much of the functionality of the industry-standard 16C650 UART.

Main features are:

- Programmable baud rates up to 2 Mbps.
- Programmable data frame of 5, 6, 7 or 8 bits of data.
- Even, odd, stick or no-parity bit generation and detection.
- Programmable 1 or 2 stop bit.
- Support of hardware flow control using CTS and RTS pins.
- Support of software flow control using programmable Xon/Xoff characters
- False start bit detection.
- Line break generation and detection.
- Programmable 8-bit wide, 64-deep transmit FIFO and 12-bit wide (8-bit data and 4-bit status), 64-deep receive FIFO.
- Support for Direct Memory Access (DMA).

4.2.2. Functional Description

The UART performs serial-to-parallel conversion on data asynchronously received from a peripheral device on the UART_RX pin, and parallel-to-serial conversion on data written by CPU for transmission on the UART_TX pin. The transmit and receive paths are buffered with internal FIFO memories allowing up to 64 data byte for transmission, and 64 data byte with 4-bit status (break, frame, parity, and overrun) for receive. FIFOs may be burst-loaded or emptied by the system processor from 1 to 16 words per transfer.

4.2.2.1. Data Transmission or Reception

Data received or transmitted is stored in two 64-byte FIFOs. The receive FIFO has an extra four bits per character for the status information:

- Error bits 8 to 10 are associated with a particular character: break error, parity error and framing error.
- Overrun indicator bit 11 is set when the FIFO is full, and the next character is completely received in the shift register. The data in the shift register is overwritten, but it is not written into the FIFO. When an empty location is available in the receive FIFO, and another character is received, the state of the overrun bit is copied into the received FIFO along with the received character. The overrun state is then cleared.

Table 13: RX FIFO errors

FIFO bit	Function	
11	Overrun indicator	
10	Break error	
9	Parity error	
8	Framing error	
7:0	Received data	

For transmission, data is written into the transmit FIFO. If the UART is enabled, it causes a data frame to start transmitting with the parameters indicated in LCRH TX. Data continues to be transmitted until there is no data left in the transmit FIFO. The BUSY flag in the UARTFR register is set as soon as data is written to the transmit FIFO (that is, the FIFO is non-empty) and remains asserted while data is being transmitted. BUSY is cleared only when the transmit FIFO is empty, and the last character has been transmitted from the shift register, including the stop bits. BUSY can be set even though the UART might no longer be enabled. For each sample of data, three readings are taken and the majority value is kept. In the following paragraphs, the middle sampling point is defined, and one sample is taken either side of it. When the receiver detect a start bit, the receive counter runs and data is sampled on the 8th cycle of that counter in normal UART mode. The start bit is valid if UART RX signal is still low on the eighth cycle of Baud16, otherwise a false start bit is detected and it is ignored. If the start bit is valid, successive data bits are sampled on every 16th cycle of Baud16 (that is 1-bit period later) according to the programmed length of the data characters. The parity bit is then checked if parity mode was enabled. Lastly, a valid stop bit is confirmed if UART_RX signal is high, otherwise a framing error has occurred. When a full word is received, the data is stored in the receive FIFO, with any error bits associated with that. The UART character frame is shown in Figure 7: "UART character frame" below.

start bit 5 to 8 data bits parity bit if enabled stop bits

Figure 12: UART Character Frame

4.3. SPI

4.3.1. Introduction

The Buffalo-B integrates a serial peripheral interface compatible with Motorola standard.

Main features are:

- Maximal supported baud rate is 1 MHz in slave mode and 8 MHz in master mode.
- Parallel-to-serial conversion on data written to an internal 32-bit wide, 16-location deep transmitter FIFO.
- Serial-to-parallel conversion on received data, buffering in a 32-bit wide 16-location deep receive FIFO.
- Programmable data frame size from 4-bit to 32-bit.
- Programmable clock bit rate and prescaler.
- Programmable clock phase and polarity in SPI mode.
- Support for Direct Memory Access (DMA).

4.3.2. Functional Overview

The SPI performs serial-to-parallel conversion on data received from a peripheral device on the SPI_RX pin, and parallel-to-serial conversion on data written by CPU for transmission on the SPI_TX pin.

The transmit and receive paths are buffered with internal FIFO memories allowing up to 16 x 32-bit values to be stored independently in both transmit and receive modes. FIFOs may be burst-loaded or emptied by the system processor or by the DMA, from one to eight words per transfer. Each 32-bit word from the system fills one entry in FIFO. The SPI includes a programmable bitrate clock divider and prescaler to generate the serial output clock signal from the SPI CLK pin.

4.3.2.1. Procedure for Enabling SPI

The SPI initialization procedure is the following (assuming clocks already enabled):

- 1. Clear the SSE bit in the CR1 register. This step is not required after a hardware or software Reset of the Buffalo-B.
- 2. Empty the receive FIFO. This step is not required after a hardware or software Reset of the device Buffalo-B.
- 3. Program IO_MODE to route SPI port signals on those GPIOs. See Section GPIO operating modes.
- 4. Program the SPI clock prescaler register (CPSR), then program the configuration registers CRO and CR1.
- 5. The transmit FIFO can optionally be filled before enabling the SPI.
- 6. Set the SSE bit to enable SPI operation.

4.3.2.2. SPI bit Rate Generation

The SPI bitrate is derived by dividing down the peripheral clock (CLK) by an even prescaler value CPSDVSR from 2 to 254, the clock is further divided by a value from 1 to 256, which is 1+SCR. The SPI frequency clock duty cycle is always 0.5.

4.3.2.3. SPI Data Endianness

All transfers can be sent and received with configurable endianness according the setting of the (T/R)ENDN bit in the CR1 registers. The cases "00b" and "11b" of TENDN and RENDN are implemented for data frame size from 4- to 32-bit. The cases "01b" and "10b" of TENDN and RENDN are implemented only for the following data frame sizes: 16-bit, 24-bit and 32-bit. Transmit data endianness:

TENDN in CR1:

Table 14: SPI TX Endianness

TENDN	Endianness
00b	The element is transmitted MSByte-first and MSbit-first.
01b	The element is transmitted LSByte-first and MSbit-first.
10b	The element is transmitted MSByte-first and LSbit-first.
11b	The element is transmitted LSByte-first and LSbit-first.

Table 15: SPI RX Endianness

RENDN	Endianness	
00b	The element is received MSByte-first and MSbit-first.	
01b	The element is received LSByte-first and MSbit-first.	
10b	The element is received MSByte-first and LSbit-first.	
11b	The element is received LSByte-first and LSbit-first.	

4.4. IIC

4.4.1. Introduction

The Buffalo-B integrates two I2C controllers. The I2C controller is an interface designed to support the physical and data link layer according to the I2C standard revision 3.0 and provides a low-cost interconnection between ICs.

Main features are:

- Up to 400 Kb/s in fast mode and up to 100 Kb/s in standard mode.
- Operating modes supported are master mode, slave mode, master/slave mode for multi-master system with bus arbitration.
- Programmable 7-bit or 10-bit addressing (also with combined formats).
- Programmable start byte procedure.
- 16-byte depth RX FIFO and 16-byte depth TX FIFO.
- Spike digital filtering on the SDA and SCL lines.
- Control timing constraint defined by the I2C standard.
- Support for Direct Memory Access (DMA).

4.4.2. Functional Description

Two wires, serial data (SDA) and serial clock (SCL) carry information between the devices connected to the bus. Each device has a unique address and can operate as either a transmitter or receiver, depending on the function of the device. A master is the device that initiates a data transfer on the bus and generates the clock signal. Any device addressed is considered at that time a slave. The I2C bus is a multi-master bus where more than one device is capable of controlling the bus. This means that more than one master could try to initiate a data transfer at the same time. The arbitration procedure relies on the wired-AND connection of all I2C interfaces to the I2C bus. If two or more masters try to put information onto the bus, the first to produce a 'one' when the other produces a 'zero' will lose the arbitration. The clock signals during arbitration are a synchronized combination of the clocks generated by the masters using the wired-AND connection to the SCL line. Generation of clock signals on the I2C bus is always the responsibility of master devices; each master generates its own clock signals when transferring data to the bus. Bus clock signals from a master can only be altered when they are stretched by a slow slave device holding down the clock line, or by another master when arbitration occurs.

Two modes:

- Standard mode with bit rate up to 100 Kb/s
- Fast mode with bit rate up to 400 Kb/s

4.4.2.1. IIC Configuration

Following a Reset, the I2C logic is disabled and must be configured when in this state.

The control register (CR) and baud rate register (BRCR) need to be programmed to configure the following parameters of the peripheral:

- Master or slave.
- 7- or 10-bit addressing mode
- Speed mode
- Clock rate

Then, if in master mode, the MCR register is used to define the transaction:

- Read or write.
- Slave addresses (7- or 10-bit) to communicate with.
- Addressing a 7- or 10-bit slave address.
- Stop condition, to generate a stop or restart condition at the end of the transaction (for consecutive transactions).
- Transaction length

5. Reference Design

The most recent schematic and design example, bill of material, and layout file are available from Pairlink Network Technology Co., Ltd. Contact us for details.

GND . Ll Y1 32.768KHz PL-Buffalo_B XTALO XTALI 3 SPI OUT SPI IN DIO6 TOOR DIO7/BOOT GND UART TX DIO9 DIO9_SWCLK UART_RX DIO10 SWDIO DIO11_RX SPI CLK DIO14 VBAT 1.70V≤VBAT≤3.60V RESET Section C WAKEUP SOURCE 3M R6 Section B: BATTARY_DET GNI

Figure 13: Module Reference Design

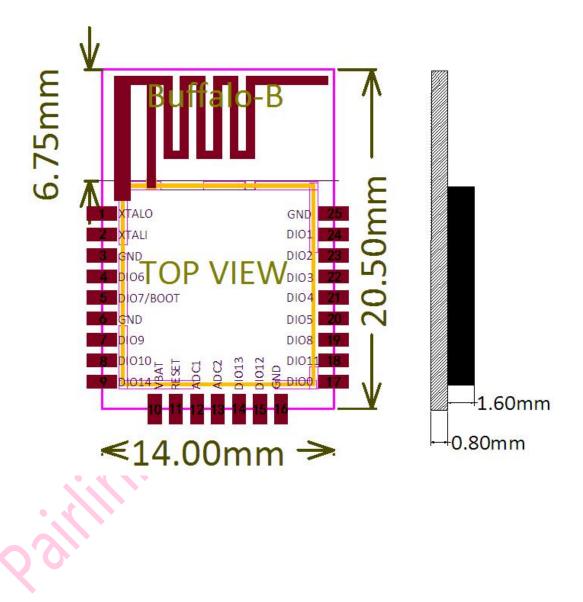
Circuit Description:

- 1: If the HW IIC function is selected, external pull-up resistors are needed.
- 2: Pin12(ADC1) and Pin13(ADC2) are ADC sampling interface.
- 3: There are two ways can wakeup module when Buffalo in deep sleep mode.
 - A). Wakeup from IO9, IO10, IO11, IO12, IO13.
 - B). Wakeup from internal timer: BLE timer 1 or BLE timer 2.
- 4: GPIO12 and GPIO13 are OD structure, needs to add pull-up resistor when use.
- 5: DIO7 multiplexing BOOT function. Buffalo will into BOOT mode when user pull-up DIO7 at power on.
- 6: Pin22 and Pin23 multiplexing for hardware PWM function.when user to use PWM interface and SPI interface at the same time, ask Pairlink to get a reasonable configuration.
- * 7: Section A:If the RTC function is selected, external 32.768K Crystal is needed
- * 8: Section B:Battery Detect.
- * 9: Section C:Interface J1 for debugging, user can select and reserve.
- * 10: Section D:If the noise of power is big, a external electrolytic capacitor(≥22uF) is needed.
- 11: Pin RESET L vacant or connect to the host.Don't be an external capacitor and resistor.

6. Appearance and Dimensions

Figure 9 shows the size of the module. The components and prominent structure are not allowed put in this size range (20.5 mm*14.0 mm*2.40 mm),

Figure 14: Module Appearance



7. Recommended Land Pattern

The following land pattern size is recommended for user board design. However, user can modify it according PCB soldering conditions. Sufficient examination is necessary if use the modified land pattern.

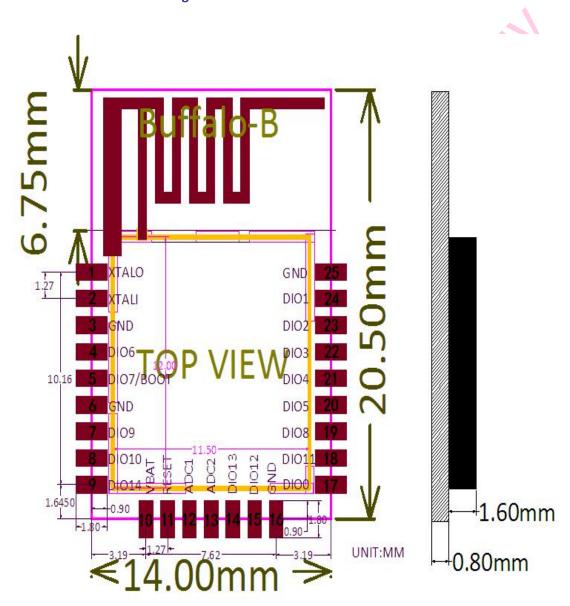
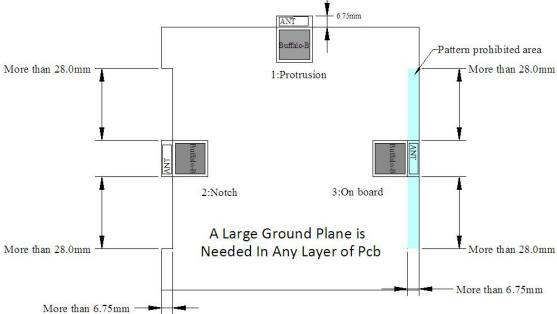


Figure 15: Mechanical Information

8. Module Layout Guideline

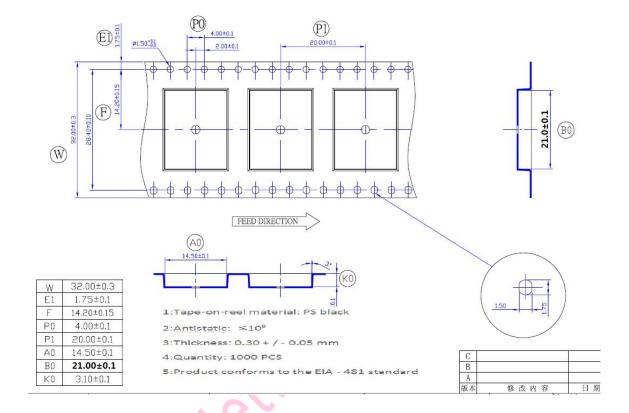
The layout on user PCB should be designed according to the following guidelines.

Figure 16: Module Placement

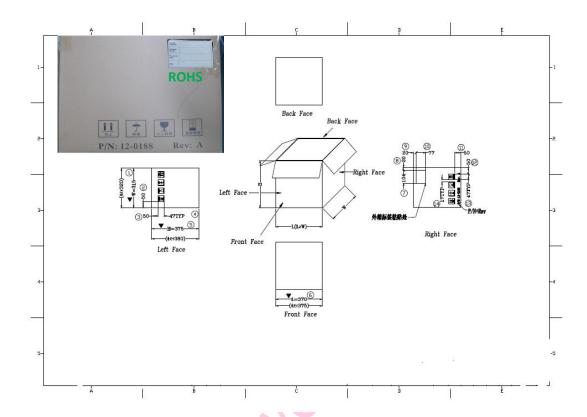


9. Packing Information

9.1. Rolling Information

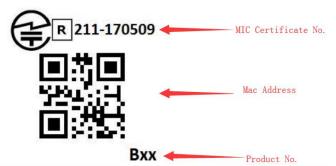


9.2. Master Carton Information

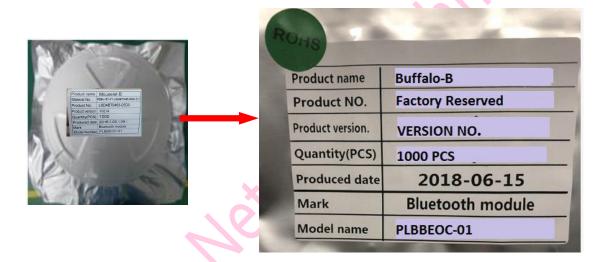


9.3. Label Information

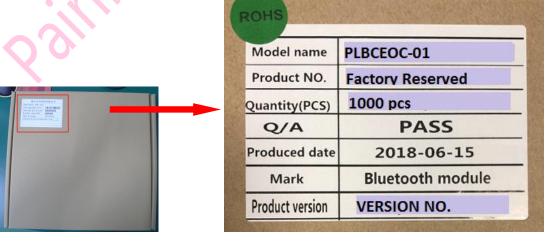
A) Label on module



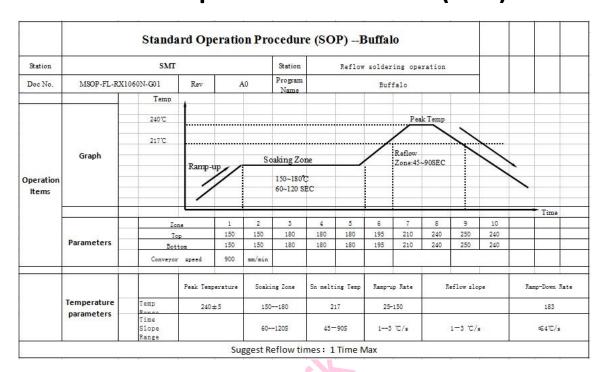
B) Label on vacuum bag



C) Label on box



10. Standard Operation Procedure (SOP)



This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Caution: Any changes or modifications to this device not explicitly approved by manufacturer could void your authority to operate this equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

The device has been evaluated to meet general RF exposure requirement This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.

This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.