SYNIC®
Intelligent Wireless

Data Sheet

Module name：IA9QH5 S83D-F Module

Project Code：SMMSBRQHC58RH4

Version 0.2

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Syncomm Technology Corp.

10F., No. 101, Sec. 2, Gongdao 5th Rd., East Dist., Hsinchu City, Taiwan, R.O.C.
Tel: +886-3-5169188
Fax: +886-3-5169111
http://www.syncomm.com.tw

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1. Features

- 5.2GHz/5.8GHz ISM Band
- GFSK modulation
- Low BOM cost
- Long distance > 30m (Line of sight)
- Support 1-1 duplex mode or 1-N broadcasting mode
- Digital I2S audio interface
- Support no audio detection function
- Support compression/un-compression mode
- Antenna diversity
- Short delay time variation
- Audio format 16/24bit , 32/44.1/48K/96KHz sampling rate
- Robust Packet error correction
- Low power consumption
- No RF induced audio noise
- Audio latency time < 20ms
  (Programmable according customized spec.)

2. Application

- Wireless HTiB Rear Speaker
- Wireless Outdoor Speaker
- Wireless TV theater
- Wireless Audio Sender
- Wireless Headphone
- Wireless Stereo Ear Microphone

3. RF Specification

Item	Min	Typ	Max	Unit	Note
Channel Range	5160	—	5240	MHz	
-20dB bandwidth	—	2.7	—	MHz	2M Mode
RF Output Power		12		dBm	Peak power at Antenna port
Sensitivity	—	-91	—	dBm	The smaller, the better

Table 1 5.2GHz RF Specification

Item	Min	Typ	Max	Unit	Note
Channel Range	5735	—	5840	MHz	
-20dB bandwidth	—	3	—	MHz	2M Mode
RF Output Power		12		dBm	Peak power at Antenna port
Sensitivity	—	-90	—-	dBm	The smaller, the better

Table 2 5.8GHz RF Specification

4. Audio Specification

2.1 CH						
	Item	Min	Typ	Max	Unit	Note
2.0 CH	SNR	90	94	—	dBr	@1kHz
	THD + N	—	-80	-75	dB	@1kHz, the smaller, the better
	Frequency Response	20	—	20k	Hz	@±1dB
	Dynamic range	90	94		dB	@1kHz
0.1 CH	SNR	90	94		dBr	@1kHz
	THD + N		-84	-80	dB	@1kHz, the smaller, the better
	Frequency Response	20		5k	Hz	@±3dB
	Dynamic range	90	94		dB	@1kHz

Note: Test condition is that using Card type EVB board with ADC: AK5357 at master mode and DAC: AK4386 at master mode.

Table 3 ADC to DAC

2.1 CH						
	Item	Min	Typ	Max	Unit	Note
2.0 CH	SNR	135	140		dBr	@1kHz
	THD + N		-100	-95	dB	@1kHz, the smaller, the better
	Frequency response	20		20k	Hz	@±1dB
	Dynamic range	95	100		dB	@1kHz
0.1 CH	SNR	130	135		dBr	@1kHz
	THD + N		-100	-95	dB	@1kHz, the smaller, the better
	Frequency response	20		5k	Hz	@±3dB
	Dynamic range	95	100		dB	@1kHz

Note: Test condition is that using sample rate 48 kHz, NFsCLK factor 512 and resolution 24.

Table 4 I2S to I2S

5. Electrical Specification

Item	Min	Typ	Max	Unit	Note
Power Supply Voltage	3.0	3.3	3.6	V	
Operating Temperature	0	25	55	℃	
2.1CH Audio Mode					
Consumption Current (TX_MODE)		210		mA	RF Power :11dBm
Consumption Current (RX_MODE)		100		mA	No GPIO driving
0.1CH Audio Mode					
Consumption Current (TX_MODE)		130		mA	RF Power :11dBm
Consumption Current (RX_MODE)		86		mA	No GPIO driving

Table 5

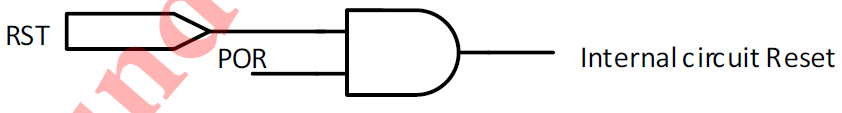
Item						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
V_{IH}	Input High Threshold	2.0	—	3.33	V	LDO_OUT=3V
V_{IL}	Input Low Threshold	-0.3	—	0.8	V	LDO_OUT=3V
V_{OH}	Output High Threshold	2.4	—	—	V	LDO_OUT=3V
V_{OL}	Output Low Threshold	—	—	0.4	V	LDO_OUT=3V

Table 6

◆ Power On Reset Characteristics

Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
Trst			10		mS	

Table 7



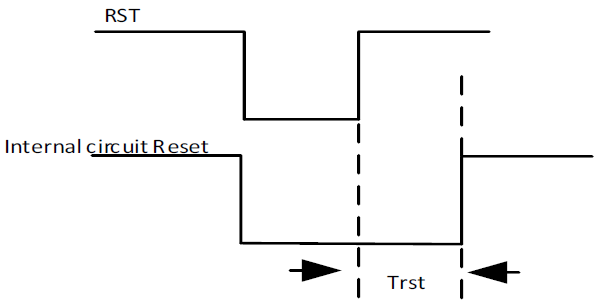


Fig 5.1 Reset Timing Chart

6. Mechanical Specification

6.1 No Shielding Case

- Dimension：20 * 40 * 6.7 mm
- PCB 4 Layers

Mechanical Drawing：

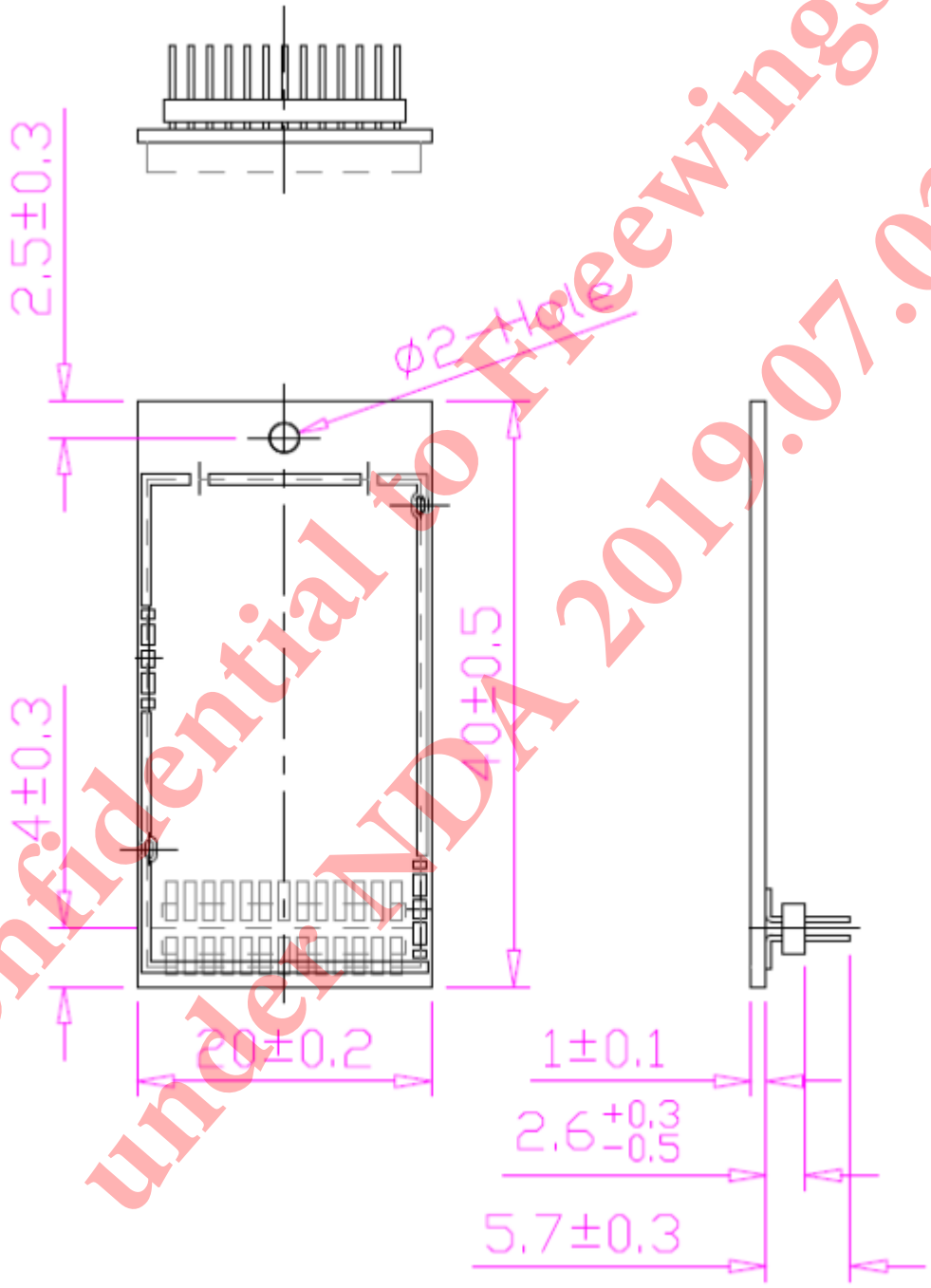


Fig 6.1 Mechanical Drawing of S83D-F Module

◆ Propose 1.27mm Female Header size：H:4.3±0.15mm W:3.0±0.15mm

6.2 With Shielding Case

- Dimension：20 * 40 * 8.7 mm
- PCB 4 Layers

Mechanical Drawing：

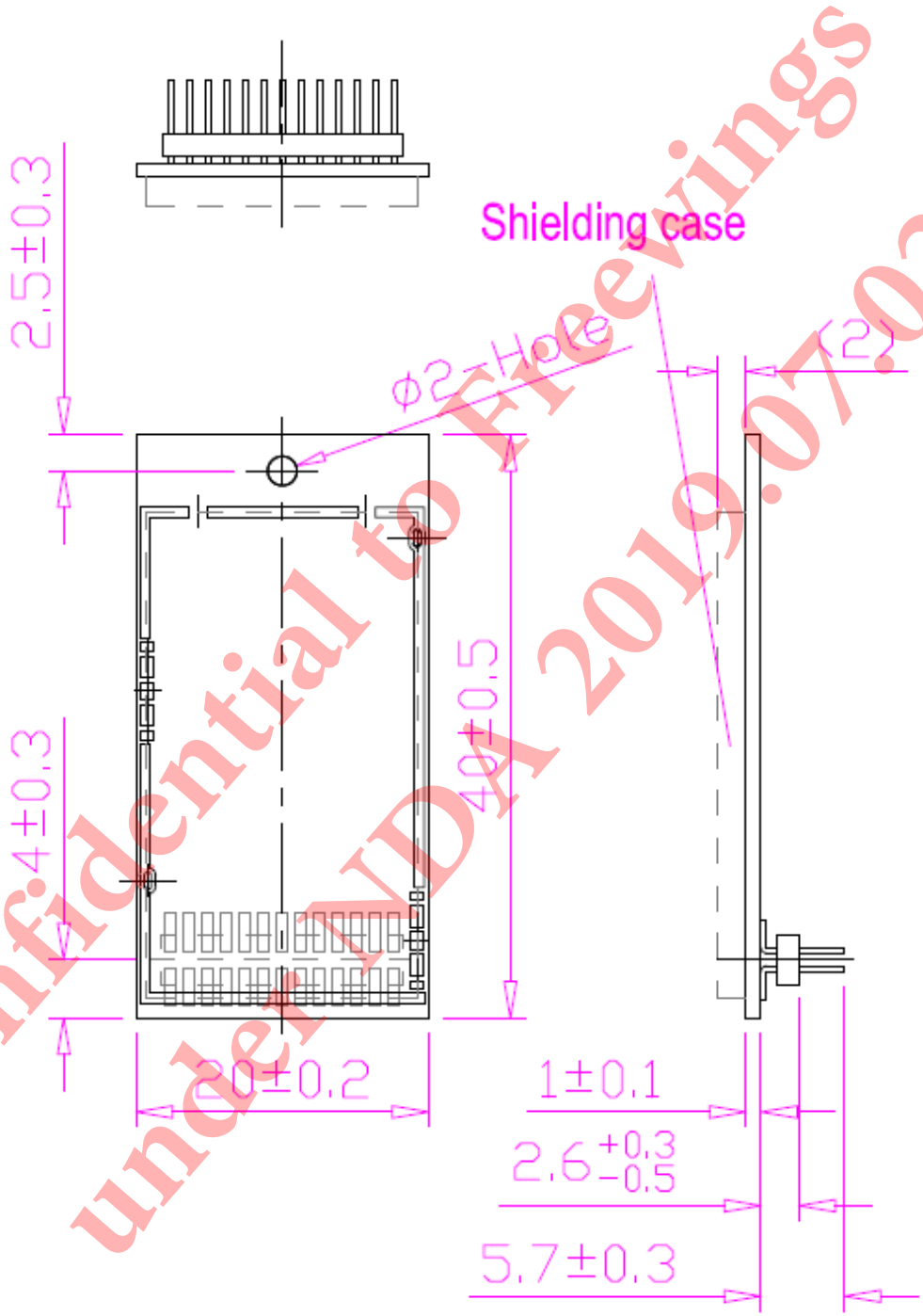
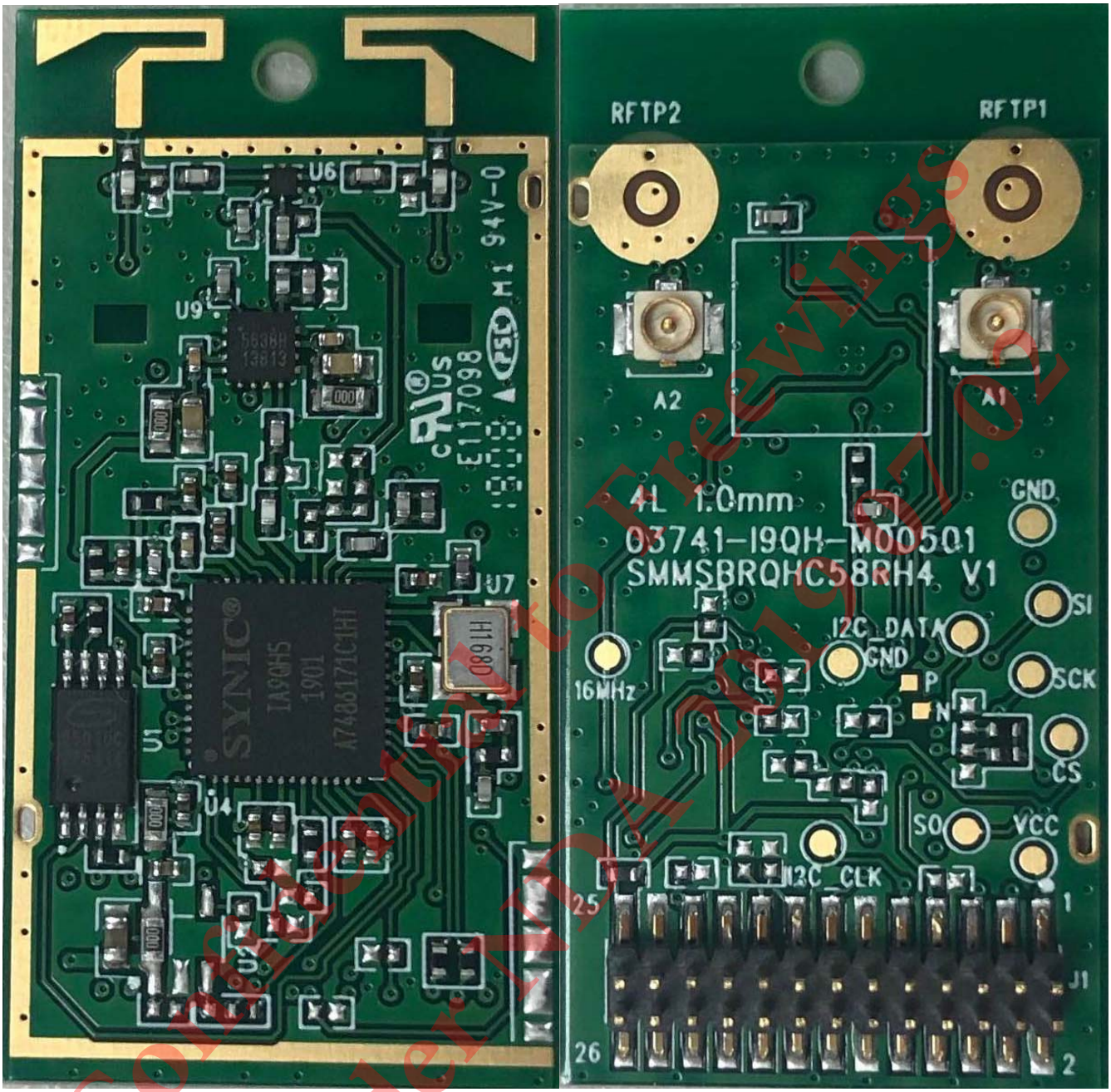
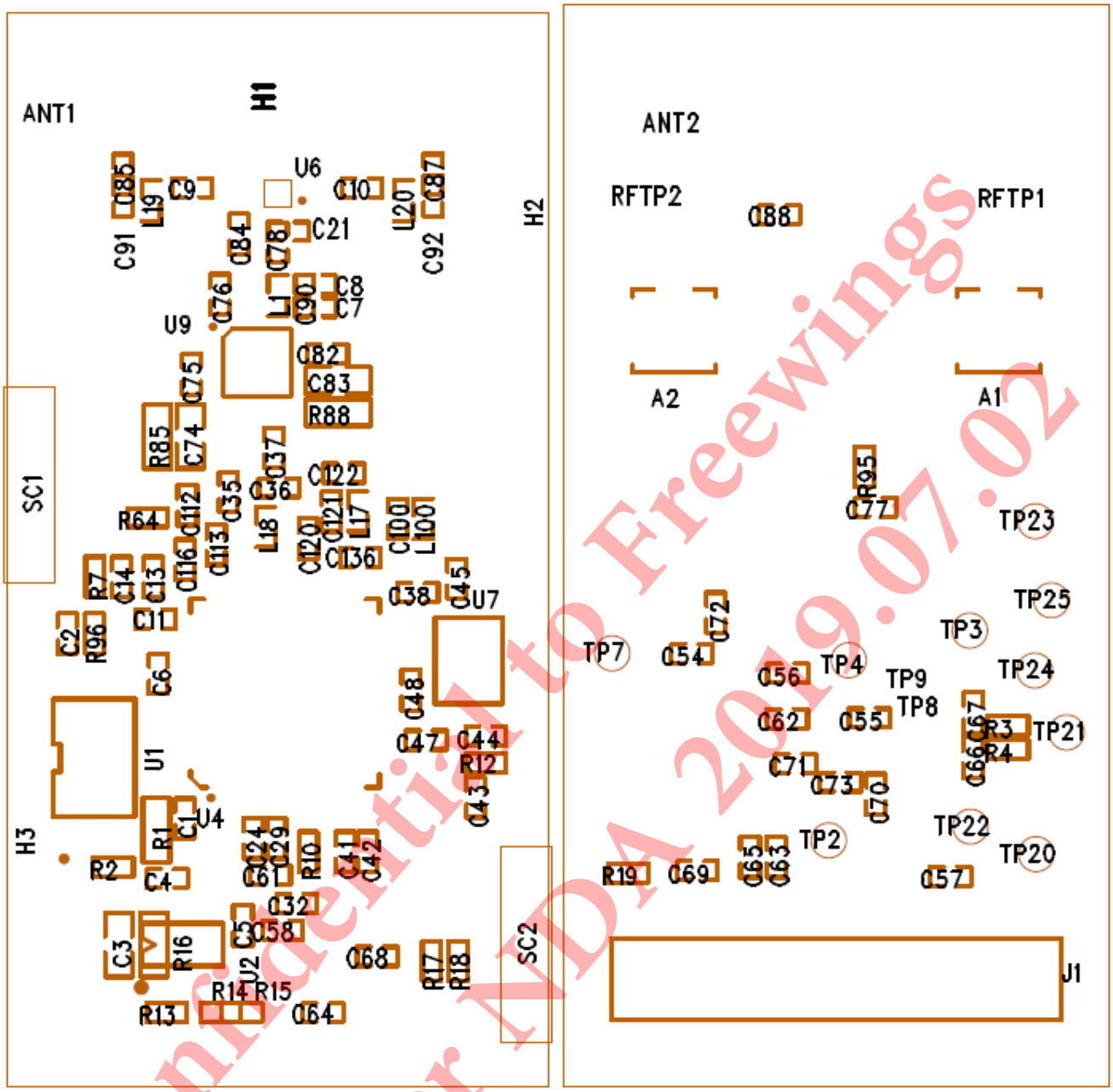


Fig 6.2 Mechanical Drawing of S83D-F Module with shielding case

◆ Propose 1.27mm Female Header size：H:4.3±0.15mm W:3.0±0.15mm





7. Block Diagram

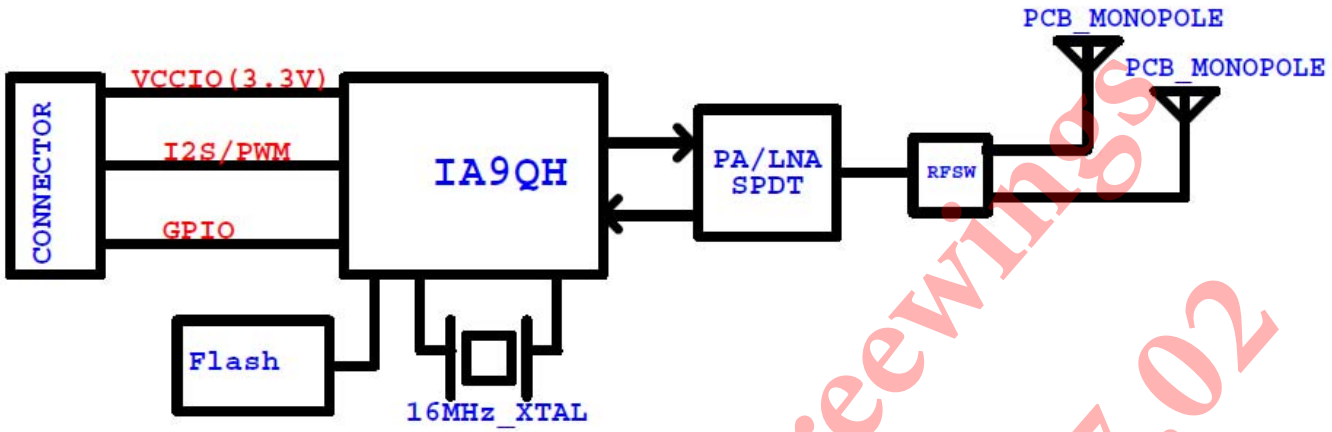


Fig 7.1 Block Diagram of IA9QH5 S83D-F Module

8. Interface

Fig 8.1 Pin sequence of S83D-F Module (Bottom View)

Pin	Name	I/O	TX Function Define	RX Function Define
1	VCCIO	P	DC 3.0 ~ 3.6V IN	DC 3.0 ~ 3.6V IN
2	DGND	P	Digital GND	Digital GND
3	SPB_I2S_MCLK	I/O	SPB I2S audio MCLK system clock output	SPB I2S audio MCLK system clock output
4	GPIO 32	I/O	GPIO	AMP MUTE
5	GPIO 14	I/O	GPIO	GPIO
6	GPIO 13	I/O	GPIO	GPIO
7	GPIO 17	I/O	GPIO	GPIO
8	GPIO 26	I/O	I2C_BUSY，Need 10K Pull High Resistor	I2C_BUSY，Need 10K Pull High Resistor
9	I2C_CLK	I/O	I2C Master/Slave clock signal	I2C Master/Slave clock signal
10	I2C_DATA	I/O	I2C Master/Slave data signal	I2C Master/Slave data signal
11	DGND	P	Digital GND	Digital GND
12	DGND	P	Digital GND	Digital GND
13	GPIO 27	I/O	GPIO	Pairing
14	GPIO 21	I/O	GPIO	GPIO
15	GPIO 16	I/O	GPIO	ON/OFF 12V
16	GPIO 0	I/O	GPIO / SAP I2S audio MCLK	GPIO / SAP I2S audio MCLK
17	M_RESET(PORN)	I/O	Internal power on reset (1)	Internal power on reset (1)
18	I2C_CLK	I/O	I2C Master/Slave clock signal	I2C Master/Slave clock signal
19	I2C_DATA	I/O	I2C Master/Slave data signal	I2C Master/Slave data signal
20	GPIO 30	I/O	GPIO	AMP RESET(L Act)
21	SPA_I2S_DATA	I/O	I2S DATA 0	SYNC LED
22	SPB_I2S_LRCK	I/O	SPB I2S audio LRCK	SPB I2S audio LRCK
23	DGND	P	Digital GND	Digital GND
24	SPB_I2S_BCK	I/O	SPB I2S audio BCK	SPB I2S audio BCK
25	GPIO 15	I/O	GPIO	ON/OFF 3.3V
26	SPB_I2S_DATA	I/O	SPB I2S audio Data	SPB I2S audio Data

Table 8 IO Function Define

Note : (1) *.Not need external RC circuit to do RC reset
*.Power On Reset Characteristics can reference section 5 Electrical Specification (page 6)
*.External controller can direct control M_RESET but should assign the control IO as input for normal operation and output low to Reset S83D-E Module

9. Design Reference

9.1 ADC/DAC Reference Design

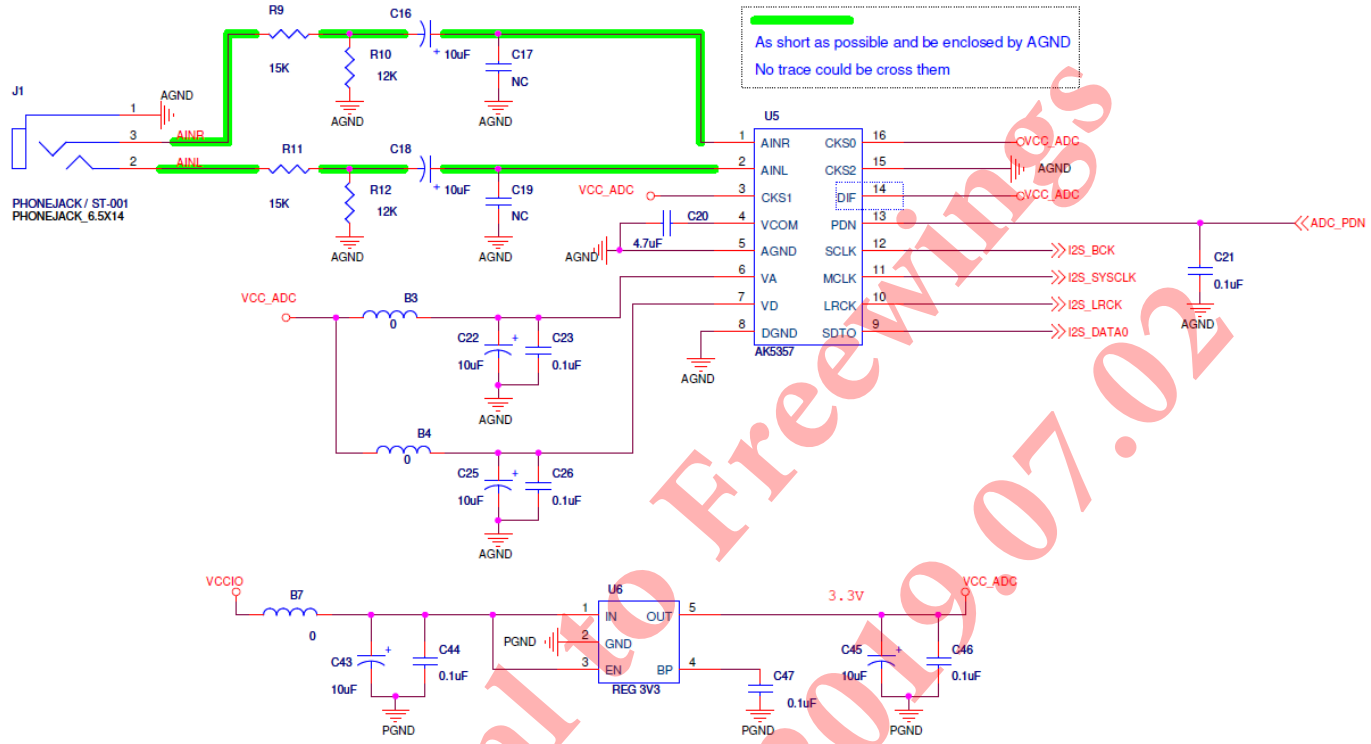


Fig 9.1 ADC reference design circuit

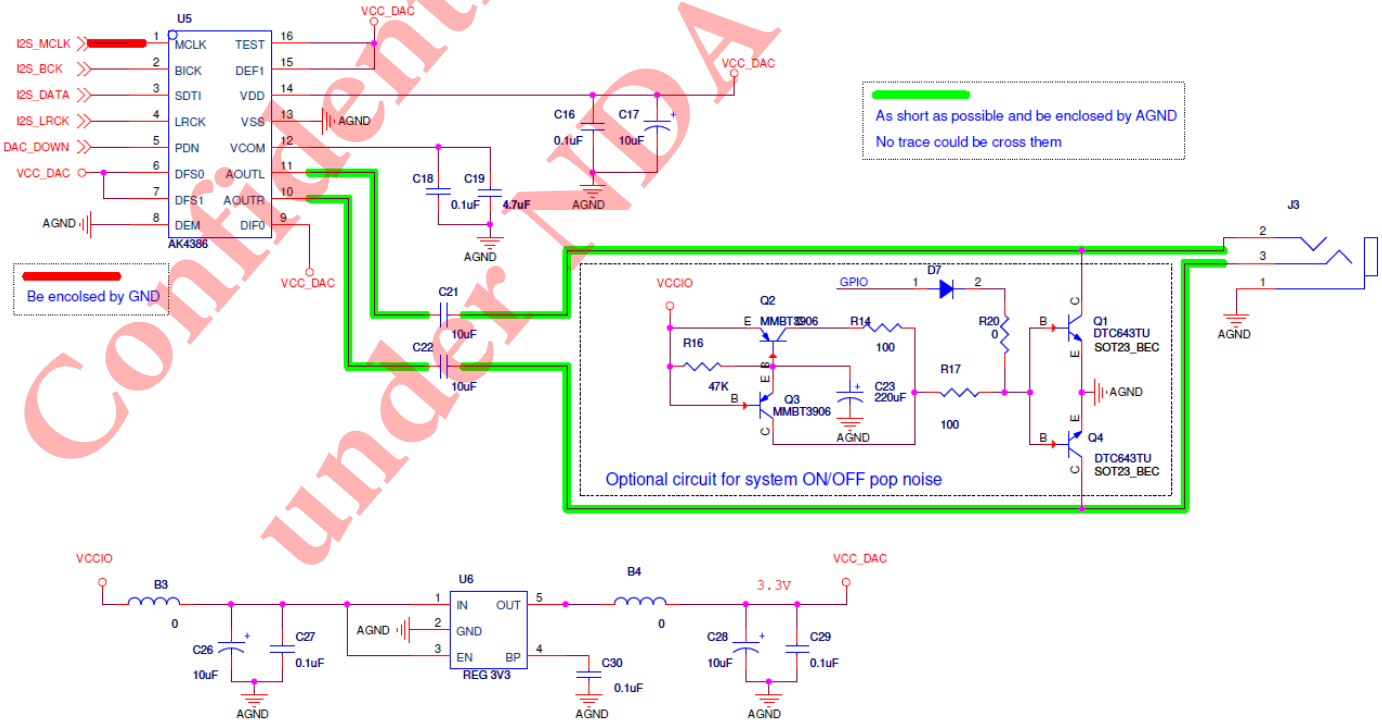


Fig 9.2 DAC reference design circuit

9.2 I2S Timing Chart

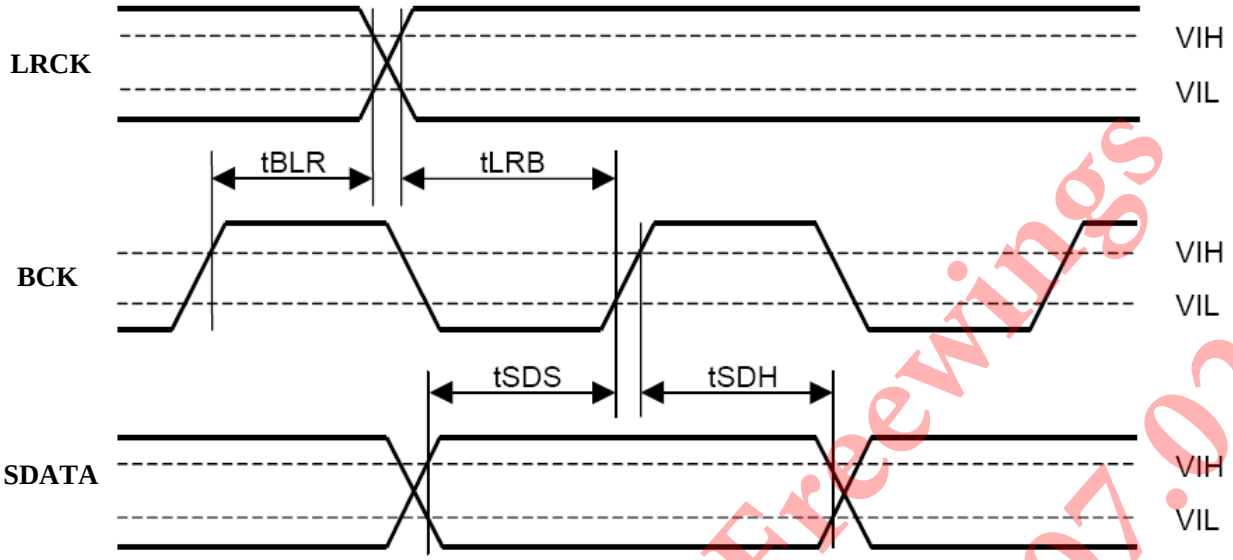


Fig 9.3 I2S timing chart

Symbol	Parameter	Min	Typ	Max	Unit
tBLR	BCK rising to LRCK edge	60			ns
tLRB	LRCK edge to BCK rise	60			ns
tSDS	SDATA setup time	60			ns
tSDH	SDATA hold time	60			ns

Table 9

10. Antenna Application

10.1 Suggested Clear Area

The recommended antenna clearance for embedded PCB antennas are shown below. Note that this clearance should be maintained when mounting the module on a motherboard.

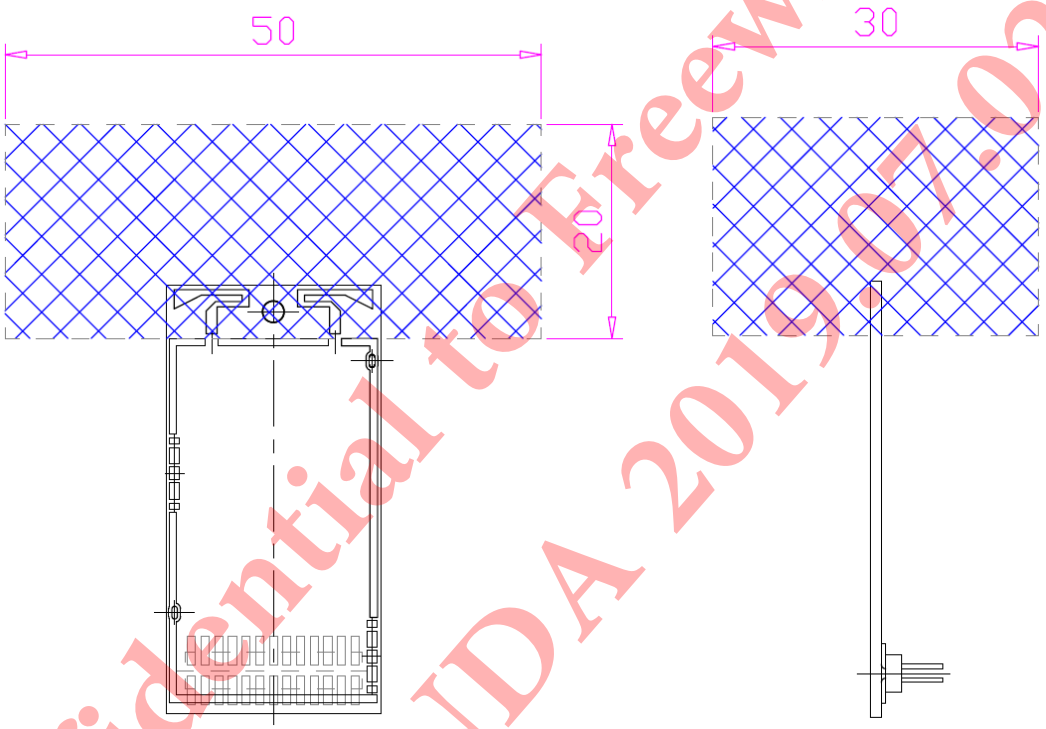
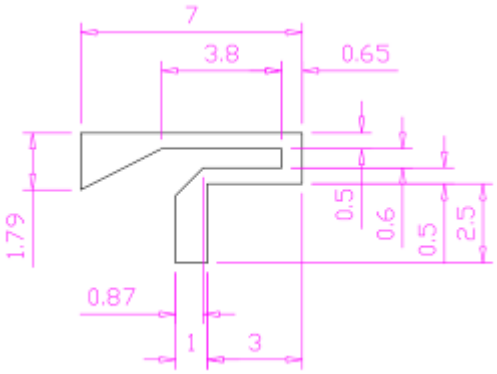


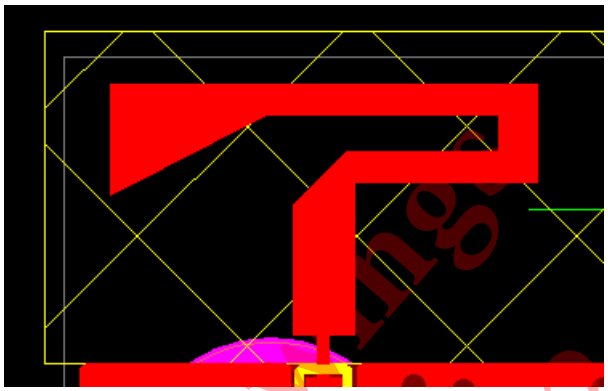
Fig 10.1 Antenna Clearance Recommendations from Top and Side View

Do not place any copper, metal or even PCB in the area marked with cross lines.

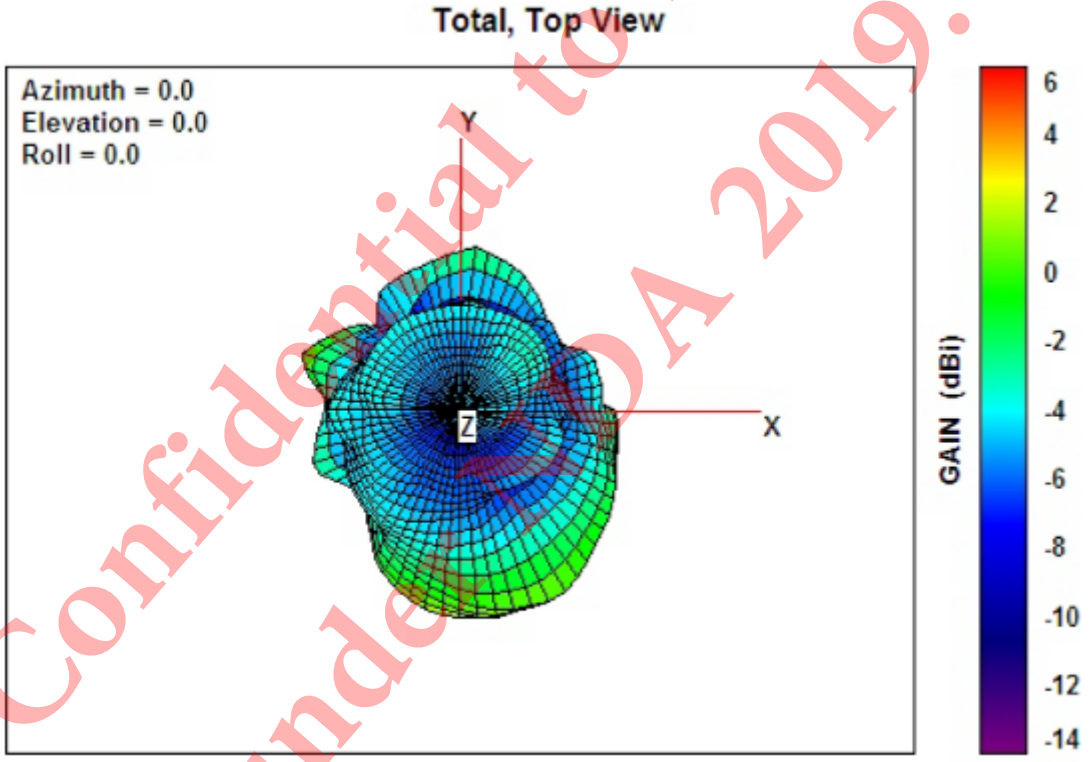
Unit : mm

10.2 Antenna Drawing

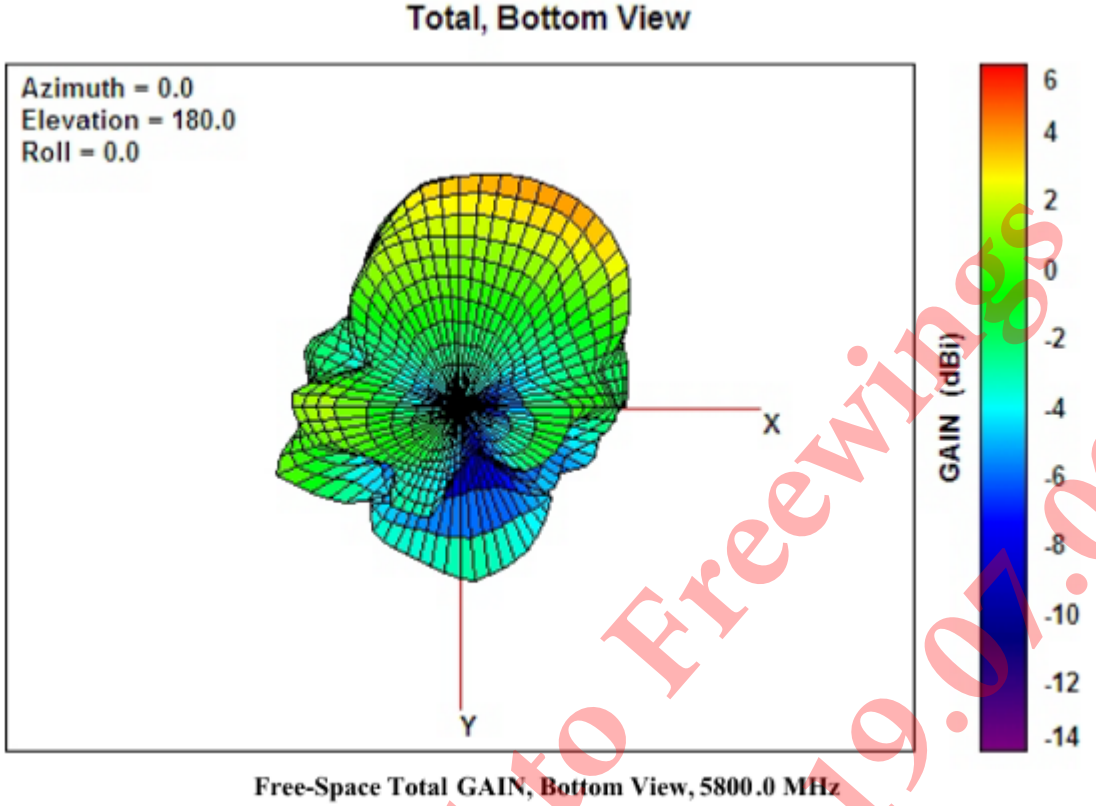




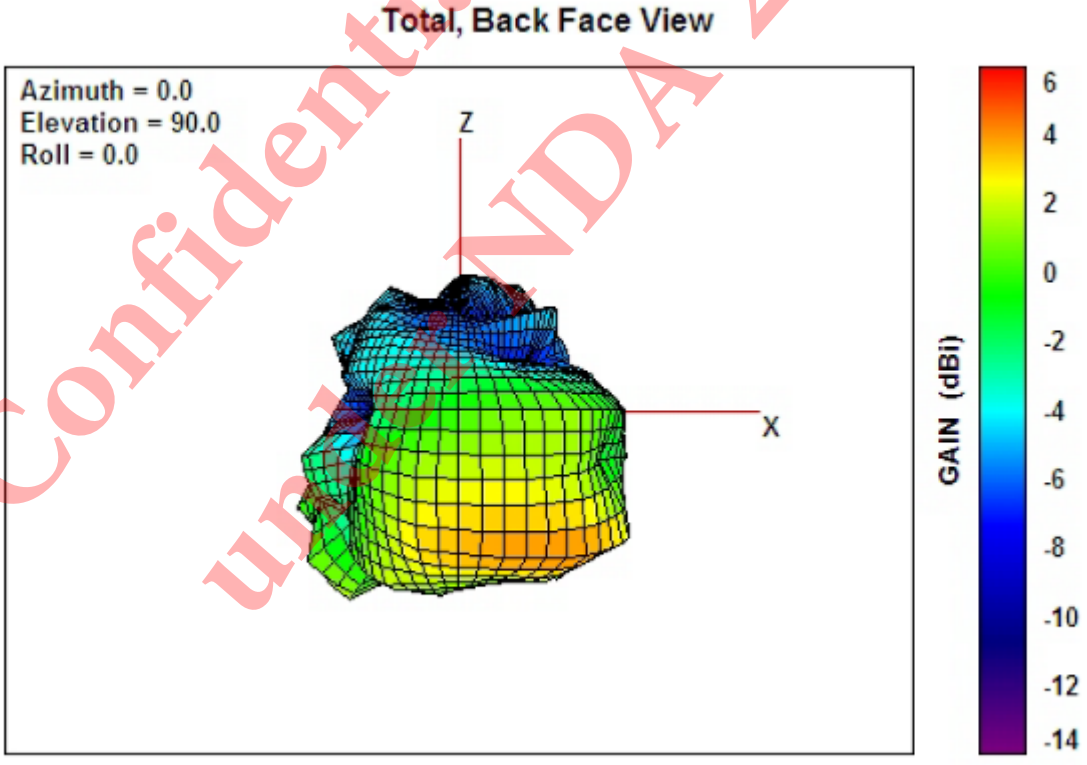
10.3 Antenna Pattern



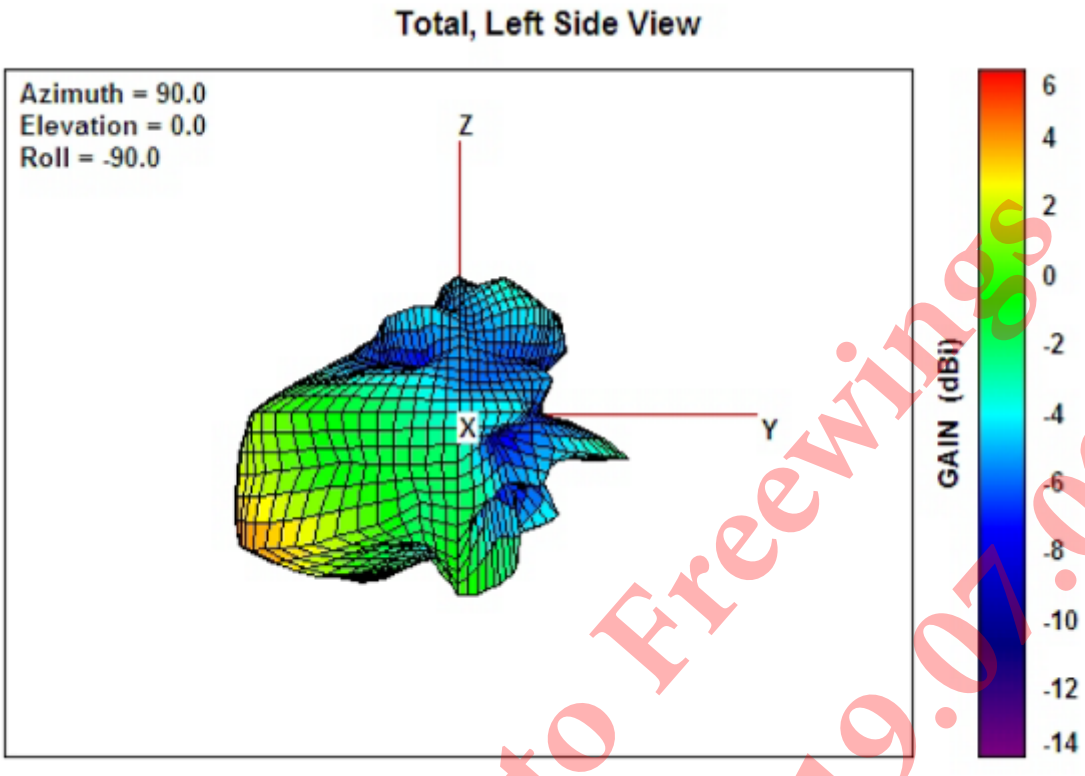
Free-Space Total GAIN, Top View, 5800.0 MHz



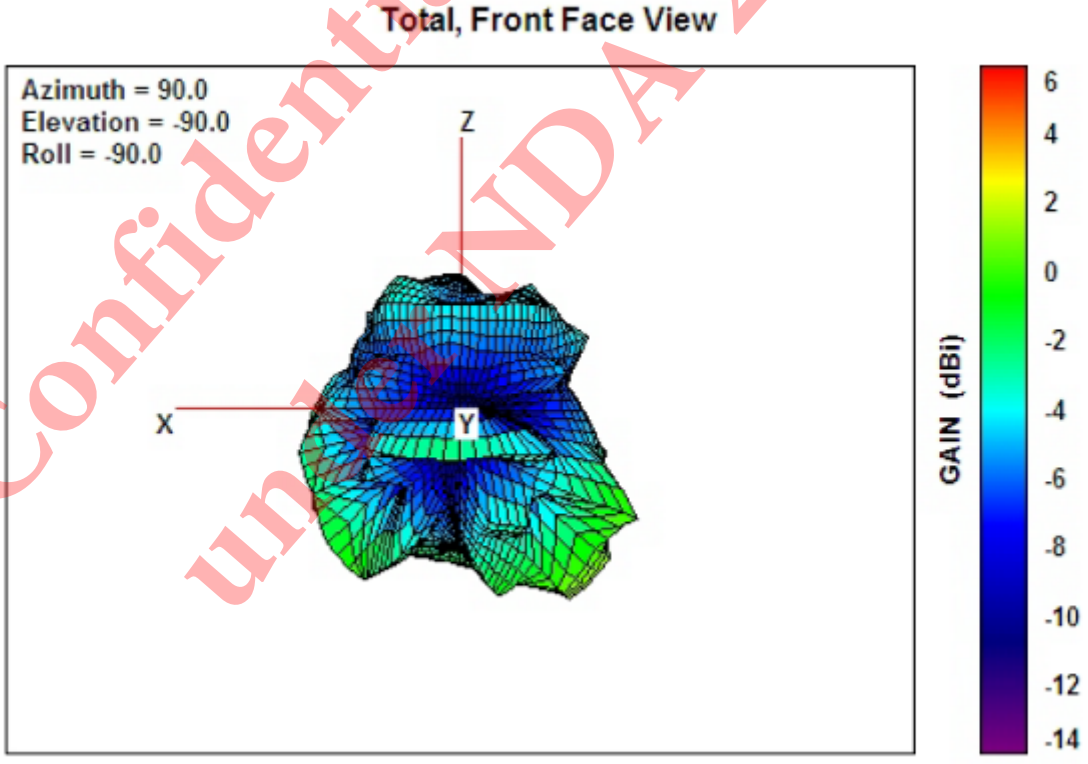
Free-Space Total GAIN, Bottom View, 5800.0 MHz



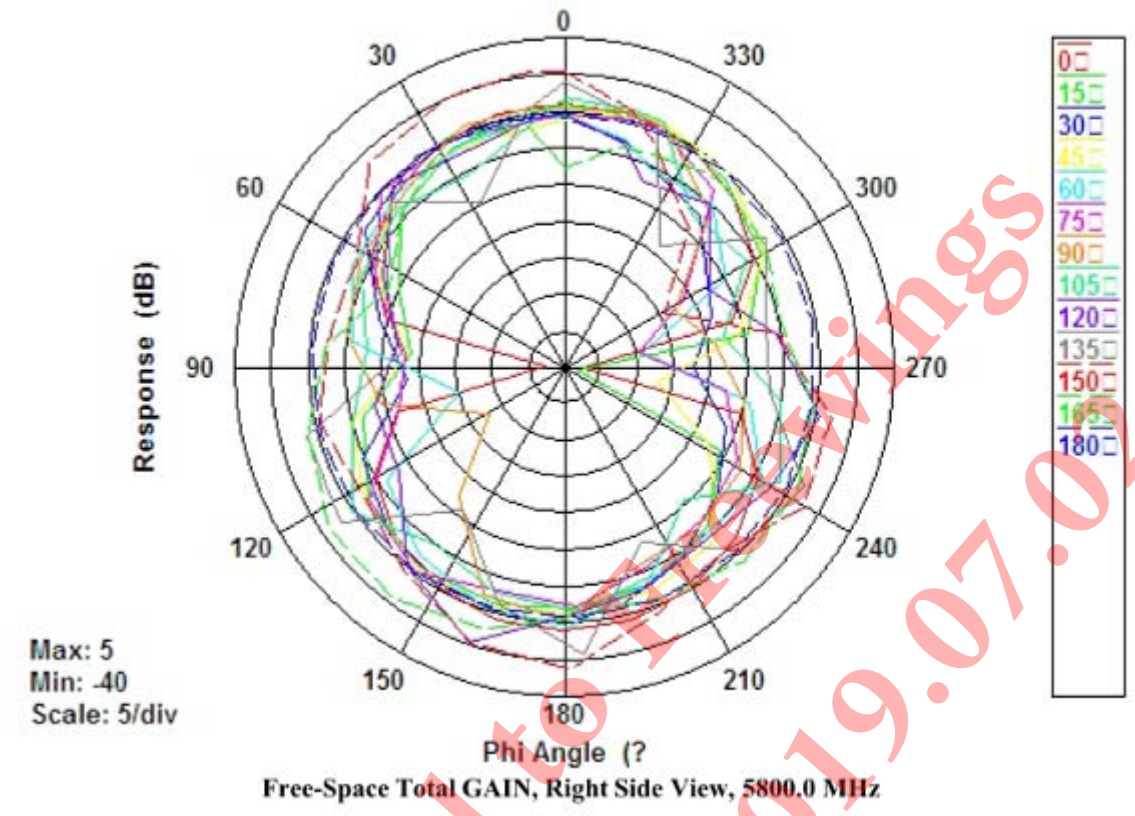
Free-Space Total GAIN, Back Face View, 5800.0 MHz



Free-Space Total GAIN, Left Side View, 5800.0 MHz



Free-Space Total GAIN, Front Face View, 5800.0 MHz



Max Antenna Gain：2.85 dBi

11. Ordering Information

Part Number	(Module) Name	Description
1A5UI-I9QH-21T100	**IA9QH5 S83D-F Module TX**	
1A5UI-I9QH-22T100	**IA9QH5 S83D-F Module TX MHF**	

Table 10

12. Revision History

Date	Revision	Descriptions
2019/02/27	0.1	First release
2019/03/21	0.2	Add Ordering Information

Table 11