IQ10 Hardware Design

LTE Module

Document Title:	IQ10 Hardware Design
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Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution:
- Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.
- This transmitter must be co-located or operated in conjunction with any other antenna or transmitter.

Radiation Exposure Statement:
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This device is intended only for OEM integrators under the following conditions:
1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and the maximum antenna gain allowed for use with this device is 2.23 dBi.
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE: In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling
This transmitter module is authorized only for use in device where the antenna may be installed such that

20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains FCC ID: 2AQRM-IQ10”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Version History

Date	Version	Description of change	Author
2023-02-28	1.00	Initial	Han.Gao Jiahao.Chen Meihao.Li Xiaomin.Luo Tianbao.Yi
2023-05-12	1.01	Update the band information (Chapter1.1, Chapter4) Update the current consumption (Chapter5.4) Update the PIN Assignment Overview (Chapter2.1)	Boru.Zhou Xiaomin.Luo
2023-07-27	1.02	Add the information about the PINs which supported wakeup function.(Chapter 2.1, Chapter 2.2) Add the information about always on GPIO interface.(Chapter 2.1, Chapter 2.2) Add PSM information. (Chapter 5.3.4) Update GNSS standalone mode reference design. (Chapter 3.10)	Boru.Zhou
2023-12-06	1.03	Update the band information (Chapter1.2, Chapter4) Update Reference sensitivity (Chapter4.1) Update the current consumption (Chapter5.4, Chapter3.1) Update the GNSS AT command and reference design(Chapter3.10)	Yang.Zhao Xiaomin.Luo
2024-08-22	1.04	Update the power supply current (Chapter3.1) Delete the PCM function introduce Update supported frequency bands(Chapter1.2) Update reference power on/off circuit(Figure 9) Update the UART hardware flow control(Chapter3.3.1) Update the VBUS circuit design(Chapter3.4.1) Update the GPIO characteristic description (Chapter3.7) Update the 3GPP Receive Sensitivity Description(Chapter4.1) Update the GNSS performance (Table 43) Update the antenna matching designation(Chapter4.5.1) Changed the tuner instructions in Chapter 4.5 Change the description of the modulation method and rate(Chapter8.1) Update related documents(Chapter8.2)	Yang.Zhao Cong.Tao
2024-08-22	1.05	Add IQ10JP band(Table 2) Update $Ton_{(USB)}$(Table 12) Update GNSS Note11 (Chapter3.10) Update Size(Table 3)	Yang.Zhao Peng.Zhang

Contents

Table Index

Figure Index

1. Introduction

This document describes the electronic specifications, RF specifications, interfaces, mechanical characteristics, and test results of the IQ10 Series module. With the help of this document, customers can quickly understand IQ10 Series module.

Associated with other software application notes and user guides, customers can use IQ10 Series to design and develop applications easily. We provides a set of evaluation boards to facilitate test and development of IQ10 module. The evaluation board tools include an EVB board, a USB cable, an antenna, a GNSS active antenna and other peripherals.

1.1. Documentation Overview

The documents listed in Table 1 primarily cover the module's technical information. To thoroughly understand the device and its application, it is necessary to study all relevant documents.

Table 1: IQ10 Series Documents Overview

No.	Document	Description
1	IQ10_Series_Hardware_Design (This document)	Mainly introducing interface functions, recommend circuit, PCB layout guideline, packaging and other hardware components, as well as the use of AT commands.
2	IQ10 Series_Reference_Design	Reference circuit applications.
3	8XS000-IQ10-TE_DL&PCB 8XS000-IQ10-NEWEVB_ DL&PCB	IQ10 TE/NEWEVB SCH&PCB PDF Document.
4	EVB_DL&PCB	EVB SCH&PCB PDF Document.
5	MOD_IQ10_124	Reference Package (PADS/AD/Cadence).
6	IQ10 Series_AT Command Manual	AT Command Manual.
7	Module Secondary SMT Process User Guide	Module secondary SMT Guidelines.
8	IQ10_TE kit_User Guide IQ10-EVB_User_Guide_Manual	The use of TE/NEWEVB board, forced download, startup, reset, and the location of other measurement points, as well as the use method in conjunction with EVB.
9	IQ10_CAT1_Module_Schematic&Layout_Checklist	IQ10 peripheral circuit schematic and PCB checklist.

NOTE

This current revision is an early release to support initial product developers. The content is subject to change without advance notice. Please confirm with FAE for the latest version.

1.2. Product Outline

The module supports LTE-TDD and LTE-FDD. The supported radio frequency bands are described in the following table.

Table 2: Module frequency bands

Standard	Frequency	IQ10E	IQ10NA	IQ10S	IQ10G	IQ10JP
LTE-FDD	LTE-FDD B1	□		□	□	□
	LTE-FDD B2		□		□	
	LTE-FDD B3	□		□	□	□
	LTE-FDD B4		□		□	
	LTE-FDD B5	□	□	□	□	
	LTE-FDD B7	□			□	
	LTE-FDD B8	□		□	□	□
	LTE-FDD B12		□		□	
	LTE-FDD B13		□		□	
	LTE-FDD B18				□	□
	LTE-FDD B19				□	□
	LTE-FDD B20	□			□	
	LTE-FDD B25				□	
	LTE-FDD B26				□	□
	LTE-FDD B28	□			□	□
	LTE-FDD B66		□		□	
	LTE-FDD B71*					
LTE-TDD	LTE TDD B34			□	□	
	LTE TDD B38			□	□	
	LTE TDD B39			□	□	
	LTE TDD B40			□	□	
	LTE TDD B41			□	□	
Category		CAT1	CAT1	CAT1	CAT1	CAT1
GNSS		Optional	Optional	Optional	Optional	Optional
WIFI SCAN		□	□	□	□	□

NOE

B71 can be selected according to your needs.

With a small physical dimension of 24*24*2.4mm, the module can meet almost any space requirement in customers' applications, such as smart phone, PDA, industrial handhold, machine-to-machine and vehicle application, etc.
The module provides 124 pins, including 80 LCC pins in the outer ring and 44 LGA pins in the inner ring. This document will introduce all the functional pins.

1.3. Hardware Interface Overview

The interfaces are described in detail in the following chapters including:

- Power supply
- USB 2.0 interface
- Three UART interfaces, one full function serial port, one ordinary serial port and one debug serial port
- One USIM interface
- I2C interface
- Two General ADC interfaces
- General input and output interfaces (GPIOs)
- Two ANT tuner control interfaces (GRFCs)
- USB_BOOT interface
- Module operation status indication interface
- Network status indication interface
- MAIN_UART_WAKEUP interface
- GNSS interfaces
- Antenna interfaces

1.4. Hardware Block Diagram

The block diagram of the IQ10 module is shown in the figure below.

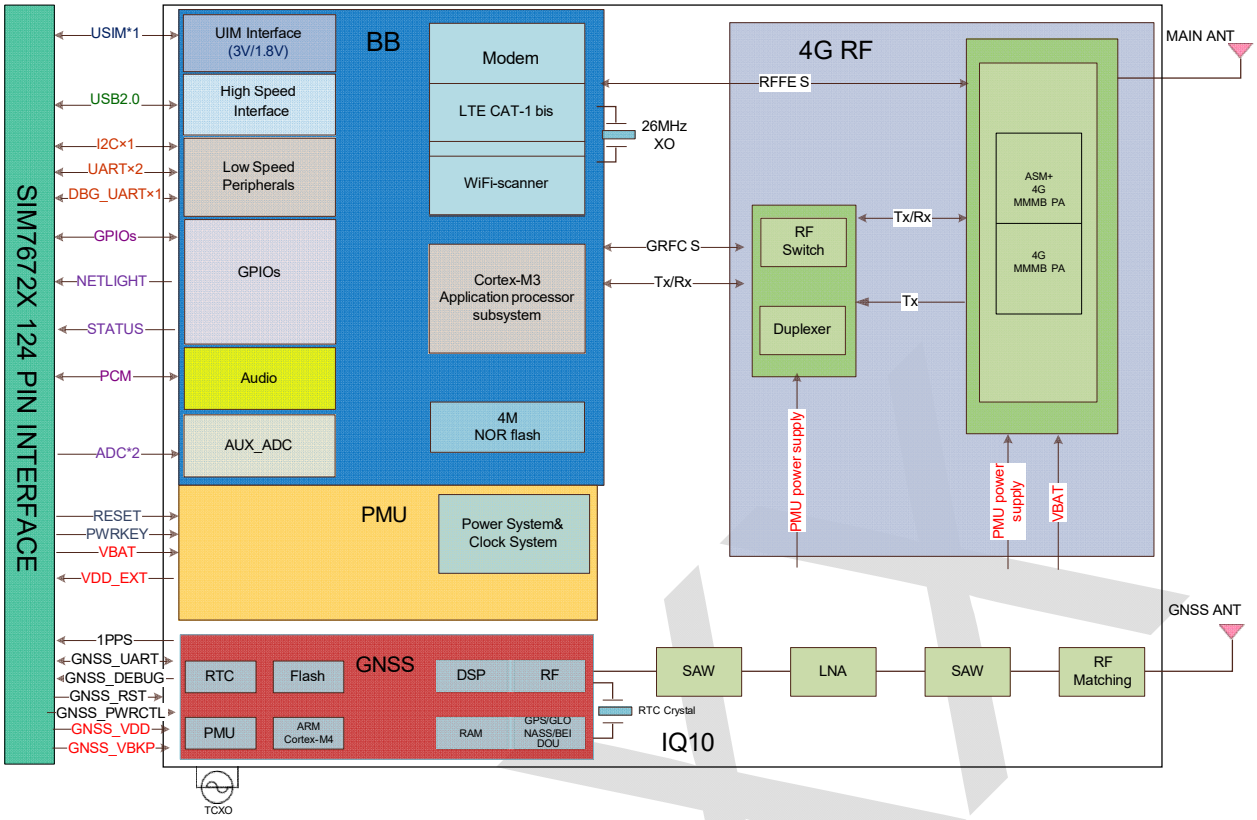

Figure 1: IQ10 block diagram

1.5. Functional Overview

Table 3: General features

Feature	Implementation
Power supply	VBAT: 3.4V~4.2V, Recommended VBAT: 3.8V
Power saving	Idle mode Typical: 4.4mA Current in Sleep mode@DRX=0.32S typical: 1.42mA (GNSS off) Current in Sleep mode@DRX=0.64S typical: 786uA (GNSS off) Current in Sleep mode@DRX=1.28S typical: 597uA (GNSS off) Current in PSM_hib mode: 2.8uA Please refer to the table 53
Radio frequency bands	Please refer to the table 2
Transmitting power	LTE power level: 3 (23dBm±2.7dB)
Data Transmission Throughput	TDD/FDD-LTE category 1: 10 Mbps (DL), 5 Mbps (UL)
Antenna	LTE antenna interface GNSS antenna interface
SMS	● MT, MO, CB, Text, PDU mode ● Short Message (SMS) storage device: USIM Card, CB does not

	support saving in SIM Card ● Support CS domain SMS
USIM interface	Support identity card: 1.8V/ 3V
USIM application toolkit	Support SAT class 3, GSM 11.14 Release 98 Support USAT
Phonebook management	Support phonebook types: SM/FD/ON/AP/SDN
PCM interface	Support PCM interface(Standard version not support)
UART interface	● Full function serial port Baud rate support from 600bps to 921600bps AT command and data can be sent through serial port Support RTS/CTS hardware flow control Support serial port multiplexing function conforming to GSM 07.10 protocol ● Debug serial port Support debug function ● AUX_UART serial port Support GNSS communication function
USB	Compliant with USB 2.0 specification and supports slave mode but not master mode. This interface can be used for AT command sending, data transmission, GNSS NMEA output, software debugging and upgrading.
Firmware upgrade	Firmware upgrade over USB interface or MAIN_UART interface
Physical characteristics	Size: 24(±0.15)mm *24(±0.15)mm *2.4(±0.20)mm Weight: 2.83(±0.1)g (Typical)
Temperature range	Normal operation temperature: -30°C to +75°C Extended operation temperature: -40°C to +85°C* Storage temperature: -40°C to +90°C

NOTE

When the module is within the extended operation temperature range, module is able to establish and maintain data transmission, SMS, etc. The performance may deviate slightly from the 3GPP specifications, but will meet 3GPP specifications again when the temperature returns to normal operating temperature levels. It is strongly recommended that customers take heat dissipation measures to ensure that the normal operating temperature of the module can't be exceeded.

2. Package Information

2.1. Pin Assignment Overview

The following figure is a top view of the pin assignment of the module for IQ10.

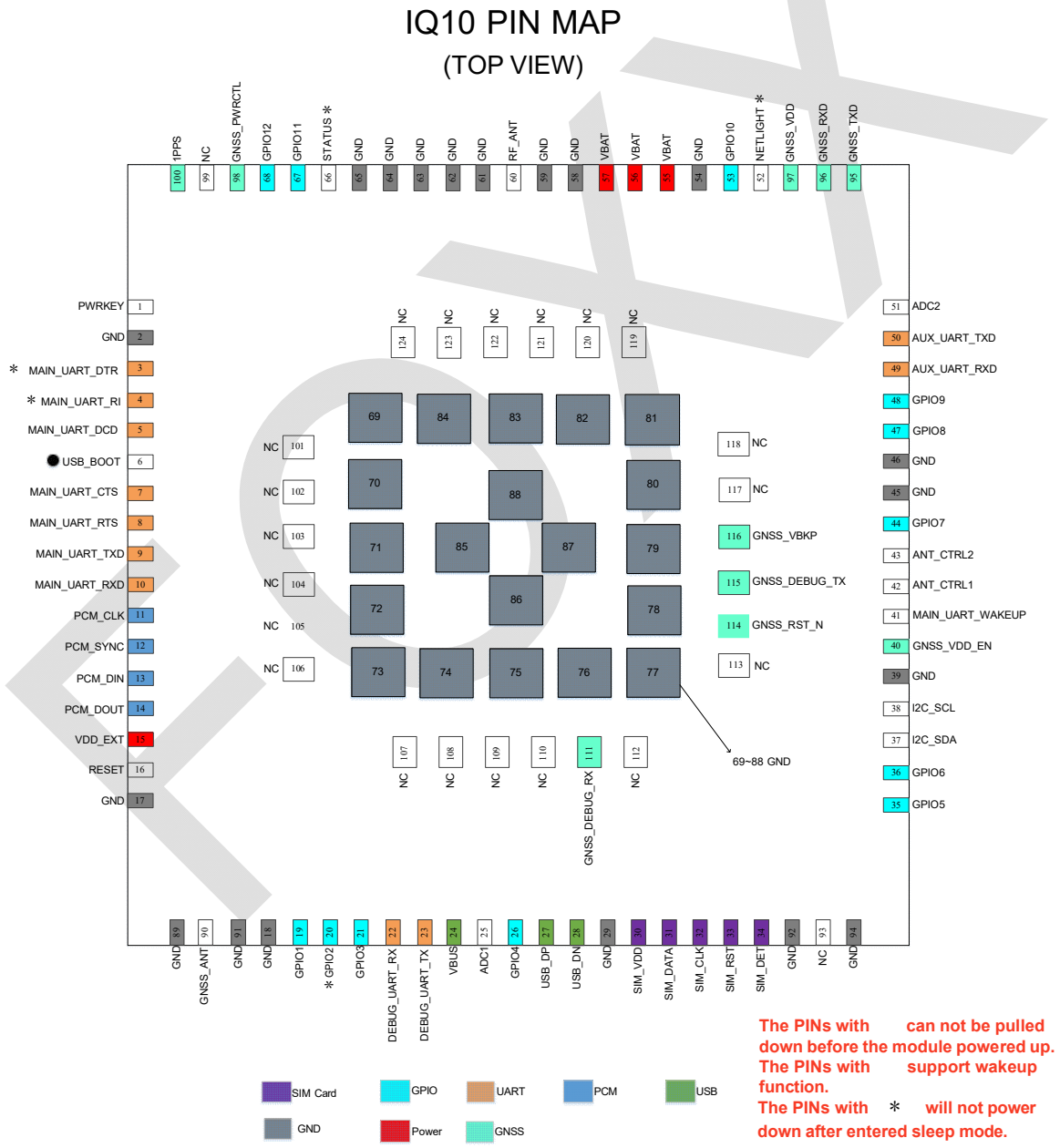

Figure 2: Pin assignment overview for IQ10

Table 4: Pin Description

PIN NO	PIN NAME	PIN NO	PIN NAME
1	PWRKEY	2	GND
3	MAIN_UART_DTR▲*	4	MAIN_UART_RI*
5	MAIN_UART_DCD	6	USB_BOOT●
7	MAIN_UART_CTS	8	MAIN_UART_RTS
9	MAIN_UART_TXD	10	MAIN_UART_RXD
11	PCM_CLK	12	PCM_SYNC
13	PCM_DIN	14	PCM_DOUT
15	VDD _EXT	16	RESET
17	GND	18	GND
19	GPIO1	20	GPIO2*
21	GPIO3	22	DEBUG_UART_RX
23	DEBUG_UART_TX	24	VBUS▲
25	ADC1	26	GPIO4
27	USB_DP	28	USB_DN
29	GND	30	SIM_VDD
31	SIM_DATA	32	SIM_CLK
33	SIM_RST	34	SIM_DET
35	GPIO5	36	GPIO6
37	I2C_SDA	38	I2C_SCL
39	GND	40	GNSS_VDD_EN
41	MAIN_UART_WAKEUP▲	42	ANT_CTRL1
43	ANT_CTRL2	44	GPIO7
45	GND	46	GND
47	GPIO8	48	GPIO9
49	AUX_UART_RXD	50	AUX_UART_TXD
51	ADC2	52	NETLIGHT*
53	GPIO10	54	GND
55	VBAT	56	VBAT
57	VBAT	58	GND
59	GND	60	RF_ANT
61	GND	62	GND
63	GND	64	GND
65	GND	66	STATUS*
67	GPIO11	68	GPIO12
69	GND	70	GND
71	GND	72	GND
73	GND	74	GND
75	GND	76	GND

77	GND	78	GND
79	GND	80	GND
81	GND	82	GND
83	GND	84	GND
85	GND	86	GND
87	GND	88	GND
89	GND	90	GNSS_ANT
91	GND	92	GND
93	NC	94	GND
95	GNSS_TXD	96	GNSS_RXD
97	GNSS_VDD	98	GNSS_PWRCTL
99	NC	100	1PPS
101	NC	102	NC
103	NC	104	NC
105	NC	106	NC
107	NC	108	NC
109	NC	110	NC
111	GNSS_DEBUG_RX	112	NC
113	NC	114	GNSS_RST_N
115	GNSS_DEBUG_TX	116	GNSS_VBKP
117	NC	118	NC
119	NC	120	NC
121	NC	122	NC
123	NC	124	NC

NOTE

'●' indicates that the pin cannot be pulled down before the module powered up, otherwise it will affect the normal start-up of the module.
'▲' indicates that the pins support wakeup function.
' * ' indicates that these interfaces are always on GPIO, they can remain the previous status when the module enters sleep mode.
GNSS_VDD_EN (PIN 40) only can be used at standalone mode!!!
NC: NOT CONNECT. Do not connect them to GND.

2.2. Pin Description

Table 5: Pin parameter abbreviation

Pin type	Description
PI	Power input
PO	Power output
AI	Analog input
AIO	Analog input/output
I/O	Bidirectional input /output
DI	Digital input
DO	Digital output
DOH	Digital output with high level
DOL	Digital output with low level
PU	Pull up
PD	Pull down
OD	Open Drain

Table 6: 1.8V IO parameters definition

Power Domain	Parameter	Description	Min	Typ.	Max
1.8V	V_{IH}	High level input	0.7 * VCC	1.8V	VCC + 0.2
	V_{IL}	Low level input	-	0V	0.2 * VCC
	R_{pu}	Pull up resistor	117KΩ	-	331KΩ
	R_{pd}	Pull down resistor	91KΩ	-	291KΩ
	I_{IH}	Input high leakage current	-10uA	-	10uA
	I_{IL}	Input low leakage current	-10uA	-	10uA
	V_{OH}	Output level range	0.8 * VCC	-	-
	V_{OL}	Output low range	-	-	0.15 * VCC
	I_{OL}	Maximum current driving capacity at low level output	-	-	-
	I_{OH}	Maximum current driving capacity at high level output V_{pad}=VCC-0.2V	-	-	-

Table 7: Pin description

Pin name	Pin No	Pin parameter		Description	Note
		Power domain	Type		
Power supply					
VBAT	55,56, 57	-	PI	Module input voltage ranges from 3.4V to 4.2V, typical values is 3.8V.	
VDD_EXT	15	-	PO	1.8V power output, output current up to 50 mA.	Default on. It can provide 1V8 power supply for GNSS. If unused, keep it open.
GND	2,17,18,29, 39,45,46, 54,58,59, 61,62,63, 64,65,69, 70,71,72, 73,74,75, 76,77,78, 79,80,81, 82,83,84, 85,86,87, 88,89,91, 92,94	-	-	Ground	
System Control					
PWRKEY	1	-	DI,PU	Power ON/OFF input, active low.	
RESET	16	-	DI,PU	System reset control input, active low.	
USIM interface					
SIM_DATA	31	1.8/3.0V	I/O,PU	SIM data signal.	This pin has been pull-up with 4.7KΩ resistor to SIM_VDD internally.
SIM_RST	33	1.8/3.0V	I/O,PU	SIM RST signal reset output.	
SIM_CLK	32	1.8/3.0V	I/O,PU	SIM CLK signal clock output.	
SIM_VDD	30	1.8/3.0V	PO	SIM card power supply output.	Supports 1.8V/3.0V output according to the card type, its output current is up to 34mA.
SIM_DET	34	1.8V	I/O,PU	SIM card insert	It can be set to

				detect.	high/low active with the AT command, refer to Document [18].
USB interface					
VBUS▲	24	-	PI	Valid USB detection input. Active high, V_{min}=3.3V, V_{max}=5.2V, V_{norm}=5V	
USB_DN	28	-	AIO	Negative electrode of the differential, bi-directional USB signal.	
USB_DP	27	-	AIO	Positive electrode of the differential, bi-directional USB signal.	
Full function UART interface					
MAIN_UART_RTS	8	1.8V	DI	DTE request to send signal to DCE	If unused, keep it open.
MAIN_UART_CTS	7	1.8V	DO	DTE clear to send signal from DCE	
MAIN_UART_RXD	10	1.8V	DI	Data input	
MAIN_UART_TXD	9	1.8V	DO	Data output	
MAIN_UART_RI *	4	1.8V	DO	Ringing indicator	
MAIN_UART_DCD	5	1.8V	DO	Carrier detection	
MAIN_UART_DTR *▲	3	1.8V	DI	DTE Ready	
Debug_UART					
DEBUG_UART_TX	23	1.8V	DOH	Debug UART, the boot log will be output during boot up.	Default used as debug port.
DEBUG_UART_RX	22	1.8V	DI		
AUX_UART					
AUX_UART_TXD	50	1.8V	DO	Data output	Two-wire serial port.
AUX_UART_RXD ▲	49	1.8V	DI	Data input	
I2C interface					
I2C_SCL	38	1.8V	OD	I2C clock output	If unused, keep it open. Need pull up to VDD_EXT externally.
I2C_SDA	37	1.8V	OD	I2C data I/O	
PCM interface					
PCM_CLK	11	1.8V	I/O,PD	PCM clock	If unused, keep it

PCM_SYNC	12	1.8V	I/O,PD	PCM frame synchronization	open.(Standard version not support)
PCM_DIN	13	1.8V	DI,PD	PCM data input	
PCM_DOUT	14	1.8V	DO,PD	PCM data output	
GPIO					
GPIO1	19	1.8V	IO,PU	General purpose I/O	If unused, keep it open.
GPIO2＊	20	1.8V	DO,PD	Only can be connect to GNSS_PWRCTRL	
GPIO3	21	1.8V	IO,PU	General purpose I/O	
GPIO4	26	1.8V	IO,PD	General purpose I/O	
GPIO5	35	1.8V	IO,PU	General purpose I/O	
GPIO6	36	1.8V	IO,PU	General purpose I/O	
GPIO7	44	1.8V	IO,PU	General purpose I/O	
GPIO8	47	1.8V	IO,PU	General purpose I/O	
GPIO9	48	1.8V	IO,PD	General purpose I/O	
GPIO10	53	1.8V	IO,PU	General purpose I/O	
GPIO11	67	1.8V	IO,PU	General purpose I/O	
GPIO12	68	1.8V	IO,PU	General purpose I/O	
GNSS interface					
GNSS_PWRCTL	98	1.8V	DI	The enable control PIN of GNSS Vcore power supply.	Active high.
GNSS_VDD_EN	40	1.8V	DI	The enable control PIN of GNSS system power supply.	It only can be used at standalone mode.
GNSS_VDD	97	-	PI	The power input for GNSS.	Module VDD_EXT (PIN 15) can be used for this power supply.
GNSS_VBKP	116	-	PI	GNSS VRTC power input, input voltage 2.0V~3.6V, recommend 2.8V power supply.	It is necessary for GNSS function!
1PPS	100	1.8V	DO	1PPS signal output	Seconds pulse signal, do not pull up before GNSS power up. It can be used for accurate timing. Output pulse signal approximately 30 seconds after successful positioning. If unused, keep it open.
GNSS_RXD	96	1.8V	DI	GNSS UART RX	Connect to MCU UART_TXD;

					Or use 1K resistor in series in module AUX_UART_TXD (PIN 50).
GNSS_TXD	95	1.8V	DO	GNSS UART TX	Connect to MCU UART_RXD; Or use 1K resistor in series in module AUX_UART_RXD (PIN 49).
GNSS_RST_N	114	-	AI	GNSS RST interface	Internal pull up, active low.
GNSS_DEBUG_TX	115	1.8V	DO	GNSS debug output	
GNSS_DEBUG_RX	111	1.8V	DI	GNSS debug input	
ANT interface					
RF_ANT	60	-	AIO	Main antenna	
GNSS_ANT	90	-	AIO	GNSS antenna	
Other pins					
ADC1	25	-	AI	General Purpose ADC1	If unused, keep it open.
ADC2	51	-	AI	General Purpose ADC2	If unused, keep it open.
NETLIGHT*	52	1.8V	DO	Network registration status indicator (LED).	
STATUS*	66	1.8V	DO	Module status indicator (LED).	
USB_BOOT●	6	1.8V	DI	Firmware download guide control input. When pull-down to GND and press PWRKEY, module will access in USB download mode.	Please reserve 2 test points for debug. Do not pull down USB_BOOT during normal power on!
ANT_CTRL1	42		DO	FEMIO for tuner switch	
ANT_CTRL2	43		DO	FEMIO for tuner switch	
MAIN_UART_WAKEUP▲	41	1.8V	DI	MAIN_UART_RXD wake-up pin.	Connect it to MAIN_UART_RXD externally if use this function.

NOTE

Please reserve test points for USB_BOOT, GND, DEBUG_UART_TX, GNSS_DEBUG_TX, GNSS_DEBUG_RX, GNSS_TXD and GNSS_RXD.

If there is no USB connector, please also reserve test points for VBUS, USB_DP, and USB_DN for firmware upgrading.

'●' Indicates that the pin cannot be pulled down before the module powered up, otherwise it will affect the normal start-up of the module.

'▲' Indicates that the pin support wakeup function.

' * ' indicates that these interfaces are always on GPIO, they can remain the previous status when the module enters sleep mode.

2.3. Mechanical Information

The following figure shows the package outline drawing of IQ10.

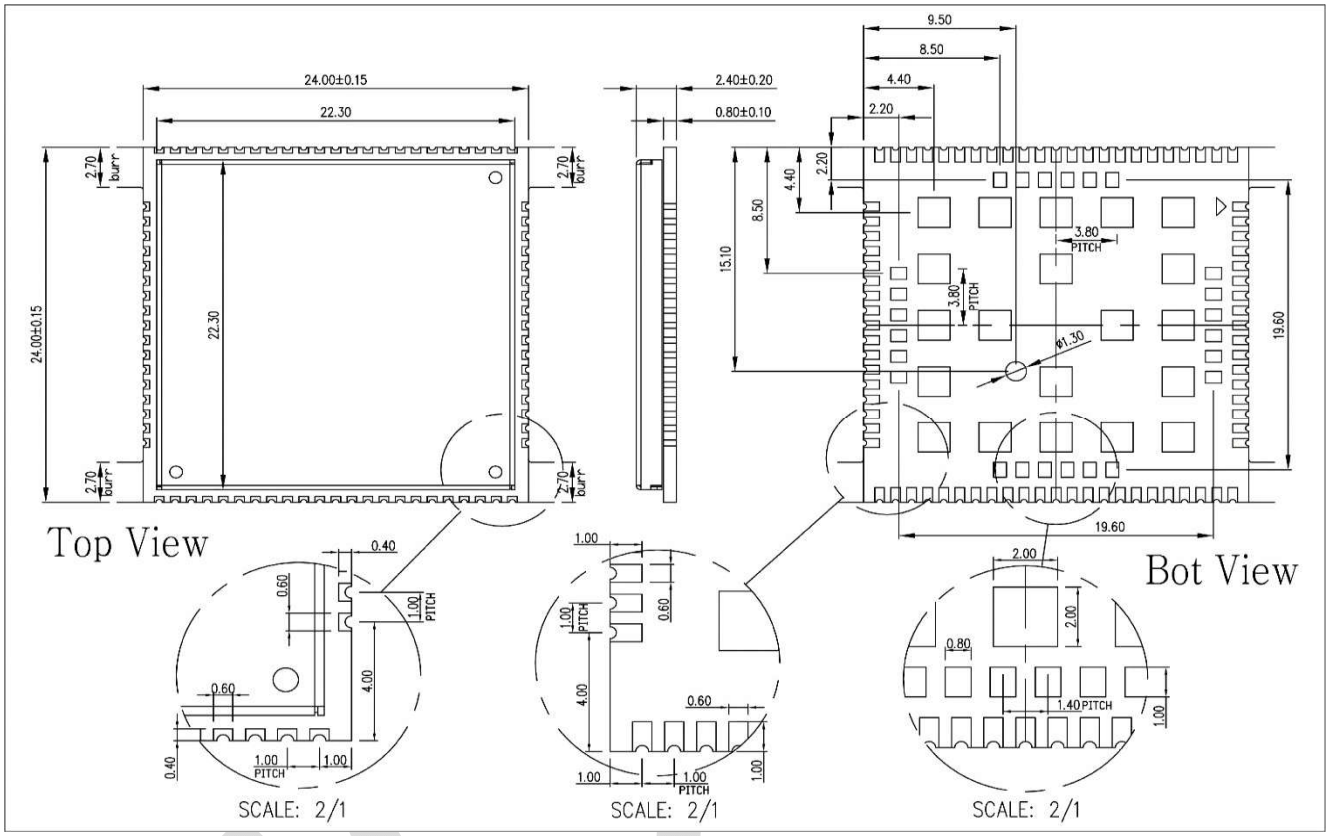

Figure 3: Dimensions (Unit: mm)

NOTE

The side length dimension is 24.00±0.15mm excluding the burr area.

3. Interface Application

3.1. Power Supply

The module offers 3 power supply pins (55, 56, 57) as VBAT power input pin. IQ10 uses these three pins supply the internal RF and baseband circuit.

When the module is transmitted at maximum power in LTE mode, the current may reach a high value instantaneously, please ensure that the external power supply capacity is no less than 1A.

Table 8: Power interface pins definition

Pin name	Pin No.	I/O	Description	Note
VBAT	55,56,57	PI	Module input voltage ranges from 3.4V to 4.2V, typical values is 3.8V.	-
GND	2,17,18,29,39,45,46,54,58,59,61,62,63,64,65,69,70,71,72,73,74,75,76,77,78,79,80,81,82, 83,84,85,86,87,88,89,91,92,94			

Table 9: VBAT pins electronic characteristic

Parameter	Description	Min.	Typ.	Max.	Unit
VBAT	Module supply voltage	3.4	3.8	4.2	V
$I_{VBAT\ (peak)}$	Module consumption peak current	-	700	850	mA
$I_{VBAT\ (power\text{-}off)}$	Module average consumption current (off leakage current)	-	1	-	uA

NOTE

Test condition: VBAT power supply 3.8V, the module is tested on EVB board, and the power input has a 100uF tantalum capacitor.

3.1.1. Power Supply Design Guide

In the customer's design, special attention must be paid to the design of the power supply. If the voltage drops below 3.4V, the RF performance of the module will be affected, the module will shut down if the voltage is too low. It is recommended to select an LDO or DC-DC chip with an enable pin, and the enable pin is controlled by the MCU.

NOTE

Ensure that the power supply can provide a continuous current of 1A, and the total capacitance of the external power supply capacitor is recommended to be no less than 100uF.

It is recommended to place four 10PF/33PF/0.1UF/1UF ceramic capacitors near VBAT to improve RF performance and system stability. At the same time, it is recommended that the VBAT layout routing width from the power supply on the PCB to the module be at least 1mm. Reference design recommendations are as follows:
If the VBAT input contains high-frequency interference, it is recommended to add magnetic beads for filtering. The recommended types of magnetic beads are BLM21PG300SN1D and MPZ2012S221A.
The reference design is recommended below:

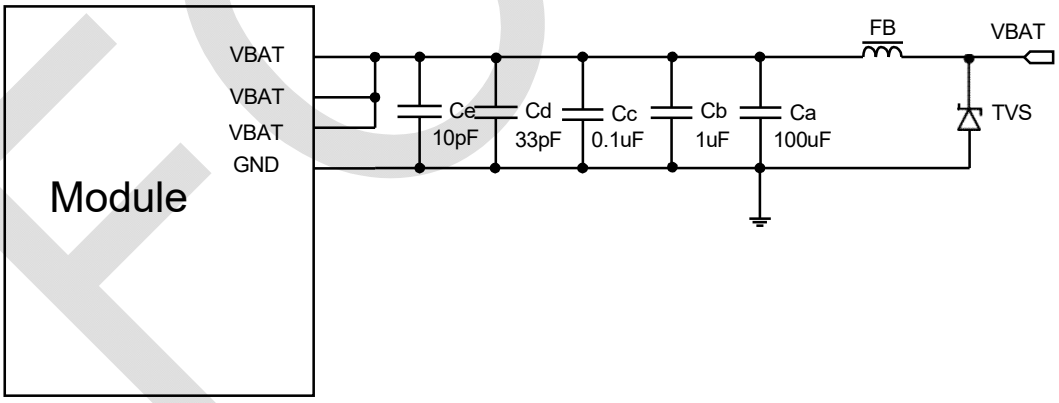

Figure 4: Power supply application circuit

In addition, in order to prevent the damage of IQ10 caused by surge and overvoltage, it is recommended to parallel one TVS on the VBAT pin of the module.

Table 10: TVS for VBAT part number list

Manufacturer	Part Number	V_{RWM}	$V_C$max	P_{PP}max	$C_J$max	Package
WILL	ESD56301D05-2/TR	5V	9.5V	1500W	700pF	DFN1610-2L
WILL	ESD56301D04-2/TR	4.85V	11V	2000W	480pF	DFN1610-2L
WAYON	WS2057KP	5V	12V	2040W	700pF	DFN1610-2L
WAYON	WS4.5DPHXM	4.85V	11V	2255W	700pF	DFN1610-2L

NOTE

When selecting TVS by customer, it is necessary to pay attention to the clamping voltage in the case of surge protection. The clamping voltage should not be higher than 6V when 100V surge input.

3.1.2. Recommended Power Supply Circuit

In order to avoid damaging the module, please do not cut off the power supply when module works normally. Only after the module is shut down by PWRKEY or AT command, the power supply can be cut off.
It is suggested that customer's design should have the ability to cut off the power supply for module in abnormal state, and then switch on the power to restart the module.
The PWR_CTRL signal indicates that the module is connected to the host and can be controlled.
When the input power is greater than 9V, the DCDC chip is recommended. When the input is less than 9V, it is recommended to use LDO power supply. The following figure shows the DC-DC regulator reference circuit:

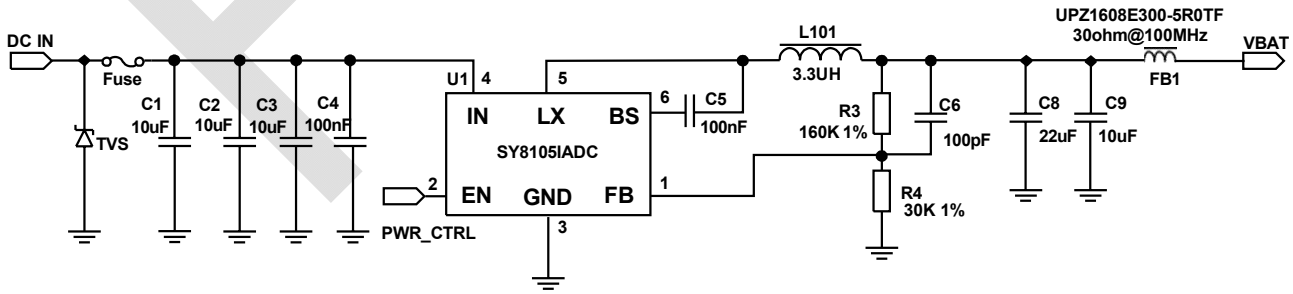

Figure 5: Power supply reference circuit

When the VBAT power is turned off, the voltage should decrease rapidly. To avoid voltage anomalies, when the VBAT is lower than the minimum value, it must be pulled below 100mV for at least 2 second before the system is powered up again.

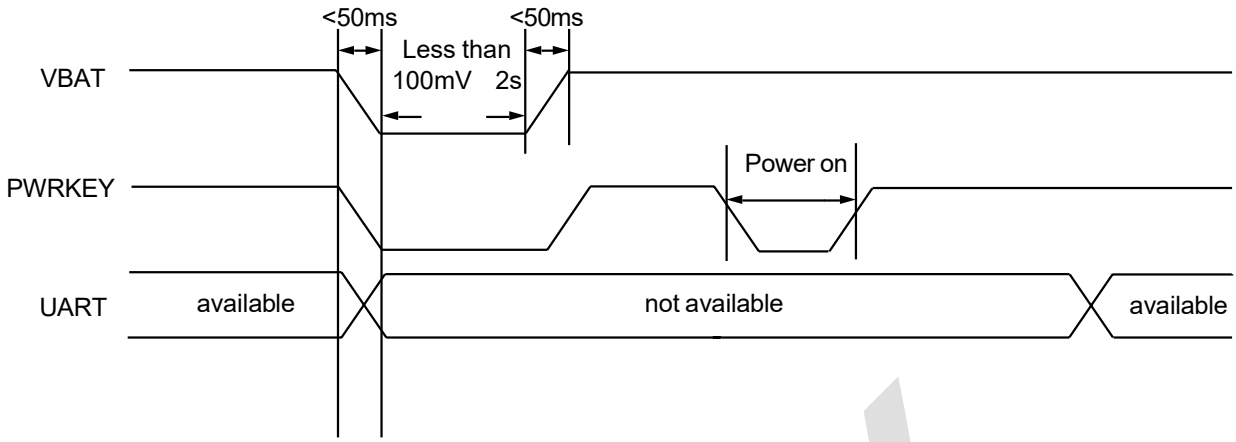

Figure 6: Power-off and power-on restart sequence

3.1.3. Voltage Monitor

AT command 'AT+CBC' can be used to monitor VBAT voltage.
AT command 'AT+CVALARM' can be used to set high/low voltage alarm, when the actual voltage exceeds the preset range, a warning message will be reported through the AT port.
AT command 'AT+CPMVT' can be used to set high/low voltage power off, when the actual voltage exceeds the preset range, the module will shut down automatically.

NOTE

Overvoltage alarm and overvoltage shutdown are off by default. For details of AT commands, please refer to document [1].

3.2. Power On/ Off and Reset

3.2.1. Power on

Table 11: PWRKEY interface pin definition

Pin name	Pin No.	I/O	Description	Note
PWRKEY	1	DI,PU	System power on/off control input, active low .	

Customer can power on the module by pulling down the PWRKEY pin. It is recommended to add TVS diode near the module pin for ESD performance. The recommended circuit is as follows:

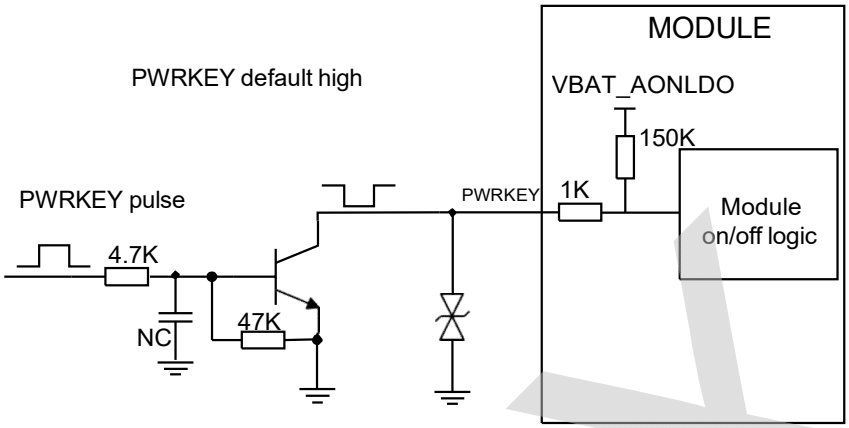

Figure 7: Reference power on/off circuit

NOTE

1. It is forbidden to pull down both RESET key and PWRKEY to power on the module at the same time.
2. If there is more than 1.3V remaining voltage before the module VBAT is powered on, the module automatically starts when it is powered on.
3. The PWRKEY is triggered by edge, it is recommended use default pull down GPIO on the collector of triode, to avoid the impulse power on the module unexpectedly. If customer need debounce function, please contact with FAE to import it.

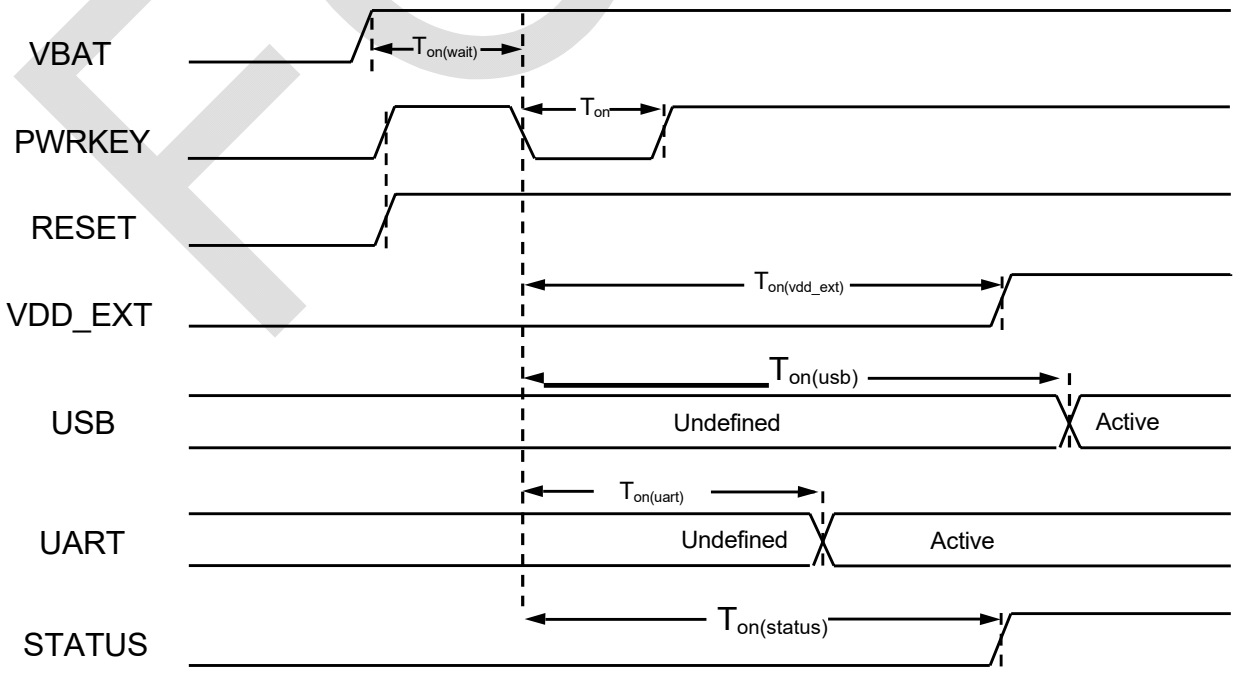

Figure 8: Power on sequence

Table 12: Power on timing and electronic characteristic

Symbol	Parameter	Min.	Typ.	Max.	Unit
$T_{on(wait)}$	The time from VBAT power-on stabilization to PWRKEY pin pull-down validity	40	-	-	ms
T_{on}	The time of active low-level impulse of PWRKEY pin to power on module	-	50	-	ms
$T_{on(vdd\_ext)}$	Output time of VDD_EXT	-	306	-	ms
$T_{on(status)}$	The time from power-on issue to STATUS pin output high level (indicating power up ready)	-	320	-	ms
$T_{on(uart)}$	The time from power-on issue to UART port ready	-	55	-	ms
$T_{on(usb)}$	The time from power-on issue to USB port ready	-	650	-	ms
V_{IH}	Input high level voltage on PWRKEY pin	-	2.1	-	V
V_{IL}	Input low level voltage on PWRKEY pin	0	0	0.4	V

3.2.2. Power off

The following methods can be used to power off the module.

- Power off by pulling the PWRKEY pin down to a low level for 2.5s.
- Power off Module by AT command 'AT+CPOF'.
- Over-voltage or under-voltage automatic power off, the voltage range can be set by 'AT+CPMVT'.
- Over-temperature or under-temperature automatic power off.

It is strongly recommended that the customer use PWRKEY or 'AT+CPOF' to shut down, and then cut off VBAT (especially when the module does not need to work). In addition, the customer cannot shut down VBAT by disconnecting it, which may cause damage to flash.

NOTE

1. When the temperature exceeds the range of - 30 ~ + 75 ℃, IQ10 will report warning information through AT port. When the temperature exceeds the range of - 40 ~ + 85 ℃, IQ10 will shut down automatically. For a detailed description of 'AT+ CPOF' and 'AT+ CPMVT', please refer to document [1].
2. The VBAT voltage must fall below 1.3V before power on. Otherwise, the module will restarts automatically.

PWRKEY can be used to power off the module. For power off sequence, please see the following figure:

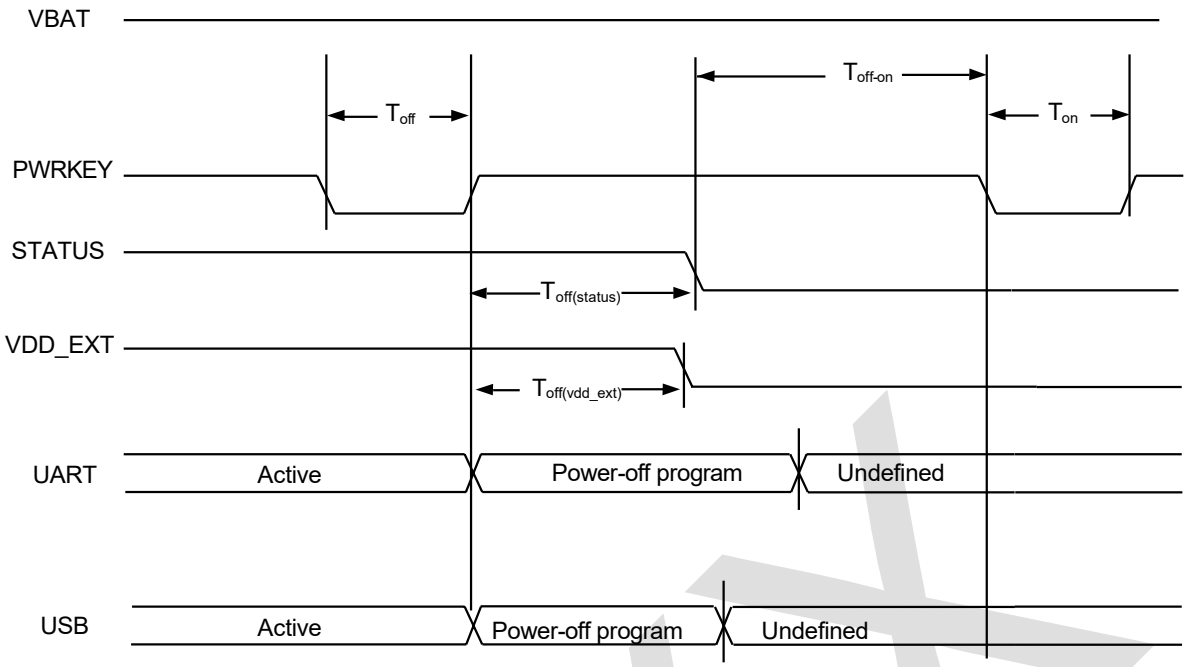

Figure 9: Power off timing sequence

Table 13: Power off sequence parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{off}	Power off low level pulse width	2.5	-	-	s
$T_{off(vdd\_ext)}$	VDD_EXT shutdown time	-	340	-	us
$T_{off(status)}$	Power off time (according to status interface)	-	480	-	us
$T_{off(uart)}$	Power off time (according to UART interface)	-	2.4	-	ms
$T_{off(usb)}$	Power off time (according to USB interface)	-	690	-	us
T_{off-on}	Power off - power on buffer time	2	-	-	s

NOTE

The status pin can be used to judge whether the module is powered on or not. When the module is powered on and initialization is completed, the status outputs a high level, otherwise the low level will be maintained all the time.

3.2.3. Reset Function

Table 14: RESET interface pin definition

Pin name	Pin No.	I/O	Description	Note
RESET	16	DI,PU	System reset control input, active low.	

The module can be reset by pulling down the reset pin to a low level.
The recommended circuit is showed as follows:

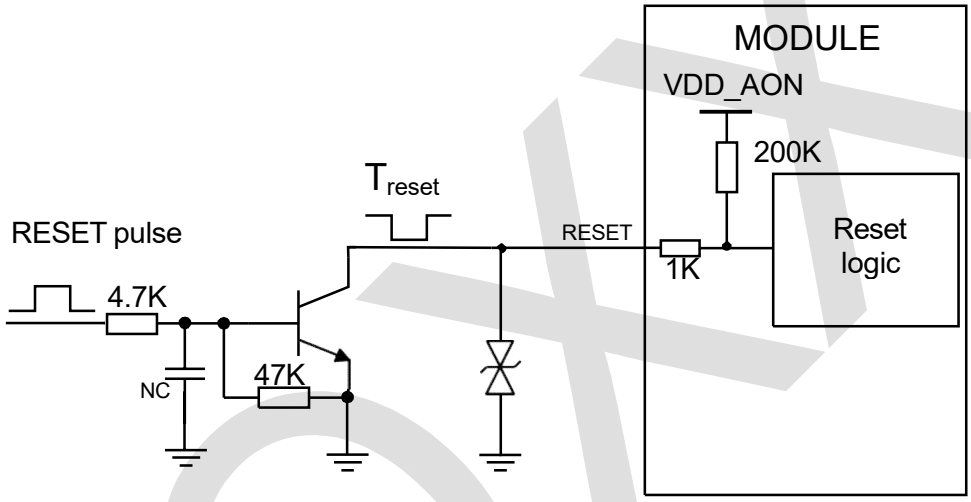

Figure 10: Reference reset circuit

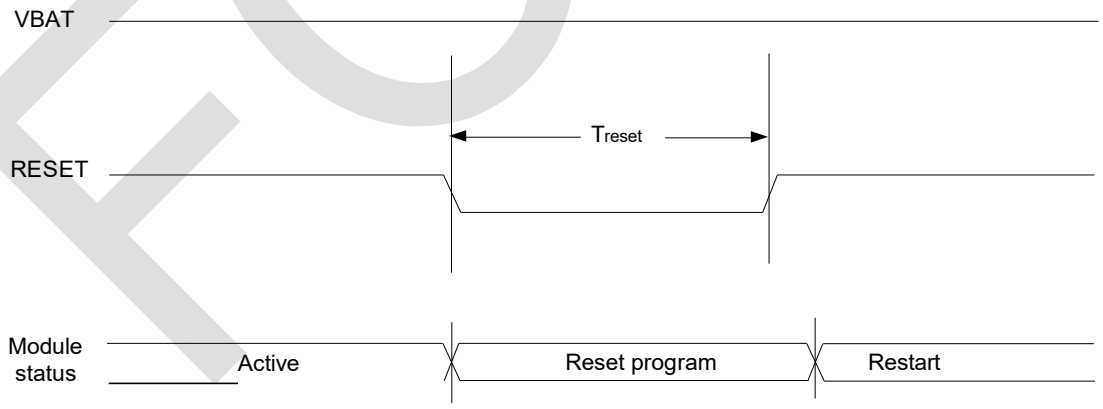

Figure 11: Reset timing sequence

Table 15: RESET pin electronic characteristic

Symbol	Description	Min.	Typ.	Max.	Unit
T_{reset}	The active low level time impulse on RESET pin to reset module	-	0.5	-	s

V_{IH}	Input high level voltage	-	1.2	-	V
V_{IL}	Input low level voltage	-0.3	0	0.4	V

NOTE

1. It is recommended to use the reset pin only in case of emergency, such as the module is not responding. The reset time is recommended to be 0.5s.
2. The RESET is triggered by edge without debounce, it is recommended use default pull down GPIO on the collector of triode, and add RC filter, to avoid the impulse reset the module unexpectedly.

3.3. UART Interface

The module provides three serial ports, the main communication serial port is MAIN_UART, one ordinary serial port for GNSS communication, and the DEBUG_UART dedicate to print log.

Table 16: UART interface pins definition

Pin name	No.	Power domain	Type	Description	Note
Full function UART interface					
MAIN_UART_RTS	8	1.8V	DI	DTE request to send signal to DCE	If unused, keep it open.
MAIN_UART_CTS	7	1.8V	DO	DTE clear to send signal from DCE	
MAIN_UART_RXD	10	1.8V	DI	Data input	
MAIN_UART_TXD	9	1.8V	DO	Data output	
MAIN_UART_RI*	4	1.8V	DO	Ringing indicator	
MAIN_UART_DCD	5	1.8V	DO	Carrier detection	
MAIN_UART_DTR*	3	1.8V	DI	DTE Ready	
Debug UART					
DEBUG_UART_TX	23	1.8V	DO	Debug UART, the boot log will be output during boot up.	Default used as debug port.
DEBUG_UART_RX	22	1.8V	DI		
AUX_UART					
AUX_UART_TXD	50	1.8V	DO	Data output	Two-wire serial port.
AUX_UART_RXD▲	49	1.8V	DI	Data input	

3.3.1. UART Design Guide

When customer uses full-function serial port, please refer to the following connection mode:

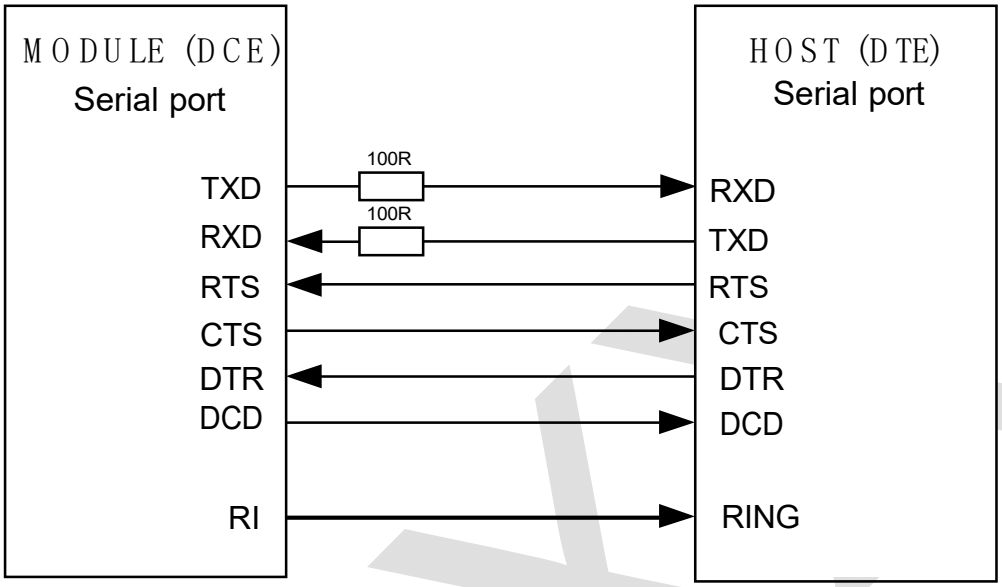

Figure 12: Serial port connection diagram (full-function mode)

When using 2-wire serial port, please refer to the following connection mode:

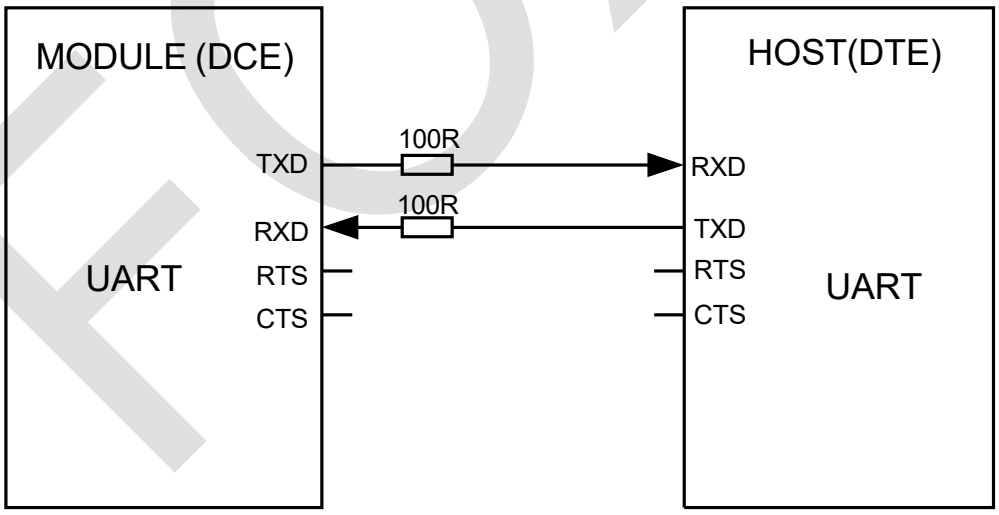

Figure 13: Serial port connection diagram (NULL mode)

The following figure shows the use of triode for level shifter circuits. Please pay special attention to the direction of signal.
The recommended triode model is MMBT3904. The RTS/CTS and other GPIOs is similar with TXD/RXD if needed.

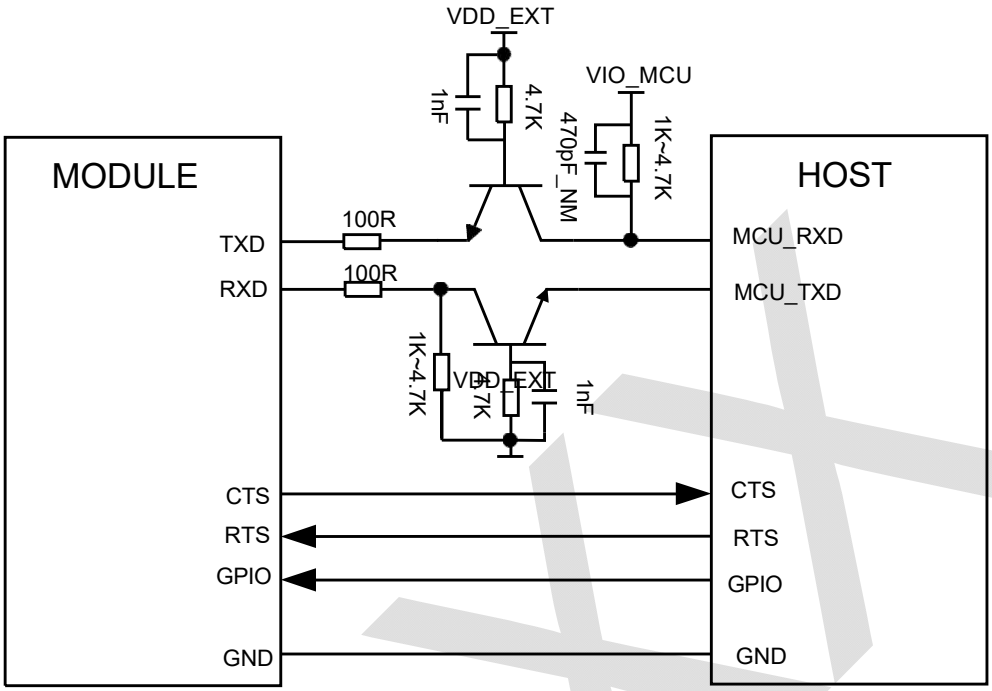

Figure 14: Triode level conversion circuit

NOTE

1. Main UART supports the following baud rates: 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400,460800 and 921600. The default baud rate is 115200bps.
2. The maximum baud rate supported by IQ10 ordinary serial port is 921600bps.
3. The parasitic capacitance of the transistor will affect the edge of the high-speed digital signal. It is not recommended to use this circuit when the signal speed is higher than 115200bps.
4. To ensure the stability of UART data transmission, it is recommended that the serial baud rate should not exceed 9600bps when setting continuous transmission (without inserting delay) and not enabling flow control function; When the baud rate is greater than 9600bps, it is recommended to insert a 50ms delay for every 256 bytes sent and add UART hardware flow control design.

3.3.2. RI and DTR Behavior

RI usually keeps high level output. When receiving a short message or URC report, RI outputs a low level for 120ms (short message)/60ms (URC), and then returns to a high-level state.

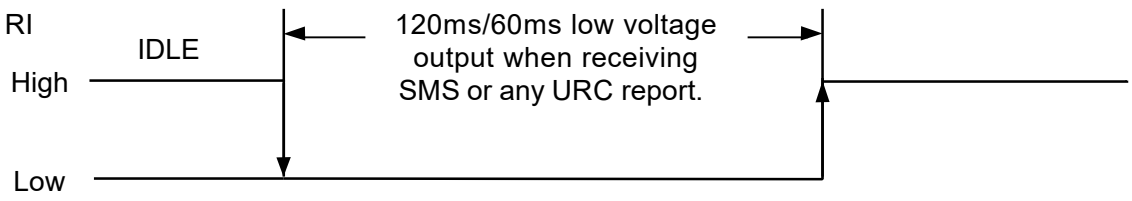

Figure 15: RI behaviour (SMS and URC report)

After setting the AT command “AT+CSCLK=1”, and then pulling up the DTR pin, module will enter into the sleep mode from the idle mode. In sleep mode, the UART is unavailable. When IQ10 enters into the sleep mode, pulling down DTR can wake up the module.
After setting the AT command “AT+CSCLK=0”, IQ10 Series remain still when the DTR pin is pulling up.

NOTE

After the module has entered into sleep mode, customers can pull DTR down to GND to wake up the module.

3.4. USB Interface

The module contains a USB interface, which complies with the USB2.0 specification as a peripheral, but does not support USB charging function and USB HOST mode.

USB supports high speed mode (480Mbps) and full speed mode (12Mbps), it is used for AT command communication, data transmission, GNSS NMEA output, firmware upgrade and software debugging.

It is recommended to reserve USB test points during design. If a main control chip is connected, 0R resistors must be reserved for switching external test points during design, as shown in the figure below.

Table 17: USB interface pins definition

Pin name	No.	Power domain	Type	Description	Note
VBUS▲	24	-	PI	Valid USB detection input. Active high, V_{min}=3.3V, V_{max}=5.2V, V_{norm}=5V	Necessary for USB port enumerate.
USB_DN	28	-	AIO	Negative electrode of the differential, bi-directional USB signal.	
USB_DP	27	-	AIO	Positive electrode of the differential,	

				bi-directional USB signal.	

3.4.1. USB Reference Design

The module can be used as a USB slave device. The recommended connection circuit diagram is as follows:

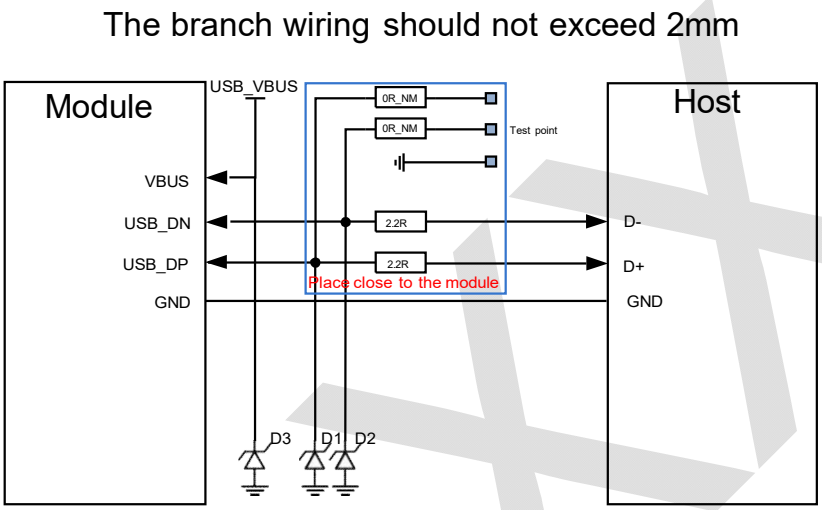

Figure 16: USB circuit diagram

In use should pay attention to the selection of D3 devices, it is recommended to choose anti-static and surge TVS devices, recommended models are shown in Table 18.

USB_VBUS is the USB detection pin for module, it's active high and the available identification voltage is 3.0V~5.2V, generally recommend to connect to the VBUS signal of external USB connector or of MCU, it also can be connected to other power supplies, such as the VBAT. If the USB_VBUS pin is connected to the power supply, it's recommended to reserve a switch circuit to ensure that the power supply can be turned off then turn it on, that make USB enumerating afresh.

Table 18: Recommended TVS Diodes for VBUS

Manufacturer	Part Number	V_{RWM}	$V_{C(max)}$	$C_{J(max)}$	Package
WAYON	WS07DP	7V	20V	1000pF	DFN1610-2L
PRISEMI	PTVSHC2EN7VU	7V	24V	750pF	DFN1610-2L
BILLSEMI	BLE7V065B6U	7V	16V	500pF	DFN1610-2L
LRC	LTVS16H7.0T5G	7V	15V	750pF	DFN1610

Table 19: Recommended TVS Diodes for USB_DP and USB_DN

Manufacturer	Part Number	V_{RWM}	$V_{C(max)}$	$C_{J(max)}$	Package
WILL	ESD9X5VU-2/TR	5V	8V	0.9pF	WBFBP-02C
LRC	LESD9L5.0T5G	5V	9.8V	0.9pF	SOD-923
WAYON	WE05DUCF	5V	14V	0.7pF	DFN1006-2L
ON	ESD9L5.0ST5G	5V	9.8V	0.9pF	SOD-923

If customer has a low power consumption demand, it is recommend add a P-MOS on the VBUS. When the module enter sleep, the VBUS must be disconnected.
If the USB HUB/SWITCH is used, the reset function is required for the Module and HUB/SWITCH either.

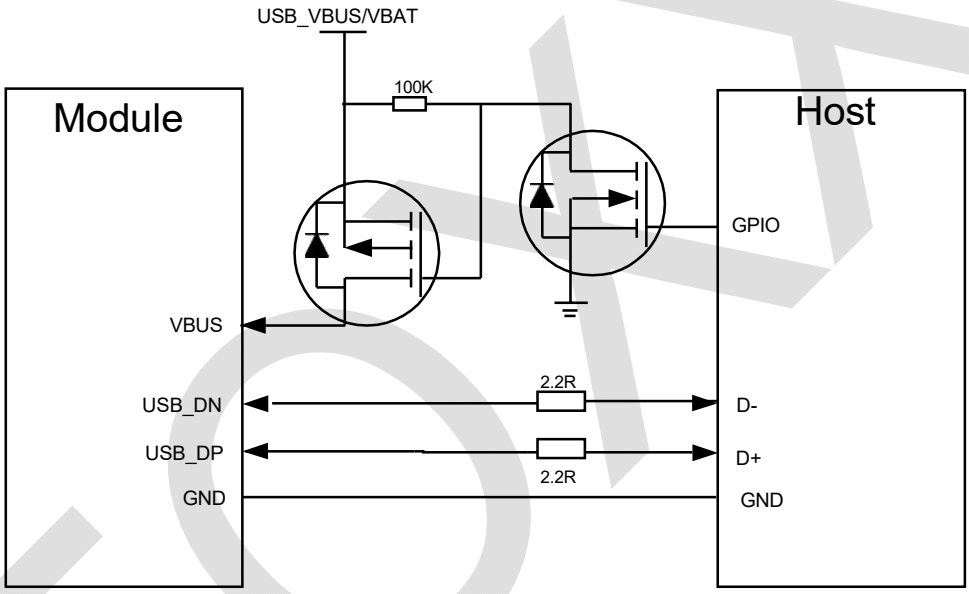

Figure 17: VBUS circuit diagram

NOTE

1. The USB data cable must be strictly routed in 90Ω +/- 10% differential. The TVS devices D1 and D2 on the data line must be selected with equivalent capacitance less than 1pF. The TVS device should be placed near the USB connector or test point, the recommended models are shown in Table 19.
2. Trace routes should be away from other sensitive signals (RF, audio, and XO).
3. The detection of USB2.0 speed is determined automatically by the USB protocol.
4. There is no need to pull up the DP external, since it may affect the device USB enumeration.
5. The software version after 240109 must require VBUS connection when USB load, otherwise the USB port will not be usable.
6. The minimum valid VBUS voltage required 3.6V if the date of manufacture before 2409.

3.4.2. USB_BOOT Interface

The module provides one forced download boot interface 'USB_BOOT'.

Table 20: USB_BOOT interface pin definition

Pin name	No.	Power domain	Type	Description	Note
USB_BOOT●	6	1.8V	DI	Firmware download guide control input. When pull-down to GND and press PWRKEY, module will access in USB download mode.	Please reserve 2 test points for debug. Do not pull down USB_BOOT during normal power on!

If the module fails to boot, customers can force upgrade through the USB_BOOT port.
Before the module is powered on, pull down the USB_BOOT pin to GND, then apply VBAT power to the module, and press PWRKEY to enter the download mode. After entering the download mode, release USB_BOOT and remove the pull-down.

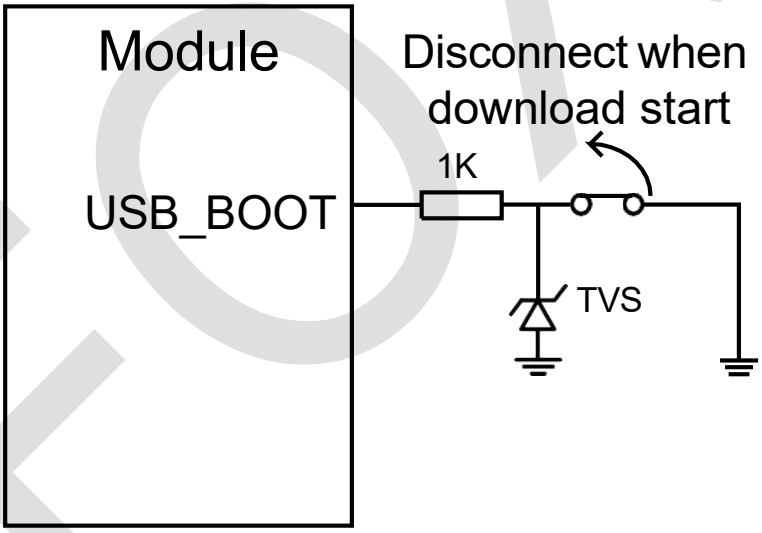

Figure 18: Reference USB_BOOT circuit

Customers will see the download port in the device manager port of the windows system.

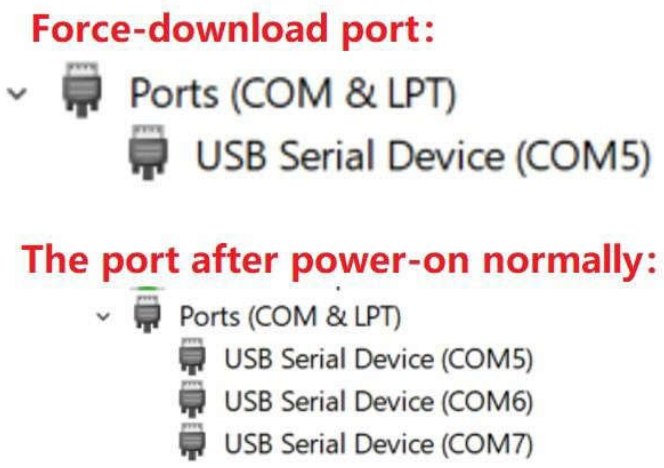

Figure 19: USB port

NOTE

1.USB_BOOT is the download control pin, this pin cannot be pulled down before the normal power on. Otherwise, it will enter the download mode.
2. The USB_BOOT has been pulled up internally, do not pull it up to VDD_EXT or any other power supply!
3. It is recommended to reserve test point to facilitate debugging and upgrading.

3.5. USIM Interface

The module supports both 1.8V and 3.0V USIM cards. The interface power of the USIM card is provided by the voltage regulator inside the module.

Table 21: USIM interface pins definition

Pin name	No.	Power domain	Type	Description	Note
SIM_DATA	31	1.8/3.0V	I/O,PU	SIM data signal.	This pin has been pull-up with 4.7KΩ resistor to SIM_VDD internally.
SIM_RST	33	1.8/3.0V	I/O,PU	SIM RST signal reset output.	
SIM_CLK	32	1.8/3.0V	I/O,PU	SIM CLK signal clock output.	
SIM_VDD	30	1.8/3.0V	PO	SIM card power supply output.	Supports 1.8V/3.0V output according to the card type, its

					output current is up to 34mA.
SIM_DET	34	1.8V	I/O,PU	SIM card insert detect.	It can be set to high/low active with the AT command, refer to document [18]

Table 22: USIM electronic characteristic in 1.8V mode (SIM_VDD=1.8V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{SIM_VDD}	LDO power output voltage	1.75	1.8	1.85	V
V_{IH}	High-level input voltage	0.7 * SIM_VDD	-	-	V
V_{IL}	Low-level input voltage	-	0	0.2 * SIM_VDD	V
V_{OH}	High-level output voltage	0.8 * SIM_VDD	-	-	V
V_{OL}	Low-level output voltage	-	0	0.15 * SIM_VDD	V

Table 23: USIM electronic characteristic in 3.0V mode (SIM_VDD=3V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{SIM_VDD}	LDO power output voltage	2.95	3	3.05	V
V_{IH}	High-level input voltage	0.7 * SIM_VDD	-	-	V
V_{IL}	Low-level input voltage	-	0	0.2 * SIM_VDD	V
V_{OH}	High-level output voltage	0.8 * SIM_VDD	-	-	V
V_{OL}	Low-level output voltage	-	0	0.15 * SIM_VDD	V

3.5.1. USIM Application Guide

It is recommended to use ESD protection component. Note that the USIM peripheral circuit should be close to the USIM card socket. The following figure shows the 6-pin SIM card holder reference circuit.

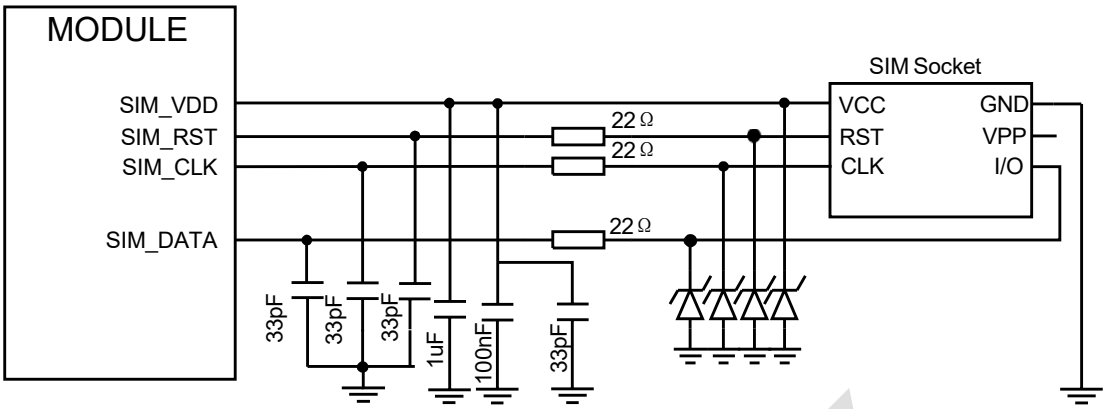

Figure 20: SIM interface reference circuit

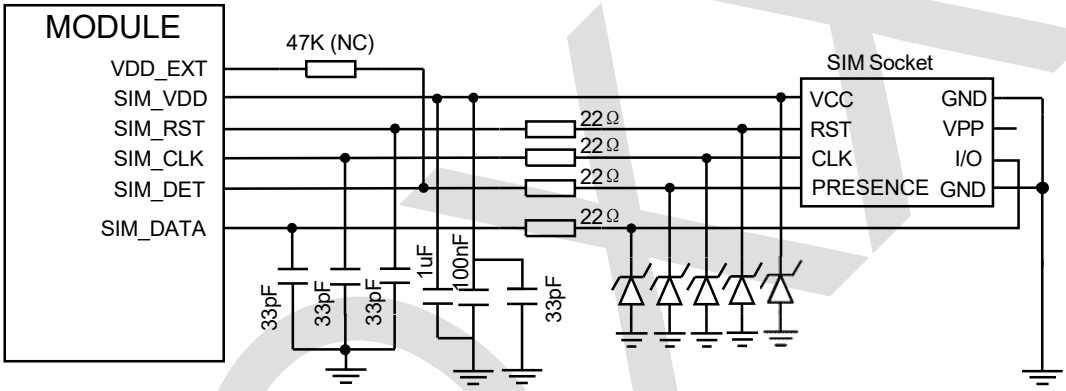

Figure 21: SIM interface reference circuit (8PIN)

NOTE

1. SIM_DATA has been pulled up with a 4.7KΩ resistor to SIM_VDD in module.
2. A 100nF capacitor on SIM_VDD is used to reduce interference.
3. Using “AT+UIMHOTSWAPON=0 or 1” to enable SIM card hot swap function. This function is disabled by default.
4. Using "AT+UIMHOTSWAPLEVEL=0 or 1"AT command to set the USIM card detection level to adapt to the signal logic.
5. For more details of AT commands about USIM, please refer to document [1].

The circuit of the USIM card is easy to be interfered with, resulting in the failure to recognize or drop the card, etc. so please follow the following principles during the design:

- Be sure to keep the USIM socket away from the main antenna during the PCB layout phase.
- USIM card traces should be away from RF, VBAT and high speed signals, at the same time the USIM card traces should be as short as possible.
- Keep the USIM socket’s GND pin directly connected to the main ground.

- To prevent SIM_CLK from other signal interference, it is suggested to make separate package to protect SIM_CLK processing.
- Place TVS near the USIM socket, and the parasitic capacitance of TVS should not be greater than 15pF, such as WS03DTUMS-B.
- Connect 22 Ω resistors in series between USIM socket and module can enhance ESD protection performance.
- The rise/fall time of SIM_CLK should not exceed 40ns.

Table 24: TVS for USIM socket part number list

Manufacturer	Part Number	V_{RWM}	$V_{C}max$	$P_{PP}max$	$C_{J}max$	Package
WAYON	WS03DTUMS-B	3.3V	8V	35W	0.7pF	DFN0603-2L
WILL	ESD9X5VU-2/TR	5V	8V	72W	0.9pF	DFN1006-2L

3.6. I2C Interface

The module provides one I2C interface, which supports standard speed clock frequency 100Kbps and high speed clock frequency 400Kbps. Its operation voltage is 1.8V.

Table 25: I2C interface pins definition

Pin name	No.	Power domain	Type	Description	Note
I2C_SCL	38	1.8V	OD	I2C clock output	If unused, keep it open. Need pull up to VDD_EXT externally.
I2C_SDA	37	1.8V	OD	I2C data I/O	

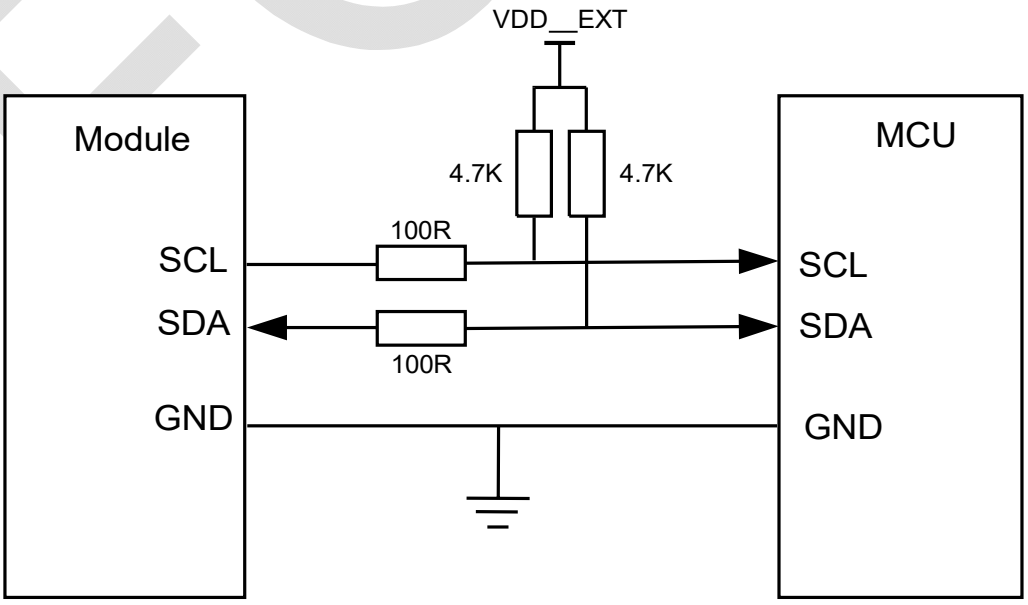

Figure 22: I2C reference circuit

NOTE

1. I2C_SCL and I2C_SDA have no pull-up resistor inside, external resistor is needed.
2. It is recommended to connect a 100R resistor in series with the I2C signal line close to the module terminal to reduce overshoot on the signal line.

3.7. GPIO Interface

The module provides multiple GPIOs.

Table 26: Standard GPIO Resources of IQ10

Pin No.	Pin name	AT command operation GPIO number	Pin typ.	Power domain	Default Type	Pad Edge wakeup
19	GPIO1	GPIO1	IO	1.8V	PU	NO
21	GPIO3	GPIO3	IO	1.8V	PU	NO
26	GPIO4	GPIO4	IO	1.8V	PD	NO
35	GPIO5	GPIO5	IO	1.8V	PU	NO
36	GPIO6	GPIO6	IO	1.8V	PU	NO
44	GPIO7	GPIO7	IO	1.8V	PU	NO
47	GPIO8	GPIO8	IO	1.8V	PU	NO
48	GPIO9	GPIO9	IO	1.8V	PD	NO
53	GPIO10	GPIO10	IO	1.8V	PU	NO
67	GPIO11	GPIO11	IO	1.8V	PU	NO
68	GPIO12	GPIO12	IO	1.8V	PU	NO

NOTE

After the platform goes into sleep mode, the regular GPIO of default type PU will follow the DRX pattern and generate pulses. It is recommended not to use regular GPIO while in sleep mode.

3.8. STATUS Interface

The STATUS pin can be used to determine whether the module is powered on or not. When the module is

powered on and initialization is complete, the status output is high, otherwise it will remain low.

Table 27: STATUS interface pin definition

Pin name	No.	Power domain	Type	Description	Note
STATUS*	42	1.8V	DO	Module operation status indication	If unused, keep it open.

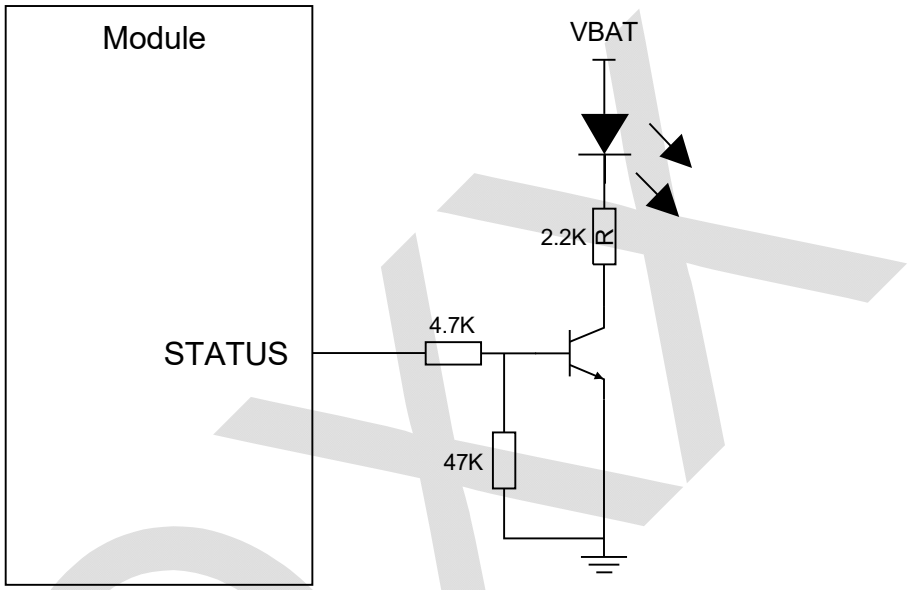

Figure 23: STATUS reference circuit

NOTE

The value of the resistor named “R” depends on the LED characteristic.

3.9. Network Status

Table 28: NETLIGHT interface pin definition

Pin name	No.	Power domain	Type	Description	Note
NETLIGHT*	52	1.8V	DO	Network registration status indicator (LED).	

The NETLIGHT pin is used to control Network Status LED, its reference circuit is shown in the following

figure.

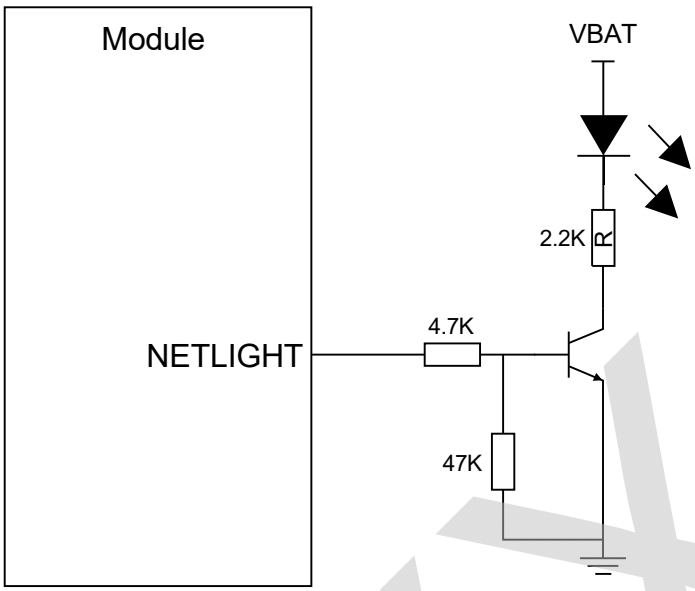

Figure 24: NETLIGHT reference circuit

NOTE

The value of the resistor named “R” depends on the LED characteristic.

The NETLIGHT signal is used to control the LED light that indicates the status of the network. The working status of this pin is shown in the table below.

Table 29: LTE mode NETLIGHT pin status

NETLIGHT pin status	Module status
Always On	Searching Network
200ms ON, 200ms OFF	Data Transmit/Registered
OFF	Power off / Sleep

3.10. GNSS Interface

The module supports GNSS function interface. GNSS provides 2 power supply input interfaces, 2 GNSS power enable control switch, 1 reset interface, 1 debug interface, 1 UART interface and 1 pulse synchronous clock signal interface, which are described in detail as follows.

Table 30: GNSS interface description

PIN Name	PIN NO	I/O	Description	Note
GNSS_VBKP	116	PI	GNSS backup power input	Power supply ranges from 2.0V to 3.6V, suggest 2.8V power supply. Cannot be open.
GNSS_VDD	97	PI	GNSS VSYS input	The power supply voltage must be no less than 1.75V and no more than 1.9V, typically 1.8V. The cable must be as short as possible, with a cable width of more than 0.3mm.
GNSS_PWRCTL	98	DI	GNSS's internal Vcore power enable control	Active high. Solution 1: Use 10K resistor in series to connect to GPIO2 (PIN20). Solution 2: Use 10K resistor in series to connect to MCU GPIO.
GPIO2*	20	DO	Use 10K resistor in series to connect to GNSS_PWRCTL(PIN98)	Only can be used for GNSS_PWRCTL, it does not support general purpose I/O.
GNSS_VDD_EN	40	DI	GNSS's internal system power enable control	Only at standalone mode it can be used by connecting to MCU GPIO with 0R resistor in series. If unused, keep it open.
GNSS_RXD	96	DI	GNSS UART RXD	1.8V power domain. Solution 1: Use 1K resistor in series to connect AUX_UART_TXD (PIN50) of the module. Solution 2: Use 1K resistor in series to connect to MCU UART_TXD.
GNSS_TXD	95	DO	GNSS UART TXD	1.8V power domain. Solution 1: Use 1K resistor in series to connect AUX_UART_RXD (PIN49) of the module. Solution 2: Use 1K resistor in series to connect to MCU UART_RXD.
1PPS◆	100	DO	GNSS pulse synchronous clock signal	Seconds pulse signal, do not pull up before starting GNSS. It can be used for accurate timing. Output pulse signal approximately 30 seconds after successful positioning. If unused, keep it open.
GNSS_DEBUG_TX◆	115	DO	GNSS debug TXD	
GNSS_DEBUG_RX	111	DI	GNSS debug RXD	
GNSS_RST_N	114	AI	GNSS RST interface	Internal pull up, active low.

GNSS recommended reference design solution 1:
IQ10 module itself provides power, power enable and UART transmission to GNSS.
A load switch on GNSS_VDD is recommended, customer can shut off the GNSS_VDD and GNSS_VCORE by send “AT+CGNSSVCORE=0” to enter RTC mode, it will decrease about 70uA of VBAT current consumption while the module is power on or sleep.
The recommended reference design is as follows:

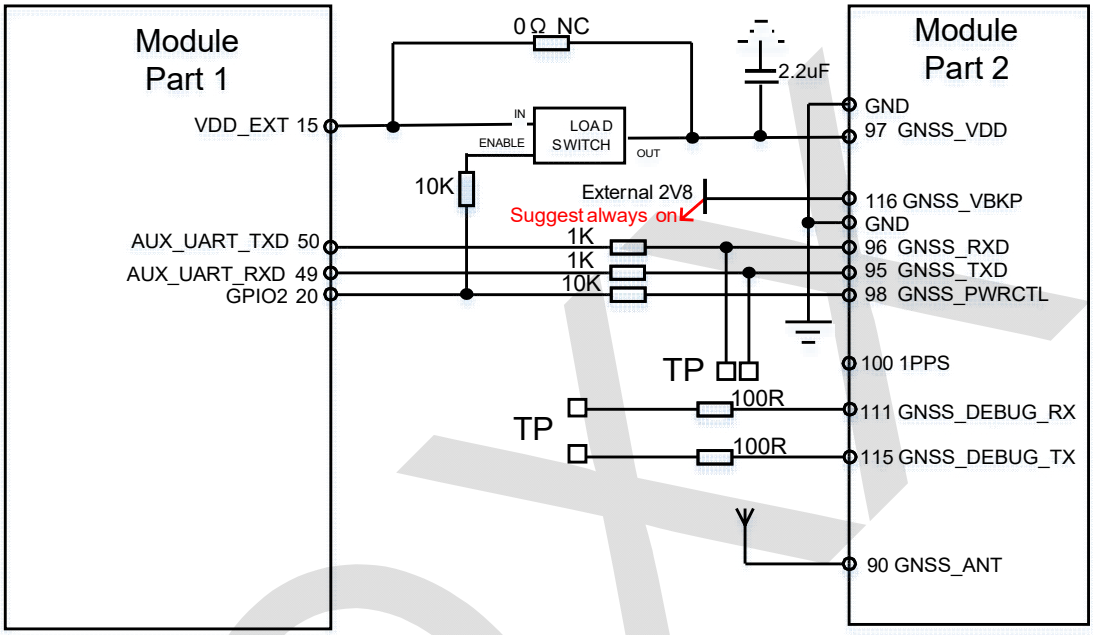

Figure 25: GNSS reference design (Non-standalone GNSS solution)

GNSS recommended reference design solution 2:
The external MCU provides power, power enable and UART transmission to GNSS, this solution is used for scenarios where GNSS can work standalone without the module powering up. The recommended reference design is as follows:

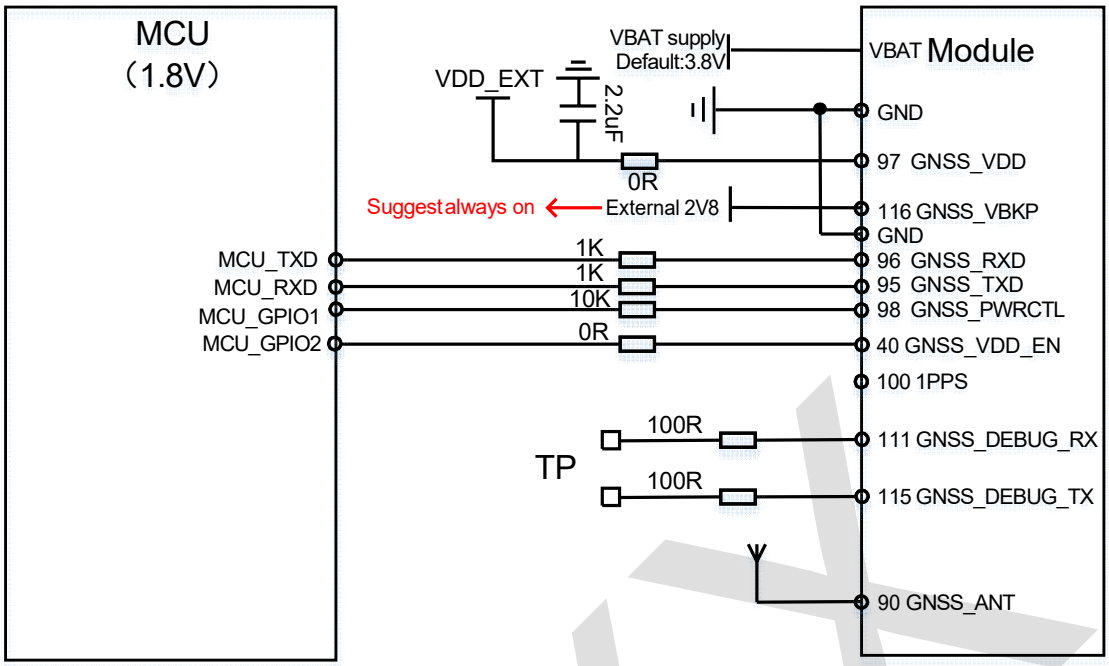

Figure 26: GNSS reference design (Standalone GNSS solution)

NOTE

1. Please place 1K resistors in series for serial communication lines to prevent leakage current to the serial ports of GNSS chip.
2. The standalone GNSS reference design is only applicable to 1.8V power domain MCU. If the MCU is not 1.8V power domain, a level shift circuit should be added.
3. The standalone GNSS design needs VBAT voltage input.
4. At standalone mode, MCU_GPIO1 and MCU_GPIO2 should be pulled up at the same time to meet the power on sequence, make sure the GNSS_VDD_EN can be drive above 1.6V.
5. The GNSS_VDD has higher requirements for power supply, PCB routing should be as short as possible, and the routing width is required to be at least 0.3mm.
6. GNSS_VBKP power supply input is a necessary condition. When 2.8V input, the typical current consumption value is 36uA.
7. Make sure to connect a 10K resistor to the GNSS_PWRCTL pin in series and then to the external enable signal.
8. In non-standalone mode, GNSS will automatically enter sleep mode when the module power on.
9. Cause of GNSS chipset characteristic, please make sure the GNSS_VDD and GNSS_PWRCTRL in on or off state simultaneously, to avoid current leakage.
10. The GNSS_VDD_EN (PIN40) is the LDO enable of VDD_EXT, do not connect them together!
11. The pins marked "◆" is forbidden to pull up before GNSS power up.

AT commands about GNSS are as following table.

Table 31: AT commands about GNSS

AT Command	Description
AT+CGNSSPWR=<n>	GNSS state control. <n>=1: Active GNSS. <n>=0: Close GNSS.
AT+CGNSSTST=<n>	Send data received from UART to NMEA port. <n>=1: Start sending data to NMEA port. <n>=0: Stop sending data to NMEA port.
AT+CGPSCOLD	Cold start GNSS.
AT+CGPSWARM	Warm start GNSS.
AT+CGPSHOT	Hot start GNSS.
AT+CGNSSSLEEP	Set GNSS into sleep mode.
AT+CGNSSWAKEUP	Wake up GNSS.
AT+CGNSSFLP=<n>	<n>=0: Disable Periodic Power Saving Mode. <n>=1: Enable Periodic Power Saving Mode.
AT+CGNSSGLP=<n>	<n>=0: Set GNSS quit low-power GLP mode. <n>=1: Set GNSS into low-power GLP mode.
AT+CGNSSFITNESS=<n>	<n>=0: Set GNSS into normal mode. <n>=1: Set GNSS into fitness mode.
AT+CGNSSALP=<n>	<n>=0: Disable both adaptive low-power power saving mode and adaptive low-power performance mode. <n>=1: Enable adaptive low-power power saving mode which might sacrifice GNSS performance in favour of a reduced power consumption. <n>=2: Enable adaptive low-power performance mode which achieves relatively good performance while keeping the power consumption low.
AT+CGNSSRTC=<n>	<n>=0: Enter RTC mode and only use external wake-up.
AT+CGNSSVCORE=<n>	<n>=0: Set GPIO2 (PIN20) output low level. <n>=1: Set GPIO2 (PIN20) output high level.

NOTE

1. Please reserve test points of GNSS_RXD and GNSS_TXD for firmware upgrade.
2. Please refer to document [1] for more AT commands about GNSS.

3.11. Other Interface

3.11.1. ADC

The module has two general ADC pins, and support VBAT ADC.

Table 32: ADC interface pins definition

Pin name	No.	Power domain	Type	Description	Note
ADC1	25	0V-1.1V	AI	General Purpose ADC	If unused, keep it open.
ADC2	51	0V-1.1V	AI	General Purpose ADC	If unused, keep it open.

The electrical characteristics are as follows:

Table 33: General ADC electronic characteristics

Characteristics	Min.	Typ.	Max.	Unit
Resolution	-	12	-	Bits
Input Range	0	-	1.1	V
Input Resistance	0.26	-	0.75	MΩ

NOTE

1. “AT+CADC=2” can be used to read the voltage of the ADC1 pin.
2. “AT+CADC2=2” can be used to read the voltage of the ADC2 pin.
3. “AT+CBC” can be used to read the voltage value of the power supply (VBAT).
4. Excessive resistance and voltage division will lead to an increase in error, suggest minimizing the resistance value as possible.
5. For more details, please refer to document [1].

3.11.2. VDD_EXT

The module provides one LDO outputs: VDD_EXT.
VDD_EXT can only provide a current capacity of 50mA. It can be used as a power supply for module

GNSS_VDD (PIN97).

Table 34: LDO output pin definition

Pin name	No.	Power domain	Type	Description	Note
VDD_EXT	15	-	PO	1.8V power output, output current up to 50 mA.	Default on. It can provide 1V8 power supply for GNSS. If unused, keep it open.

Table 35: VDD_EXT electrical characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD_EXT}	Output voltage	-	1.8	-	V
I_O	Output current	-	-	50	mA

NOTE

1. If the module enters PSM mode, the VDD_EXT will be powered off.
2. If the power damaged, it will affect the system startup, it is recommended that customers add TVS protection. The recommended model is ESD56051N.

Table 36: TVS for VDD_EXT part number list

Manufacturer	Part Number	V_{RWM}	$V_C$max	$C_J$max	Package
WILLSEMI	ESD56051N-2/TR	3.3V	10V	65F	DFN1006-2L

3.11.3. MAIN_UART_WAKEUP

The module provides a MAIN_UART_WAKEUP interface, which can connect to MAIN_UART_RXD externally to wake up the module.

Table 37: MAIN_UART_WAKEUP interface pin definition

Pin name	No.	Power domain	Type	Description	Note
MAIN_UART_WAKEUP▲	41	1.8V	DI	MAIN_UART_RXD wake-up pin.	Connect it to MAIN_UART_RXD externally if use this function.

4. RF Specifications

4.1. LTE Specifications

Table 38: Conducted transmission power

Frequency	Power	Min.
LTE-FDD B1	23dBm +/-2.7dB	<-40dBm
LTE-FDD B2	23dBm +/-2.7dB	<-40dBm
LTE-FDD B3	23dBm +/-2.7dB	<-40dBm
LTE-FDD B4	23dBm +/-2.7dB	<-40dBm
LTE-FDD B5	23dBm +/-2.7dB	<-40dBm
LTE-FDD B7	23dBm +/-2.7dB	<-40dBm
LTE-FDD B8	23dBm +/-2.7dB	<-40dBm
LTE-FDD B12	23dBm +/-2.7dB	<-40dBm
LTE-FDD B13	23dBm +/-2.7dB	<-40dBm
LTE-FDD B18	23dBm +/-2.7dB	<-40dBm
LTE-FDD B19	23dBm +/-2.7dB	<-40dBm
LTE-FDD B20	23dBm +/-2.7dB	<-40dBm
LTE-FDD B25	23dBm +/-2.7dB	<-40dBm
LTE-FDD B26	23dBm +/-2.7dB	<-40dBm
LTE-FDD B28	23dBm +/-2.7dB	<-40dBm
LTE-FDD B66	23dBm +/-2.7dB	<-40dBm
LTE-TDD B34	23dBm +/-2.7dB	<-40dBm
LTE-TDD B38	23dBm +/-2.7dB	<-40dBm
LTE-TDD B39	23dBm +/-2.7dB	<-40dBm
LTE-TDD B40	23dBm +/-2.7dB	<-40dBm
LTE-TDD B41	23dBm +/-2.7dB	<-40dBm

Table 39: E-UTRA operating bands

E-UTRA	UL Freq.	DL Freq.	Duplex Mode
1	1920~1980 MHz	2110~2170 MHz	FDD
2	1850~1910MHz	1930~1990MHz	FDD
3	1710~1785 MHz	1805~1880 MHz	FDD
4	1710~1755MHz	2110~2155MHZ	FDD
5	824 ~ 849 MHz	869 ~ 894MHz	FDD
7	2500~2570MHz	2620~2690MHz	FDD
8	880~915 MHz	925~960 MHz	FDD
12	699~716MHz	729~746MHz	FDD
13	777~787MHz	746~756MHz	FDD
18	815~830MHz	860~875MHz	FDD
19	830~845MHz	875~890MHz	FDD
20	832~862MHz	791~821MHz	FDD
25	1850~1915MHz	1930~1995MHz	FDD
26	814~849MHz	859~894MHz	FDD
28	703~748MHz	758~803MHz	FDD
66	1710~1780MHz	2110~2200MHz	FDD
34	2010~2025MHz	2010~2025MHz	TDD
38	2570~2620 MHz	2570~2620 MHz	TDD
39	1880~1920 MHz	1880~1920 MHz	TDD
40	2300~2400 MHz	2300~2400 MHz	TDD
41	2535~2655 MHz	2535~2655 MHz	TDD

Table 40: Conducted receive sensitivity

Frequency	Receive sensitivity(Typical)	Receive sensitivity
LTE FDD/TDD	Refer to the table 41	3GPP

Table 41: Reference sensitivity (QPSK)

E-UTRA Band	3GPP TS36.521-1						Actual	Duplex Mode
	1.4 MHz	3MHz	5MHz	10MHz	15 MHz	20 MHz	10 MHz	
1	-	-	-100	-97	-95.2	-94	-98.5	FDD
2	-102.7	-99.7	-98	-95	-93.2	-92	-96.5	FDD
3	-101.7	-98.7	-97	-94	-92.2	-91	-98.5	FDD
4	-104.7	-101.7	-100	-97	-95.2	-94	-97.5	FDD
5	-103.2	-100.2	-98	-95	-	-	-99.5	FDD

7	-	-	-98	-95	-93.2	-92	-100	FDD
8	-102.2	-99.2	-97	-94	-	-	-99.5	FDD
12	-101.7	-98.7	-97	-94	-	-	-98	FDD
13	-	-	-97	-94	-	-	-97.5	FDD
18	-	-	-99.3	-96.3	-94.5	-	-99.5	FDD
19	-	-	-99.3	-96.3	-94.5	-	-99.5	FDD
20	-	-	-97	-94	-91.2	-90	-98	FDD
25	-101.2	-98.2	-96.5	-93.5	-91.7	-90.5	-95.5	FDD
26	-102.7	-99.7	-97.5	-94.5	-92.7	-	-99.5	FDD
28	-	-100.2	-98.5	-95.5	-93.7	-91	-99	FDD
66	-104.2	-101.2	-99.5	-96.5	-94.7	-93.5	-97	FDD
34	-	-	-100	-97	-95.2	-	-99.5	TDD
38	-	-	-100	-97	-95.2	-94	-101	TDD
39	-	-	-100	-97	-95.2	-94	-99.5	TDD
40	-	-	-100	-97	-95.2	-94	-100	TDD
41	-	-	-98	-95	-93.2	-92	-101	TDD

4.2. LTE Antenna Requirements

For better overall performance, it is recommended that the antenna design should refer to the index requirements in the following table.

Table 42: LTE antenna requirements

Passive	Recommended standard
Operating band	Please refer to the table 2
Direction	Omnidirectional
Gain	> -3dBi (Avg)
Input impedance	50 ohm
Efficiency	> 50 %
Maximum input power	50W
VSWR	< 2
Isolation	>20dB
PCB insertion loss(<1GHz)	<0.5dB
PCB insertion loss(1GHz~2.2GHz)	<1dB
PCB insertion loss(2.3GHz~2.7GHz)	<1.5dB

4.3. GNSS Specifications

Table 43: GNSS operating bands

Type	Frequency
GPS L1	1575.42±1.023MHz
GLONASS G1	1601.7±6.75MHz
BeiDou B1I	1561.098±2.046MHz
GALILEO E1	1575.42±1.023MHz

Table 44: GNSS performance

GNSS	Description	Performance			
		Min	Type	Max	Unit
Horizontal Position Accuracy	Automatic position		0.98		m
Velocity Accuracy	Without Aid		0.1		m/s
	DFPS		0.05		m/s
Timing Accuracy			10		ns
Dynamic Performance	Maximum Altitude			18000	m
	Maximum Velocity			500	m/s
	Maximum Acceleration			4	G
TTFF (A-GPS off) GPS(L1)+GLONASS+BEIDOU	Hot start		0.62		s
	Warm start		19.03		s
	Cold start		19.95		s
TTFF (A-GPS off) Weak signal cold start GPS(L1)+GLONASS+BEIDOU	GSS7000=-130dB		14.84		s
	GSS7000=-142dB		73.33		s
	GSS7000=-146dB		164.76		s
	GSS7000=-147dB		312.85		s
TTFF (A-GPS on) Cold start (EPO in flash mode)	GPS		0.24		s
	GPS+BD		0.50		s
	GPS+GLONASS		0.32		s
	GPS+GLONASS+BD		0.29		s
Sensitivity GPS (L1)	Autonomous acquisition (cold start)		-148		dBm
	Re-acquisition		-157.5		dBm
	Tracking		-166		dBm
Sensitivity GPS(L1)+GLONASS	Autonomous acquisition (cold start)		-148		dBm