MeiG SLM828G Module Hardware Design Manual

Controlled Version Number: V1.3

Release Date: 2022/09/07

MeiG Smart Technology Co.,Ltd
A Global Leading IoT Terminals and Wireless Data Solutions Provider
Add：32/F,Building B,Shenzhen International Innovation Center, No.1006 Shennan Avenue,Futian District,Shenzhen,China
Tel：+86-755-83218588 Fax：+86-755-83219788
E-mail：ir@meigsmart.com Web：www.meigsmart.com

Important Notice

Copyright Notice

Statement of No Guarantee

MeiG Smart Technology Co., Ltd makes no representations or guarantees, either express or implied, for any contents in this document, and assumes no responsibility for the merchantability and fitness for a particular purpose or any indirect, extraordinary or consequential losses.

Confidentiality Claim

The information contained in this document (including any annexes) is confidential. The recipient understands that the document obtained by him is confidential and shall not be used for any purpose other than the stated purpose, and he shall not disclose this document to any third party.

Disclaimer

The company assumes no responsibility for property damage or personal injury caused by customers' improper operation. Customers are requested to develop corresponding products according to the technical specifications and reference designs in the manual. Before the disclaimer, the company has the right to change the contents of this manual according to the needs of technological development, and the version is subject to change without further notice.

Revision History

Version No.	Date	Reason for Revision
V1.0	2022-02-10	First Edition
V1.1	2022-03-25	1. Modify chapter 2.2 power consumption content 2. Add chapter 3 note part 3. Add chapter 5 antenna index
V1.2	2022-05-10	1. Modify chapter 2.2 power consumption content 2. Modify chapter 4.2 GNSS antenna interface content 3. Modify chapter 5.1 antenna interface content 4. Modify chapter 5.2 RF output power, receiving sensitivity, working frequency and antenna index 5. Modify chapter 6.4 module power consumption range
V1.3	2022-09-07	1. Modify chapter 2.1 frequency band information 2. Modify chapter 2.2 USB interface driver information 3. Modify chapter 3.3 USB_SS_RX_P,USB_SS_RX_M PIN, USIM1_DET ,USIM2_DET, I2C_SDA, I2C_SCLIO, DC, SD_CMD, SD_CLK, SD_DET IO information 4. Modify chapter 3.6.2 power on/off note information 5. Modify chapter 3.8.1 USIM/SIM interface description 6. Modify chapter 3.9.1 USB_SS_RX_P,USB_SS_RX_M PIN 7. Modify chapter 3.9.3 USB driver description 8. Modify chapter 3.10 IIC description 9. Modify chapter 3.11 network instructions reference design diagram 10. Modify chapter 3.14 SD_CMD, SD_CLK, SD_DET IO status 11. Modify chapter 4.2 antenna access method 12. Modify chapter 4.3 GNSS performance 13. Modify chapter 5.2.2 table 32 frequency band information 14. Modify chapter 5.2.3 table 34 frequency band information 15. Modify chapter 5.2.5 frequency band information 16. Modify chapter 6.5 environmental reliability requirements 17. Modify chapter 8.3 package method

Contents

Table Index

Figure Index

1 Introduction

This document defines the SLM828G module and its air interface and hardware interface for connecting to customer applications.

This document helps customers quickly understand SLM828G module interface specifications, electrical characteristics, mechanical specifications, and related product information. With the help of this document, combined with our application manual and user instructions, customers can quickly apply the SLM828G module to wireless applications.

SLM828G wireless module is a broadband wireless terminal product suitable for TDD-LTE/FDD-LTE/WCDMA network systems.

The SLM828G supports the following access rates:

- TDD-LTE single band supports downlink 256QAM rate up to: DL430Mbps/UL90Mbps
- FDD-LTE single band supports downlink 256QAM rate up to: DL600Mbps/UL150Mbps
- WCDMA rate up to DC HSPA+: 42Mbps/5.76Mbps;
- Support downlink 3CA MIMO 4X4 combination, and the downlink rate can reach CAT12

SLM828G module can provide voice, short message, address book, GPS/Beidou and other functions while providing high-speed broadband data access. SLM828G module can be widely used in mobile broadband access, video surveillance, security, on-board equipment and other products.

1.1 Safety Instructions

By complying with the following safety principles, you can ensure personal safety and protect the products and working environment from potential damage:

	Driving safety first! When you drive, do not use handheld mobile terminal device unless it has a hands-free function. Please stop the car before calling!
	Please turn off the mobile terminal device before boarding. The wireless function of mobile terminal shall not be turned on in the aircraft to prevent interference with the aircraft communication system. Ignoring this reminder may affect flying safety or even violate the law.
	In hospitals or health care facilities, pay attention to whether there are restrictions on the use of mobile terminal device. RF interference will cause medical equipment to be abnormal, so mobile terminal device may need to be turned off.
	Mobile terminal device cannot always be effectively connected, for example, if the mobile device has no expense or the SIM is invalid. When you encounter the above situations in an emergency, please make an emergency call, meanwhile, ensure that your device is turned on and in an area with sufficient signal strength.
	Your mobile terminal device will receive and transmit radio frequency signals when it is turned on. There will be radio frequency interference when it is close to TV, radio, computer or other electronic equipment.
	Please keep mobile device away from inflammable gases. Please turn off the mobile terminal device when you are near a fueling station, oil depot, chemical plant or explosion site. There will be potential safety hazards when operating electronic equipment in any place with potential explosion hazard.

1.2 Purpose of the Document

This document describes the basic functions, main features, hardware interface and usage, structural characteristics, power consumption indicators and electrical characteristics of SLM828G wireless module, and guides users to embed the SLM828G module in the design of various application terminals.

1.3 List of Contents

This document is divided into the following parts:

- Chapter 1, mainly introduces the safety instructions and purpose of the document;
- Chapter 2, introduces the basic functions and main features of the SLM828G wireless module;
- Chapter 3, introduces the functions, characteristics and usage methods of each hardware interface of SLM828G module;
- Chapter 4, introduces GNSS related features;
- Chapter 5, introduces the relevant content and precautions of the antenna interface;
- Chapter 6, introduces the electrical characteristics of SLM828G module;
- Chapter 7, introduces the features and precautions structure of the SLM828G module;
- Chapter 8, introduces the precautions of the SLM828G module in storage and production;
- Chapter 9, appendix A, reference documents and term abbreviations;
- Chapter 10, appendix B GPRS coding schemes.

2 Product Overview

2.1 Basic Description

SLM828G is a series of TDD-LTE/FDD-LTE/WCDMA wireless communication modules with diversity receiving function. It supports TDD-LTE, FDD-LTE, and is compatible with WCDMA DC-HSPA+ network data connection, which can provide voice (PCM), SMS, address book, and other functions for customers.

The following table lists the frequency bands supported by SLM828G:

Table 1 Frequency Band Supported by SLM828G Module

Network	SLM828G-EU	SLM828G-LA
FDD-LTE	B1/B3/B5/B7/B8/B20/B28/B32	B2/B4(66)/B5/B7/B8/B20/B28
TDD-LTE	B38/B39/B40/B41/B42/B43	B38/B39/B40/B41/B42/B43/B48
WCDMA	B1/B3/B5	B2/B4/B5
GNSS L1	GPS, Glonass, Galileo, BeiDou	GPS, Glonass, Galileo, BeiDou
DL 2CA	B1+B1/B3/B5/B7/B8/B20/B28/B32/B38/B40/B41/B42; B3+B3/B5/B7/B8/B20/B28/B32/B38/B40/B41/B42; B5+B5/B7/B38/B40/B41/B42; B7+B7/B8/B20/B28/B32; B8+B32/B38/B39/B40/B41/B42; B20+B32/B38/B40/B42; B28+B32/B38/B40/B41/B42; B38+B38; B39+B39/B41; B40+B40/B42; B41+B41/B42; B42+B42.	B2+B2/B4/B5/B7/B28/B66; B4+B4/B5/B7/B28; B5+B5/B7/B38/B40/41/48/66; B7+B7/B8/B20/B28/B42/B66; B8+B38/B39/B40/B41/B42; B20+B38/B40/B42; B28A+B38/B40/B41/B42; B38+B38; B39+B39/B41; B40+B40/B42; B41+B41/B42; B42+B42; B66+B66.
DL 3CA	B3+B5+B7/38/40; B3+B7+B7/B8/B20/B28/B32/B42; B3+B8+B38/B40; B3+B20+B32/B38/B42; B3+B28+B38/B40/B41/B42; B3+B40+B40; B3+B41+B41/B42; B5+B7+B7; B5+B40+B40; B7+B7+B8/B20/B28; B7+B20+B32+B42; B8+B39+B39; B8+B40+B40; B8+B41+B41; B8+B42+B42;	B2+B2+B4/B5/B66; B2+B4+B4/B5/B7/28; B2+B5+B5/B48/B66; B2+B7+B7/B66; B2+B66+B66; B4+B4+B5/B7; B4+B5+B5; B4+B7+B7; B5+B5+B66; B5+B7+B7; B5+B40+B40; B5+B48+B48; B5+B66+B66; B8+B39+B39; B8+B40+B40;

	B20+B38+B38; B20+B40+B40; B28+B40+B40; B28+B41+B41/B42; B39+B41+B41; B40+B40+B40/B42; B41+B41+B41; B42+B42+B42.	B8+B41+B41; B8+B42+B42; B20+B38+B38; B20+B40+B40; B28+B40+B40; B28+B41+B41/42; B28+B42+B42; B39+B39+B41; B39+B41+B41; B40+B40+B40/B42; B40+B42+B42; B41+B41+B41/B42; B41+B42+B42; B42+B42+B42; B66+B66+B66.
UL 2CA	3C/5B/7C/38C/40C/41C/42C	2C/7C/38C/40C/41C/42C
MIMO	4*4 MIMO: FDD：B1/B3/B7/ TDD：B38/39/B40/B41/B42/B43：	4*4 MIMO: FDD:2/4/7/66 TDD:38/40/41/42/43

The SLM828G module adopts an advanced highly integrated design scheme, which integrates radio frequency and baseband on a PCB to complete wireless reception, transmission, baseband signal processing, and audio signal processing functions. It adopts a single-sided layout. The module structure size is 37*39.5*2.8mm. It can meet almost all application requirements, such as mobile broadband access, video surveillance, handheld terminals, in-vehicle devices, ultrabooks, etc

2.2 Key Features

The following table describes the features of the SLM828G module in detail.

Table 2 SLM828G Key Features List

Parameter	Description
Power Supply	● VPH_PWR supply voltage range: 3.3V~4.2V ● Typical supply voltage: 3.8V
Transmit Power	● Class 3 (24dBm±2dB) for WCDMA bands ● Class 3 (23dBm±2dB) for LTE FDD bands ● Class 3 (23dBm±2dB) for LTE TDD bands
LTE features	● Support downlink 3CA and MIMO 4X4 combination, the downlink rate can reach CAT12 ● Support 1.4 ~ 20MHz RF bandwidth ● Downlink supports multi-user MIMO ● FDD: the maximum uplink rate is 150Mbps, support downlink 256QAM, the maximum downlink rate is 600Mbps ● TDD: the maximum uplink rate is 90Mbps, support downlink 256QAM, the maximum downlink rate is 430Mbps
WCDMA features	● Support 3GPP R8 DC-HSPA+ ● Support 16-QAM，64-QAM and QPSK modulation ● 3GPP R6 CAT6 HSUPA: The maximum uplink rate is 5.76Mbps ● 3GPP R8 CAT24 DC-HSPA+: The maximum downlink rate is 42Mbps
Network protocol features	● Support TCP/UDP/PPP/FTP/HTTP/SMTP/MMS/NTP/PING /QMI protocol ● Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol)
Short message service (SMS)	● Text and PDU mode ● Point-to-point MO and MT ● Short message cell broadcast ● Short message storage: stored in the module by default
USIM card interface	● Support USIM/SIM card: 1.8V and 3.0V
Audio features	● Support 1 digital audio interface: PCM interface ● WCDMA: AMR/AMR-WB ● LTE: AMR/AMR-WB ● Support echo cancellation and noise suppression
PCM interface	● For audio use, an external Codec chip is required ● Support 8-bit A-law, u-law and 16-bit linear coding formats ● Support long frame mode and short frame mode ● Support master and slave modes, but it can only be used as master mode in long frame mode
USB interface	● Compatible with USB3.0&2.0 (slave mode only), data transfer rate up

	to 5.0Gbps/480Mbps ● Used for AT command, data transmission, GNSS NMEA output, software debugging and software upgrade ● USB drive: Supports Windows7, Windows 8/8.1, Windows10, Windows11, Linux 2.6 or later, and Android 2.3/4.0/4.4/5.0 or later
Serial port	● Main serial: Used for AT instruction communication and data transmission The maximum baud rate is 921600bps. The default baud rate is 115,200 BPS Support RTS and CTS hardware flow control ● Debug serial port: For Linux control, log output Baud rate is 115,200 bps ● Bluetooth UART interface: For Bluetooth communication, reusable into SPI interface * Baud rate is 115,200 bps
PCIe ×1 Interface*	● PCI Express Specification Revision 2.1 and support 5Gbps per channel ● Used for data transmission
RX- diversity	● Support LTE/WCDMA RX-diversity
GNSS Features	● Qualcomm Gen9HT - Lite ● Protocol: NMEA 0183
AT command	● Compliant with 3GPP TS 27.007, 27.005, newly add MeiG AT command
Network indication	● NET_MODE &NET_STATUS indicates the network connection status ● STATUS Indicates the system status
Antenna interface	● Main antenna（ ANT_MAIN） ● RX-diversity antenna（ANT_DIV） ● GNSS antenna（ANT_GNSS） ● MIMO antenna（ANT_MIMO1 和 ANT_MIMO2）
Physical properties	● Size: 37*39.5*2.8mm ● Weight: <11g
Temperature range	● Normal working temperature: -30℃～+75℃ ● Restricted working temperature: -40℃～+85℃ ● Storage temperature: -45℃～+90℃
Software upgrade	● USB interface & Support FOTA and DFOTA*
RoHS	● All parts are fully compliant with EU RoHS standard
Environment humidity	● 5%~95%
ESD	● VPH_PWR, GND: air discharge ±10KV, contact discharge ±5KV ● Antenna interface: air discharge ±8KV, contact discharge ±4KV ● Other interfaces: air discharge ±1KV, contact discharge ±0.5KV
Power Consumption	● Sleep mode: < 5mA ● Data mode: < 800mA (LTE maximum power)

Interface	● 299Pin LGA interface
External interface	● Power interface ● USB 2.0&USB3.0 interface ● USIM1/USIM2 interface (support 3.0V, 1.8V） ● PCM interface ● I2C interface ● Hardware reset interface ● Net Status ● GPIOs ● PCIE ● UART ● SDIO* ● W_Disable ● WAKEup ● RF MAIN/DIV/GNSS

2.3 Functional Block Diagram

The following is a block diagram of SLM828G, which elaborates its main functional parts.

- Power management
- Baseband chip
- LPDDR2 SDRAM+NAND Flash
- RF part
- Peripheral interface

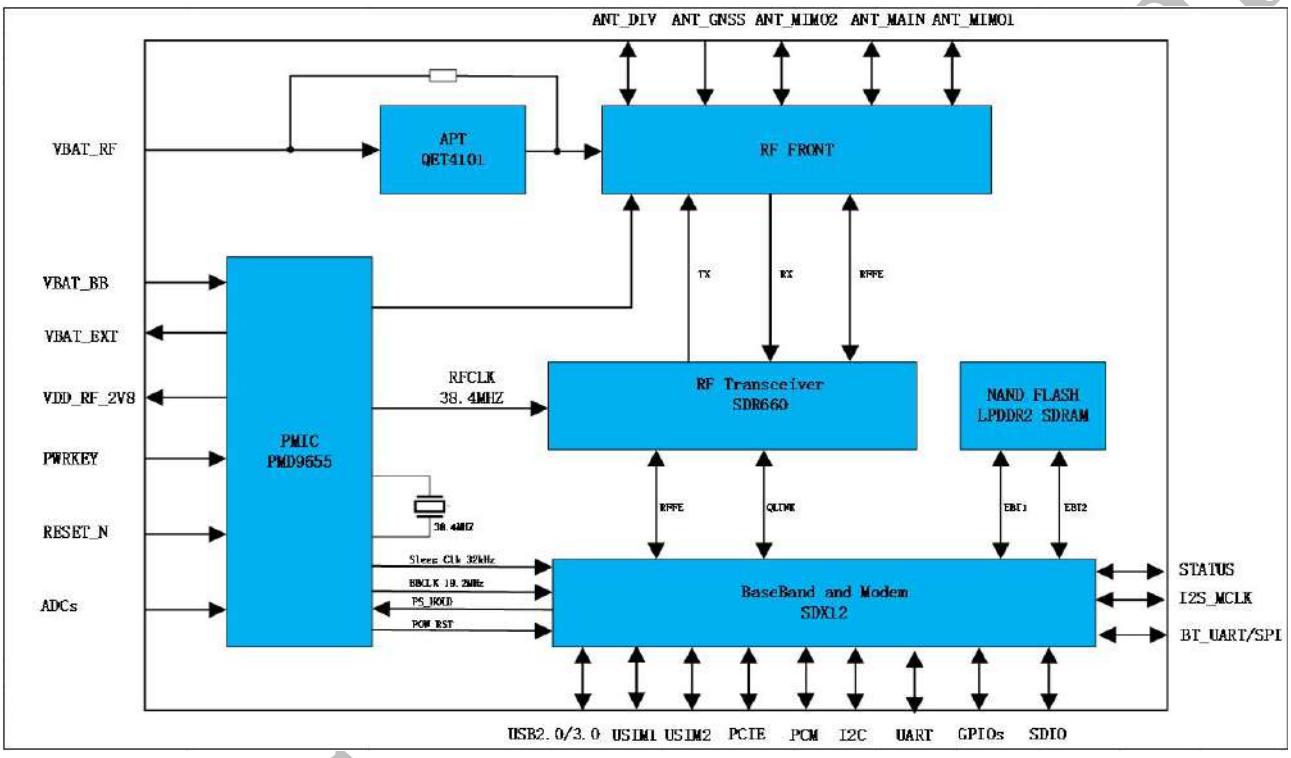

Figure 1 Functional Block Diagram

2.4 Evaluation Board

To help test and use SLM828G module, MeiG Smart Technology Co., Ltd provides a set of evaluation board. Evaluation board tools include antenna and other peripherals.

For details on how to use the evaluation board, please refer to the *SLM828G_EVB_User Manual*.

3 Application Interfaces

3.1 Basic Description

SSLM828G module adopts 299PIN LGA interface and provides the following functional interfaces:

- Power interface
- USB 2.0&USB3.0 interface
- USIM/SIM card interface (Support 3.0V, 1.8V)
- PCM interface
- I2C interface
- Hardware reset interface
- Net Status
- GPIOs
- PCIE
- UART
- SDIO*
- W_Disable
- WAKEup
- RF MAIN/DIV/GNSS
- SPI
- ADC
- USB_BOOT interface

Note:

1. " * " are in development.
2. BT UART interface can also be reused as SPI interface

3.2 LGA interface distribution

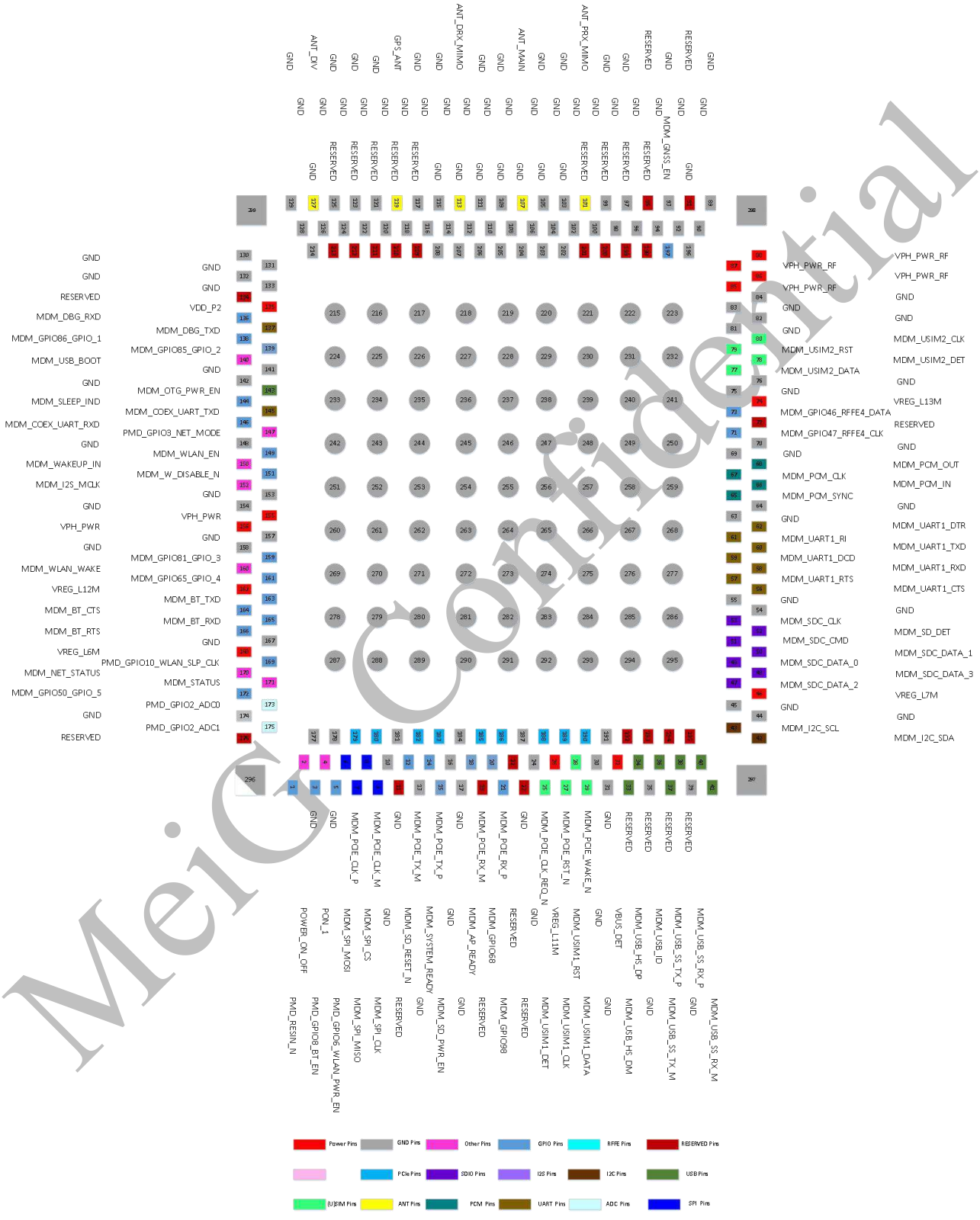

Figure 2 Module pin Number (perspective)

Note:

1. Keep all RESERVED pins and unused pins unconnected.
2. GND pins 215~299 should be connected to the ground in the design.

3.3 Pin Description

The following table describes each pin definition of the SLM828G module.

Table 3 IO Parameter definition

IO Type	Description
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain
IO	Input/Output

Table 4 Pin Description

Power					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Characteristic**	**Remark**
VBAT_BB	155,156	PI	Baseband power input	Vmax=4.2V Vmin=3.3V Vnorm=3.8V	The power supply must be able to provide more than 2A current
VBAT_RF	85,86,87, 88	PI	RF power input	Vmax=4.2V Vmin=3.3V Vnorm=3.8V	The power supply must be able to provide more than 2A current
VDD_EXT_1V8	168	PO	Module output power supply	Vnorm=1.8V IOmax=50mA	1.8V power output after power on
VDD_RF_2V8	162	PO	Module output power supply	Vnorm=2.85V IOmax=120mA	2.8V power output after power on

VDD_P2	135	PI	SD card power	-	If using SD card, connect VDD_P2 to SD_VIO*, if using eMMC* or not using SDIO interface, connect VDD_P2 to VDD_EXT _1V8
Reset					
Pin Name	**Pin Name**	**Pin Name**	**Pin Name**	**Pin Name**	**Pin Name**
RESET_N	1	DI	Reset module	VIHmax=2.1V VIHmin=1.3V VILmax=0.5V	1.8V power domain, internal pull-up, active low
PWRKEY	2	DI	Module switch signal	VIHmax=2.1V VIHmin=1.3V VILmax=0.5V	1.8V power domain, internal pull-up, active low
USB_BOOT	140	DI	USB download mode control signal, high efficiency	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	Enters to the 1.8 V on the USB before starting the loading mode, suggest reserve test points
PON_1	4	DI	Module power on control signal, active at high level	-	Reserved, can change the power on mode in the external
Module Status Indication					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Characteristic**	**Remark**
NET_MODE	147	DO	Registered network type indicator	VOHmin=1.35V VOLmax=0.45V	1.8V power domain, disconnect when not in use.
NET_STATUS	170	DO	Network connection status indicator (default)	VOHmin=1.35V VOLmax=0.45V	1.8V power domain, disconnect when not in use.
STATUS	171	DO	Indicates system operating status	VOHmin=1.35V VOLmax=0.45V	1.8V power domain, disconnect when not in use.
USB Interface					
Pin Name	**Pin Name**	**Pin Name**	**Pin Name**	**Pin Name**	**Pin Name**
USB_DP	34	IO	USB 2.0 Differential	Compliant with USB2.0	Requires 90Ω differential impedance

			Data Signal (+)	specification	
USB_DM	33	IO	USB 2.0 Differential Data Signal (-)	Compliant with USB2.0 specification	Requires 90Ω differential impedance
USB_SS_TX_M	37	AO	USB 3.0 Differential Sending Signal (-)	Compliant with USB3.0 specification	Requires 90Ω differential impedance
USB_SS_TX_P	38	AO	USB 3.0 Differential Sending Signal (+)	Compliant with USB3.0 specification	Requires 90Ω differential impedance
USB_SS_RX_P	40	AI	USB 3.0 Differential Reception Signal (+)	Compliant with USB3.0 specification	Requires 90Ω differential impedance
USB_SS_RX_M	41	AI	USB 3.0 Differential Reception Signal (-)	Compliant with USB3.0 specification	Requires 90Ω differential impedance
USB_VBUS	32	PI	USB detection	Vmax=5.25V Vmin=3.3V	Used to test whether the USB reign
USB_ID*	36	DI	OTG Identification signal	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V power domain, disconnect when not in use; Reserved
OTG_PWR_EN*	143	DO	OTG pwr enable	VOLmax=0.45V VOHmin=1.35V	Reserved
USIM Card Interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Characteristic**	**Remark**
USIM1_DET	25	DI	(U)SIM1 card hot plug detection	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	External pull up to 1.8V, support hot plug.
USIM1_VDD	26	PO	(U)SIM1 power supply voltage	IOmax=50mA 1.8V (U)SIM: Vmax=1.9V Vmin=1.7V 3.0V (U)SIM: Vmax=3.05V Vmin=2.75V	Automatic identification of module 1.8 V or 3.0 V USIM card
USIM1_CLK	27	DO	(U)SIM1 card clock line	1.8V (U)SIM: VOLmax=0.4V VOHmin=1.45V 3.0V (U)SIM:	-

				VOLmax=0.4V VOHmin=2.3V	
USIM1_RST	28	DO	(U)SIM1 card reset line	1.8V (U)SIM: VOLmax=0.4V VOHmin=1.45V 3.0V (U)SIM: VOLmax=0.4V VOHmin=2.3V	-
USIM1_DATA	29	IO	(U)SIM1 card data cable	1.8V (U)SIM: VILmax=0.36V VIHmin=1.26V VOLmax=0.4V VOHmin=1.45V 3.0V (U)SIM: VILmax=0.57V VIHmin=2V VOLmax=0.4V VOHmin=2.3V	Need to pull up to USIM1_VDD with a pull-up resistance of 10K
USIM2_VDD	74	PO	(U)SIM2 power supply voltage	IOmax=50mA 1.8V (U)SIM: Vmax=1.9V Vmin=1.7V 3.0V (U)SIM: Vmax=3.05V Vmin=2.75V	Automatic identification of module 1.8 V or 3.0 V USIM card. Disconnect if not used.
USIM2_DATA	77	IO	(U)SIM2 card data cable	1.8V (U)SIM: VILmax=0.36V VIHmin=1.26V VOLmax=0.4V VOHmin=1.45V 3.0V (U)SIM: VILmax=0.57V VIHmin=2V VOLmax=0.4V VOHmin=2.3V	Need to pull up to USIM2_VDD with a pull-up resistance of 10K. Disconnect if not used.
USIM2_DET	78	DI	(U)SIM2 card hot plug detection	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	External pull up to 1.8V, disconnect if not used. Support hot plug.
USIM2_RST	79	DO	(U)SIM2 card reset line	1.8V (U)SIM: VOLmax=0.4V VOHmin=1.45V For 3.0V (U)SIM: VOLmax=0.4V VOHmin=2.3V	Disconnect if not used.
USIM2_CLK	80	DO	(U)SIM2 card clock line	1.8V (U)SIM: VOLmax=0.4V VOHmin=1.45V	Disconnect if not used.

				3.0V (U)SIM: VOLmax=0.4V VOHmin=2.3V	
ANT Tuner Control Interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Characteristic**	**Remark**
ANT_MIMO1	101	DO	MIMO1 antenna	-	50 Ω characteristic impedance, disconnect when not in use
ANT_MAIN	107	IO	Main antenna	-	50 Ω characteristic impedance,
ANT_MIMO2	113	DO	MIMO2 antenna	-	50 Ω characteristic impedance, disconnect when not in use
ANT_GNSS	119	DO	GNSS antenna	-	550 Ω characteristic impedance, disconnect when not in use
ANT_DIV	127	DO	Diversity antenna	-	50 Ω characteristic impedance, disconnect when not in use
I2C Interfacce					
Pin Name	**Pin Name**	**Pin Name**	**Pin Name**	**Pin Name**	**Pin Name**
I2C_SDA	42	OD	I2C data	-	Module internal pull up 1.8 V, disconnected if not used.
I2C_SCL	43	OD	I2C clock	-	Module internal pull up 1.8 V, disconnected if not used.
I2S_MCLK	152	DO	Output clock signal	-	Can be used as external CODEC input clock signal, disconnected if not used.
PCM Interface					
Pin Name	**Pin Name**	**Pin Name**	**Pin Name**	**Pin Name**	**Pin Name**
PCIE_CLK_P	179	AI,AO	RC mode: PCIe differential clock + output (default) EP mode: PCIe differential clock + input	Complies with PCIe Gen2.0 protocol standards	Difference 100 Ω impedance control

PCIE_CLK_M	180	AI,AO	RC mode: PCIe Differential clock - output (default) EP mode: PCIe differential clock - input	-	Difference 100 Ω impedance control
PCIE_TX_M	182	AO	PCIE_ Data transmission signal -	-	Difference 100 Ω impedance control
PCIE_TX_P	183	AO	PCIE_Data transmission signa +	-	Difference 100 Ω impedance control
PCIE_RX_M	185	AI	PCIE_ Data receiving signal -	-	Difference 100 Ω impedance control
PCIE_RX_P	186	AI	PCIE_ Data receiving signal +	-	Difference 100 Ω impedance control
PCIE_CLKREQ	188	IO	PCIeClock request	VOLmax=0.45V VOHmin=1.35V VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	External pull-up 100 k Ω resistance RC mode: Request input (default) EP mode: request output, disconnect when not in use.
PCIE_HOST_RST_N	189	IO	PCIe reset	VOLmax=0.45V VOHmin=1.35V VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	RC mode: PCIe resets output
PCIE_WAKE	190	IO	PCIe wake up	VOLmax=0.45V VOHmin=1.35V VILmin=-0.3V VILmax=0.6V	External pull-up 100 k Ω resistance RC mode: PCIe wake up input (default) EP mode: PCIe wake up output
PCM Interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Characteristic**	**Remark**
PCM_SYNC	65	IO	PCM data synchronization signal	VOLmax=0.45V VOHmin=1.35V VILmin=-0.3V VILmax=0.6V	1.8V power domain, module as the master device, the pin output signal, module as the

				VIHmin=1.2V VIHmax=2.0V	slave device, the pin input signal.disconnect when not in use.
PCM_IN	66	DI	PCM data input	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V power domain, disconnect when not in use.
PCM_CLK	67	IO	PCM clock	VOLmax=0.45V VOHmin=1.35V VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V power domain, module as the master device, the pin output signal, module as the slave device, the pin input signal.disconnect when not in use.
PCM_OUT	68	DO	PCM data output	VOLmax=0.45V VOHmin=1.35V	1.8V power domain, disconnect when not in use.
SPI interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Characteristic**	**Remark**
SPI_MOSI	6	DO	SPI data input and output signals	VOLmax=0.45V VOHmin=1.35V	1.8V power domain, disconnect when not in use.
SPI_MISO	7	DI	SPI data input and output signals	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V power domain, disconnect when not in use.
SPI_CS	8	DO	SPI chip selection signal	VOLmax=0.45V VOHmin=1.35V	1.8V power domain, disconnect when not in use.
SPI_CLK	9	DO	SPI clock signal	VOLmax=0.45V VOHmin=1.35V	1.8V power domain, disconnect when not in use.
SDIO interface *					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Characteristic**	**Remark**
SD_VIO*	46	PO	SD card: SDIO pull-up	1.8V SD card: Vmax=1.9V Vmin=1.75V 3.0V SD card: Vmax=3.05V Vmin=2.75V IOmax=50mA	Support 1.8V&3V If using SD card, connect to VDD_P2
SD_DATA0	49	IO	SDC data bit0	1.8V SD card: VOLmax=0.45V	Disconnect when not in use.

SD_DATA1	50	IO	SDC data bit1	VOHmin=1.4V VILmin=-0.3V VILmax=0.58V VIHmin=1.3V VIHmax=2.0V 3.0V SD card: VOLmax=0.35V VOHmin=2.15V VILmin=-0.3V VILmax=0.7V VIHmin=1.8V VIHmax=3.15V VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V VOLmax=0.45V VOHmin=1.35V VOLmax=0.45V VOHmin=1.35V	Disconnect when not in use.
SD_DATA2	47	IO	SDC data bit2		Disconnect when not in use.
SD_DATA3	48	IO	SDC data bit3		Disconnect when not in use.
SD_CMD	51	DO	SD card command signal		Disconnect when not in use.
SD_CLK	53	DO	SD card clock signal		Disconnect when not in use.
SD_ DET	52	DI	SD card hot plug detection signal		Disconnect when not in use.
SD_RESET_N*	12	DO	Reset output signal		Connect the SD chip. Reserved
SD_PWR_EN	15	DO	External SD card power switch control signal		Reserved
ADC interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Characteristic**	**Remark**
ADC0	173	AI	Analog to digital input port 0	0-1.875V	Disconnect when not in use.
ADC1	175	AI	Analog to digital input port 1	0-1.875V	Disconnect when not in use.
RFFE interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Characteristic**	**Remark**
RFFE_CLK*	71	DO	External control RFFE interface	VOLmax=0.45V VOHmin=1.35V	Reserved
RFFE_DATA*	73	IO	External control RFFE interface	VOLmax=0.45V VOHmin=1.35V VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	Reserved
Sleep wake up pin					

Pin Name	Pin Number	I/O	Description	DC Characteristic	Remark
W_DISABLE_N	151	DI	Flight mode control	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V power domain, default pull-up. Low level module into flight mode, disconnect when not in use.
SLEEP_IND	144	DO	Sleep status indicator	VOLmax=0.45V VOHmin=1.35V	1.8V power domain, disconnect when not in use.
WAKEUP_IN	150	DI	External device wakes up module	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	Default low active, software configurable, 1.8V power domain, disconnect when not in use.
SYSTEM_READY	14	IO	Module sleep status detection signal	-	Reserved
AP_READY	18	IO	Host sleep status detection signal	-	Reserved
WLAN control interface *					
WLAN_PWR_EN*	5	DO	Wlan power supply is enabled	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain, disconnect when not in use.
COEX_UART_RXD*	146	DI	LTE/WLAN shared serial port receiving signal cable	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain, disconnect when not in use.
COEX_UART_TXD*	145	DO	LTE/WLAN shared serial port sending signal cable	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain, disconnect when not in use.
WLAN_EN*	149	DO	Wake up WLAN module	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain, disconnect when not in use.
WLAN_WAKE*	160	DI	WLAN chip wakes up module signal	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	1.8V power domain, disconnect when not in use.
WLAN_SLP_CLK*	169	DO	WLAN sleep clock signal	V_{OL}max=0.45V V_{OH}min=1.35V	1.8V power domain, disconnect when not in use.
Main UART interface					

Pin Name	Pin Number	I/O	Description	DC Characteristic	Remark
CTS	56	DO	Clear to send	VOLmax=0.45V VOHmin=1.35V	1.8V power domain, disconnect when not in use.
RTS	57	DI	Request to send	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V power domain, disconnect when not in use.
UART1_RXD*	58	DI	Module receiving data	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V power domain, disconnect when not in use.
UART1_DCD*	59	DO	Output carrier detection module	VOLmax=0.45V VOHmin=1.35V	1.8V power domain, disconnect when not in use.
UART1_TXD*	60	DO	Module sending data	VOLmax=0.45V VOHmin=1.35V	1.8V power domain, disconnect when not in use.
UART1_RI	61	DO	Output module is ringing	VOLmax=0.45V VOHmin=1.35V	1.8V power domain, disconnect when not in use.
UART1_DTR*	62	DI	Ready, sleep mode control	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V power domain, disconnect when not in use.
Debug UART interface					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Characteristic**	**Remark**
DBG_TXD	137	DO	DEBUG serial port sending	VOLmax=0.45V VOHmin=1.35V	1.8V power domain, disconnect when not in use.
DBG_RXD	136	DI	DEBUG serial port receiving	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V power domain, disconnect when not in use.
Bluetooth UART interface *					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Characteristic**	**Remark**
BT_EN*	3	DO	BT function enable pin	VOLmax=0.45V VOHmin=1.35V	1.8V power domain, disconnect when not in use.
UART2_TXD*	163	DO	Bluetooth serial port sends data signals	VOLmax=0.45V VOHmin=1.35V	1.8V power domain, disconnect when not in use.

BT_CTS	164	DO	Bluetooth serial port clear sends data signal	VOLmax=0.45V VOHmin=1.35V	1.8V power domain, disconnect when not in use.
UART2_RXD*	165	DI	Bluetooth serial port receives data signals	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V power domain, disconnect when not in use.
BT_RTS	166	DI	Bluetooth serial port request data signal	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	1.8V power domain, disconnect when not in use.
General GPIO*					
Pin Name	**Pin Number**	**I/O**	**Description**	**DC Characteristic**	**Remark**
GPIO_1	138	IO	General GPIO	VOLmax=0.45V VOHmin=1.35V VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	Disconnect when not in use.
GPIO_2	139	IO	Genera GPIO		Disconnect when not in use.
GPIO_3	159	IO	Genera GPIO		Disconnect when not in use.
GPIO_4	161	IO	Genera GPIO		Disconnect when not in use.
GPIO_5	172	IO	Genera GPIO		Disconnect when not in use.
RESERVED					
Pin Number : 11 19~23 72 91 95 192~195 197~201 209~213 134 176					
GND					
Pin Number : 10 13 16 17 24 30 31 35 39 44 45 54 55 63 64 69 70 75 76 81~84 89 90 92~94 96~100 102~106 108~112 114~118 120~126 128~133 141 142 148 153 154 157 158 167 174 177 178 181 184 187 191 196 202~208 214~299					

Note:

1. " * " are in development.

3.4 Module Working Mode

Table 5 List of Working Modes

Mode	Description

WCDMA	WCDMA IDLE	The module system is in an idle state and has registered to the WCDMA network, and the module is now ready for sending and receiving services.
	WCDMA TALK	In the module WCDMA voice service, the power consumption of the module depends on the network settings.
	WCDMA DATA	In WCDMA data transmission, the power consumption of the module depends on the network settings (such as the power control level), the data uplink and downlink rate, and the related settings of WCDMA.
HSPA	HSPA IDLE	The module is ready for HSPA data transmission. However, no data is sent or received at this time. The power consumption of the module depends on the network settings.
	HSPA DATA	In HSPA data transmission, the power consumption of the module depends on the network settings (such as the power control level), the data uplink and downlink rate, and the related settings of HSPA.
TD-LTE	TD-LTE IDLE	The module is ready for TD-LTE data transmission. However, no data is sent or received at this time. The power consumption of the module depends on the network settings.
	TD-LTE DATA	In TD-LTE data transmission, the power consumption of the module depends on the network settings (such as the power control level), the data uplink and downlink rate, and the related settings of TD-LTE.
FDD-LTE	FDD-LTE IDLE	The module is ready for FDD-LTE data transmission. However, no data is sent or received at this time. The power consumption of the module depends on the network settings.
	FDD-LTE DATA	In FDD-LTE data transmission, the power consumption of the module depends on network settings (such as the power control level), the data uplink and downlink rate, and the related settings of TD-LTE.
Minimum functional mode	VBAT_BB/VBAT_RF uninterruptible power supply. Use AT+CFUN=0 to make the module enter the minimum function mode. At this time, the RF transceiver of the module is disabled. Use the AT+CFUN=1 module to re-open the transceiver registration network to the normal function mode.	
Flight mode	The W_DISABLE_N pin can set the module to flight mode. In this mode, the RF does not work.	
Sleep mode	In this mode, the power consumption of the module will be reduced to a very low level, but the module can still receive paging, SMS, phone calls and TCP/UDP data.	
Shutdown mode	Low voltage shutdown. In this mode, the PMU stops supplying power to the baseband (BB) and radio frequency (RF), the software stops working, and the serial port is blocked.	

3.5 Power Design

3.5.1 Pin Description

SLM828G has 6 VBAT pins for connecting to external power supply (recommended supply 4A), which can be divided into two power domains:

- Four VBAT_RF pins are used to power the module RF;
- Two VBAT_BB pins are used to power the baseband.

Table 6 Power Related Interface

Pin Name	Pin Number	Description	Min. Value	Typical Value	Max. Value	Unit
VBAT_BB	155,156	Module baseband power input	3.3	3.8	4.2	V
VBAT_RF	85,86,87,88	Module RF power input	3.3	3.8	4.2	V

3.5.2 Reduce Voltage Drop

The power supply range of SLM828G is 3.3V~4.2V. During data transmission or talking, the instant high power transmission will form current peak, resulting in large ripple. If the instantaneous voltage drop causes the power supply voltage to be too low, the module will shut down. To ensure the normal operation of the module, ensure that the power supply is sufficient and the input voltage is not lower than 3.3V. The figure below is the voltage drop situation during burst transmission in 3G, 4G and 5G networks.

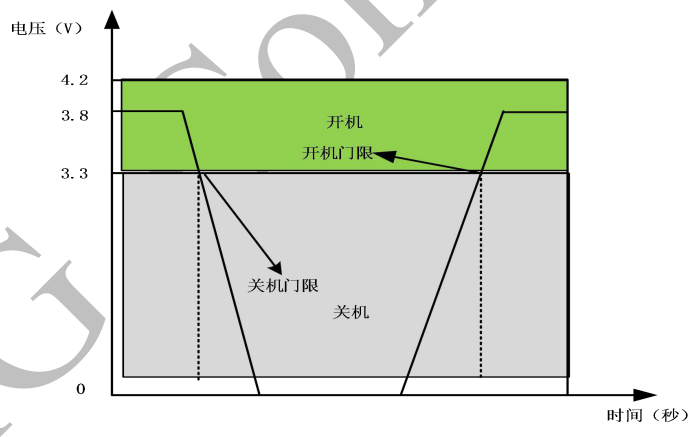

Figure 3 Switching machine threshold

The figure below shows the voltage drop when registered for burst transmission under the network.

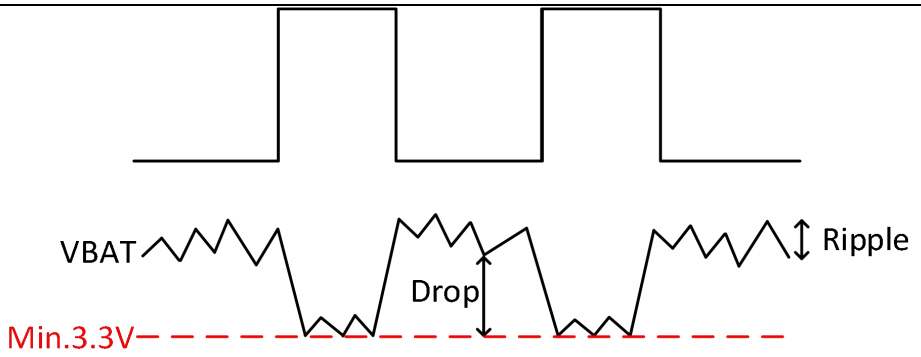

Figure 4 Burst transmission power requirements

To reduce voltage drop, require 100uF filter capacitor with a low ESR. Chip multilayer ceramic capacitors (MLCC) have the best ESR. It is recommended to add three ceramic capacitors (100nF, 33pF, 10pF) to VBAT_BB and VBAT_RF pins, the capacitors should be placed close to the VBAT pins.

In addition, in order to ensure better power supply performance, TVS tube is added near the input end of the module VBAT to improve the surge voltage withstand capacity of the module. SYT01S05DWC is recommended. If VBAT has high-frequency interference, magnetic bead filtering is recommended. MGLB3216M601T2R0-LF is recommended. When external power supplies are connected to modules, VBAT_BB and VBAT_RF needs to use star wiring. The width of each network cable must not be smaller than 2mm. In principle, the longer the VBAT cable is, the wider the cable width is.

The reference circuit is as follows:

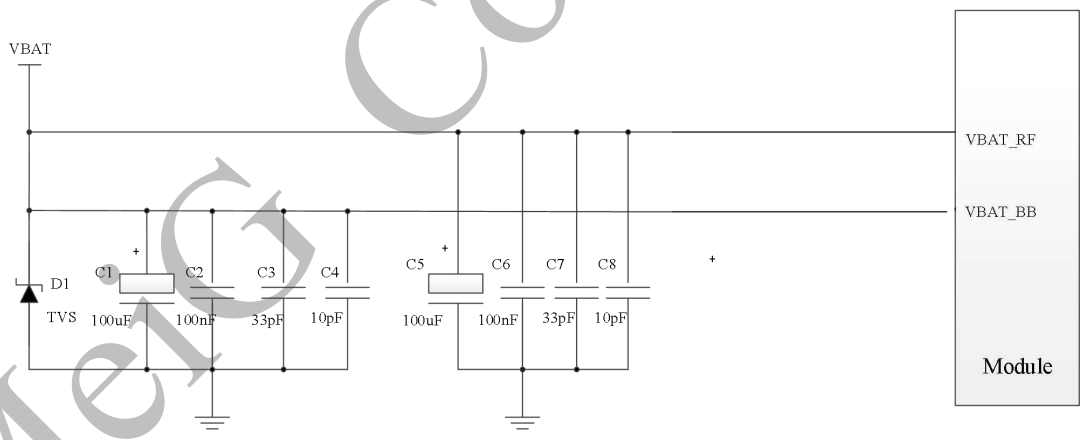

Figure 5 Power Supply Circuit

3.5.3 Power Supply Reference Circuit

The design of the module power supply is very important, because the performance of the module depends heavily on power supply. The power supply can provide at least 4A of current. If the voltage difference between the input and output is not very large, it is recommended to choose LDO as the power supply; if the voltage difference between the input and output is large, DCDC is preferred as the power supply.

Below is the reference design of the power supply circuit. The design uses SILERGY DCDC model SY8156ADC, and the peak output current can reach 5A.

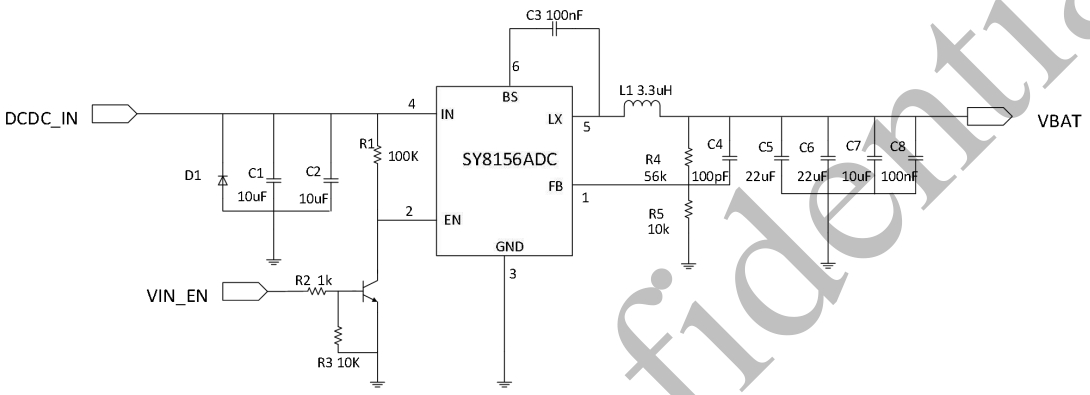

Figure 6 DC Power Supply Circuit

3.5.4 Other voltage output

SLM828G module normally started, there is a 1.8V voltage output (VREG_L6M) on Pin168, which can be used as external level reference and level pull-up. Pin162 has a 2.8V voltage output, Pin46 is SD_VIO* (VREG_L7M), you can choose to power VDDP2 using VREG_L7M or VREG_L6M through the base plate.

3.6 Starting / Shutdown

3.6.1 Level Boot

The starting mode of SLM828G is push button boot. When the module is in shutdown mode, can start the module by pulling the PWRKEY for more than 1.6s. It is recommended to use the power-on drive circuit to control the PWRKEY pin (with internal pull-up). The reference circuit is as follows:

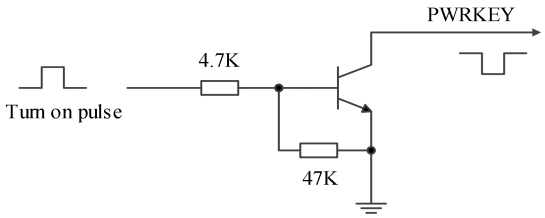

Figure 7 Open set drive reference boot circuit

Another way to control PWRKEY pin is to directly switch through a button. TVS should be placed near the button for ESD protection. The reference circuit is as follows:

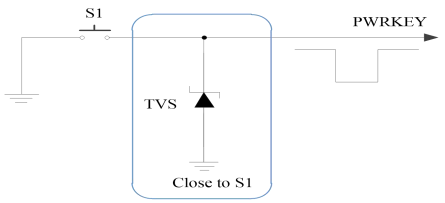

Figure 8 The buttons on the reference circuit

In addition to power on the module by PWRKEY, can also power on the module by raising PON_1 on the baseplate. PON_1 pin module has 100K internal pull-down, and external pull-up ensure that the PON_1 pin voltage is not less than 1.2V. The reference circuit is as follows:

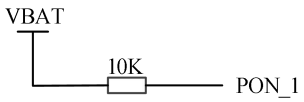

Figure 9 PON_1 power-on reference circuit

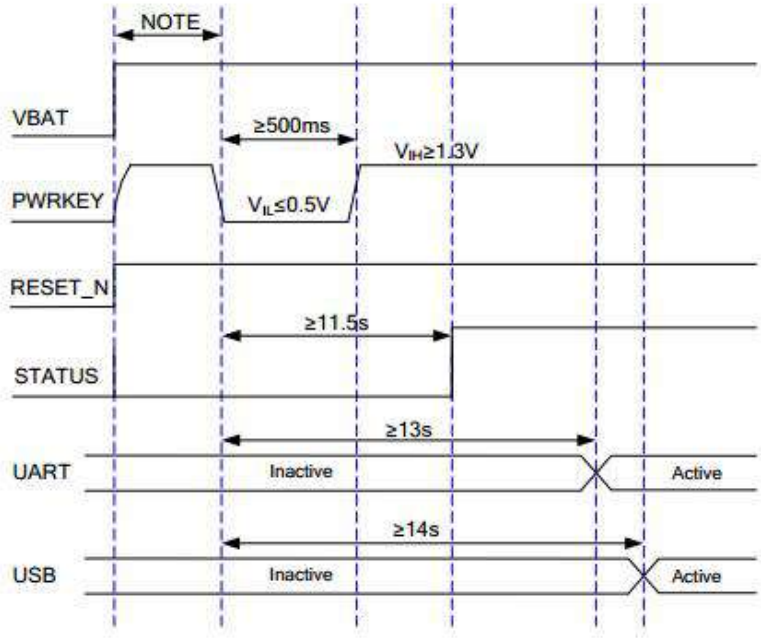

Figure 10 Power-on scene sequence diagram

Note: Ensure that the PWRKEY is lowered 30ms after the VBAT is powered on.

3.6.2 Level Shutdown

Modules can be shutdown in the following ways:

1. Press shutdown: Control module shutdown through PWRKEY pin. When the module is on, pull down the PWRKEY pin for more than 4s and release it, the module will execute shutdown process;

2. Command shutdown: Use AT+Poweroff command to control module shutdown.

The following figure shows the shutdown scenario.

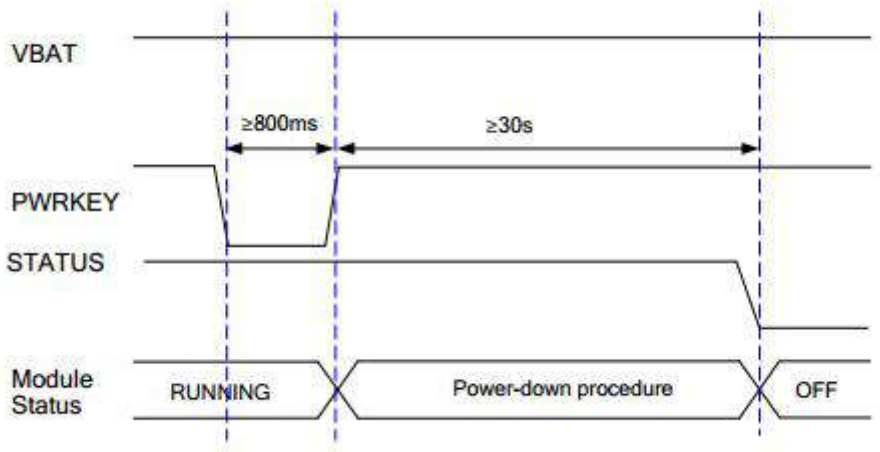

Figure 11 Shutdown scene sequence diagram

Note:

1. To avoid damage the internal circuit of the module, do not turn off the power when the module is in normal use. The power supply can be cut off only after the module is shut down by the PWRKEY or AT command.

2. When the AT command is used to shut down the module, ensure that the PWRKEY remains in the high level after the shutdown command is executed. Otherwise, the module will power on again after successfully shutting down

3.7 Reset function

There are two reset methods for SLM828G: hardware reset and AT command reset.

3.7.1 Reset by Hardware

When the module is working, lower the RESET_N pin to reset the module. The RESET_N signal is sensitive to interference. Therefore, it is recommended that the cable routing on the interface board of the module be as short as possible and should be packaged.

Table 7 RESET_N Pin Description

Pin Name	Pin Number	Description	Remark
RESET_N	1	Reset module	Active low

The reference circuit diagram is as follows: customers can use the open collector drive circuit or button to control the RESET_N pin.

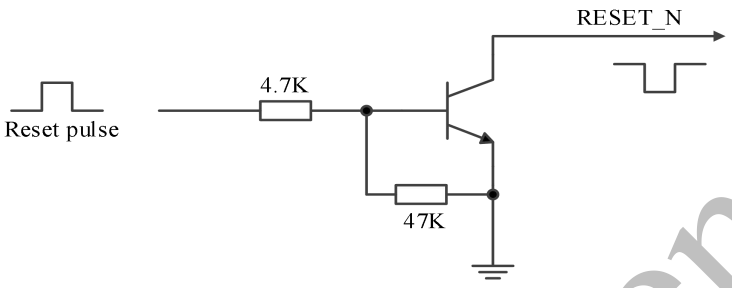

Figure 12 RESET_N Reset Open Collector Reference Circuit

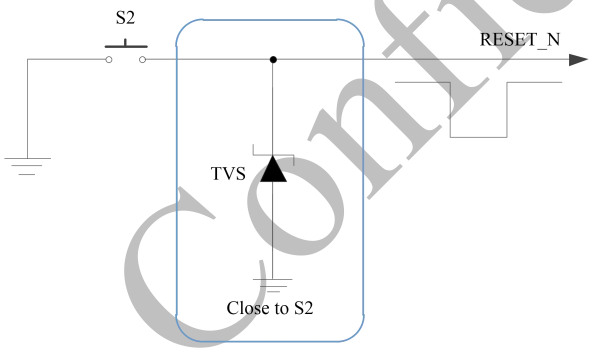

Figure 13 RESET_N Reset Button Reference Circuit

The reset sequence diagram is as follows:

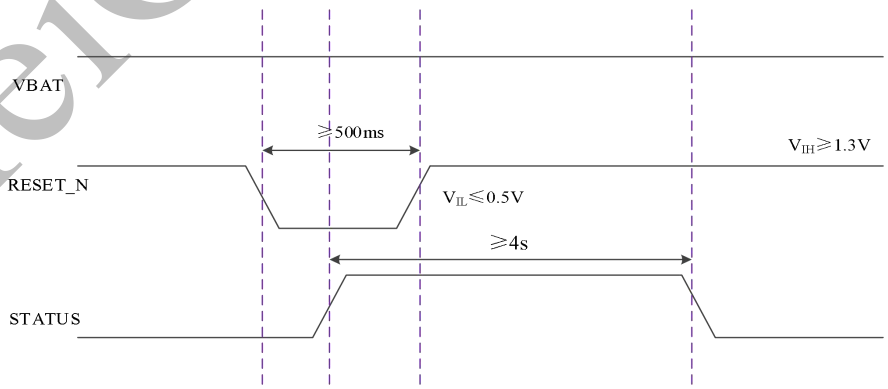

Figure 14 RESET_N Reset Sequence Diagram

3.7.2 Reset by AT Command

Through the AT port of the SLM828G USB, input the AT+RESET command to reset and restart the SLM828G.

3.8 USIM/SIM Interface

USIM card interface circuit meets the requirements of ETSI and IMT-2000 SIM interfaces. SLM828G series modules support USIM card of 1.8V and 3.0V.

3.8.1 USIM/SIM Card Interface Pin Description

SLM828G provides two sets of USIM/SIM interface signals as shown in the following table.

Table 8 USIM/SIM Interface

Pin Name	Pin Number	I/O	Description	Remark
USIM1_DET	25	DI	(U)SIM1 card hot plug detection	External pull up to 1.8V, support hot plug
USIM1_VDD	26	PO	(U)SIM1 card power supply voltage	The module automatically recognizes 1.8V or 3.0V USIM card.
USIM1_CLK	27	DO	(U)SIM1 card clock line	-
USIM1_RST	28	DO	(U)SIM1 card reset line	-
USIM1_DATA	29	IO	(U)SIM1 card data cable	Need to be pulled up to USIM1_VDD, pull-up resistors suggested 10K.
USIM2_VDD	74	PO	(U)SIM2 card power supply voltage	The module automatically recognizes 1.8V or 3.0V USIM card. Disconnect if not used.
USIM2_DATA	77	IO	(U)SIM2 card data cable	Need to be pulled up to USIM2_VDD, pull-up resistors suggested 10K. Disconnect if not used.
USIM2_DET	78	DI	(U)SIM2 card hot plug detection	External pull up to 1.8V, disconnect if not used, support hot plug.
USIM2_RST	79	DO	(U)SIM2 card reset line	Disconnect if not used.
USIM2_CLK	80	DO	(U)SIM2 card clock line	Disconnect if not used.

The SLM828G series modules support the USIM card hot plug function through the USIM_DET pin. The USIM_DET pin is an input interrupt detection pin. Hot plug function can be enabled or disabled by using the AT command. Set high/low detection. By default, hot swap is not supported.

The following figure is the reference design of SIM card connector with SIM card detection function:

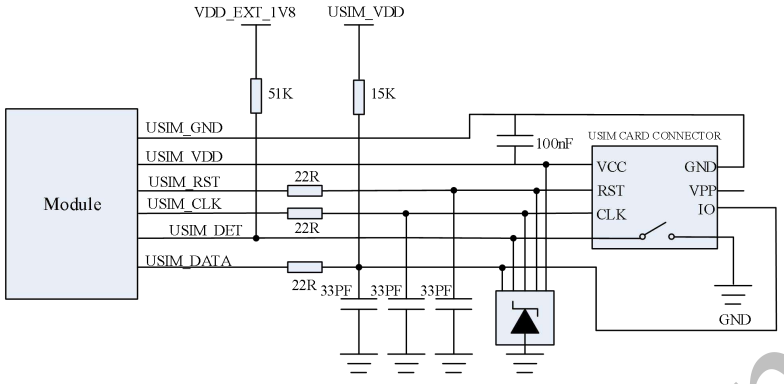

Figure 15 Reference Design Drawing of 8-Pin USIM/SIM Card Connector

SIM card connector is divided into two types according to the different design of the manufacturer:

1. Normally open type of detection pin of SIM card connector: when there is no card, the detection pin is disconnected from the ground and the module detects high level. The detection pin is connected to the ground when the card is inserted, and the module detects low level.

2. Normally closed type of detection pin of SIM card holder: when there is no card, the detection pin is connected to the ground, and the module detects low level. The detection pin is disconnected from the ground when the card is inserted, and the module detects a high level.

The detection logic of the software should be configured according to the design of the SIM card. By default, the SLM828G module software detects low level and identifies card insertion.

If USIM card detection is not required, keep the USIM_DET pin disconnect. The figure below is the 6-pin USIM card connector interface reference circuit:

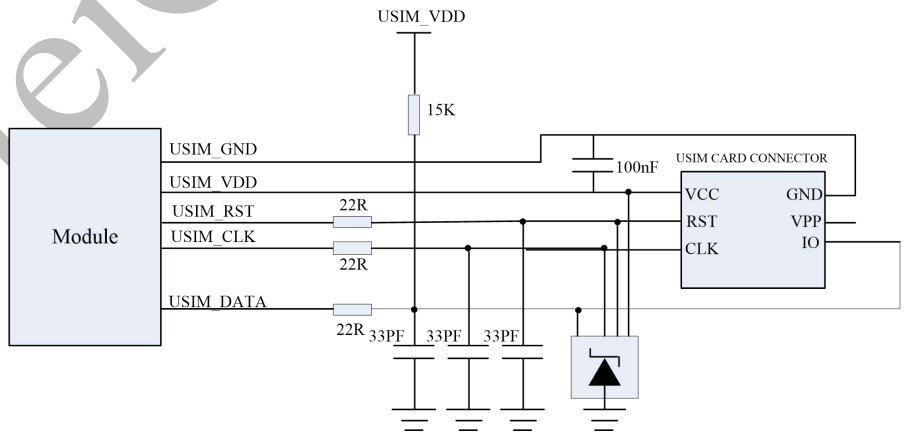

Figure 16 Reference Design Drawing of 6-Pin USIM/SIM Card Connector

In the circuit design of USIM card interface, in order to ensure the good performance and reliability of USIM card, it is recommended to follow the following design principles in circuit design:

- USIM_DATA needs a pull-up resistor to USIM_VDD, this pull-up resistor is 15kΩ; this pull-up resistor is helpful to increase the anti-interference ability of SIM card. When the routing of USIM card is too long or there is an interference source nearby, it is recommended to add a pull-up resistor near the card connector;
- Connect a 22Ω resistor in series to the USIM_DATA, USIM_CLK and USIM_RST circuits, so as to suppress stray EMI, enhance ESD protection and facilitate debugging;
- In order to improve the anti-static ability, add TVS and ESD protective device with parasitic capacitance not greater than 15pF to USIM_VDD, USIM_DATA, USIM_CLK and USIM_RST circuits;
- Connect a 33pF capacitor in parallel to USIM_VDD, USIM_DATA, USIM_CLK and USIM_RST circuits to filter out GSM900 interference; the peripheral parts of USIM card should be placed as close to USIM card connector as possible;
- USIM card connector is placed close to the module, and try best to ensure that the routing length of USIM card signal line does not exceed 200mm;
- The USIM card signal routing is far away from the RF routing and VBAT power routing;
- To prevent crosstalk between USIM_CLK signals and USIM_DATA, the wiring distance between USIM_CLK signals and USIM_DATA should be 3W.

Note: If SIM Connectors that do not support hot plug are directly used for hot plug of USIM/SIM card, it may damage USIM /SIM card or SLM828G USIM /SIM interface.

3.9 USB Interface

SLM828G series provides a USB2.0 and USB3.0 interface that complies with the USB specifications, supporting overspeed (5.0Gbps), high speed (480Mbps) and full speed (12Mbps) modes. The USB port is used for AT command exchange, data transfer, software debugging, and version upgrade.

3.9.1 USB Pin Description

SLM828G series modules provide USB2.0 andUSB3.0 interface.

Table 9 USB Interface Description

Pin Name	Pin Number	I/O	Description	Remark
USB_DP	34	IO	USB 2.0 Differential Data Signal (+)	Requires 90Ω differential impedance
USB_DM	33	IO	USB 2.0 Differential Data Signal（-）	Requires 90Ω differential impedance
USB_SS_TX_M	37	AO	USB 3.0 Differential sending signal（-）	Requires 90Ω differential impedance

USB_SS_TX_P	38	AO	USB 3.0 Differential sending signal（+）	Requires 90Ω differential impedance
USB_SS_RX_P	40	AI	USB 3.0 Differential receiving signal（+）	Requires 90Ω differential impedance
USB_SS_RX_M	41	AI	USB 3.0 Differential receiving signal（-）	Requires 90Ω differential impedance
USB_VBUS	32	PI	USB detection	Used to test whether the USB reign
USB_ID*	36	DI	OTG identification signal	1.8V, disconnect if not used. Reserved
OTG_PWR_EN*	143	DO	OTG pwr enable	Reserved

3.9.2 USB Reference Circuit

The application reference circuit of SLM828G module USB interface is shown in the following figure.

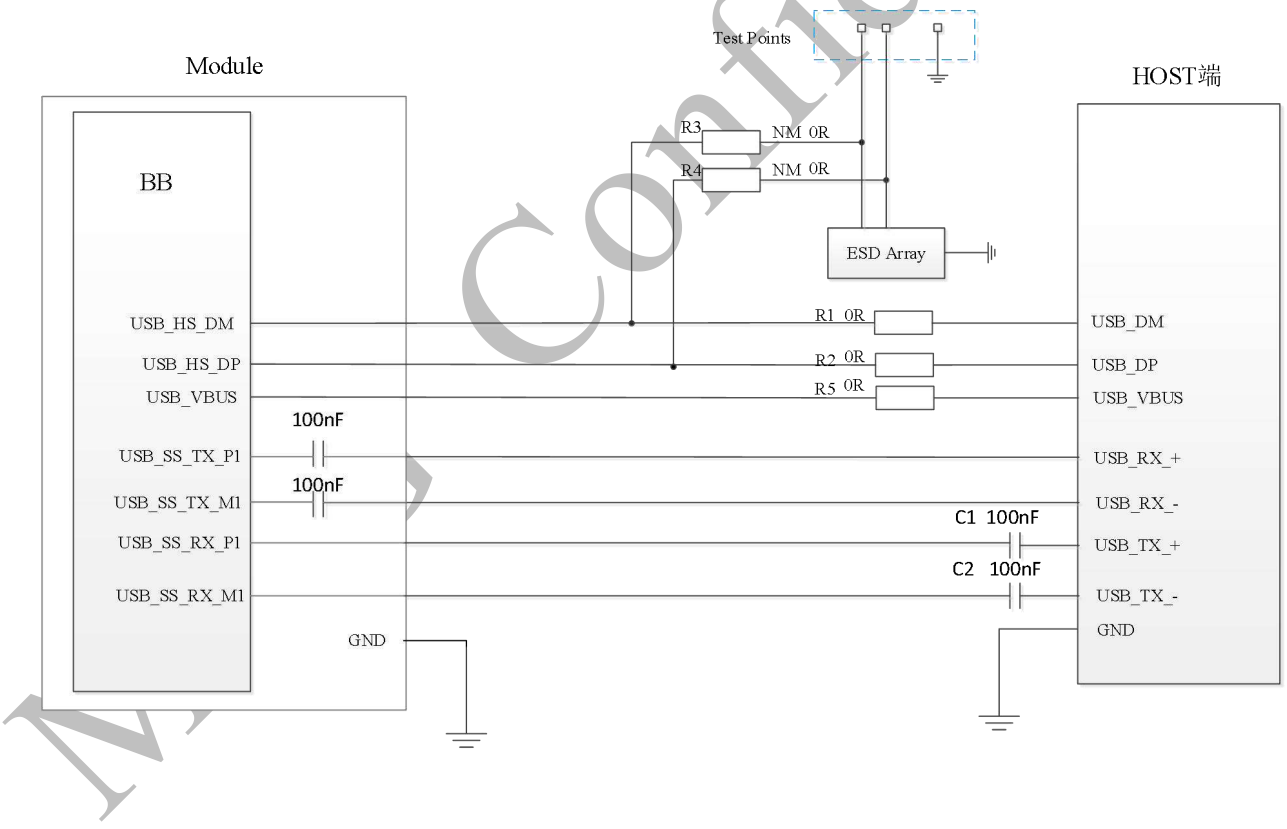

Figure 17 USB Interface Reference Design

In order to meet the requirements of signal integrity of USB data cable, capacitor C1/C2 must be placed close to HOST, and 100nF capacitor has been added to USB transmitter inside the module. The branch connecting the test point must be as short as possible. In the design of USB interface circuit, in order to ensure the performance of USB, it is recommended to follow the following principles in circuit design:

- When the USB interface of the module is connected externally. Module USB_TX signal is connected to RX signal, and module USB_RX signal is connected to TX signal.
- To decrease the signal disturbance when USB transmits data in high-speed, put R1 and R2 on USB_HS_DM and USB_HS_DP in series to increase accuracy of data transmission. Both R1 and R2 are recommended to use 0Ω;
- To improve the antistatic performance of USB ports, ESD protection devices are recommended for the USB_HS_DP, USB_HS_DM, USB_TX_P, USB_TX_M, USB_RX_P, and USB_RX_M. DP/DM is suggested to use ESD components that is less than 2pF, TX/RX is suggested to use ESD components that is less than 0.5pF, the ESD protection components should be closed to USB connector as possible.
- To increase the signal disturbance when USB3.0 transmits data in high-speed, add 100nF capacity to TX of HOST to increase the performance of EMI.
- To ensure USB can work reliably, should consider more about USB protection when designing, e.g. add 90Ω impedance for USB_HS_DP, USB_HS_DM, USB_TX_P, USB_TX_M, USB_RX_P, USB_RX_M, layout as the request of differential strictly, avoid disturbance signal.
- Don't layout USB line under crystal, oscillator, magnetic device and RF, advice layout differential line in layer and earth at left/right.

3.9.3 USB Driver

SLM828G module supports various operating systems, such as Windows7, Windows 8/8.1, Windows10, Windows11, Linux 2.6 or later, Android 2.3/4.0/4.4/5.0 or later.

USB driver provides different files for different OS, VID and PID, please contact technical support for details.

SLM828G also supports Linux and Android series embedded operating systems. As a Linux kernel system, the system will come with its driver usbserial.ko, and no special SLM828G USB driver is provided. All are to load the system's usbserial.ko to load the SLM828G module USB. The key is to find the driver file usbserial.ko, load PID and VID into the system.

3.10 PCM&SPI&IIC Interface

SLM828G provides PCM, SPI and IIC interfaces

The following table describes PCM interface signals

Table 10 PCM interface description

Pin Name	Pin Number	I/O	Description	Remark
PCM_SYNC	65	DI	PCM data synchronization signal	1.8V power domain. Module as the master device, the pin as the output signal, module as the slave device, the pin as the input signal. Disconnect when not in use.

PCM_IN	66	DO	PCM data input	1.8V power domain, disconnect when not in use
PCM_CLK	67	IO	PCM clock	1.8V power domain. Module as the master device, the pin as the output signal, module as the slave device, the pin as the input signal. Disconnect when not in use.
PCM_OUT	68	IO	PCM data output	1.8V power domain, disconnect when not in use

PCM interface and supports the following 2 modes:

- Short frame mode: the module can be the master or slave
- Long frame mode: the module can only be the main device

In short frame mode, data is sampled on the falling edge of PCM_CLK and sent on the rising edge. The falling edge of PCM_SYNC represents the high effective bit. PCM_CLK supports 128, 256, 512, 1024 and 2048kHz speech coding.

In the long frame mode, data is sampled on the falling edge of PCM_CLK and sent on the rising edge. The rising edge of PCM_SYNC represents the high effective bit. Only 128 kHz PCM_CLK and 8kHz, 50% duty cycle PCM_SYNC are supported.

SLM828G module supports 8-bit A-law, u-law and 16-bit linear encoding formats. The following two figures are the short frame mode sequence diagram (PCM_SYNC=8 kHz, PCM_CLK=2048kHz) and the long frame mode sequence diagram (PCM_SYNC=8 kHz, PCM_CLK=128kHz).

The clock and mode can be set by the AT instruction, default setting is short frame mode, PCM_SYNC=8 kHz, PCM_CLK=2048 kHz.

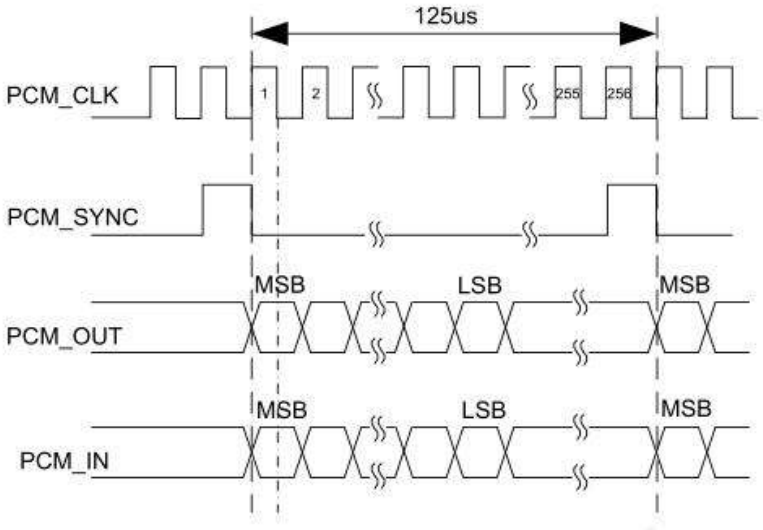

Figure 18 Short frame Mode Sequence Diagram

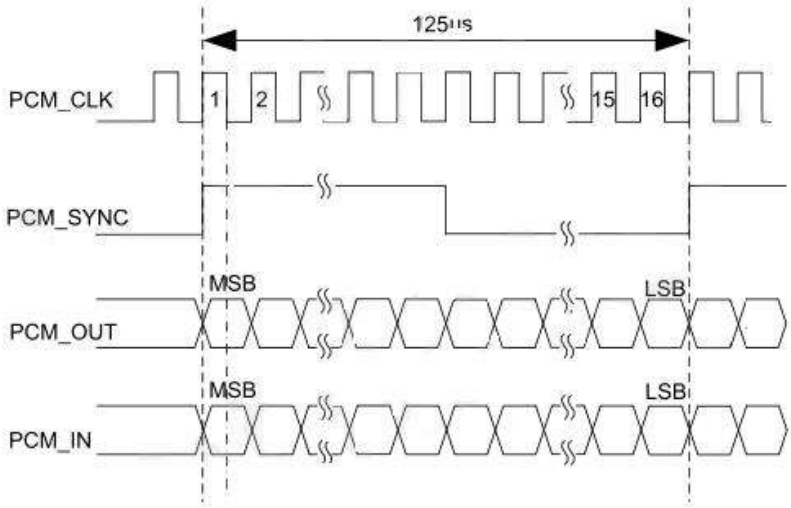

Figure 19 Long frame Mode Sequence Diagram

The following table describes the SPI interfaces

Table 11 SPI interface description

Pin Name	Pin Number	I/O	Description	Remark
SPI_MOSI	6	DO	SPI Data input and output signals	1.8V power domain, disconnect when not in use
SPI_MISO	7	DI	SPI Data input and output signals	1.8V power domain, disconnect when not in use
SPI_CS	8	DO	SPI Film selection signal	1.8V power domain, disconnect when not in use
SPI_CLK	9	DO	SPI Clock signal	1.8V power domain, disconnect when not in use

SPI interface timing diagram is shown below.

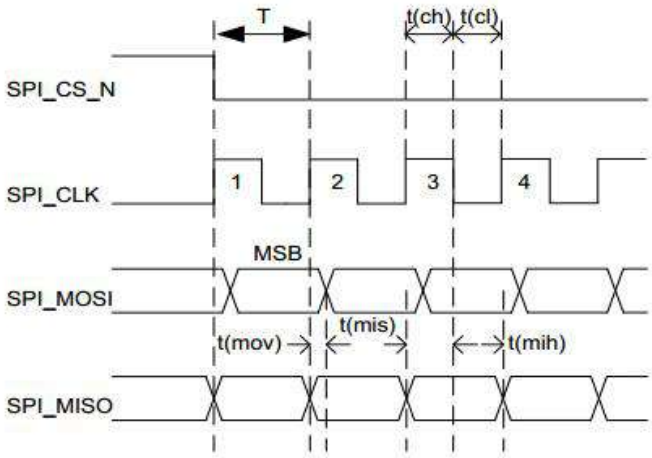

Figure 20 SPI interface timing diagram

SPI timing of related parameters shown in the following table.

Table 12 SPI interface timing requirement

Type	Description	Minimum	Typical	Maximum	Unit
T	SPI clock period	20.0	-	-	ns
t(ch)	SPI clock high level time	9.0	-	-	ns
t(cl)	SPI clock low level time	9.0	-	-	ns
t(mov)	SPI master data output valid time	-5.0	-	5.0	ns
t(mis)	SPI master data input setup time	5.0	-	-	ns
t(mih)	SPI master data input hold time	1.0	-	-	ns

Table 13 I2C interface description

Pin Name	Pin Number	I/O	Description	Remark
I2C_SDA	42	OD	I2C data	Module internal pull up 1.8 V, disconnect when not in use.
I2C_SCL	43	OD	I2C clock	Module internal pull up 1.8 V, disconnect when not in use.
I2S_MCLK	152	DO	I2S output clock signal	Can be used as external CODEC input clock signal, disconnect when not in use.

The following figure shows the SPI and PCM interface reference design of the external Slic chip (SI32185):

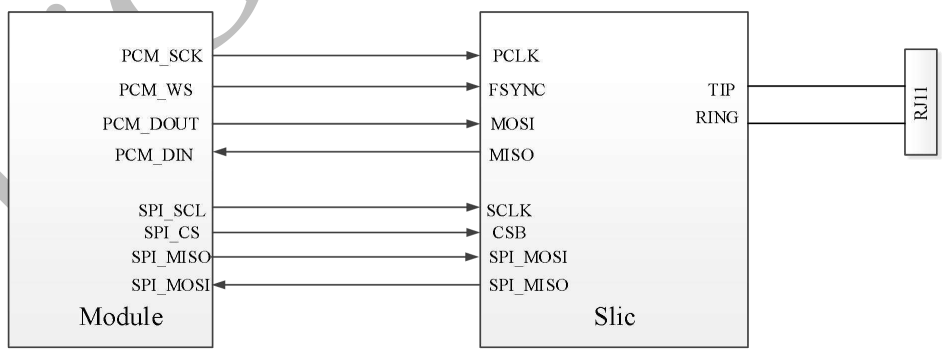

Figure 21 PCM&SPI Circuit reference design

SLM828G can be equipped with external Codec chip, configured with PCM&I2C interface to realize voice call function. The following is a reference design for the PCM interface with an external Codec chip (I2C module internal pull-up):

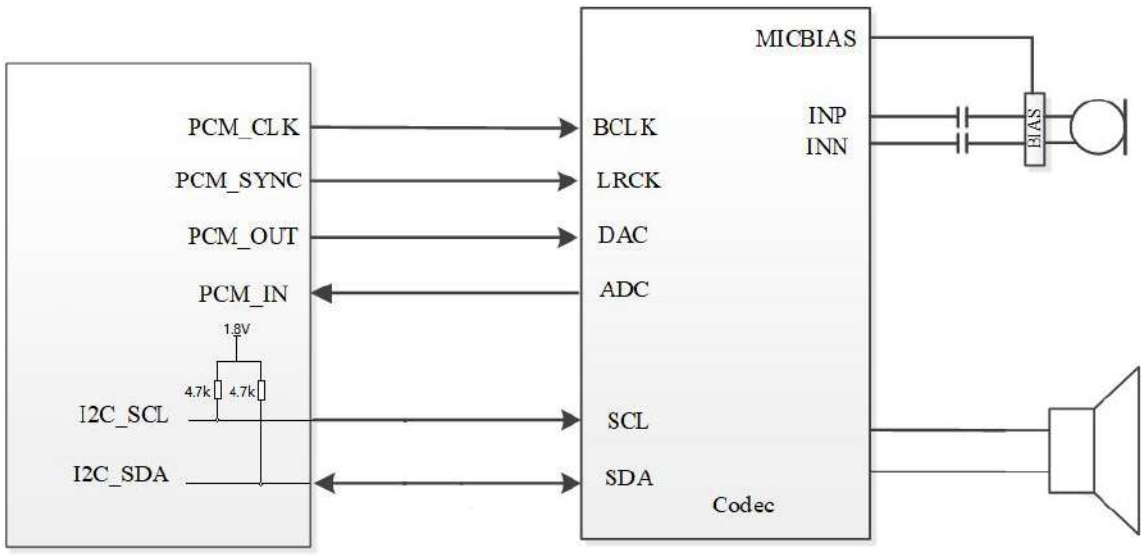

Figure 22 PCM&IIC Circuit reference design

3.11 Network Status Indication

The network status indicator pin is used to drive the network status indicator. SLM828G module has three network STATUS pins: NET_MODE, STATUS and NET_STATUS. The following two tables describe pin definitions and logic level variations for different network states.

Table 14 Network Indicator Pin Description

Pin Name	Pin Number	I/O	Remark
NET_MODE	147	DO	Registered network type indicator
NET_STATUS	170	DO	Network connection status indicator(default)
STATUS	171	DO	System working status indicator

Table 15 Network Indication Work Status Description

Mode	Status	Description
NET_MODE	Blinking (2000ms ON/500ms OFF)	Activate 4G
	Close	Others
NET_ STATUS	Blinking (100ms ON/300ms OFF)	Successfully registered data services exist

	Blinking (100ms ON/3000ms OFF)	Registered successfully
	Blinking (100ms ON/800ms OFF)	Search process
	Close	Others (flight mode, no service, shutdown, etc.)
STATUS	Steady light	Power on
	Close	Others

The indicator interface reference circuit of SLM828G is shown in the figure below. The brightness of LED can be controlled by adjusting the resistance value of R.

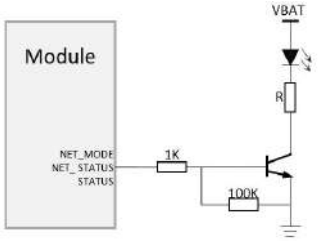

Figure 23 Network Instructions Reference Design Diagram

3.12 ADC Function

SLM828G provides two AD conversion interfaces. AT+ADCREAD is used to read the sampling values of each ADC channel. For specific AT commands, please refer to our AT command set.

In order to improve the accuracy of ADC voltage measurement, ADC needs to be covered during wiring.

Table 16 ADC Pin Description

Pin Name	Pin Number	Description	Voltage Range	Remark
ADC0	173	0 AD converter interface	0 – 1.875V	Disconnect if not in use
ADC1	175	1 AD converter interface	0 – 1.875V	Disconnect if not in use

Note:

1. Suggest the ADC input pin using partial pressure circuit.
2. Without power supply for the module, the ADC interface cannot be directly connected to any input voltage.

3.13 PCIe Interface

SLM828G module provides one PCIe Gen2 port. PCIe supports a maximum rate of 5 Gb/s.

The PCIe interface pins are defined as follows:

Table 17 PCIe Interface Pin Description

Pin Name	Pin Number	I/O	Description	Remark
PCIE_CLK_P	179	AI,AO	RC mode: PCIe Differential clock + output (default) EP mode: PCIeDifferential clock + input	Difference 100 Ω impedance control
PCIE_CLK_M	180	AI,AO	RC mode: PCIe Differential clock - output (default) EP mode: PCIe Differential clock - input	Difference 100 Ω impedance control
PCIE_TX_M	182	AO	PCIE_ transmission send - signal	Difference 100 Ω impedance control
PCIE_TX_P	183	AO	PCIE_ transmission send + signal	Difference 100 Ω impedance control
PCIE_RX_M	185	AI	PCIE_ transmission reception - signal	Difference 100 Ω impedance control
PCIE_RX_P	186	AI	PCIE_ transmission reception + signal	Difference 100 Ω impedance control
PCIE_CLKREQ	188	IO	PCIe clock request	External pull-up 100 k Ω resistance RC mode: Request input (default) EP mode: Request output Disconnect when not in use.
PCIE_HOST_RST_N	189	IO	PCIe reset	RC mode: PCIe reset output
PCIE_WAKE	190	IO	PCIe wake up	External pull-up 100 k Ω resistance RC mode: PCIe wake up input (default) EP mode: PCIe wake up output

PCIe interface for RC mode and Ethernet PHY communication reference:

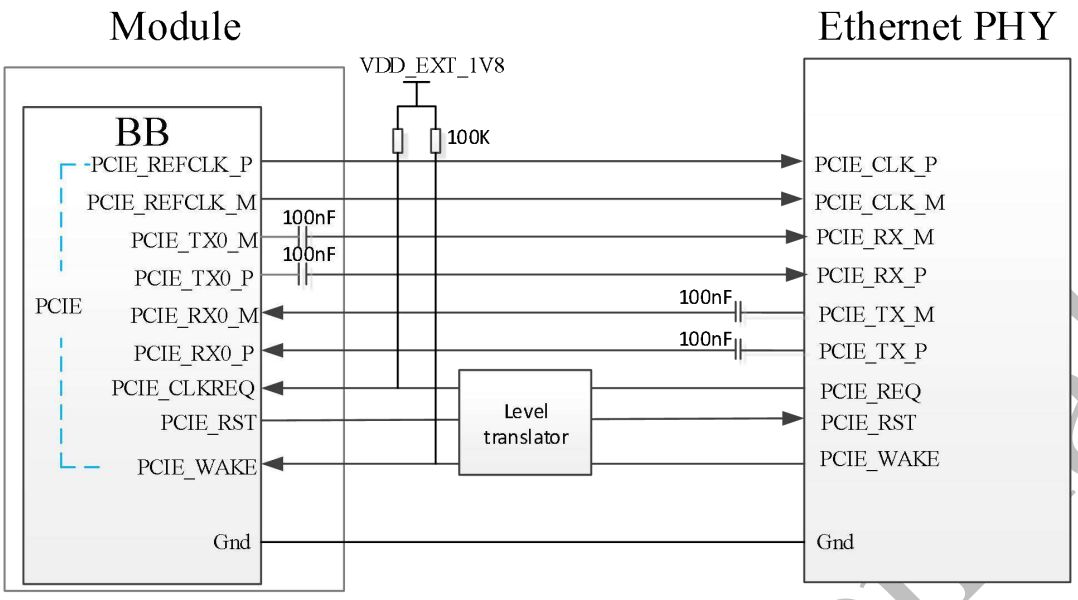

Figure 24 PCIe and Ethernet PHY connection reference circuit

PCIe interface used for communication with HOST in EP mode

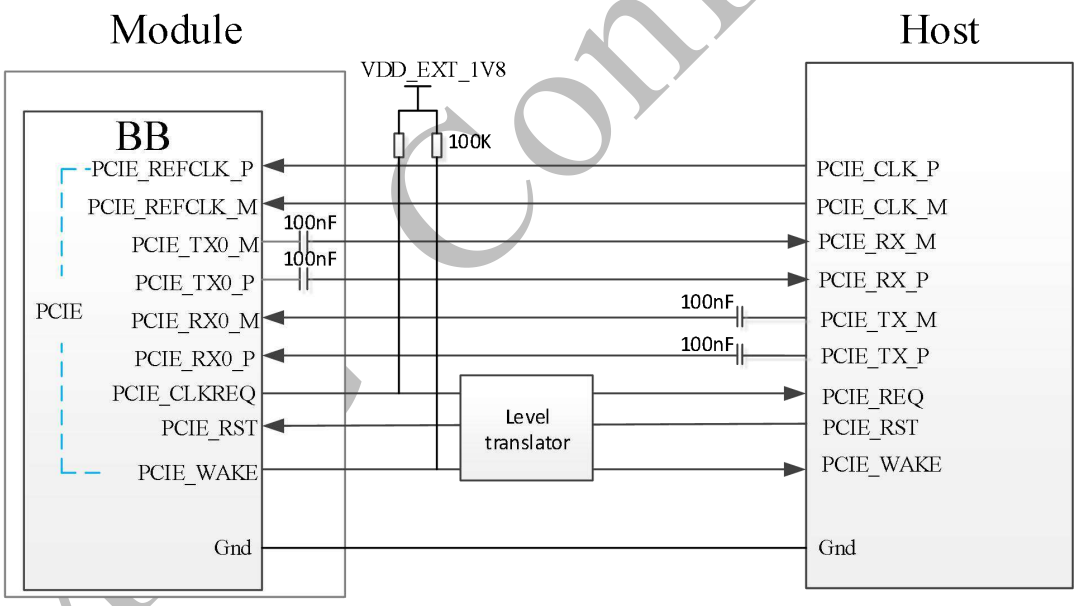

Figure 25 PCIe and HOST connection reference circuit

PCIe in circuit design suggestions please see following principles:

- The module has a 100nF AC capacitor for PCIe_TX_P/M signals. Do not need to add an AC capacitor on the peer PCIe TX signal cable.
- PCIE_CLKREQ, PCIE_RST, PCIE_WAKE signal power domain is 1.8V, CLKREQ and WAKE signals need external pull-up, level conversion circuit needs to be added when the levels are inconsistent.
- Differential impedance control of 100 Ω ±10Ω is required for PCIe differential cabling. A complete reference plane is required for cabling.

- Internal equal length control is required for PCIe differential cabling. The internal equal length must be less than 0.15mm. The PCIe cabling length should be as short as possible.
- Keep the PCIe signal cable away from sensitive signals, such as RF circuits, analog signals, clock signals, DCDC and so on.

3.14 SDIO Interface*

SLM828G module SDIO interface support SD card. Interface pins are defined in the following table:

Table 18 Interface pins description

Pin Name	Pin Number	I/O	Description	Remark
SD_VIO*	46	PO	SD card: SDIO Pull-up	L7 control (select SD card function)
SD_DATA0	49	IO	SDC data bit0	Disconnect if not in use.
SD_DATA1	50	IO	SDC data bit1	Disconnect if not in use.
SD_DATA2	47	IO	SDC data bit2	Disconnect if not in use.
SD_DATA3	48	IO	SDC data bit3	Disconnect if not in use.
SD_CMD	51	DO	SD card command signal	Disconnect if not in use.
SD_ DET	52	DI	SD card hot plug detection signal	Disconnect if not in use.
SD_CLK	53	DO	SD card clock signal	Disconnect if not in use.
SD_PWR_EN	15	IO	External SD card power switch control signal	Reserved

Below is the SD card reference design:

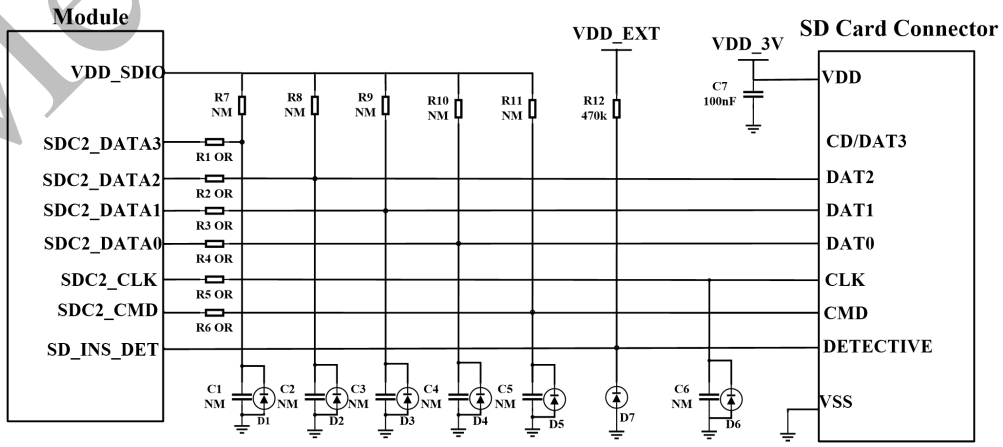

Figure 26 SD card reference design

Please follow the below principles to design SD card circuit:

- SD card power supply with voltage range of 2.7V to 3.6V and current of 0.8A shall be provided. VDD_SDIO has a maximum output current of 50mA and can be used as a pull-up level for SDIO signals.
- To prevent the current fluctuation beyond the maximum range when the SD card is inserted, the bypass capacitor C7 of the SD card power supply should be less than 5uF
- To avoid bus jitter, the SDIO signal needs to be pulled up to VDD_SDIO through R7 to R11 resistors. The resistance value between 10 ~ 100 k Ω, recommended value 100 k Ω.
- To improve signal quality, it is recommended to add 0 ohm series matching between module and SD card from R1 to R6, as close as possible to the module end. Bypass capacitor C1 to C6 reserved, not attached by default.
- In order to better prevent static electricity, it is recommended that TVS be added to the pin of SD card.
- SDIO load capacitance should be less than 40pf.
- SDIO signal wiring is very important, the impedance is controlled at 50Ω (±10%).
- Keep SDIO signals away from other sensitive signals, such as RF circuits, analog signals, clock signals and DCDC signals.
- It is recommended that the cable length difference between CLK and DATA/CMD be less than 1mm, and the total cable length be less than 50mm. The length of cabling inside the module is 27mm. Therefore, the length of external cabling must be smaller than 23mm.
- Ensure that the distance between adjacent cables is twice the width of the cables, and that the capacitance is less than 40pf.

3.15 USB_BOOT Interface

SLM828G module supports emergency download mode from the USB2.0 interface. Before the module is power on, pull the USB_BOOT to 1.8V (VDD_EXT_1V8 is recommended). When the module is started, it will enter the forced USB download mode. In this mode, the software of the module can be upgraded through the USB2.0 interface

Table 19 USB_BOOT pin defination

Pin Name	Pin Number	I/O	Description	Voltage Range
USB_BOOT	140	DI	Emergency download mode control input, active at high level	1.8V power domain, advised to reserve test points. Disconnect when not in use.

USB_BOOT interface reference circuit is as follows:

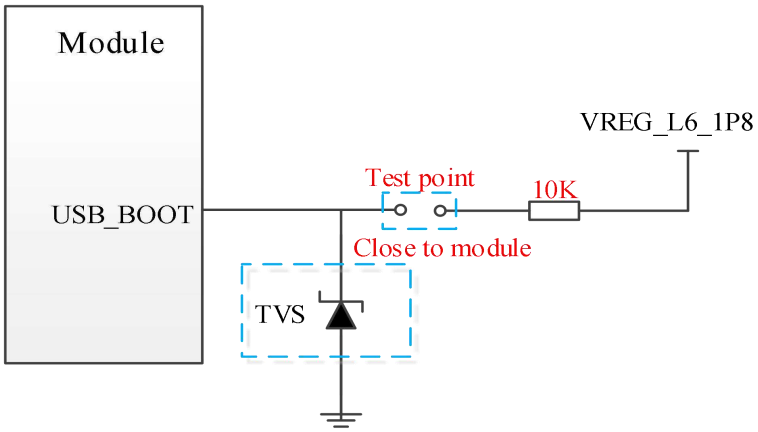

Figure 27 USB_BOOT interface reference circuit

3.16 Sleep wake up

A low level signal is given to the module through the W_DISABLE_N pin of the SLM828G and the module enters flight mode at which time the RF transceiver unit will stop working. Raising the W_DISABLE_N pin module will re-enter normal mode.

When the Wakeup_in pin is pulled down, the module is allowed to enter sleep mode. When the Wakeup_in pin is pulled up or some other wake-up signal is received, the module exits sleep mode and SLEEP_IND is used to indicate the state.

3.17 Serial ports

The module has three serial ports: main serial port, DEBUG serial port and reserved bluetooth serial port.

Serial port to support 9600,19200,38400,57600,115200,230400,460800 baud rate, the default baud rate to 115200 BPS, can be configured to support the RTS and CTS flow control. Used for data transmission and AT command transmission. The debugging serial port supports the baud rate of 115200bps and is used for Linux control and log printing.

Table 20 Serial port pin description

Main UART imterface				
Pin Name	**Pin Number**	**I/O**	**Description**	**Remark**
CTS	56	DO	Clear to send	1.8V power domain, disconnect when not in use.
RTS	57	DI	Request to send	1.8V power domain, disconnect when not in use.

UART1_RXD*	58	DI	Module receiving data	1.8V power domain, disconnect when not in use.
UART1_DCD*	59	DO	Output carrier detection module	1.8V power domain, disconnect when not in use.
UART1_TXD*	60	DO	Module sending data	1.8V power domain, disconnect when not in use.
UART1_RI	61	DO	Output module is ringing	1.8V power domain, disconnect when not in use.
UART1_DTR*	62	DI	Ready, sleep mode control	11.8V power domain, disconnect when not in use.

Table 21 Serial port pin description

Debug UART interface				
Pin Name	**Pin Number**	**I/O**	**Description**	**Remark**
DBG_TXD	137	DO	DEBUG serial port sending	1.8V power domain, disconnect when not in use.
DBG_RXD	136	DI	DEBUG serial port receiving	1.8V power domain, disconnect when not in use.

Table 22 Bluetooth serial port pin definition

Bluetooth UART interface*				
Pin Name	**Pin Number**	**I/O**	**Description**	**Remark**
BT_EN*	3	DO	BT function enable pin	1.8V power domain, disconnect when not in use.
UART2_TXD*	163	DO	Bluetooth serial port sends data signals	1.8V power domain, disconnect when not in use.
BT_CTS	164	DO	Bluetooth serial port clear sends data signal	1.8V power domain, disconnect when not in use.
UART2_RXD*	165	DI	Bluetooth serial port receives data signals	1.8V power domain, disconnect when not in use.
BT_RTS	166	DI	Bluetooth serial port request to send data signal	1.8V power domain, disconnect when not in use.

Table 23 Serial Port Logic Level

Parameter	Minimum Value	Maximum Value	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	1.2	2.0	V
V_{OL}	0	0.45	V

V_{OH}	1.35	1.8	V

The serial port level of SLM828G module is 1.8V. If the customer host level is inconsistent, a level converter should be added to the serial port application. The following figure is a reference design:

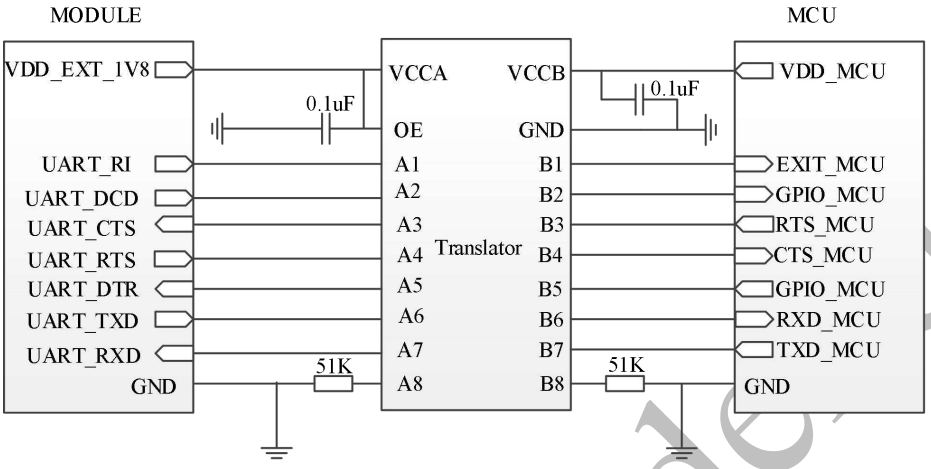

Figure 28 UART Level switching reference circuit

3.18 Adjustable Antenna Control Interface *

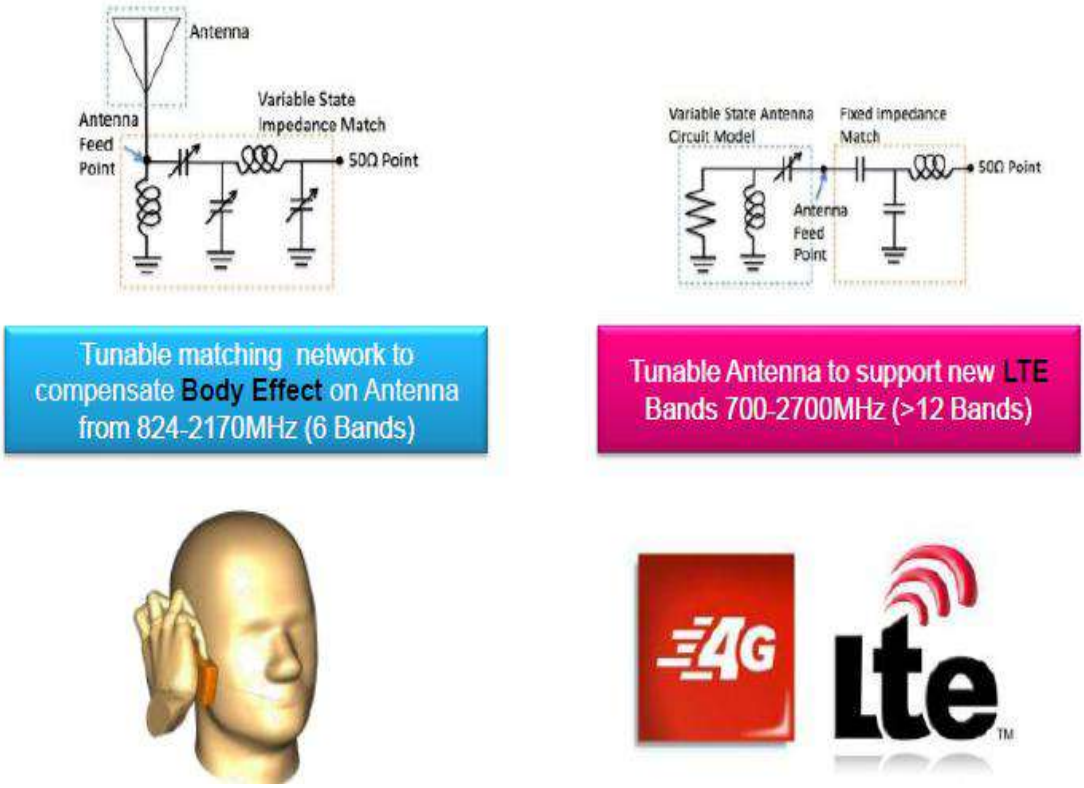

Figure 29 Principle of adjustable antenna

SLM828G supports RFFE interfaces or dedicated GPIO adjustable antenna control interfaces for antenna performance optimization and conditions. Customers can choose one of these based on their tuner design. Below is the definition of pin RFFE and dedicated GPIO interfaces

Table 24 Adjustable antenna interface Pin Description

Adjustable antenna interface				
Pin Name	Pin Number	I/O	Description	Remark
VDD_RF_2V8	162	PO	Module output power supply	Disconnect when not in use
RFFE_CLK*	71	DO	External control RFFE interface	Disconnect when not in use
RFFE_DATA*	73	IO	External control RFFE interface	Disconnect when not in use
GPIO_3	159	IO	General GPIO	Disconnect when not in use
GPIO_4	161	IO	General GPIO	Disconnect when not in use
GPIO_5	172	IO	General GPIO	Disconnect when not in use

3.19 GPIOs*

In addition to three GPIO dedicated to external tuner control, the module provides two generic input/output interfaces for customer design.

Table 25 GPIOs Interface Description

General GPIO Interface				
Pin Name	Pin No	I/O	Description	Remark
GPIO_1	138	IO	General GPIO	Disconnect when not in use
GPIO_2	139	IO	General GPIO	Disconnect when not in use

4 GNSS

4.1 Basic Description

SLM828G includes a complete embedded GNSS solution that supports Qualcomm Gen9C-Lite (GPS, Glonass, Galileo, BeiDou).

The SLM828G module supports the standard NMEA-0183 protocol and outputs 1Hz NMEA sentences through the USB interface by default.

4.2 GNSS Antenna Interface

The following table is the pin definition and frequency specification of GNSS antenna interface.

Table 26 Antenna interface pin definition

Pin Name	Pin No.	Description	I/O	Remark
ANT_GNSS	119	GNSS antenna interface	AI	50 Ω impedance

Table 27 GNSS frequency

Type	Frequency	Unit
GPS/Galileo/QZSS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
BeiDou	1561.098±2.046	MHz

GNSS needs to be connected to an active antenna, the reference design is shown in the figure below:

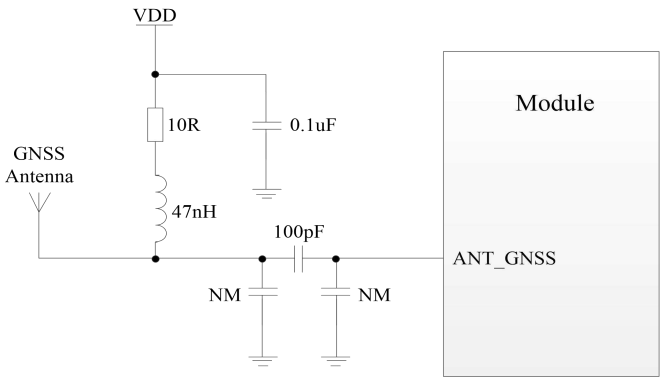

Figure 30 GNSS antenna reference circuit

Note: Customers can choose external LDO power supply according to the type of active antenna.

4.3 GNSS performance

The following table lists the GNSS performance of the SLM828G module.

Table 28 SLM828G GNSS performance

Parameter	Description	Performance index
Positioning accuracy (wide place)	CEP-50	<5m
Initial Positioning Time TTFF(wide place)	Cold reboot	35S
	Warm boot	30S
	Hot reboot	2S
Sensitivity	Cold reboot	-146dBm
	Capture	-157dBm
	Track	-158dBm

Note: this data is tested using 18dB gain LNA.

4.4 Layout Guidance

Customers need to follow the following Layout guidelines in design:

- Digital signals such as USIM card, USB interface, camera module, display interface and SD card should be kept away from the antenna
- Sensitive analog signals should be far away from the GNSS signal path, and ground holes should be added for isolation and protection
- ANT_GNSS layout maintains 50Ω characteristic impedance

5 Antenna Interfaces

5.1 Antenna Interface Introduction

SLM828G module is designed with the main antenna interface, diversity antenna interface and a GNSS antenna interface. The antenna interface impedance is 50Ω.

Table 29 RF Antenna Pin Definition

Pin Name	Pin No.	I/O	Description	Remark
ANT_MIMO1	101	DO	MIMO1 antenna	50Ω impedance
ANT_MAIN	107	DO	Main antenna	50Ω impedance
ANT_MIMO2	113	DO	MIMO2 antenna	50Ω impedance
ANT_GNSS	119	DO	GNSS antenna	50Ω impedance
ANT_DIV	127	DO	Diversity antenna	50Ω impedance

It is recommended to use antenna with 50Ω impedance matching the RF connector of the module. (To ensure communication capability in all frequency bands, please connect both main and auxiliary antennas.)

The reference design circuit for antenna connection of ANT_MAIN, ANT_DIV, ANT_MIMO1 and ANT_MIMO2 is shown below. In order to obtain better RF performance, it is necessary to reserve π type matching circuit, and the capacitor is not attached by default.

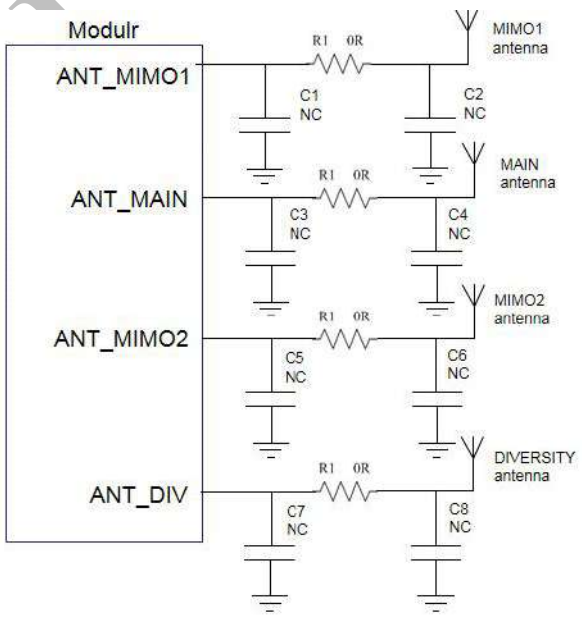

Figure 31 RF reference circuit

It is recommended to choose the RF adapter cable carefully. The user needs to choose the RF adapter cable with the smallest loss possible. It is recommended to use the RF adapter cable with the following RF loss requirements:

- WCDMA2100<1.5dB
- WCDMA900<1dB
- TDD-LTE<1.5dB
- FDD-LTE<1.5dB

5.2 Antenna Installation

5.2.1 Antenna Requirements

The main antenna, diversity antenna and GNSS antenna requirements are as follows:

Table 30 Antenna Requirements

Type	Requirements
GNSS	Frequency range: 1561-1615MHz
	Polarization: RHCP or linear
	VSWR：< 2（Typ.）
	Active antenna noise figure: <1.5 dB
	Active antenna gain:> -2 dBi
	Active antenna built-in LNA gain: 20 dB (typical value)
	Active antenna total gain:> 18 dBi (typical value)
WCDMA /TDD-LTE/FDD-LTE	VSWR：< 2
	Gain (dBi): 1
	Maximum input power (W): 50
	Input impedance (ohm): 50
	Polarization type: vertical direction
	Cable insertion loss: < 1dB
	（WCDMA B4，LTE B4） Cable insertion loss: < 1.5dB

	（WCDMA B2/B4/B5， LTE B2/B4/B5/B7/B8/B20/B28/B38/B39/B40/B41/B42/B43/B48） Cable insertion loss: < 2dB

5.2.2 RF Output Power

The RF output power of SLM828G series modules is shown in the following table.

Table 31 RF Output Power（LA）

Network mode	Band	Max	Min
WCDMA	Band2/4/5	23dBm ± 2.7dB	-56dBm ± 4dB
TDD-LTE	Band38	23dBm ± 2.7dB	≤-44 ± 1dBm
	Band39	23dBm ± 2.7dB	≤-44 ± 1dBm
	Band40	23dBm ± 2.7dB	≤-44 ± 1dBm
	Band41	23dBm ± 2.7dB	≤-44 ± 1dBm
	Band42	23dBm ± 2.7dB	≤-44 ± 1dBm
	Band43	23dBm ± 2.7dB	≤-44 ± 1dBm
	Band48	23dBm ± 2.7dB	≤-44 ± 1dBm
FDD-LTE	Band2	23dBm ± 2.7dB	≤-44 ± 1dBm
	Band4	23dBm ± 2.7dB	≤-44 ± 1dBm
	Band5	23dBm ± 2.7dB	≤-44 ± 1dBm
	Band7	23dBm ± 2.7dB	≤-44 ± 1dBm
	Band8	23dBm ± 2.7dB	≤-44 ± 1dBm
	Band20	23dBm ± 2.7dB	≤-44 ± 1dBm
	Band28	23dBm ± 2.7dB	≤-44 ± 1dBm
	Band66	23dBm ± 2.7dB	≤-44 ± 1dBm

Table 32 RF Output Power（EU）

Network mode	Band	Max	Min

WCDMA	Band1/3/5	23dBm ± 2.7dB	-56dBm ± 4dB
TDD-LTE	Band38	23dBm ± 2.7 dB	≤-44 ± 1dBm
	Band39	23dBm ± 2.7 dB	≤-44 ± 1dBm
	Band40	23dBm ± 2.7 dB	≤-44 ± 1dBm
	Band41	23dBm ± 2.7 dB	≤-44 ± 1dBm
	Band42	23dBm ± 2.7 dB	≤-44 ± 1dBm
	Band43	23dBm ± 2.7 dB	≤-44 ± 1dBm
FDD-LTE	Band1	23dBm ± 2.7 dB	≤-44 ± 1dBm
	Band3	23dBm ± 2.7 dB	≤-44 ± 1dBm
	Band5	23dBm ± 2.7 dB	≤-44 ± 1dBm
	Band7	23dBm ± 2.7 dB	≤-44 ± 1dBm
	Band8	23dBm ± 2.7 dB	≤-44 ± 1dBm
	Band20	23dBm ± 2.7 dB	≤-44 ± 1dBm
	Band28	23dBm ± 2.7 dB	≤-44 ± 1dBm

5.2.3 RF Receiving Sensitivity

Table 33 RF Receiving Sensitivity（LA）

Network mode	Band	Receive sensitivity
WCDMA	Band2	-108dBm
	Band4	-108dBm
	Band5	-108dBm
TDD-LTE	Band38	-98dBm
	Band39	-99dBm
	Band40	-97dBm
	Band41	-97dBm

	Band42	-97dBm
	Band43	-97dBm
	Band48	-97dBm
FDD-LTE	Band2	-98dBm
	Band4	-98dBm
	Band5	-99dBm
	Band7	-96dBm
	Band8	-99dBm
	Band20	-99dBm
	Band28	-99dBm
	Band66	-97dBm

Table 34 RF Receiving Sensitivity（EU）

Network mode	Band	Receive sensitivity
WCDMA	Band1	-108dBm
	Band3	-108dBm
	Band5	-108dBm
TDD-LTE	Band38	-97dBm
	Band39	-97dBm
	Band40	-97dBm
	Band41	-97dBm
	Band42	-97dBm
	Band43	-97dBm
FDD-LTE	Band1	-97dBm
	Band3	-98dBm

	Band5	-99dBm
	Band7	-96dBm
	Band8	-99dBm
	Band20	-99dBm
	Band28	-99dBm
	Band32	-98dBm

Note:

WCDMA, LTE sensitivity test results.

5.2.4 Working Frequency

Table 35 Working Frequency（LA+EU）

Network mode	Band	Receive	Transmit
WCDMA	Band1	2110~2170MHz	1920~1980MHz
	Band2	1930~1990MHz	1850~1910MHz
	Band3	1805~1880MHz	1710~1785MHz
	Band4	2110~2155MHz	1710~1755MHz
	Band5	869~894MHz	824~ 849MHz
TDD-LTE	Band38	2570~2620MHz	2570~2620MHz
	Band39	1880~1920MHz	1880~1920MHz
	Band40	2300~2400MHz	2300~2400MHz
	Band41	2496~2690MHz	2496~2690MHz
	Band42	3400~3600MHz	3400~3600MHz
	Band43	3600~3800MHz	3600~3800MHz
	Band48	3550~3700MHz	3550~3700MHz
FDD-LTE	Band1	2110~2170MHz	1920~1980MHz

Band2	1930~1990MHz	1850~1910MHz
Band3	1805~1880MHz	1710~1785MHz
Band4	2110~2155MHz	1710~1755MHz
Band5	869~894MHz	824~849MHz
Band7	2620~2690MHz	2500~2570MHz
Band8	925~960MHz	880~915MHz
Band20	791~821MHz	832~862MHz
Band28	758~803MHz	703~748MHz
Band32	1452~1496MHz	/
Band66	2110~2180MHz	1710~1780MHz

5.2.5 Antenna Index

Table 36 Antenna Index Requirements（LA+EU）

Network Mode	Band	Vswr	Gain Peak	Avg.	Effi.	SAR	TRP (dBm)	TIS (dBm)
WCDMA	Band1/2/3/4/5						19	<-106
TDD-LTE	Band38	<2.5:1	>0dBi	>-4dBi	>40%	<1.6W/Kg	19	<-98
	Band39						19	<-97
	Band40						19	<-98
	Band41						19	<-98
	Band42						19	<-96
	Band43						19	<-96
	Band48						19	<-96
FDD-LTE	Band1						19	TBD
	Band2						19	<-99
	Band3						19	TBD

	Band4	19	<-99
	Band5	19	<-97
	Band7	19	<-99
	Band8	19	<-98
	Band20	19	<-97
	Band28	19	<-95
	Band32	/	TBD
	Band66	19	<-99

Table 37 Diversity Antenna Index Requirements（LA+EU）

Mode	Band	VSWR	Gain /Avg.	Efficiency	ρ	Isolation
WCDMA	Band1/2/3/4/5					
TDD-LTE	Band38					
	Band39					
	Band40					
	Band41					
	Band42					
	Band43					
	Band48	<2.5:1	>-4dBi	>25%	<0.5	<-8dB
FDD-LTE	Band1					
	Band2					
	Band3					
	Band4					
	Band5					
	Band7					

Band8
Band20
Band28
Band32
Band66

6 Electrical Characteristics

6.1 Limit Voltage Range

The limit voltage range refers to the maximum voltage range that the module power supply voltage and the digital and analog input/output interfaces can withstand. Working outside this range may cause damage to the product. The limit voltage range of SLM828G is shown in the following table.

Table 38 Limit Operating Voltage Range

Parameter	Description	Minimum	Typical	Maximum	Unit
VBAT_BB VBAT_RF	SLM828G power supply	3.3	3.8	4.2	V
	RMS average supply current	0		0.9	A
	In the instantaneous voltage drop of each time slot, the peak current of IVPH_PWR may reach 2A (power transmission per 4.6ms time slot)			400	mV
GPIO	Digital IO level supply voltage	-0.3	1.8	2.0	V
	Power supply voltage in shutdown mode	-0.25		0.25	V

6.2 Temperature Range

SLM828G module is recommended to work in the environment of -30~+75℃. At the same time, the module can work in the extended operating temperature range, and can work normally at the extended temperature, individual indicators may decrease. The storage temperature of the module refers to the normal storage temperature range of the module without power-on. The module may be damaged if the storage temperature exceeds this range.

Table 39 Module Temperature Range

Parameter	Minimum	Typical	Maximum	Unit
Working temperature	-35	+25	+75	℃
Extended operating temperature	-40		+85	℃
Storage temperature	-45		+90	℃

6.3 Electrical Characteristics of Interface Operating State

VL: logic low level;

VH: logic high level;

Table 40 Logic Levels of Ordinary Digital IO Signals

Signal	VL		VH		Unit
	Minimum	Maximum	Minimum	Minimum	
Digital Input	-0.3	0.3*Vpin_min	0.3*Vpin_max	Vpin_max	V
Digital Output	GND	0.2	Vpin_min-0.2	Vpin	V

Note: Vpin_min=1.45V, Vpin_max=2.0V (Vpin is the high level of the digital interface, Vpin=1.8V)

Table 41 Electrical Characteristics of Power Supply in Working Status

Parameter	I/O	Minimum	Typical	Maximum	Unit
VPH_PWR	PI	3.3	3.8	4.2	V
SIM_VCC	PO	1.7/2.85	1.8/3.0	1.9/3.15	V

6.4 Module power consumption range

The following is the power consumption of the SLM828G module in each working mode. For more product information, please contact us.

Table 42 Power Consumption

Product Model	Type	Mode	Transmission Rate	Channel	Average current (mA)
SLM828G	LTE	P Max	2M	Band7 20M 20850	23dbm/788
		10dBm	25M	Band7 20M 20850	10.9dbm/379
		0dBm	2M	Band7 20M 20850	-0.52dbm/283
		P Min	2M	Band7 20M 20850	-43.5dbm/274

		Idle mode	/	Band7 20M 20850	14.9mA
		Sleep mode	/	Band7 20M 20850	3.75 mA
SLM828G	WCDMA	P Max	2M	Band4 1312	24.4dbm/703
		10dBm	25M	Band4 1312	9.7dbm/269
		0dBm	2M	Band4 1312	0.1dbm/202
		P Min	2M	Band4 1312	-55.2dbm/196
		Idle mode	/	Band4 1312	9.4mA
		Sleep mode	/	Band7 20M 20850	2.804mA

6.5 Environmental Reliability Requirements

Table 43 Environmental Reliability Requirements

Test Item	Test Conditions
Cryogenic storage	1) TL (test temperature value) : -45℃ 2) To (test time) : 48h 3) Tc (sample recovery time) : 2H Note: The sample is not powered on
High temp storage	1) TH (test temperature value) : 90℃ 2) To (test time) : 48h 3) Tc (sample recovery time) : 2H Note: The sample is not powered on
Low temp running	1) TL (test temperature value) : -40℃ 2) To (test time) : 48h 3) Tc (sample recovery time) : 2H 4) U1 (atmospheric pressure) : to1 (atmospheric test time) : 12h Note: The sample is powered on
High temp running	1) TH (test temperature value) : 85℃ 2) To (test time) : 48h 3) Tc (sample recovery time) : 2H 4) U1 (normal pressure) : specification voltage to1 (atmospheric test time) : 12h Note: The sample is powered on
Temp cycle test	1) TH (test temperature value) : +85℃ 2) TL (test temperature value) : -40℃ 3) Tv (temperature change rate) : 1°/min 4) to1 (Holding time at high temperature) : 60min 5) to2 (low temperature holding time) : 60min

	6) Cycles: 24 Cycles 7) tc (sample recovery time) : 1H Note: The sample works normally when powered on
Temp step test	1) TH (test temperature value) : +85℃ 2) TL (test temperature value) : -40℃ 3) Tv (temperature change rate) : 1°/min 4) to (holding time per 10 degrees) : 60min 5) tc (sample recovery time) : 1H 6) Vcc: maximum voltage Note: The sample works normally when powered on
Alternating heat and humid test	1) TH (test temperature value) : +85℃ 2) TL (test temperature value) : -40℃ 3) D (humidity value set for test) : 95%RH 4) Tv (temperature change rate) : ≤3° /min 5) Dv (rate of change) : ≤3%RH 6) to (hold time) : 60min 7) Cycles: 10 Cycles 8) tc (sample recovery time) : 2H
Temperature impact	1) TH (test temperature value) : +90℃ 2) TL (test temperature value) : -45℃ 3) Tr (transfer time) : ≤ 30S 4) to (holding time) : 30min 5) Cycles: 25 Cycles 6) tc (sample recovery time) : 1H Note: The sample is not powered on
Sine vibration test	1) sinusoidal frequency sweep: 5~9Hz, 1.2mm; 9 ~ 2000 hz; 5m/s2 2) Frequency sweep rate: 1oct /min. Three axes, six cycles per axis.
Working impact test	1) Semi-sine wave, peak acceleration: 300 m/ s2; 2) Pulse duration: 6ms; 3) 6 directions, 5 hits in each direction.
Free drop test	1) The prototype is shut down, and the test surface is greater than or equal to 3mm thick steel plate; 2) Drop height: 1m; 3) Drop times: 1 time for each of the 6 surfaces, and 12 times for the 2 cycles
Double 85 test	1) TH (test temperature value) : +85℃ 2) RH (test set humidity value) : 85% RH 3) Tv (temperature change rate) : ≤3° /min 4) Dv (rate of change) : ≤3%RH 5) Tc1 (sample temperature stabilization time) : 500h 6) Tc2 (sample recovery time) : 2H Power-on standby test Inspection time points: 168H, 336H, 500H
Normal temperature LTEBand7 Maximum power Hang up for a	1) TL (test temperature value) : 25℃ 2) To (test time) : 12h Note: The sample is powered on and connected to the meter registered

long time	p-max

6.6 ESD Characteristic

SLM828G is a consumer terminal product. Although the ESD problem has been considered and set ESD protected in the module design. However, it is considered that the SLM828G module may also have ESD problems during transportation and secondary development. Therefore, the developer must consider the protection of the final product ESD problem, In addition to the anti-static treatment of packaging, please refer to the recommended circuit of the interface design in the document when the customer applies.

Table 44 ESD Performance parameters (temperature: 25℃, humidity :45 %)

Test Point	Contact discharge	Air discharge	Unit
VPH_PWR,GND	±5	±10	KV
Other interfaces	±0.5	±1	KV
Antenna interface	±4	±8	KV

7 Mechanical Characteristics

7.1 Mechanical Dimensions

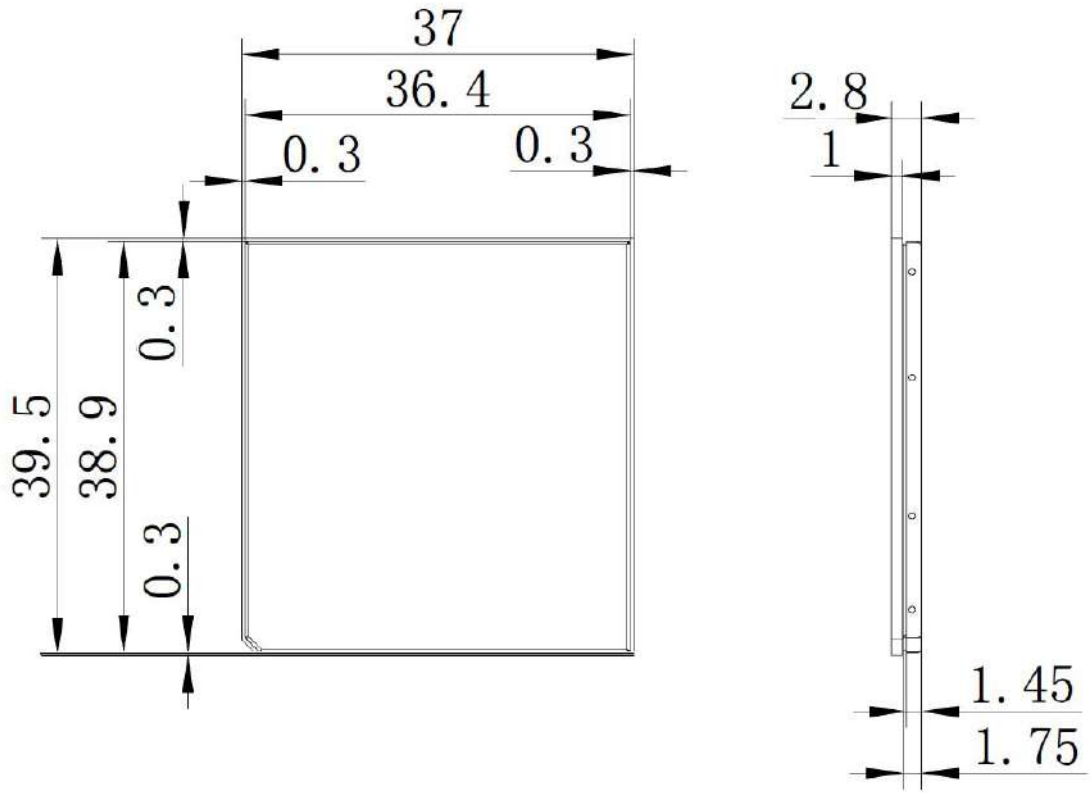

Figure 32 Top and Side View Dimensions (unit: mm)

7.2 Module Top View

Figure 33 Module Top View

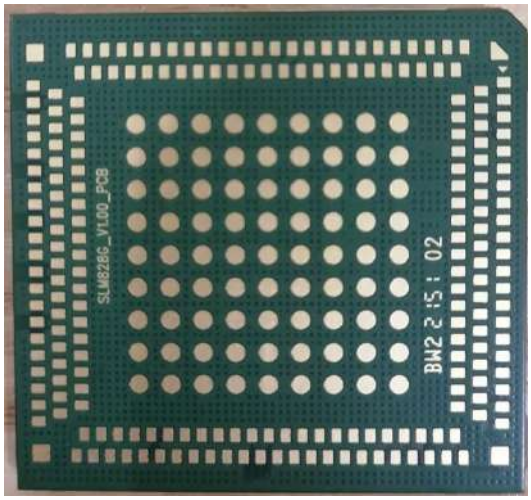

Figure 34 Module Bottom View

8 Storage and Production

8.1 Storage

The SLM828G module will be delivered in vacuum sealed bags. The storage of modules must comply with the following conditions:

1. When the ambient temperature is lower than 40℃ and the air humidity is lower than 90%, the module can be stored in a vacuum sealed bag for 12 months.
2. When the vacuum sealed bag is opened, if the following conditions are met, the module can be directly subjected to reflow soldering or other high-temperature processes:

- Module storage air humidity is less than 10%
- The ambient temperature of the module is lower than 30℃, the air humidity is lower than 60%, and the factory can complete the patch within 72 hours
- If the module is in the following conditions, it needs to be baked before placement:
- When the ambient temperature is 23°C (5°C fluctuations up and down are allowed), the humidity displayed on the humidity indicator card is greater than 10%
- When the vacuum sealed bag is opened, the ambient temperature of the module is lower than 30°C, and the air humidity is lower than 60%, but the factory failed to complete the patch within 72 hours
- When the vacuum sealed bag is opened, the module storage air humidity is greater than 10%

If the module needs to be baked, please bake it at 125°C (5°C fluctuations up and down are allowed) for 48 hours.

Note: The packaging of the module cannot withstand such a high temperature. Before baking the module, please remove the module packaging.

8.2 Production welding

The reflow temperature curve of the module is shown below.

Figure 35 Reflow temperature curve

8.3 Packaging

SLM828G is packaged with carrier band. Each volume contains 200 modules, and the following figure shows the packaging details:

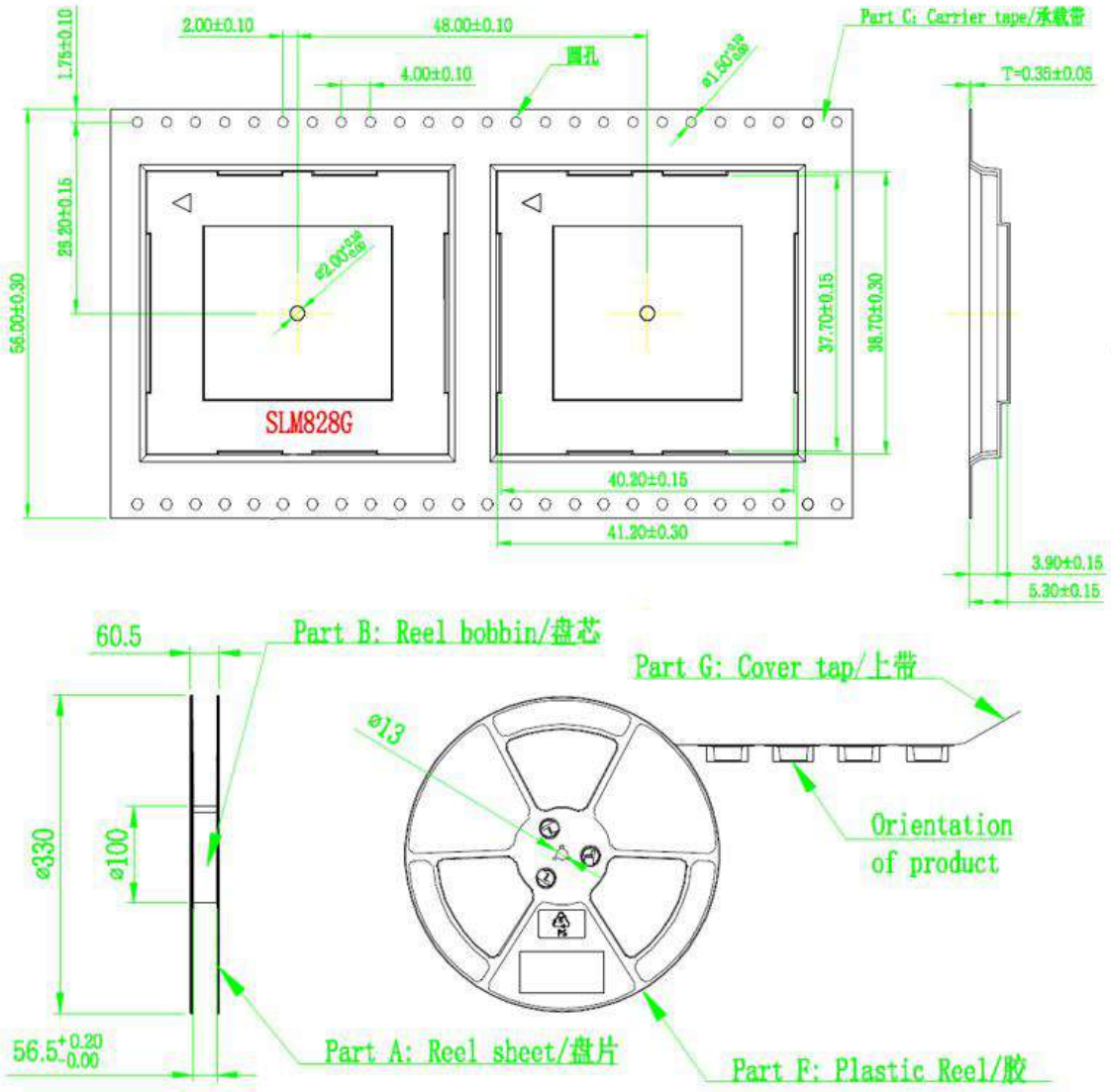

Figure 36 Package diagram

Figure 37 Packaging flow chart

9 Appendix A Reference and Abbreviations

9.1 Reference Documents

- SLM828G Module Specification
- SLM828G AT Command Set
- SLM828G_ EVB User Manual
- SLM828G Application Business Process Manual

9.2 Abbreviations

Table 45 Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
BER	Bit Error Rate
BTS	Base Transceiver Station
PCI	Peripheral Component Interconnect
CS	Circuit Switched (CS) domain
CSD	Circuit Switched Data
DCE	Data communication equipment
DTE	Data terminal equipment
DTR	Data Terminal Ready
EDGE	Enhanced Data rates for GSM Evolution
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge

FR	Frame Relay
GMSK	Gaussian Minimum Shift Keying
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HSPA	HSPA High-Speed Packet Access
HSPA+	HSPA High-Speed Packet Access+
IEC	International Electro-technical Commission
IMEI	International Mobile Equipment Identity
MEID	Mobile Equipment Identifier
I/O	Input/Output
ISO	International Standards Organization
ITU	International Telecommunications Union
bps	bits per second
LED	Light Emitting Diode
M2M	Machine to machine
MO	Mobile Originated
MT	Mobile Terminated
NTC	Negative Temperature Coefficient
PC	Personal Computer
PCB	Printed Circuit Board
PCS	Personal Cellular System

PCM	Pulse Code Modulation
PCS	Personal Communication System
PDU	Packet Data Unit
PPP	Point-to-point protocol
PS	Packet Switched
QPSK	Quadrate Phase Shift Keying
SIM	Subscriber Identity Module
TCP/IP	Transmission Control Protocol/ Internet Protocol
UART	Universal asynchronous receiver-transmitter
USIM	Universal Subscriber Identity Module
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
WCDMA	Wideband Code Division Multiple Access
TDD-LTE	Time Division Long Term Evolution
FDD-LTE	Frequency Division Duplexing Long Term Evolution
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value

V_{OL}min	Minimum Output Low Level Voltage Value

10 Appendix B GPRS Coding Schemes

Table 46 Description of Different Coding Schemes

Mode	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data rate Kb/s	9.05	13.4	15.6	21.4

15.19 Labeling requirements.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

15.21 Changes or modification warning.

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

15.105 Information to the user.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.

-Increase the separation between the equipment and receiver.

-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

-Consult the dealer or an experienced radio/TV technician for help

RF warning for Mobile device:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This module is intended for OEM integrators only. Per FCC KDB 996369 D03 OEM Manual v01 guidance, the following conditions must be strictly followed when using this certified module:

KDB 996369 D03 OEM Manual v01 rule sections:

2.2 List of applicable FCC rules

This module has been tested for compliance to FCC Part 15

2.3 Summarize the specific operational use conditions

The module is tested for standalone mobile RF exposure use condition. Any other usage conditions such as co-location with other transmitter(s) or being used in a portable condition will need a separate reassessment through a class II permissive change application or new certification.

2.4 Limited module procedures

Not application

2.5 Trace antenna designs

Not application

2.6 RF exposure considerations

This equipment complies with FCC mobile radiation exposure limits set forth for an

uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator & your body. If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.

2.7 Antennas

The following antennas have been certified for use with this module; antennas of the same type with equal or lower gain may also be used with this module. The antenna must be installed such that 20 cm can be maintained between the antenna and users.

Antenna Type:Dipole
Antenna connector:RP-SMA

Mode	Band 2	Band 4	Band 5	Band 7	Band 66	Band 38	Band 41	Band 40a
Antenna Gain (dBi)	-0.8	-1.4	-0.8	1.7	-1.4	1.9	2.4	0.2
Mode	Band 40b	Band 42	Band 43	Band 48	Band CA_38C	Band CA_41C	Band CA_42C	
Antenna Gain (dBi)	0.2	1.5	1.2	0.2	1.9	2.4	1.5	

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following: “Contains FCC ID: 2APJ4-SRM955”. The grantee's FCC ID can be used only when all FCC compliance requirements are met.

2.9 Information on test modes and additional testing requirements

This transmitter is tested in a standalone mobile RF exposure condition and any co-located or simultaneous transmission with other transmitter(s) or portable use will require a separate class II permissive change re-evaluation or new certification.

2.10 Additional testing, Part 15 Subpart B disclaimer

This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rule requirements if applicable. As long as all conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information To the End User:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual

OEM/Host manufacturer responsibilities

OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and EMF essential requirements of the FCC rules. This module must not be incorporated into any other device or system without retesting for compliance as multi-radio and combined equipment