AB1611 Datasheet

Version: 1.2

Release date: 13 March 2019

Document Revision History

Revision	Date	Description
0.1	28 February 2018	Initial version
0.2	21 December 2018	Update information
1.0	14 January 2019	Formal release version
1.1	31 January 2019	Update peripheral information Update ordering information
1.2	13 March 2019	Update package information

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1. System Overview

1.1. General description

AB1611 is an optimized single-chip solution which integrates baseband, radio, and flash memory for game controllers, mobile payments, and wearable device applications. It meets the Bluetooth Version 5.0 specification. The embedded 512KB flash is flexible and allows for custom software development, and support for nine AIOs allows for game controller applications.

1.2. Features

- BT5.0
- Embedded 32-bit MCU with 16/72MHz clock rate
- Embedded 512KB Flash
- 64KB SRAM
- 9 AIO support (12bit)
- 21 GPIO support
- 32MHz Xtal needed
- Tx power 0/9.5dBm selected
- Rx sensitivity -94dBm@1Mbps/-103dBm@125Kbps
- Integrate 1.8V switching regulator and 1.8V LDO regulator
- Ultra-low power consumption for battery enabled applications
- SPI(Master/slave) x1, UART x2, I2C x1, I2S x1, DMIC x2, PWM x8/16-bit timer, 32-bit timer x3, keyscan 16x8
- QFN 5x5 40-pin package

1.3. Applications

- SIG mesh
- Data transparent

1.4. Block diagram

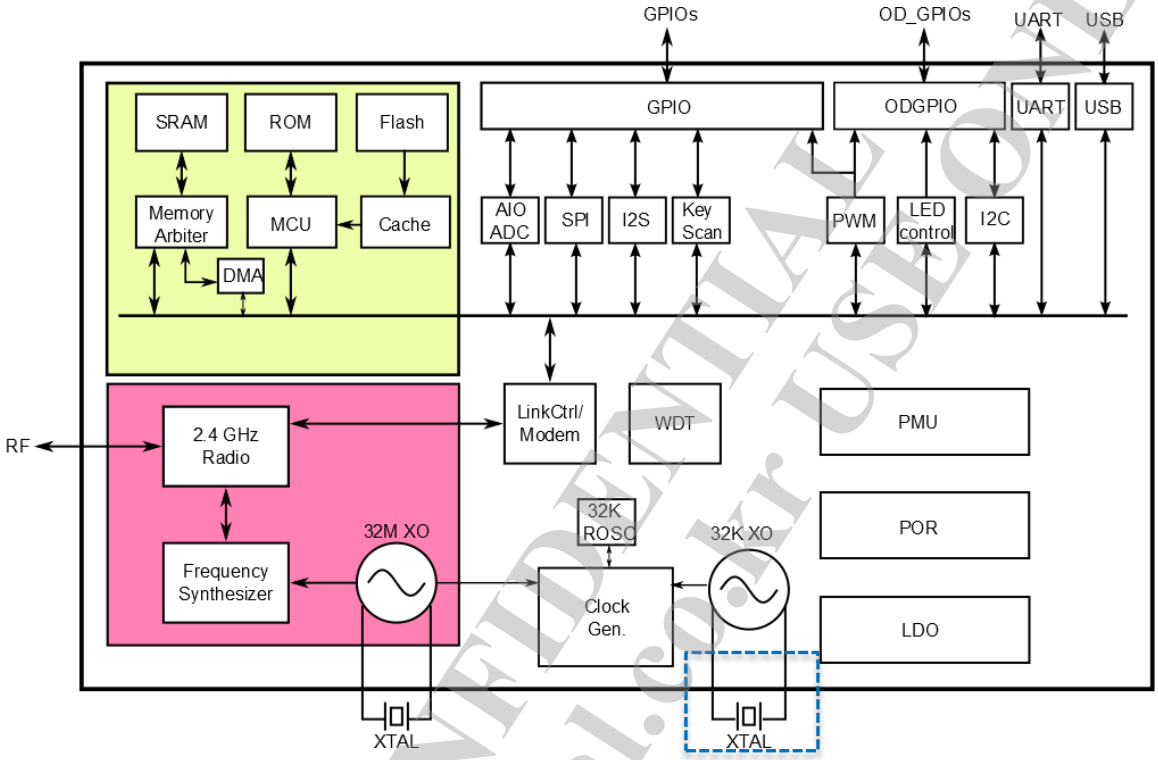


Figure 0-1 Functional block diagram (32K xo is optional)

2. Product Description

2.1. Pin definition

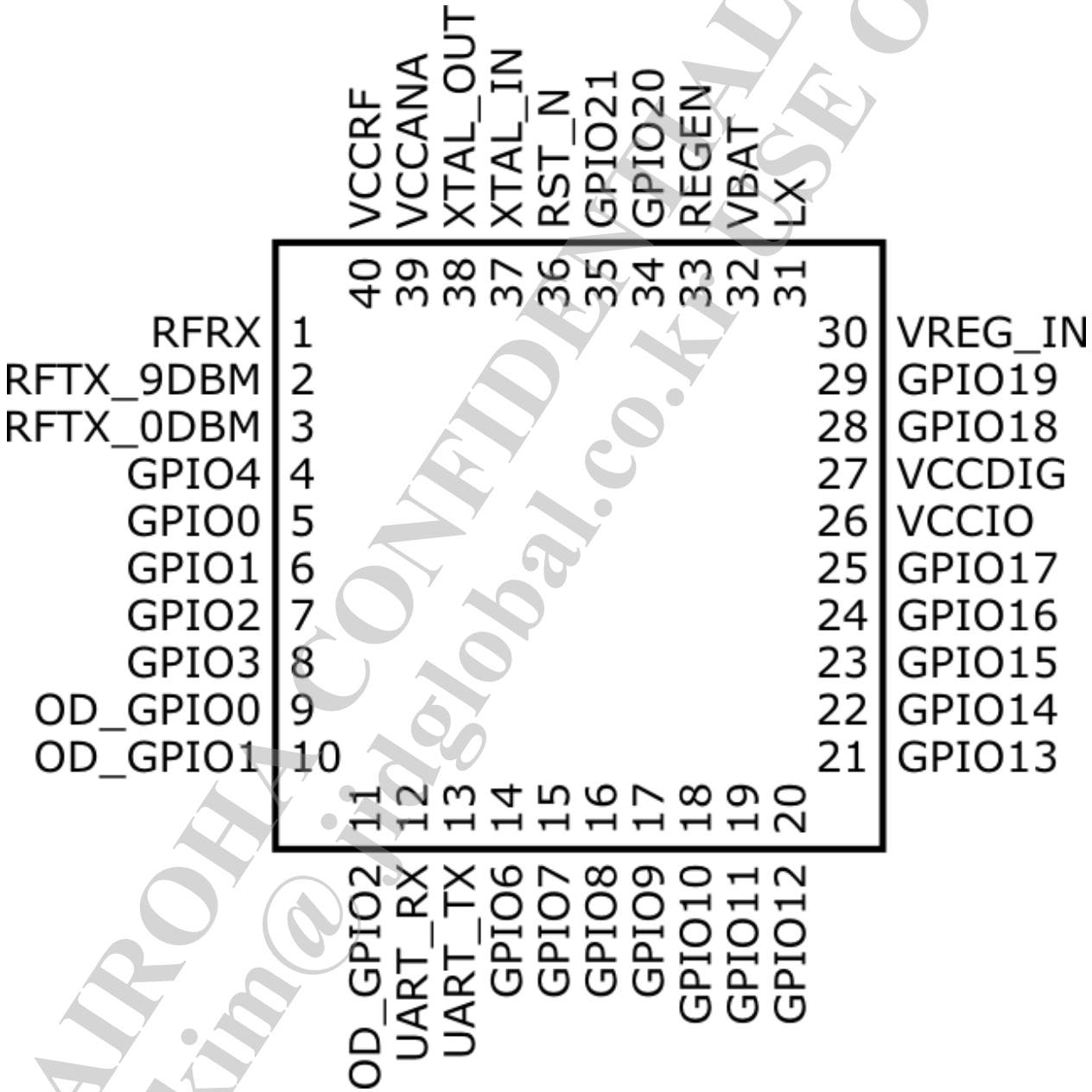


Figure 2.1-1 Pin definition

2.2. Pin description

Table 2.2-1 Pin description

PIN	SIGNAL	TYPE	DESCRIPTION	ALTERNATIVE
1	RFRX	Input, RFRX	RF input	

PIN	SIGNAL	TYPE	DESCRIPTION	ALTERNATIVE
2	RFTX_9dBm	Output, RFTX for 9.5dBm	RF output	
3	RFTX_0dBm	Output, RFTX for 0dBm	RF output	
4	GPIO4	Input/Output, Digital	Programmable IO	
5	GPIO0	Input/Output, Digital	Programmable IO	
6	GPIO1	Input/Output, Digital	Programmable IO	
7	GPIO2	Input/Output, Digital	Programmable IO	
8	GPIO3	Input/Output, Digital	Programmable IO	
9	OD_GPIO0	Input/Output, Open Drain	Programmable IO	I2C_SDA
10	OD_GPIO1	Input/Output, Open Drain	Programmable IO	I2C_SCK
11	OD_GPIO2	Input/Output, Open Drain	Programmable IO	
12	UART_RX	Input, Digital	UART RX	
13	UART_TX	Output, Digital	UART TX	
14	GPIO6	Input/Output, Digital	Programmable IO	SPI_CSN*
15	GPIO7	Input/Output, Digital	Programmable IO	SPI_MOSI*
16	GPIO8	Input/Output, Digital	Programmable IO	SPI_MISO*
17	GPIO9	Input/Output, Digital	Programmable IO	SPI_SCK*
18	GPIO10	Input/Output, Digital	Programmable IO	
19	GPIO11	Input/Output, Digital	Programmable IO	
20	GPIO12	Input/Output, Digital	Programmable IO	SPI_CSN*
21	GPIO13	Input/Output, Digital	Programmable IO	AIO SPI_MOSI*
22	GPIO14	Input/Output, Digital	Programmable IO	AIO SPI_MISO*
23	GPIO15	Input/Output, Digital	Programmable IO	AIO SPI_SCK*
24	GPIO16	Input/Output, Digital	Programmable IO	AIO
25	GPIO17	Input/Output, Digital	Programmable IO	AIO
26	VCCIO	Supply, 1.7V~3.6V	VCC for IO	
27	VCCDIG	Supply, 1.5V	VCC Digital Supply LDO1.5V output	Need Capacitor for regulated
28	GPIO18	Input/Output, Digital	Programmable IO	AIO XO32K
29	GPIO19	Input/Output, Digital	Programmable IO	AIO XO32K
30	VREG_IN	Analog	Switch regulator feedback path/ LDO output	
31	LX	Analog	Switching Regulator output	
32	VBAT	Supply, 1.9V~3.6V	VCC for LDO and Buck	
33	REGEN	input	Power key	
34	GPIO20	Input/Output, Digital	Programmable IO	AIO

PIN	SIGNAL	TYPE	DESCRIPTION	ALTERNATIVE
35	GPIO21	Input/Output, Digital	Programmable IO	AIO
36	RST_N	Input, Digital	Global reset, active low	Pull high resistor: 137K ohm
37	XTAL_IN	Analog	Crystal input	XO32M_IN
38	XTAL_OUT	Analog	Crystal output	XO32M_OUT
39	VCCANA	Supply, 1.5V	VCC for Analog	
40	VCCRF	Supply, 1.7V/1.9V	VCC for RF	

- All GPIOx(x= 0~21) is default input function and pull high with VCCIO power domain.
- UART2/I2S/DMIC/PWM can be configured via any GPIO.
- SPI can be configured via GPIO6/7/8/9 or GPIO12/13/14/15.

3. Electrical Characteristics

3.1. Absolute maximum ratings

Any stress in excess of the absolute maximum ratings listed below could cause damage to AB1611.

Table 3.1-1 Absolute maximum rating

Item	Min.	Max.	UNIT
I/O supply voltage (VCCIO)	**-0.3**	**3.6**	**V**
Analog/RF supply voltage (VCCANA, VCCRF)	**-0.3**	**2.0**	**V**
Operating temperature	**-40**	**+105**	**°C**
Storage temperature	**-65**	**+150**	**°C**

3.2. Recommended operating conditions

Table 3.2-1 Recommended operating conditions

Item	Min.	Typ.	Max.	Unit
Battery supply voltage (VBAT)	1.9		3.6	V
Analog supply voltage (VCCANA)		1.5		V
RF supply voltage (VCCRF)*		1.7/1.9		V
I/O supply voltage (VCCIO)	1.7		3.6	V

*VCCRF =1.7V for < 3.5dBm Tx power, 1.9V for > 3.5dBm Tx power

3.3. Digital terminals

Table 3.3-1 Digital terminals

Item	Min.	Typ.	Max.	Unit
Input Voltage Levels				
Input logic level low (V_{IL})	0		0.3*VCCIO	V
Input logic level high (V_{IH})	0.7*VCCIO		VCCIO+0.4	V
Output Voltage Levels (1.7V≦VCCIO≦3.6)				
Output logic level low (V_{OL}), I_O=4.0mA			0.2	V
Output logic level high (V_{OH}), I_O=-4.0mA	VCCIO-0.2			V

3.4. Reference clock

Table 3.4-1 Reference clock

Item	Min.	Typ.	Max.	Unit
Crystal Requirement				

Item	Min.	Typ.	Max.	Unit
Nominal Frequency		32		MHz
Load Capacitance		9		pF
Frequency Stability over Temperature		±20		ppm
Crystal optional				
Nominal Frequency		32.768		KHz
Load Capacitance		7		pF
Frequency Stability over Temperature		±250		ppm

3.5. Radio characteristics

3.5.1. Transmitter

Table 3.5-1 Transmitter

Item		Min.	Typ.	Max.	Unit
Maximum RF transmit power			9.5		dBm
RF power accuracy				±3	dB
In-band emissions	≥ +3MHz			-30	dBm
	+2MHz			-20	dBm
	-2MHz			-20	dBm
	≤ -3MHz			-30	dBm
Modulation characteristics	Δf1avg	225		275	KHz
	Percent of Δf2max > 185kHz	99.9		100	%
	Δf2avg/Δf1avg		1		
Center freq. deviation, Fn (n = 0,1,2,….k)		-150		+150	KHz
Freq. drift, |F0 - Fn| (n = 2,3,4,…k)		-50		+50	KHz
Initial freq. drift, |F1 - F0|		-20		+20	KHz
Max. freq. drift rate, |Fn - Fn-5| (n = 6,7,8,…k)		-20		+20	KHz/50us
Harmonics (cable mode)			-45		dBm

3.5.2. Receiver

Table 3.5-2 Receiver

Item		Min.	Typ.	Max.	Unit
Sensitivity*			-92/-94		dBm
Maximum input level		-10			dBm
Co-Channel interference, C/I				21	dB
Adjacent channel interference, C/I	F = F0+1MHz			15	dB
	F = F0-1MHz			15	dB
	F = F0+2MHz			-17	dB
	F = F0-2MHz (image+1)			-15	dB

Item		Min.	Typ.	Max.	Unit
	F = F0+3MHz			-27	dB
	F = F0-3MHz (image)			-9	dB
Intermodulation		-50			dBm
Blocking	30-2000 MHz	-30			dBm
	2003-2399 MHz	-35			dBm
	2484-2997 MHz	-35			dBm
	3000-12750 MHz	-30			dBm
PER report integrity			50		%

*0dBm for -92dBm, 9.5dBm for -94dBm

3.6. Power

3.6.1. Switching regulator

External inductor = 10uH, external capacitor = 4.7uF

Table 3.6-1 Switching regulator

Item	Condition	Min.	Typ.	Max.	Unit
Input Voltage*1		1.9	3	3.6	V
Output Voltage *2		1.5	1.7/1.9	2	V
Rated Output Current (Iout)	Normal mode		50		mA
	Retention mode			2	mA

*1: input voltage needs > 0.2V than output voltage
*2: output voltage for VCCRF

3.6.2. 1.8V LDO

External capacitor = 4.7uF

Table 3.6-2 1.8V LDO

Item	Condition	Min.	Typ.	Max.	Unit
Input Voltage		1.9	3	3.6	V
Output Voltage		1.5	1.7/1.9	2	V
Rated Output Current (Iout)	Normal mode		50		mA
	Retention mode			2	mA

*: output voltage for VCCRF

3.6.3. 1.5V LDO (for Digital/Analog)

External capacitor = 1uF

Table 3.6-3 1.5V LDO

Item	Condition	Min.	Typ.	Max.	Unit

Item	Condition	Min.	Typ.	Max.	Unit
Input Voltage		1.4	1.7	3.6	V
Output Voltage		1.1		1.6	V
Rated Output Current (Iout)	Normal mode		20		mA
	Retention mode			1	mA

3.6.4. Power fail monitor

Table 3.6-4 Power fail monitor

Item	Condition	Min.	Typ.	Max.	Unit
Programmable threshold		1.9		3.3	V
Threshold voltage tolerance		-5		+5	%
Threshold voltage hysteresis			200		mV
Current consumption			0.6		uA

3.7. Typical current consumption

Table 3.7-1 Typical current consumption

Parameter	Current (avg.)	Units	Notes
Tx current @9.5dBm	27.9	mA	
Tx current @0dBm	11.44	mA	
Rx current @1Mbps (9.5dBm)	11.8	mA	
Rx current @1Mbps (0dBm)	8.4	mA	
Sleep	4	uA	
Deep-sleep	0.6	uA	
Shutdown	0.2	uA	

Note: The current consumption values were recorded under the following conditions:
1. Buck mode, VCCIO=VBAT pin=3V
2. 9.5dBm & 3.5dBm difference due to buck voltage
3. LEDs disconnected.

3.8. AIOADC specification

Table 3.8-1 AIO ADC

Item	Condition	Min.	Typ.	Max.	Unit
Number of input channels for AIO			9		
Input voltage range		0		3.3	V
Input resistance			300		Kohm

Item	Condition	Min.	Typ.	Max.	Unit
Conversion time		1		2048	Us
ENOB	sampling rate = 3.9kHz		12		bits
Current consumption			1.5		mA
Integral nonlinearity				±2	LSB
Differential nonlinearity				±1	LSB

3.9. Analog comparator

Table 3.9-1 Analog comparator

Item	Condition	Min.	Typ.	Max.	Unit
Input voltage range		0		3.6	V
Programmable comparator ratio		1/4		1	
Input offset voltage		-50		50	mV
Current consumption			0.6		uA

3.10. Embedded flash specification

Table 3.10-1 Erase and program performance

Item	Condition	Min.	Typ.	Max.	Unit
Sector erase cycle time (4KB)			60		ms
Block erase cycle time (32KB)			0.3		s
Block erase cycle time (64KB)			0.5		s
Chip erase cycle time			4		s
Page program cycle time			0.4		s
Erase/program cycle			100,000		cycles

Note:

1. A typical erase assumes the following conditions: 25°C, typical operation voltage, and all zero patterns.
2. Under the worst conditions of 105°C and minimum operating voltage.
3. A typical program assumes the following conditions: 25°C, typical VCC, and a checkerboard pattern.

4. Function Description

4.1. Radio transceiver

The AB1611 RF transceiver is a 2.4GHz-band transceiver for Bluetooth data applications. There are three primary functions – transmitter, receiver, and synthesizer. The Baseband Processing Unit supplies the control signals for these functions.

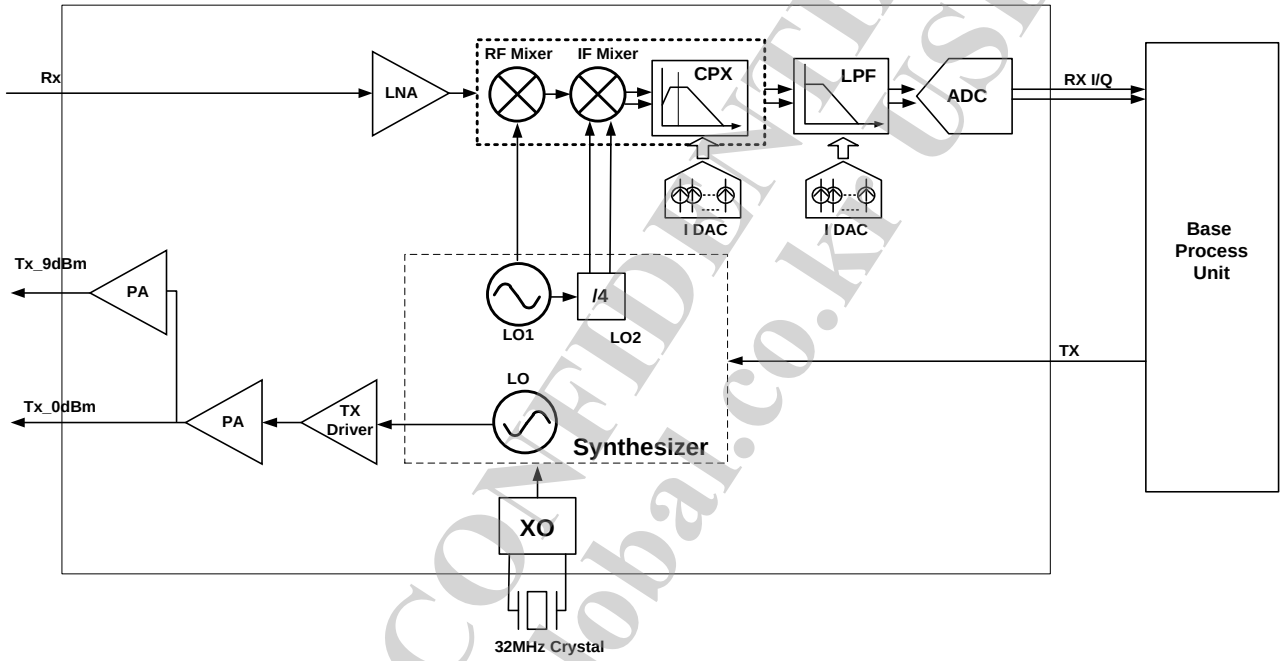


Figure 4.1-1 Radio transceiver

4.1.1. RF front end

The RX input port and TX_0dBm/Tx_9dBm output ports use different RF terminals. It can be selected by difference of TX power requirements.

4.1.2. Receiver

The AB1611 RF receiver contains two parts: An RF front-end and an IF part. The RF front-end contains an LNA and an RF mixer, and an IF Mixer. The IF part contains a complex filter (CPX) and a low-pass filter (LPF) for out-band filtering.

The LNA input uses the same RF ports as the TX output. The RX front-end gain can be adjusted, and thus reduces the probability of bit errors caused by a poor signal-to-noise ratio. The LNA is followed by an RF mixer and an IF mixer that down-converts the RF signal to the IF band.

During the IF process, the down-converted signal is filtered by CPX and LPF and is then sent to the ADC for demodulation. The 3dB bandwidth of the LPF can be adjusted via the RF registers. The RX front end provides more than 80dB gain control range.

4.1.3. Transmitter

The AB1611 RF transmitter contains a synthesizer, a TX driver, and a TXPA stage. The TX baseband signals are fed from the digital baseband and the synthesizer is used to synthesize the channel frequency and directly convert the baseband signal to an RF modulation signal. The TX driver and TX PA amplify the output power to the necessary level.

4.1.4. Synthesizer

The AB1611 features a fractional-N synthesizer with an embedded VCO and loop filter without the need for external components. It also integrates an internal crystal oscillator. Only an external 32MHz crystal is necessary.

4.2. OD_GPIO/GPIO

OD_GPIO includes OD_GPIO0/1/2. All of them are an open drain type output with a ground domain ESD, and can be used as LED drivers. OD_GPIO1 is also an engineer mode pin for downloading flash.

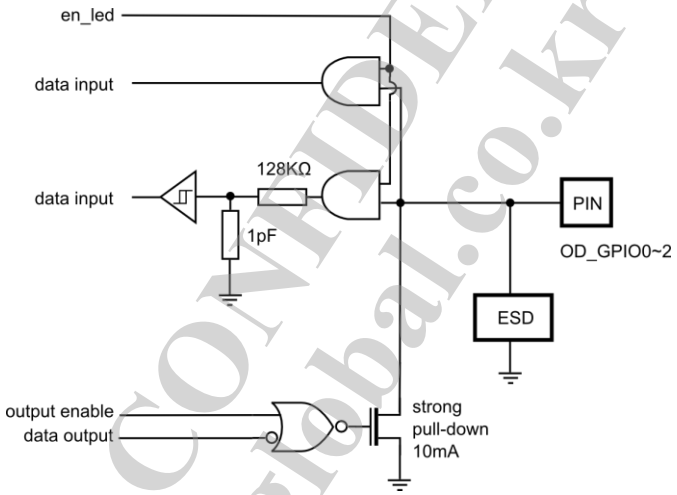


Figure 4.2-1 OD_GPIO0~2 ports

GPIO0~21 are default input pull high with VCCIO power domain, and can be configured to normal outputs. They are with VCCIO power domain ESD and ground domain ESD. Analog input mode is supported on the GPIO13~21.

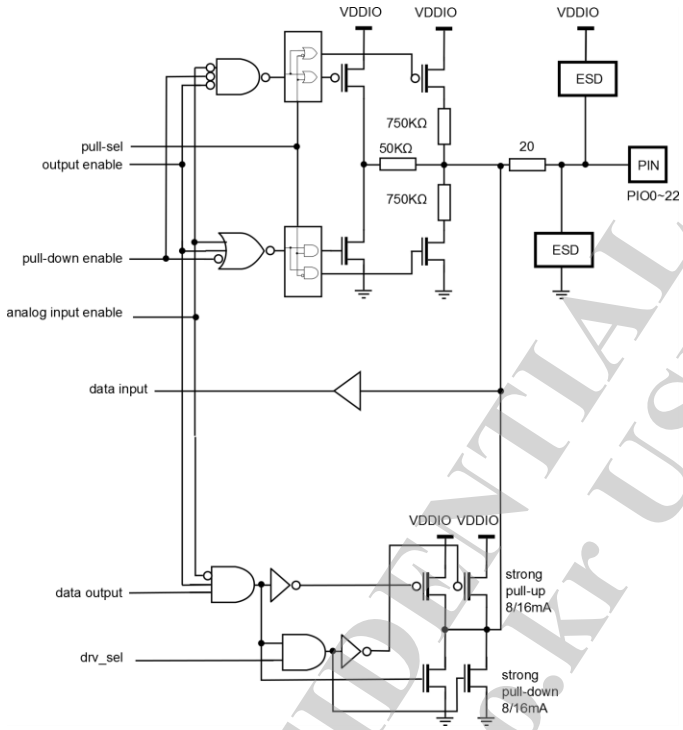


Figure 4.2-2 GPIO0~21 ports

4.3. Baseband processing unit

The baseband processing unit contains a Link Manager and a Modem to manage the Bluetooth protocol and the data transmission and reception via the RF channels.

4.3.1. Link manager

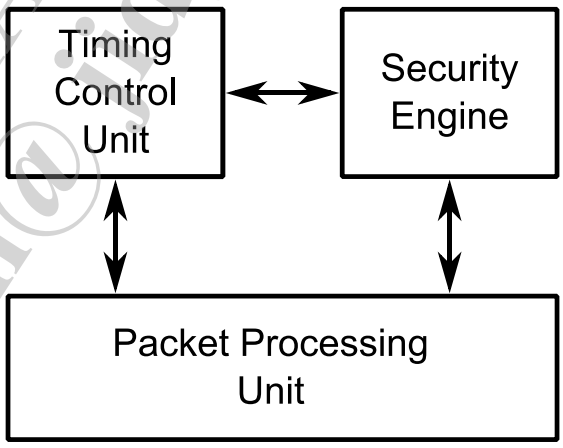


Figure 4.3-1 Link manager

The Link Manager contains a Timing Control Unit, a Security Engine, and a Packet Processing Unit. The Timing Control Unit generates and keeps the timing information for all Bluetooth links. The Packet Processing Unit assembles and disassembles Bluetooth packets and has dedicated hardware for processing data whitening and a

cyclic redundancy check (CRC). The Security Engine encrypts and decrypts the data if the encryption option is turned on. AES, P256 and SHA256 are supported.

4.3.2. Modem

The Modem only supports Bluetooth Low Energy (BLE) mode. It satisfies the requirements of the Bluetooth version 5.0 Low Energy specification.

4.4. MCU system

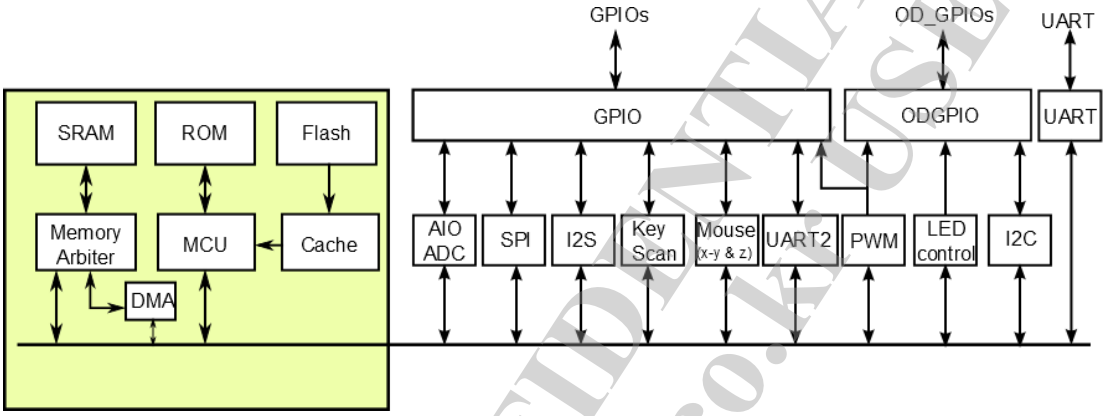


Figure 4.4-1 MCU system

The AB1611 MCU is the Andes N801-S. It is a 32-bit MCU that is optimized for performance and has enough power for embedded applications.

The MCU system has a 64K-byte boot ROM that contains the codes that are necessary during the power-up process or a system reset.

The MCU system also contains a 512K-byte flash memory that allows for the best customization for different applications.
The SRAM size in AB1611 is 64K bytes.

The MCU system also provides various peripherals, such as SPI, UART, I2C, PWM, etc.

4.5. Serial interfaces

4.5.1. SPI

The SPI communicates with external devices. The 3-wire and 4-wire mode SPI interfaces are supported. SPI_MOSI is the data I/O pin of the SPI interface when the 3-wire mode is selected.
The SPI interface is shared with GPIOs. and the mapping tables are listed below.

Table 4.5-1 SPI GPIO mapping table

GPIO pins	SPI Master/slave mode 0	SPI Master/slave mode 1
GPIO6	SPI_CSN	
GPIO7	SPI_MOSI	
GPIO8	SPI_MISO	
GPIO9	SPI_SCK	

GPIO pins	SPI Master/slave mode 0	SPI Master/slave mode 1
GPIO12		SPI_CSN
GPIO13		SPI_MOSI
GPIO14		SPI_MISO
GPIO15		SPI_SCK

The SPI Interface provides much flexibility that can fit most SPI slave devices. The polarity and phase of SCK can be both programmed and results in four combinations. The NCS to SCK delay, the SCK to NCS delay, and SCK period are also programmed. The timing relationships of SPI Interface are illustrated below.

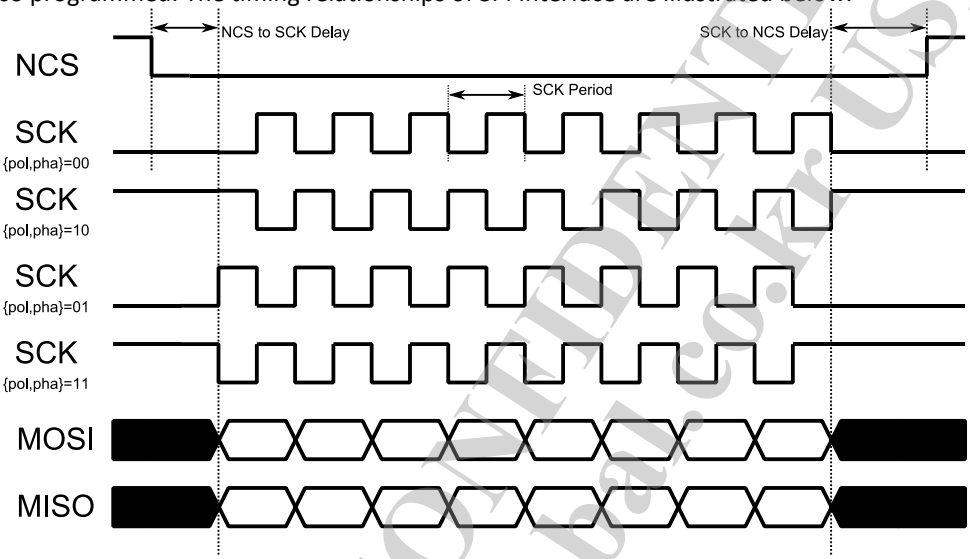


Figure 4.5-1 SPI interface timing diagram

The SPI Interface also supports multiple bytes in a single transfer. A Hold Delay can be set between each byte, as shown in the following figure.

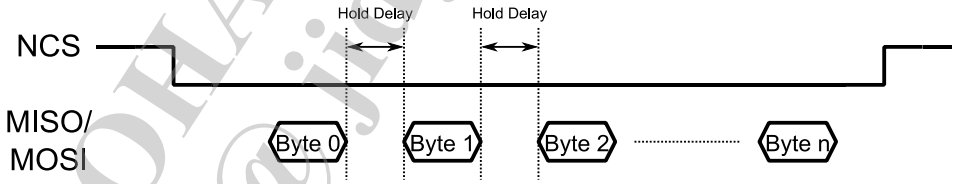


Figure 4.5-2 SPI Interface multiple bytes transfer

4.5.2. UART

AB1611 supports two UARTs. One is dedicated pin and the other can be configured via GPIOs. The UART interface supports flexible configurations as shown below. There are local FIFOs and DMA which provide high throughput serial communication. The UART also supports the hardware flow control. When it is enabled, two additional signals, UART_RTS and UART_CTS, are required. To provide the maximum flexibility, both UART_RTS and UART_CTS can be configured via any available GPIOs.

Table 4.5-2 UART configuration parameters

Configuration Parameters	Supported Values
Data Length	8 bits

Configuration Parameters	Supported Values
Flow control	Hardware RTS/CTS None
Parity	Even Odd None
Number of stop bits	1 or 2
Baud rate	1200 2400 4800 9600 19200 38400 57600 76800 115200 230400 460800 921600 1228800 2000000

Table 4.5-3 Baud rate accuracy per bit

Baud Rate	Percent Error for 12MHz clk_sys	Percent Error for 16MHz clk_sys
1200	0	0.00
2400	0	0.00
4800	0	0.01
9600	0	-0.02
19200	0	0.04
38400	0.16	-0.08
57600	0.16	-0.08
76800	0.16	0.16
115200	0.16	-0.08
230400	0.16	0.64
460800	0.16	-0.79
921600	0.16	2.12
1228800	-2.34	0.16
2000000	0	0

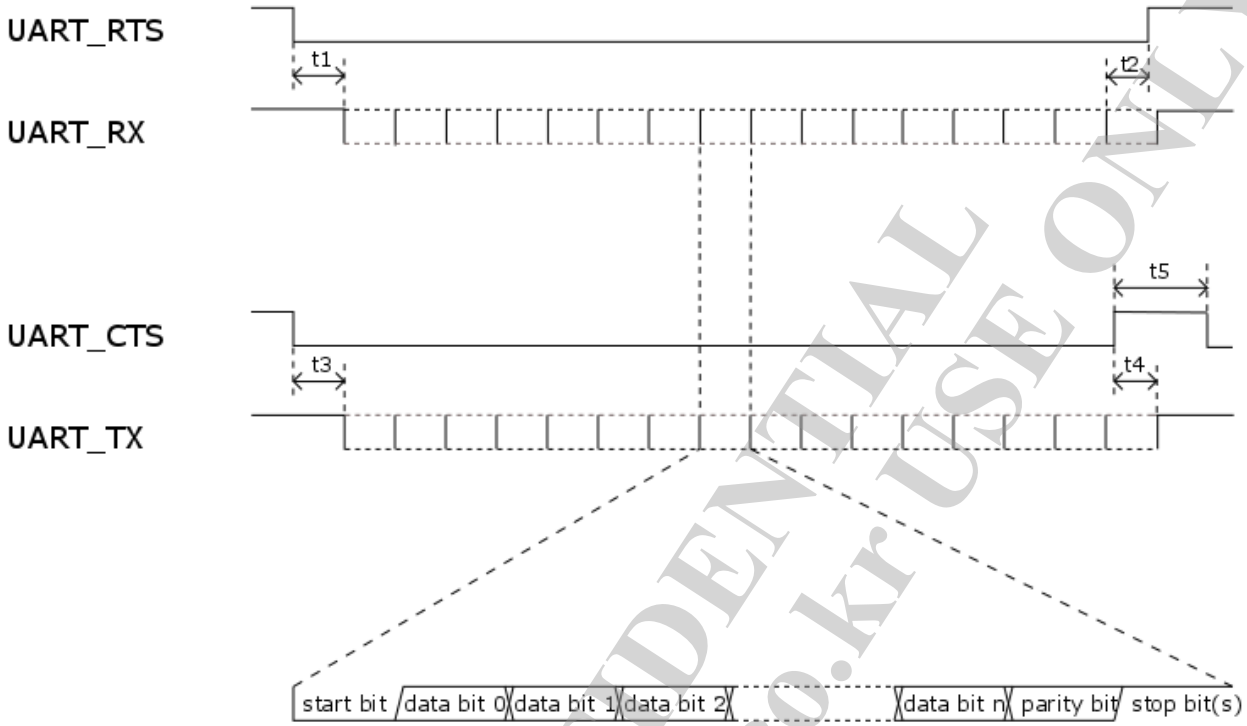


Figure 4.5-3 UART timing diagram

Table 4.5-4 Description of the symbols in Figure 4.5-3

symbol	description	min	max	unit
t1	RTS low to start receiving	0	-	us
t2	Last 2 byte received to RTS high	-	1	byte
t3	CTS low to start transmitting	0.5	1.5	bit
t4	CTS high to stop transmitting	-	1	byte
t5	CTS-high pulse width	1	-	bit

4.5.3. I2C

The I2C is a master interface. It supports 100, 400 and 800 KHz clock rates. For controlling EEPROM, a write protect (WP) signal is also supported through GPIO. The I2C interface provides several data formats and can fit various I2C peripherals. Sequential read and write are supported to improve throughputs.

The red S squares mean START or repeated START condition, while the red P squares mean STOP condition of transactions in Figure 4.5-4 ~Figure 4.5-8. The green A squares mean Acknowledge (ACK) or Not Acknowledge (NACK) bit in Figure 4.5-4 ~ Figure 4.5-8. Please note that the ACK or NACK is issued by a receiver. For example, if it's a transmission, ACK or NACK will be issued by the slave. On the other hand, if it's a requesting for data, ACK or NACK will be issued by the master. The W squares, a data bit, mean transmission(WRITE), while R squares mean requesting for data(READ) in Figure 4.5-4 ~ Figure 4.5-8. The detailed timing of red S squares, red P square, green A squares, & data bits can be seen in Figure 4.5-9.

Figure 4.5-4 I2C write transfer for 8-bit register addressing mode

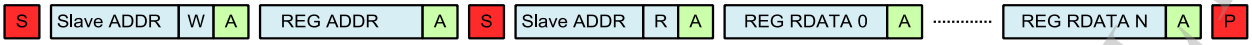


Figure 4.5-5 I2C read transfer for 8-bit register addressing mode

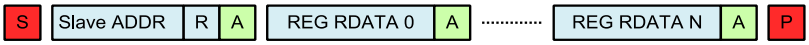


Figure 4.5-6 I2C read transfer with current address for 8-bit register addressing mode

Figure 4.5-7 I2C write transfer for 16-bit register addressing mode

Figure 4.5-8 I2C read transfer for 16-bit register addressing mode

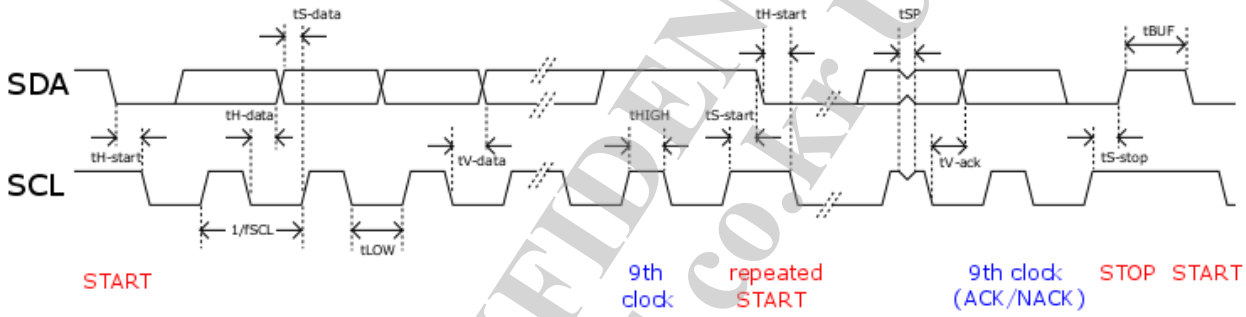


Figure 4.5-9 Definition of timing on the I2C bus

Table 4.5-5 Description of the symbols in Figure 4.5-9

symbol	description	Standard-mode		Fast-mode		Fast-mode Plus		unit
		min	max	min	max	min	max	
fSCL	SCL clock frequency	0	100	0	400	0	800	KHz
tLOW	LOW period of the SCL clock	5.00	-	1.58	-	0.67	-	us
tHIGH	HIGH period of the SCL clock	5.00	-	0.92	-	0.58	-	us
tS-start	Set-up time for a repeated START condition	6.33	-	1.33	-	0.67	-	us
tH-start	Hold time for a START or repeated START condition	1.33	-	0.50	-	0.25	-	us
tH-data	Hold time for data	0	-	0	-	0	-	us
tS-data	Set-up time for data	250	-	100	-	50	-	ns
tV-data	Data valid time	1.00	1.00	0.58	0.58	0.17	0.17	us
tV-ack	Data valid acknowledge time	1.00	1.00	0.58	0.58	0.17	0.17	us
tS-stop	Set-up time for STOP condition	1.00	8.00	0.50	2.00	0.25	1.00	us
tBUF	Bus free time between a START & STOP condition	3.33	-	0.83	-	0.42	-	us
tSP	Pulse width spikes must be suppressed by the input filer	0	83.3	0	83.3	0	83.3	ns

4.6. PWM

The PWM is designed to generate programmable pulse width of outputs. There is one timer to count cycles of the peripheral clock (PCLK) and can optionally generate interrupts or perform other actions at specified timer values based on 2 set of four match registers. The peripheral clock is provided by the system clock.

4.7. System timers

AB1611 offers three 32-bits system timers -- timer0, timer1 and timer2. They are designed to count cycles of the peripheral clock (PCLK) or an external signal, and optionally generate interrupts or perform other actions at specified timer values based on four match registers. The peripheral clock is provided by the system clock or 32KHz clock. In timer mode, there is additional reset and capture function to support measuring the pulse period of input signal (only timer0).

4.8. Key scanner

The Key Scanner is designed to optimize the power consumptions for keyboard applications. The key matrix size, both columns and rows, is programmed and the maximum matrix size is 8x16. The hardware de-bouncing and ghost key detection are also supported.

The Key Scanner scans key events autonomously in the background and stores them in the key buffers. Once key events are changed, like key-pressed or key-released, it will issue the interrupt. The microcontroller only needs to wait the interrupt and can sleep or process other tasks without key events.

4.9. I2S

The I2S is a simple serial interface for sending stereo audio bit streams. AB1611 supports three I2S modes. The timing diagrams for the three modes are shown in the following diagram.

Right Justified Mode (Supports N = 32/24/16-Bit)

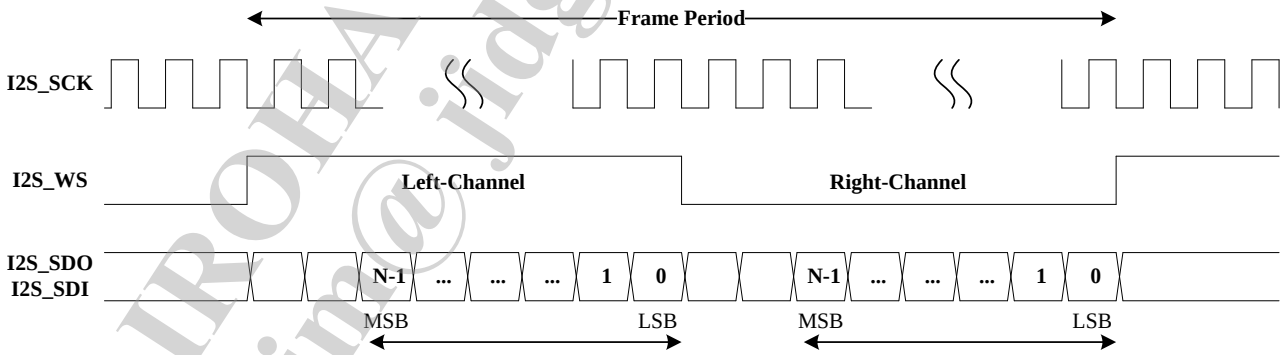


Figure 4.9-1 Right justified mode

I2S Justified Mode (Supports N = 32/24/16-Bit)

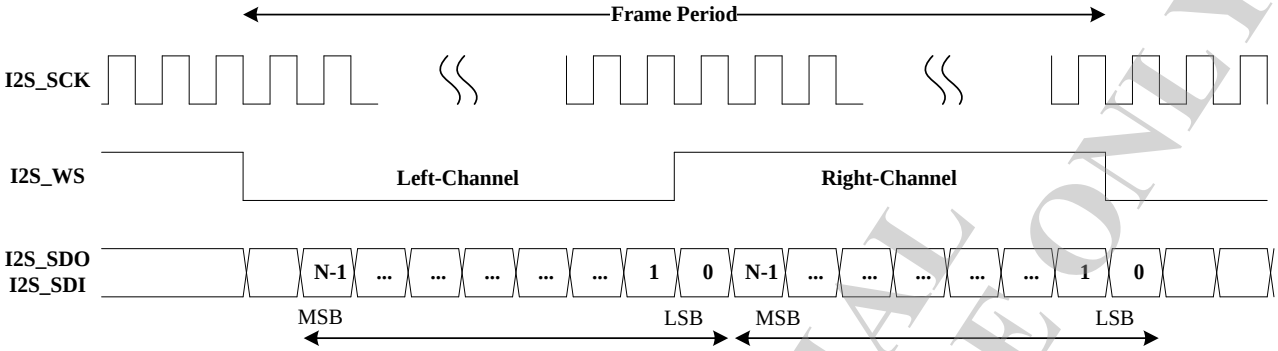


Figure 4.9-2 I2S justified mode

Left Justified Mode (Supports N = 32/24/16-Bit)

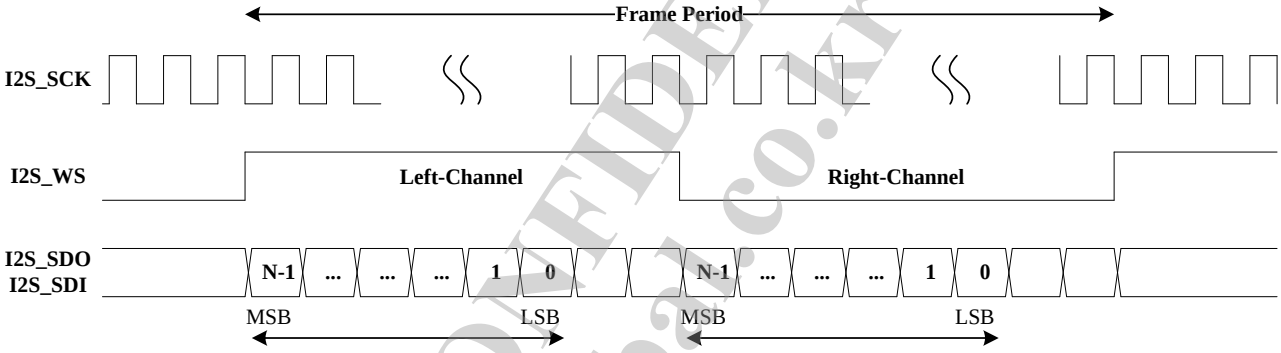


Figure 4.9-3 Left justified mode

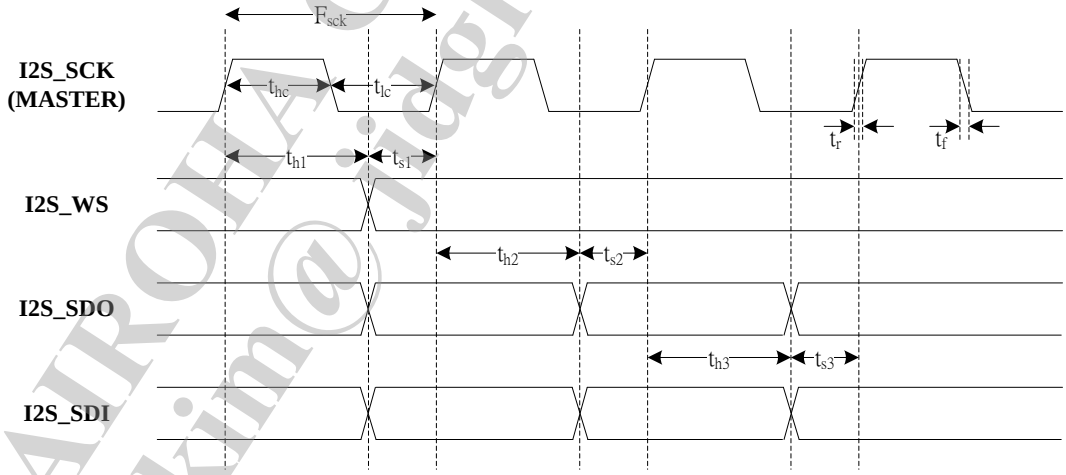


Figure 4.9-4 Timing for I2S master mode

Table 4.9-1 Description of the symbols in Figure 4.9-4

symbol	description	min
F_{sck}	Clock Frequency	16K
t_{hc}	Clock high	240ns

symbol	description	min
t_{lc}	Clock low	240ns
t_{s1}	Set-up time	20ns
t_{h1}	Hold time	20ns
t_{s2}	Set-up time	20ns
t_{h2}	Hold time	20ns
t_{s3}	Set-up time	20ns
t_{h3}	Hold time	20ns
t_r	Rise time (10% - 90%, 30pF)	8ns
t_f	Fall time (90% - 10%, 30pF)	8ns

4.10. DMIC

AB1611 supports two DMIC and two wire mode. One is one-wire mode that left and right channel use one share data pin. Another is two-wire mode that left and right channel use different data pin. Timing diagrams and interface connection are drawn below. The sample phase for each wire mode is also programmable.

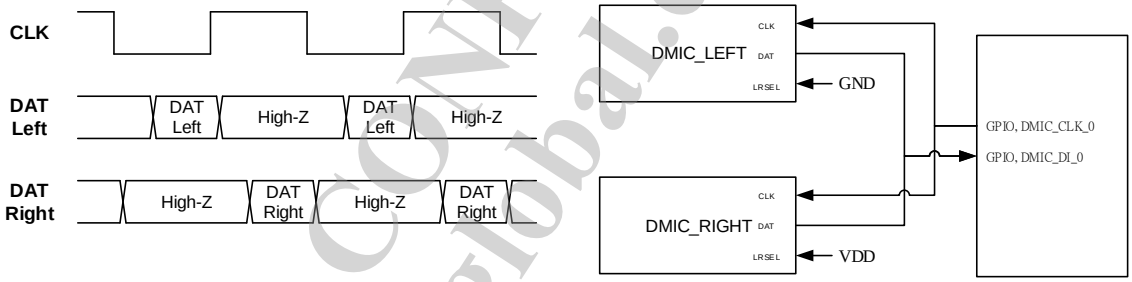


Figure 4.10-1 DMIC timing diagram and one-wire mode connection

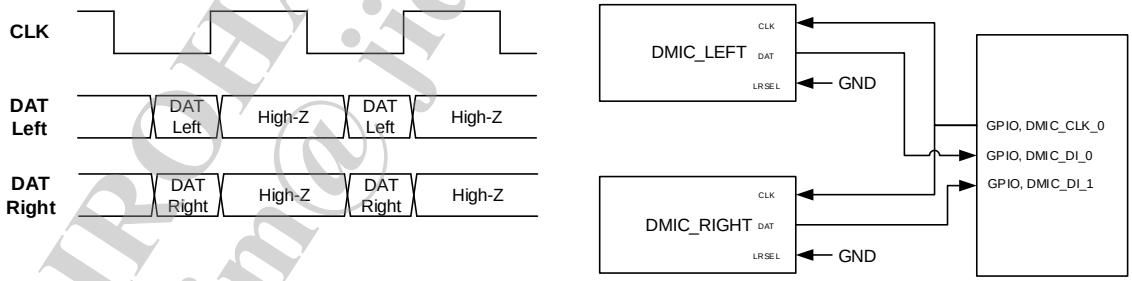


Figure 4.10-2 DMIC timing diagram and two-wire mode connection

Following table shows the phase relationship between DATA and CLK of DMIC.

Table 4.10-1 DMIC data valid and sample phase table

Wire Mode	Channel	Valid	Sample Phase	LRSEL
One-Wire	DMIC_L	Falling CLK	Rising CLK	GND
	DMIC_R	Rising CLK	Falling CLK	VDD
Two-Wire	DMIC_L	Falling CLK	Rising CLK	GND

Wire Mode	Channel	Valid	Sample Phase	LRSEL
	DMIC_R	Falling CLK	Rising CLK	GND

4.11. Power management / regulation

AB1611 integrates a Power Management Unit (PMU), Bulk regulator and LDO regulator.

4.11.1. Buck/LDO regulator

The Buck Regulators are embedded to convert VBAT to 1.8V voltage to supply AB1611. The block shows the buck circuit with LC component (L+C1). The LDO Regulators are embedded to convert VBAT to 1.8V voltage to supply AB1611 (C2). Both Buck and LDO support retention mode with lower quiescent current for low power operation.

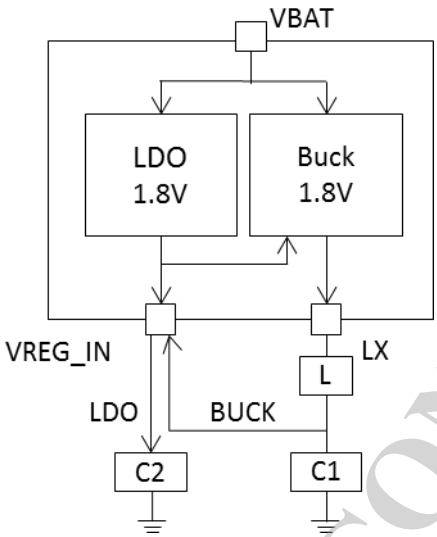


Figure 4.11-1 Buck_LDO regulator circuit

4.11.2. Power management unit

The Power Management Unit (PMU) is designed in AB1611 for the power management tasks. The PMU controls the Buck and LDO Regulator power in sequence. During general operations, MCU may get into sleep mode for power saving. During power saving, the PMU monitors the keys and wakes up the MCU if one of the keys is pressed. PMU also monitors the battery voltage and reports to MCU.

4.11.3. Power fail monitor

AB1611 provides power fail monitor function to monitor battery voltage. The threshold voltage can be calibrated by user in MP stage. When battery voltage drops below threshold voltage, it will generate an interrupt to MCU. Since the power fail monitor consumes very low current, it can be used in sleep mode or deep-sleep mode to wake up whole system.

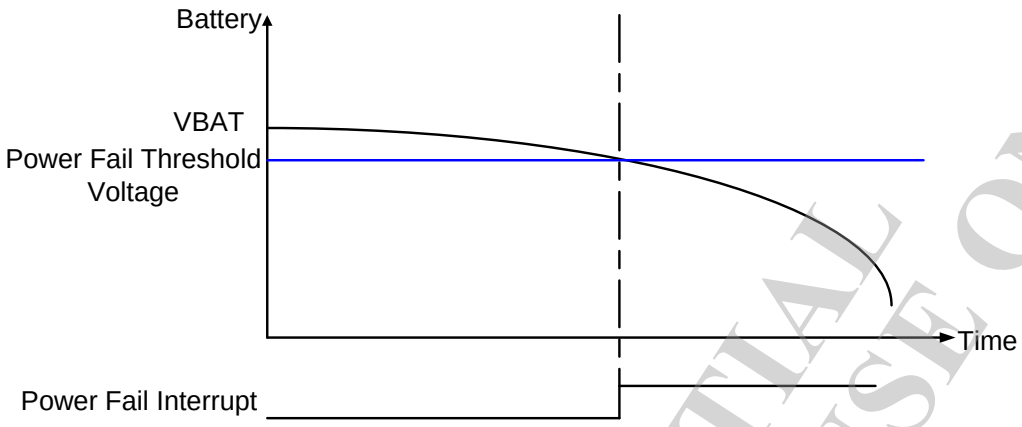


Figure 4.11-2 Power fail monitor

4.12. Analog comparator

AB1611 integrates an analog comparator which is used as a wakeup source. It allows a system wakeup to be triggered by the voltage level of a differential or single ended analog input applied through the port pins. The comparator has very low current consumption, and is operational in the register retention mode.

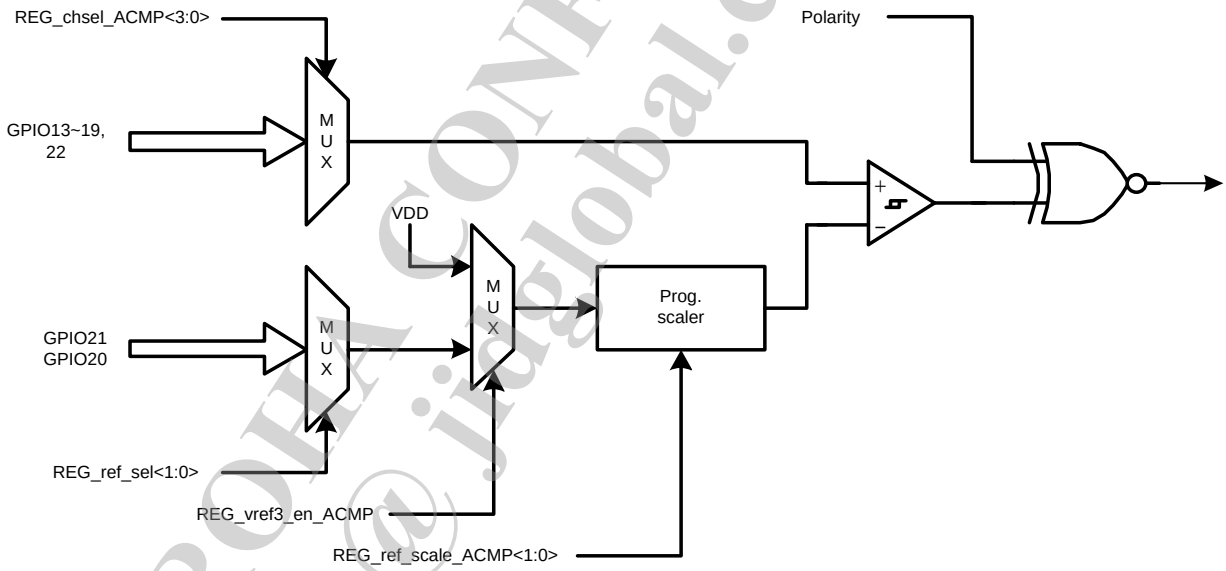


Figure 4.12-1 Analog comparator

One out of up to 8 different port pins may be used to apply a voltage to the non-inverting comparator input. The inverting comparator input can be connected to 25%, 50%, 75% or 100% of either VDD or an arbitrary reference from GPIO20 or GPIO21.

The polarity of the comparator output is programmable. The default behavior is that a wakeup is triggered when the non-inverting input rises above the inverting input.

The comparator has a switched capacitor input clocked at 32kHz. It is recommended to connect a 330pF bypass capacitor between the analog input pin(s) and VSS. This reduces voltage transients introduced by the switching.

The capacitor may be omitted if the signal source has an output resistance smaller than 100kΩ. The input bias current of the comparator is typically below 100nA.

4.13. Clock generation

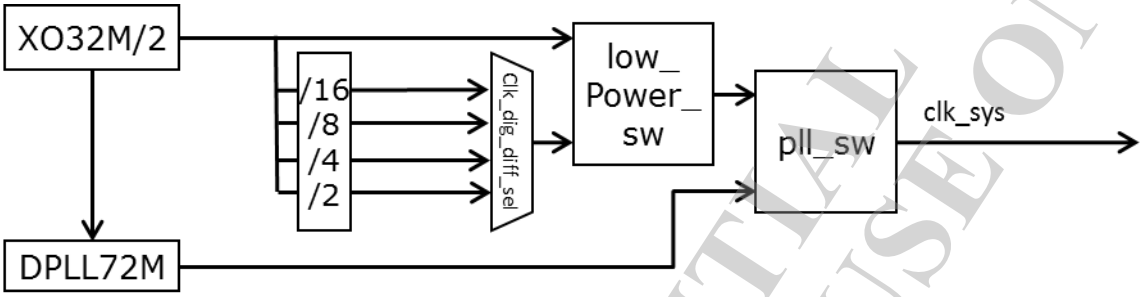


Figure 4.13-1 Clock generation block diagram

The clock source of 16MHz in the MCU platform is from Xtal32M divided by 2. Upon power-on or chip reset, AB1611 uses 16MHz as the clock source. A 72MHz PLL in the chip is provided to generate faster system clock for MCU platform, and slower clocks such as 1MHz, 2MHz, 4MHz and 8MHz divided from 16MHz are also selectable for power reduction. The clock source of 32KHz selected from ROSC32K or xtal32.768K is used to provide slow clock source to key scanner, mouse controller, PMU and LED.

4.14. Power control

AB1611 supports various power control features for power saving purpose. There are four special power modes:

- Active mode
- Sleep mode
- Deep-sleep mode
- Shutdown mode

In different power mode, power management unit (PMU) controls Buck/LDO/clocks to reduce power consumption automatically, as shown in Table 4.14-1 Operating power mode.

Table 4.14-1 Operating power mode

Power mode	Buck/LDO	System clock	32KHz clock	Wake-up pins
Active	ON	ON	ON	-
Sleep	Retention	OFF	ON	All input pins
Deep-sleep	Retention	OFF	ON/OFF	All input pins
shutdown	OFF	OFF	OFF	REGEN

REGEN Pin connects from GND to VBAT for power on. In active mode, MCU clock rate may also can be controlled by changing clock sources, bypassing PLL, or altering clock divider value. Sleep mode and deep-sleep mode are two types of low power modes supported by AB1611. In low power mode, system clock is stopped and Buck/LDO enter retention mode to reduce leakage current. All input pins serve as external wake-up pins to PMU to wake up chip from low power mode. For further power reduction, most of digital circuit is shut off and 32KHz clock is also selectable to be turned off in deep-sleep mode. The IC is power off in shutdown mode.

4.15. AIO ADC

AB1611 integrates an AIO ADC which is used to sense the general purpose input (GPIO) and converted to digitized data. It maximum allows 10 AIO input ideally, but 9 due to the package constraint. A simple input configuration as shown in Figure 4.15-1 AIO input configuration of ADC. It consists of programmable gain amplifier (PGA) and ADC circuit as shown in **Error! Reference source not found.**. The selected MUX output is related to input channel controlled by aio_ch_en<22:13>. The default operation mode sense the one GPIO input once when AIOADC activated which is called single AIO mode. One PGA input connects to measured GPIO, the other input connects to internal common voltage (VCM).

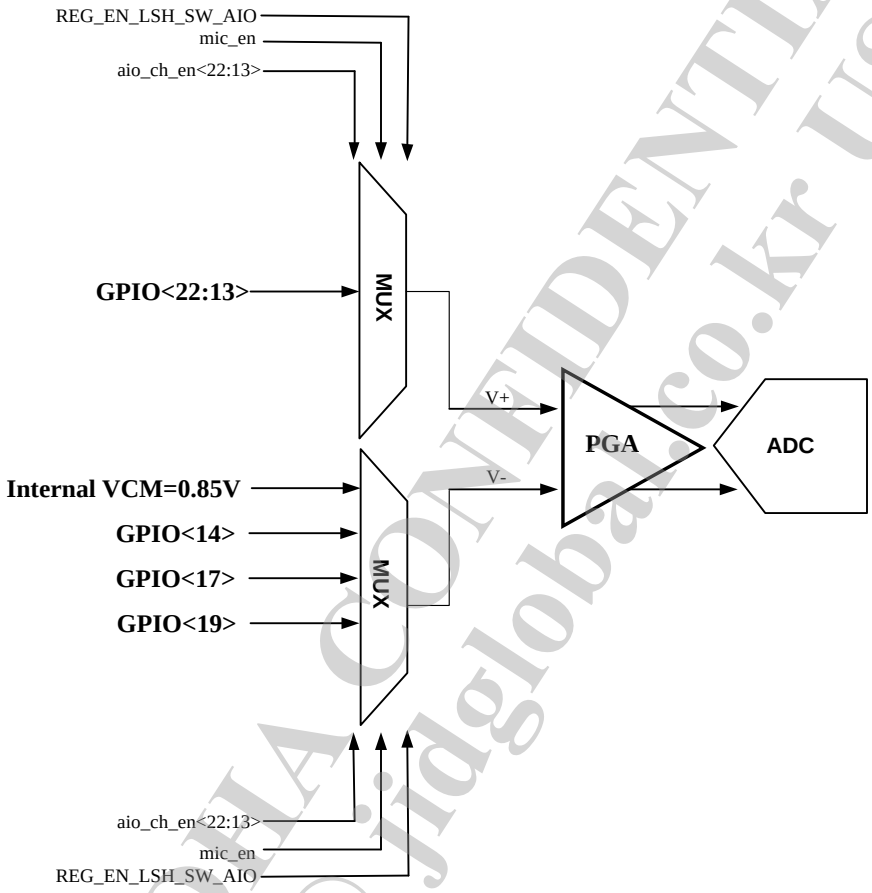


Figure 4.15-1 AIO input configuration of ADC

Another operation mode senses the two GPIO different inputs once when AIOADC activated which is called differential AIO mode. When the control REG_EN_LSH_SW_AIO is 1, three pairs of GPIO13/GPIO14, GPIO16/GPIO17, and GPIO18/GPIO19 inputs operate in differential AIO mode. ADC senses the two GPIO from input MUX and calculates the difference. But others GPIO still operation in single AIO mode only. The related specification is shown in Table 3.8-1.

5. Software

5.1. Protocol stack

The Airoha AB1611 includes the complete BLE stack/profiles. The BLE stack includes ATT, GATT, Security Manager and standard based services/profiles. In summary, AB1611 enables customers to support BT 5.0 data communication in their products very easily. Figure 5.1-1 shows the AB1611 software architecture.

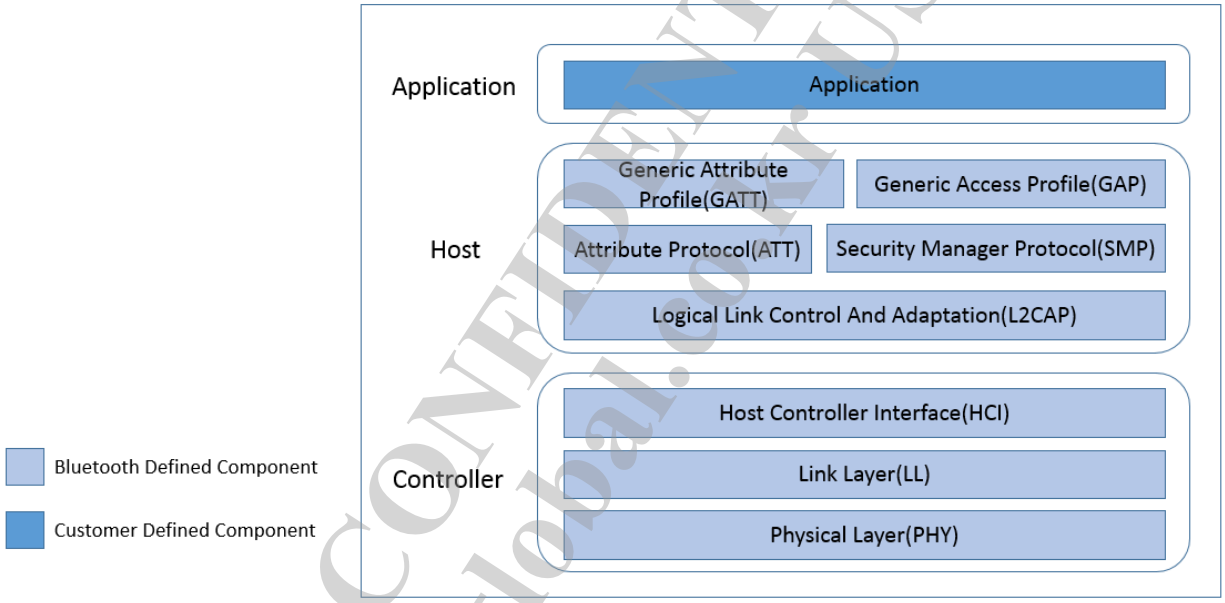


Figure 5.1-1 AB1611 Software Stack

5.2. Software development environment

The AB1611 software architecture allows customers to develop their own software as the application layer very easily. A plug-in architecture allows the customers to process data packets at many different software layers so that very flexible customization can be achieved. Airoha provides all of the necessary source codes, documentations and project files to customers enabling a fast development cycle for customers to create added value and differentiations for their end products.

For BT 5.0, Airoha provides a very simple way to define any proprietary GATT profiles either by C code or by GUI. Thus developing software for AB1611 is easy and flexible.

5.3. Test and configuration tools

Two tools are provided for manufacture testing and configuration as shown below:

- AB1611 configuration tool
  - AB1611 configuration tool provides a GUI for customers to define their own proprietary GATT

profiles. Only minimum coding, such as data processing call back function, is required to achieve a GATT profile.

- AB1611 Mass-Production tool
    - AB1611 Mass-Production tool is used during customer production stage and it provides the capability for downloading/verifying flash memory, testing RF performance, ADC calibration, and updating Bluetooth device address. It works with the Airoha provided Test Control Board (TCB) hardware. The Mass-Production tool greatly improves the test and verification efficiency in manufacturing stage.

6. Ordering and package Information

6.1. Ordering information

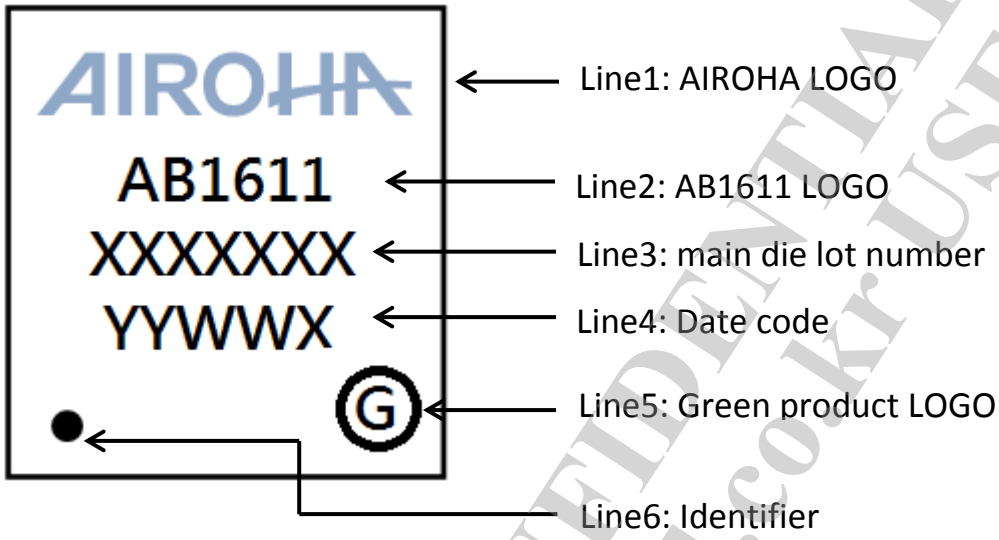
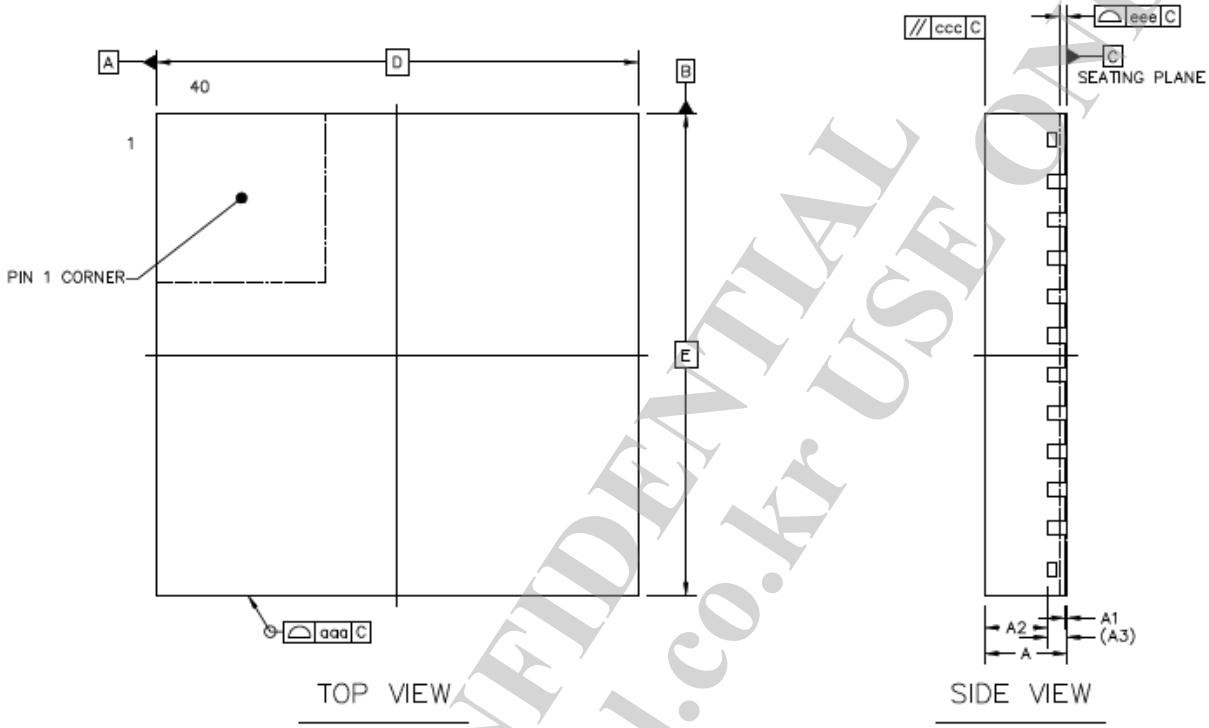


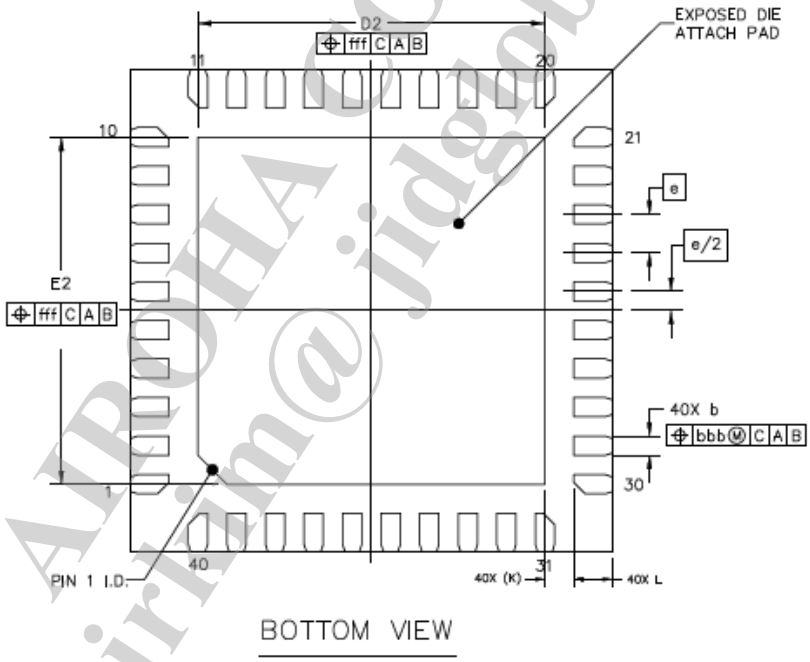
Figure 6.1-1. Mass production top marking of AB1611 devices

Table 6.1-1. Ordering information

Product number	Package	Description
AB1611N	QFN	5mm*5mm, 40-pin, 0.4mm pitch

6.2. Package information





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	3.5	3.6	3.7
	Y	E2	3.5	3.6	3.7
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

Figure 6.2-1 Package Information