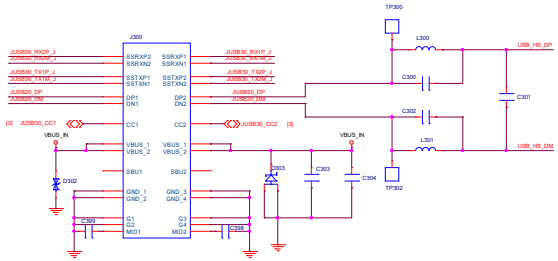
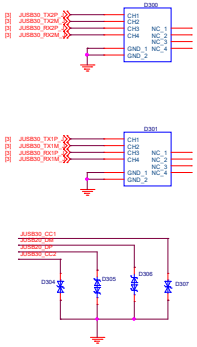
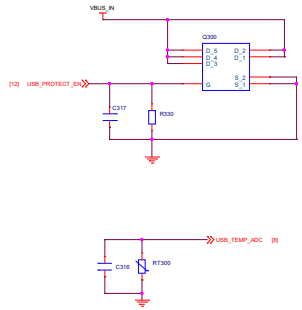
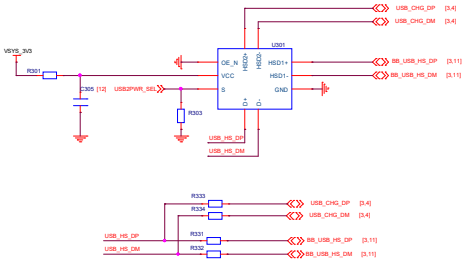
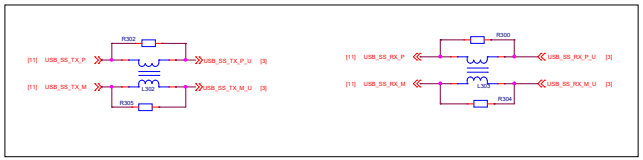
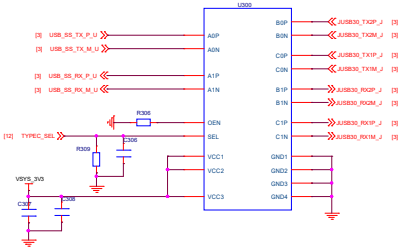

J300
TP300
L300
C300
C302
L301
TP302
USB_HS_DP
USB_HS_DM
C301
VBUS_IN
D302
D303
C303
C304
C309
C308

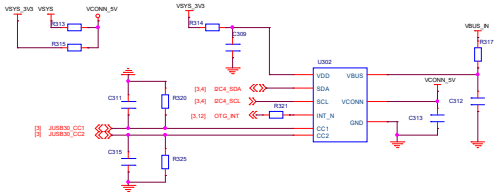

D300
D301
D304
D305
D306
D307

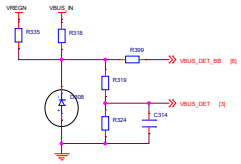

VBUS_IN
G300
C317
R330
USB_TEMP_ADC
C316
RT300

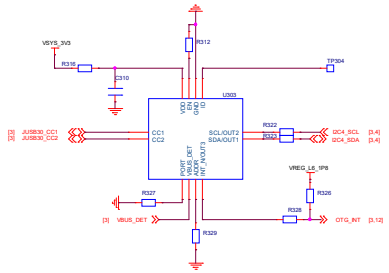

U301
R301
C305
R303
R333
R334
R331
R332

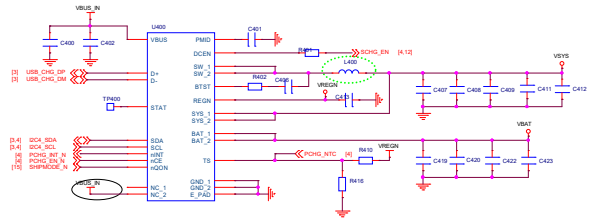

R302
L302
R305
R300
L303
R304

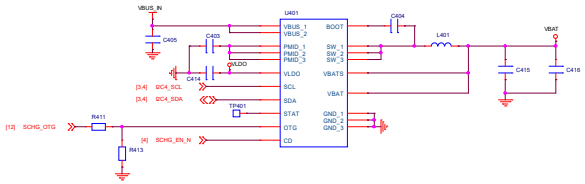

U300
R306
C306
R309
C307
C308


U302
R313
R315
R314
C309
C311
R320
R321
C315
R325
C312
C313
R317

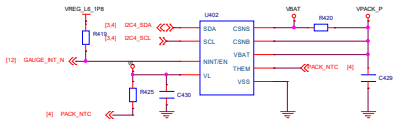

R335
R318
R309
R319
R324
C314

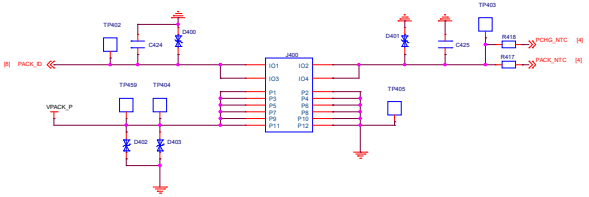

U303
R312
R316
C310
TP304
R322
R323
R327
R329
R326
R328

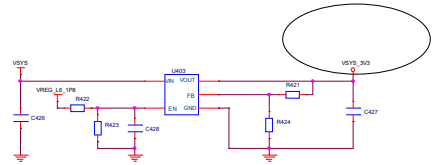

VBUS_IN
U400
C400
C402
C401
VBUS
PMID
DCEN
SW_1
SW_2
BTST
REGN
SYS_1
SYS_2
BAT_1
BAT_2
TS
GND_1
GND_2
E_PAD
R401
SCHG_EN
[4,12]
L400
VSYS
[3] USB_CHG_DP
[3] USB_CHG_DM
D+
D-
R402
C405
VREGN
C407
C408
C409
C411
C412
TP400
STAT
VBAT
[3,4] I2C4_SDA
[3,4] I2C4_SCL
[4] PCHG_INT_N
[4] PCHG_EN_N
[15] SHIPMODE_N
SDA
SCL
nINT
nCE
nQON
PCHG_NTC
[4]
R415
R416
C419
C420
C422
C423
VBUS_IN
NC_1
NC_2

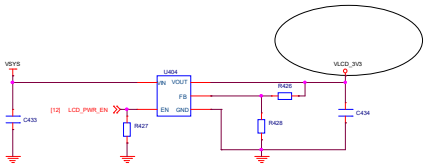

VBUS_IN
C405
U401
VBUS_1
VBUS_2
PMID_1
PMID_2
PMID_3
VLDO
SCL
SDA
STAT
OTG
CD
BOOT
SW_1
SW_2
SW_3
VBATS
VBAT
GND_1
GND_2
GND_3
C403
VLDO
C414
[3,4] I2C4_SCL
[3,4] I2C4_SDA
TP401
C404
L401
C415
C416
[12] SCHG_OTG
R411
[4] SCHG_EN_N
R413

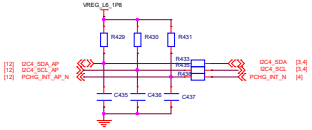

VREGN
R403
PCHG_EN_N
[4]
R406
Q400
R408
C417
[12] PCHG_EN
R414
VREGN
VLDO
R404
R405
SCHG_EN_N
[4]
R407
Q401
R409
C418
[4,12] SCHG_EN
R415

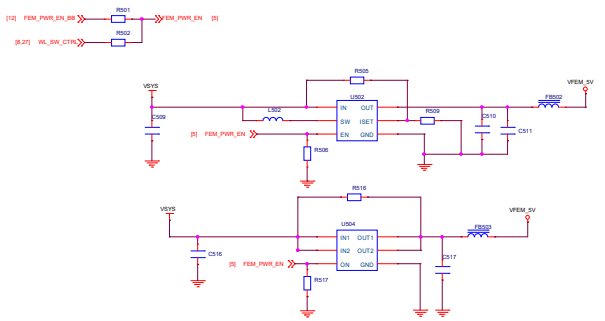

VREG_L6_1P8
[3,4] I2C4_SDA
[3,4] I2C4_SCL
R419
U402
SDA
SCL
NINT/EN
VL
CSNS
CSNB
VBAT
THEM
VSS
VBAT
R420
VPACK_P
[12] GAUGE_INT_N
R425
C430
VPACK_NTC
[4]
[4] PACK_NTC
C429

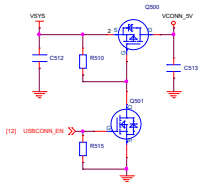

TP402
C424
D400
[8] PACK_ID
J400
IO1
IO3
P1
P3
P5
P7
P9
P11
IO2
IO4
P2
P4
P6
P8
P10
P12
D401
C425
TP403
R418
PCHG_NTC
[4]
R417
PACK_NTC
[4]
VPACK_P
TP459
TP404
TP405
D402
D403

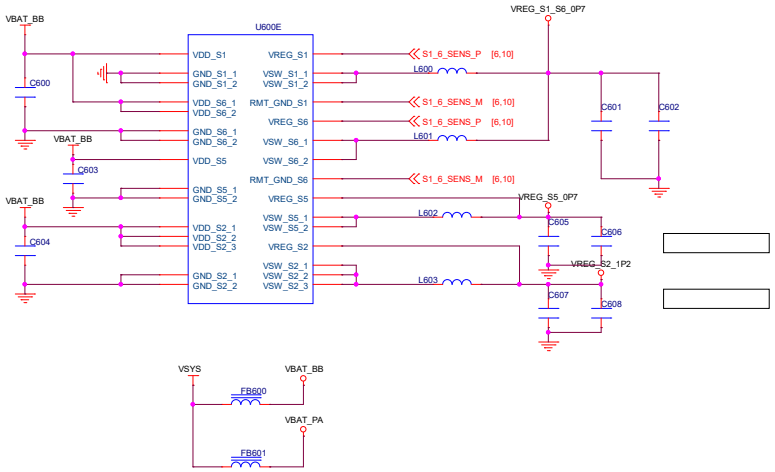

VSYS
VREG_L6_1P8
C426
U403
VIN
VOUT
FB
EN
GND
R422
R423
C428
VSYS_3V3
R421
R424
C427

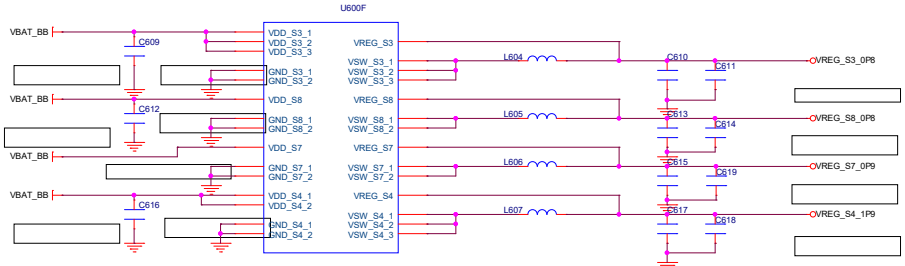

VSYS
C433
U404
VIN
VOUT
FB
EN
GND
[12] LCD_PWR_EN
R427
R426
R428
VLCD_3V3
C434

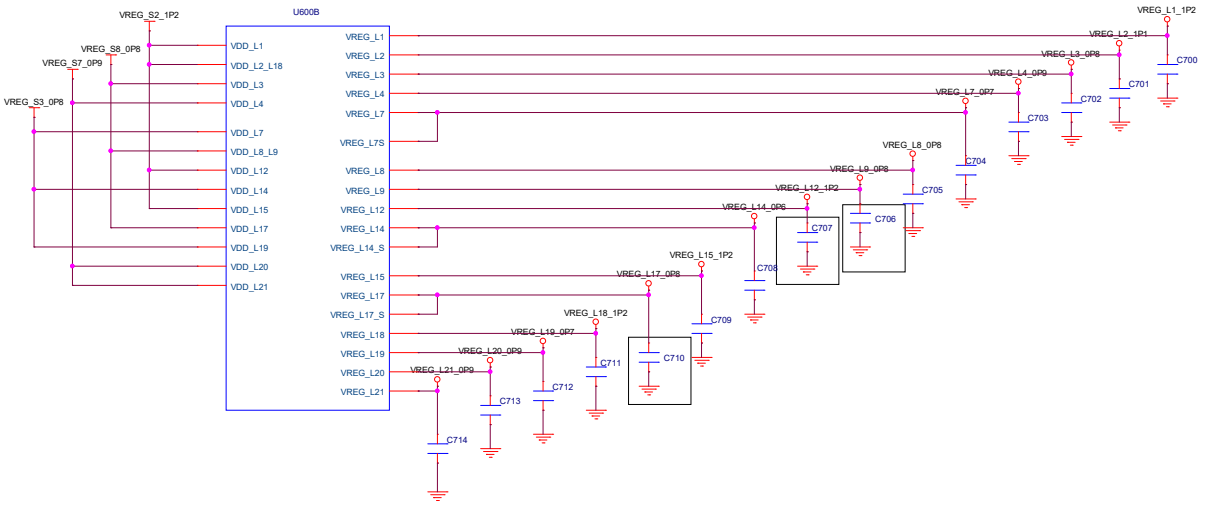

VREG_L6_1P8
R429
R430
R431
[12] I2C4_SDA_AP
[12] I2C4_SCL_AP
[12] PCHG_INT_AP_N
R432
R433
R434
I2C4_SDA
[3,4]
I2C4_SCL
[3,4]
PCHG_INT_N
[4]
C435
C436
C437

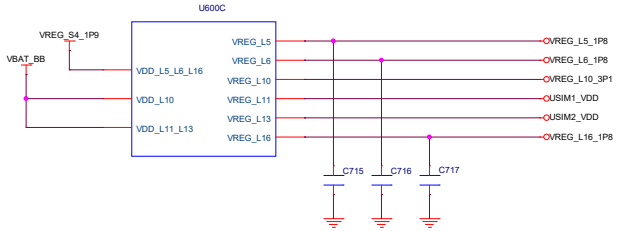

R501
R502
FEM_PWR_EN_BB
WL_SW_CTRL
FEM_PWR_EN
R505
U502
IN
OUT
SW
ISET
EN
GND
L502
R509
C509
C510
C511
FB502
VSYS
VFEM_5V
R506
R516
U504
IN1
OUT1
IN2
OUT2
ON
GND
C516
C517
R517
FB503

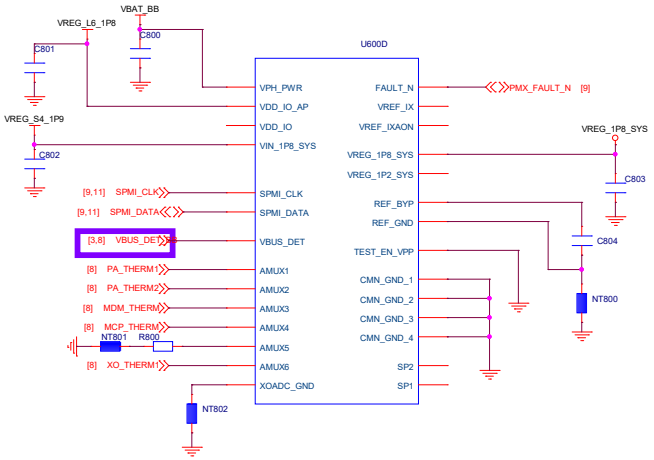

Q500
Q501
VSYS
VCONN_5V
C512
R510
C513
R515
USBCONN_EN

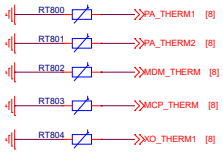

U600E
VBAT_BB
VREG_S1_S6_0P7
VDD_S1
VREG_S1
GND_S1_1
GND_S1_2
VSW_S1_1
VSW_S1_2
VDD_S6_1
VDD_S6_2
RMT_GND_S1
VREG_S6
GND_S6_1
GND_S6_2
VSW_S6_1
VSW_S6_2
VDD_S5
RMT_GND_S6
GND_S5_1
GND_S5_2
VREG_S5
VSW_S5_1
VSW_S5_2
VDD_S2_1
VDD_S2_2
VDD_S2_3
VREG_S2
VSW_S2_1
VSW_S2_2
VSW_S2_3
GND_S2_1
GND_S2_2
S1_6_SENS_P [6,10]
S1_6_SENS_M [6,10]
S1_6_SENS_P [6,10]
S1_6_SENS_M [6,10]
L600
L601
L602
L603
C600
C601
C602
C603
C604
C605
C606
C607
C608
VREG_S5_0P7
VREG_S2_1P2
VSYS
VBAT_BB
FB600
VBAT_PA
FB601

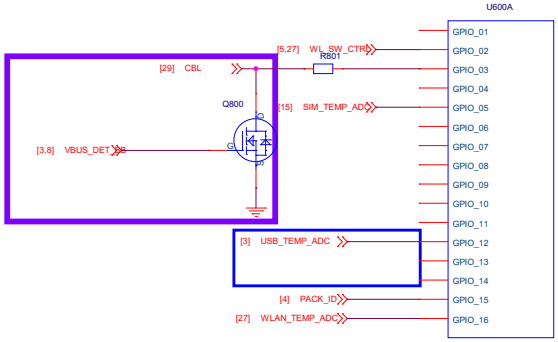

U600F
VBAT_BB
VDD_S3_1
VDD_S3_2
VDD_S3_3
VREG_S3
GND_S3_1
GND_S3_2
VSW_S3_1
VSW_S3_2
VSW_S3_3
VDD_S8
VREG_S8
GND_S8_1
GND_S8_2
VSW_S8_1
VSW_S8_2
VDD_S7
VREG_S7
GND_S7_1
GND_S7_2
VSW_S7_1
VSW_S7_2
VDD_S4_1
VDD_S4_2
VREG_S4
GND_S4_1
GND_S4_2
VSW_S4_1
VSW_S4_2
VSW_S4_3
L604
L605
L606
L607
C609
C610
C611
C612
C613
C614
C615
C616
C617
C618
C619
VREG_S3_0P8
VREG_S8_0P8
VREG_S7_0P9
VREG_S4_1P9

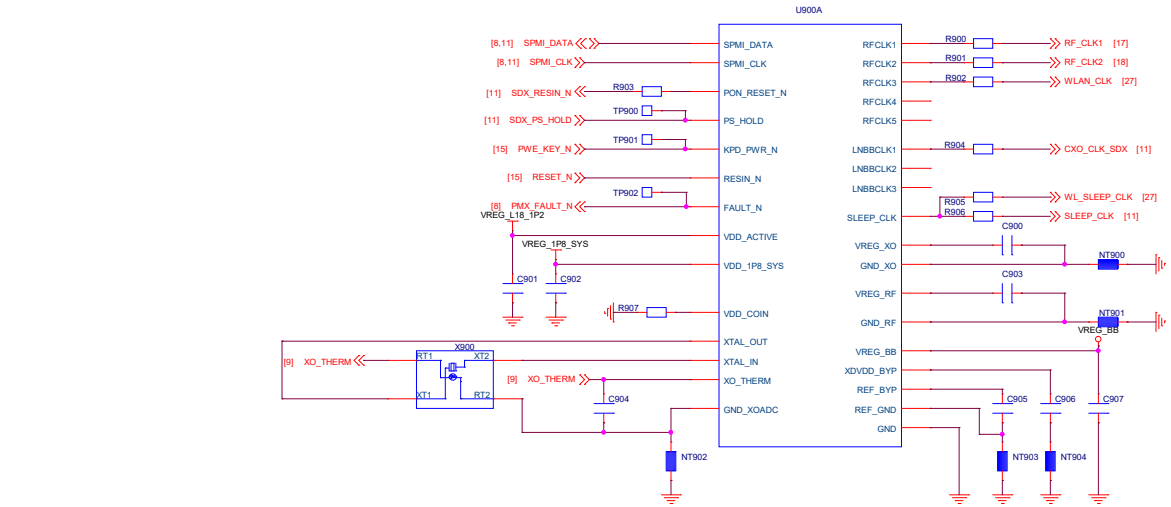

U600B
VREG_S2_1P2
VREG_S8_0P8
VREG_S7_0P9
VREG_S3_0P8
VDD_L1
VDD_L2_L18
VDD_L3
VDD_L4
VDD_L7
VDD_L8_L9
VDD_L12
VDD_L14
VDD_L15
VDD_L17
VDD_L19
VDD_L20
VDD_L21
VREG_L1
VREG_L2
VREG_L3
VREG_L4
VREG_L7
VREG_L7S
VREG_L8
VREG_L9
VREG_L12
VREG_L14
VREG_L14_S
VREG_L15
VREG_L17
VREG_L17_S
VREG_L18
VREG_L19
VREG_L20
VREG_L21
VREG_L1_1P2
VREG_L2_1P1
VREG_L3_0P8
VREG_L4_0P9
VREG_L7_0P7
VREG_L8_0P8
VREG_L9_0P8
VREG_L12_1P2
VREG_L14_0P8
VREG_L15_1P2
VREG_L17_0P8
VREG_L18_1P2
VREG_L19_0P7
VREG_L20_0P9
VREG_L21_0P9
C700
C701
C702
C703
C704
C705
C706
C707
C708
C709
C710
C711
C712
C713
C714

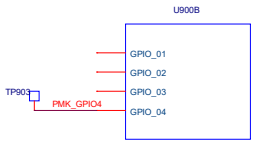

U600C
VREG_S4_1P9
VBAT_BB
VDD_L5_L6_L16
VDD_L10
VDD_L11_L13
VREG_L5
VREG_L6
VREG_L10
VREG_L11
VREG_L13
VREG_L16
VREG_L5_1P8
VREG_L6_1P8
VREG_L10_3P1
USIM1_VDD
USIM2_VDD
VREG_L16_1P8
C715
C716
C717

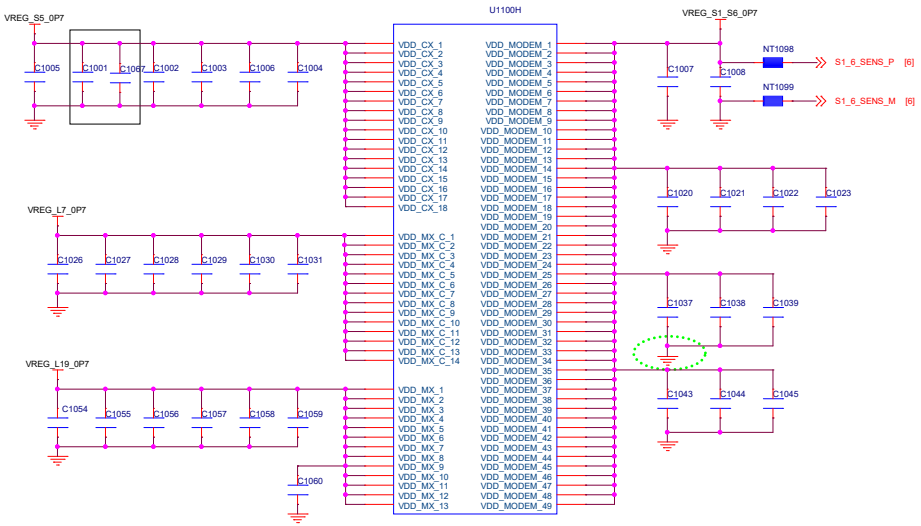

VBAT_BB
VREG_L6_1P8
C800
C801
U600D
VPH_PWR
VDD_IO_AP
VDD_IO
VIN_1P8_SYS
VREG_S4_1P9
C802
[9,11] SPMI_CLK
[9,11] SPMI_DATA
[3,8] VBUS_DET
[8] PA_THERM1
[8] PA_THERM2
[8] MDM_THERM
[8] MCP_THERM
NT801
R800
[8] XO_THERM1
NT802
SPMI_CLK
SPMI_DATA
VBUS_DET
AMUX1
AMUX2
AMUX3
AMUX4
AMUX5
AMUX6
XOADC_GND
FAULT_N
VREF_IX
VREF_IXAON
VREG_1P8_SYS
VREG_1P2_SYS
REF_BYP
REF_GND
TEST_EN_VPP
CMN_GND_1
CMN_GND_2
CMN_GND_3
CMN_GND_4
SP2
SP1
[9] PMX_FAULT_N
VREG_1P8_SYS
C803
C804
NT800


RT800
RT801
RT802
RT803
RT804
[8] PA_THERM1
[8] PA_THERM2
[8] MDM_THERM
[8] MCP_THERM
[8] XO_THERM1


U600A
[29] CBL
R601
[5,27] WL_SW_CTRL
Q800
[15] SIM_TEMP_ADC
[3,8] VBUS_DET
[3] USB_TEMP_ADC
[4] PACK_ID
[27] WLAN_TEMP_ADC
GPIO_01
GPIO_02
GPIO_03
GPIO_04
GPIO_05
GPIO_06
GPIO_07
GPIO_08
GPIO_09
GPIO_10
GPIO_11
GPIO_12
GPIO_13
GPIO_14
GPIO_15
GPIO_16


U900A
[8,11] SPMI_DATA
[8,11] SPMI_CLK
[11] SDX_RESIN_N
[11] SDX_PS_HOLD
[15] PWE_KEY_N
[15] RESET_N
[8] PMX_FAULT_N
VREG_L18_1P2
VREG_1P8_SYS
C901
C902
R903
TP900
TP901
TP902
R907
[9] XO_THERM
X900
RT1
XT2
XT1
RT2
[9] XO_THERM
C904
NT902
SPMI_DATA
SPMI_CLK
PON_RESET_N
PS_HOLD
KPD_PWR_N
RESIN_N
FAULT_N
VDD_ACTIVE
VDD_1P8_SYS
VDD_COIN
XTAL_OUT
XTAL_IN
XO_THERM
GND_XOADC
RFCLK1
RFCLK2
RFCLK3
RFCLK4
RFCLK5
LNBBCLK1
LNBBCLK2
LNBBCLK3
SLEEP_CLK
VREG_XO
GND_XO
VREG_RF
GND_RF
VREG_BB
XDVDD_BYP
REF_BYP
REF_GND
GND
R900
R901
R902
R904
R905
R906
C900
C903
NT900
NT901
VREG_BB
C905
C906
C907
NT903
NT904
RF_CLK1 [17]
RF_CLK2 [18]
WLAN_CLK [27]
CXO_CLK_SDX [11]
WL_SLEEP_CLK [27]
SLEEP_CLK [11]


U900B
GPIO_01
GPIO_02
GPIO_03
GPIO_04
TP903
PMK_GPIO4


U1100H
VREG_S5_0P7
VREG_S1_S6_0P7
VREG_L7_0P7
VREG_L19_0P7
NT1098
NT1099
S1_6_SENS_P [6]
S1_6_SENS_M [6]
C1005
C1001
C1007
C1002
C1003
C1006
C1004
C1007
C1008
C1020
C1021
C1022
C1023
C1026
C1027
C1028
C1029
C1030
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C1037
C1038
C1039
C1054
C1055
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C1057
C1058
C1059
C1043
C1044
C1045
C1060
VDD_CX_1
VDD_CX_2
VDD_CX_3
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VDD_CX_6
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VDD_CX_14
VDD_CX_15
VDD_CX_16
VDD_CX_17
VDD_CX_18
VDD_MX_C_1
VDD_MX_C_2
VDD_MX_C_3
VDD_MX_C_4
VDD_MX_C_5
VDD_MX_C_6
VDD_MX_C_7
VDD_MX_C_8
VDD_MX_C_9
VDD_MX_C_10
VDD_MX_C_11
VDD_MX_C_12
VDD_MX_C_13
VDD_MX_C_14
VDD_MX_1
VDD_MX_2
VDD_MX_3
VDD_MX_4
VDD_MX_5
VDD_MX_6
VDD_MX_7
VDD_MX_8
VDD_MX_9
VDD_MX_10
VDD_MX_11
VDD_MX_12
VDD_MX_13
VDD_MODEM_1
VDD_MODEM_2
VDD_MODEM_3
VDD_MODEM_4
VDD_MODEM_5
VDD_MODEM_6
VDD_MODEM_7
VDD_MODEM_8
VDD_MODEM_9
VDD_MODEM_10
VDD_MODEM_11
VDD_MODEM_12
VDD_MODEM_13
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VDD_MODEM_16
VDD_MODEM_17
VDD_MODEM_18
VDD_MODEM_19
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VDD_MODEM_28
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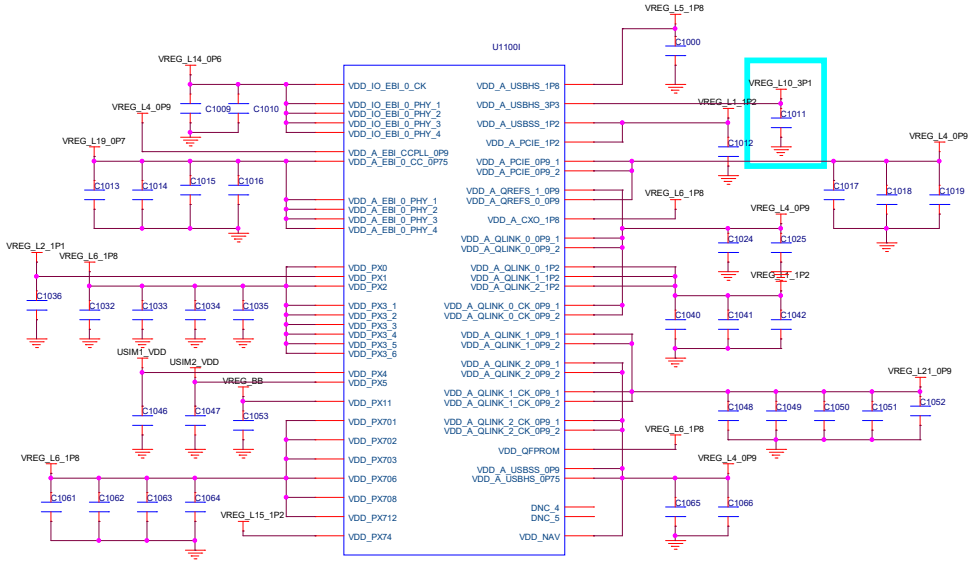
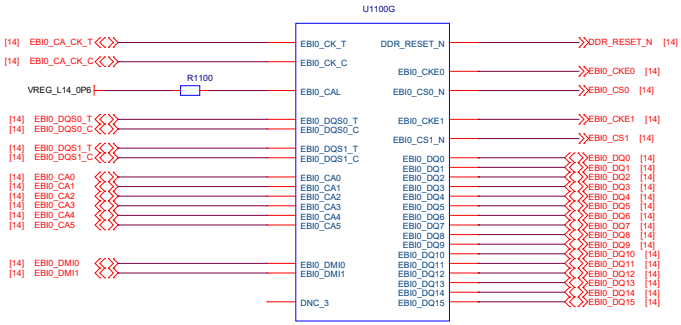
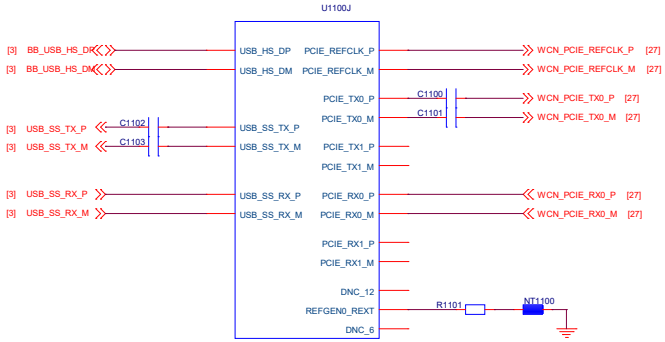
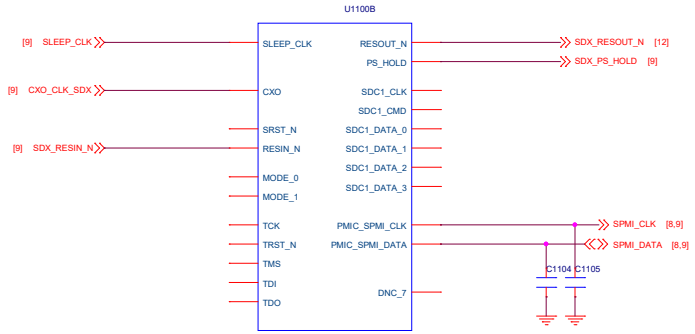
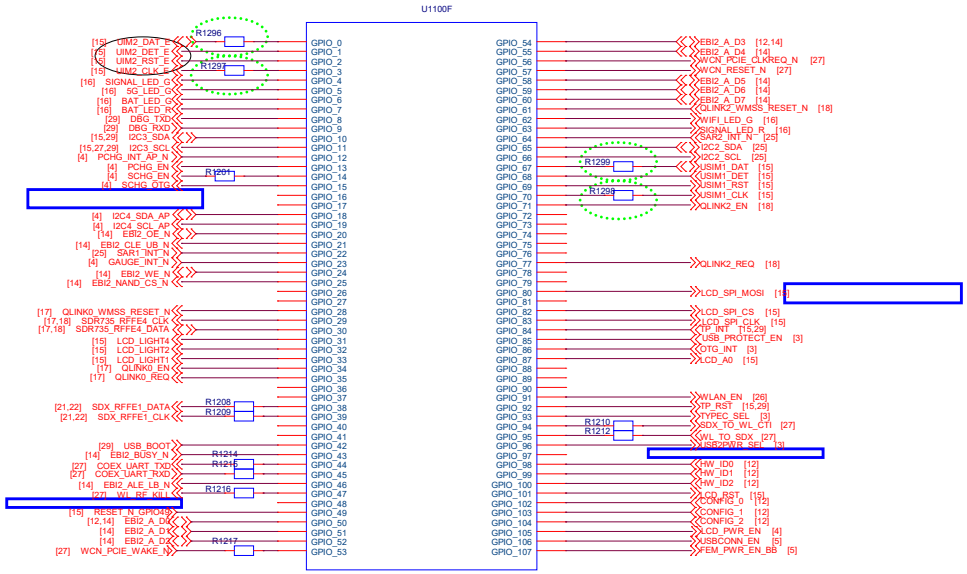
VDD_MODEM_30
VDD_MODEM_31
VDD_MODEM_32
VDD_MODEM_33
VDD_MODEM_34
VDD_MODEM_35
VDD_MODEM_36
VDD_MODEM_37
VDD_MODEM_38
VDD_MODEM_39
VDD_MODEM_40
VDD_MODEM_41
VDD_MODEM_42
VDD_MODEM_43
VDD_MODEM_44
VDD_MODEM_45
VDD_MODEM_46
VDD_MODEM_47
VDD_MODEM_48
VDD_MODEM_49

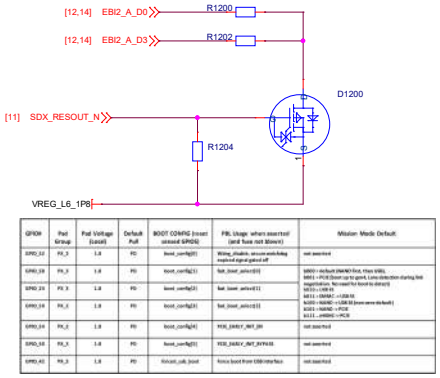

U1100I
VREG_L5_1P8
VREG_L14_0P6
VREG_L4_0P9
VREG_L19_0P7
VREG_L10_3P1
VREG_L1_1P2
VREG_L2_1P1
VREG_L6_1P8
USIM1_VDD
USIM2_VDD
VREG_BB
VREG_L15_1P2
VREG_L21_0P9
C1000
C1009
C1010
C1011
C1012
C1013
C1014
C1015
C1016
C1017
C1018
C1019
C1024
C1025
C1036
C1032
C1033
C1034
C1035
C1040
C1041
C1042
C1046
C1047
C1053
C1048
C1049
C1050
C1051
C1052
C1061
C1062
C1063
C1064
C1065
C1066
VDD_IO_EBI_0_CK
VDD_IO_EBI_0_PHY_1
VDD_IO_EBI_0_PHY_2
VDD_IO_EBI_0_PHY_3
VDD_IO_EBI_0_PHY_4
VDD_A_EBI_CCPLL_0P9
VDD_A_EBI_0_CC_0P75
VDD_A_EBI_0_PHY_1
VDD_A_EBI_0_PHY_2
VDD_A_EBI_0_PHY_3
VDD_A_EBI_0_PHY_4
VDD_PX0
VDD_PX1
VDD_PX2
VDD_PX3_1
VDD_PX3_2
VDD_PX3_3
VDD_PX3_4
VDD_PX3_5
VDD_PX3_6
VDD_PX4
VDD_PX5
VDD_PX11
VDD_PX701
VDD_PX702
VDD_PX703
VDD_PX706
VDD_PX708
VDD_PX712
VDD_PX74
VDD_A_USBHS_1P8
VDD_A_USBHS_3P3
VDD_A_USBSS_1P2
VDD_A_PCIE_1P2
VDD_A_PCIE_0P9_1
VDD_A_PCIE_0P9_2
VDD_A_QREFS_1_0P9
VDD_A_QREFS_0_0P9
VDD_A_CXO_1P8
VDD_A_QLINK_0_0P9_1
VDD_A_QLINK_0_0P9_2
VDD_A_QLINK_0_1P2
VDD_A_QLINK_1_1P2
VDD_A_QLINK_2_1P2
VDD_A_QLINK_0_CK_0P9_1
VDD_A_QLINK_0_CK_0P9_2
VDD_A_QLINK_1_0P9_1
VDD_A_QLINK_1_0P9_2
VDD_A_QLINK_2_0P9_1
VDD_A_QLINK_2_0P9_2
VDD_A_QLINK_1_CK_0P9_1
VDD_A_QLINK_1_CK_0P9_2
VDD_A_QLINK_2_CK_0P9_1
VDD_A_QLINK_2_CK_0P9_2
VDD_QFPROM
VDD_A_USBSS_0P9
VDD_A_USBHS_0P75
DNC_4
DNC_5
VDD_NAV


U1100G
[14] EBI0_CA_CK_T
[14] EBI0_CA_CK_C
R1100
VREG_L14_0P6
[14] EBI0_DQS0_T
[14] EBI0_DQS0_C
[14] EBI0_DQS1_T
[14] EBI0_DQS1_C
[14] EBI0_CA0
[14] EBI0_CA1
[14] EBI0_CA2
[14] EBI0_CA3
[14] EBI0_CA4
[14] EBI0_CA5
[14] EBI0_DMI0
[14] EBI0_DMI1
EBI0_CK_T
EBI0_CK_C
EBI0_CAL
EBI0_DQS0_T
EBI0_DQS0_C
EBI0_DQS1_T
EBI0_DQS1_C
EBI0_CA0
EBI0_CA1
EBI0_CA2
EBI0_CA3
EBI0_CA4
EBI0_CA5
EBI0_DMI0
EBI0_DMI1
DNC_3
DDR_RESET_N
EBI0_CKE0
EBI0_CS0_N
EBI0_CKE1
EBI0_CS1_N
EBI0_DQ0
EBI0_DQ1
EBI0_DQ2
EBI0_DQ3
EBI0_DQ4
EBI0_DQ5
EBI0_DQ6
EBI0_DQ7
EBI0_DQ8
EBI0_DQ9
EBI0_DQ10
EBI0_DQ11
EBI0_DQ12
EBI0_DQ13
EBI0_DQ14
EBI0_DQ15
DDR_RESET_N [14]
EBI0_CKE0 [14]
EBI0_CS0 [14]
EBI0_CKE1 [14]
EBI0_CS1 [14]
EBI0_DQ0 [14]
EBI0_DQ1 [14]
EBI0_DQ2 [14]
EBI0_DQ3 [14]
EBI0_DQ4 [14]
EBI0_DQ5 [14]
EBI0_DQ6 [14]
EBI0_DQ7 [14]
EBI0_DQ8 [14]
EBI0_DQ9 [14]
EBI0_DQ10 [14]
EBI0_DQ11 [14]
EBI0_DQ12 [14]
EBI0_DQ13 [14]
EBI0_DQ14 [14]
EBI0_DQ15 [14]

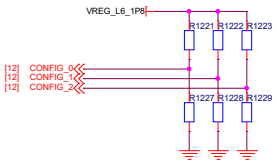

U1100J
[3] BB_USB_HS_DP
[3] BB_USB_HS_DM
[3] USB_SS_TX_P
[3] USB_SS_TX_M
[3] USB_SS_RX_P
[3] USB_SS_RX_M
C1102
C1103
USB_HS_DP
USB_HS_DM
USB_SS_TX_P
USB_SS_TX_M
USB_SS_RX_P
USB_SS_RX_M
PCIE_REFCLK_P
PCIE_REFCLK_M
PCIE_TX0_P
PCIE_TX0_M
PCIE_TX1_P
PCIE_TX1_M
PCIE_RX0_P
PCIE_RX0_M
PCIE_RX1_P
PCIE_RX1_M
DNC_12
REFGEN0_REXT
DNC_6
C1100
C1101
R1101
NT1100
WCN_PCIE_REFCLK_P [27]
WCN_PCIE_REFCLK_M [27]
WCN_PCIE_TX0_P [27]
WCN_PCIE_TX0_M [27]
WCN_PCIE_RX0_P [27]
WCN_PCIE_RX0_M [27]

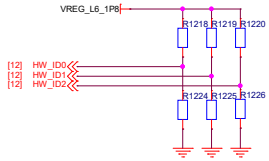

U1100B
[9] SLEEP_CLK
[9] CXO_CLK_SDX
[9] SDX_RESIN_N
SLEEP_CLK
CXO
SRST_N
RESIN_N
MODE_0
MODE_1
TCK
TRST_N
TMS
TDI
TDO
RESOUT_N
PS_HOLD
SDC1_CLK
SDC1_CMD
SDC1_DATA_0
SDC1_DATA_1
SDC1_DATA_2
SDC1_DATA_3
PMIC_SPMI_CLK
PMIC_SPMI_DATA
DNC_7
SDX_RESOUT_N [12]
SDX_PS_HOLD [9]
SPMI_CLK [8,9]
SPMI_DATA [8,9]
C1104
C1105

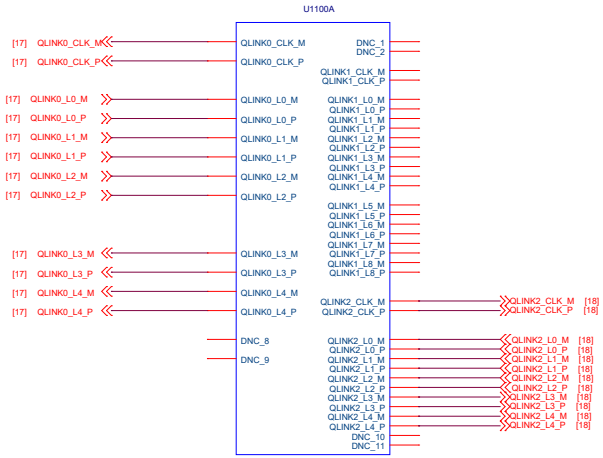


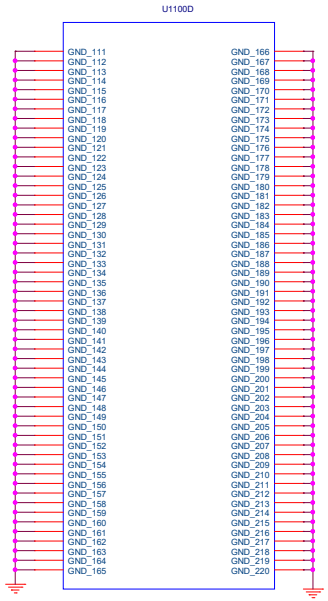


GPIO#	Pad Group	Pad Voltage (used)	Default Pull	BOOT CONFIG (reset sensed GPIO)	FBL Usage when asserted (and fuse not blown)	Mission Mode Default
GPIO_52	PA_5	1.8	PD	boot_config[0]	Wiring_disable, secure-mode debug, explored signal pulled off	not asserted
GPIO_53	PA_6	1.8	PD	boot_config[1]	fast_boot_select[0]	b000 = default (NAND first, then UFS) b001 = PCIE (boot up to gen4, Long detection during link negotiation. No need for host to detect) b010 = USB HS b011 = EMMC -> USB HS b100 = NAND -> USB SS (non-secure device) b101 = NAND -> PCIE b111 = JTAG/HS -> PCIE
GPIO_54	PA_7	1.8	PD	boot_config[2]	fast_boot_select[1]	
GPIO_55	PA_8	1.8	PD	boot_config[3]	fast_boot_select[2]	
GPIO_56	PA_9	1.8	PD	boot_config[4]	RSE_BASEV_INIT_DN	not asserted
GPIO_57	PA_10	1.8	PD	boot_config[5]	RSE_BASEV_INIT_PWR5S	not asserted
GPIO_58	PA_11	1.8	PD	fdcust_usb_boot	force boot from EMMC/the fuse	not asserted






U1100A
[17] QLINK0_CLK_M
[17] QLINK0_CLK_P
[17] QLINK0_L0_M
[17] QLINK0_L0_P
[17] QLINK0_L1_M
[17] QLINK0_L1_P
[17] QLINK0_L2_M
[17] QLINK0_L2_P
[17] QLINK0_L3_M
[17] QLINK0_L3_P
[17] QLINK0_L4_M
[17] QLINK0_L4_P
QLINK0_CLK_M
QLINK0_CLK_P
QLINK0_L0_M
QLINK0_L0_P
QLINK0_L1_M
QLINK0_L1_P
QLINK0_L2_M
QLINK0_L2_P
QLINK0_L3_M
QLINK0_L3_P
QLINK0_L4_M
QLINK0_L4_P
DNC_8
DNC_9
DNC_1
DNC_2
QLINK1_CLK_M
QLINK1_CLK_P
QLINK1_L0_M
QLINK1_L0_P
QLINK1_L1_M
QLINK1_L1_P
QLINK1_L2_M
QLINK1_L2_P
QLINK1_L3_M
QLINK1_L3_P
QLINK1_L4_M
QLINK1_L4_P
QLINK1_L5_M
QLINK1_L5_P
QLINK1_L6_M
QLINK1_L6_P
QLINK1_L7_M
QLINK1_L7_P
QLINK1_L8_M
QLINK1_L8_P
QLINK2_CLK_M
QLINK2_CLK_P
QLINK2_L0_M
QLINK2_L0_P
QLINK2_L1_M
QLINK2_L1_P
QLINK2_L2_M
QLINK2_L2_P
QLINK2_L3_M
QLINK2_L3_P
QLINK2_L4_M
QLINK2_L4_P
DNC_10
DNC_11
QLINK2_CLK_M [18]
QLINK2_CLK_P [18]
QLINK2_L0_M [18]
QLINK2_L0_P [18]
QLINK2_L1_M [18]
QLINK2_L1_P [18]
QLINK2_L2_M [18]
QLINK2_L2_P [18]
QLINK2_L3_M [18]
QLINK2_L3_P [18]
QLINK2_L4_M [18]
QLINK2_L4_P [18]


U1100D
GND_111
GND_112
GND_113
GND_114
GND_115
GND_116
GND_117
GND_118
GND_119
GND_120
GND_121
GND_122
GND_123
GND_124
GND_125
GND_126
GND_127
GND_128
GND_129
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GND_134
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GND_136
GND_137
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GND_200
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GND_202
GND_203
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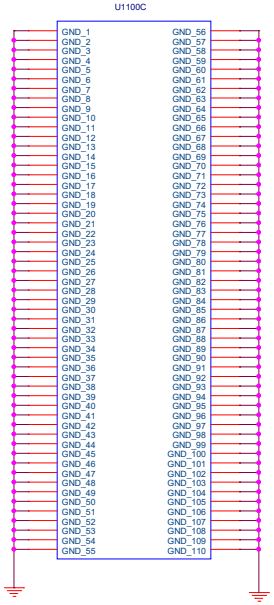
GND_211
GND_212
GND_213
GND_214
GND_215
GND_216
GND_217
GND_218
GND_219
GND_220


U1100C
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
GND_12
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GND_87
GND_88
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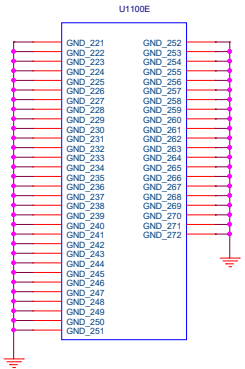
GND_90
GND_91
GND_92
GND_93
GND_94
GND_95
GND_96
GND_97
GND_98
GND_99
GND_100
GND_101
GND_102
GND_103
GND_104
GND_105
GND_106
GND_107
GND_108
GND_109
GND_110


U1100E
GND_221
GND_222
GND_223
GND_224
GND_225
GND_226
GND_227
GND_228
GND_229
GND_230
GND_231
GND_232
GND_233
GND_234
GND_235
GND_236
GND_237
GND_238
GND_239
GND_240
GND_241
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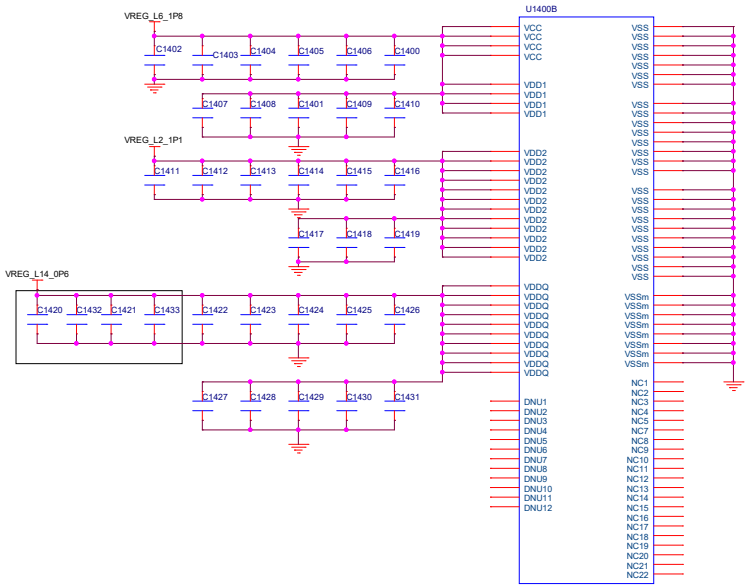
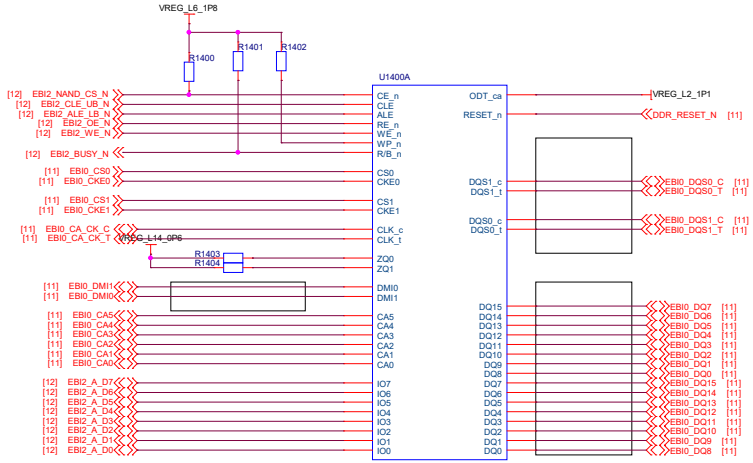
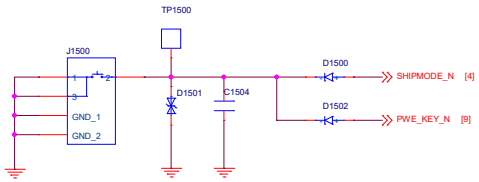
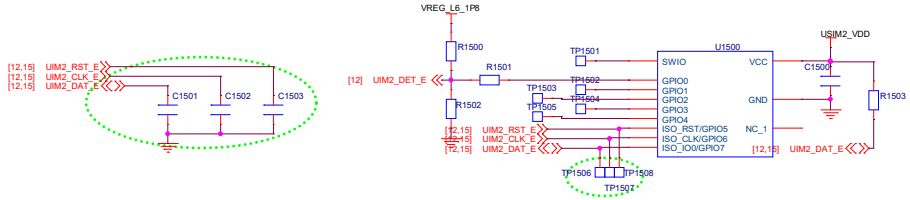
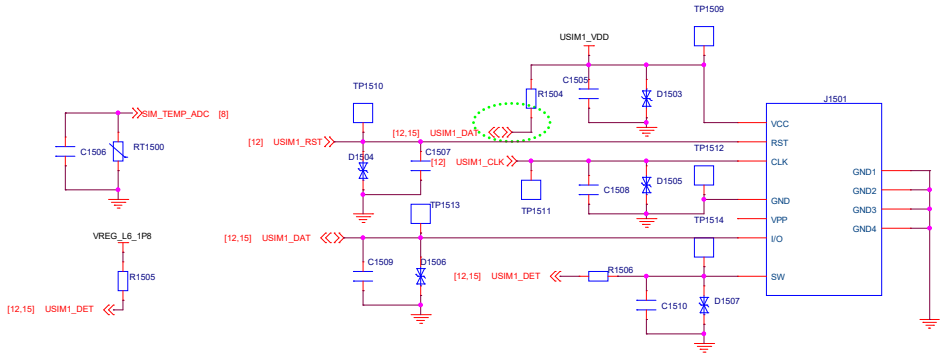
GND_248
GND_249
GND_250
GND_251
GND_252
GND_253
GND_254
GND_255
GND_256
GND_257
GND_258
GND_259
GND_260
GND_261
GND_262
GND_263
GND_264
GND_265
GND_266
GND_267
GND_268
GND_269
GND_270
GND_271
GND_272

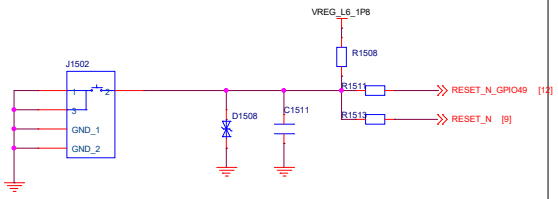

VREG_L6_1P8
C1402
C1403
C1404
C1405
C1406
C1400
C1407
C1408
C1401
C1409
C1410
VREG_L2_1P1
C1411
C1412
C1413
C1414
C1415
C1416
C1417
C1418
C1419
VREG_L14_0P6
C1420
C1432
C1421
C1433
C1422
C1423
C1424
C1425
C1426
C1427
C1428
C1429
C1430
C1431
U1400B
VCC
VDD1
VDD2
VDDQ
DNU1
DNU2
DNU3
DNU4
DNU5
DNU6
DNU7
DNU8
DNU9
DNU10
DNU11
DNU12
VSS
VSSm
NC1
NC2
NC3
NC4
NC5
NC7
NC8
NC9
NC10
NC11
NC12
NC13
NC14
NC15
NC16
NC17
NC18
NC19
NC20
NC21
NC22

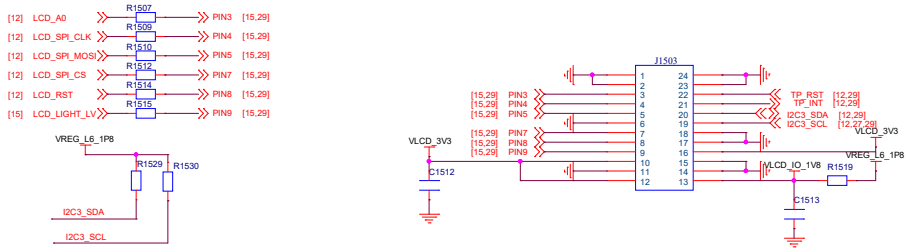

VREG_L6_1P8
R1400
R1401
R1402
U1400A
[12] EBI2_NAND_CS_N
[12] EBI2_CLE_UB_N
[12] EBI2_ALE_LB_N
[12] EBI2_OE_N
[12] EBI2_WE_N
[12] EBI2_BUSY_N
[11] EBI0_CS0
[11] EBI0_CKE0
[11] EBI0_CS1
[11] EBI0_CKE1
[11] EBI0_CA_CK_C
[11] EBI0_CA_CK_T
VREG_L14_0P6
R1403
R1404
[11] EBI0_DMI1
[11] EBI0_DMI0
[11] EBI0_CA5
[11] EBI0_CA4
[11] EBI0_CA3
[11] EBI0_CA2
[11] EBI0_CA1
[11] EBI0_CA0
[12] EBI2_A_D7
[12] EBI2_A_D6
[12] EBI2_A_D5
[12] EBI2_A_D4
[12] EBI2_A_D3
[12] EBI2_A_D2
[12] EBI2_A_D1
[12] EBI2_A_D0
CE_n
CLE
ALE
RE_n
WE_n
WP_n
R/B_n
CS0
CKE0
CS1
CKE1
CLK_c
CLK_t
ZQ0
ZQ1
DMI0
DMI1
CA5
CA4
CA3
CA2
CA1
CA0
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IO0
ODT_ca
RESET_n
DQS1_c
DQS1_t
DQS0_c
DQS0_t
DQ15
DQ14
DQ13
DQ12
DQ11
DQ10
DQ9
DQ8
DQ7
DQ6
DQ5
DQ4
DQ3
DQ2
DQ1
DQ0
VREG_L2_1P1
DDR_RESET_N [11]
EBI0_DQS0_C [11]
EBI0_DQS0_T [11]
EBI0_DQS1_C [11]
EBI0_DQS1_T [11]
EBI0_DQ7 [11]
EBI0_DQ6 [11]
EBI0_DQ5 [11]
EBI0_DQ4 [11]
EBI0_DQ3 [11]
EBI0_DQ2 [11]
EBI0_DQ1 [11]
EBI0_DQ0 [11]
EBI0_DQ15 [11]
EBI0_DQ14 [11]
EBI0_DQ13 [11]
EBI0_DQ12 [11]
EBI0_DQ11 [11]
EBI0_DQ10 [11]
EBI0_DQ9 [11]
EBI0_DQ8 [11]

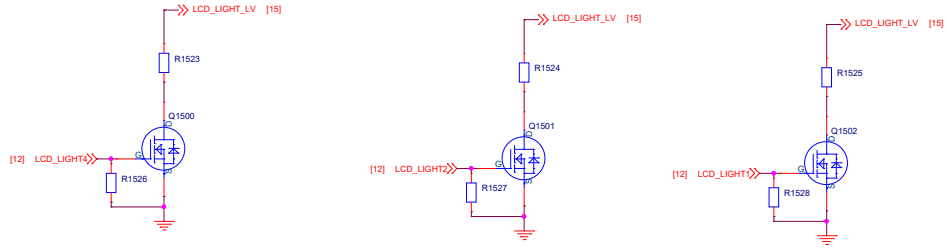

TP1500
J1500
D1500
D1501
C1504
D1502
SHIPMODE_N [4]
PWE_KEY_N [9]
GND_1
GND_2

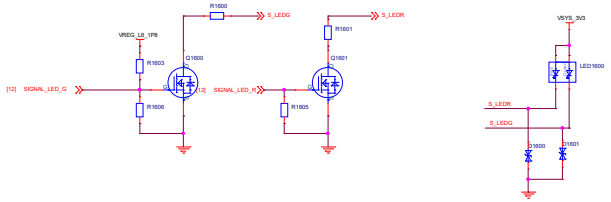

[12,15] UIM2_RST_E
[12,15] UIM2_CLK_E
[12,15] UIM2_DAT_E
C1501
C1502
C1503
VREG_L6_1P8
R1500
R1501
R1502
[12] UIM2_DET_E
TP1501
TP1502
TP1503
TP1504
TP1505
U1500
SWIO
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
ISO_RST/GPIO5
ISO_CLK/GPIO6
ISO_IO0/GPIO7
VCC
GND
NC_1
USIM2_VDD
C1500
R1503
[12,15] UIM2_DAT_E
TP1506
TP1508
TP1507


SIM_TEMP_ADC [8]
C1506
RT1500
VREG_L6_1P8
R1505
[12,15] USIM1_DET
TP1509
USIM1_VDD
C1505
R1504
D1503
TP1510
[12] USIM1_RST
[12,15] USIM1_DAT
C1507
D1504
[12] USIM1_CLK
TP1512
TP1513
TP1511
C1508
D1505
TP1514
C1509
D1506
R1506
C1510
D1507
J1501
VCC
RST
CLK
GND
VPP
I/O
SW
GND1
GND2
GND3
GND4

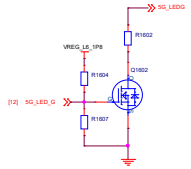

VREG_L6_1P8
R1508
J1502
R1511
R1513
D1508
C1511
RESET_N_GPIO49 [12]
RESET_N [9]
GND_1
GND_2

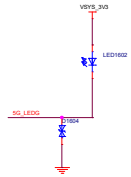

[12] LCD_A0
[12] LCD_SPI_CLK
[12] LCD_SPI_MOSI
[12] LCD_SPI_CS
[12] LCD_RST
[15] LCD_LIGHT_LV
R1507
R1509
R1510
R1512
R1514
R1515
PIN3 [15,29]
PIN4 [15,29]
PIN5 [15,29]
PIN7 [15,29]
PIN8 [15,29]
PIN9 [15,29]
VREG_L6_1P8
R1529
R1530
I2C3_SDA
I2C3_SCL
J1503
[15,29] PIN3
[15,29] PIN4
[15,29] PIN5
[15,29] PIN7
[15,29] PIN8
[15,29] PIN9
TP_RST [12,29]
TP_INT [12,29]
I2C3_SDA [12,29]
I2C3_SCL [12,27,29]
VLCD_3V3
C1512
VLCD_IO_1V8
R1519
C1513

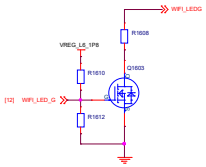

LCD_LIGHT_LV [15]
R1523
Q1500
[12] LCD_LIGHT
R1526
R1524
Q1501
[12] LCD_LIGHT2
R1527
R1525
Q1502
[12] LCD_LIGHT1
R1528

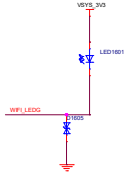

R1600
S_LEDG
S_LEDR
R1601
VREG_L6_1P8
Q1600
Q1601
R1603
[12] SIGNAL_LED_G
[12] SIGNAL_LED_R
R1606
R1605

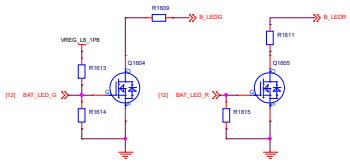
VSYS_3V3
LED1600
S_LEDR
S_LEDG
R1600
Q1601

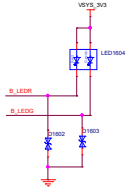

5G_LEDG
R1602
VREG_L6_1P8
Q1602
R1604
[12] 5G_LED_G
R1607

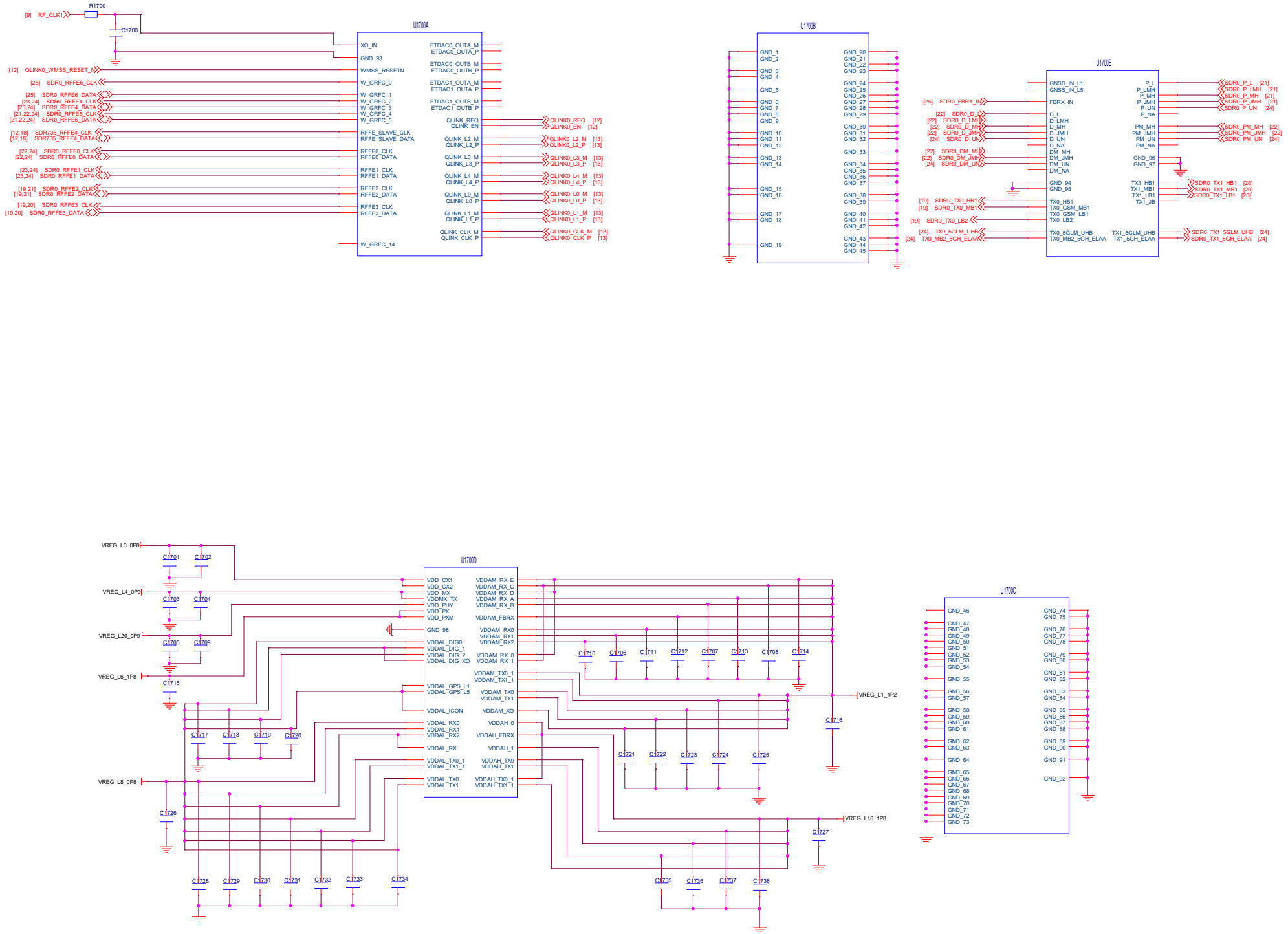

VSYS_3V3
LED1602
5G_LEDG
R1604

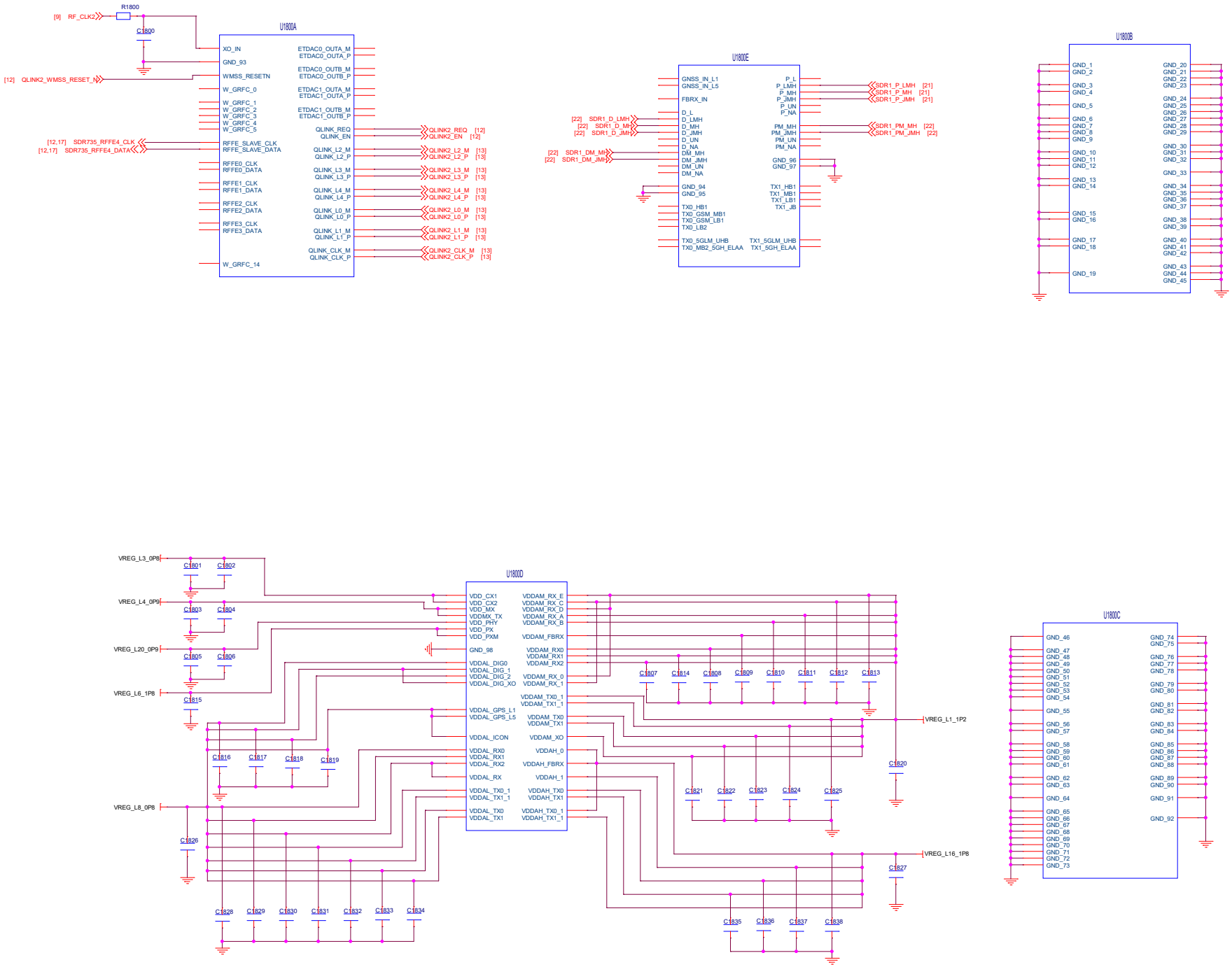

WIFI_LEDG
R1608
VREG_L6_1P8
Q1603
R1610
[12] WIFI_LED_G
R1612

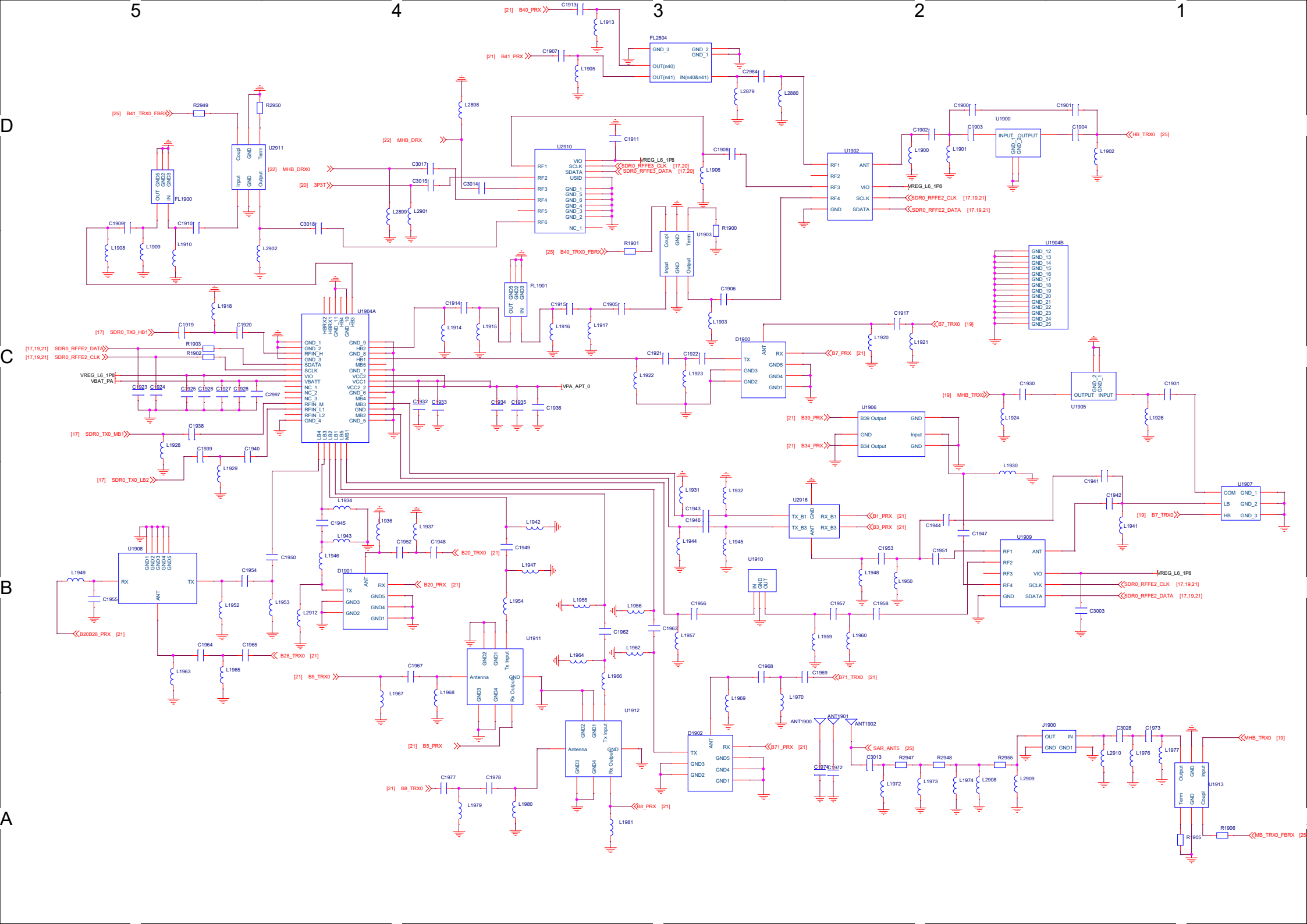

VSYS_3V3
LED1601
WIFI_LEDG
R1605


R1609
B_LEDG
B_LEDR
R1611
VREG_L6_1P8
Q1604
Q1605
R1613
[12] BAT_LED_G
[12] BAT_LED_R
R1614
R1615


VSYS_3V3
LED1604
B_LEDR
B_LEDG
Q1602
Q1603


R1700
[9] RF_CLK1
C1700
U1700A
XO_IN
GND_93
[12] QLINK0_WMSS_RESET_N
WMSS_RESETN
[25] SDR0_RFFE6_CLK
W_GRFC_0
[25] SDR0_RFFE6_DATA
[23,24] SDR0_RFFE4_CLK
[23,24] SDR0_RFFE4_DATA
[21,22,24] SDR0_RFFE5_CLK
[21,22,24] SDR0_RFFE5_DATA
W_GRFC_1
W_GRFC_2
W_GRFC_3
W_GRFC_4
W_GRFC_5
[12,18] SDR735_RFFE4_CLK
[12,18] SDR735_RFFE4_DATA
RFFE_SLAVE_CLK
RFFE_SLAVE_DATA
[22,24] SDR0_RFFE0_CLK
[22,24] SDR0_RFFE0_DATA
RFFE0_CLK
RFFE0_DATA
[23,24] SDR0_RFFE1_CLK
[23,24] SDR0_RFFE1_DATA
RFFE1_CLK
RFFE1_DATA
[19,21] SDR0_RFFE2_CLK
[19,21] SDR0_RFFE2_DATA
RFFE2_CLK
RFFE2_DATA
[19,20] SDR0_RFFE3_CLK
[19,20] SDR0_RFFE3_DATA
RFFE3_CLK
RFFE3_DATA
W_GRFC_14
ETDAC0_OUTA_M
ETDAC0_OUTA_P
ETDAC0_OUTB_M
ETDAC0_OUTB_P
ETDAC1_OUTA_M
ETDAC1_OUTA_P
ETDAC1_OUTB_M
ETDAC1_OUTB_P
QLINK_REQ
QLINK_EN
QLINK_L2_M
QLINK_L2_P
QLINK_L3_M
QLINK_L3_P
QLINK_L4_M
QLINK_L4_P
QLINK_L0_M
QLINK_L0_P
QLINK_L1_M
QLINK_L1_P
QLINK_CLK_M
QLINK_CLK_P
QLINK0_REQ [12]
QLINK0_EN [12]
QLINK0_L2_M [13]
QLINK0_L2_P [13]
QLINK0_L3_M [13]
QLINK0_L3_P [13]
QLINK0_L4_M [13]
QLINK0_L4_P [13]
QLINK0_L0_M [13]
QLINK0_L0_P [13]
QLINK0_L1_M [13]
QLINK0_L1_P [13]
QLINK0_CLK_M [13]
QLINK0_CLK_P [13]
U1700B
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
GND_12
GND_13
GND_14
GND_15
GND_16
GND_17
GND_18
GND_19
GND_20
GND_21
GND_22
GND_23
GND_24
GND_25
GND_26
GND_27
GND_28
GND_29
GND_30
GND_31
GND_32
GND_33
GND_34
GND_35
GND_36
GND_37
GND_38
GND_39
GND_40
GND_41
GND_42
GND_43
GND_44
GND_45
U1700E
GNSS_IN_L1
GNSS_IN_L5
[25] SDR0_FBRX_IN
FBRX_IN
[22] SDR0_D_L
[22] SDR0_D_LMH
[22] SDR0_D_MH
[22] SDR0_D_JMH
[24] SDR0_D_UN
D_L
D_LMH
D_MH
D_JMH
D_UN
D_NA
[22] SDR0_DM_MH
[22] SDR0_DM_JMH
[24] SDR0_DM_UN
DM_MH
DM_JMH
DM_UN
DM_NA
GND_94
GND_95
[19] SDR0_TX0_HB1
[19] SDR0_TX0_MB1
TX0_HB1
TX0_GSM_MB1
TX0_GSM_LB1
TX0_LB2
[19] SDR0_TX0_LB2
[24] TX0_5GLM_UHB
[24] TX0_MB2_5GH_ELAA
TX0_5GLM_UHB
TX0_MB2_5GH_ELAA
P_L
P_LMH
P_MH
P_JMH
P_UN
P_NA
PM_MH
PM_JMH
PM_UN
PM_NA
GND_96
GND_97
TX1_HB1
TX1_MB1
TX1_LB1
TX1_JB
TX1_5GLM_UHB
TX1_5GH_ELAA
SDR0_P_L [21]
SDR0_P_LMH [21]
SDR0_P_MH [21]
SDR0_P_JMH [21]
SDR0_P_UN [24]
SDR0_PM_MH [22]
SDR0_PM_JMH [22]
SDR0_PM_UN [24]
SDR0_TX1_HB1 [20]
SDR0_TX1_MB1 [20]
SDR0_TX1_LB1 [20]
SDR0_TX1_5GLM_UHB [24]
SDR0_TX1_5GH_ELAA [24]
VREG_L3_0P8
C1701
C1702
VREG_L4_0P9
C1703
C1704
VREG_L20_0P9
C1705
C1709
VREG_L6_1P8
C1715
C1717
C1718
C1719
C1720
VREG_L8_0P8
C1726
C1728
C1729
C1730
C1731
C1732
C1733
C1734
U1700D
VDD_CX1
VDD_CX2
VDD_MX
VDDMX_TX
VDD_PHY
VDD_PX
VDD_PXM
GND_98
VDDAL_DIG0
VDDAL_DIG_1
VDDAL_DIG_2
VDDAL_DIG_XO
VDDAL_GPS_L1
VDDAL_GPS_L5
VDDAL_ICON
VDDAL_RX0
VDDAL_RX1
VDDAL_RX2
VDDAL_RX
VDDAL_TX0_1
VDDAL_TX1_1
VDDAL_TX0
VDDAL_TX1
VDDAM_RX_E
VDDAM_RX_C
VDDAM_RX_D
VDDAM_RX_A
VDDAM_RX_B
VDDAM_FBRX
VDDAM_RX0
VDDAM_RX1
VDDAM_RX2
VDDAM_RX_0
VDDAM_RX_1
VDDAM_TX0_1
VDDAM_TX1_1
VDDAM_TX0
VDDAM_TX1
VDDAM_XO
VDDAH_0
VDDAH_FBRX
VDDAH_1
VDDAH_TX0
VDDAH_TX1
VDDAH_TX0_1
VDDAH_TX1_1
C1710
C1706
C1711
C1712
C1707
C1713
C1708
C1714
C1721
C1722
C1723
C1724
C1725
C1716
C1727
C1735
C1736
C1737
C1738
VREG_L1_1P2
VREG_L16_1P8
U1700C
GND_46
GND_47
GND_48
GND_49
GND_50
GND_51
GND_52
GND_53
GND_54
GND_55
GND_56
GND_57
GND_58
GND_59
GND_60
GND_61
GND_62
GND_63
GND_64
GND_65
GND_66
GND_67
GND_68
GND_69
GND_70
GND_71
GND_72
GND_73
GND_74
GND_75
GND_76
GND_77
GND_78
GND_79
GND_80
GND_81
GND_82
GND_83
GND_84
GND_85
GND_86
GND_87
GND_88
GND_89
GND_90
GND_91
GND_92


R1800
[9] RF_CLK2
C1800
U1800A
XO_IN
GND_93
[12] QLINK2_WMSS_RESET_N
WMSS_RESETN
W_GRFC_0
W_GRFC_1
W_GRFC_2
W_GRFC_3
W_GRFC_4
W_GRFC_5
[12,17] SDR735_RFFE4_CLK
[12,17] SDR735_RFFE4_DATA
RFFE_SLAVE_CLK
RFFE_SLAVE_DATA
RFFE0_CLK
RFFE0_DATA
RFFE1_CLK
RFFE1_DATA
RFFE2_CLK
RFFE2_DATA
RFFE3_CLK
RFFE3_DATA
W_GRFC_14
ETDAC0_OUTA_M
ETDAC0_OUTA_P
ETDAC0_OUTB_M
ETDAC0_OUTB_P
ETDAC1_OUTA_M
ETDAC1_OUTA_P
ETDAC1_OUTB_M
ETDAC1_OUTB_P
QLINK_REQ
QLINK_EN
QLINK_L2_M
QLINK_L2_P
QLINK_L3_M
QLINK_L3_P
QLINK_L4_M
QLINK_L4_P
QLINK_L0_M
QLINK_L0_P
QLINK_L1_M
QLINK_L1_P
QLINK_CLK_M
QLINK_CLK_P
QLINK2_REQ [12]
QLINK2_EN [12]
QLINK2_L2_M [13]
QLINK2_L2_P [13]
QLINK2_L3_M [13]
QLINK2_L3_P [13]
QLINK2_L4_M [13]
QLINK2_L4_P [13]
QLINK2_L0_M [13]
QLINK2_L0_P [13]
QLINK2_L1_M [13]
QLINK2_L1_P [13]
QLINK2_CLK_M [13]
QLINK2_CLK_P [13]
U1800E
GNSS_IN_L1
GNSS_IN_L5
FBRX_IN
D_L
D_LMH
D_MH
D_JMH
D_UN
D_NA
DM_MH
DM_JMH
DM_UN
DM_NA
GND_94
GND_95
TX0_HB1
TX0_GSM_MB1
TX0_GSM_LB1
TX0_LB2
TX0_5GLM_UHB
TX0_MB2_5GH_ELAA
[22] SDR1_D_LMH
[22] SDR1_D_MH
[22] SDR1_D_JMH
[22] SDR1_DM_MH
[22] SDR1_DM_JMH
P_L
P_LMH
P_MH
P_JMH
P_UN
P_NA
PM_MH
PM_JMH
PM_UN
PM_NA
GND_96
GND_97
TX1_HB1
TX1_MB1
TX1_LB1
TX1_JB
TX1_5GLM_UHB
TX1_5GH_ELAA
SDR1_P_LMH [21]
SDR1_P_MH [21]
SDR1_P_JMH [21]
SDR1_PM_MH [22]
SDR1_PM_JMH [22]
U1800B
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
GND_12
GND_13
GND_14
GND_15
GND_16
GND_17
GND_18
GND_19
GND_20
GND_21
GND_22
GND_23
GND_24
GND_25
GND_26
GND_27
GND_28
GND_29
GND_30
GND_31
GND_32
GND_33
GND_34
GND_35
GND_36
GND_37
GND_38
GND_39
GND_40
GND_41
GND_42
GND_43
GND_44
GND_45
VREG_L3_0P8
VREG_L4_0P9
VREG_L20_0P9
VREG_L6_1P8
VREG_L8_0P8
C1801
C1802
C1803
C1804
C1805
C1806
C1815
C1816
C1817
C1818
C1819
C1826
C1828
C1829
C1830
C1831
C1832
C1833
C1834
U1800D
VDD_CX1
VDD_CX2
VDD_MX
VDDMX_TX
VDD_PHY
VDD_PX
VDD_PXM
GND_98
VDDAL_DIG0
VDDAL_DIG_1
VDDAL_DIG_2
VDDAL_DIG_XO
VDDAL_GPS_L1
VDDAL_GPS_L5
VDDAL_ICON
VDDAL_RX0
VDDAL_RX1
VDDAL_RX2
VDDAL_RX
VDDAL_TX0_1
VDDAL_TX1_1
VDDAL_TX0
VDDAL_TX1
VDDAM_RX_E
VDDAM_RX_C
VDDAM_RX_D
VDDAM_RX_A
VDDAM_RX_B
VDDAM_FBRX
VDDAM_RX0
VDDAM_RX1
VDDAM_RX2
VDDAM_RX_0
VDDAM_RX_1
VDDAM_TX0_1
VDDAM_TX1_1
VDDAM_TX0
VDDAM_TX1
VDDAM_XO
VDDAH_0
VDDAH_FBRX
VDDAH_1
VDDAH_TX0
VDDAH_TX1
VDDAH_TX0_1
VDDAH_TX1_1
C1807
C1814
C1808
C1809
C1810
C1811
C1812
C1813
C1820
C1821
C1822
C1823
C1824
C1825
C1827
C1835
C1836
C1837
C1838
VREG_L1_1P2
VREG_L16_1P8
U1800C
GND_46
GND_47
GND_48
GND_49
GND_50
GND_51
GND_52
GND_53
GND_54
GND_55
GND_56
GND_57
GND_58
GND_59
GND_60
GND_61
GND_62
GND_63
GND_64
GND_65
GND_66
GND_67
GND_68
GND_69
GND_70
GND_71
GND_72
GND_73
GND_74
GND_75
GND_76
GND_77
GND_78
GND_79
GND_80
GND_81
GND_82
GND_83
GND_84
GND_85
GND_86
GND_87
GND_88
GND_89
GND_90
GND_91
GND_92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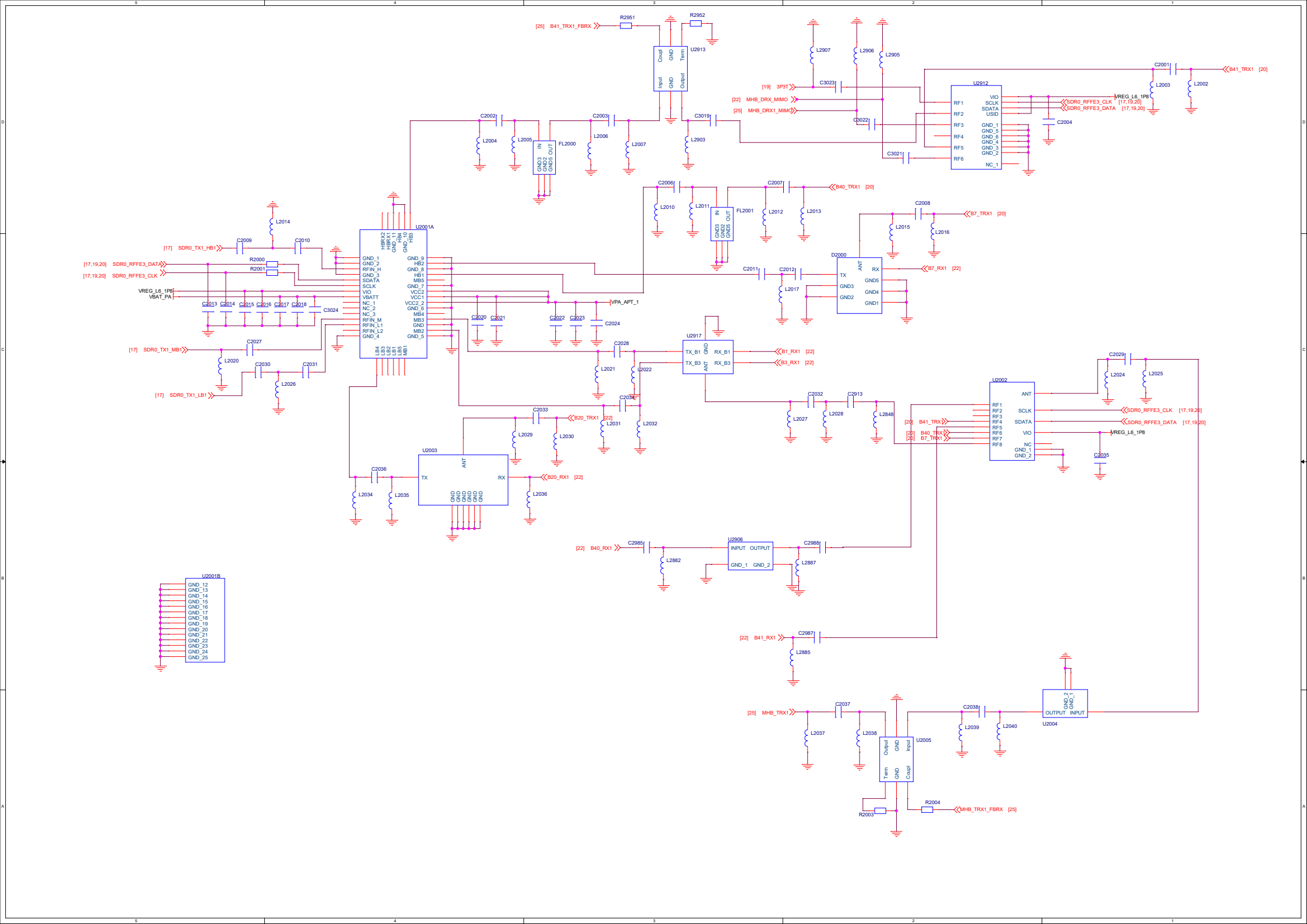
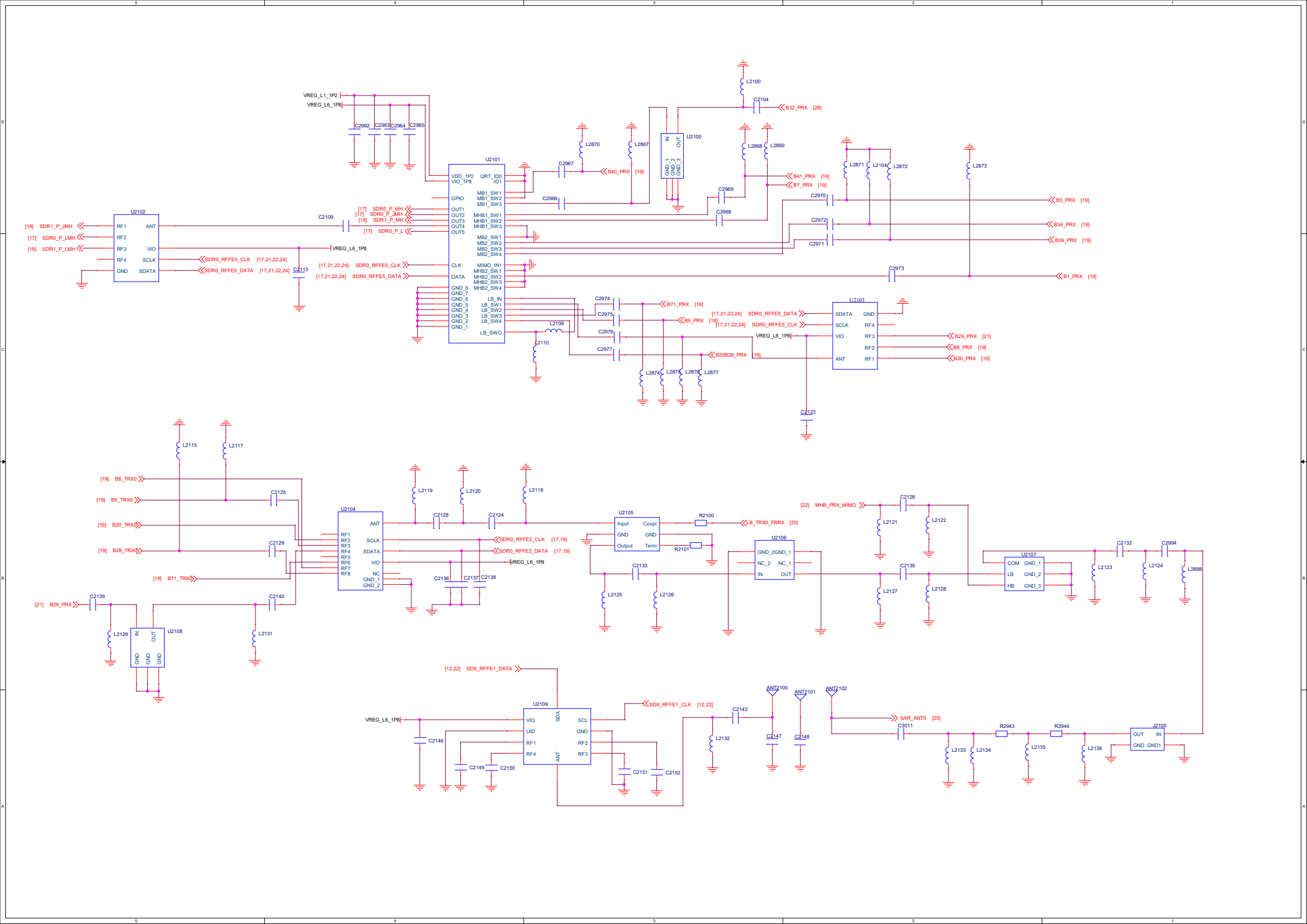
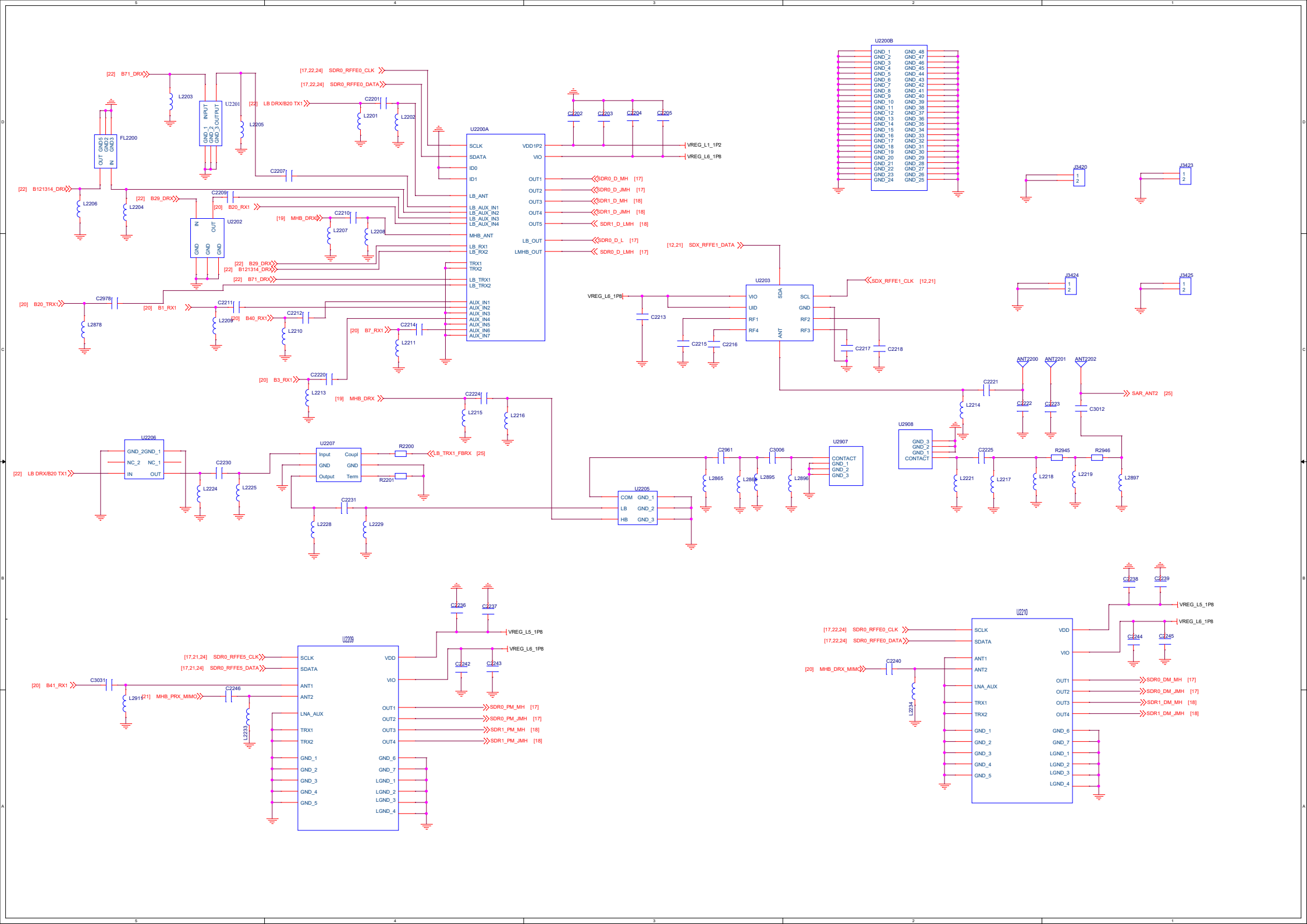
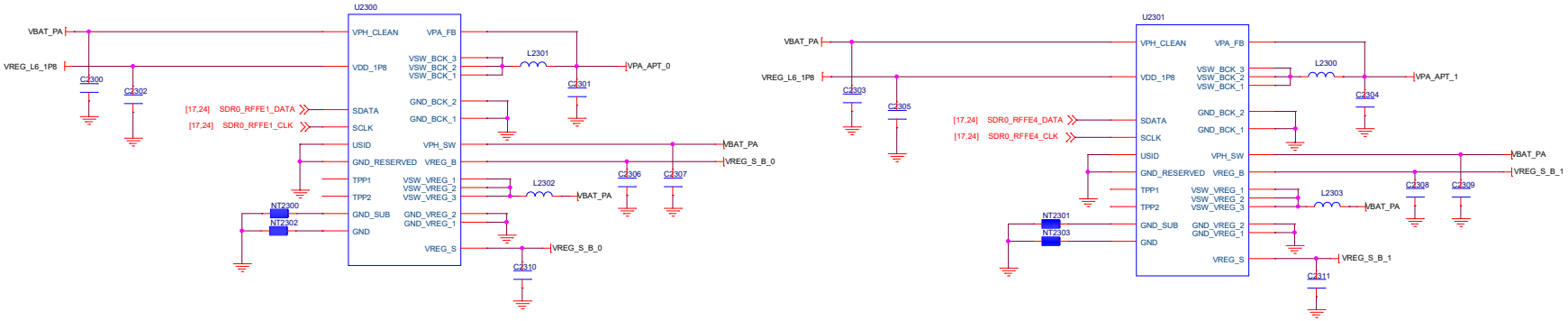
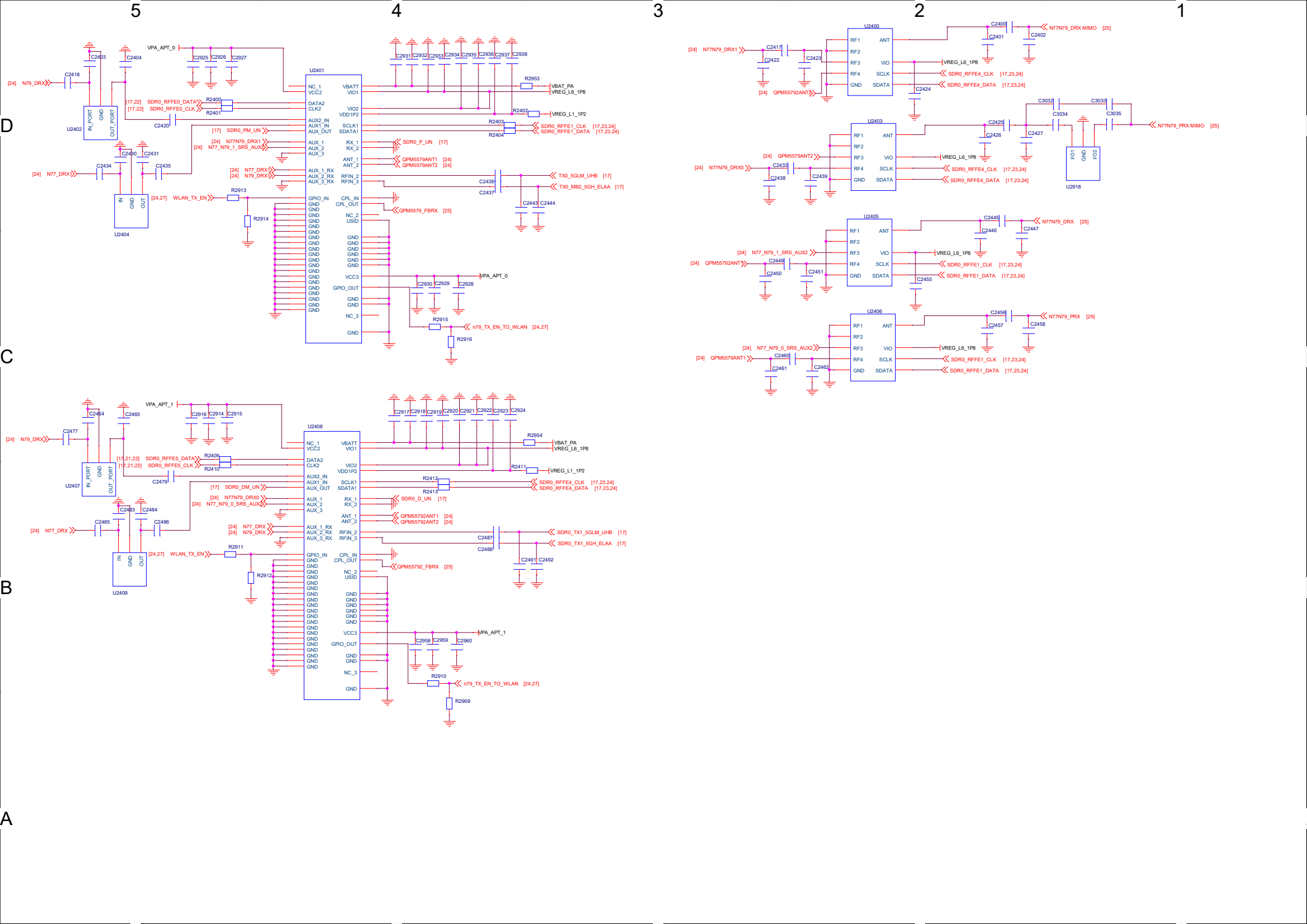
D
C
B
A
U1904A
U2911
U2910
U1902
U1903
U1900
U1904B
U1905
U1906
U1907
U1908
U1909
U2916
U1910
U1911
U1912
U1913
FL1900
FL1901
FL2804
D1900
D1901
D1902
J1900
ANT1900
ANT1901
ANT1902
[25] B41_TRX0_FBRX
[22] MHB_DRX
[22] MHB_DRX0
[20] 3P3T
[25] B40_TRX0_FBRX
[17] SDR0_TX0_HB1
[17] SDR0_TX0_MB1
[17] SDR0_TX0_LB2
[17,19,21] SDR0_RFFE2_DATA
[17,19,21] SDR0_RFFE2_CLK
VREG_L6_1P8
VBAT_PA
VPA_APT_0
[21] B40_PRX
[21] B41_PRX
[21] B39_PRX
[21] B34_PRX
[19] MHB_TRX0
[19] B7_TRX0
[21] B7_PRX
[21] B20_TRX0
[21] B20_PRX
[21] B28_TRX0
[21] B5_TRX0
[21] B5_PRX
[21] B8_TRX0
[21] B8_PRX
[21] B71_TRX0
[21] B71_PRX
[21] B1_PRX
[21] B3_PRX
[17,19,21] SDR0_RFFE2_CLK
[17,19,21] SDR0_RFFE2_DATA
SAR_ANT5 [25]
[25] MB_TRX0_FBRX


R2951
R2952
[25] B41_TRX1_FBRX
U2913
Coupl
GND
Term
Input
GND
Output
L2907
L2906
L2905
[19] 3P3T
C3023
[22] MHB_DRX_MIMO
[25] MHB_DRX1_MIMO
C3022
C3021
U2912
VIO
SCLK
SDATA
USID
RF1
RF2
RF3
RF4
RF5
RF6
GND_1
GND_5
GND_6
GND_4
GND_3
GND_2
NC_1
C2001
L2003
L2002
B41_TRX1 [20]
VREG_L6_1P8
SDR0_RFFE3_CLK [17,19,20]
SDR0_RFFE3_DATA [17,19,20]
C2004
C2002
L2004
L2005
FL2000
IN
GND3
GND2
GND5
OUT
C2003
L2006
L2007
C3019
L2903
C2006
L2010
L2011
FL2001
C2007
L2012
L2013
B40_TRX1 [20]
C2008
L2015
L2016
B7_TRX1 [20]
D2000
ANT
TX
GND3
GND2
RX
GND5
GND4
GND1
B7_RX1 [22]
C2011
C2012
L2017
L2014
U2001A
[17] SDR0_TX1_HB1
C2009
C2010
[17,19,20] SDR0_RFFE3_DATA
[17,19,20] SDR0_RFFE3_CLK
R2000
R2001
VREG_L6_1P8
VBAT_PA
C2013
C2014
C2015
C2016
C2017
C2018
C3024
[17] SDR0_TX1_MB1
C2027
L2020
C2030
C2031
L2026
[17] SDR0_TX1_LB1
HBRX2
HBRX1
GND_HB
GND_HB
HB3
GND_1
GND_2
RFIN_H
GND_3
SDATA
SCLK
VIO
VBATT
NC_1
NC_2
NC_3
RFIN_M
RFIN_L1
RFIN_L2
GND_4
GND_9
HB2
GND_8
HB1
MB5
GND_7
VCC2
VCC1
VCC2_2
GND_6
MB4
MB3
GND
MB2
GND_5
LB4
LB3
LB2
LB1
LB5
MB1
VPA_APT_1
C2020
C2021
C2022
C2023
C2024
C2028
L2021
L2022
C2034
C2033
L2029
L2030
L2031
L2032
B20_TRX1 [22]
U2003
ANT
TX
RX
GND
GND
GND
GND
GND
GND
C2036
L2034
L2035
L2036
B20_RX1 [22]
U2917
TX_B1
TX_B3
GND
ANT
RX_B1
RX_B3
B1_RX1 [22]
B3_RX1 [22]
C2032
C2913
L2027
L2028
L2848
U2002
ANT
RF1
RF2
RF3
RF4
RF5
RF6
RF7
RF8
SCLK
SDATA
VIO
NC
GND_1
GND_2
[20] B41_TRX
[20] B40_TRX
[20] B7_TRX1
C2029
L2024
L2025
SDR0_RFFE3_CLK [17,19,20]
SDR0_RFFE3_DATA [17,19,20]
VREG_L6_1P8
C2035
[22] B40_RX1
C2985
L2882
U2906
INPUT
OUTPUT
GND_1
GND_2
C2988
L2887
[22] B41_RX1
C2987
L2885
U2001B
GND_12
GND_13
GND_14
GND_15
GND_16
GND_17
GND_18
GND_19
GND_20
GND_21
GND_22
GND_23
GND_24
GND_25
[25] MHB_TRX1
C2037
L2037
L2038
C2038
L2039
L2040
U2005
Output
GND
Input
Term
GND
Coupl
U2004
GND_2
GND_1
OUTPUT
INPUT
R2003
R2004
MHB_TRX1_FBRX [25]


VREG_L1_1P2
VREG_L6_1P8
C2962
C2963
C2964
C2965
U2101
VDD_1P2
VIO_1P8
QRT_ID0
ID1
GPIO
MB1_SW1
MB1_SW2
MB1_SW3
OUT1
OUT2
OUT3
OUT4
OUT5
MHB1_SW1
MHB1_SW2
MHB1_SW3
MB2_SW1
MB2_SW2
MB2_SW3
MB2_SW4
CLK
DATA
MIMO_IN1
MHB2_SW1
MHB2_SW2
MHB2_SW3
MHB2_SW4
GND_8
GND_7
GND_6
GND_5
GND_4
GND_3
GND_2
GND_1
LB_IN
LB_SW1
LB_SW2
LB_SW3
LB_SW4
LB_SWO
U2102
RF1
RF2
RF3
RF4
GND
ANT
VIO
SCLK
SDATA
[18] SDR1_P_JMH
[17] SDR0_P_LMH
[18] SDR1_P_LMH
C2109
C2113
[17] SDR0_P_MH
[17] SDR0_P_JMH
[18] SDR1_P_MH
[17] SDR0_P_L
[17,21,22,24] SDR0_RFFE5_CLK
[17,21,22,24] SDR0_RFFE5_DATA
C2967
C2966
C2968
C2969
L2870
L2867
L2868
L2869
U2100
IN
OUT
GND_1
GND_2
GND_3
L2100
C2104
B32_PRX [28]
B40_PRX [19]
B41_PRX [19]
B7_PRX [19]
L2871
L2104
L2872
L2873
C2970
C2972
C2971
B3_PRX [19]
B34_PRX [19]
B39_PRX [19]
C2973
B1_PRX [19]
C2974
C2975
C2976
C2977
L2109
L2110
B71_PRX [19]
B5_PRX [19]
B20B28_PRX [19]
L2874
L2875
L2876
L2877
U2103
SDATA
SCLK
VIO
ANT
GND
RF4
RF3
RF2
RF1
B29_PRX [21]
B8_PRX [19]
B20_PRX [19]
C2123
L2115
L2117
[19] B8_TRX0
[19] B5_TRX0
[19] B20_TRX0
[19] B28_TRX0
[19] B71_TRX0
C2125
C2129
U2104
L2119
L2120
L2118
C2128
C2124
C2136
C2137
C2138
SDR0_RFFE2_CLK [17,19]
SDR0_RFFE2_DATA [17,19]
U2105
Input
Coupl
GND
Output
Term
R2100
R2101
LB_TRX0_FBRX [25]
U2106
GND_2
GND_1
NC_2
NC_1
IN
OUT
C2133
L2125
L2126
[22] MHB_PRX_MIMO
C2126
L2121
L2122
C2135
L2127
L2128
U2107
COM
LB
HB
C2132
C2994
L2123
L2124
L2888
[21] B29_PRX
C2139
C2140
L2129
L2131
U2108
C2146
C2149
C2150
[12,22] SDX_RFFE1_DATA
U2109
VIO
UID
RF1
RF4
SDA
SCL
GND
RF2
RF3
ANT
SDX_RFFE1_CLK [12,22]
C2151
C2152
C2143
L2132
ANT2100
ANT2101
ANT2102
C2147
C2148
SAR_ANT0 [25]
C3011
R2943
R2944
L2133
L2134
L2135
L2136
J2100
OUT
IN
GND
GND1


U2200B
GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14 GND_15 GND_16 GND_17 GND_18 GND_19 GND_20 GND_21 GND_22 GND_23 GND_24
GND_48 GND_47 GND_46 GND_45 GND_44 GND_43 GND_42 GND_41 GND_40 GND_39 GND_38 GND_37 GND_36 GND_35 GND_34 GND_33 GND_32 GND_31 GND_30 GND_29 GND_28 GND_27 GND_26 GND_25
J3420
J3423
J3424
J3425
U2200A
SCLK SDATA ID0 ID1 LB_ANT LB_AUX_IN1 LB_AUX_IN2 LB_AUX_IN3 LB_AUX_IN4 MHB_ANT LB_RX1 LB_RX2 TRX1 TRX2 LB_TRX1 LB_TRX2 AUX_IN1 AUX_IN2 AUX_IN3 AUX_IN4 AUX_IN5 AUX_IN6 AUX_IN7
VDD1P2 VIO OUT1 OUT2 OUT3 OUT4 OUT5 LB_OUT LMHB_OUT
[17,22,24] SDR0_RFFE0_CLK
[17,22,24] SDR0_RFFE0_DATA
[22] B71_DRX
[22] LB DRX/B20 TX1
[22] B121314_DRX
[22] B29_DRX
[20] B20_RX1
[19] MHB_DRX
[20] B20_TRX1
[20] B1_RX1
[20] B40_RX1
[20] B7_RX1
[20] B3_RX1
[22] B71_DRX
VREG_L1_1P2
VREG_L6_1P8
[17,22,24] SDR0_D_MH [17]
[17,22,24] SDR0_D_JMH [17]
[17,22,24] SDR0_D_MH [18]
[17,22,24] SDR0_D_JMH [18]
[17,22,24] SDR1_D_LMH [18]
[17,22,24] SDR0_D_L [17]
[17,22,24] SDR0_D_LMH [17]
FL2200
U2201
U2202
U2203
U2205
U2206
U2207
U2209
U2210
U2907
U2908
[12,21] SDX_RFFE1_DATA
[12,21] SDX_RFFE1_CLK
VREG_L6_1P8
SAR_ANT2 [25]
ANT2200
ANT2201
ANT2202
[22] LB DRX/B20 TX1
LB_TRX1_FBRX [25]
[17,21,24] SDR0_RFFE5_CLK
[17,21,24] SDR0_RFFE5_DATA
[20] B41_RX1
[21] MHB_PRX_MIMO
VREG_L5_1P8
VREG_L6_1P8
SDR0_PM_MH [17]
SDR0_PM_JMH [17]
SDR1_PM_MH [18]
SDR1_PM_JMH [18]
[17,22,24] SDR0_RFFE0_CLK
[17,22,24] SDR0_RFFE0_DATA
[20] MHB_DRX_MIMO
SDR0_DM_MH [17]
SDR0_DM_JMH [17]
SDR1_DM_MH [18]
SDR1_DM_JMH [18]


U2300
VPH_CLEAN
VPA_FB
VDD_1P8
VSW_BCK_3
VSW_BCK_2
VSW_BCK_1
L2301
VPA_APT_0
C2301
GND_BCK_2
GND_BCK_1
SDATA
SCLK
USID
VPH_SW
GND_RESERVED
VREG_B
TPP1
TPP2
VSW_VREG_1
VSW_VREG_2
VSW_VREG_3
L2302
GND_SUB
GND_VREG_2
GND_VREG_1
GND
VREG_S
C2306
C2307
C2310
NT2300
NT2302
VBAT_PA
VREG_L6_1P8
C2300
C2302
[17,24] SDR0_RFFE1_DATA
[17,24] SDR0_RFFE1_CLK
VREG_S_B_0
U2301
C2303
C2305
[17,24] SDR0_RFFE4_DATA
[17,24] SDR0_RFFE4_CLK
L2300
VPA_APT_1
C2304
L2303
C2308
C2309
C2311
NT2301
NT2303
VREG_S_B_1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4
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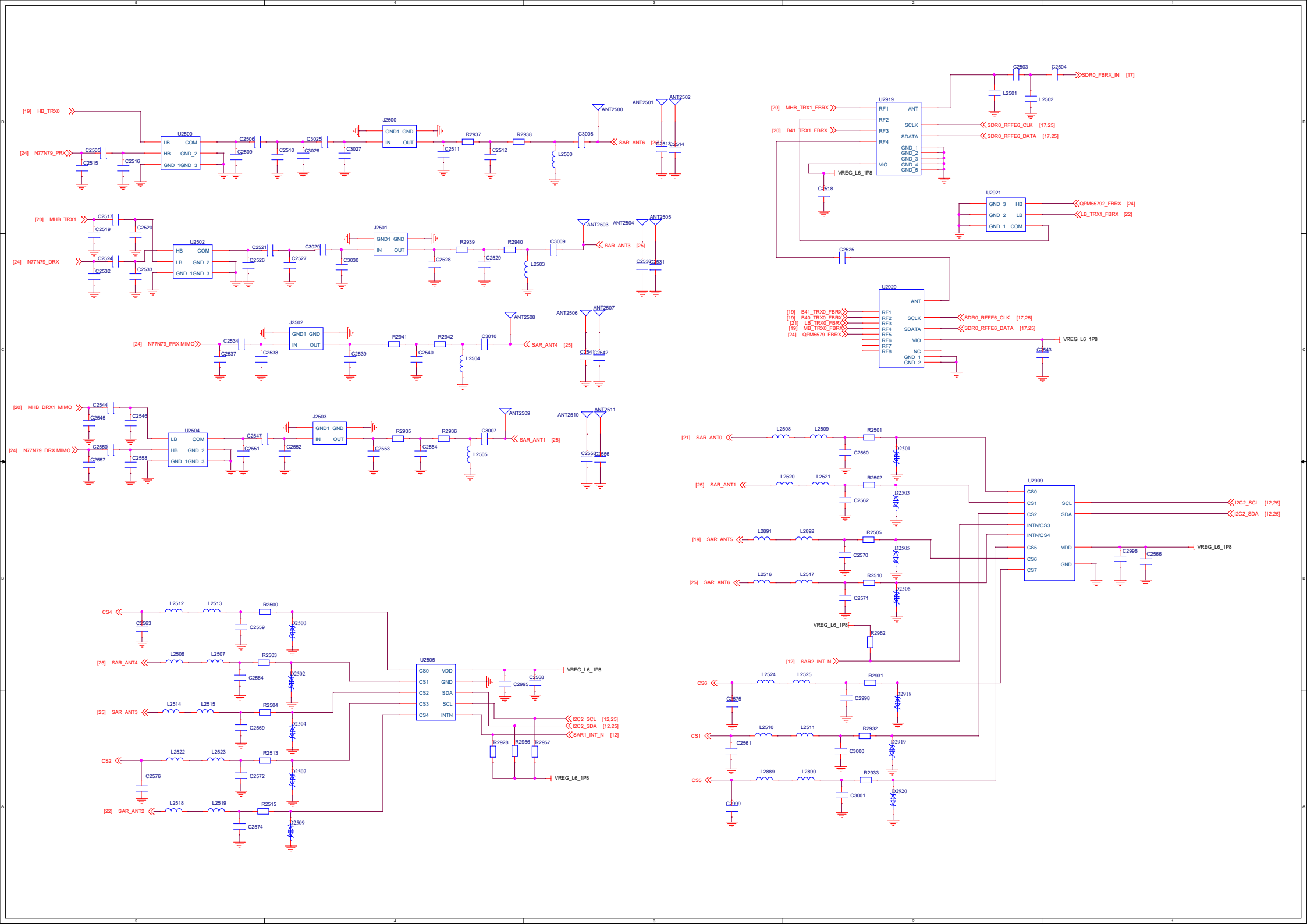
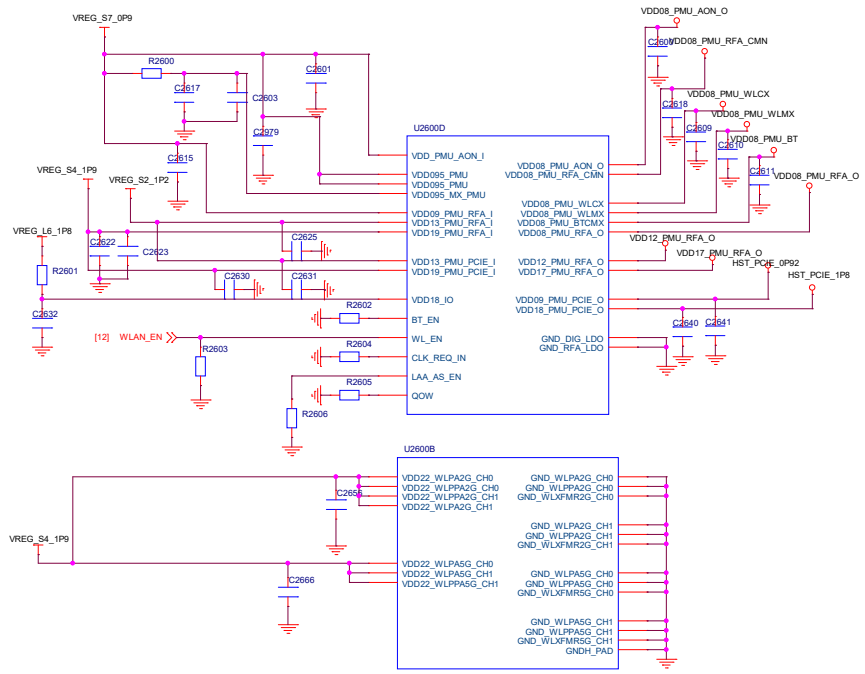
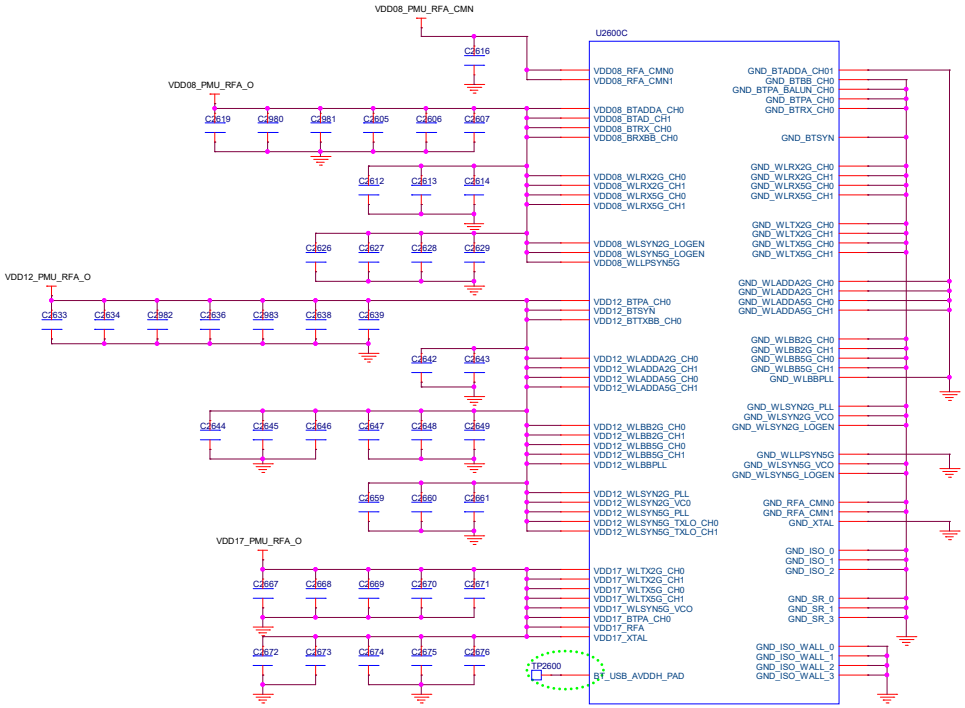
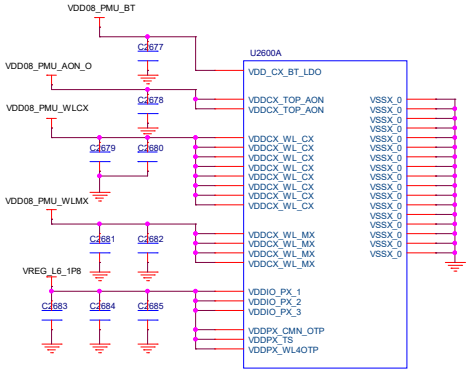
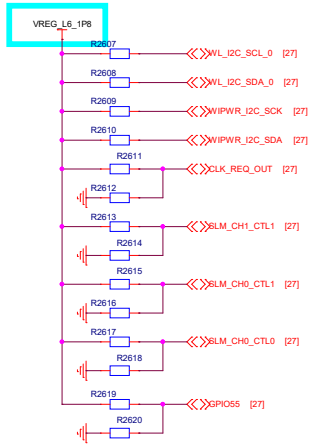
2
1
D
C
B
A
U2401
U2402
U2404
U2400
U2403
U2405
U2406
U2408
U2407
U2409
U2918
VPA_APT_0
VPA_APT_1
VBAT_PA
VREG_L6_1P8
VREG_L1_1P2
WLAN_TX_EN
n79_TX_EN_TO_WLAN
QPM5579_FBRX
QPM55792_FBRX
SDR0_P_UN
SDR0_D_UN
SDR0_PM_UN
SDR0_DM_UN
SDR0_RFFE0_DATA
SDR0_RFFE0_CLK
SDR0_RFFE1_CLK
SDR0_RFFE1_DATA
SDR0_RFFE4_CLK
SDR0_RFFE4_DATA
SDR0_RFFE5_DATA
SDR0_RFFE5_CLK
SDR0_TX1_5GLM_UHB
SDR0_TX1_5GH_ELAA
TX0_5GLM_UHB
TX0_MB2_5GH_ELAA
N77N79_DRX MIMO
N77N79_PRX MIMO
N77N79_DRX
N77N79_PRX
N77N79_DRX1
N77N79_DRX0
N77_N79_1_SRS_AUX
N77_N79_0_SRS_AUX
QPM5579ANT1
QPM5579ANT2
QPM55792ANT1
QPM55792ANT2


[19] HB_TRX0
[24] N77N79_PRX
U2500
LB COM
HB GND_2
GND_1 GND_3
C2505
C2515
C2516
C2506
C2509
C3025
C3026
C2510
C3027
J2500
GND1 GND
IN OUT
C2511
R2937
R2938
C2512
L2500
C3008
ANT2500
SAR_ANT6 [25]
ANT2501
ANT2502
C2513
C2514
[20] MHB_TRX1
[24] N77N79_DRX
U2502
HB COM
LB GND_2
GND_1 GND_3
C2517
C2519
C2520
C2524
C2532
C2533
C2521
C2526
C3029
C2527
C3030
J2501
GND1 GND
IN OUT
C2528
R2939
R2940
C2529
L2503
C3009
ANT2503
SAR_ANT3 [25]
ANT2504
ANT2505
C2530
C2531
[24] N77N79_PRX MIMO
J2502
GND1 GND
IN OUT
C2534
C2537
C2538
C2539
R2941
R2942
C2540
L2504
C3010
ANT2508
SAR_ANT4 [25]
ANT2506
ANT2507
C2541
C2542
[20] MHB_DRX1_MIMO
[24] N77N79_DRX MIMO
U2504
LB COM
HB GND_2
GND_1 GND_3
C2544
C2545
C2546
C2550
C2557
C2558
C2547
C2551
C2552
J2503
GND1 GND
IN OUT
C2553
R2935
R2936
C2554
L2505
C3007
ANT2509
SAR_ANT1 [25]
ANT2510
ANT2511
C2555
C2556
CS4
L2512
L2513
R2500
C2563
C2559
D2500
[25] SAR_ANT4
L2506
L2507
R2503
C2564
D2502
[25] SAR_ANT3
L2514
L2515
R2504
C2569
D2504
CS2
L2522
L2523
R2513
C2576
C2572
D2507
[22] SAR_ANT2
L2518
L2519
R2515
C2574
D2509
U2505
CS0 VDD
CS1 GND
CS2 SDA
CS3 SCL
CS4 INTN
C2995
C2568
VREG_L6_1P8
I2C2_SCL [12,25]
I2C2_SDA [12,25]
SAR1_INT_N [12]
R2928
R2956
R2957
VREG_L6_1P8
[20] MHB_TRX1_FBRX
[20] B41_TRX1_FBRX
U2919
RF1 ANT
RF2
RF3 SCLK
RF4 SDATA
GND_1
GND_2
GND_3
GND_4
GND_5
VIO
VREG_L6_1P8
C2518
C2503
C2504
SDR0_FBRX_IN [17]
L2501
L2502
SDR0_RFFE6_CLK [17,25]
SDR0_RFFE6_DATA [17,25]
U2921
GND_3 HB
GND_2 LB
GND_1 COM
QPM55792_FBRX [24]
LB_TRX1_FBRX [22]
C2525
U2920
ANT
[19] B41_TRX0_FBRX
[19] B40_TRX0_FBRX
[21] LB_TRX0_FBRX
[19] MB_TRX0_FBRX
[24] QPM5579_FBRX
RF1
RF2
RF3
RF4
RF5
RF6
RF7
RF8
SCLK
SDATA
VIO
NC
GND_1
GND_2
SDR0_RFFE6_CLK [17,25]
SDR0_RFFE6_DATA [17,25]
VREG_L6_1P8
C2543
[21] SAR_ANT0
L2508
L2509
R2501
C2560
D2501
[25] SAR_ANT1
L2520
L2521
R2502
C2562
D2503
[19] SAR_ANT5
L2891
L2892
R2505
C2570
D2505
[25] SAR_ANT6
L2516
L2517
R2510
C2571
D2506
VREG_L6_1P8
R2962
[12] SAR2_INT_N
U2909
CS0
CS1
CS2
INTN/CS3
INTN/CS4
CS5
CS6
CS7
SCL
SDA
VDD
GND
I2C2_SCL [12,25]
I2C2_SDA [12,25]
C2996
C2566
VREG_L6_1P8
CS6
L2524
L2525
R2931
C2575
C2998
D2918
CS1
L2510
L2511
R2932
C2561
C3000
D2919
CS5
L2889
L2890
R2933
C3001
D2920
C2999



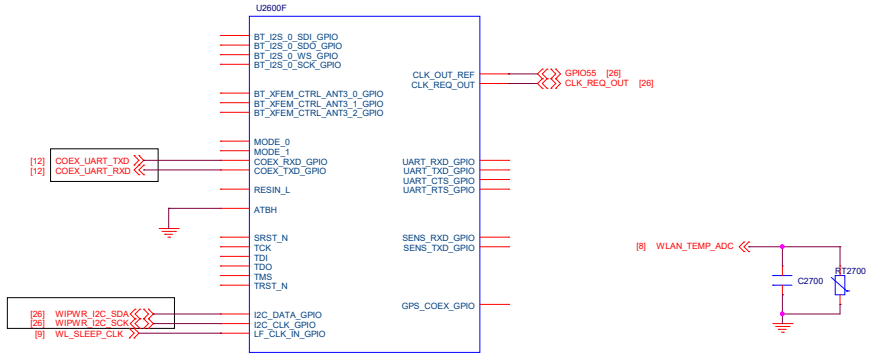


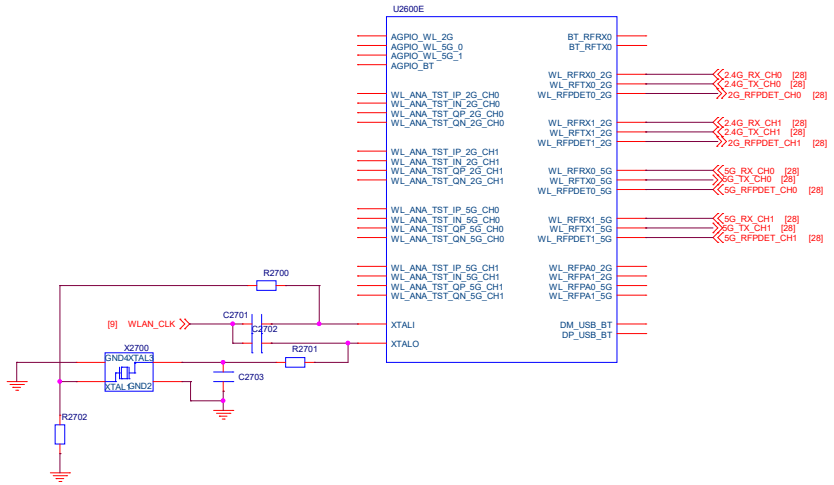


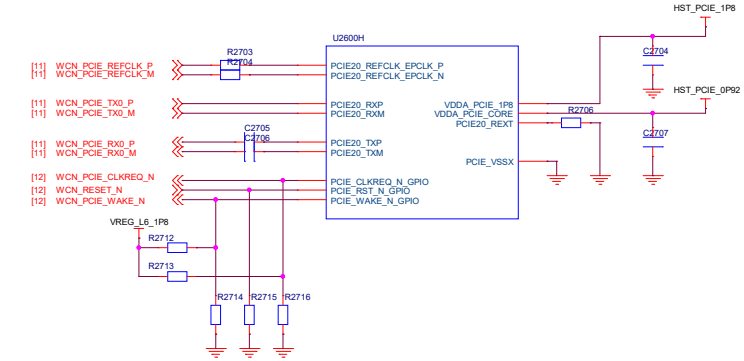


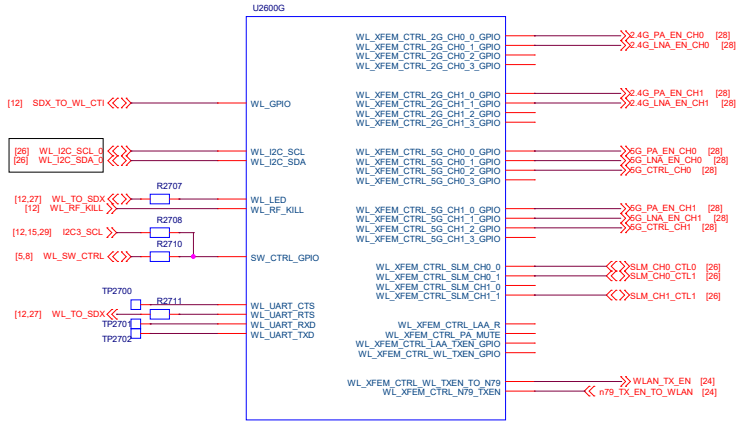
NOTES:
1) FOR REF CLK = 48MHZ: CLK_SEL[1] = 0, CLK_SEL[0] = 0
2) FOR REF CLK = 76.8MHZ: CLK_SEL[1] = 0, CLK_SEL[0] = 1 (DEFAULT)
3) FOR REF CLK = 96MHZ: CLK_SEL[1] = 1, CLK_SEL[0] = 0
4) FOR REF CLK = 38.4MHZ: CLK_SEL[1] = 1, CLK_SEL[0] = 1

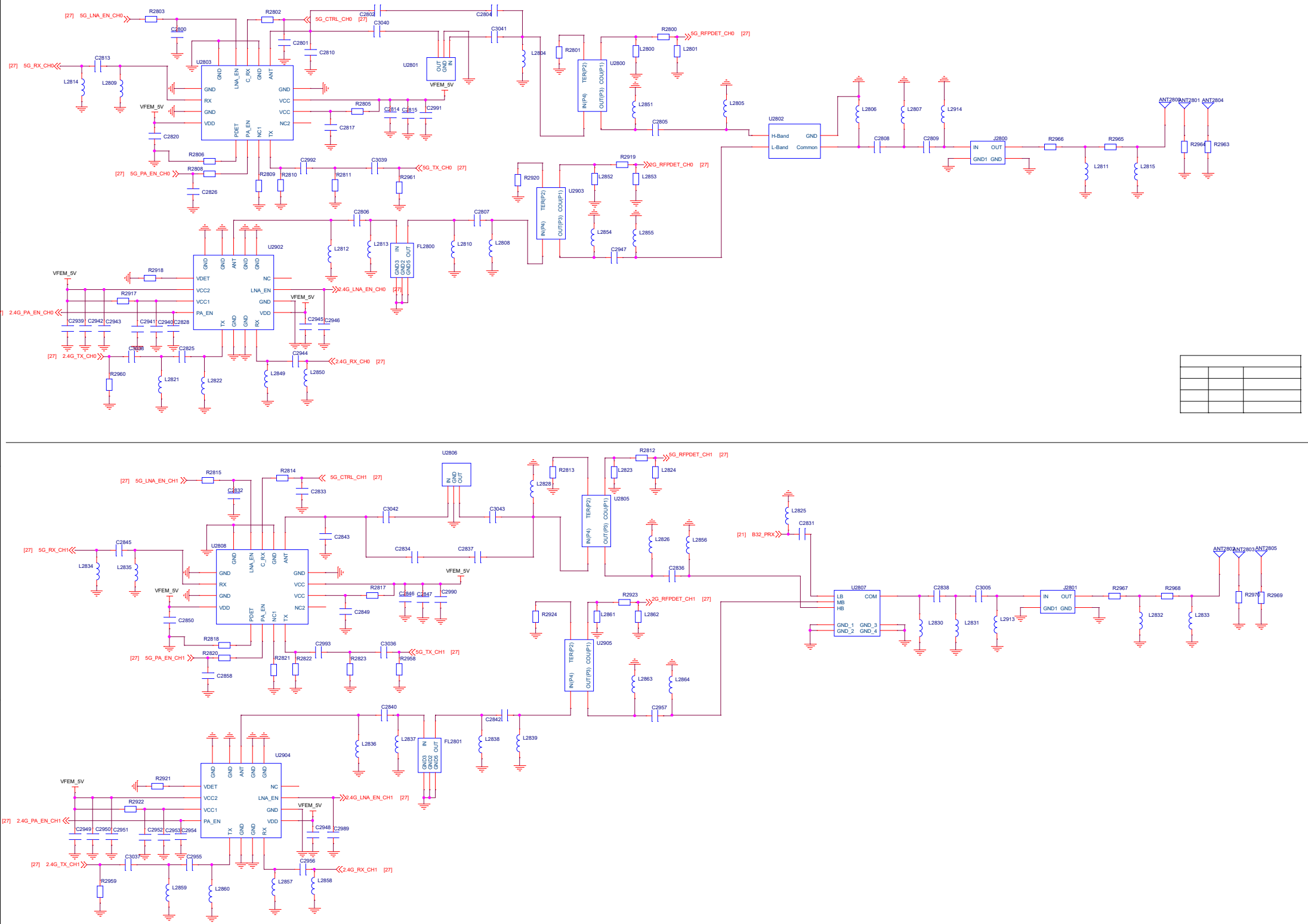
R19	GPIO_39	XO_TCXO_SEL	■ 0: XO ■ 1: TCXO	0


U2600F
BT_I2S_0_SDI_GPIO
BT_I2S_0_SDO_GPIO
BT_I2S_0_WS_GPIO
BT_I2S_0_SCK_GPIO
CLK_OUT_REF
CLK_REQ_OUT
GPIO55 [26]
CLK_REQ_OUT [26]
BT_XFEM_CTRL_ANT3_0_GPIO
BT_XFEM_CTRL_ANT3_1_GPIO
BT_XFEM_CTRL_ANT3_2_GPIO
MODE_0
MODE_1
[12] COEX_UART_TXD
[12] COEX_UART_RXD
COEX_RXD_GPIO
COEX_TXD_GPIO
UART_RXD_GPIO
UART_TXD_GPIO
UART_CTS_GPIO
UART_RTS_GPIO
RESIN_L
ATBH
SRST_N
TCK
TDI
TDO
TMS
TRST_N
SENS_RXD_GPIO
SENS_TXD_GPIO
GPS_COEX_GPIO
[26] WIPWR_I2C_SDA
[26] WIPWR_I2C_SCK
[9] WL_SLEEP_CLK
I2C_DATA_GPIO
I2C_CLK_GPIO
LF_CLK_IN_GPIO
[8] WLAN_TEMP_ADC
C2700
RT2700

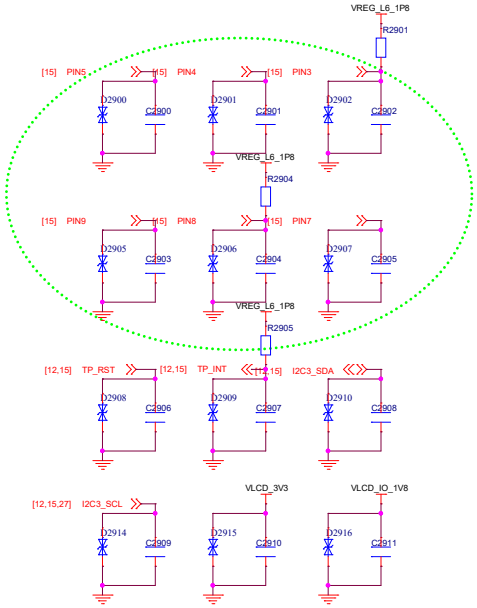

U2600E
AGPIO_WL_2G
AGPIO_WL_5G_0
AGPIO_WL_5G_1
AGPIO_BT
BT_RFRX0
BT_RFTX0
WL_RFRX0_2G
WL_RFTX0_2G
WL_RFPDET0_2G
2.4G_RX_CH0 [28]
2.4G_TX_CH0 [28]
2G_RFPDET_CH0 [28]
WL_ANA_TST_IP_2G_CH0
WL_ANA_TST_IN_2G_CH0
WL_ANA_TST_QP_2G_CH0
WL_ANA_TST_QN_2G_CH0
WL_RFRX1_2G
WL_RFTX1_2G
WL_RFPDET1_2G
2.4G_RX_CH1 [28]
2.4G_TX_CH1 [28]
2G_RFPDET_CH1 [28]
WL_ANA_TST_IP_2G_CH1
WL_ANA_TST_IN_2G_CH1
WL_ANA_TST_QP_2G_CH1
WL_ANA_TST_QN_2G_CH1
WL_RFRX0_5G
WL_RFTX0_5G
WL_RFPDET0_5G
5G_RX_CH0 [28]
5G_TX_CH0 [28]
5G_RFPDET_CH0 [28]
WL_ANA_TST_IP_5G_CH0
WL_ANA_TST_IN_5G_CH0
WL_ANA_TST_QP_5G_CH0
WL_ANA_TST_QN_5G_CH0
WL_RFRX1_5G
WL_RFTX1_5G
WL_RFPDET1_5G
5G_RX_CH1 [28]
5G_TX_CH1 [28]
5G_RFPDET_CH1 [28]
WL_ANA_TST_IP_5G_CH1
WL_ANA_TST_IN_5G_CH1
WL_ANA_TST_QP_5G_CH1
WL_ANA_TST_QN_5G_CH1
WL_RFPA0_2G
WL_RFPA1_2G
WL_RFPA0_5G
WL_RFPA1_5G
XTALI
XTALO
DM_USB_BT
DP_USB_BT
R2700
[9] WLAN_CLK
C2701
C2702
X2700
GND4XTAL3
XTAL GND2
R2701
C2703
R2702

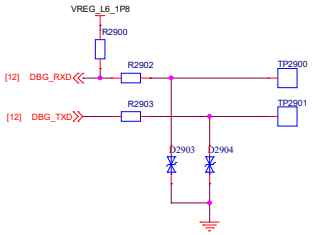

U2600H
HST_PCIE_1P8
HST_PCIE_0P92
[11] WCN_PCIE_REFCLK_P
[11] WCN_PCIE_REFCLK_M
R2703
R2704
PCIE20_REFCLK_EPCLK_P
PCIE20_REFCLK_EPCLK_N
C2704
[11] WCN_PCIE_TX0_P
[11] WCN_PCIE_TX0_M
PCIE20_RXP
PCIE20_RXM
VDDA_PCIE_1P8
VDDA_PCIE_CORE
PCIE20_REXT
R2706
C2707
C2705
C2706
[11] WCN_PCIE_RX0_P
[11] WCN_PCIE_RX0_M
PCIE20_TXP
PCIE20_TXM
PCIE_VSSX
[12] WCN_PCIE_CLKREQ_N
[12] WCN_RESET_N
[12] WCN_PCIE_WAKE_N
PCIE_CLKREQ_N_GPIO
PCIE_RST_N_GPIO
PCIE_WAKE_N_GPIO
VREG_L6_1P8
R2712
R2713
R2714
R2715
R2716

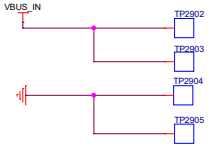

U2600G
WL_XFEM_CTRL_2G_CH0_0_GPIO
WL_XFEM_CTRL_2G_CH0_1_GPIO
WL_XFEM_CTRL_2G_CH0_2_GPIO
WL_XFEM_CTRL_2G_CH0_3_GPIO
2.4G_PA_EN_CH0 [28]
2.4G_LNA_EN_CH0 [28]
[12] SDX_TO_WL_CTI
WL_GPIO
WL_XFEM_CTRL_2G_CH1_0_GPIO
WL_XFEM_CTRL_2G_CH1_1_GPIO
WL_XFEM_CTRL_2G_CH1_2_GPIO
WL_XFEM_CTRL_2G_CH1_3_GPIO
2.4G_PA_EN_CH1 [28]
2.4G_LNA_EN_CH1 [28]
[26] WL_I2C_SCL_0
[26] WL_I2C_SDA_0
WL_I2C_SCL
WL_I2C_SDA
WL_XFEM_CTRL_5G_CH0_0_GPIO
WL_XFEM_CTRL_5G_CH0_1_GPIO
WL_XFEM_CTRL_5G_CH0_2_GPIO
WL_XFEM_CTRL_5G_CH0_3_GPIO
5G_PA_EN_CH0 [28]
5G_LNA_EN_CH0 [28]
5G_CTRL_CH0 [28]
[12,27] WL_TO_SDX
[12] WL_RF_KILL
R2707
WL_LED
WL_RF_KILL
WL_XFEM_CTRL_5G_CH1_0_GPIO
WL_XFEM_CTRL_5G_CH1_1_GPIO
WL_XFEM_CTRL_5G_CH1_2_GPIO
WL_XFEM_CTRL_5G_CH1_3_GPIO
5G_PA_EN_CH1 [28]
5G_LNA_EN_CH1 [28]
5G_CTRL_CH1 [28]
[12,15,29] I2C3_SCL
R2708
[5,8] WL_SW_CTRL
R2710
SW_CTRL_GPIO
WL_XFEM_CTRL_SLM_CH0_0
WL_XFEM_CTRL_SLM_CH0_1
WL_XFEM_CTRL_SLM_CH1_0
WL_XFEM_CTRL_SLM_CH1_1
SLM_CH0_CTL0 [26]
SLM_CH0_CTL1 [26]
SLM_CH1_CTL1 [26]
TP2700
R2711
[12,27] WL_TO_SDX
TP2701
TP2702
WL_UART_CTS
WL_UART_RTS
WL_UART_RXD
WL_UART_TXD
WL_XFEM_CTRL_LAA_R
WL_XFEM_CTRL_PA_MUTE
WL_XFEM_CTRL_LAA_TXEN_GPIO
WL_XFEM_CTRL_WL_TXEN_GPIO
WL_XFEM_CTRL_WL_TXEN_TO_N79
WL_XFEM_CTRL_N79_TXEN
WLAN_TX_EN [24]
n79_TX_EN_TO_WLAN [24]

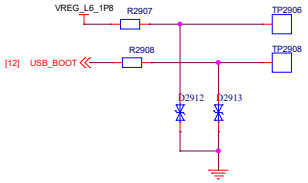

[27] 5G_LNA_EN_CH0
R2803
R2802
5G_CTRL_CH0 [27]
C2802
C2804
C2800
C3040
C3041
C2801
C2810
U2801
OUT GND IN
VFEM_5V
L2804
R2801
R2800
5G_RFPDET_CH0 [27]
U2800
TER(P2) COU(P1) IN(P4) OUT(P3)
L2800
L2801
L2851
C2805
L2805
[27] 5G_RX_CH0
C2813
L2814
L2809
U2803
GND LNA_EN C_RX GND ANT
GND RX GND VDD
GND VCC VCC NC2
PDET PA_EN NC1 TX
R2805
C2814
C2815
C2991
C2817
VFEM_5V
C2820
R2806
[27] 5G_PA_EN_CH0
R2808
C2826
R2809
R2810
C2992
C3039
5G_TX_CH0 [27]
R2811
R2961
U2802
H-Band GND
L-Band Common
L2806
L2807
L2914
C2808
C2809
J2800
IN OUT
GND1 GND
R2966
R2965
L2811
L2815
ANT2800
ANT2801
ANT2804
R2964
R2963
R2920
R2919
2G_RFPDET_CH0 [27]
U2903
TER(P2) COU(P1) IN(P4) OUT(P3)
L2852
L2853
L2854
L2855
C2947
C2806
C2807
L2812
L2813
FL2800
GND3 GND2 GND5 IN OUT
L2810
L2808
U2902
GND GND ANT GND GND
VDET NC
VCC2 LNA_EN
VCC1 GND
PA_EN VDD
TX GND GND RX
VFEM_5V
R2918
R2917
[27] 2.4G_PA_EN_CH0
2.4G_LNA_EN_CH0 [27]
C2939
C2942
C2943
C2941
C2940
C2828
C2945
C2946
C2944
[27] 2.4G_TX_CH0
C2838
C2825
2.4G_RX_CH0 [27]
R2960
L2821
L2822
L2849
L2850

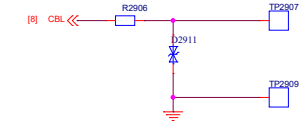
U2806
IN GND OUT
R2815
R2814
[27] 5G_LNA_EN_CH1
5G_CTRL_CH1 [27]
C2832
C2833
C3042
C3043
C2843
C2834
C2837
R2813
L2828
R2812
5G_RFPDET_CH1 [27]
L2823
L2824
U2805
TER(P2) COU(P1) IN(P4) OUT(P5)
L2826
L2856
C2836
L2825
C2831
[21] B32_PRX
[27] 5G_RX_CH1
C2845
L2834
L2835
U2808
GND LNA_EN C_RX GND ANT
GND RX GND VDD
GND VCC VCC NC2
PDET PA_EN NC1 TX
VFEM_5V
R2817
C2846
C2847
C2990
C2849
C2850
R2818
R2820
[27] 5G_PA_EN_CH1
C2858
R2821
R2822
C2993
C3036
R2823
R2958
5G_TX_CH1 [27]
R2924
R2923
2G_RFPDET_CH1 [27]
U2905
TER(P2) COU(P1) IN(P4) OUT(P5)
L2861
L2862
L2863
L2864
C2957
U2807
LB COM MB HB GND_1 GND_3 GND_2 GND_4
C2838
C3005
L2830
L2831
L2913
J2801
IN OUT GND1 GND
R2967
R2968
L2832
L2833
ANT2802
ANT2803
ANT2805
R2970
R2969
C2840
C2842
L2836
L2837
FL2801
GND3 GND2 GND5 IN OUT
L2838
L2839
U2904
GND GND ANT GND GND
VDET NC
VCC2 LNA_EN
VCC1 GND
PA_EN VDD
TX GND GND RX
VFEM_5V
R2921
R2922
[27] 2.4G_PA_EN_CH1
2.4G_LNA_EN_CH1 [27]
C2949
C2950
C2951
C2952
C2953
C2954
C2948
C2989
C3037
C2955
C2956
[27] 2.4G_TX_CH1
2.4G_RX_CH1 [27]
R2959
L2859
L2860
L2857
L2858

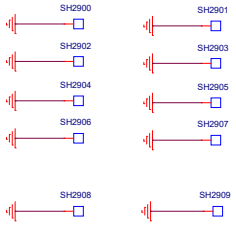

VREG_L6_1P8
R2901
[15] PIN5
[15] PIN4
[15] PIN3
D2900
C2900
D2901
C2901
D2902
C2902
VREG_L6_1P8
R2904
[15] PIN9
[15] PIN8
[15] PIN7
D2905
C2903
D2906
C2904
D2907
C2905
VREG_L6_1P8
R2905
[12,15] TP_RST
[12,15] TP_INT
[12,15] I2C3_SDA
D2908
C2906
D2909
C2907
D2910
C2908
VLCD_3V3
VLCD_IO_1V8
[12,15,27] I2C3_SCL
D2914
C2909
D2915
C2910
D2916
C2911


VREG_L6_1P8
R2900
[12] DBG_RXD
R2902
TP2900
[12] DBG_TXD
R2903
TP2901
D2903
D2904


VBUS_IN
TP2902
TP2903
TP2904
TP2905


VREG_L6_1P8
R2907
TP2906
[12] USB_BOOT
R2908
TP2908
D2912
D2913


[8] CBL
R2906
TP2907
D2911
TP2909


SH2900
SH2901
SH2902
SH2903
SH2904
SH2905
SH2906
SH2907
SH2908
SH2909


MARK2900
MARK2901
MARK2902
MARK2903
MARK2904
MARK2905
MARK2906
MARK2907