

TURBOX™ C40X SOM DATASHEET

Thundercomm Confidential

Thunder**comm**

Version	Date	Description
V0.1	2019-11-01	Initial Version
V0.2	2020-02-01	1.Added TurboX™C405 information and updated SoM pin definitions. 2. Added descriptions of HDMI, MIPI DSI, DECAP, Sleep Clock and SPMI interfaces.
V0.3	2020-02-06	1.SoM marking 5-3 2.Content for Figures and Tables
V0.5	2020-02-20	Update in 4.16.2 BT Performance
V0.6	2020-02-26	Update in 4.16.2 BT Performance
V0.7	2020-03-16	Update in 5.2 Package dimensions
V0.8	2020-03-27	Update SDC2 performance description
V0.9	2020-09-16	Correct the description error of the Bluetooth version.
V1.0	2020-10-15	1.Add C403 information. 2.Update the pin definition of SoM.
V1.1	2020-11-23	Fix the inconsistency of LDO output current description, such as LDO6 and LDO7.
V1.2	2020-12-29	Delete the description about FM.
V1.3	2021-01-14	Delete the description about BT2.
V1.4	2021-01-30	Update current consumption data.

Contents

1 Overview.....	6
1.1 TurboX™ C40x Module Abstract.....	6
1.2 Reference Documents.....	6
1.3 Terms and Acronyms.....	6
2 TurboX™ C40x SoM Introduction.....	9
2.1 Key features.....	9
2.2 Hardware Block Diagram.....	12
2.3 TurboX™ C40x Major Components Location.....	13
3 Interfaces Description.....	13
3.1 Interfaces Parameter Definitions.....	14
3.2 Pin Description.....	15
3.3 Interfaces Detail Description.....	23
3.3.1 Power Supply Interface.....	23
3.3.2 RGMII Interfaces.....	24
3.3.3 SPDIF Interface.....	24
3.3.4 Audio Interface.....	24
3.3.5 USB Interface.....	27
3.3.6 PCIe Interface.....	27
3.3.7 MIPI DSI Interface.....	28
3.3.8 HDMI Interface.....	28
3.3.9 JTAG Interface.....	29
3.3.10 SDIO Interface.....	29
3.3.11 BLSP Interface.....	30
3.3.12 Power On Interface.....	31
3.3.13 Reset Interface.....	31
3.3.14 Boot Configuration Interface.....	32

3.3.15 Debug UART Interface.....	34
3.3.16 PWM.....	34
3.3.17 Sleep Clock.....	34
3.3.18 SPML.....	35
3.3.19 Antenna Interface.....	35
4 Electrical Characteristics.....	36
4.1 Absolute Maximum Ratings.....	36
4.2 Operating Conditions.....	36
4.3 Output Power.....	36
4.4 Digital-logic characteristics.....	37
4.4.1 Digital GPIO characteristics.....	37
4.4.2 SD card digital I/O characteristics.....	37
4.5 USB.....	39
4.6 SLIMbus.....	39
4.7 I2S.....	40
4.8 PDM.....	42
4.9 I2C.....	43
4.10 SPI.....	43
4.11 Current Sink.....	44
4.12 Sleep Clock.....	44
4.13 SPML.....	44
4.14 MIPI DSI.....	45
4.15 Power Consumption.....	45
5 Mechanical Size.....	46
5.1 Mechanical Size.....	46
5.2 Package dimensions.....	47
5.3 SoM Marking.....	48
6 SMT Assembly Guide.....	49

Figure

Figure 2-1 TurboX™ C40x SoM Hardware System Block Diagram.....	12
Figure 2-2 TurboX™ C40x SoM.....	13
Figure 3-1 TurboX™ C40x PIN Map (Top View).....	15
Figure 3-3 Audio.....	25
Figure 3-4 Power on signal.....	31
Figure 3-5 Power on signal.....	33
Figure 5-1 Top View.....	46
Figure 5-2 Side View.....	46
Figure 5-3 Bottom View.....	46
Figure 5-4 package dimensions.....	47
Figure 5-5 SOM print.....	48

Table

Table 2-1 Connector part number and information.....	13
Table 3-1 Interfaces parameter definitions.....	15
Table 3-2 Power supply definition.....	23
Table 3-4 RGMII interface definition.....	24
Table 3-5 SPDIF interface definition.....	24
Table 3-6 Audio interface definition.....	25
Table 3-7 USB interface definition.....	27
Table 3-8 PCIe interface definition.....	28
Table 3-9 MIPI DSI interface definition.....	28
Table 3-10 HDMI interface definition.....	28

Table 3- 11	SSC interface definition.....	29
Table 3- 12	SDIO interface definition.....	29
Table 3- 13	BLSP interface definition.....	30
Table 3- 14	Power on interface definition.....	31
Table 3- 15	Reset interface definition.....	32
Table 3- 16	Sensor interrupt definition.....	33
Table 3- 17	Debug UART interface definition.....	34
Table 3- 18	PWM definition.....	34
Table 3- 19	SLEEP_CLK definition.....	35
Table 3- 20	SPMI definition.....	35
Table 3- 21	Antenna interface definition.....	35
Table 4- 1	Absolute rating condition.....	36
Table 4- 2	Operating condition.....	36
Table 4- 3	Output power.....	37
Table 4- 4	digital IO voltage performance.....	37
Table 4- 5	SD digital IO voltage performance (1.8V/2.95V).....	38
Table 4- 6	SDIO.....	38
Table 4- 7	USB.....	39
Table 4- 8	SLIMbus.....	40
Table 4- 9	I2S.....	41
Table 4- 10	I2C.....	43
Table 4- 11	Current sink specification.....	44
Table 4- 12	Current sink specification.....	44
Table 4- 13	Sleep Clock specification.....	44
Table 4- 14	SPMI standard.....	45
Table 4- 15	MIPI DSI standard.....	45
Table 4- 16	Power Consumption.....	46
Table 5- 1	SOM Marking.....	49

1 Overview

1.1 TurboX™ C40x Module Abstract

TurboX™ C40x is high level performance intelligent module, integrating Android or Linux system, based on Qualcomm QCS40x processor. It includes a 64-bit Arm Cortex-A53 qual-core (dual-core for C403) 1.4 GHz application processor, two Qualcomm® Hexagon™ QDSP6 v66 with Low Power Island and Voice accelerators.

TurboX™ C40x integrated 2 × 2 (or 1 × 1) WLAN 802.11 a/b/g/n/ac, Bluetooth v5.x specification.

TurboX™ C40x provides a variety of GPIO, I2C, UART and SPI standard interfaces. In addition, SoM common standard protocol interfaces such as USB3.0, USB2.0, SPI, RGMII, I2S and SLIMBUS.

TurboX™ C40x provide convenient and stable system software solution for use in the Smart Speaker, Smart Assistant, Mesh router, and Soundbar markets.

The size of TurboX™ C40x module is 33.8mm*33.8mm*2.6mm, weight 18g, with 287PINs.

1.2 Reference Documents

Document
80-YB403-1 QCS403 NSP DATA SHEET
80-YB404-1 QCS404 NSP DATA SHEET
80-YB405-1 QCS405 NSP DATA SHEET
80- YB405-1 SOM1 REFERENCE SCHEMATIC
80-YB406-1 PM405 WLNSP POWER MANAGEMENT DATA SHEET

1.3 Terms and Acronyms

Acronym/Terminology	Description
ADC	Analog-to-digital converter
BER	Bit error rate
BLSP	BAM-based low-speed peripheral
eMMC	Embedded Multimedia Card

GPIO	General Purpose Input/output
EBI	External bus interface
GNSS	Global navigation satellite system
HDMI	High-Definition Multimedia Interface
LPDDR	Low Power Double Data Rate
LPI	Low Power Island
LCD	Liquid crystal display
MIPI-DSI	Mobile Industry Processor Interface Display Serial Interface
NFC	Near field communicator
PMIC	Power Management Integrated Circuit
OSC	Oscillator
PA	Power amplifier
PCB	Printed circuit board
PCIe	Peripheral component interconnect express
PCM	Pulse-coded modulation
PM	Power management
PWM	Pulse width modulation
SDC	Secure digital controller
SDRAM	Synchronous dynamic random access memory
SLIMbus	Serial Low-power Inter-chip Media Bus
SPI	Serial peripheral interface
SPMI	Serial power management interface
TCXO	Temperature-compensated crystal oscillator
SoC	System on Chip
XTAL	Crystal
SDIO	Secure Digital Input / Output
UART	Universal Asynchronous Receiver Transmitter

USB	Universal serial bus
I2S	Inter-IC Sound
I2C	Inter-integrated circuit
WCN	Wireless connectivity network
WLAN	Wireless local area network
SMPS	Switched-mode power supply
SOM	System On Module
RGMII	Reduced gigabit media-independent interface

2 TurboX™ C40x SoM Introduction

2.1 Key features

The following table shows the detailed features and performance on TurboX™ C404 TurboX™ C405 and TurboX™ C403.

Processors	
Applications Processor	Arm Cortex-A53 microprocessor cores, 64-bit processor, Quad-core (Dual-core for C403) 1.4 GHz,
Digital signal processing	Two Qualcomm® Hexagon™ QDSP6 v66 with Low Power Island and Voice accelerators
Operating System	LE(Linux Enablement): QCS40X_2019.SPF.1.1
Memory	eMCP,8GB eMMC5.1+8Gb LPDDR3 eMCP,4GB eMMC + LPDDR3 512GB (validating)
Multimedia	
Display support	TurboX™ C404 and TurboX™ C403 General display interfaces: SPI TurboX™ C405 General display interfaces: One 4-lane MIPI DSI ports, DSI support up to 720P, HDMI support up to 1080p 30fps, SPI. Graphics: Adreno 306 at 600 MHz.
Video	
Audio	MP3, AAC, ALAC, FLAC, He-AAC v1/v2, WMA 9/Pro, Dolby Digital, Dolby Digital Plus, Dolby TruHD, DTS:X
Wireless connectivity	

WLAN	2.4G/5G, support 802.11 a/b/g/n/ac, 2 X 2 MIMO(WCN3999) 2.4G/5G, support 802.11 a/b/g/n/ac, 1 X 1 MIMO(WCN3980) Support SoAP mode
Bluetooth	Support Bluetooth 5.x + HS BLE, Backwards compatible with Bluetooth 1.2, 2.X + enhanced data rate.
Connectivity	
USB	one USB 2.0 high-speed and one USB 3.0 super-speed
PCIe	1x PCIe, PCIe v2 PHY and 2.1 controller
Ethernet RGMII	1x Ethernet RGMII
SDIO	4-bit, SD 3.0 SDC2 is dual-V SD/MMC card, eMMC NAND, eSD/eMMC boot
BLSP	Can be configured as 2x SPI or 3x I2C or 5x UART
UART	up to 4 MHz
I2C	Sensors etc
SPI	Sensors etc
SLIMbus	One, highly multiplexed, high-speed, baseline WCD9335
MI2S	Full duplex stereo or up to quad channel Tx/Rx MI2S (x1) Up to 2 channel for multi-channel audio applications (x1)
PCM	Short and long sync PCM support.
Sleep Clock	32.768 KHz sleep clock.
SPMI	Dedicated power management interface for external charging system.
GPIOs	10+ GPIO, LPI GPIO and PM GPIO ports.

Other	
ADC Interface	Support ADC interfaces used for input voltage sense, battery temperature detection and general purpose ADC
Touchscreen support	Capacitive panels via ext IC (I2C, SPI, and interrupts)
Physical size	Size: 33.8mm x 33.8mm x 2.6mm Weight: approx.18g
Working temperature	-20° C ~ +70° C
RoHS	All hardware components are fully compliant with EU RoHS directive

2.2 Hardware Block Diagram

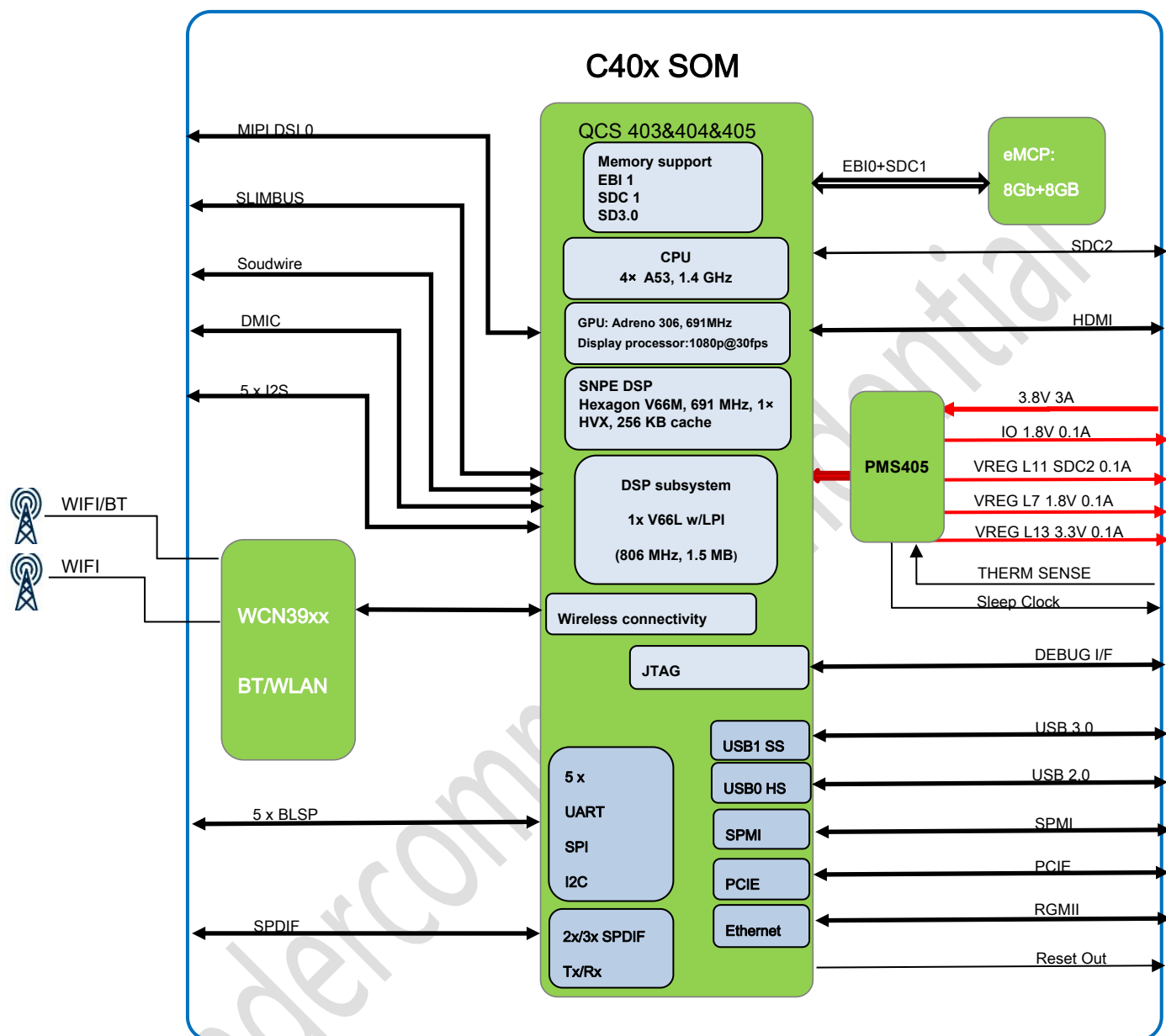


Figure 2- 1 TurboX™ C40x SoM Hardware System Block Diagram

2.3 TurboX™ C40x Major Components Location

TurboX™ C40x major components as below map.

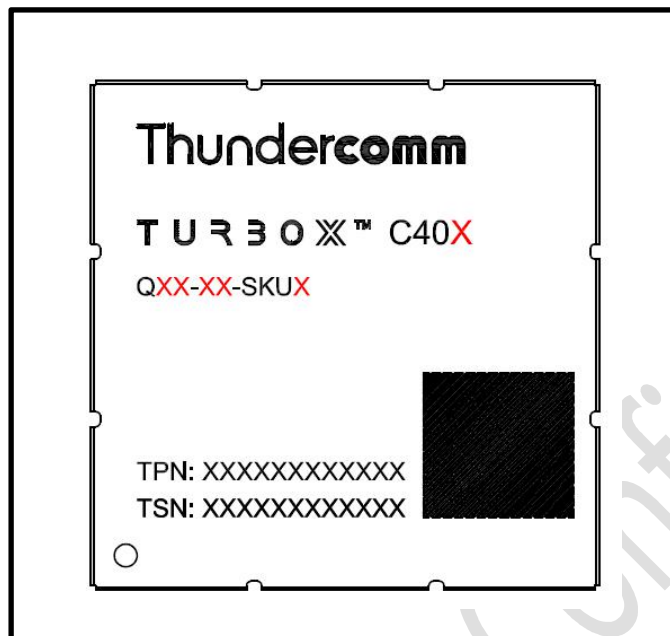


Figure 2- 2 TurboX™ C40x SoM

Below table indicates connectors detail information.

Part Reference	Description	Manufacturer
U500	QCS403/404/405, Arm cortex-A53 processor.	QUALCOMM
U1100	PMS405, power management.	QUALCOMM
U1300	WCN3999 or WCN3980, single-die wireless local area network.	QUALCOMM
U1200	eMMC+ LPDDR3 memory.	

Table 2- 1 Connector part number and information

3 Interfaces Description

This chapter introduces all the interfaces definition, purpose to guide developer easy to design and verification on TurboX™ C40x SoM module.

3.1 Interfaces Parameter Definitions

Symbol	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
DI	Digital input(CMOS)
DSI	Supply voltage for MIPI_DSI I/Os; tied to VDD_MIPi (1.2 V only)
DO	Digital output(CMOS)
H	High-voltage tolerant
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
MIPI	Mobile industry processor interface
NP	Contains no internal pull
OD	Open drain
PD	Contains an internal pull-down device
PI	Power input
PO	Power output
PD	Contains an internal pull-down device
PU	Contains an internal pull-up device
P3	Power group 3, it is 1.8V.
P2	SDC Power group 2, it is 1.8V or 2.95V.
P12	SSC Power group 12, it is 1.8V.

V_Internal	Internally generated supply voltage for some power-on circuits
V_Config	Software configurable (3.6V or 1.8V)

Table 3- 1 Interfaces parameter definitions

3.2 Pin Description

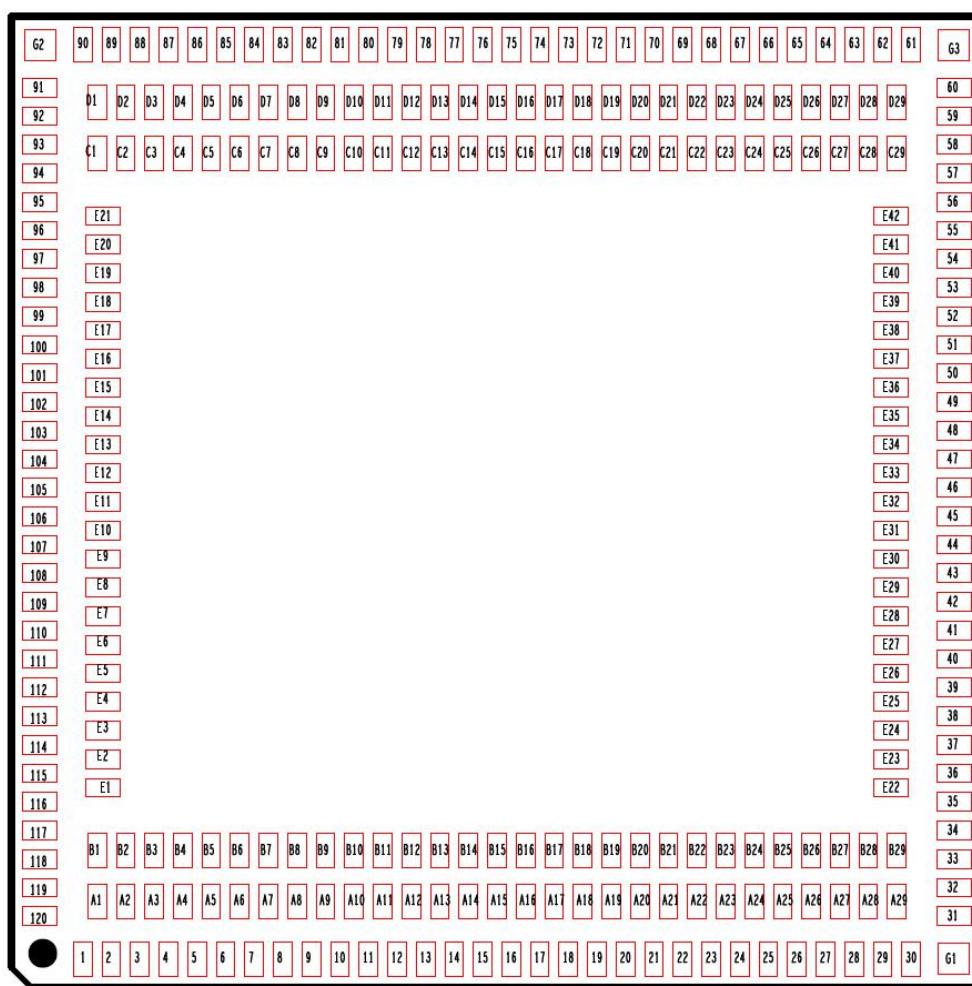


Figure 3- 1 TurboX™ C40x PIN Map (Top View)

Pad#	Function	Voltage	Type	Function description
1	MIPI_DSIO_CLK_M			MIPI display serial interface 0 clock negative. For TurboX™ C404 do not connect.
2	MIPI_DSIO_CLK_P			MIPI display serial interface 0 clock positive. For TurboX™ C404 do not connect.
3	GND			
4	MIPI_DSIO_L2_M			MIPI display serial interface 0 lane 2 negative For TurboX™ C404 do not connect.

5	MIPI_DSI0_L2_P			MIPI display serial interface 0 lane 2 positive. For TurboX™ C404 do not connect.
6	GND			
7	MIPI_DSI0_L3_M			MIPI display serial interface 0 lane 3 negative For TurboX™ C404 do not connect.
8	MIPI_DSI0_L3_P			MIPI display serial interface 0 lane 3 positive. For TurboX™ C404 do not connect.
9	GND			
10	PCIE0_TX_P	/	DO	PCIE transmitter plus
11	PCIE0_TX_M	/	DO	PCIE transmitter minus
12	GND			
13	USB0_HS_DM	/	IO	USB0 HS data minus
14	USB0_HS_DP	/	IO	USB0 HS data plus
15	GND			
16	GPIO_35	1.8V	IO	Can be configured as GPIO
17	GPIO_34	1.8V	IO	Can be configured as GPIO
18	GND			
19	SPDIF_RX_COAX_RCA	/	DI	SPDIF receive port for electrical input
20	SPDIF_RX_COAX_EP	/	DI	SPDIF receive port for optical input
21	GND			
22	GPIO_26	1.8V	IO	Can be configured as GPIO
23	GPIO_27	1.8V	IO	Can be configured as GPIO
24	GPIO_28	1.8V	IO	Can be configured as GPIO
25	GPIO_29	1.8V	IO	Can be configured as GPIO
26	GND			
27	GPIO_39	1.8V	IO	Can be configured as GPIO
28	GPIO_40	1.8V	IO	Can be configured as GPIO
29	GPIO_41	1.8V	IO	Can be configured as GPIO
30	GPIO_42	1.8V	IO	Can be configured as GPIO
31	GND			
32	LPI_GPIO_1	1.8V	IO	Can be configured as GPIO
33	LPI_GPIO_2	1.8V	IO	Can be configured as GPIO
34	LPI_GPIO_3	1.8V	IO	Can be configured as GPIO
35	LPI_GPIO_4	1.8V	IO	Can be configured as GPIO
36	GND			
37	LPI_GPIO_15	1.8V	IO	Can be configured as GPIO
38	LPI_GPIO_14	1.8V	IO	Can be configured as GPIO
39	LPI_GPIO_13	1.8V	IO	Can be configured as GPIO
40	LPI_GPIO_12	1.8V	IO	Can be configured as GPIO
41	LPI_GPIO_11	1.8V	IO	Can be configured as GPIO
42	GND			
43	GPIO_97	1.8V	IO	Can be configured as GPIO
44	GPIO_98	1.8V	IO	Can be configured as GPIO

45	GPIO_99	1.8V	IO	Can be configured as GPIO
46	GPIO_100	1.8V	IO	Can be configured as GPIO
47	GPIO_101	1.8V	IO	Can be configured as GPIO
48	GPIO_102	1.8V	IO	Can be configured as GPIO
49	GND			
50	ANT_WL_Chain 1		RF IO	Antenna port for WIFI Tx/Rx chain 1
51	GND			
52	GND			
53	NC		-	-
54	GND			
55	GND			
56	NC			
57	GND			
58	GND			
59	ANT_WL_Chain 0		RF IO	Antenna port for WIFI Tx/Rx chain 0
60	GND			
61	GND			
62	GND			
63	GND			
64	GPIO_30	1.8V	IO	Can be configured as GPIO
65	GPIO_31	1.8V	IO	Can be configured as GPIO
66	GPIO_32	1.8V	IO	Can be configured as GPIO
67	GPIO_33	1.8V	IO	Can be configured as GPIO
68	GND			
69	GPIO_37	1.8V	IO	Can be configured as GPIO
70	GPIO_38	1.8V	IO	Can be configured as GPIO
71	GND			
72	GND			
73	GND			
74	VPH_PWR	3.8V	PI	Power supply input for SoM all operations.
75	VPH_PWR	3.8V	PI	Power supply input for SoM all operations.
76	VPH_PWR	3.8V	PI	Power supply input for SoM all operations.
77	GND			
78	GND			
79	GND			
80	VPH_PWR	3.8V	PI	Power supply input for SoM all operations.
81	VPH_PWR	3.8V	PI	Power supply input for SoM all operations.
82	VPH_PWR	3.8V	PI	Power supply input for SoM all operations.
83	VPH_PWR	3.8V	PI	Power supply input for SoM all operations.
84	GND			
85	GND			
86	GND			
87	VPH_PWR	3.8V	PI	Power supply input for SoM all operations.

88	VPH_PWR	3.8V	PI	Power supply input for SoM all operations.
89	VPH_PWR	3.8V	PI	Power supply input for SoM all operations.
90	VREG_L6_1P8	1.8V	PO	Low voltage switch supply output 1.8V for IO and pull up voltage;
91	GPIO_116	1.8V	IO	Can be configured as GPIO
92	GPIO_115	1.8V	IO	Can be configured as GPIO
93	GPIO_114	1.8V	IO	Can be configured as GPIO
94	GPIO_113	1.8V	IO	Can be configured as GPIO
95	GPIO_112	1.8V	IO	Can be configured as GPIO
96	GPIO_111	1.8V	IO	Can be configured as GPIO
97	GPIO_110	1.8V	IO	Can be configured as GPIO
98	LPI_GPIO_18	1.8V	IO	Can be configured as GPIO
99	LPI_GPIO_19	1.8V	IO	Can be configured as GPIO
100	GND			
101	GPIO_96	1.8V	IO	Can be configured as GPIO
102	GPIO_95	1.8V	IO	Can be configured as GPIO
103	GPIO_94	1.8V	IO	Can be configured as GPIO
104	GPIO_93	1.8V	IO	Can be configured as GPIO
105	GPIO_92	1.8V	IO	Can be configured as GPIO
106	GPIO_91	1.8V	IO	Can be configured as GPIO
107	GPIO_90	1.8V	IO	Can be configured as GPIO
108	GPIO_89	1.8V	IO	Can be configured as GPIO
109	GPIO_88	1.8V	IO	Can be configured as GPIO
110	GPIO_87	1.8V	IO	Can be configured as GPIO
111	GND			
112	GPIO_43	1.8V	IO	Can be configured as GPIO
113	GPIO_44	1.8V	IO	Can be configured as GPIO
114	GPIO_45	1.8V	IO	Can be configured as GPIO
115	GPIO_46	1.8V	IO	Can be configured as GPIO
116	GND			
117	GPIO_50	1.8V	IO	Can be configured as GPIO
118	GPIO_49	1.8V	IO	Can be configured as GPIO
119	GPIO_48	1.8V	IO	Can be configured as GPIO
120	GPIO_47	1.8V	IO	Can be configured as GPIO
A1	MIPI_DSI0_L0_P			MIPI display serial interface 0 lane 0 positive. For TurboX™ C404 do not connect.
A2	MIPI_DSI0_L1_P			MIPI display serial interface 0 lane 1 positive. For TurboX™ C404 do not connect.
A3	GND			
A4	PCIE0_REFCLK_M	/	/	PCIE reference clock output (-)
A5	HDMI_TX2_P	/	/	HDMI TMDS data 2 positive. For TurboX™ C404 do not connect.
A6	HDMI_TX1_P	/	/	HDMI TMDS data 1 positive.

				For TurboX™ C404 do not connect.
A7	HDMI_TCLK_P	/	/	HDMI clock positive. For TurboX™ C404 do not connect.
A8	HDMI_TX0_P	/	/	HDMI TMDS data 0 positive. For TurboX™ C404 do not connect.
A9	PCIE0_RX_M	/	DI	PCIE receiver minus
A10	USB_SS_TX_M	/	DO	USB 3.0 transmitter differential pair minus
A11	USB_SS_RX_P	/	DI	USB 3.0 receiver differential pair plus
A12	USB1_HS_DP	/	IO	USB1 HS data plus
A13	GND			
A14	SDC2_CLK	SDC2	IO	Secure digital controller 2 clock
A15	SDC2_DATA_1	SDC2	IO	Secure digital controller 2 data bit 1
A16	SDC2_DATA_3	SDC2	IO	Secure digital controller 2 data bit 3
A17	GND			
A18	GPIO_14	1.8V	IO	Can be configured as GPIO
A19	GPIO_16	1.8V	IO	Can be configured as GPIO
A20	USB1_HS_ID	1.8V	DI	USB1 ID Pin
A21	GPIO_21	1.8V	IO	Can be configured as GPIO
A22	GND			
A23	GND			
A24	GND			
A25	GPIO_52	1.8V	IO	Can be configured as GPIO
A26	GPIO_54	1.8V	IO	Can be configured as GPIO
A27	GPIO_56	1.8V	IO	Can be configured as GPIO
A28	GPIO_58	1.8V	IO	Can be configured as GPIO
A29	GND			
B1	MIPI_DSI0_L0_M	/	/	MIPI display serial interface 0 lane 0 negative For TurboX™ C404 do not connect.
B2	MIPI_DSI0_L1_M	/	/	MIPI display serial interface 0 lane 1 negative For TurboX™ C404 do not connect.
B3	GND			
B4	PCIE0_REFCLK_P	/	/	PCIE reference clock output (+)
B5	HDMI_TX2_M	/	/	HDMI TMDS data 2 negative. For TurboX™ C404 do not connect.
B6	HDMI_TX1_M	/	/	HDMI TMDS data 1 negative. For TurboX™ C404 do not connect.
B7	HDMI_TCLK_M	/	/	HDMI clock negative. For TurboX™ C404 do not connect.
B8	HDMI_TX0_M	/	/	HDMI TMDS data 0 negative. For TurboX™ C404 do not connect.
B9	PCIE0_RX_P	/	DI	PCIE receiver plus
B10	USB_SS_TX_P	/	DO	USB 3.0 transmitter differential pair plus
B11	USB_SS_RX_M	/	DI	USB 3.0 receiver differential pair minus

B12	USB1_HS_DM	/	IO	USB1 HS data minus
B13	GND			
B14	SDC2_DATA_2	SDC2	IO	Secure digital controller 2 data bit 2
B15	SDC2_DATA_0	SDC2	IO	Secure digital controller 2 data bit 0
B16	SDC2_CMD	SDC2	IO	Secure digital controller 2 command
B17	GND			
B18	GPIO_15	1.8V	IO	Can be configured as GPIO
B19	GND			
B20	USB0_HS_ID	1.8V	DI	USB0 ID Pin
B21	GND			
B22	QCS_RESOUT_N	1.8V	D0	QCS reset output (active low)
B23	GND			
B24	GPIO_51	1.8V	IO	Can be configured as GPIO
B25	GPIO_53	1.8V	IO	Can be configured as GPIO
B26	GPIO_55	1.8V	IO	Can be configured as GPIO
B27	GPIO_57	1.8V	IO	Can be configured as GPIO
B28	GPIO_59	1.8V	IO	Can be configured as GPIO
B29	GPIO_119	1.8V	IO	Can be configured as GPIO
C1	PON_1	V_Internal	DI	Level-high triggered power-on input
C2	NC	-	-	Do not connect
C3	WCD_MCLK	1.8V	DO	Audio reference clock output for WCD
C4	PM_GPIO_06	1.8V	IO	PMS405 GPIO, and can be configured as GPIO
C5	PM_RESIN_N	1.8V	DI	Power management reset in (active low)
C6	KPDPWR_N	V_Internal	DI	Power-on trigger, level trigger (active low)
C7	PM_GPIO_04	1.8V	IO	PMS405 GPIO, and can be configured as GPIO
C8	NC			Do not connect
C9	GND			
C10	VREG_L11_SDC2	SDC2	PO	Power output for SD card pull up voltage;
C11	VREG_L13_3P3	3.3V	PO	3.3V LDO power output, 100mA
C12	GND			
C13	GPIO_61	1.8V	IO	Can be configured as GPIO
C14	GPIO_63	1.8V	IO	Can be configured as GPIO
C15	GPIO_65	1.8V	IO	Can be configured as GPIO
C16	GPIO_67	1.8V	IO	Can be configured as GPIO
C17	GND			
C18	GPIO_70	1.8V	IO	Can be configured as GPIO
C19	GPIO_72	1.8V	IO	Can be configured as GPIO
C20	GPIO_74	1.8V	IO	Can be configured as GPIO
C21	GPIO_76	1.8V	IO	Can be configured as GPIO
C22	GND			
C23	GPIO_22	1.8V	IO	Can be configured as GPIO
C24	GPIO_24	1.8V	IO	Can be configured as GPIO
C25	GND			

C26	GPIO_17	1.8V	DO	MSM_UART_TX
C27	GPIO_19	1.8V		Can be configured as GPIO
C28	GND			
C29	GPIO_118	1.8V	IO	Can be configured as GPIO
D1	PA_THERM1		AI	ADC for external temperature sensor
D2	SLEEP_CLK	1.8V	D0	32.7 KHZ sleep output
D3	PM_GPIO_12	V_Config	IO	PMS405 GPIO, and can be configured as GPIO
D4	PM_GPIO_03	V_Config	IO	PMS405 GPIO, and can be configured as GPIO
D5	NC			Do not connect
D6	NC			Do not connect
D7	GND			
D8	QCS_PS_HOLD	1.8V	DI	Power supply hold control input
D9	GND			
D10	VREG_L7_1P8	1.8V	PO	1.8V LDO power output, 100mA
D11	GND			
D12	GPIO_60	1.8V	IO	Can be configured as GPIO
D13	GPIO_62	1.8V	IO	Can be configured as GPIO
D14	GPIO_64	1.8V	IO	Can be configured as GPIO
D15	GPIO_66	1.8V	IO	Can be configured as GPIO
D16	GPIO_68	1.8V	IO	Can be configured as GPIO
D17	GPIO_69	1.8V	IO	Can be configured as GPIO
D18	GPIO_71	1.8V	IO	Can be configured as GPIO
D19	GPIO_73	1.8V	IO	Can be configured as GPIO
D20	GPIO_75	1.8V	IO	Can be configured as GPIO
D21	GPIO_77	1.8V	IO	Can be configured as GPIO
D22	GND			
D23	GPIO_23	1.8V	IO	Can be configured as GPIO
D24	GPIO_25	1.8V	IO	Can be configured as GPIO
D25	GND			
D26	GPIO_18	1.8V	DI	MSM_UART_RX
D27	GPIO_20	1.8V	IO	Can be configured as GPIO
D28	GPIO_117	1.8V	IO	Can be configured as GPIO
D29	GND			
E1	GND			
E2	GPIO_78	1.8V	IO	Can be configured as GPIO
E3	GPIO_79	1.8V	IO	Can be configured as GPIO
E4	GPIO_80	1.8V	IO	Can be configured as GPIO
E5	GPIO_81	1.8V	IO	Can be configured as GPIO
E6	SPMI_CLK_CON	1.8V	DO	System power management interface clock.
E7	SPMI_DATA_CON	1.8V	IO	System power management interface data
E8	LPI_GPIO_5	1.8V	IO	Can be configured as GPIO
E9	LPI_GPIO_20	1.8V	IO	Can be configured as GPIO
E10	GND			

E11	GPIO_86	1.8V	IO	Can be configured as GPIO
E12	GND			
E13	GPIO_103	1.8V	IO	Can be configured as GPIO
E14	GND			
E15	GPIO_104	1.8V	IO	Can be configured as GPIO
E16	GPIO_105	1.8V	IO	Can be configured as GPIO
E17	GPIO_106	1.8V	IO	Can be configured as GPIO
E18	GPIO_107	1.8V	IO	Can be configured as GPIO
E19	GPIO_108	1.8V	IO	Can be configured as GPIO
E20	GPIO_109	1.8V	IO	Can be configured as GPIO
E21	GND			
E22	GND			
E23	LPI_GPIO_6	1.8V	IO	Can be configured as GPIO
E24	LPI_GPIO_7	1.8V	IO	Can be configured as GPIO
E25	GND			
E26	LPI_GPIO_8	1.8V	IO	Can be configured as GPIO
E27	LPI_GPIO_9	1.8V	IO	Can be configured as GPIO
E28	LPI_GPIO_10	1.8V	IO	Can be configured as GPIO
E29	GND			
E30	GND			
E31	GND			
E32	GND			
E33	JTAG_SRST_N	/	DI	JTAG reset for debug
E34	JTAG_TCK	/	DI	JTAG clock input
E35	JTAG_TDI	/	DI	JTAG data input
E36	JTAG_TDO	/	DI	JTAG data output
E37	JTAG_TMS	/	B	JTAG mode-select input
E38	JTAG_TRST_N	/	DI	JTAG reset
E39	GND			
E40	GPIO_36	1.8V	IO	Can be configured as GPIO
E41	GND			
E42	GND			
G1	GND			
G2	GND			
G3	GND			

3.3 Interfaces Detail Description

3.3.1 Power Supply Interface

Below table describes all interfaces of SoM Power Supply. For the detail parameter request, please refer the chapter on Electrical specifications.

Power Supply				
Pin Name	PIN Location	Type	Description	Notes
VPH_PWR	74,75,76,80,81,82,83,87,88,89	PI	Power supply input for SoM all operations.	
VREG_L6_1P8	90	PO	Low voltage switch supply output 1.8V for IO and pull up voltage;	
VREG_L11_SDC2	C10	PO	Power output for SD card pull up ;	
VREG_L7_1P8	D10	PO	1.8V LDO power output, Max 100mA	
VREG_L13_3P3	C11	PO	3.3V LDO power output, Max 100mA	
GND	3,6,12,15,18,21,26,31,36,42,49,51,52,54, ,55,57,58,60,61,61,63,68,71,72,73,77,78, ,79,84,85,86,100,111,116, A3,B3,D7,C9,D9,D11,D12,A13,B13,A17, B17,C17,B19,B21,A22,B22,C22,D22,A2 3,B23,A24,C25,D25,C28,A29,D29, E1,E6,E7,E10,E12,E14,E21,E22,E25,E2 9,E30,E31,E32,E39,E41,E42, F4,F5,F6, G1,G2,G3	GND		

Table 3- 2 Power supply definition

3.3.2 RGMII Interfaces

The SoM supports RGMII interfaces can connect Ethernet transceiver.

RGMII Interface						
Pin Name	PIN	Location	Voltage	Type	Description	Notes
GPIO_61		C13	1.8V	DI	Ethernet transceiver interrupt input	
GPIO_63		C14	1.8V	DO	RGMII transmit clock output	
GPIO_64		D14	1.8V	DO	RGMII transmit data 3 output	
GPIO_65		C15	1.8V	DO	RGMII transmit data 2 output	
GPIO_66		D15	1.8V	DO	RGMII transmit data 1 output	
GPIO_67		C16	1.8V	DO	RGMII transmit data 0 output	
GPIO_68		D16	1.8V	DO	RGMII transmit enable output	
GPIO_69		D17	1.8V	DI	RGMII receive clock input	
GPIO_70		C18	1.8V	DI	RGMII receive data 3 input	
GPIO_71		D18	1.8V	DI	RGMII receive data 2 input	
GPIO_72		C19	1.8V	DI	RGMII receive data 1 input	
GPIO_73		D19	1.8V	DI	RGMII receive data 0 input	
GPIO_74		C20	1.8V	DI	RGMII receive data valid, RGMII input	
GPIO_75		D20	1.8V	IO	Management data	
GPIO_76		C21	1.8V	DO	Management data clock reference	

Table 3- 4 RGMII interface definition

3.3.3 SPDIF Interface

The SoM has a digital audio dedicated interface SPDIF. It's an input port only, and receiving audio signals in SPDIF format.

SPDIF Interface						
Pin Name	PIN	Location	Voltage	Type	Description	Notes
SPDIF_RX_COAX_RCA		19	-	DI	SPDIF receive port for electrical input	
SPDIF_RX_COAX_EP		20	-	DI	SPDIF receive port for optical input	

Table 3- 5 SPDIF interface definition

3.3.4 Audio Interface

The SoM provides the audio system digital processing functions.

The SoM provide SLIMBUS, I2S, SWR and DMIC interfaces for audio system. The multiplexing of these interfaces is as follows.

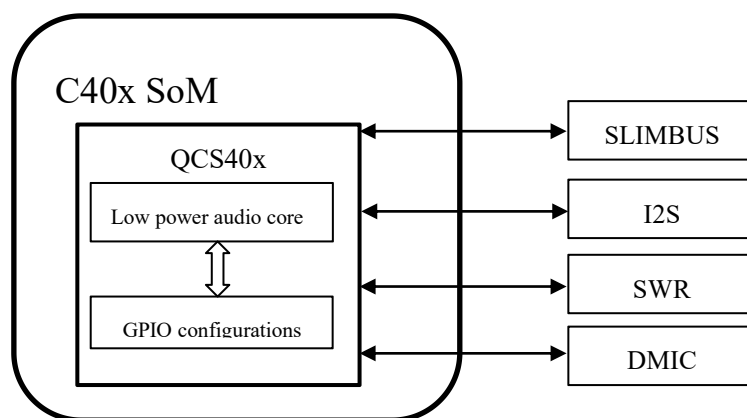


Figure 3- 3 Audio

One port Serial low-power interchip media bus (SLIMBUS) interface is dedicate for external codec IC, which can build system's audio functions.

SLIMBUS Interface

Pin Name	PIN	Location	Voltage	Type	Description	Notes
LPI_GPIO_2	33		1.8V	DO	Audio SLIMBUS clock	
LPI_GPIO_3	34		1.8V	IO	Audio SLIMBUS data0	
LPI_GPIO_4	35		1.8V	IO	Audio SLIMBUS data1	

Table 3- 6 Audio interface definition

Six ports inter-IC sound (I2S) interfaces can connect audio devices.

I2S Interface

Pin Name	PIN	Location	Voltage	Type	Description	Notes
GPIO_87	110		1.8V	DO	I2S 1 SCK	
GPIO_88	109		1.8V	DO	I2S 1 WS	
GPIO_89	108		1.8V	IO	I2S 1 Data0	
GPIO_90	107		1.8V	IO	I2S 1 Data1	
GPIO_91	106		1.8V	IO	I2S 1 Data2	
GPIO_92	105		1.8V	IO	I2S 1 Data3	
GPIO_93	104		1.8V	IO	I2S 1 Data4	
GPIO_94	103		1.8V	IO	I2S 1 Data5	
GPIO_95	102		1.8V	IO	I2S 1 Data6	
GPIO_96	101		1.8V	IO	I2S 1 Data7	
GPIO_97	43		1.8V	DO	I2S 2 SCK	
GPIO_98	44		1.8V	DO	I2S 2 WS	
GPIO_99	45		1.8V	IO	I2S 2 Data0	
GPIO_100	46		1.8V	IO	I2S 2 Data1	
GPIO_101	47		1.8V	IO	I2S 2 Data2	
GPIO_102	48		1.8V	IO	I2S 2 Data3	
GPIO_104	E15		1.8V	DO	I2S 3A SCK	
GPIO_105	E16		1.8V	DO	I2S 3A WS	
GPIO_106	E17		1.8V	IO	I2S 3A Data0	

GPIO_107	E18	1.8V	IO	I2S 3A Data1	
GPIO_108	E19	1.8V	IO	I2S 3A Data2	
GPIO_109	E20	1.8V	IO	I2S 3A Data3	
GPIO_52	A25	1.8V	DO	I2S 3B SCK	
GPIO_53	B25	1.8V	DO	I2S 3B WS	
GPIO_54	A26	1.8V	IO	I2S 3B Data0	
GPIO_55	B26	1.8V	IO	I2S 3B Data1	
GPIO_56	A27	1.8V	IO	I2S 3B Data2	
GPIO_57	B27	1.8V	IO	I2S 3B Data3	
GPIO_110	97	1.8V	DO	I2S 4 SCK	
GPIO_111	96	1.8V	DO	I2S 4 WS	
GPIO_112	95	1.8V	IO	I2S 4 Data0	
GPIO_113	94	1.8V	IO	I2S 4 Data1	
GPIO_114	93	1.8V	IO	I2S 4 Data2	
GPIO_115	92	1.8V	IO	I2S 4 Data3	
LPI_GPIO_8	E26	1.8V	DO	I2S 5 SCK	
LPI_GPIO_9	E27	1.8V	DO	I2S 5 WS	
LPI_GPIO_10	E28	1.8V	IO	I2S 5 Data0	
LPI_GPIO_11	41	1.8V	IO	I2S 5 Data1	
LPI_GPIO_12	40	1.8V	IO	I2S 5 Data2	
LPI_GPIO_13	39	1.8V	IO	I2S 5 Data3	

One port Sound wire (SWR) interface is dedicate for external audio amplify of Qualcomm.

SWR Interface

Pin Name	PIN	Location	Voltage	Type	Description	Notes
LPI_GPIO_5		E8	1.8V	DO	Sound wire interface clock	
LPI_GPIO_20		E9	1.8V	IO	Sound wire interface data	

Four ports digital microphone (DMIC) interfaces can connect 8x digital microphones.

DICM Interface

Pin Name	PIN	Location	Voltage	Type	Description	Notes
LPI_GPIO_8		E26	1.8V	DO	Digital MIC0/1 clock	
LPI_GPIO_9		E27	1.8V	IO	Digital MIC0/1 data	
LPI_GPIO_10		E28	1.8V	DO	Digital MIC2/3 clock	
LPI_GPIO_11		41	1.8V	IO	Digital MIC2/3 data	
LPI_GPIO_12		40	1.8V	DO	Digital MIC4/5 clock	
LPI_GPIO_13		39	1.8V	IO	Digital MIC4/5 data	
LPI_GPIO_14		38	1.8V	DO	Digital MIC6/7 clock	
LPI_GPIO_15		37	1.8V	IO	Digital MIC6/7 data	

3.3.5 USB Interface

The SoM support USB host and slave. Dual USB port support, one is USB 2.0 high-speed, the other is USB 3.0 super-speed/USB 2.0 high-speed compliant. The USB1 support host mode only.

SS/HS USB1 (3.0/2.0) Interface						
Pin Name	PIN	Location	Voltage	Type	Description	Notes
USB_SS_TX_M		A10	-	DO	USB 3.0 transmitter differential pair minus	
USB_SS_TX_P		B10	-	DO	USB 3.0 transmitter differential pair plus	
USB_SS_RX_P		A11	-	DI	USB 3.0 receiver differential pair plus	
USB_SS_RX_M		B11	-	DI	USB 3.0 receiver differential pair minus	
USB1_HS_DP		A12	-	IO	USB1 HS data plus	Require differential impedance of 90Ω.
USB1_HS_DM		B12	-	IO	USB1 HS data minus	
PM_GPIO_12		D3	1.8V	DI	VBUS1 insertion detection	
USB0_HS_ID		A20	1.8V	DI	USB0 ID Pin	
HS USB0 (2.0) Interface						
Pin Name	PIN	Location	Voltage	Type	Description	Notes
USB0_HS_ID		B20	1.8V	AI	USB0 ID Pin	
USB0_HS_DM		13	-	IO		
USB0_HS_DP		14	-	IO		
PM_GPIO_06		C4	1.8V	DI	VBUS0 insertion detection	

Table 3- 7 USB interface definition

3.3.6 PCIe Interface

The SoM support one Peripheral Component Interconnect Express (PCIe) interfaces, which can be used for general-purpose peripherals.

PCIe Interface						
Pin Name	PIN	Location	Voltage	Type	Description	Notes
PCIE0_REFCLK_M		A4	-	-	PCIE reference clock output (-)	
PCIE0_REFCLK_P		B4	-	-	PCIE reference clock output (+)	
PCIE0_RX_M		A9	-	DI	PCIE receiver minus	
PCIE0_RX_P		B9	-	DI	PCIE receiver plus	
PCIE0_TX_M		11	-	DO	PCIE transmitter minus	
PCIE0_TX_P		10	-	DO	PCIE transmitter plus	

Table 3- 8 PCIe interface definition

3.3.7 MIPI DSI Interface

TurboX™ C405 support MIPI of display, and can be up to FHD 30 fps. This is one 4-lane MIPI DSI port, and supported only on TurboX™ C405.

MIPI DSI Interface						
Pin Name	PIN	Location	Voltage	Type	Description	Notes
MIPI_DSI0_CLK_P	2		-	DO	MIPI display serial interface 0 clock positive	
MIPI_DSI0_CLK_M	1		-	DO	MIPI display serial interface 0 clock negative	
MIPI_DSI0_L0_P	A1		-	DO	MIPI display serial interface 0 lane 0 positive	
MIPI_DSI0_L0_M	B1		-	DO	MIPI display serial interface 0 lane 0 negative	
MIPI_DSI0_L1_P	A2		-	DO	MIPI display serial interface 0 lane 1 positive	
MIPI_DSI0_L1_M	B2		-	DO	MIPI display serial interface 0 lane 1 negative	
MIPI_DSI0_L2_P	5		-	DO	MIPI display serial interface 0 lane 2 positive	
MIPI_DSI0_L2_M	4		-	DO	MIPI display serial interface 0 lane 2 negative	
MIPI_DSI0_L3_P	8		-	DO	MIPI display serial interface 0 lane 3 positive	
MIPI_DSI0_L3_M	7		-	DO	MIPI display serial interface 0 lane 3 negative	

Table 3- 9 MIPI DSI interface definition

3.3.8 HDMI Interface

HDMI support up to 1080p 30 fps, and supported only on TurboX™ C405.

HDMI Interface						
Pin Name	PIN	Location	Voltage	Type	Description	Notes
HDMI_TCLK_P	A7		-	DO	HDMI TMDS clock positive	
HDMI_TCLK_M	B7		-	DO	HDMI TMDS clock negative	
HDMI_TX0_P	A8		-	DO	HDMI TMDS data 0 positive	
HDMI_TX0_M	B8		-	DO	HDMI TMDS data 0 negative	
HDMI_TX1_P	A6		-	DO	HDMI TMDS data 1 positive	
HDMI_TX1_M	B6		-	DO	HDMI TMDS data 1 negative	
HDMI_TX2_P	A5		-	DO	HDMI TMDS data 2 positive	
HDMI_TX2_M	B5		-	DO	HDMI TMDS data 2 negative	
GPIO_14	A18		-	DO	HDMI_TX_CEC	
GPIO_15	B18		-	DO	HDMI_DDC_CLK	
GPIO_16	A19			IO	HDMI_DDC_DATA	
GPIO_77	D21			DI	HDMI_Hot_plug	

Table 3- 10 HDMI interface definition

3.3.9 JTAG Interface

The SoM has a JTAG interface for debug.

JTAG Interface						
Pin Name	PIN	Location	Voltage	Type	Description	Notes
JTAG_SRST_N		E33	-	DI,PU	JTAG reset for debug	
JTAG_TCK		E34	-	DI,PU	JTAG clock input	
JTAG_TDI		E35	-	DI,PU	JTAG data input	
JTAG_TDO		E36	-	-	JTAG data output	
JTAG_TMS		E37	-	B,PU	JTAG mode-select input	
JTAG_TRST_N		E38	-	DI,PD	JTAG reset	
QCS_RESIN_N		C2	1.8V	DI	System reset input	
QCS_PS_HOLD		D8	1.8V	DI	Power supply hold control input	

Table 3- 11 SSC interface definition

3.3.10 SDIO Interface

The SoM support dual 4-laneSDIO, SDC2 connect to SD-card.

The SDIO is high-speed signal group. It should protect other sensitive signals/circuits from SD corruption, and protect SD signals from noisy signals (clock, RF and so on).

- The clock can be up to 50 Mhz.
- The signals routing should be 36-50ohm impedance control.
- CLK to DATA/CMD length matching less than 2mm.
- The spacing to all other signals should 2X line width
- Maximum bus capacitance less than 1.0pF.
- Each trace needs to be next to a ground plane.

SDIO (SDC2) Interface					
Pin Name	PIN Location	Voltage	Type	Description	Notes
SDC2_CLK	A14	P2	DO	Secure digital controller 2 clock	
SDC2_CMD	B16	P2	IO	Secure digital controller 2 command	
SDC2_DATA_3	A16	P2	IO	Secure digital controller 2 data bit 3	
SDC2_DATA_2	B14	P2	IO	Secure digital controller 2 data bit 2	
SDC2_DATA_1	A15	P2	IO	Secure digital controller 2 data bit 1	
SDC2_DATA_0	B15	P2	IO	Secure digital controller 2 data bit 0	
GPIO_59	B28	P3	DI	SD_CARD_DET_N need pull up to P3	

Table 3- 12 SDIO interface definition

3.3.11 BLSP Interface

These GPIOs are available as BAM-based low-speed peripheral (BLSP) interface ports that can be configured for UART, SPI, or I2C operation.

I2C is a two-wire bus that can be routed to multiple devices; each line of each bus is supplemented by a 2.2kΩ pull-up resistor.

2-wire UART Tx/Rx and I2C SDA/SCL ports can be used simultaneously.

BLSP Interface-1								
BLSP Number	GPIO	PIN Location	Voltage	Type	Description			Notes
					SPI	UART	I2C	
0	30	64	P3	IO	MOSI	TX	-	
	31	65	P3	IO	MISO	RX	-	
	32	66	P3	IO	CS_N	CTS_N	SDA	
	33	67	P3	IO	CLK	RFR_N	SCL	
1	22	C23	P3	IO	MOSI_A	TX	-	
	23	D23	P3	IO	MISO_A	RX	-	
	24	C24	P3	IO	CS_N_A	CTS_N	SDA	
	25	D24	P3	IO	CLK_A	RFR_N	SCL	
2	17	C26	P3	IO	MOSI	TX	-	
	18	D26	P3	IO	MISO	RX	-	
	19	C27	P3	IO	CS_N	CTS_N	SDA	
	20	D27	P3	IO	CLK	RFR_N	SCL	
4	37	69	P3	IO	MOSI	TX	-	
	38	70	P3	IO	MISO	RX	-	
	117	D28	P3	IO	CS_N	CTS_N	SDA	
	118	C29	P3	IO	CLK	RFR_N	SCL	

Table 3-3-12-1 BLSP interface definition

BLSP Interface-2								
BLSP Number	GPIO	PIN Location	Voltage	Type	Description			Notes
					SPI	UART	I2C	
5	26	22	P3	IO	MOSI	TX	-	
	27	23	P3	IO	MISO	RX	-	
	28	24	P3	IO	CS_N	CTS_N	SDA	
	29	25	P3	IO	CLK	RFR_N	SCL	
	44	113	P3	IO	CS1_N	-	-	
	45	114	P3	IO	CS2_N	-	-	
	46	115	P3	IO	CS3_N	-	-	

Table 3- 13 BLSP interface definition

3.3.12 Power On Interface

Dedicated PMIC circuits continuously monitor events that might trigger a power-on sequence. If an event occurs, these circuits power on the IC, determine the device's available power sources, enable the correct source.

There are two events that will be triggered.

When insert battery or other power supply and pull down KPDPWR_N to ground, SoM will be power on automatically. It is longer than 1s with pressing power-on key, for power on event. And it is suggested for 3s powering on system.

Other power on event, when pull up PON_1 pin to power, it is high-level triggered with a valid trigger range between 1.17 V to VPH_PWR, and insert battery or power supply, SoM will be power on automatically.

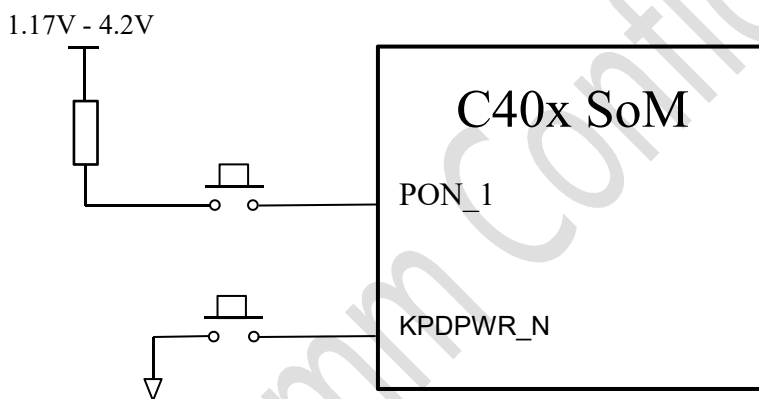


Figure 3-4 Power on signal

Power on Interface					
Pin Name	PIN Location	Voltage	Type	Description	Notes
KPDPWR_N	C6	V_INT	DI	Power-on trigger, level trigger (active low)	
PON_1	C1	1.17V - 4.2V	DI	Level-high triggered power-on input	

Table 3- 14 Power on interface definition

3.3.13 Reset Interface

Three stage reset and external resets.

- Stage 1 reset – software-configurable bark

PMIC generates interrupt, giving the SoC device the opportunity to fix the problem or gracefully reset the system. Example events that can cause a bark: Over temperature indicates system is getting too hot. PMIC watchdog indicates that it has not kicked.

- Stage 2 –software-configurable bite

If reset is ignored, PMIC will force a reset event (selectable by software).

- Stage 3 –hardware mandatory bite

The user can generate a mandatory reset by a long key press of KYPD_PWR to resets PMIC back to factory default.

Reset Pin					
Pin Name	PIN Location	Voltage	Type	Description	Notes
KDPWR_N	C6	V_INT	DI	Long press to reset PMIC. (active low)	

Table 3- 15 Reset interface definition

These reset triggers each have individual debounce and delay timers. Their default values are 10.256 seconds for stage 1 and 2 seconds for stage 2, respectively, and they share the stage 3 reset timer. Stage 1 and stage 2 timers run in series, and stage 3 timer runs independently (parallel) of stage 1 and stage 2 timers. If the stage 3 timer is set to a lower value than that of stage 1 and stage 2 combined, then the stage 3 reset happens first. The stage 3 default values is 128 seconds.

3.3.14 Boot Configuration Interface

There are two types of boot-related fuses:

- Fast boot fuse is used by the boot code to determine which memory device should the chip use for boot.
- Secure boot fuse where device encryption is used to ensure that the code running on QCS40x is from a trusted source.

Configure fuses or BOOT_CONFIG pins.

- BOOT_CONFIG pins provide flexibility during product development.
- Fuses should be blown for production devices.
- BOOT_CONFIG [3:1] is MSB-aligned with Fast_Boot [2:0].

Boot Configurations:

BOOT_CONFIG[3:1]	Boot Options	Notes
0b000	Try SDC1 --> SDC2 --> USB2.0	default
0b001	Try SDC2 --> SDC1	
0b010	Try SDC1	
0b011	Try USB2.0	

Default boot configuration (0b000) is eMMC on SDC1.

Special boot-related GPIO features:

- They are sensed for boot-purposes during IC reset (during fuse sense).
- After bootup, use them for normal GPIO functions.
- Do not have pull-ups on GPIO_55, GPIO_56, GPIO_57, and GPIO_49 prior to blowing FAST_BOOT fuses.

The boot configuration function of the preceding GPIOs is sampled at the rising edge of RESOUT_N reassertion.

Boot Configuration Interface					
Pin Name	PIN Location	Voltage	Type	Description	Notes
GPIO_45	114	P3	IO	Forced USB boot; Configurable I/O	
GPIO_55	B26	P3	IO	Fast boot select bit 0 (configure external boot device); WDOG_DISABLE. Configurable I/O	
GPIO_56	A27	P3	IO	Fast boot select bit 1 (configure external boot device); Configurable I/O	
GPIO_57	B27	P3	IO	Fast boot select bit 2 (configure external boot device); Configurable I/O	
GPIO_49	118	P3	IO	Fast boot select bit 3 (configure external boot device); Configurable I/O	

Table 3- 16 Sensor interrupt definition

Forced USB boot

During development or factory production, boot from USB_HS port are forced by using GPIO_45.

- FORCED_USB_BOOT (GPIO_45) always takes precedence, regardless of the state of the BOOT_CONFIG GPIOs or FAST_BOOT_SEL fuses.
- FORCED_USB_BOOT is checked first during the boot device detection prior to BOOT_CONFIG GPIOs.
- GPIO_45 = 1 forces the SDM device to boot from USB_HS port.

Blow the FORCE_USB_BOOT_DISABLE fuse to disable the feature that forces USB boot using GPIO_45.

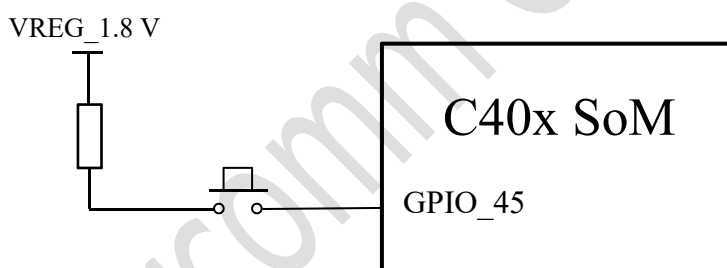


Figure 3- 5 Power on signal

Other boot configuration bits are listed in the table below, and do not have pull up on these IOs also.

Other Boot Configuration Interface					
Pin Name	PIN Location	Voltage	Type	Description	Notes
GPIO_54	A26	P3	IO	Fast boot select bit 4 (configure external boot device); Configurable I/O	
GPIO_52	A26	P3	IO	Fast boot select bit 5 (configure external boot device); Configurable I/O	
GPIO_51	B24	P3	IO	Fast boot select bit 6 (configure external boot device); Configurable I/O	
GPIO_48	119	P3	IO	Fast boot select bit 7 (configure external boot device); Configurable I/O	

GPIO_59	B28	P3	IO	Fast boot select bit 8 (configure external boot device); Configurable I/O	
GPIO_46	115	P3	IO	Fast boot select bit 9 (configure external boot device); Configurable I/O	
GPIO_79	E3	P3	IO	Fast boot select bit 10 (configure external boot device); Configurable I/O	
GPIO_78	E2	P3	IO	Fast boot select bit 11 (configure external boot device); Configurable I/O	
GPIO_47	120	P3	IO	Fast boot select bit 12 (configure external boot device); Configurable I/O	
GPIO_50	117	P3	IO	Fast boot select bit 13 (configure external boot device); Configurable I/O	
GPIO_80	E4	P3	IO	Fast boot select bit 14 (configure external boot device); Configurable I/O	

3.3.15 Debug UART Interface

This interface is dedicated for debug.

Debug UART Pins					
Pin Name	PIN Location	Voltage	Type	Description	Notes
GPIO_17	C26	P3	DO	MSM_UART_TX	
GPIO_18	D26	P3	DI	MSM_UART_RX	

Table 3- 17 Debug UART interface definition

3.3.16 PWM

The GPIO_03 can be configured to send the output of the PWM waveform through special functions that can control the external current drivers for LED.

PWM Pin					
Pin Name	PIN Location	Voltage	Type	Description	Notes
PM_GPIO_03	D4	Software configurable: VIN0 = 3.6V (Nominal) VIN1 = 1.8V	DO	Configurable GPIO	

Table 3- 18 PWM definition

3.3.17 Sleep Clock

The sleep-clock output from PMS405, and it is generated following ways:

- Calibrated low-frequency RC oscillator, periodically uses the 38.4 MHz XO signal for calibration, achieving accuracy suitable for the real-time clock.
- Using the 38.4 MHz XO circuit and dividing its output by 1172 to create a 32.7645 KHz signal. This signal is used as the start-up sleep clock.

SLEEP_CLK Pin					
Pin Name	PIN Location	Voltage	Type	Description	Notes
SLEEP_CLK	D2	1.8V	DO	32.7 KHZ sleep output.	

Table 3- 19 SLEEP_CLK definition

3.3.18 SPMI

The SPMI is a bidirectional, two-line digital interface for communication between Qualcomm chipsets, which meets the relevant information for voltage and current level requirements.

SPMI Pin					
Pin Name	PIN Location	Voltage	Type	Description	Notes
SPMI_CLK_CON	E6	1.8v	DO	System power management interface clock	
SPMI_DATA_CON	E7	1.8v	IO	System power management interface data	

Table 3- 20 SPMI definition

3.3.19 Antenna Interface

The SoM provides the fully-integrated WLAN, Bluetooth function.

- WLAN supports 2 × 2 (WCN3999) and 1 × 1 (WCN3980) multiple input, multiple output (MIMO) with two spatial streams IEEE802.11 a/b/g/n/ac WLAN standards.
- Supports Bluetooth +LE5.x + HS enabling seamless integration of WLAN/Bluetooth and low energy technology.
- Concurrent operation for WLAN and BT.

Antenna interface					
Pin Name	PIN Location	Voltage	Type	Description	Notes
ANT_WL_Chain 1	50	-	RF IO	Antenna port for WIFI Tx/Rx chain 1	
ANT_WL_Chain 0	59	-	RF IO	Antenna port for WIFI/BT Tx/Rx chain 0	

Table 3- 21 Antenna interface definition

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

The SoM needs to be designed in the operating conditions which is shown as below table beyond its absolute maximum ratings may damage the device.

Parameter	Min	Max	Units
Input Power voltage			
Voltage on any input or output pin	-0.5	VPH_PWR+0.5	V
VPH_PWR	-0.5	6.0	V

Table 4- 1 Absolute rating condition

4.2 Operating Conditions

The SoM needs to be designed in the operating conditions which is shown as below table.

Parameters	Min	Typical	Max	Units
Input Power voltage				
VPH_PWR	+3.0	3.6	+5.0	V
Supply voltage, digital I/O	+1.75	-	+1.85	V
VPH_PWR	0.8			A
Thermal conditions				
Operating temperature	-20	25	70	°C
Storage temperature	-20	-	70	°C

Table 4- 2 Operating condition

Note: For the thermal conditions, operating and storage min and max temperature is only when the module is fully tested and approved in the Initial Production stage.

4.3 Output Power

The SoM provide power supply for external device. Below map show the details.

Function	Default voltage(V)	Programable range(V)	Rated current(mA)	Default ON	Expected use
----------	--------------------	----------------------	-------------------	------------	--------------

VREG_L6_1P8	+1.8	-	100	Y	1.8V IO pull up voltage;
VREG_L11_SDC2	+2.95	+1.8--+3.3	100	Y	Power output for SD card data pull up
VREG_L7_1P8	+1.8	+1.7--+1.89	100	N	1.8V LDO power output, 100mA
VREG_L13_3P3	+1.8	+1.8--+1.8	100	N	1.8V LDO power output, 100mA

Table 4- 3 Output power

4.4 Digital-logic characteristics

The digital I/O's performance depends on its pad type, usage, and power supply voltage.

The SoM IO voltage level is the same with P3 except the SD card and analog input/output.

The I2C, USB, MIPI and UART comply with the standards, and additional specifications are not required.

All other digital I/Os require performance specifications and are organized within this section.

4.4.1 Digital GPIO characteristics

The GPIO ports are digital I/Os that can be programmed for a variety of configurations. General performance specifications for are the different configurations.

The following table shows the digital GPIO characteristics:

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, CMOS/Schmitt,	0.65* P3	-	V
VIL	Low-level input voltage, CMOS/Schmitt,	-	0.35* P3	V
VSHYS	Schmitt hysteresis voltage	100	-	mV
VOH	High-level output voltage, CMOS	P3-0.45	-	V
VOL	Low-level output voltage, CMOS	-	0.45	V
RPULL-UP	Pull-up and Pull-down resistance	55	390	KΩ
Rk	Keeper resistance	30	150	KΩ

Table 4- 4 digital IO voltage performance

4.4.2 SD card digital I/O characteristics

The SD card is powered by P2 supply; the power is 1.8V and 2.95V. the following table shows the SD card

digital I/O characteristics:

Parameter	Description	Min	Typical	Max	Units
VIH	High-level input voltage	1.27V/1.84V	-	2.0V/2.98V	V
VIL	Low-level input voltage	-0.3	-	0.58/0.74	V
VHYS	Schmitt hysteresis voltage	100	-	-	mV
RPULL-UP	Pull-up resistance	10 K	-	100K	Ω
RPULL-DOWN	Pull-down resistance	10 K	-	100K	Ω
RKEEPER-UP	Keeper-up resistance	10 K	-	100K	Ω
RKEEPER-DOWN	Keeper-down resistance	10 K	-	100K	Ω
VOH	High-level output voltage	1.4/2.21	-	-	V
VOL	Low-level output voltage	0/0	-	0.45/0.36	V

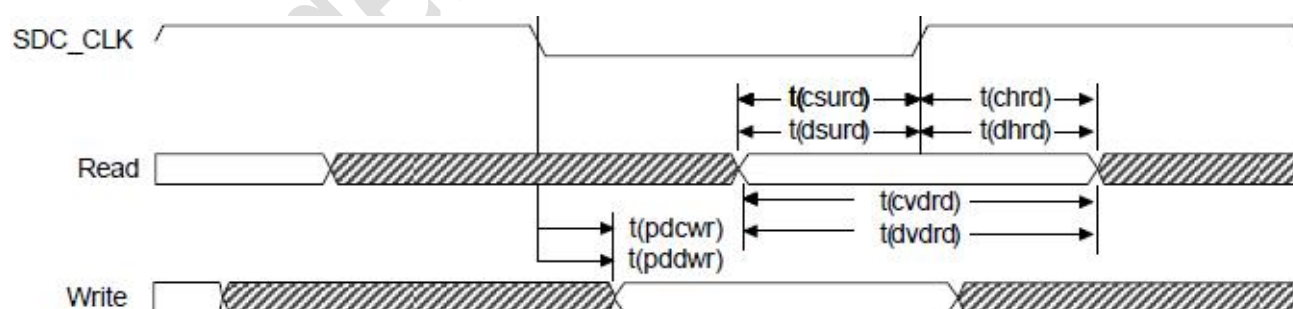
Table 4- 5 SD digital IO voltage performance (1.8V/2.95V)

The SoM Supports SD standards and exceptions

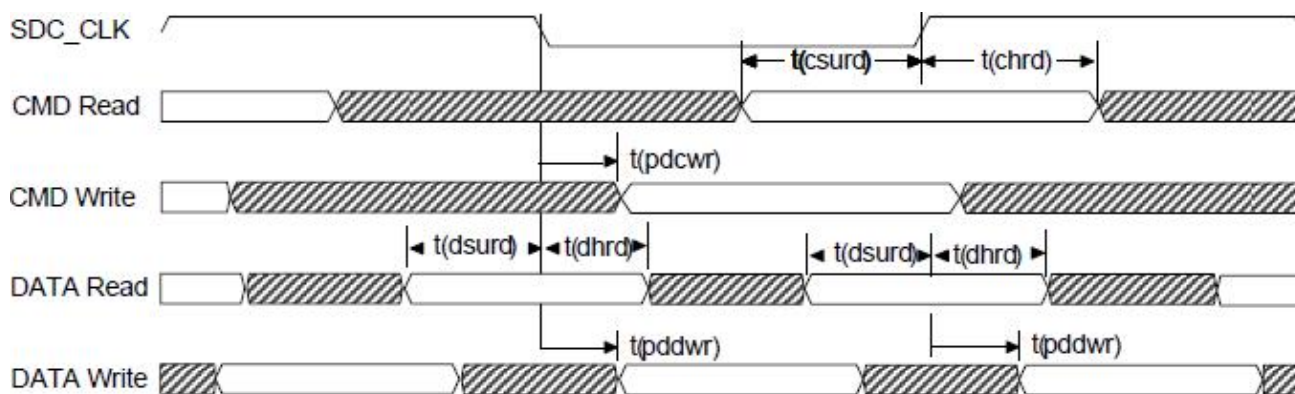
Applicable standard	Feature exceptions	Device variations
Multi Media Card Host Specification, version 5.1 (JESD84-B51 - JEDEC)	None	Timing specifications as below pictures
Secure Digital: Physical Layer Specification version 3.0	None	
SDIO Card Specification version 2.0	None	

Table 4- 6 SDIO

Single data rate - SDR mode



Double data rate - DDR mode



Secure digital interface timing

Parameter	Description	Min	Typical	Max	Units
DDR mode - SDC2, up to 50 MHz					
tchrd	Command hold	1.50	-	-	ns
tcsurd	Command setup	6.30	-	-	ns
tdhrd	Data hold	1.50	-	-	ns
tdsurd	Data setup	2.00	-	-	ns
tpddwr	Propagation delay on data write	0.80	-	6.00	ns
tpdcwr	Propagation delay on command write	-8.20	-	3.00	ns

4.5 USB

THE SoM supports USB standards and exceptions.

Applicable standard	Feature exceptions	APQ variation
Universal Serial Bus Specification, Revision 2.0 (April 27, 2000 or later)	None	Operating voltages, system clock, and VBUS
On-The-Go Supplement to the USB 2.0 Specification (June 24, 2003, Revision 1.0 or later)	Supports the host mode aspect of OTG only	None

Table 4- 7 USB

4.6 SLIMbus

THE SoM supports SLIMbus HDMI standards and exceptions

Applicable standard	Feature exceptions	APQ variation
MIPI Alliance Specification for Serial Low-power Interchip Media Bus,	No support of the CHANGE_CONTENT() message by any of the devices in the component. Only the manager is given the ability to	The maximum clock output slew rate might

Version 1.01.011	manage data channels in the system. ■ No support for the elemental access mode for information and value elements. ■ No support for the following transport protocols. - Asynchronous half-duplex - Extended asynchronous half-duplex ■ No support for the locked transport protocol ■ No support of a partial mask in CHANGE_VALUE message	be greater than 20% * VDD [V/ns] for the 15 pF load condition.
------------------	---	---

Table 4- 8 SLIMbus

SLIMbus frequencies

SLIMbus	SVS	Nom1	Turbo	Units
Slimbus1 (IFM)	24.57	24.57	24.57	MHz
Slimbus2 (QCA) (IFM)	24.57	24.57	24.57	MHz
Slimbus1 (XFM)	23.1	23.1	23.1	MHz
Slimbus2 (XFM)	22.4	22.4	22.4	MHz

4.7 I2S

THE SoM I2S standards and exceptions:

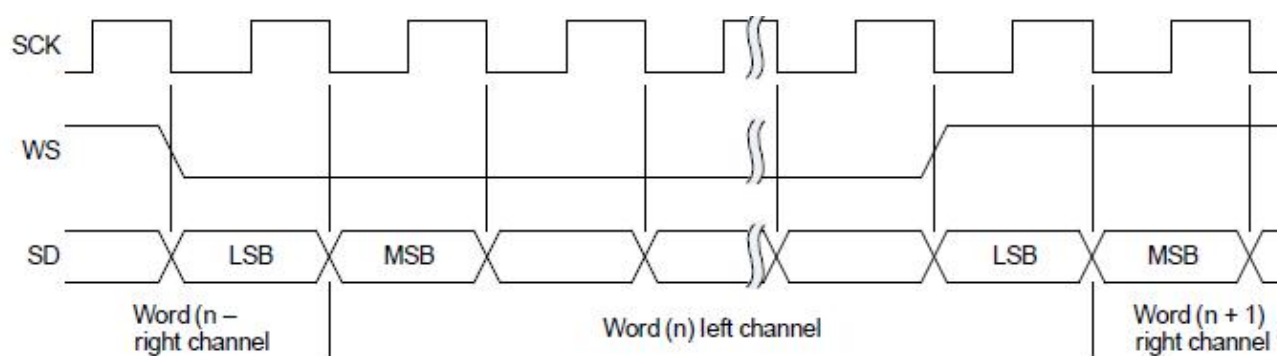
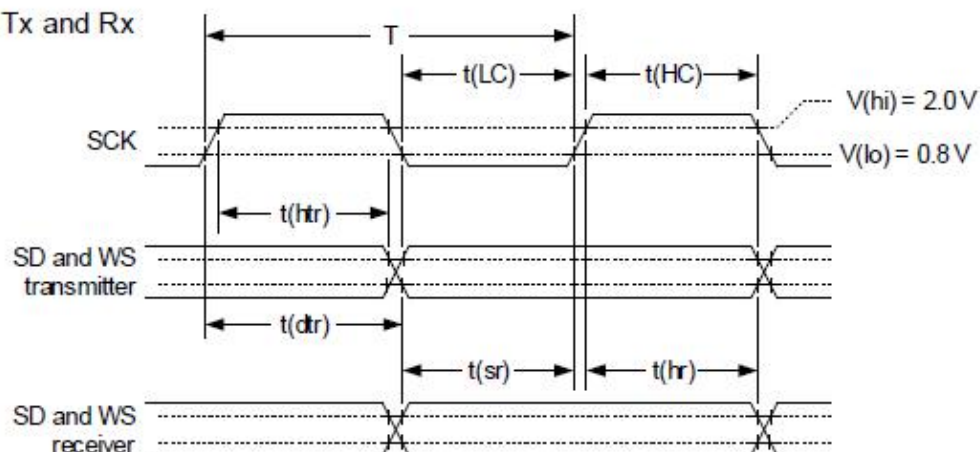
Legacy I2S interfaces for primary and secondary microphones and speakers.

The multiple I2S (MI2S) interface for microphone and speaker functions, including audio for HDMI.

Applicable standard	Feature exceptions	Device variations
Philips I2S Bus Specifications revised June 5, 1996	None	Timing – When an external SCK clock is used, a duty cycle between 45% to 55% is required.

Table 4- 9 I2S

High-level I2S timing

I²S timing details – Tx and Rx

I2S interface timing

Parameter	Description	Min	Typical 1	Max	Units
Using internal SCK					
F	Frequency. Load capacitance is between 10 and 40pF.			12.288	MHZ
T	Clock period. Load capacitance is between 10 and 40pF.	81.380	-	-	ns
t(HC)	Clock high. Load capacitance is between 10 and 40pF.	0.45 x T		0.55 x T	ns
t(LC)	Clock low. Load capacitance is between 10 and 40pF.	0.45 x T		0.55 x T	ns
t(sr)	SD and WS input setup time. Load capacitance is between 10 and 40pF.	16.276	-	-	ns
t(hr)	SD and WS input hold time. Load capacitance is between 10 and 40pF.	0	-	-	ns
t(dtr)	SD and WS output delay. Load capacitance is between 10 and 40pF.	-	-	65.100	ns
t(htr)	SD and WS output hold time. Load capacitance is between 10 and 40pF.	0	-	-	ns
Using external SCK					
F	Frequency. Load capacitance is between 10 and 40pF.			12.288	MHZ
T	Clock period. Load capacitance is between 10 and 40pF.	81.380	-	-	ns
t(HC)	Clock high. Load capacitance is between 10 and 40pF.	0.45 x T		0.55 x T	ns
t(LC)	Clock low. Load capacitance is between 10 and 40pF.	0.45 x T		0.55 x T	ns
t(sr)	SD and WS input setup time. Load capacitance is between 10 and 40pF.	16.276	-	-	ns
t(hr)	SD and WS input hold time. Load capacitance is between 10 and 40pF.	0	-	-	ns
t(dtr)	SD and WS output delay. Load capacitance is between 10 and 40pF.	-	-	65.100	ns
t(htr)	SD and WS output hold time. Load capacitance is between 10 and 40pF.	0	-	-	ns

I2S interface frequencies

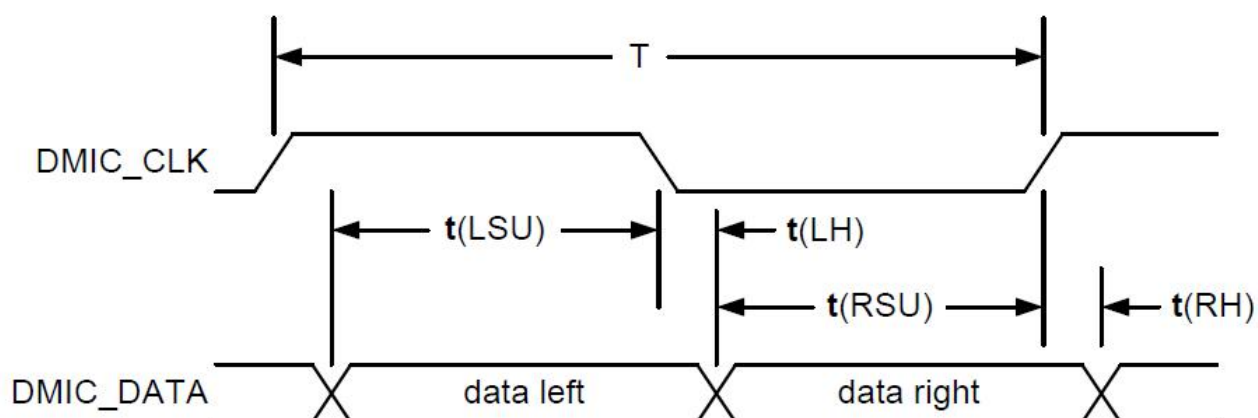
Interface	Frequency achieved
I2S1	24.57 MHz
I2S2	12.288 MHz
I2S3A	12.288 MHz
I2S3B	12.288 MHz
I2S5	24.57 MHz
I2S6	12.288 MHz

4.8 PDM

THE SoM PDM interfaces for primary and secondary digital microphones.

DMIC interfaces running at 9.6 MHz clock.

PDM interfaces timing



PDM interface timing

Parameter	Description	Min	Typical	Max	Units
Using internal SCK					
T	DMIC clock period	163	-	1666	ns
t(LSU)	Data left setup time to the clock falling edge	5	-	-	ns
t(LH)	Data left hold time to the clock falling edge	0	-	-	ns
t(RSU)	Data right setup time to the clock rising edge	5	-	-	ns
t(RH)	Data right hold time to the clock falling edge	0	-	-	ns

4.9 I2C

THE SoM I2C standards and exceptions:

Applicable standard	Feature exceptions
<i>I²C Specification</i> , version 5.0, October 2012	None

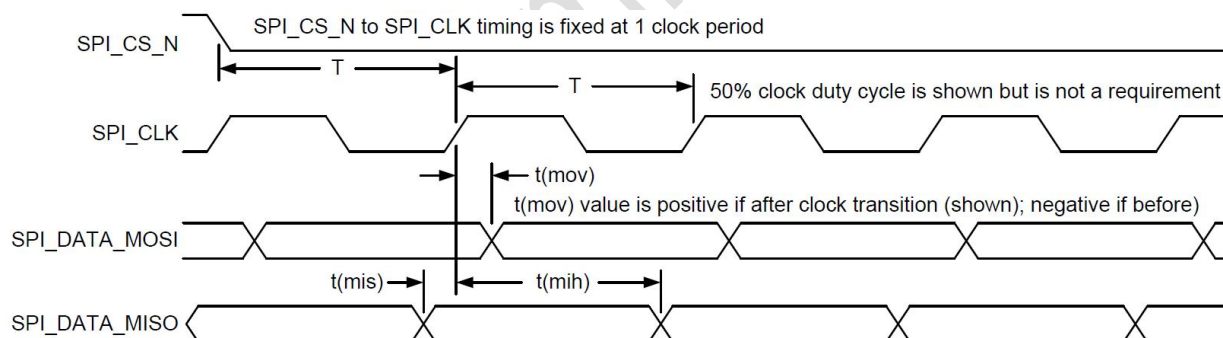
Table 4- 10 I2C

4.10 SPI

The following are the SPI features and comparisons:

- Supports 4 - bit (MISO, MOSI, CS, CLK) synchronous serial data link.
- Support for master-only mode, up to 50 MHz on all SPI interfaces.
- Master device initiates data transfers; Multiple slave devices are supported by using chip-selects.
- No explicit communication framing, error-checking, or defined data word lengths; The transfers are strictly at the raw bit level.
- As an SPI master, the core supports several SPI system configurations (as defined by the SPI protocol).

SPI master timing diagram



SPI master timing characteristics at 50 MHz

Parameter	Description	Min	Typical	Max	Units
T	SPI clock period: 50 MHz maximum	20	-	-	ns
t(ch)	Clock high	9.0	-	-	ns
t(cl)	Clock low	9.0	-	-	ns
t(mov)	Master output valid	-5.0	-	5.0	ns
t(mis)	Master input setup	5.0	-	-	ns
t(mih)	Master input hold	1.0	-	-	ns
T	SPI clock period: 26 MHz maximum	38	-	-	ns
t(ch)	Clock high	17	-	-	ns

t(cl)	Clock low	17	-	-	ns
t(mov)	Master output valid	-5.0	-	5.0	ns
t(mis)	Master input setup	5.0	-	-	ns
t(mih)	Master input hold	1.0	-	-	ns

Table 4- 11 Current sink specification

4.11 Current Sink

PM_GPIO_03 is capable of sinking current (up to 10 mA). In addition, since the PWM module can be routed to the current sink, different blinking and dimming patterns can be achieved.

Parameter	Description	Min	Typical	Max	Units
			1		
Rated current sink		9	-	12	mA

Table 4- 12 Current sink specification

4.12 Sleep Clock

The sleep output characteristics: (voltage levels, drive strength, and so on see Digital GPIO characteristics),

Parameter	Description	Min	Typical	Max	Units
			1		
Period jitter (rms)	38.4 MHz XO/1172	-	-	10	ns RMS
Frequency drift	Shift in frequency in any 2.5 sec window at constant temperature	-	-	2	ppm
RTC accuracy	CalIRC provides a jittery clock that provides a long term averaged accurate RTC clock; time accuracy defined over	-	-	200	ppm

Table 4- 13 Sleep Clock specification

4.13 SPMI

THE SoM SPMI standards and exceptions:

Applicable standard	Feature exceptions
MIPI Alliance Specification for System Power Management Interface (SPMI) version 1.0	None

Table 4- 14 SPMI standard

4.14 MIPI DSI

THE SoM MIPI DSI standards and exceptions:

Applicable standard	Feature exceptions
<i>MIPI Alliance Specification v1.01 for Display Serial Interface</i>	None
<i>MIPI D-PHY Specification v0.65, v0.81, v0.90</i>	

Table 4- 15 MIPI DSI standard

4.15 Power Consumption

The following current consumption records are measured on TurboX C40x DK, and any specific equipment configuration or use different from DK may increase power consumption.

Test Condition: Room temperature (25°C).	
Measure power for 60 sec.	
Test case	QCS404/QCS405 PMS405 & 1GB LPDDR3 WCN3999 (mA)
Sleep mode	< 2.4
Airplane mode with display OFF, keyword detection OFF	33.5
Bluetooth paired (sniff + scan) Adder (from WCN399x, does not chane with QCS part)	34.1
WLAN DTIM3/DTIM1 Adder	44.1/44.9
Local MP3 audio playback in tunnel mode (excluding speaker PA)	51.3
WLAN PNO (preferred network order) scan (60s) Adder	48.2
WLAN [2.4 GHz 1x1 config] streaming MP3 [128 kps] audio playback in tunnel mode (excluding speaker PA)	201.2
Bluetooth A2DP Rx local audio playback (excluding speaker PA)	101.1
Bluetooth HFP voice call with Fluence Pro v2.1	34.7
Current leak while power off	< 0.2

Table 4- 16 Power Consumption

5 Mechanical Size

5.1 Mechanical Size

The size of TurboX™ 40x SoM is 33.8 X 33.8mm. Thickness is 2.6mm;

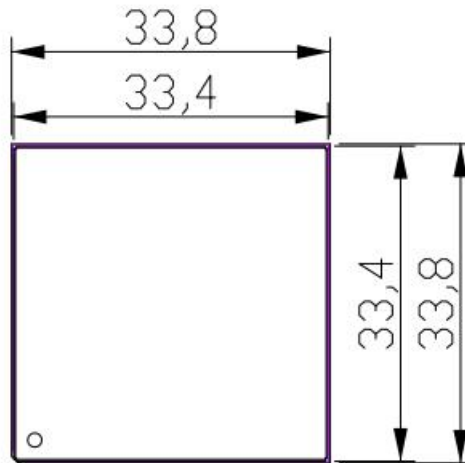


Figure 5-1 Top View

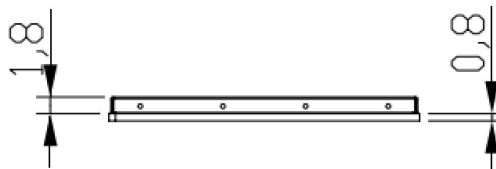


Figure 5-2 Side View

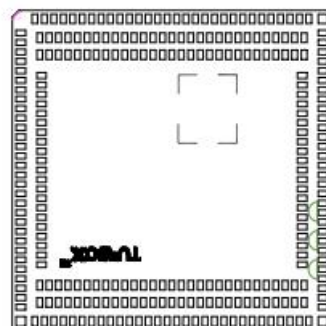


Figure 5-3 Bottom View

5.2 Package dimensions

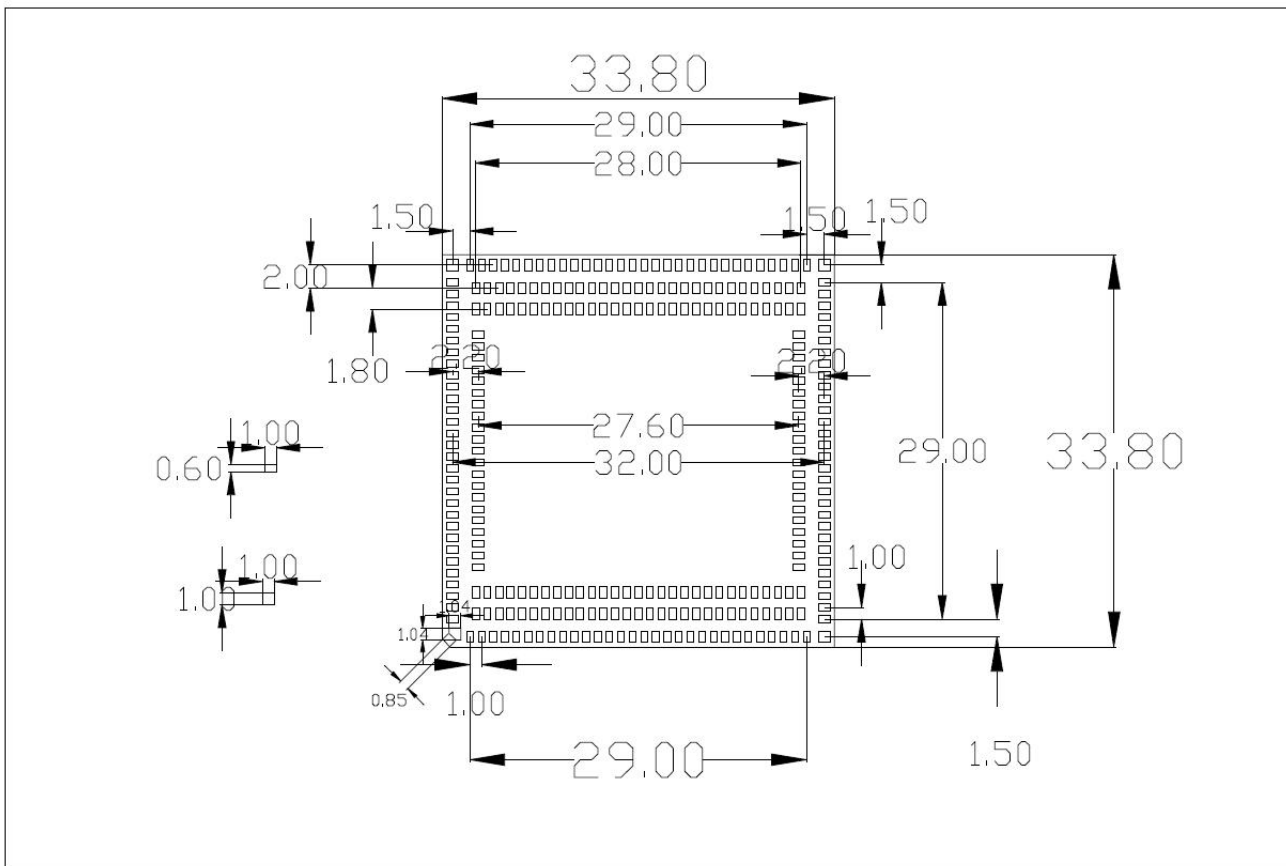


Figure 5-4 package dimensions

5.3 SoM Marking

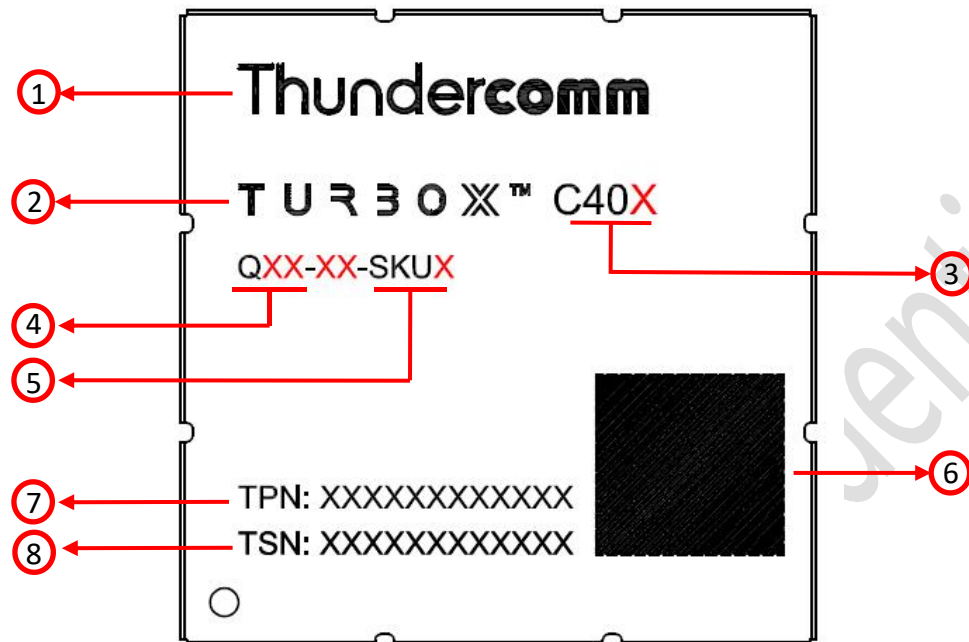


Figure 5- 5 SOM print

- ① Thundercomm Logo.
- ② Product Logo.
- ③④⑤ Product Configuration Code.
- ⑥ QR Code.
- ⑦ Thundercomm Part Number.
- ⑧ Thundercomm Serial Number.

Part Number	Configuration		
	③	④	⑤
	QCS405	WCN3980	eMCP,8GB eMMC5.1+8Gb LPDDR3
	QCS404	WCN3980	eMCP,8GB eMMC5.1+8Gb LPDDR3
	QCS405	WCN3999	eMCP,8GB eMMC5.1+8Gb LPDDR3
	QCS404	WCN3999	eMCP,8GB eMMC5.1+8Gb LPDDR3
	QCS404	WCN3999	eMCP,8GB eMMC5.1+8Gb LPDDR3

Table 5- 1 SOM Marking

6 SMT Assembly Guide

About the requirements of module secondary assembly please refer to the

Thundercomm_Module_Secondary_SMT_Assembly_Guide_V0.1, any query please contact with your vendor.

The device has been evaluated to meet general RF exposure requirement.

TurboX C404 is a module without antenna. The following 2 types of antennas are recommended:

Antenna Type A	
Antenna Manufacturer:	MOLEX
Brand Name:	N/A
Part No.:	ANT1/ANT2: 1461530100
Antenna Type:	ANT1/ANT2: Dipole Antenna
Antenna Gain:	Bluetooth ANT1: 3.00dBi 2.4GWIFI ANT1/ANT2: 3.00dBi 5G WIFI ANT1/ANT2: 4.00dBi

or

Antenna Type B	
Antenna Manufacturer:	INPAQ TECHNOLOGY CO., LTD
Brand Name:	N/A
Part No.:	ANT1: RFPCA292034IMLB901 ANT2: RFPCA292016IMLB901
Antenna Type:	ANT1/ANT2:PIFA Antenna
Antenna Gain:	Bluetooth ANT1: 3.49dBi 2.4GWIFI ANT1: 3.49dBi; 2.4GWIFIANT2: 3.51dBi 5G WIFI ANT1: 5.52dBi 5G WIFI ANT2: 5.55dBi

Trade Name: TurboX

Manufacturer: Thundercomm Technology Co., Ltd

Manufacturer Address: Building 4, No. 99, Data Valley Middle Road, Xiantao District, Yubei District, Chongqing, China

CE statements:

Do not use the module in the environment at too high or too low temperature,
never expose the module under strong sunshine or too wet environment.

The suitable temperature for the product and accessories is -20°C-70°C.

RF exposure information: The Maximum Permissible Exposure (MPE) level has been calculated based on a distance of d=20 cm between the device and the human body. To maintain compliance with RF exposure requirement, use product that maintain a 20cm distance between the device and human body.

Receiver category:1

Maximum output power

Frequency		Max. EIRP
Bluetooth	BLE:2402-2480MHz	8.96dBm
	BR+EDR:2402-2480MHz	9.75dBm
Wi-Fi	2412~2472MHz	19.43dBm
	5180-5240MHz	22.93dBm
	5260-5320MHz	19.79dBm
	5500-5700MHz	19.78dBm
	5745-5825MHz	13.76dBm

The device for operation in the band 5150 – 5350 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems.

	AT	BE	BG	CH	CY	CZ	DE	DK
	EE	EL	ES	FI	FR	HR	HU	IE
	IS	IT	LI	LT	LU	LV	MT	NL
	PL	PT	RO	SE	SI	SK	TR	UK

EU Regulatory Conformance

Hereby, Thundercomm Technology Co., Ltd declares that this device is in compliance with the essential requirements and other relevant provisions of Directive 2014/53/EU.



FCC statements:

The device for operation in the band 5150 – 5350 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems.

Federal Communication Commission (FCC) Radiation Exposure Statement

When using the product, maintain a distance of 20cm from the body to ensure compliance with RF exposure requirements.

This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:

- (1) this device may not cause harmful interference, and
- (2) this device must accept any interference received, including interference that may cause undesired operation.

NOTE: The manufacturer is not responsible for any radio or TV interference caused by unauthorized modifications or changes to this equipment. Such modifications or changes could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

EU Declaration of Conformity (DoC)

Hereby we,

Name of manufacturer: **Thundercomm Technology Co., Ltd**

Address:

Building 4, No. 99, Data Valley Middle Road, Xiantao District, Yubei District, Chongqing, China

Zip code & City:

Chongqing

Country:

China

Telephone number:

18664928002

declare that this DoC is issued under our sole responsibility and that this product:

Product description:

Turbox C404 SOM

Type designation(s):

TurboX C404

Trademark:

TurboX

Hardware version:

TurboX C404 SOM V06

Software version:

LE1

Software version note: Some software updates will be released by the manufacturer to fix some bug or enhance some function after placing on the market. All versions released by the manufacturer have been verified and still compliance with the related rules. All RF parameters (e.g.: frequency range, output power) are not accessible to the user, and can't be changed by the user.

This product can be used across EU member states.

Object of the declaration

TurboX C404 are Turbox C404 SOM and incorporate Wi-Fi, Bluetooth technologies.

is in conformity with the relevant Union harmonization legislation:

Radio Equipment directive: **2014 / 53 / EU**

and other Union harmonization legislation where applicable:

RoHS directive: **2011 / 65 / EU**

WEEE directive: **2012 / 19 / EU**

with reference to the following standards applied:

Health: EN 50663:2017; EN 62311:2008;

Safety: EN 62368-1:2014+A11:2017;

EMC: ETSI EN 301 489-1 V2.2.3; ETSI EN 301 489-17 V3.2.4;

RF: ETSI EN 300 328 V2.2.2; ETSI EN 301 893 V2.1.1; ETSI EN 300 440 V2.2.1;



The Notified Body *Telefication* with Notified Body number **0560** performed:

Applicable Modules: B+C

Where applicable: The issued the EU-type examination certificate: 212140058/AA/00.

Description of accessories and components, including software, which allow the radio equipment to operate as intended and covered by the DoC:

Antenna Type A	ANT1 Bluetooth : Dipole Antenna, 3dBi ANT1/ANT2 WIFI: Dipole Antenna, 3dBi(2.4GHz), 4dBi(5GHz) Manufacturer: MOLEX Part No.: 1461530100
----------------	--

or

Antenna Type B	ANT1 Bluetooth : PIFA Antenna, 3.49dBi ANT1 WIFI: PIFA Antenna, 3.49dBi(2.4GHz), 5.52dBi(5GHz) ANT2 WIFI: PIFA Antenna, 3.51dBi(2.4GHz), 5.55dBi(5GHz) Manufacturer: INPAQ TECHNOLOGY CO., LTD Part No.: ANT1: RFPCA292034IMLB901; ANT2: RFPCA292016IMLB901
----------------	---

Note: This product will not be sold with the antenna. The above two types of antennas are only used for testing.

.....
...

Signed for and on behalf of:

Chongqing 2021.02.07

Place and date of issue

Qiyong Zhou

Name, Function, and signature