

Thundercomm TurboX C2290/CM2290 SOM

Datasheet

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Revision History

Version	Date	Author	Description
V1.0	Mar 16, 2021	Qiming Duan	Initial release
V1.1	Aug 11, 2021	Qiming Duan	Add the following sections: • <u>1.6. Stencil design and aperture</u> • <u>1.7. Module laser marking</u>
V1.2	Aug 16, 2021	Qiming Duan	Add the following sections: • <u>1.3. Major component location</u> • <u>1.8. SMT assembly guide</u>
V1.3	Oct 09, 2021	Qiming Duan	• Update memory and DMIC description in <u>Table 1-2. Key features and performance of C(M)2290 SOM</u> • Change definition of Pin#128, Pin#139 and Pin#189199 in <u>Table 2-2. Pin assignment</u> • Add a note at the end of <u>2.2. Interfaces detail description</u> • Update <u>Table 2-3. Pin definition of power supply interface</u> and add a note in <u>2.2.1. Power supply interface.</u> • Update <u>Table 2-8. GPIO QUP configuration</u> and add a note in <u>2.2.6. QCM2290 GPIO.</u> • Update <u>Table 2-10. PMIC GPIO interface pad parameters</u>
V1.4	Feb 11, 2022	Qiming Duan	Update display support information in <u>Table 1-1. Key features and performance of QCM2290 processor</u> ; remove DisplayPort.
V1.4.1	Mar 01, 2022	Qiming Duan	Update the note below <u>Table 2-8. GPIO QUP configuration</u>
V1.5	May 25, 2022	Qiming Duan	• Remove C-PHY 1 from <u>Table 1-1.</u> ● Remove SoundWire relevant information. • Update <u>Table 1-2, Table 2-2, Table 2-3, and Table 3-4.</u> • Update <u>Figure 1-1, Figure 1-2, Figure 1-4 and Figure 1-5</u> <u>Figure 1-8</u> • Remove GPIO_8, GPIO_9, GPIO_10 and GPIO_11 from <u>Table 2-8</u> • Update the following sections: □ <u>1.6. Stencil design and aperture</u> <u>1.7. Module laser marking</u> <u>03.2. Operating conditions</u> • Add introduction in <u>3.1. Absolute maximum ratings</u> • Complete the contents of <u>3.16. Power consumption</u> • Complete the contents of <u>3.18. RF performance.</u> • Add new section <u>3.19. GPS performance.</u>

V1.6	July 12, 2022	Qiming Duan	• Update <u>Table 1-2</u>. • Update <u>Figure 1-1, Figure 1-2, Figure 1-4, Figure 1-5, and Figure 1-6</u> • Update description of Pad#75 in <u>Table 2-2</u>. • Add <u>Table 2-3</u> and <u>Table 3-2</u>. • Update operating temperature scope to:-25℃ to 75℃. • Complete thermal test data in <u>3.17. Thermal</u> • Fix format problems.
V1.7	Apr 17, 2023	Qiming Duan	• Update <u>Table 1-2</u> • Update <u>1.4. Mechanical size</u>. • Add Chapter 4. Packaging
V1.7.1	Aug 29, 2023	Qiming Duan	• Add note*to <u>Table 1-2</u> • Update 1.8. SMT assemblyguide

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About This Document

- Illustrations in this documentation might look different from your product.
- Depending on the model,some optional accessories,features,and software programs might not be available on your device.
- Depending on the version of operating systems and programs,some user interface instructions might not be applicable to your device.
- Documentation content is subject to change without notice.Thundercomm makes constant improvements on the documentation of your computer,including this guidebook.

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Chapter 1.Overview

Thundercomm TurboX C2290/CM2290 SOM (System on Module) is designed based on the Qualcomm QCM2290 platform. It brings high-value features to entry-level devices, designed to support all-day battery life, fast LTE connectivity, enhanced camera, advanced graphics, etc. The form factor of the module is 34mm*35mm(C2290)/51mm*35mm(CM2290) LGA package which can be fit into device such as translator, handheld POS, home gateways, household cleaning Robotics, Dash Camera, PDA & tablet, etc. It is ideal platform for both industrial and consumer applications requiring high data rates multimedia function, and help to rapidly develop cost-effective cellular devices to the market.

ONOTE: “TurboX” referred to herein is the English text of our registered trademark T

UR30X

1.1.Key features

The following tables present the detailed features and performances on Thundercomm TurboX C2290/CM2290 SOM.

Table 1-1.Keyfeatures and performance of QCM2290 processor

	QCM2290 processor
Application Processor	64-bit Arm Cortex-A53 Quad-core applications processor at 2.0GHz with 512 KB L2 cache
DSP	QDSP6 v66K Dedicated DSP shared between Snapdragon sensor core and low-power audio subsystem
GPU	Qualcomm® Adreno™ GPU 702 at 845 MHz GPU with 64-bit addressing
Memory support	• Dual-channel non-PoP high-speed memory-LPDDR4X SDRAM designed for an 1804 MHz clock (2×16-bit) • Single-channel non-PoP high-speed memory-LPDDR3 SDRAM designed for a 933 MHz clock (1×32-bit)
Display support	• One 4-lane DSI D-PHY, 1.2 at 1.5 Gbps per lane, split link supported. • Upto HD+ (1680×720 at 60Hz)
External memory	• eMMC5.1 • SD3.0
Camera support	• MIPI combination D-PHY 1.2 configurable in 4/4 or 4/2/1 • D-PHY: 2.5 Gbps/lane • 2x ISP: 13+13MP or 25 MP at 30 fps ZSL • Real-time sensor input resolution: 25MP or 13+13 MP • 25 MP 30 ZSL with a dual ISP • 48 MP resolution in nZSL mode • 13 MP 30 ZSL with a single ISP
Viedo performance	Encode: • 1080p30-bit HEVC (H.265) • 1080p30-bit H.264 Decode: • 1080p30-bit H.264 • 1080p30-bit HEVC (H.265), VP9 • Concurrency • 1080p 30 decode+720p 30 encode • HFR capture • 480p 120
Connectivity	1x USB 3.1

Table 1-2.Key features and performance of C2290/CM2290 SOM

C2290/CM2290 SOM	
Processor	QCM2290
Operating System	Android, Linux
Memory*	1GB LPDDR4x+8GB eMMC 2GB LPDDR4x+16GB eMMC 3GB LPDDR4x+16GB eMMC
Display Interface	1x4-lane DSI D-PHY 1.2
Camera Interface	2x 4-lane CSI D-PHY 1.2
Audio Interface	2x DMIC port, support up to 4x DMIC 3x AMIC 1x EAR 1x Line out 1x headphone (HPHL+HPHR) • 2x MI2S (MI2S0 multiplexing pins with two DMIC ports)
USB	1x Type-C USB (PM4125-3)/1x Micro USB (PM4125-2)
WLAN	• WCN3950, Support 1×1, 802.11 a/b/g/n/ac, support Bluetooth 5.0, BLE, or • WCN3910, Support 1×1, 802.11 b/g/n, support Bluetooth 5.0, BLE
RF Bands (CM2290 only)	EMEA: • LTE:B1/B2/B3/B5/B7/B8/B20/B28 (A+B)/B38/B39/B40/B41 • WCDMA:B1/B2/B5/B8 • GSM:850/900/1800/1900 MHz North America: • LTE:B2/B4/B5/B7/B12/B13/B14/B17/B25/B41/B66/B71
UIM	2x UIM
QUP	Up to 5 QUP, 4 QUP (LPI), support UART, I2C, I3C, SPI
SDIO	1x4-bit, SD 3.0
JTAG	On board JTAG test points
Dimensions and Form Factor	Size:34 mm x35 mm x3 mm (C2290);51 mm×35mm x3 mm (CM2290) Weight:7.3g (C2290);10.7g (CM2290) • Interface form factor:LGA
Operating Temperature	-25°C to 75°C
RoHS	All hardware components are fully compliant with EU RoHS directive.

*:Please note that storage devices such as UFS,eMMC,NAND,etc.have a limit to the total amount of data that can be written.Exceeding this limit can cause damage to the storage device.

1.3.Major component location

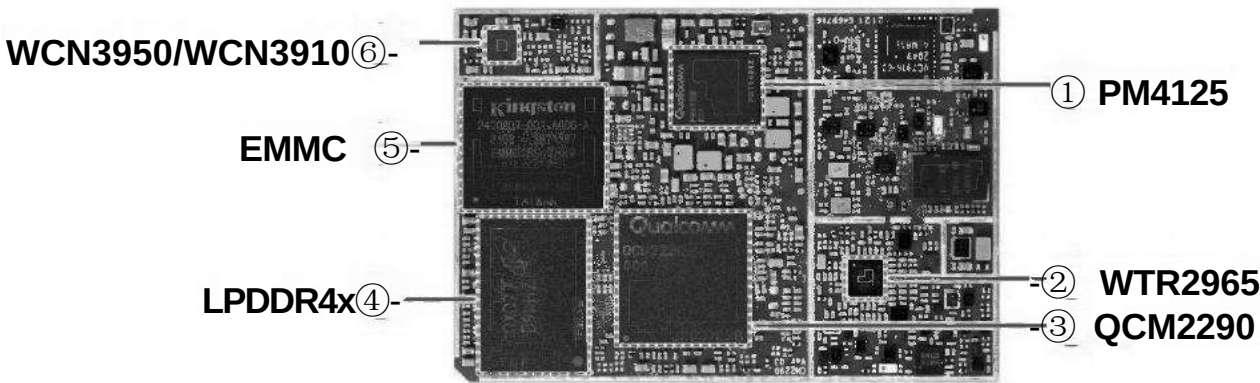


Figure 1-3.CM2290 SOM Major Component Location

1.4.Mechanical size

·TurboX C2290 SOM:34 mmx35 mm x3 mm

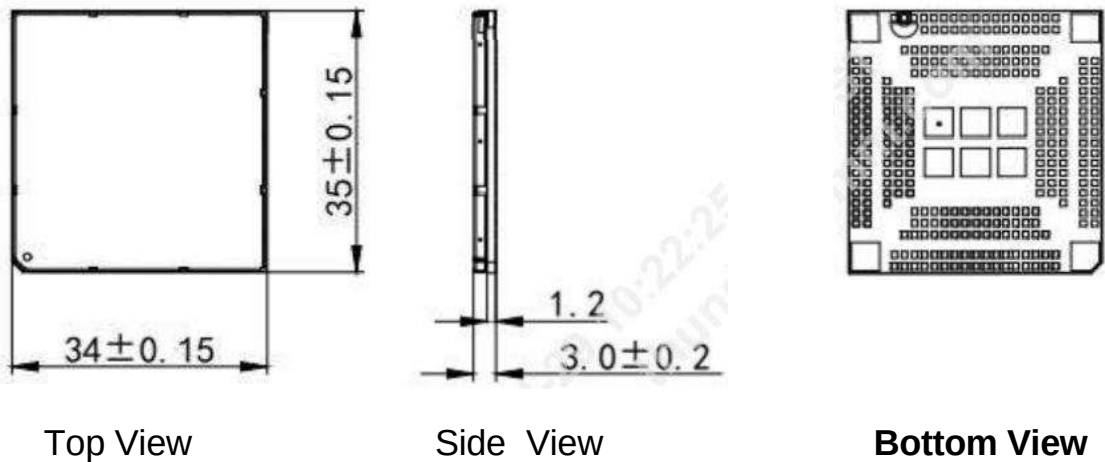


Figure 1-4.C2290 SOM Dimension

·TurboX CM2290 SOM:51 mm x35 mmx3 mm

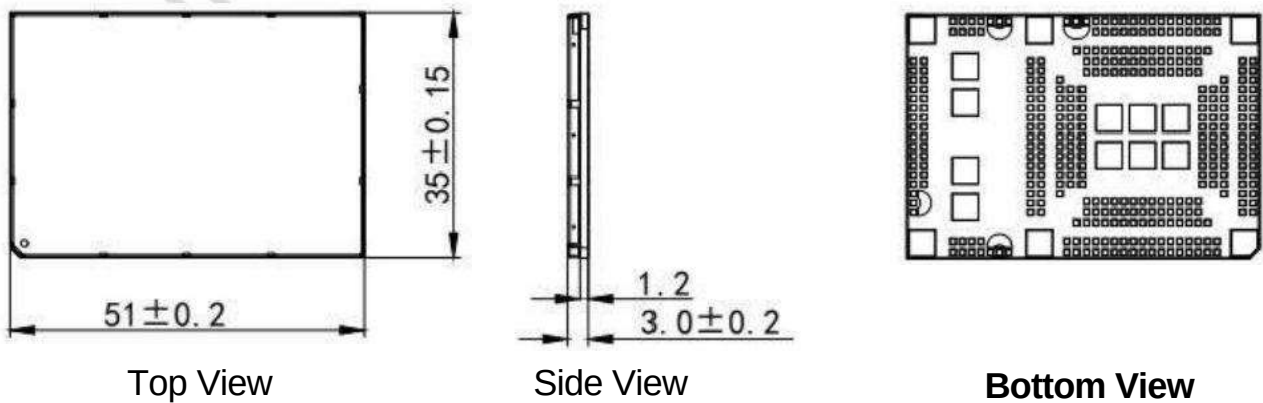


Figure 1-5.CM2290 SOM Dimension

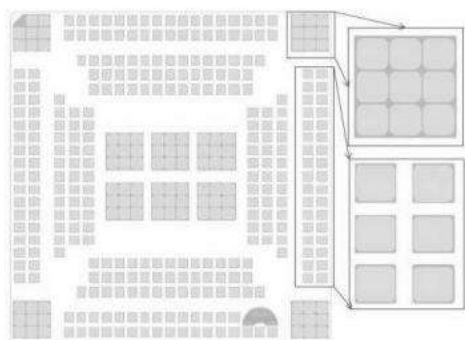


Figure 1-7. Stencil Aperture Diagram (C2290)

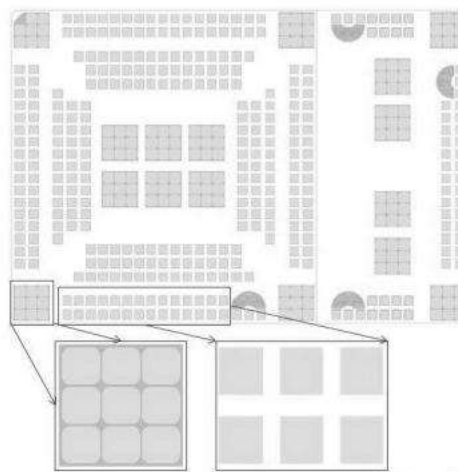


Figure 1-8. Stencil Aperture Diagram (CM2290)

Requirement description

• Stencil thickness

Area of the module should be partly stepped-up to 0.15mm-0.18mm.

• Pads on four sides

The aperture for each single pad should be centered with area reduced to 75%-85%. And the shape should be rectangle with round chamfers (see Figure 1-7 and Figure 1-8).

• Pads at four corners

The stencil aperture should be designed with 60%~65% area of the corresponding pad (see Figure 1-7 and Figure 1-8).

• Ground pads at the center

The stencil aperture should be designed with 60%~65% area of the corresponding pad (see Figure 1-7 and Figure 1-8).

• Arc-shaped pad

There is no need to design stencil apertures for the arc-shaped pad marked in wathet blue color.

1.7.Module laser marking

Refer to Figure 1-9 for the module laser marking of TurboX CM2290.

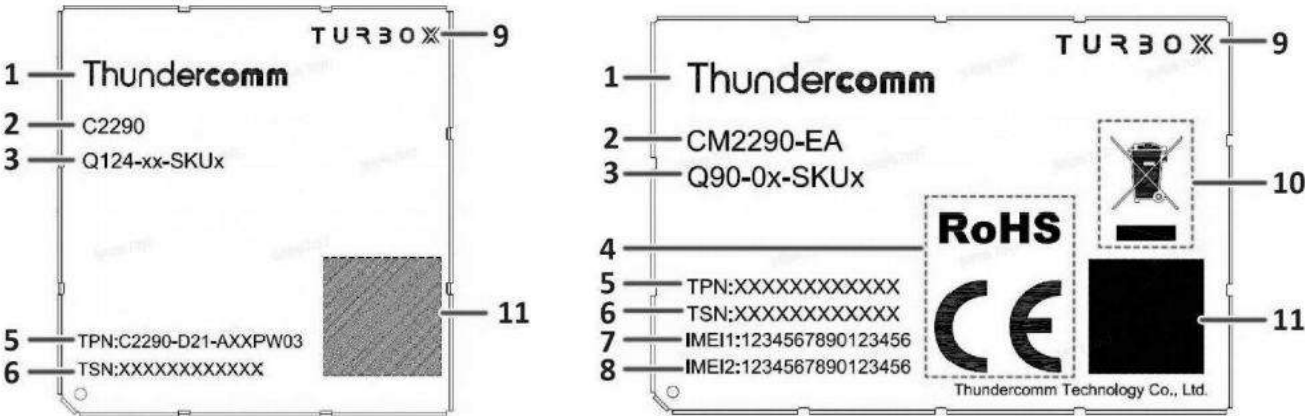


Figure 1-9.Laser Marking of CM2290 SOM

Table 1-3.Module laser marking description

1.Company name/logo	7. IMEI1 number
2.Product name	8. IMEI2 number
3.PCBA version	9. SOM brand
4.Certificate information	10. Eco-mark
5.Product number	11. QR code
6.Serial number	

—NOTE:

- Figure 1-9 is for reference only and may vary with the specific module.
- The part number may be updated.Please confirm with the supplier about the accurate information.

1.8.SMT assembly guide

To reduce module trial cost and improve project implementation efficiency,it is **strongly recommended to** comprehend TurboX Common SMT Assembly Guidelines and TurboX LCC/LGA Module Carrier Board Design Guidelines for DFM before the early stage of module layout design.

Additionally,if necessary,you can contact us at service@thundercomm.com for assistance in review of PCBA placement design.

Chapter 2.Interface Description

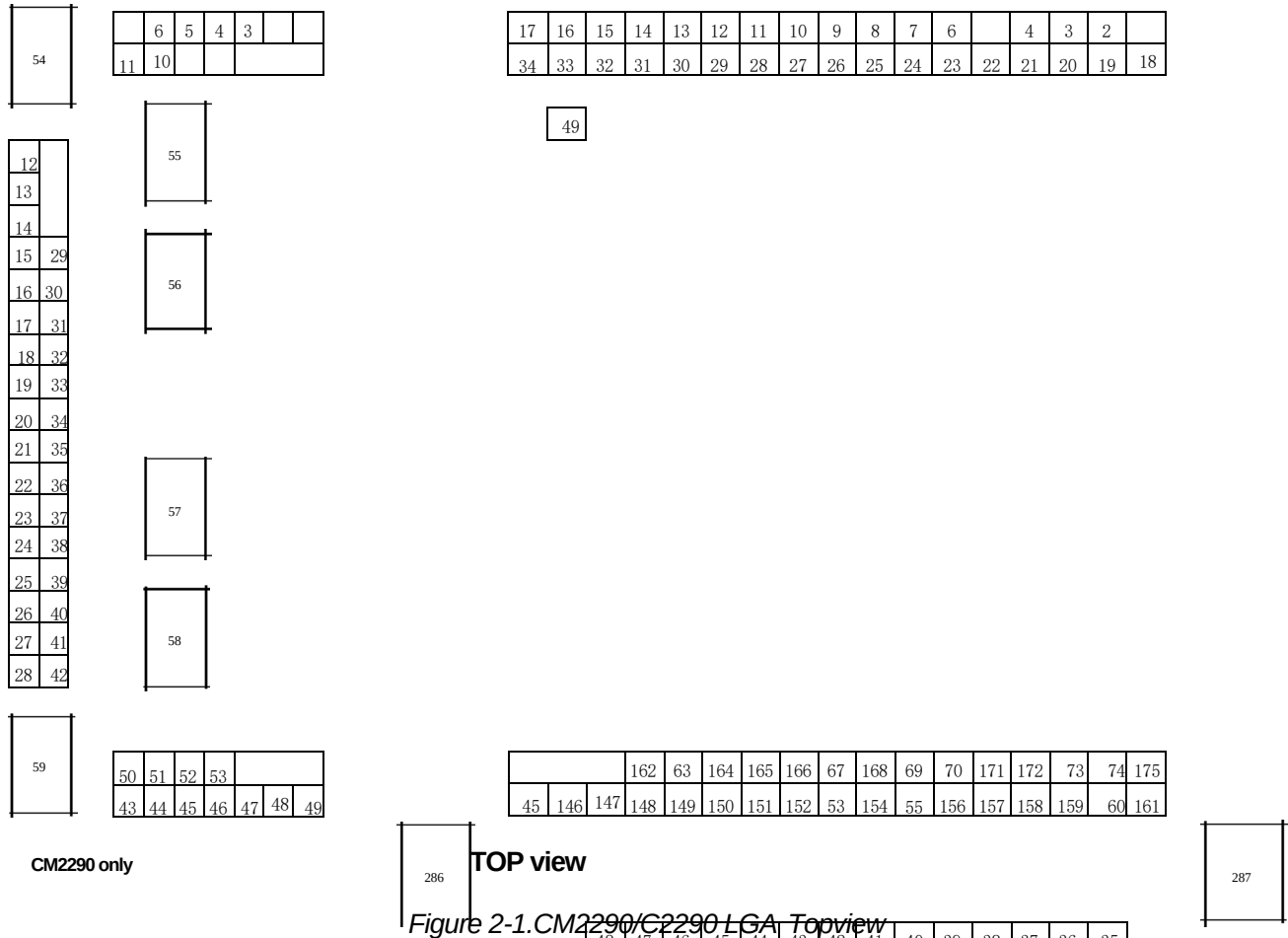
This chapter introduces all the interfaces definitions, purpose is to guide developer easy to design with Thundercomm TurboX C2290/CM2290 SOM.

2.1.Interfaces parameter definitions

Table 2-1.Interface description

Symbo	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP:pdpu = default no-pull with programmable options following the colon (:) PD:nppukp = default pull-down with programmable options following the colon (:) PU:nppdkp = default pull-up with programmable options following the colon (:) KP:nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pul
OD	Open drain
PD	Contains an internal pull-down device
PI	Power input
PO	Power output
PU	Contains an internal pull-up device

2.2.Interfaces detail description



①NOTE: The additional pins of CM2290 have been allocated independent group at the left side of LGA.

Table 2-2.Pin assignment

Pad No.	Pad Name	GPI	No	Function	Configurable Functions	Pad Voltage	Pad Type	Description
1	SDC2_DATA_1	83	100	15	127	1.8/2.97	BH	Secure digital data
2	SDC2_CMD	86	103	118	130	1.8/2.97	BH	Secure digital command
9	CSI1_B1_LN1_M	88	105	120	132	CSI	A1, A0	MIPI CSI (DPHY), differential lane 1-minus
10	CSI1_A1_LN1_P	91	108			CSI	A1, A0	MIPI CSI (DPHY), differential lane 1-plus
11	CSI0_C1_LN2_P					CSI	A1, A0	MIPI CSI0 (DPHY), differential lane 2-plus
12	CSI0_A2_LN2_M					CSI	A1, A0	MIPI CSI0 (DPHY), differential lane 2-minus
13	CSI0_B1_LN1_M					CSI	A1, A0	MIPI CSI0 (DPHY), differential lane 1-minus

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
14	CSIO_A1_LN1_P				CSI	A1, A0	MIPI CSIO(DPHY), differential lane 1-plus
18	SDC2_DATA_3				1.8/2.97	BH-PD: nppukp	Secure digital controller 2 data bit 3
19	SDC2_DATA_2				1.8/2.97	BH-PD: nppukp	Secure digital controller 2 data bit 2
20	SDC2_DATA_0				1.8/2.97	BH-PD: nppukp	Secure digital controller 2 data bit 0
21	SDC2_CLK				1.8/2.97	BH-NP: pdpukp	Secure digital controller 2 clock
26	CSI1_A2_LN2_M				CSI	A1, A0	MIPI CSI1(DPHY), differential lane 2-minus
27	CSI1_C1_LN2_P				CSI	A1, A0	MIPI CSI1(DPHY), differential lane 2-plus
28	CSI1_B2_LN3_P				CSI	A1, A0	MIPI CSI1(DPHY), differential lane 3-plus
29	CSI1_C2_LN3_M				CSI	A1I, A0	MIPI CSI1(DPHY), differential lane 3-minus
30	CSIO_C2_LN3_M				CSI	A1, A0	MIPI CSIO(DPHY), differential lane 3-minus
31	CSIO_B2_LN3_P				CSI	A1, A0	MIPI CSIO(DPHY), differential lane 3-plus
35	CCI_12C_SCL0	GPIO_23	N		1.8	B-PD: nppukp	Configurable I/O
				CCI_12C_SCL0		D0	Dedicated camera control interface I2C0 clock
				QDSS_GPIO_TRACE DATA_LOCA[7]		D0	QDSS trace data bit 7 A
36	CCI_12C_SDA0	GPIO_22	N		1.8	B-PD: nppukp	Configurable I/O
				CCI_12C_SDA0		B	Dedicated camera control interface I2C0 serial data
				QDSS_GPIO_TRACE DATA_LOCA[6]		D0	QDSS trace data bit 6 A
37	CAM_MCLK1	GPIO_21	N		1.8	B-PD: nppukp	Configurable I/O
				CAM_MCLK1		D0	Cameramaster clock 1
				QDSS_GPIO_TRACE DATA_LOCA[5]		D0	QDSS trace data bit 5 A
38	CSI1_C0_LN0_M				CSI	A1, A0	MIPI CSI1(DPHY), differential lane 0-minus

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
39	CSI1_BO_LNO_P				CSI	A1, AO	MIPI CSI 1 (DPHY), differential lane 0-plus
40	CSI1_NC_CLK_P				CSI	A1, AO	MIPI CSI 1 (DPHY), differential clock-plus
41	CSI1_AO_CLK_M				CSI	A1, AO	MIPI CSI1 (DPHY), differential clock-minus
42	CSIO_BO_LNO_P				CSI	A1, AO	MIPI CSIO (DPHY), differential lane 0-plus
43	CSIO_CO_LNO_M				CSI	A1, AO	MIPI CSIO (DPHY), differential lane 0-minus
44	CSIO_AO_CLK_M				CSI	A1, AO	MIPI CSIO (DPHY), differential clock-minus
45	CSIO_NC_CLK_P				CSI	A1, AO	MIPI CSI 0 (DPHY), differential clock-plus
46	MIPI_DSI1_CLK_P				DSI	A1, AO	MIPI DSI1 (DPHY), differential clock-plus
47	MIPI_DSI1_CLK_M				DSI	A1I, AO	MIPI DSI1 (DPHY), differential clock-minus
50	LCD0_RST	GPIO_28	Y		1.8	B- PD:nppukp	Configurable I/O
				CAM_MCLK3		DO	Camera master clock 3
				CCI_TIMER2		DO	Camera control interface timer 2
				QDSS_CTL_TRIGO_OUT_MIRB		DO	QDSS trigger output 0 B
				PWM[1]		DO	PWM output 1
51	NFC_CLK_REQ	GPIO_44	N		1.8	B- PD:nppukp	Configurable I/O
				GRFC7		DO	Generic RF controller bit 7
				BOOT_CONFIG[9]		DI	Boot configuration control bit 9
52	CCI_12C_SCL1	GPIO_30	N		1.8	B- PD:nppukp	Configurable I/O
				CCI_12C_SCL1		DO	Dedicated camera control interface I2C1 clock
53	LCD_TE	GPIO_81	Y		1.8	B- PD:nppukp	Configurable I/O
				MDP_VSYNC_OUT_0		DO	MDP vertical sync-output 0
				MDP_VSYNC_OUT_1		DO	MDP vertical sync-output 1

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
				MDP_VSYNC_P		DI	MDP vertical sync-primary
54	NFC_INT_N	GPIO_70	Y		1.8	B- PD:nppukp	Configurable I/O
				SPI_CS_N		DO	QUP 0 SE1, lane 3 :SPI_CS_N
				UART_RX		DI	QUP 0 SE1, lane 3:UART_RX
				GCC_GP3_CLK_MIR A		DO	Global general purpose clock 3 A
				QDSS_GPIO_TRACE DATA_LOCB[13]		DO	QDSS trace data bit 13 B
55	NFC_12C_SCL	LPI_GPIO_22	N		1.8	B- PD:nppukp	Configurable I/O
				SPI_MOSI		DO	LPI_QUP 0 SE1, lane 1: SPI_MOSI
				UART_RFR		DO	LPI_QUP 0 SE1, lane 1: UART_RFR
				12C_SCL		DO	LPI_QUP 0 SE1, lane 1: 12C_SCL
				3C_SCL		DO	LPI QUP 0 SE1, lane 1 13C_SDA
56	TP_RST	GPIO_71	N		1.8	B- PD:nppukp	Configurable I/o
				SPI_SCLK		DO	QUP 0 SE2, lane 2 :SPI_SCLK
				UART_TX		DO	QUP 0 SE 2, lane 2: UART_TX
57	NFC_SPI_MOS	GPIO_01	N		1.8	B- PD:nppukp	Configurable I/o
				SPI_MOSI		DO	QUP 0 SE0, lane 1: SPI_MOSI
				UART_RFR		DO	QUP 0 SE0, lane 1: UART_RFR
				12C_SCL		DO	QUP 0 SE0, lane 1:12C_SCL
				3C_SCL		DO	QUP 0 SE0, lane 1:13C_SCL
				QDSS_GPIO_TRACE DATA_LOCB[9]		DO	QDSS trace data bit 9 B
58	CCI_I2C_SDA1	GPIO_29	N		1.8	B- PD:nppukp	Configurable I/o
				CCI_2C_SDA1		B	Dedicated camera control interface 12C1 serial data

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
59	NFC_SPI_MISO	GPIO_00	Y		1.8	B PD:nppukp	Configurable I/O
				SPI_MISO		DI	QUP 0 SE0, lane 0: SPI_MISO
				UART_CTS		DI	QUP 0 SE0, lane 0: UART_CTS
				12C_SDA		B	QUP 0 SE0, lane 0:12C_SDA
				3C_SDA		B	QUP 0 SE0, lane 0:13C_SDA
				QDSS_GPIO_TRACE DATA_LOCB[8]		DO	QDSS trace data bit 8 B
60	NFC_SPI_SCLK	GPIO_02	N		1.8	B- PD:nppukp	Configurable I/O
				SPI_SCLK		DO	QUP 0 SE0, lane 2:SPI_SCLK
				UART_TX		DO	QUP 0 SE0, lane 2:UART_TX
				QDSS_GPIO_TRACE DATA_LOCB[10]		DO	QDSS trace data bit 10 B
61	NFC_12C_SDA	LPI_GPIO_21	Y		1.8	B- PD:nppukp	Configurable I/O
				SPI_MISO		DI	LPI_QUP 0 SE1, lane 0: SPI_MISO
				UART_CTS		D	LPI_QUP 0 SE1, lane 0: UART_CTS
				12C_SDA		B	LPI_QUP 0 SE1, lane 0: 12C_SDA
				13C_SDA		B	LPI_QUP 0 SE1, lane 0: 13C_SDA
62	NFC_SPI_CS_N	GPIO_03			1.8	B- PD:nppukp	Configurable I/O
				SPI_CS_N_0		DO	QUP 0 SE0, lane 3:SPI_CS_N
				UART_RX		DI	QUP 0 SE0, lane 3:UART_RX
				QDSS_GPIO_TRACE DATA_LOCB[11]		DO	QDSS trace data bit 11B
63	NFC_DWL_REQ	GPIO_31	Y		1.8	B- PD:nppukp	Configurable I/O
				GP_PDM_MIRB[0]		DO	General-purpose PDM_Mirror_B0

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
64	CAM_MCLK0	GPIO_20	N		1.8	B- PD:nppukp	Configurable I/O
				CAM_MCLK0		DO	Camera master clock 0
				QDSS_GPIO_TRACE DATA_LOCA[4]			QDSS trace data bit4A
65	CAM1_RST	GPIO_19	Y		1.8	B- PD:nppukp	Configurable I/O
				QDSS_GPIO_TRACE DATA_LOCA[3]		DO	QDSS trace data bit 3A
66	BOOT_CONFIG_2	GPIO_51	N		1.8	B- PD:nppukp	Configurable I/O
				GRFC14		DO	Generic RF controller bit 14
				BOOT_CONFIG[2]		DI	Boot configuration control bit 2
				PWM[2]		DO	PWM output 2
67	NFC_EN	GPIO_69	Y		1.8	B- PU:nppukp	Configurable I/O
				SPI_SCLK		DO	QUP 0 SE1, lane 2 :SPI_SCLK
				UART_TX		DO	QUP 0 SE1, lane 2:UART_TX
				GCC_GP2_CLK_MIR A		DO	Global general-purpose clock 2 A
				QDSS_GPIO_TRACE DATA_LOCB[12]		DO	QDSS trace data bit 12 B
68	CAM0_1V8_EN	GPIO_52	N		1.8	B- PD:nppukp	Configurable I/O
				GRFC15		DO	Generic RF controller bit 15
				NAV_GPIO_2_MIR A		B	Generic I/O for GNSS
72	WDOG_DISABLE	GPIO_48	N		1.8	B- PD:nppukp	Configurable I/O
				GRFC11		DO	Generic RF controller bit 11
				QDSS_GPIO_TRACE DATA_LOCA[15]		DO	QDSS trace data bit 15 A
				BOOT_CONFIG[0]		DI	Boot configuration control bit 0

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
73	PRESS_INT	GPIO_97	Y		1.8	B- PD:nppukp	Configurable I/O
				SPI_MOSI		DO	QUP 0 SE4, lane 1: SPI_MOSI
				UART_RFR		DO	QUP 0 SE4, lane 1: UART_RFR
				I2C_SCL		DO	QUP 0 SE4, lane1:I2C_SCL
				NAV_GPIO_2_MIR C		B	Generic IO for GNSS
				MDP_VSYNC_s		DI	MDP vertical sync-secondary
				GP_PDM_MIRA[2]		DO	General-purpose PDM_Mirror_A 2
				QDSS_CTI_TRIGO_OUT_MIRA		DO	QDSS trigger output 0 A
				QDSS_CTI_TRIG1_N_MIRA		DI	QDSS trigger input 1A
74	WSAI_EN	GPIO_42	N		1.8	B- PD:nppukp	Configurable I/O
				GRFC5		DO	Generic RF controller bit 5
				NAV_GPIO_1_MIR A		B	Generic IO for GNSS
75	CLK_GPS				1.8	DO	Clock for GNSS (C2290 only; for CM2290, this pin is NC)
76	MIPI_DSIO_L1_M				DSI	A1, A0	MIPI DSI 0 (DPHY) differential lane 1-minus
77	MIPI_DSIO_L2_M				DSI	A1, A0	MIPI DSI 0 (DPHY), differential lane 2-minus
78	MIPI_DSIO_CLK_P				DSI	A1, A0	MIPI DSI 0 (DPHY) differential clock-plus
79	MIPI_DSIO_L0_M				DSI	A1, A0	MIPI DSI 0 (DPHY), differential lane 0-minus
80	MIPI_DSIO_L3_P				DSI	A1, A0	MIPI DSI 0 (DPHY) differential lane 3-plus
81	CAM_MCLK2	GPIO_27	Y		1.8	B- PD:nppukp	Configurable I/o
				CAM_MCLK2		DO	Camera master clock 2
				QDSS_CTI_TRIGO_I N_MIRB		DO	QDSS trigger input 0 B

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
82	APPS_12C_SDA	GPIO_04	Y		1.8	B- PD:nppukp	Configurable I/O
				SPI_MISO		DI	QUP 0 SE1, lane 0: SPI_MISO
				UART_CTS		DI	QUP 0 SE1, lane 0: UART_CTS
				I2C_SDA		B	QUP 0 SE1, lane 0:I2C_SDA
83	APPS_12C_SCL	GPIO_05	N		1.8	B- PD:nppukp	Configurable I/O
				SPI_MOSI		DO	QUP 0 SE1, lane 1: SPI_MOSI
				UART_RFR		DO	QUP 0 SE1, lane 1: UART_RFR
				I2C_SCL		DO	QUP 0 SE1, lane 1:I2C_SCL
85	HDMI_OUT_INT	GPIO_39	Y		1.8	B- PD:nppukp	Configurable I/O
				GRFC2		DO	Generic RF controller bit 2
86	VREG_L19A_1P8					PO	L19 LDO regulated output, only used for UIM2
87	ANT_FM_RX					A1	FM headset antenna. If not used, connect to ground.
88	DBG_UART_RX	GPIO_13	Y		1.8	B- PD:nppukp	Configurable I/O
				UART_RX		DI	QUP 0 SE4, lane 3:UART_RX
				SPI_CS_N		DO	QUP 0 SE4, lane 3: SPI_CS_N
90	HDMI_IN_INT	GPIO_36			1.8	B- PD:nppukp	Configurable I/o
93	MIPI_DSIO_L1_P				DSI	A1, AO	MIPI DSIO (DPHY), differential lane 1-plus
94	MIPI_DSIO_L2_P				DSI	A1, AO	MIPI DSIO (DPHY), differential lane 2-plus
95	MIPI_DSIO_CLK_M				DSI	A1, AO	MIPI DSIO (DPHY), differential clock-minus
96	MIPI_DSIO_L0_P				DSI	A1, AO	MIPI DSIO (DPHY), differential lane 0-plus
97	MIPI_DSIO_L3_M				DSI	A1, AO	MIPI DSIO (DPHY), differential lane 3-minus

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
99	WCD_RST	GPIO_82	N		1.8	B- PD:nppukp	Configurable I/O
				SPI_CS_N_1		DO	QUP 0 SE0, lane 4 :SPI_CS_N_1
				PWM[6]		DO	PWM output 6
100	TS_2C_SDA	GPIO_06	Y		1.8	B- PD:nppukp	Configurable I/O
				SPI_MISO		DI	QUP 0 SE2, lane 0: SPI_MISO
				UART_CTS		DI	QUP 0 SE2, lane 0: UART_CTS
				2C_SDA		B	QUP 0 SE2, lane 0:2C_SDA
101	HW_VERSION	PM_GPIO_01					Reserved. Pull up pull down resistor inside SOM. Float this pin
102	SNSR_12C_SDA	GPIO_109	Y		1.8	B- PD:nppukp	Configurable I/O
				QDSS_GPIO_TRACE DATA_LOCB[2]		DO	QDSS trace data bit 2 B
				LPI_GPIO_19:12C_SDA		B	LPI_QUP 0 SE0, lane 0: 12C_SDA
				LPI_GPIO_19:13C_SDA		B	LPI_QUP 0 SE0, lane 0: 13C_SDA
103	SNSR_12C_SCL	GPIO_110	N		1.8	B- PD:nppukp	Configurable I/O
				QDSS_GPIO_TRACE DATA_LOCB[3]		DO	QDSS trace data bit 3 B
				LPI_GPIO_20:12C_SCL		DO	LPI_QUP 0 SE0, lane 1: 12C_SCL
				LPI_GPIO_20:13C_SCL		DO	LPI_QUP 0 SE0, lane 1: 13C_SCL
104	DBG_UART_TX	GPIO_12	N		1.8	B- PD:nppukp	Configurable I/O
				UART_TX		DO	QUP 0 SE4, lane 2:UART_TX
				SPI_SCLK		DO	QUP 0 SE4, lane 2:SPI_SCLK
106	VREG_L14A_1P8					PO	L13 LDO regulated output
108	USB_SS_SEL	GPIO_45	N		1.8	B- PD:nppukp	Configurable I/O
				GRFC8		DO	Generic RF controller bit 8
				BOOT_CONFIG[10]		DI	Boot configuration control bit 10

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
110	IO_GNSS_BB_IP					A1	GNSS receiver baseband input, in-phase plus. C2290 only. CM2290 NC this pin.
111	IO_GNSS_BB_QP					A1	GNSS receiver baseband input, quadrature plus. C2290 only. CM2290 NC this pin.
112	VREG_L10A_1P3					P0	L10 LDO regulated output
113	VREG_L16A_1P8					P0	L16 LDO regulated output
114	CAN_INT	GPIO_46	Y		1.8	B-PD:nppukp	Configurable I/O
				GRFC9		D0	Generic RF controller bit 9
				BOOT_CONFIG[11]		DI	Boot configuration control bit 11
116	LPI_GPIO_26	LPI_GPIO_26	Y		1.8	B-PD:nppukp	Configurable I/O
				SPL_CS_N		D0	LPI_QUP 0 SE1, lane 3: SPI_CS_N
				UART_RX		DI	LPI_QUP 0 SE1, lane 3: UART_RX
				UART_RX		DI	LPI_QUP 0 SE6, lane 3: UART_RX
117	LPI_GPIO_25	LPI_GPIO_25	N		1.8	B-PD:nppukp	Configurable I/o
				SPI_SCLK		D0	LPI_QUP 0 SE1, lane 2: SPI_SCLK
				UART_TX		D0	LPI_QUP 0 SE1, lane 2: UART_TX
				UART_TX		D0	LPI_QUP 0 SE6, lane 2: UART_TX
118	TPO_INT	GPIO_54	N		1.8	B-PD:nppukp	Configurable I/o
				RFFE1_CLK		D0	RF front-end 1 interface clock
119	TS_12C_SCL	GPIO_07	N		1.8	B-PD:nppukp	Configurable I/o
				SPI_MOSI		D0	QUP 0 SE2, lane 1: SPI_MOSI
				UART_RFR		D0	QUP 0 SE2, lane 1: UART_RFR
				12C_SCL		D0	QUP 0 SE2, lane 1: 12C_SCL

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
120	USB_SS-H_HS-L_SEL		N			DI	Connect to micro USBID. Reserve this pin when CM2290-SKU1/CM2290-SKU2
123	EXT_GPS_LNA_EN0	GPIO_63	Y		1.8	DO	Reverve for CM229. Only used for GNSS system in C2290 design.
124	BOOT_CONFIG_1	GPIO_50	N		1.8	B- PD:nppukp	Configurable I/o
				GRFC13		DO	Generic RF controller bit 13
				BOOT_CONFIG[1]		DI	Boot configuration control bit 1
125	CAMO_DVDD_EN	GPIO_25	Y		1.8	B- PD:nppukp	Configurable I/o
				CCI_ASYNC_IN0		DI	Camera control interface async o
				CCI_TIMER0		DO	Cameracontrol interface timer 0
				QDSS_GPIO_TRACE_DATA_LOCA[9]		DO	QDSS trace data bit 9A
128	SM_GPIO_111	GPIO_111	N		1.8	B- PD:nppukp	Configurable I/O
				LPI_GPIO_23:UART_CTS		DI	LPI_QUP 0 SE5, lane 0:UART_CTS
				LPI_GPIO_23:12C_sDA		B	LPI_QUP 0 SE5, lane 0: 12C_SDA
				LPI_GPIO_23:UART_TX		DO	LPI_QUP 0 SE5, lane 2:UART_TX
129	UIM1_DATA	GPIO_76			1.8/2.95	B- PD:nppukp	Configurable I/o
				UIM1_DATA		B	Uim1 data(dual voltage)
130	UIM1_CLK	GPIO_77	N		1.8/2.95	B- PD:nppukp	Configurable I/o
				UIM1_CLK		DO	UIM1 clock (dual voltage)
131	UIM2_DATA	GPIO_72	Y		1.8/2.95	B- PD:nppukp	Configurable I/o
				UIM2_DATA		B	UIM2 data(dual voltage)
				QDSS_CTI_TRIG1_N_MIRB		DI	QDSS trigger input 1B
				PWM[3]		DO	PWM output 3

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
132	UIM2_CLK	GPIO_73	N		1.8/2.95	B- PD:nppukp	Configurable I/O
				UIM2_CLK		DO	UIM2 clock (dual voltage)
				QDSS_CTL_TRIG1_OUT_MIRB		DO	QDSS trigger output 1B
133	ACCL_INT1	GPIO_32	Y		1.8	B- PD:nppukp	Configurable I/O
				CCI_TIMER3		DO	Camera control interface timer 3
				GP_PDM_MIRB[1]		DO	General-purpose PDM_Mirror_B1
134	WGR_GNSS_SSBI_TX	GPIO_59	N		1.8	B- PD:nppukp	Configurable I/O
				RFEE4_DATA		B	RF front-end 4 interface data
				SSBI_WTR1_TX		DO	Single serial bus interface transmitter
				BOOT_CONFIG[6]		DI	Boot configuration control bit 6
135	WGR_GNSS_SSBI_RX	GPIO_60	N		1.8	B- PD:nppukp	Configurable I/O
				RFEE4_CLK		DO	RF front-end 4 interface clock
				SSBI_WTR1_RX		DI	Single serial bus interface receiver
139	SM_GPIO_112	GPIO_112	Y		1.8	B- PD:nppukp	Configurable I/O
				LPI_GPIO_24:UART_RFR		DO	LPI_QUP 0 SE5, lane 1:UART_RFR
				LPI_GPIO_24:12C_SCL		DO	LPI_QUP 0 SE5, lane 1:12C_SCL
				LPI_GPIO_24:UART_RX		DI	LPI_QUP 0 SE5, lane 3:UART_RX
140	UIM1_RESET	GPIO_78			1.8/2.95	B- PD:nppukp	Configurable I/O
				UIM1_RESET		DO	UIM1 reset (dual voltage)
141	UIM1_PRESENT	GPIO_79	Y		1.8	B- PD:nppukp	Configurable I/O
				UIM1_PRESENT		D	UIM1 presence detection

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
142	UIM2_PRESENT	GPIO_75	Y		1.8	B- PD:nppukp	Configurable I/O
				UIM2_PRESENT		D	UIM2 presence detection
				PWM[5]		DO	PWM output 5
143	MI25_MCLK1_A	GPIO_108	N		1.8	B- PD:nppukp	Configurable I/O
				NAV_GPIO_2_MIR B		B	Generic IO for GNSS
				LPI_GPIO_18:MI25 _MCLK1_A		DO	MI2S Master Clock 1_A
144	WSA1_INT	GPIO_37	N		1.8	B- PD:nppukp	Configurable I/O
				GRFCO		DO	Generic RF controller bit 0
146	ANT_2G_5G_WLAN					A1/A0	2.4G WLAN RF Tx/Rx, 5G WLAN/BT Tx/Rx
148	MAG_INT_N	GPIO_34	Y		1.8	B- PD:nppukp	Configurable I/o
149	USB_CC2					AI	CC2 pin for the USB Type-C connector. Requires IEC ESD protection. Reserve this pin when using CM2290-SKU5/C2290-SKU2.
150	TCA2_INT	PM_GPIO_03			MVnote		Configurable; default digital input with 10 μ A pull-down
151	HDMI_IN_RST	PM_GPIO_04			Mynote ₂		Configurable; default digital input with 10 μ A pull-down
153	VBATT_VSNS_P					AI	Battery voltage sense input plus. Connect to the battery positive remote sense node or connect this directly to the battery positive node
154	BL_PWM_OUT	PM_GPIO_02			Mvnote2		Configurable; default digital input with 10 μ A pull-down
155	KYPD_VOL_DOW N_N				1.8	DI	Input pad used for generating a stage 2 and/or stage 3 reset when held at a logic low
156, 170	VREG_L15A_1P8					P0	L15 LDO regulated output
157	VREG_L17A_3P0					P0	L17 LDO regulated output
159	CLK_NFC					DO	RF XO clock digital buffer output 3

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
160	HSDET_L					A1	Headset detection
161	AMIC3_INP					A1	Microphone input 3, positive
162	ALSP_INT_N	GPIO_35	Y		1.8	B- PD:nppukp	Configurable I/O
163	USB_CC1					A1	OTG mode enable or CC1 pin for the USB Type-C connector(user programmable).Require IEC protection.Reserve this pin when usingCM2290-SKU5/C2290-SKU2.
165	PM_GPIO_08	PM_GPIO_08			1.8		Configurable;default digital input with 10 μ A pull-down
166	TCA1_INT	GPIO_80	Y		1.8	B- PD:nppukp	Configurable I/O
				SPI_CS_N		DO	QUP 0 SE2, lane 3 :SPI_CS_N
				UART_RX		DI	QUP 0 SE2, lane 3:UART_RX
167	VBATT_VSNS_M					A1	Battery voltage sense input minus.Connect to the battery negative remote sense node or connect this directly to the battery negative node
168	PM_GPIO_09	PM_GPIO_09		Reserved for e-LDO	1.8	DO	Reserved for e-LDO PM_GPIO_09 is configured as an output and driven high during power on sequence to enable e-LDO. For non e-LDO instances, PM_GPIO_09 should not be used for general purpose.
173	MIC_BIAS3					AO	Microphone bias 3
174	MIC_BIAS1					AO	Microphone bias 1
175	AMIC3_INM					A1	Microphone input 3, negative
177	RED_LED					AO	RG LED low side current sink for the red LED
179	GYRO_INT	GPIO_33	Y		1.8	B- PD:nppukp	Configurable I/O
				GP_PDM_MIRB[2]		DO	General-purpose

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
							PDM_Mirror_B 2
180	FLASH_LED1					AO	Anode connection of flash LED 1. Connect cathode to nearest ground.
181	BATT_ID					AI	Battery ID input to the ADC It can be used for missing battery detection.
182, 183, 184	VPH_PWR					PI, PO	Primary system supply node, SCHG regulated node
185	PM_OPTION					AI	ADC based PON OPTION decode
186	VREG_USB_3P1					PO	eLDO regulated output
187	VREG_L13A_1P8					PO	L13 LDO regulated output
188	TCA2_RST	PM_GPIO_07			1.8		Configurable; default digital input with 10 μ A pull-down.
189	CHG_SKIN_THERM	PM_GPIO_05			1.8		Configurable; default digital input with 10 μ A pull-down.
190	MICBIAS2					AO	Microphone bias 2
191	GREEN_LED					AO	RG LED low side current sink for the green LED
193	KYPD_PWR_N					DI	Input pad generally connected to a keypad power-on button and when grounded, initiate the power-on sequence. Can also be configured for generating a stage 2 and/or stage 3 reset if held at a logic low for longer durations. Pulled up internally.
194	UIM2_RESET	GPIO_74	N		1.8/2.95	B- PD:nppukp	Configurable I/o
				UIM2_RESET		DO	UIM2 reset (dual voltage)
				PWM[4]		DO	PWM output 4
195, 196, 197, 202	VBATT					PI, PO	Battery voltage node, connected to BATFET. Output is for charging, and input is for all the other operations.

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
198	BATT_THERM					A1	Battery temperature input to ADC for measuring the pack temperature. It is used for charger safe operation and BMS/Qualcomm battery gauge.
199	USB_CONN_THERM	PM_GPIO_06			1.8		Configurable; default digital input with 10 μ A pull-down
200	KEY_VOLP_N	GPIO_96	Y		1.8	B- PD:nppukp	Configurable I/O
				SPI_MISO		DI	QUP 0 SE4, lane 0: SPI_MISO
				UART_CTS		DI	QUP 0 SE4, lane 0: UART_CTS
				I2C_SDA		B	QUP 0 SE4, lane 0: I2C_SDA
				NAV_GPIO_1_MIR C		B	Generic IO for GNSS
				MDP_VSYNC_E		DI	MDP vertical sync-external
				GP_PDM_MIRA[1]		DO	General-purpose PDM_Mirror_A1
				SD_WRITE_PROTECT		DO	SD card write protect
				QDSS_CTI_TRIG0_1 N_MIRA		DI	QDSS trigger input 0A
				QDSS_CTI_TRIG1_ OUT_MIRA		DO	QDSS trigger output 1A
205, 206	USB_VBUS					PI, PO	Input power from the source (USB), or output during USB-OTG. This is a power entry node for the charger and connects to the OVP circuitry.
207	VIB_DRV_LDO_P					PO	High side output for vibrator
209	USB0_HS_DM					A1, AO	USB0 high-speed data-minus
210	USB0_HS_DP					A1, AO	USB0 high-speed data-plus

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
211	CHG_LED_SINK					A1	Charger Indication LED driver, connects to LED cathode
213	CAN_SPI_CS2	GPIO_86	Y		1.8	B- PD:nppukp	Configurable I/O
				SPI_CS_N_2		DO	QUP 0 SE0, lane 5 :SPI_CS_N_2
				GCC_GP1_CLK_MIRB		DO	Global general-purpose clock 1B
216	CBL_PWR_N					DI	Alternate input pad, which can be used to initiate the power-on sequence when grounded; pulled up internally.
217	HPH_L					AO	Headphone output, left channel
218	VCOIN				2.5~3.2	A1, AO	Coin-cell battery/capacitor or backup battery charger supply and input. Last remaining available source to maintain xVdd backed registers.
219	AMIC1_INP					AI	Microphone input 1, positive
220	AMIC1_INM					AI	Microphone input 1, negative
221	AMIC2_INP					AI	Microphone input 2, positive
225	USB0_SS_RX1_P					A1	USB0 super-speed receive 1-plus
226	USB0_SS_RX1_M					A1	USB0 super-speed receive 1-minus
227	USB0_SS_TX1_M					AO	USB0 super-speed transmit 1-minus
228	USB0_SS_TX1_P					AO	USB0 super-speed transmit 1-plus
229	CAMO_RST	GPIO_18	Y		1.8	B- PD:nppukp	Configurable I/O
				QDSS_GPIO_TRACE_DATA_LOCA[2]		DO	QDSS trace data bit24
				PWM[0]		DO	PWM output 0

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
232	CAMO_AVDD_EN	GPIO_26			1.8	B- PD:nppukp	Configurable I/O
				QDSS_GPIO_TRACE DATA_LOCA[10]		DO	QDSS trace data bit 10 A
233	SD_DET_IN	GPIO_88	Y		1.8	B- PD:nppukp	Configurable I/O
234	HPH_R					AO	Headphone output, right channel
235	HPH_REF					GND	Headphone ground reference
236	EAR_OUT_M					AO	Earpiece output, negative
237	EAR_OUT_P					AO	Earpiece output, positive
238	AMIC2_INM					A1	Microphone input 2, negative
243	FAN_PWM	GPIO_106	Y		1.8	B- PD:nppukp	Configurable I/O
				NAV_GPIO_0_MIR B		B	Generic IO for GNSS
				GCC_GP3_CLK_MIR B		DO	Global general purpose clock 3 B
				QDSS_GPIO_TRACE CTL_LOCB		DO	QDSS trace control B
				LPI_GPIO_16:LPI_ MI252_DATA0		B	LPI_MI2S 2 Data 0
244	FORCED_USB_BOOT_POL_SEL			FORCED_USB_BOOT_POL_SEL		DI	Forced USB boot polarity select
247	WSA2_INT	GPIO_107			1.8	B- PD:nppukp	Configurable I/O
				NAV_GPIO_1_MIR B		B	Generic IO for GNSS
				GCC_GP2_CLK_MIR B		DO	Global general-purpose clock 2 B
				QDSS_GPIO_TRACE DATA_LOCB[0]		DO	QDSS trace data bit 0 B
				LPI_GPIO_17:LPI_ MI252_DATA1		B	LPI_MI252 Data 1
				LPI_GPIO_17:MI25 _MCLK1_C		DO	MI2S Master Clock 1_C
248	HDMI_OUT_RST	GPIO_47	N		1.8	B- PD:nppukp	Configurable I/O
				GRFC10		DO	Generic RF controller bit10

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
				NAV_GPIO_0_MIR A		B	Generic IO for GNSS
				QDSS_GPIO_TRACE DATA_LOCA[14]		DO	QDSS trace data bit 14 A
250	CAM2_RST	GPIO_24	Y		1.8	B- PD:nppukp	Configurable I/O
				CCI_TIMER1		DO	Camera control interface timer 1
				GCC_GP1_CLK_MIR A		DO	Global general-purpose clock 1
				QDSS_GPIO_TRACE DATA_LOCA[8]		DO	QDSS trace data bit 8 A
251	VREG_L21A_2P96					PO	L21 LDO regulated output
252	CDC_LO_M					AO	Line output, negative
253	CDC_LO_P					AO	Line output, positive
254	SPI_SCLK	GPIO_16	N		1.8	B- PD:nppukp	Configurable I/o
				UART_TX		DO	QUP 0 SE5, lane 2:UART_TX
				SPI_SCLK		DO	QUP 0 SE5, lane 2 :SPI_SCLK
				QDSS_GPIO_TRACE DATA_LOCB[6]		DO	QDSS trace data bit 6 B
255	SPI_MISO	GPIO_14	Y		1.8	B- PD:nppukp	Configurable I/O
				SPI_MISO		DI	QUP 0 SE5, lane 0: SPI_MISO
				UART_CTS		DI	QUP 0 SE5, lane 0: UART_CTS
				I2C_SDA		B	QUP 0 SE5, lane 0:I2C_SDA
				QDSS_GPIO_TRACE DATA_LOCB[4]		DO	QDSS trace data bit 4B
259	DMIC_DATA_1	GPIO_99	Y		1.8	B- PD:nppukp	Configurable I/o
				LPI_GPIO_7:LPI_D MIC1_DATA		DI	LPI_Digital MIC1 data
				LPI_GPIO_7:LPI_MI 250_WS		DO	LPI_MI2S 0Word Select

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
261	DMIC_DATA_2	GPIO_101	Y		1.8	B- PD:nppukp	Configurable I/O
				LPI_GPIO_9:LPI_D MIC2_DATA		DI	LPI_Digital MIC2 Data
				LPI_GPIO_9:LPI_MI 250_DATA1		B	LPI_MI2S 0 Data 1
				LPI_GPIO_9:MI2S_ MCLK1_B		DO	Master Clock 1B
262	MI2S1_WS	GPIO_103	Y		1.8	B- PD:nppukp	Configurable I/O
				LPI_GPIO_11:LPI_ MI2S1_WS		DO	LPI_MI2S 1Word Select
				LPI_GPIO_11:LPI_D MIC4_DATA		DI	LPI_Digital MIC4 Data
263	VREG_L4A_2P96					PO	L4 LDO regulated output
264	VREG_L18A_1P8					PO	L18 LDO regulated output
266	SPI_CS	GPIO_17	Y		1.8	B- PD:nppukp	Configurable I/o
				UART_RX		DI	QUP 0 SE5, lane 3:UART_RX
				SPI_CS_N		DO	QUP 0 SE5, lane 3 :SPI_CS_N
				QDSS_GPIO_TRACE DATA_LOCB[7]		DO	QDSS trace data bit 7 B
267	SPI_MOSI	GPIO_15			1.8	B- PD:nppukp	Configurable I/O
				SPI_MOSI		DO	QUP 0 SE5, lane 1: SPI MOS
				UART_RFR		DO	QUP 0 SE5, lane 1: UART_RFR
				I2C_SCL		DO	QUP 0 SE5, lane1:I2C_SCL
				QDSS_GPIO_TRACE DATA_LOCB[5]		DO	QDSS trace data bit 5B

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
268	FORCED_USB_BOOT	GPIO_95	Y		1.8	B- PD:nppukp	Configurable I/O
				NAV_GPIO_0_MIR C		B	Generic IO for GNSS
				GP_PDM_MIRA[0]		DO	General-purpose PDM_Mirror_A 0
				QDSS_GPIO_TRACE DATA_LOCB[15]		DO	QDSS trace data bit 15 B
				FORCED_USB_BOOT		DI	The FORCE_USB_BOOT is checked first during the boot device detection, prior to BOOT_CONFIG GPIO states. GPIO_95=active (high or low) forces the device to boot from the USB_HS port. To disable the feature that forces USB boot using GPIO_95, blow the FORCE_USB_BOOT_DISABLE fuse.
270	CAM_MUX_EN	GPIO_113	N		1.8	B- PD:nppukp	Configurable I/o
271	TCA1_RST	GPIO_40	N		1.8	B- PD:nppukp	Configurable I/O
				GRFC3		DO	Generic RF controller bit 3
272	DMIC_CLK_1	GPIO_98	N		1.8	B- PD:nppukp	Configurable I/O
				LPI_GPIO_6:LPI_D MIC1_CLK		DO	LPI_Digital MIC1 Clock
				LPI_GPIO_6:LPI_MI 2S0_CLK		DO	LPI_MI2S0 Clock
273	DMIC_CLK_2	GPIO_100	N		1.8	B- PD:nppukp	Configurable I/O
				LPI_GPIO_8:LPI_D MIC2_CLK		DO	LPI_Digital MIC 2 Clock
				LPI_GPIO_8:LPI_MI 2S0_DATA0		B	LPI_MI2S 0 Data 0

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
274	MI2S1_CLK	GPIO_102	Y		1.8	B- PD:nppukp	Configurable I/O
				LPI_GPIO_10:LPI_MI2S1_CLK		DO	LPI_MI2S 1 Clock
				LPI_GPIO_10:LPI_DIG4_CLK		DO	LPI_Digital MIC4 Clock
277	USB0_SS_RX0_P					A1	USB0 super-speed receive 0-plus
278	USB0_SS_RX0_M					A1	USB0 super-speed receive 0-minus
279	USB0_SS_TX0_P					A0	USB0 super-speed transmit 0-plus
280	USB0_SS_TX0_M					A0	USB0 super-speed transmit 0-minus
281	SM_GPIO_41	GPIO_41	N		1.8	B- PD:nppukp	Configurable I/O
				GRFC4		DO	Generic RF controller bit 4
282	BOT_CFG_3	GPIO_53	N		1.8	B- PD:nppukp	Configurable I/O
				RFFE1_DATA		B	RF front-end 1 interface data
				GSM1_TX_PHASE_D		DO	GSM 1 transmit phase adjustdata bit
				BOOT_CONFIG[3]		DI	Boot configuration control bit 3
283	CAM_MUX_SEL	GPIO_114	N		1.8	B- PD:nppukp	Configurable I/o
284	MI2S1_DATA1	GPIO_105	Y		1.8	B- PD:nppukp	Configurable I/O
				QDSS_GPIO_TRACE_CLK_LOCB		DO	QDSS trace clock B
				LPI_GPIO_13:LPI_DIG3_DATA		D	LPI_Digital MIC3 Data
				LPI_GPIO_13:LPI_MI2S1_DATA1		B	LPI_MI2S 1 Data 1
				LPI_GPIO_13:MI2S1_MCLK0_A		DO	MI2S Master Clock0A

Pad No.	Pad Name	GPIO No.	Wake-up Function	Configurable Functions	Pad Voltage	Pad Type	Description
285	MI251_DATA0	GPIO_104	Y		1.8	B- PD:nppukp	Configurable I/O
				QDSS_GPIO_TRACE DATA_LOCB[1]		DO	QDSS trace data bit 1B
				LPI_GPIO12:LPI D MIC3_CLK		DO	LPI_Digital MIC 3 Clock
				LPI_GPIO_12:LPI_ MI2S1_DATA0		B	LPI_MI2S 1 Data 0
				PWM[8]		DO	PWM output 8
98, 145, 147, 286, 287, 288, 289 290, 291, 292 293, 294, 295	GND						Ground
3, 4, 5, 6, 7, 8, 15, 16, 17, 22, 23, 24, 25, 32, 33, 34, 48, 49, 69, 70, 71, 75, 84, 89, 91, 92, 105, 107, 109, 110 111, 115, 121, 122, 126, 127 136, 137, 138 152, 158, 164 169, 171, 172, 176, 178, 192, 201, 203, 204 208, 212, 214 215, 230, 231, 239, 240, 241, 242, 245, 246, 249, 256, 257 258, 260, 265, 269, 275, 276	NC						No connection

NOTE:

- For CM2290,Pin#75,110 and 111 are NC.
- For C2290,Pin#75,110 and 111 are not NC.Pin#75 is CLK_GPS,Pin#110 is IO_GNSS_BB_IP and Pin#111 is IO_GNSS_BB_QP.
- MV pad voltage will be either at 1.8V or VPH_PWR range based on the VINx selected.
- Ensure that there are no external pull-ups on the GPIOs (GPIO_43,GPIO_44,GPIO_45,GPIO_46, GPIO_48,GPIO_50,GPIO_51,GPIO_53,GPIO_57,GPIO_59,GPIO_6 1) if secure boot is not required.The external pull-ups can force the device to enter secure boot or to select a different boot device.

Table 2-3.RF interfaces for CM2290 only

Pad Number	Pin Number	Voltage	IO	Description	Wake-up (yes/no)	GPIO#
2	ANT_DRX		RF_IO	Diversity Antenna		
5	VREG_L20A_2P85		P0	L20A LDO regulated output		
6	VREG_L15A_1P8		P0	L15A LDO regulated output		
8	RFEE3_DATA	1.8	B-PD:nppukp	Configurable I/O		
			B	RF front-end 3 interface data		
			DI	Boot configuration control bit 5		
9	RFEE3_CLK	1.8	B-PD:nppukp	Configurable I/O		
			D0	RF front-end 3 interface clock		
13	ANT_GPS_L1_IN		RF_IN	GPS_ANTENNA		
48	ANT_PRI			Primary_Antenna		
1, 3, 12, 14, 47, 4 9, 54, 56, 57, 58, 59	GND					
4, 7, 10, 11, 15, 1 6, 17, 18, 19, 20, 21, 22, 23, 24, 25 , 26, 27, 28, 29, 3 0, 31, 32, 33, 34, 35, 36, 37, 38, 39 , 40, 41, 42, 43, 4 4, 45, 46, 50, 51, 52, 53	NC					

2.2.1.Power supply interface

Refer to Table 2-3 for all SOM Power Supply interface descriptions. For the detailed parameter, please refer to Chapter 3. Electrical Characteristics.

Table 2-4. Pin definition of power supply interface

Pin Name	Pin#	Type	Description
VCOIN	218	A1, A0	Coin-cell charge and supply
VIB_DRV_LDO_P	207	P0	Power supply for Haptics driver
USB_VBUS	205, 206	PI, P0	Input power from the source (USB), or output during USB-OTG
VPH_PWR	182, 183, 184	PI, P0	Primary system supply node, SCHG regulated node
VBATT	195, 196, 197, 202	PI, P0	Battery voltage node, connects to BATFET. Output is for charging, and input is for all other operations
VREG_L4A_2P96	263	P0	2.96 V, only used for SD gpio pull up.
VREG_L10A_1P3	112	P0	Floating, reserved for debug.
VREG_L13A_1P8	187	P0	Floating, reserved for debug.
VREG_L14A_1P8	106	P0	Floating, reserved for debug.
VREG_L15A_1P8	156, 170 RF:6*	P0	Power for SOM system 1.8, only used for GPIOs pull up
VREG_L16A_1P8	113	P0	Floating, reserved for debug.
VREG_L17A_3P0	157	P0	Power for sensor 3.0.
VREG_L18A_1P8	264	P0	Power for QCM2290/UIM1/NFC, only used for UIM1/NFC
VREG_L19A_1P8	86	P0	Power for QCM2290/UIM2/NFC, only used for UIM2/NFC
VREG_L21A_2P96	251	P0	Power for SD 2.96, only used for SD power
VREG_USB_3P1	186	P0	Power for the QCM2290 USB HS 3.1, unavailable on devices of customer
VREG_L20A_2P85	RF:5*	P0	Floating, reserved for debug.
FLASH_LED1	180	A0	Anode connection of flash LED 1. Connect cathode to nearest ground

NOTE:*indicates these pins are available only on CM2290.

2.2.2. Control signals

Table 2-5. Pin definition of control signals

PAD Name	Pad	Voltage	Type	Description	Notes
KYPD_PWR_N	193	1.8	DI	Input pad generally connected to a keypad power-on button and when grounded, initiates the power-on sequence. Can also be configured for generating a stage 2 and/or stage 3 reset if held at a logic low for longer durations. Pulled up internally.	Active low level
CBL_PWR_N	216	1.8	DI	Alternate input pad, which can be used to initiate the power-on sequence when grounded; pulled up internally.	Active low level
KYPD_VOL_DOWN_N	155	1.8	DI	Input pad used for generating a stage 2 and/or stage 3 reset when held at a logic low.	
WDOG_DISABLE	72	1.8	DI	Gates the watchdog expired signal.	
SM_GPIO_89	120	1.8	DI	1.8V push-pull tri-state output indicating CC1 or CC2 connection (orientation).	QCM2290 GPIO89 PM4125(CC_OUT)
BATT_ID	181		AI	Battery ID input to the ADC.	
PM_OPTION	185		AI	Option hardware configuration control.	
BATT_THERM	198		AI	Battery temperature input to ADC for measuring the pack temperature	
KEY_VOLP	200	1.8	DI	Volume +Key	
FORCED_USB_BOOT_POL_SEL	244	1.8	DI	Forced USB boot polarity select, default SEL=L, FORCE_USB_BOOT=H	
FORCED_USB_BOOT	268	1.8	DI	Forced a USB boot	
CAM_MUX_EN	270	1.8	DO	Cameral mux enable	Assign IO function
CAM_MUX_SEL	283	1.8	DO	Cameral mux select	Assign IO function
ACCL_INT1	133	1.8	DI	Accelerometer INT	Assign IO function
GYRO_INT	179	1.8	DI	Gyros INT	Assign IO function
NFC_EN	67	1.8	DO	NFCenable	Assign IO function

BATT_ID is used for the different battery pack identification, which support ranges from 7.5k to 450kohm.

BATT_THERM reports the temperature of the battery pack to system. In general, it is recommended to use NTC 100K 1%B=4350 in the battery pack and 100Kohm resistance instead for the non-battery use case.

2.2.3. USB interface

The SOM supports 1xUSB 3.1 connector (no DisplayPort function supported).

Table 2-6. Pad description of USB interface

PAD Name	Pad	Typ.	Description	Notes
USB_CC1	163	AI	OTG mode enable or CC1 pin for the USB Type-C connector (user programmable)	PM4125
USB_CC2	149	AI	CC2 pin for the USB Type-C connector	PM4125
USB0_HS_DP	210	AI, AO	USB high-speed data-plus	QCM2290
USB0_HS_DM	209	AI, AO	USB high-speed data-minus	QCM2290
USB0_SS_RX0_P	277	AI	USB super-speed receive 0-plus	QCM2290
USB0_SS_RX0_M	278	AI	USB super-speed receive 0-minus	QCM2290
USB0_SS_TX0_P	279	AI, AO	USB super-speed transmit 0-plus	QCM2290
USB0_SS_TX0_M	280	AI, AO	USB super-speed transmit 0-minus	QCM2290
USB0_SS_RX1_P	225	AI	USB super-speed receive 1-plus	QCM2290
USB0_SS_RX1_M	226	AI	USB super-speed receive 1-minus	QCM2290
USB0_SS_TX1_M	227	AI, AO	USB super-speed transmit 1-minus	QCM2290
USB0_SS_TX1_P	228	AI, AO	USB super-speed transmit 1-plus	QCM2290

2.2.4.Camera interface

The SOM supports 2x4-lane CSIs D-PHY,1.2 at 2.5Gbps per lane.

Table 2-7.Pad description of camera interface

PAD Name	Pad	Typ.	Description	Notes
CSIO_A0_CLK_M	44	AI, AO	CSI 0,differential clock-minus	MIPI CSI
CSIO_NC_CLK_P	45		CSI 0,differential clock-plus	
CSIO_B0_LN0_P	42		CSI 0,differential lane 0-plus	
CSIO_CO_LN0_M	43		CSI 0,differential lane 0-minus	
CSIO_B1_LN1_M	13		CSI 0,differential lane 1-minus	
CSIO_A1_LN1_P	14		CSI 0,differential lane 0-plus	
CSIO_C1_LN2_P	11		CSI 0,differential lane 1-plus	
CSIO_A2_LN2_M	12		CSI 0,differential lane 2-minus	
CSIO_C2_LN3_M	30		CSI 0,differential lane 3-minus	
CSIO_B2_LN3_P	31		CSI 0,differential lane 3-plus	
CSI1_NC_CLK_P	40		CSI1,differential clock-plus	
CSI1_A0_CLK_M	41		CSI 1,differential clock-minus	
CSI1_CO_LN0_M	38		CSI 1,differential lane 0-minus	
CSI1_B0_LN0_P	39		CSI 1,differential lane 0-plus	
CSI1_B1_LN1_M	9		CSI 1,differential lane 1-minus	
CSI1_A1_LN1_P	10		CSI 1,differential lane 1-plus	
CSI1_A2_LN2_M	26		CSI 1,differential lane 2-minus	
CSI1_C1_LN2_P	27		CSI 1,differential lane 2-plus	
CSI1_B2_LN3_P	28		CSI 1,differential lane 3-plus	
CSI1_C2_LN3_M	29		CSI 1,differential lane 3-minus	
CAM_MCLK0	64	D0	Camera master clock 0	
CAM_MCLK1	37		Camera master clock 1	
CAM_MCLK2	81		Camera master clock 2	
CCI_12C_SCL0	35	B-PD:nppukp B	Dedicated camera control interface I2C0 serial clock	
CCI_12C_SDA0	36		Dedicated camera control interface I2C0 serial data	
CCI_12C_SCL1	52		Dedicated camera control interface I2C1 serial clock	
CCI_12C_SDA1	58		Dedicated camera control interface I2C1 serial data	

CCI I2C needsto be pulled up to 1.8V (VREG_L15A_1P8)with external 2.2K.2x CSI interfaces can set up multiple combination dependent with the use case.Furthermore,the 4 lanes of CSI interface can be configured as 2-lane plus 1-lan interfaces or 1-lan plus 1-lane interface.

DCLK →DCLK_A
DLN0 →DLN0_A
DLN1 → DLN1_A
DLN2→DLN0_B
DLN3→DCLK_B

DCLK→DCLK_A
DLNO →DLNO_A
DLN2 → DLN0_B
DLN3→DCLK_B

2.2.5.Display interface

The SOM supports 1x4-lane DSI D-PHY 1.2 at 1.5Gbps per lane.

Table 2-8.Display interface pad description

PAD Name	Pad	Typ.	Description	Notes
MIPI_DSI0_CLK_P	78	A0	DSIO differential clock-plus	MIPI DSI
MIPI_DSI0_CLK_M	95		DSIO differential clock-minus	
MIPI_DSI0_L0_P	96		DSIO differential lane 0-plus	
MIPI_DSI0_L0_M	79		DSIO differential lane 0-minus	
MIPI_DSI0_L1_P	93		DSIO differential lane 1-plus	
MIPI_DSI0_L1_M	76		DSIO differential lane 1-minus	
MIPI_DSI0_L2_P	94		DSIO differential lane 2-plus	
MIPI_DSI0_L2_M	77		DSIO differential lane 2-minus	
MIPI_DSI0_L3_P	80		DSIO differential lane 3-plus	
MIPI_DSI0_L3_M	97		DSIO differential lane 3-minus	
MIPI_DSI1_CLK_P	46		DSI1 differential clock-plus	
MIPI_DSI1_CLK_M	47		DSI1 differential clock-minus	

2.2.6.GPIO

These GPIOs of C2290/CM2290 are available as QUP(Qualcomm universal peripheral)interface ports that can be configured for UART or/and SPI or/and I2C or/and I3C operation(Note:Only one protocol can be selected in one QUP engine at a time).

There are 9xQUP engines (SE in the following chart)

I2C is a two-wire bus that can be routed to multiple devices;each line of each bus needs to be supplemented by a 2.2kQ pull-up resistor.

Table 2-9.GPIO QUP configuration

	GPIO	Serial Engine	Lane	Multiplexed Interface			
QUPO	GPIO_0	SE0	0	SPI_MISO	UART_CTS_N	I2C_SDA	I2C_SDA
	GPIO_1			SPI_MOSI	UART_RFR_N	I2C_SCL	I3C_SCL
	GPIO_2		2	SPI_SCLK	UART_TX_N		
	GPIO_3		3	SPI_CS_0_N	UART_RX_N		
	GPIO_82		4	SPI_CS_1_N			
	GPIO_86		5	SPI_CS_2_N			
	GPIO_4	SE1	0	SPI_MISO	UART_CTS_N	I2C_SDA	
	GPIO_5			SPI_MOSI	UART_RFR_N	I2C_SCL	
	GPIO_69		2	SPI_SCLK	UART_TX_N		
	GPIO_70		3	SPI_CS_0_N	UART_RX_N		
	GPIO_6	SE2	0	SPI_MISO	UART_CTS_N	I2C_SDA	
	GPIO_7			SPI_MOSI	UART_RFR_N	I2C_SCL	
	GPIO_71		2	SPI_SCLK	UART_TX_N		
	GPIO_80		3	SPI_CS_0_N	UART_RX_N		
	GPIO_96	SE4	0	SPI_MISO	UART_CTS_N	I2C_SDA	

	GPIO	Serial Engine	Lane	Multiplexed Interface			
	GPIO_97		1	SPI_MOSI	UART_RFR_N	2C_SCL	
	GPIO_12		2	SPI_SCLK	UART_TX_N		
	GPIO_13		3	SPI_CS_0_N	UART_RX_N		
	GPIO_14	SE5	0	SPI_MISO	UART_CTS_N	2C_SDA	
	GPIO_15		1	SPI_MOSI	UART_RFR_N	2C_SCL	
	GPIO_16		2	SPI_SCLK	UART_TX_N		
	GPIO_17		3	SPI_CS_0_N	UART_RX_N		
QUP (LPI)	LPI_GPIO_19	SE0	0			2C_SDA	12C3_SDA2 GPIO_109
	LPI_GPIO_20		1			2C_SCL	12C3_SCL GPIO_110
	LPI_GPIO_21	SE1	0	SPI_MISO	UART_CTS_N	2C_SDA	12C3_SDA
	LPI_GPIO_22		1	SPI_MOSI	UART_RFR_N	2C_SCL	12C3_SCL
	LPI_GPIO_25		2	SPI_SCLK	UART_TX_N		
	LPI_GPIO_26		3	SPI_CS_0_N	UART_RX_N		
	LPI_GPIO_23	SE5	0		UART_TX_N	2C_SDA	GPIO_111
	LPI_GPIO_24		1		UART_RX_N	2C_SCL	GPIO_112
	LPI_GPIO_25	SE6	0		UART_TX_N		
	LPI_GPIO_26		1		UART_RX_N		

—NOTE:

- GPIO_109,GPIO_110,GPIO_111,GPIO_112 are only used for LPI_GPIO function.
- GPIO_109 and GPIO_110 are only used for 12C for sensors.
- LPI_GPIO21 and LPI_GPIO_22 are only used for I3C for sensors.
- GPIO_111,GPIO_112,LPI_GPIO_25,LP_GPIO_26 are reserved pins.

Table 2-10. Pad description of GPIO interface

PAD Name	PAD	Voltage	Wake-up	Description
NFC_SPI_MISO	59	1.8V	Y	Configurable I/O QUP 0 SE0, lane 0: SPI_MISO QUP 0 SE0, lane 0: UART_CTS QUP 0 SE0, lane 0: 12C_SDA QUP 0 SE0, lane 0: 13C_SDA QDSS trace data bit 8B
NFC_SPI_MOSI	57			Configurable I/O QUP 0 SE0, lane 1: SPI_MOSI QUP 0 SE0, lane 1: UART_RFR QUP 0 SE0, lane 1: 12C_SCL QUP 0 SE0, lane 1: 13C_SCL QDSS trace data bit 9B
NFC_SPI_SCLK	60			Configurable I/O QUP 0 SE0, lane 2: SPI_SCLK QUP 0 SE0, lane 2: UART_TX QDSS trace data bit 10 B
NFC_SPI_CS_N	62		Y	Configurable I/O QUP 0 SE0, lane 3: SPI_CS_N QUP 0 SE0, lane 3: UART_RX QDSS trace data bit 11B
SM_GPIO_82	99			Configurable I/O QUP 0 SE0, lane 4: SPI_CS_N_1 PWM output 6
NFC_CLK_REQ	213		Y	Configurable I/O QUP 0 SE0, lane 5: SPI_CS_N_2 Global general-purpose clock 1B
APPS_12C_SDA	82		Y	Configurable I/O QUP 0 SE1, lane 0: SPI_MISO QUP 0 SE1, lane 0: UART_CTS QUP 0 SE1, lane 0: 12C_SDA
APPS_12C_SCL	83			Configurable I/O QUP 0 SE1, lane 1: SPI_MOSI QUP 0 SE1, lane 1: UART_RFR QUP 0 SE1, lane 1: 12C_SCL
NFC_EN	67		Y	Configurable I/O QUP 0 SE1, lane 2: SPI_SCLK QUP 0 SE1, lane 2: UART_TX Global general-purpose clock 2 A QDSS trace data bit 12 B
NFC_INT_N	54		Y	Configurable I/O QUP 0 SE1, lane 3: SPI_CS_N QUP 0 SE1, lane 3: UART_RX Global general-purpose clock 3A QDSS trace data bit 13 B
Touch_12C_SDA	100		Y	Configurable I/O QUP 0 SE2, lane 0: SPI_MISO QUP 0 SE2, lane 0: UART_CTS QUP 0 SE2, lane 0: 12C_SDA
Touch_12C_SCL	119			Configurable I/O QUP 0 SE2, lane 1: SPI_MOSI QUP 0 SE2, lane 1: UART_RFR QUP 0 SE2, lane 1: 12C_SCL
SM_GPIO_71	56			Configurable I/O QUP 0 SE2, lane 2: SPI_SCLK QUP 0 SE2, lane 2: UART_TX
SM_GPIO_80	166		Y	Configurable I/O QUP 0 SE2, lane 3: SPI_CS_N QUP 0 SE2, lane 3: UART_RX
KEY_VOLP	200		Y	Configurable I/O QUP 0 SE4, lane 0: SPI_MISO QUP 0 SE4, lane 0: UART_CTS QUP 0 SE4, lane 0: 12C_SDA Generic IO for GNSS MDP vertical sync-external General-purpose PDM_Mirror_A1 SD card write protect QDSS trigger input 0A QDSS trigger output 1A

PAD Name	PAD	Voltage	Wake-up	Description
SM_GPIO_97	73	1.8V	Y	Configurable I/O QUP 0 SE4, lane 1:SPI_MOSI QUP 0 SE4, lane 1:UART_RFR QUP 0 SE4, lane1:12C_SCL Generic IO for GNSS MDP vertical sync-secondary General-purpose PDM_Mirror_A2 QDSS trigger output 0 A QDSS trigger input 1A
DBG_UART_TX	104			Configurable I/O QUP 0 SE4, lane 2:UART_TX QUP 0 SE4, lane 2:SPI_SCLK
DBG_UART_RX	88		Y	Configurable I/O QUP 0 SE4, lane 3:UART_RX QUP 0 SE4, lane 3:SPI_CS_N
SPI_MISO	255		Y	Configurable I/O QUP 0 SE5, lane 0:SPI_MISO QUP 0 SE5, lane 0:UART_CTS QUP 0 SE5, lane 0:12C_SDA QDSS trace data bit 4B
SPI_MOSI	267			Configurable I/O QUP 0 SE5, lane 1:SPI_MOSI QUP 0 SE5, lane 1:UART_RFR QUP 0 SE5, lane1:12C_SCL QDSS trace data bit 5 B
SPI_SCLK	254			Configurable I/O QUP 0 SE5, lane 2:UART_TX QUP 0 SE5, lane 2:SPI_SCLK QDSS trace data bit 6 B
SPI_CS_N	266		Y	Configurable I/O QUP 0 SE5, lane 3:UART_RX QUP 0 SE5, lane 3:SPI_CS_N QDSS trace data bit 7 B
I3C_SDA	61		Y	Configurable I/O LPI_QUP 0 SE1, lane 0:SPI_MISO LPI_QUP 0 SE1, lane 0:UART_CTS LPI_QUP 0 SE1, lane 0:12C_SDA LPI_QUP 0 SE1, lane 0:I3C_SDA
I3C_SCL	55			Configurable I/O LPI_QUP 0 SE1, lane 1:SPI_MOSI LPI_QUP 0 SE1, lane 1:UART_RFR LPI_QUP 0 SE1, lane 1:12C_SCL LPI_QUP 0 SE1, lane 1:I3C_SDA
LPI_GPIO_25	117			Configurable I/O LPI_QUP 0 SE1, lane 2:SPI_SCLK LPI_QUP 0 SE1, lane 2:UART_TX LPI_QUP 0 SE6, lane 2:UART_TX
LPI_GPIO_26	116		Y	Configurable I/O LPI_QUP 0 SE1, lane 3:SPI_CS_N LPI_QUP 0 SE1, lane 3:UART_RX LPI_QUP 0 SE6, lane 3:UART_RX

2.2.7.PMIC GPIO

The supported GPIO interfaces of PM4125 are listed as follows. The GPIO features can be customized on PM4125 device (special connections that can exist only in specific GPIO locations).

Table 2-11.PMIC GPIO interface padparameters

PAD Name	PAD	Voltage	Type	SpecialFunction	Notes
PM_GPIO_01	101	1.8V/VPH_PWR	AI, AO	reserve	PM4125 Configurable; default digital input with 10 μ A pull-down
BL_PWM_OUT	154	1.8V/VPH_PWR		PWM_OUT for backlight	
PM_GPIO_03	150	1.8V/VPH_PWR		reserve	
PM_GPIO_04	151	1.8V/VPH_PWR		reserve	
CHG_SKIN_THERM	189	1.8V		Thermal detection with thermistor	
USB_CONN_THERM	199	1.8V		Thermal detection with thermistor	
PM_GPIO_07	188	1.8V			
PM_GPIO_08	165	1.8V		reserve	
PM_GPIO_09	168	1.8V		reserve	

It is recommended to select 100K 1%B=4250 thermistor for temperature monitoring. Unused pins can be floated if no special feature is implemented.

2.2.8.SD card I/O interface

The SOM supports one 4-lane SDIO (Secure Input and Output Interface).

Table 2-12.Pad description of SDIO

PAD Name	PAD	Voltage	Type	Description	Notes
SDC2_CMD	2	1.8/2.97	BH-PD:nppukp	Secure digital controller 2 command	
SDC2_CLK	21		BH-PD:nppukp	Secure digital controller 2 clock	
SDC2_DATA_0	20		BH-PD:nppukp	Secure digital controller 2 databit 0	
SDC2_DATA_1	1		BH-PD:nppukp	Secure digital controller 2 data bit 1	
SDC2_DATA_2	19		BH-PD:nppukp	Secure digital controller 2 data bit 2	
SDC2_DATA_3	18		BH-NP:dpukp	Secure digital controller 2 data bit 3	
SD_DET_IN	233	1.8V	B-PD:nppukp	Configurable I/O	GPIO_88

The SD_CARD_DET_N is used for SD card detection.

2.2.9.UIM (User Identifier Module)

The SOM supports 2x dual voltage UIM.

Table 2-13. Pad description of UIM

PAD Name	PAD	Voltage	Type	Description
UIM1_DATA	129			Configurable I/O UIM1 data (dual voltage)
UIM1_CLK	130			Configurable I/O UIM1 clock (dual voltage)
UIM1_RESET	140	1.8 Vor 2.95V		Configurable I/O UIM1 reset (dual voltage)
UIM1_PRESENT	141		B-PD:nppukp	Configurable I/O UIM1 presence detection
UIM2_DATA	131		D0	Configurable I/O UIM2 data (dual voltage) QDSS trigger input 1B PWM output 3
UIM2_CLK	132	1.8 Vor 2.95V		Configurable I/O UIM2 clock (dual voltage) QDSS trigger output 1B
UIM2_RESET	194			Configurable I/O UIM2 reset (dual voltage) PWM output 4
UIM2_PRESENT	142		B-PD:nppukp D0	Configurable I/O UIM2 presence detection PWM output 5

The UIM1_PRESENT and UIM2_PRESENT are high level respectively with SIM1 and SIM2 cards inserted.

2.2.10.12S interface

Table 2-14. Pad description of 12S interface

PAD Name	PAD	Voltage	GPIO#	Description
MI2S1_MCLK	143	1.8V	GPIO_108	Configurable I/O Generic IO for GNSS MI2S Master Clock 1_A
MI2S1_CLK	274		GPIO_102	Configurable I/O LPI_MI2S 1 Clock LPI_Digital MIC 4 Clock
MI2S1_WS	262		GPIO_103	Configurable I/O LPI_MI2S 1 Word Select LPI_Digital MIC4 Data
MI2S1_DATA0	285		GPIO_104	Configurable I/O QDSS trace data bit 1 B LPI_Digital MIC3 Clock LPI_MI2S 1 Data 0 PWM output 8
MI2S1_DATA1	284		GPIO_105	Configurable I/O QDSS trace clockB LPI_Digital MIC3 Data LPI_MI2S 1 Data 1 MI2S Master Clock 0A

2.2.11.RF (Radio Frequency)**Table 2-15.Pad description of RF interface**

PAD Name	PAD	Voltage	Type	Description	Notes
ANT_FM_RX	87		A1	FM headset antenna. If not used, connect to ground	WCN3950
ANT_2G_5G_WLAN	146		A1/A0	5G WLAN RF Tx/Rx 2G WLAN/BT Tx/Rx	WCN3950
IO_GNSS_BB_IP	110		A1	GNSS receiver baseband input, in-phase plus	
IO_GNSS_BB_QP	111		A1	GNSS receiver baseband input, quadrature plus	
RFFE3_DATA	RF:8		D0	RF front-end 3 interface data	
RFFE3_CLK	RF:9		D0	RF front-end 3 interface clock	
ANT_DRX	RF:2			Antenna DRX	CM2290 RF only
ANT_GPS_L1_IN	RF:13		RF_IN	GPS_ANTENNA	CM2290 RF only
ANT_PRI	RF:48			Primary_Antenna	CM2290 RF only

Chapter 3. Electrical Characteristics

3.1. Absolute maximum ratings

The absolute maximum ratings (Table 3-1) reflect the stress levels that, if exceeded, may cause permanent damage to the device. No functionality is guaranteed outside the operating specifications. Functionality and reliability are only guaranteed within the operating conditions described in 3.2. Operating conditions.

Table 3-1. Absolute rating conditions

Parameter	Min	Max	Units
Input Power Voltage			
USB_VBUS	-0.3	16	V
VBAT	2.7	4.75	V
VPH_PWR	-0.3	5.25	V
VBATT_SNS_P	2.7	5.25	V
ESD			
ESD-HBM model rating		±2000	V
ESD-CDM model rating		±500	V

NOTE: The ESD (Electro-Static Discharge) parameters can only be valid and available when the module is fully tested and approved in the Initial Production stage.

3.2. Operating conditions

The SOM needs to be designed in the operation conditions shown as below

Table 3-2. Operating conditions

Parameters	Min	Typical	Max	Units
Input power voltage				
USB_VBUS	3.6		6	V
VBAT	3.4	3.9	4.35	V
VPH_PWR	3.4	3.9	4.35	V
VBATT_SNS_P	3.4	3.9	4.6	V
VCOIN	2.5		3.2	V
Thermal conditions				
Operating temperature	-25	25	75	°C
Storage temperature	-40		70	°C

NOTE: The min and max operating temperatures specified in the above table shall not exceed those of relevant IC (see Table 3-3).

Table 3-3.ICtemperature

Chipset	Thermal Condition (min, °C)	Thermal Condition (max, °C)
QCM2290	Ta=-30	Tj=95
PM4125	Tj=-30	Tj=125
LPDDR	Ta=-25	Ta=85
EMMC	Ta=-25	Ta=85

—NOTE:

·Ta:a=ambient,temperature of the working environment.

·Tj:j=junction,junction temperature,which can be simply understood as the chip internal temperature.

3.3.Power input/output

The SOM provide power supply for external devices,like camera modules,SD card,Sensors,and so on.
Below map shows the details.

Table 3-4.Input power padparameters

Pad Name	Voltage(V)	Range (V)	Rated current (mA)	Expected use
USB VBUS	5	4~6	TBD	
VBAT	4.2	3.4~4.35	TBD	
VPH PWR	4.2	3.4~4.35	TBD	

Table 3-5.Output power pad parameters

Pad Name	Voltage (V)	Range (V)	Rated current (mA)	Expected use
VREG_L13A_1P8	1.8	1.77~1.83	260	Floating,reserved for debug
VREG_L15A_1P8	1.8	1.7~1.9	630	Used for GPIO PU
VREG_L16A_1P8	1.8	1.77~1.83	200	Floating,reserved for debug
VREG_L17A_3P0	3.0	2.97~3.03	190	Sensor power
VREG_L18A_1P8	1.8	1.78~2.95	67	UIM1/NFC
VREG_L19A_1P8	1.8	1.78~2.95	67	UIM2/NFC
VREG_L21A_2P96	2.96	2.85~3.07	840	SD card
FLASH_LED1			1000	Flash led

3.4.Digital-logic characteristics

The digital I/O's performance depends on its pad type,usage,and power supply voltage.The SOM IO voltage level is the same with **VDDPX_3** except those for the SD card and analog input/output.The design of I2C, USB,MIPI,and UART interfaces complies with the corresponding standards.

3.4.1.Digital GPIO characteristics

Table 3-6.Digital GPIO characteristics

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, CMOS/Schmitt	0.65 xVDDPX	VDDPX+0.3	V
VIL	Low-level input voltage, CMOS/Schmitt	-0.3	0.35 xVDDPX	V
VOH	High-level output voltage, CMOS	VDDPX-0.45	VDDPX	V
VOL	Low-level output voltage, CMOS	0.0	0.45	V

3.4.2.SD card/UIM digital I/O characteristics

The SD card is powered by P2(1.8V or 2.96V).

Table 3-7.SD card 2.95V digital I/O interface characteristics

Parameter	Description	Min	Typical	Max	Units
VIH	High-level input voltage	0.625xVDDPX		VDDPX+0.3	V
VIL	Low-level input voltage	-0.3		0.25x VDDPX	V
RPULL-UP	Pull-up resistance	10K		100K	Ω
RPULL-DOWN	Pull-down resistance	10K		100K	Ω
VOH	High-level output voltage	0.75xVDDPX		VDDPX	V
VOL	Low-level output voltage	0		0.125x VDDPX	V

Table 3-8.SD card 1.8V digital I/O interface characteristics

Parameter	Description	Min	Typical	Max	Units
VIH	High-level input voltage	1.27		2	V
VIL	Low-level input voltage	-0.3		0.58	V
RPULL-UP	Pull-up resistance	10K		100K	Ω
RPULL-DOWN	Pull-down resistance	10 K		100K	Ω
VOH	High-level output voltage	1.4			V
VOL	Low-level output voltage			0.45	V

Table 3-9.UIM 2.95V digital I/O interface characteristics

Parameter	Description	Min	Typical	Max	Units
V _{IH}	High-level input voltage	0.7xVDDPX		VDDPX+0.3	V
V _{IL}	Low-level input voltage	-0.3		0.2xVDDPX	V
RPULL-UP	Pull-up resistance	10 K		100K	Q
RPULL-DOWN	Pull-down resistance	10 K		100K	Q
V _{OH}	High-level output voltage	0.8xVDDPX		VDDPX	V
V _{OL}	Low-level output voltage	0		0.45	V

Table 3-10. UIM 1.8V digital I/O interface characteristics

Parameter	Description	Min	Typical	Max	Units
V _{IH}	High-level input voltage	0.7xVDDPX		VDDPX+0.3	V
V _{IL}	Low-level input voltage	-0.3		0.2xVDDPX	V
RPULL-UP	Pull-up resistance	10K		100K	Q
RPULL-DOWN	Pull-down resistance	10K		100K	Q
V _{OH}	High-level output voltage	0.8xVDDPX		VDDPX	V
V _{OL}	Low-level output voltage	0		0.45	V

3.5.MIPI(Mobile Industry Processor Interface)

The supported MIPI interface complies with MIPI standards.

Table 3-11.Supported MIPI_CSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for DPHYv1.2	Supports only unidirectional data receiving
MIPI Alliance Specification for CPHYv1.0	None

Table 3-12.Supported MIPI_DSI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for D-PHYv1.2	None

3.6.USB interface

Table 3-13.USB standards and exceptions

Applicable standard	Feature exceptions	Device variations
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	Feature exceptions SS Gen2.	None
Universal Serial Bus Specification, Revision 2.0 (April 27, 2000 or later)	Low speed is not supported in device mode	Operating voltages, system clock, and VBUS
On-The-Go Supplement to the USB 2.0 Specification (June 24, 2003, Revision 1.0 A or later)	Supports the host mode aspect of OTG only	None

3.7.SD interface

Table 3-14.Supported SDIO standards and exceptions

Applicable standard	Feature exceptions
Multi-Media Card Host Specification, version 5.1	None
Secure Digital:Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

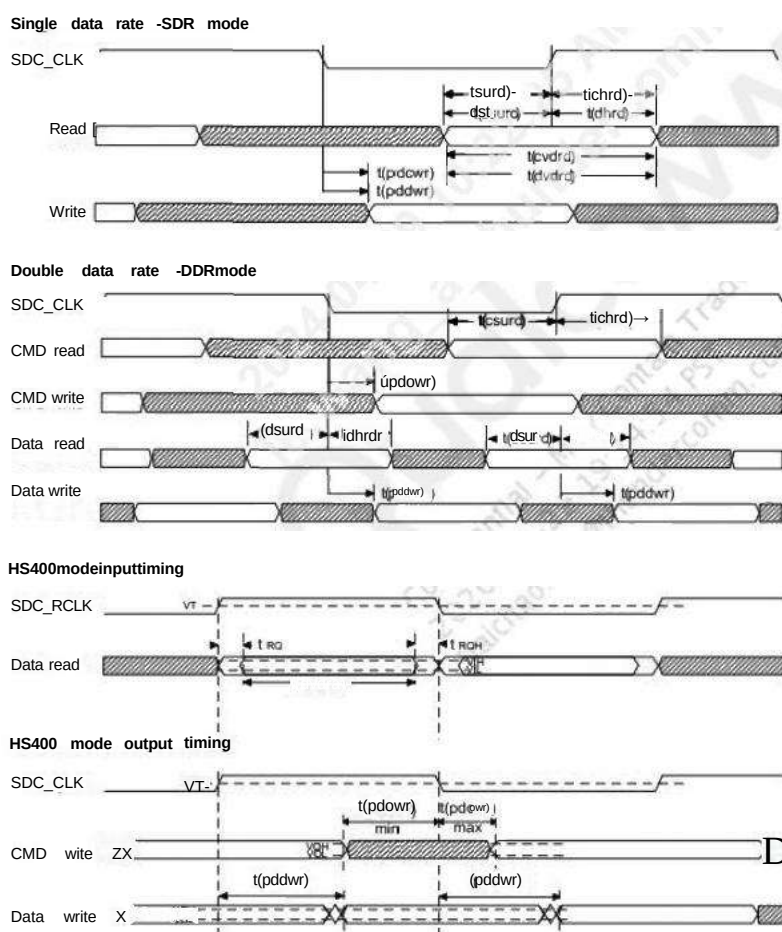


Figure 3-1.SD Interface Timing

3.8.12S

Table 3-15.Supported I2S standards and exceptions

Applicable standard	Feature exceptions	Device variations
Philips I2S Bus Specifications revised June 5, 1996	None	Timing. See below Figure. When an external SCK clock is used, a duty cycle between 45% to 55% is required.

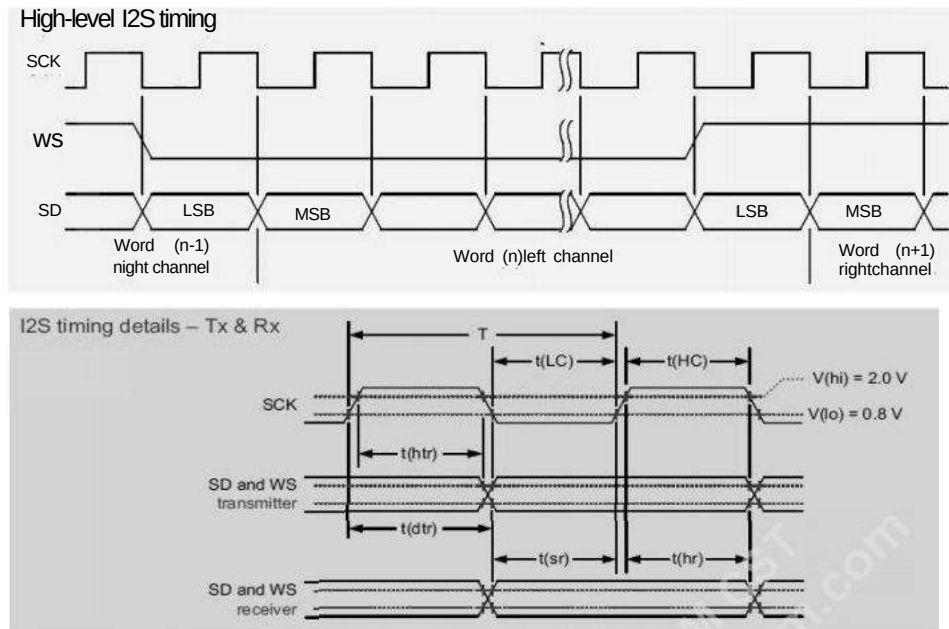


Figure 3-2.12S Timing Diagram

Table 3-16.12S timing characteristics

Parameter	Comm	Min	Typ.	Max	Unit
Using internal SCK					
Frequency				24.576	MHz
T	Clock period	-	40.69		ns
t(HC)	Clock high	-	$0.45 \times T$	$0.55 \times T$	ns
t(LC)	Clock low		$0.45 \times T$	$0.55 \times T$	ns
t(sr)	SD and WS input setup time		8.14		ns
t(hr)	SD and WS input hold time		0		ns
t(dtr)	SD and WS output delay			6.10	ns
t(htr)	SD and WS output hold time delay		0		ns
Using external SCK					
Frequency				24.576	MHz
T	Clock period		40.69		ns
t(HC)	Clock high		$0.45 \times T$	$0.55 \times T$	ns
t(LC)	Clock low		$0.45 \times T$	$0.55 \times T$	ns
t(sr)	SD and WS input setup time		8.14		ns
t(hr)	SD and WS input hold time		0		ns
t(dtr)	SD and WS output delay			6.10	ns

3.9.Digital microphone PDM interface

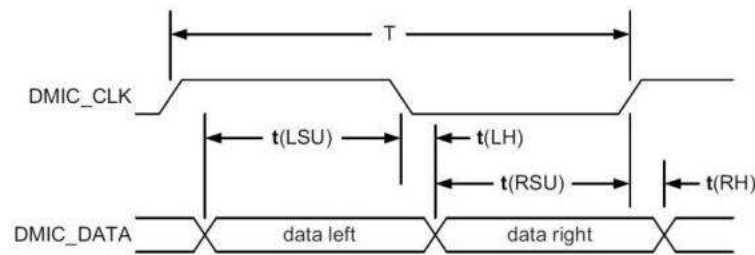


Figure 3-3.DMIC Timing Diagram

Table 3-17. DMIC parameters

Parameter	Comments	Min	Typ.	Max	Unit
T	DMIC clock period	163		1666	ns
t(LSU)	Data left setup time to clock	5			ns
t(LH)	Data left hold time to clock falling	0			ns
T(RSU)	Data right setup time to clock	5			ns
t(RH)	Data right hold time to clock	0			ns

3.10.12C

Table 3-18.SupportedI2C standards and exceptions

Applicable standard	Feature exceptions
12C Specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported

3.11.13C

Table 3-19.Supported 13C standards and exceptions

Applicable standard	Feature exceptions
13C Specification, version 1.0	

3.12.SPI

The QCM2290 supports SPI master mode only.Only six out of 9 QUP ports can be configured as a SPI master.

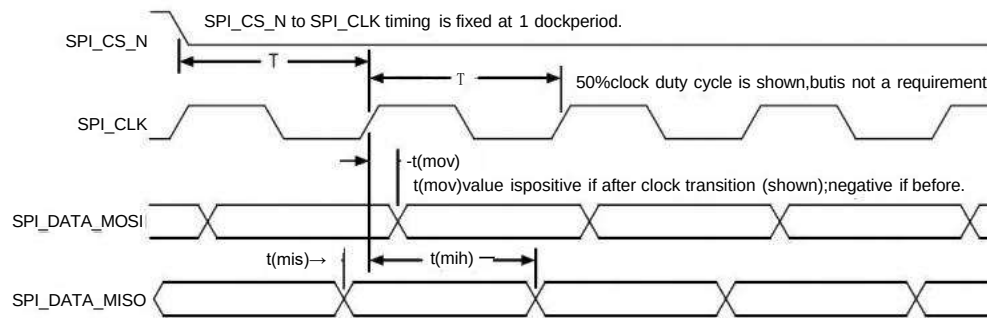


Figure 3-4.SPI Timing Diagram

Table 3-20.SPI parameters

Parameter	Comments	Min	Typ.	Max	Unit
T(SPI clock period)	50MHz max.	20		—	ns
t(ch)	Clock high	9			ns
t(cl)	Clock low	9			ns
t(mov)	Master output valid	-5	-	5	ns
t(mis)	Master input setup	5	-	—	ns

3.13.Fuel gauge

Qualcomm battery gauge is a hybrid of voltage and current based state of charge.The core of PM4125 Qualcomm battery gauge hardware consists of accumulator,which periodically samples,accumulates,and saves Vbatt and Ibatt values into PMIC register to read and process SoC.

The same hardware is reused for an online battery ESR estimation,where V and I readings are run and saved to record pre-ESR and ESR pulse Vbatt and Ibatt values.The software reads the registers for ESR estimation.

3.14.LED

The QCM2290 supports RGLD and Flash LED.

3.14.1.RG LED

Table 3-21.RG LED parameters

Parameter	Comments	Min	Typ.	Max	Unit
Isource	RG output per channel			9	mA
FPWM	PWM frequency		TBD		kHz

3.14.2.Flash LED

The supported high-current driver works in various concurrency scenarios and allows different LED configurations.

Table 3-22.Fash LED parameters

Parameter	Comments	Min	Type	Max	Unit
Maximum current per LED	LED1			1	A
Current resolution programmable	LED1	5	12.5	12.5	mA

3.15.PWM

SOM has one PWM output channel. **PM_GPIO_02** is for WLED brightness control.

3.16.Power consumption

Table 3-23.C2290 Power consumption

S/N	Test item and test condition	Power consumption (mA)
1	Leakage current in power-off status, average value	0.04
2	Sleep(Idle Mode), average value	3.3

Table 3-24.CM2290 Power consumption

S/N	Test item and test condition	Power consumption (mA)
1	Leakage current in power-off status, average value	0.05
2	Sleep(Idle Mode), average value	4.66

3.17.Thermal

Refer to the following tables for the thermal test data.A heat sink solution is strongly recommended to guarantee high performance of the SOM.

Table 3-25. Thermal test condition

	C2290	CM2290
HW Version	• Com10:V02 • Interposer:V06 • SOM:V02	• Com10:V02 - Interposer:V05 • SOM:V04 SKU5
SW Version	FlatBuild_Turbox- CM2290_c2290_32go_la1.0.1.L.userdebug.2 0220317.093443	FlatBuild_Turbox- CM2290_xx.xx_la1.0.1.D.userdebug.2021083 1.1244
Test Purpose	Test the chip temperature when C2290 is running at 25°C.	Test the chip temperature when CM2290 is running at 25°C
Test Procedure	1.Set the temperature test chamber to 25°C 2.Connect main IO board to 12V power supply and SOM to 4.2V power supply individually. 3.Set CPU load to maximum. 4.Open the camera and start to preview. 5.Set LCD brightness to maximum. NOTE: Test 1 hour(test point:read the temperature data from chip).	1.Set the temperature test chamber to 25°C. 2.Connect main IO board to 12V power supply and SOM to4.2V power supply individually. 3.Set LTE mode to:BI20M Max power 4.Set CPU load to maximum. 5.Open the cameraand start to preview. 6.Set LCD brightness to maximum. NOTE: Test 1 hour (test point:read the temperature data from chip)
DUT No.	TSN:MTS0411003PU	TSN:MTR38M1200CP

Table 3-26.Thermal test result

NOTE: Read from the data acquisition instrument

Test Location (Chip Model)	CM2290 Temperature (Max, °C)	C2290 Temperature(Max, °C)
Environment Temperature	24.5	23.08
CM2290	66.8	45.8
DDR	56.2	41.7
EMMC	65.2	40.2
PM4125	53	44.7
WCN3950	55.6	39.2
VC7643	63.7	NA
VC7916	51.1	NA

3.18.RF performance

Refer to the table below for the RF performance test results.

Table 3-27.RF Performance

RF performance					
Tx Characteristics					
Parameter	Comments	Min	Typ	Max	Unit
RF OUTPUT POWER	GSM		31±3		dBm
RF OUTPUT POWER	WCDMA	<-50	24+1/-3		dBm
RF OUTPUT POWER	LTE FDD BANDS	<-40	23±2		dBm
RF OUTPUT POWER	LTEBAND1	<-40		22.5	dBm
RF OUTPUT POWER	LTE TDD BANDS	<-40	23±2		dBm
Rx Characteristics					
Parameter	Comments	Min	Typ	Max	Unit
Receiving Sensitivity	GSM 850		-109.5		dBm
Receiving Sensitivity	GSM 900		-109.5		dBm
Receiving Sensitivity	GSM 1800		-109		dBm
Receiving Sensitivity	GSM 1900		-109		dBm
Receiving Sensitivity	WCDMA B1(SISO)		-110		dBm
Receiving Sensitivity	WCDMA B2(SISO)		-110		dBm
Receiving Sensitivity	WCDMA B5(SISO)		-108.5		dBm
Receiving Sensitivity	WCDMA B8(SISO)		-111		dBm
Receiving Sensitivity(10MHz)	LTE B1(SISO)		-98		dBm
Receiving Sensitivity(10MHz)	LTE B2 (SISO)		-98.7		dBm
Receiving Sensitivity(10MHz)	LTE B3 (SISO)		-98.1		dBm
Receiving Sensitivity(10MHz)	LTE B5 (SISO)		-98.1		dBm
Receiving Sensitivity(10MHz)	LTE B7 (SISO)		-97.1		dBm
Receiving Sensitivity(10MHz)	LTE B8 (SISO)		-98.7		dBm
Rx Characteristics					
Parameter	Comments	Min	Typ	Max	Unit
Receiving Sensitivity(10MHz)	LTE B20(SISO)		-98.7		dBm
Receiving Sensitivity(10MHz)	LTE B28A (SISO)		-97		dBm
Receiving Sensitivity(10MHz)	LTE B28B (SISO)		-97		dBm
Receiving Sensitivity(10MHz)	LTE B34 (SISO)		-98.5		dBm
Receiving Sensitivity(10MHz)	LTEB38(SISO)		-97.5		dBm
Receiving Sensitivity(10MHz)	LTE B39 (SISO)		-98.3		dBm
Receiving Sensitivity(10MHz)	LTEB40(SISO)		-97.9		dBm
Receiving Sensitivity(10MHz)	LTE B41(SISO)		-97.7		dBm

3.19.GPS performance

Table 3-28.GPS Performance

GPS RF Performance	
Conditions:VBAT=4.0V;signal source=-130dBm/Hz;temperature:25℃	
C/N0	40.50

Chapter 4.Packaging

4.1.Common packaging for C2290 SOM modules

C2290 SOM modules are packaged in carrier tapes. Refer to figure 4-1 for size of the carrier tape.

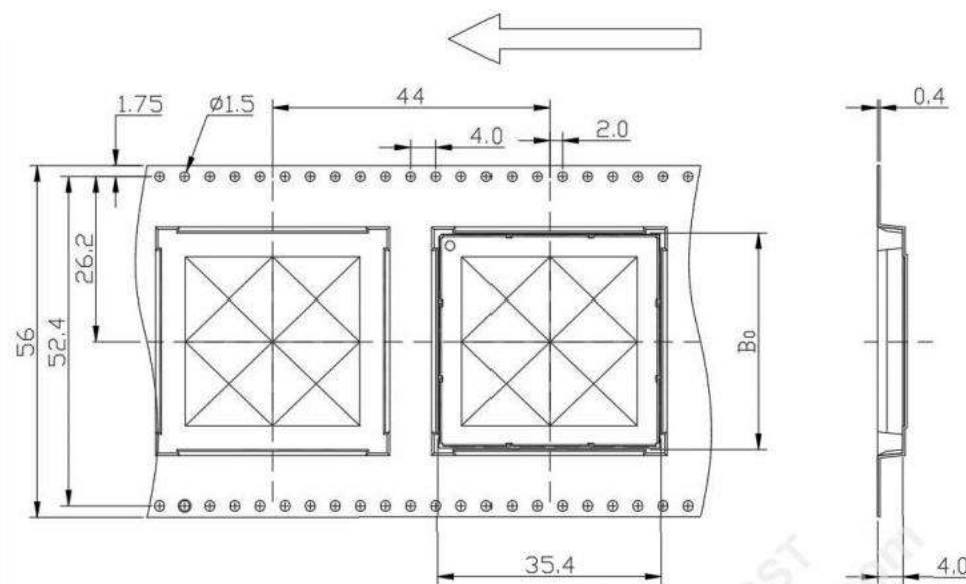


Figure 4-1.Carrier Tape Size (Unit:mm)

Refer to Figure 4-2 for the packaging Scheme:

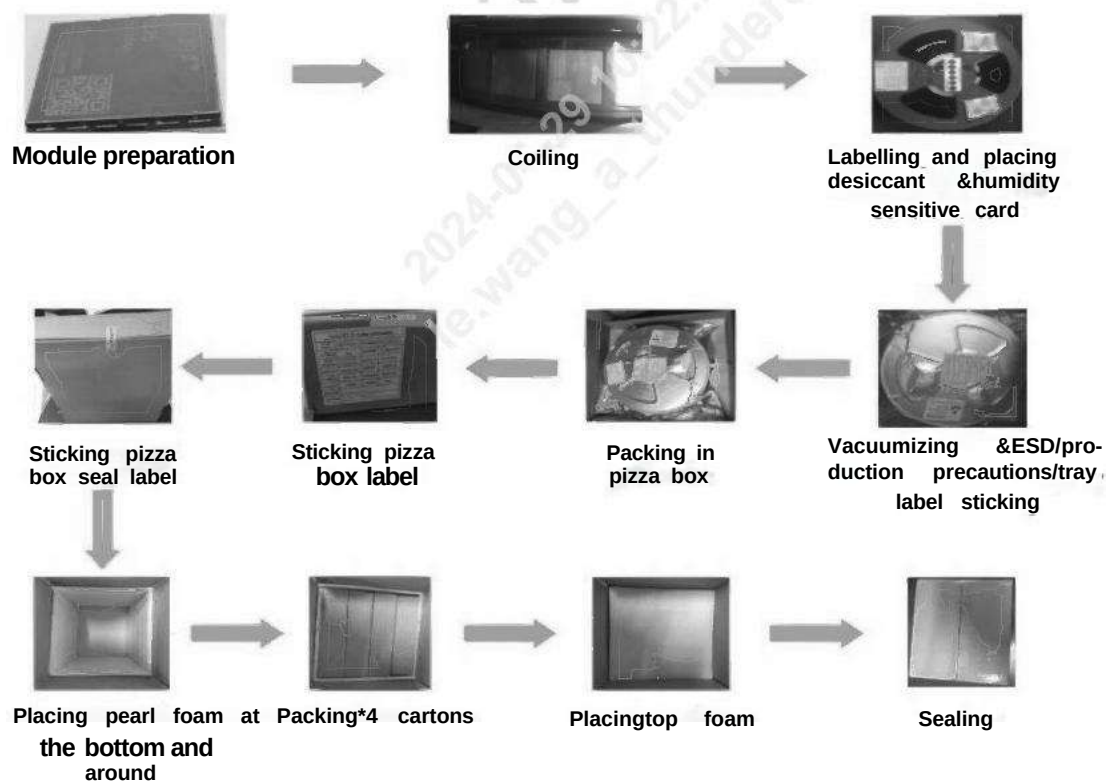


Figure 4-2.Packaging Scheme

—NOTES:

- Before packing,clear all foreign bodies and fingerprint on the shielding case and bottom pad,and put the modules onto the carrier tape.
- Fill the roll with roll core.
- Fill each reel with 150 sets of SOM modules and reserve space for 10 sets before and after the coil.
- Fill each carton with 4 pizza boxes,600 sets of modules per box.

Refer to Figure 4-3 for the C2290 SOM label.

包装标签信息/Label information			
供应商名称 Vendor		客户名称 Customer	
商品名称 Product Name	Smart Module	型号/Model	TurboX C2290
品牌/Brand		产品编码/TPN	
订单号/Order No.		客户料号 Part No.	
生产日期/MFG Date		箱号/Carton No.	
原产地/Made in	China	数量/QTY	
毛重/G. W.		净重/N. W.	
检验结果/0Qc		备注/Remark	

Manufacture: Thundercomm Technology Co., Ltd.
Address: No. 107, Middle Datagu Road, Xiantao Street, Yubei District, Chongqing, China, 401122





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In all EU member states, operation of 5150-5350 MHz is restricted to indoor use only.

Figure 4-3.C2290 SOM Label

4.2.Common packaging for CM2290 SOM modules

Refer to Figure 4-4 below for single-layer tray packaging. The SOM modules shall be chamfered per the tray chamfer and loaded according to the sequence of IMEI number. One Plastic tray(③) can be loaded with 15 sets of SOM.

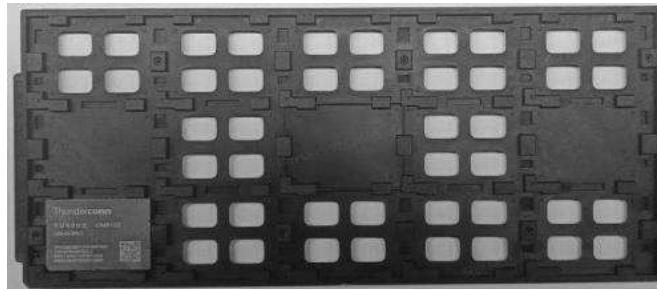


Figure 4-4. Single-layer Tray Packaging

Refer to Figure 4-5 for stacking of trays. Plastic trays(③)are stacked into 11 layers. Put Activated Clay(⑤) at the top and bottom of tray (1 pcs for each),and then put 11 trays into one Foil bag(④).Put the Wet sensitive identification card(⑦)into the Foil bag(④).The packaging capacity of Foil bag(④)is:15*10=150 sets of SOM

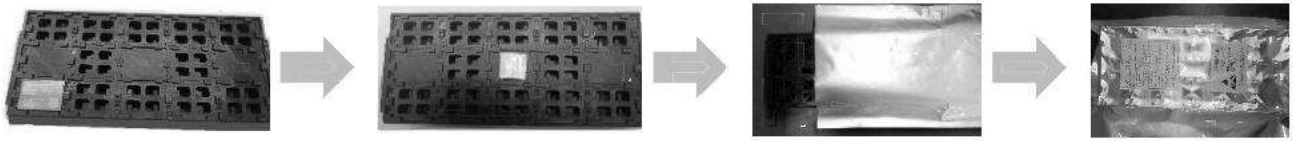


Figure 4-5. Stacking of Trays

The carton packaging is shown as in Figure 4-6. Put two Foil bags ④ into one EPE inner box ②, and then put the EPE inner box ② and Pearl cotton partition ⑥ into a carton ①. The packaging capacity of a carton is: 150*2=300 sets of SOM.

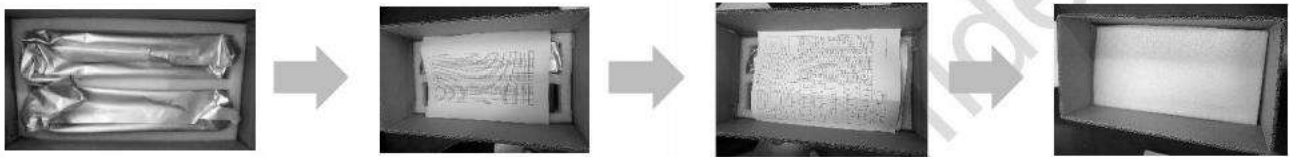


Figure 4-6. Carton Packaging

Table 4-1. BOM list of packaging

Item	PN	Description	Dimensions (mm)	Material	Q' ty
①	TBD	Carton	395*208*206	230/180/120/180/230-BC	1
②	TBD	EPE inner box	385*195*170	20kg/m ³ , antistatic EPE	1
③	TBD	Plastic tray	322.6x136x7.62	PPE (Black)	22
④	TBD	Foil bag	510*260*0.22	Composite of aluminum foil (PET), PE and film	2
⑤	TBD	Activated Clay	2g	N/A	4
⑥	TBD	Pearl cotton partition	385*195*20	20kg/m ³ , antistatic EPE	1
⑦	TBD	Wet sensitive identification card	75*50	Paper card	2
⑧	TBD	Label	100*100	80g coated paper	1

Refer to Figure 4-7 for the label.

包装标签信息/Label information			
供应商名称 Vendor		客户名称 Customer	
商品名称 Product Name	Smart Module	型号/Mode	TurboX CM2290-EMEA
品牌/Brand	TurboX	产品编码/TPN	
订单号/Order No.		客户料号 Part No.	
生产日期/MFG Date		箱号/Carton No.	
原产地/Made in	China	数量/QTY	
毛重/G. W.		净重/N. W.	
检验结果/OQc		备注/Remark	

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Figure 4-7.CM2290 SOM Label

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Appendix 3. Product certification information

FCC Radiation Exposure Statement

This device complies with FCC radiation exposure limits set forth for an uncontrolled environment and it also complies with Part 15 of the FCC RF Rules. This equipment must be installed and operated in accordance with provided instructions and the antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. End-users and installers must be provided with antenna installation instructions and consider removing the no-collocation statement.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- (1) this device may not cause harmful interference, and
- (2) this device must accept any interference received, including interference that may cause undesired operation.

Caution!

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This module is intended for OEM integrators only. Per FCC KDB 996369 D03 OEM Manual v01 guidance, the following conditions must be strictly followed when using this certified module:

KDB 996369 D03 OEM Manual v01 rule sections:

2.2 List of applicable FCC rules

This module has been tested for compliance to FCC:

FCC CFR Title 47, Part 15, Subpart C

2.3 Summarize the specific operational use conditions

The module is tested for standalone mobile RF exposure use condition. Any other usage conditions such as co-location with other transmitter(s) or being used in a portable condition will need a separate reassessment through a class II permissive change application or new certification.

2.4 Limited module procedures

Not application

2.5 Trace antenna designs

Not application

2.6 RF exposure considerations

This equipment complies with FCC mobile radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator & your body. If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.

2.7 Antennas

Antenna Type: Monopole	BT/WIFI 2.4G 1.69dBi
	WIFI 5G 0.7dBi

This device is intended only for host manufacturers under the following conditions:

The transmitter module may not be co-located with any other transmitter or antenna.

The module shall be only used with the monopole antennas that has been originally tested and certified with this module.

The antenna must be either permanently attached or employ a 'unique' antenna coupler.

As long as the conditions above are met, further transmitter test will not be required. However, the host manufacturer is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

2.8 Label and compliance information

The final end product must be labeled in a visible area with the following: "Contains FCC ID: 2AOHHTURBOXC2290". The grantee's FCC ID can be used only when all FCC compliance requirements are met.

2.9 Information on test modes and additional testing requirements

This transmitter is tested in a standalone mobile RF exposure condition and any co-located or simultaneous transmission with other transmitter(s) or portable use will require a separate class II permissive change re-evaluation or new certification.

2.10 Additional testing, Part 15 Subpart B disclaimer

This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement applicable to the final host. The final host will still need to be reassessed for compliance to this portion of rule requirements if applicable.

As long as all conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be respon

sible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Manual Information To the End User:

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual

OEM/Host manufacturer responsibilities

OEM/Host manufacturers are ultimately responsible for the compliance of the Host and Module. The final product must be reassessed against all the essential

requirements of the FCC rule such as FCC Part 15 Subpart B before it can be placed on the US market. This includes reassessing the transmitter module for compliance with the Radio and EMF essential requirements of the FCC rules. This module must

not be incorporated into any other device or system without retesting for compliance as multi-radio and combined equipment

Frequency band: 5150 - 5250 MHz:

Indoor use: Inside buildings only. Installations and use inside road vehicles and train carriages are not permitted.

Limited outdoor use: If used outdoors, equipment shall not be attached to a fixed installation or to the external body of road vehicles, a fixed infrastructure or a fixed outdoor antenna. Use by unmanned aircraft systems (UAS) is limited to within the 5170 - 5250 MHz band.

Frequency band: 5250 - 5350 MHz:

Indoor use: Inside buildings only. Installations and use in road vehicles, trains and aircraft are not permitted. Outdoor use is not permitted.

Frequency band: 5470 - 5725 MHz:

Installations and use in road vehicles, trains and aircraft and use for unmanned aircraft systems (UAS) are not permitted.



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For C2290 CE DOC POWER

Frequency	MAX test power
2400MHZ-2483.5MHZ	19.60 ± 2 dBm
5150MHZ-5250MHZ	17.39 ± 2 dBm
5250MHZ-5350MHZ	17.55 ± 2 dBm
5470MHZ-5725MHZ	16.35 ± 2 dBm
5725MHZ-5850MHZ	13.45 ± 2 dBm