ALT1210MOD-VZ-01 User Module

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Document Revision Control

Edition	Issued By	Date	Description
0.1	Alon K.	17-12-2017	Initial specification
0.2	Alon K.	11-01-2018	Minor modifications and additions
1.0	Alon K.	12-01-2018	FCC statement and end user guidelines

Table of Contents

1. Scope

The purpose of this document is to be used as a basic user manual for designers developing products based on the ALT1210MOD-VZ-01 module.

2. General Specifications

ALT1210MOD-VZ-01 is the smallest CAT-1 LTE module offering LTE connectivity for space constraint devices such as sport watches, kid's trackers, music players and other wearable devices. This module is ideal for moderate bandwidth applications requiring real-time communication along with long battery life.

2.1. General Features

Frequency range	**B4**	UL:1710-1755MHz, DL: 2110-2155MHz
	B13	UL:777-787MHz, DL: 746-756MHz
LTE Category		Category 1 (SW upgradable to CAT-M1)
Bandwidth	**B4**	5/10/15/20MHz
	B13	5/10MHz
Antenna		Single antenna
Carrier		Verizon
Supplies		Li-ion battery compatible and 1.8V always on supply
Operating Temperature		-20°C ~ +60°C
Dimensions		15mmx15mmx1.5mm
Weight		0.8g
Control Options		AT Commands
Data Interface		AT commands over SPI
Debug Interface		USB CDC-ECM
Control Interface		4 wire interface

2.2. Interfaces

SPI	x1 , 4-pin SPI
UART	x2 ,Max throughput 1mbps
E-SIM	1.8V only, external pull-up/down resistor required for clock stop mode
QSPI Flash	Interface for external serial flash (required for module operation) and for internal flash (required for calibration data storage)
HS USB 2.0	Used for production and debug

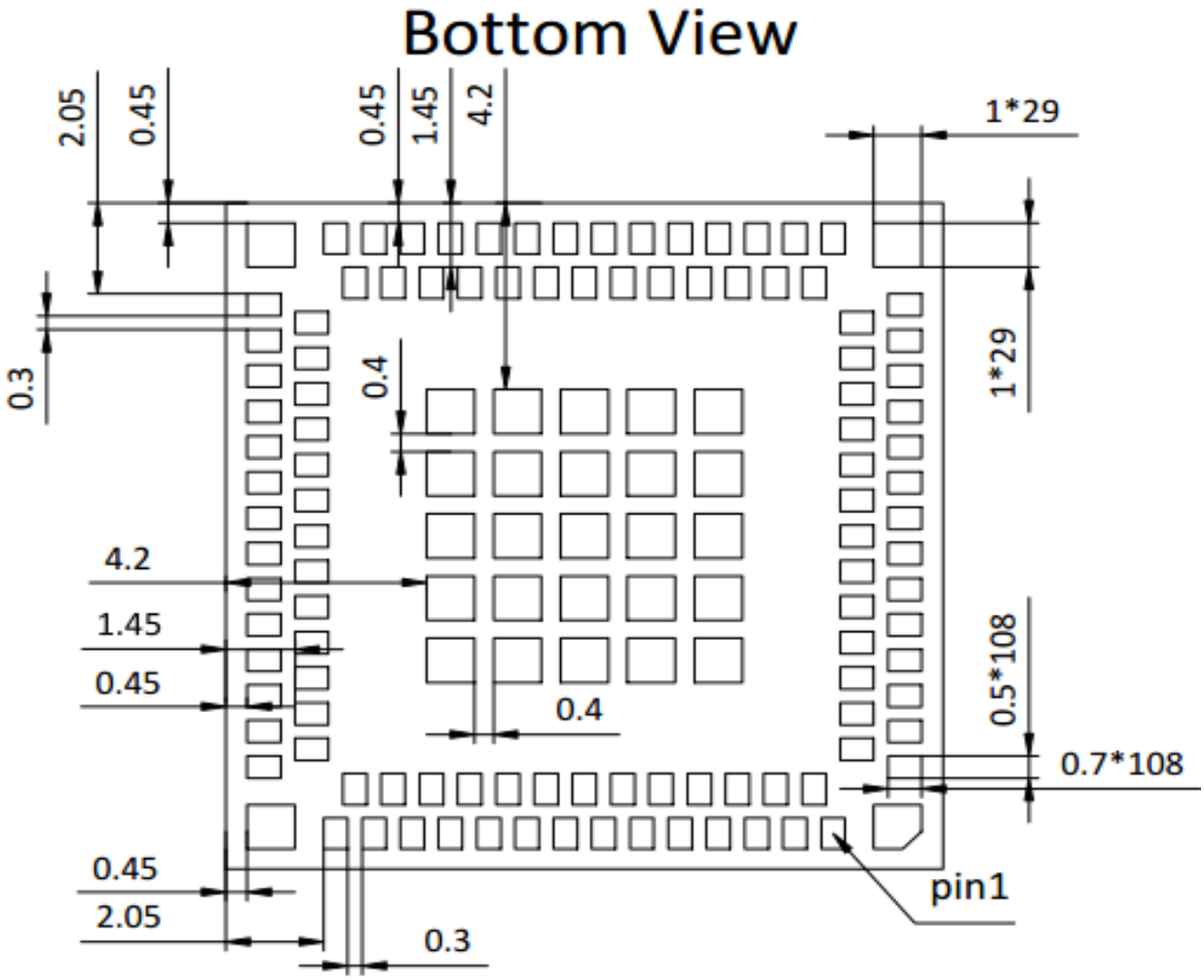
2.3. Electrical Specification

Item	Min	Typ	Max	Units	Notes
Required Power Supplies Rating					
VBAT	3.2	3.8	4.3	V	If USB interface is not used the Vin voltage can be further reduced up to 3.0V
I_{VBAT}			400	mA	
VPA	3.0	3.3	4.3	V	
I_{VPA}			350	mA	For 23dbm max output power
1v8_IO_IN	1.71	1.8	1.89	V	
$I_{1v8\_IO\_IN}$			50	mA	IOs consumption is less than 50mA
VDD_RET_IN	1.71	1.8	1.89	V	
$I_{VDD\_RET\_IN}$			150	mA	
Radio Performance					
Max TX power for B13	22	23	25	dBm	Not including MPR rules
Max TX power for B4	22	23	25	dBm	Not including MPR rules
Sensitivity B13	-94	-96		dBm	10MHz, MCS5, single antenna
Sensitivity B4	-94	-96		dBm	10MHz, MCS5, single antenna

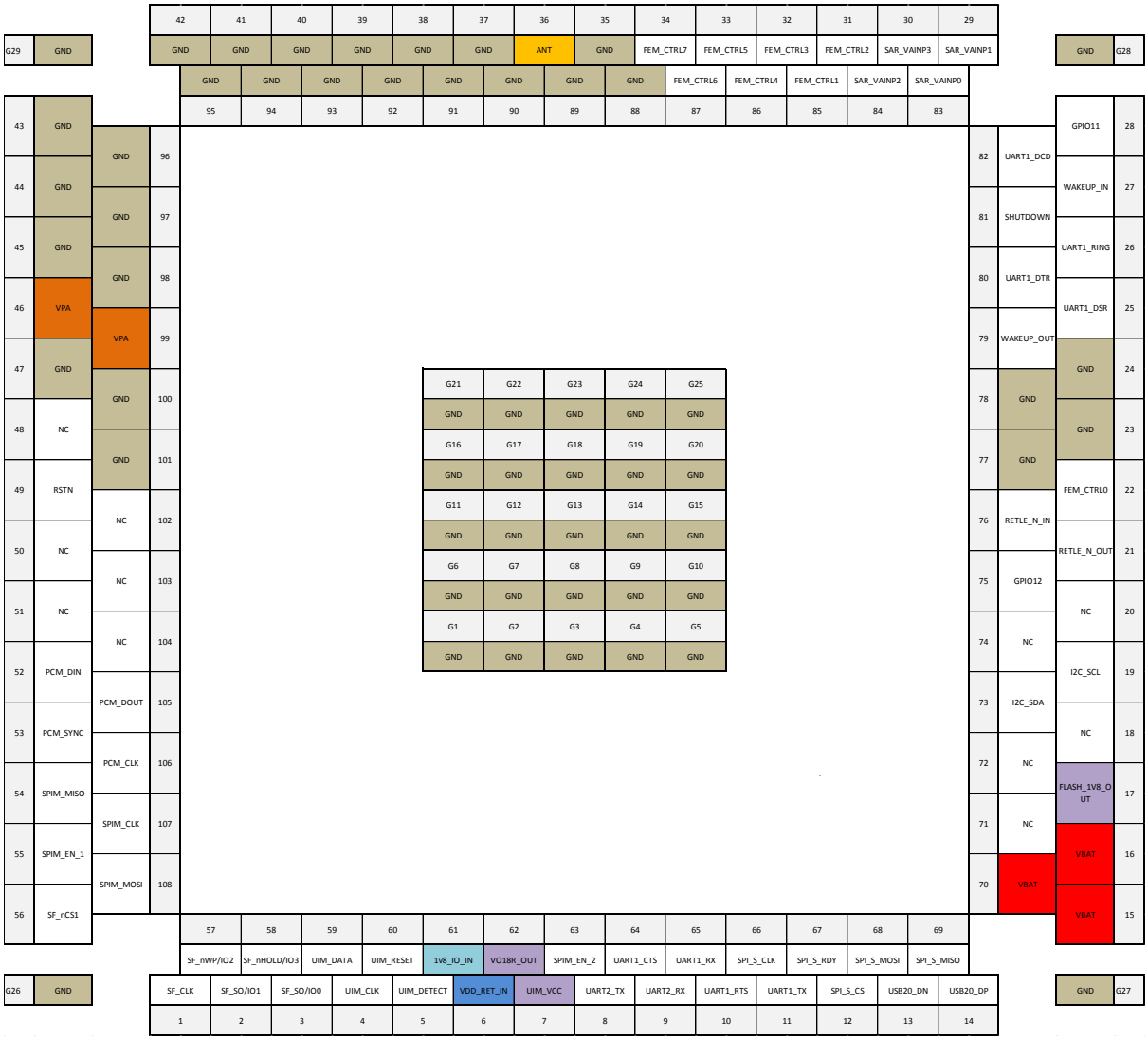
3. Pinout

3.1. Land Pattern

- Module size : 15 X 15 mm
- Pad size :
  - Signal pin: 0.7 X 0.5 mm
  - Thermal pin: 1.0 X 1.0 mm
- Pitch
  - same loop : 0.8 mm
  - 1st to 2nd loop : 1.0mm
- Gap
  - Pad to edge : 0.45mm
  - Pad to pad : 0.3mm



3.2. Pinout (TOP VIEW)



3.3. Pins Description

	Pin name	Pin Description	Pin count
Power Supply Inputs	VBAT	Main module supply 3.4-4.2V	7
	VPA	RF PA output stage supply 3.4-4.2V	
	1v8_IO_IN	1.8V input for module interface IOs	
	VDD_RET_IN	1.8V input for DDR supply (can be supplied from !V8_IO or from VO18R)	
Control pins	WAKEUP	Signal from host to wakeup modem (active high)	7
	HOST_WAKEUP	Signal from modem to wakeup host (active high)	
	SHUTDOWN	Signal from host to shutdown modem (active high)	
	RETLE_N_IN	DDR retention control (Input)	
	RETLE_N_OUT	Default DDR retention control signal (Output)	
	RSTN	Digital reset signal	
	ALARMZ	Optional control line for external module power supply (high=OFF, Low=ON), open drain	
SIM	UIM_VCC	power supply output for external SIM card	5
	UIM_CLK	SIM interface clock signal	
	UIM_DATA	SIM interface data signal	
	UIM_RESET	SIM interface reset signal	
	UIM_DETECT	SIM interface detect signal (Active high)	
USB	USB20_DP	USB interface possitive signal (differential)	2
	USB20_DN	USB interface negative signal (differential)	
UART2	UART2_TX	UART2 TX pin (output)	2
	UART2_RX	UART2 TX pin (input)	
UART1	UART1_TX	UART1 TX pin (output)	4
	UART1_RX	UART1 RX pin (input)	
	UART1_RTS	UART1 RTS pin (output)	
	UART1_CTS	UART1 RTS pin (input)	
I2C	I2C_SDA	I2C interface data signal	2
	I2C_SCL	I2C interafce clock signal	
Serial Flash	FLASH_1V8_OUT	Internal 1.8V digital supply rail	7
	SF_CLK	Serial flash clock signal	
	SF_SI/IO0	Serial flash data in signal	
	SF_SO/IO1	Serial flash data out signal	
	SF_nWP/IO2	Serial flash write protect signal	
	SF_nHOLD/IO3	Serial flash HOLD signal	
	SF_nCS1	Serial flash chips select signal	
SPI Master	SPI_M_CLK	SPI master interface clock signal	4
	SPI_M_MOSI	SPI master interface data out signal	
	SPI_M_MISO	SPI master interface data in signal	
	SPI_M_EN_1	SPI master interface enable pin signal	
SAR ADC	SAR_VAINP0	ADC input	4
	SAR_VAINP1	ADC input	
	SAR_VAINP2	ADC input	
	SAR_VAINP3	ADC input	
Digital IOs (GPIOs and Interfaces)	PCM_CLK	GPIO or PCM interface clock signal	16
	PCM_OUT	GPIO or PCM interface data out signal	
	PCM_IN	GPIO or PCM interface data in signal	
	PCM_FS	GPIO or PCM interface frame sync signal	
	SPI_S_MISO	GPIO or SPI slave data out signal	
	SPI_S_MOSI	GPIO or SPI slave data in signal	
	SPI_S_CS	GPIO or SPI slave chip select signal	
	SPI_S_RDY	GPIO or SPI slave ready signal	
	SPI_S_CLK	GPIO or SPI slave clk signal	
	SPI_M_EN_2	GPIO or SPI master enable2 signal	
	GPIO11	GPIO	
	GPIO12	GPIO	
	UART1_DTR	GPIO or Fast UART DTR signal (input)	
	UART1_RING	GPIO or Fast UART RING signal (output)	
	UART1_DCD	GPIO or Fast UART DCD signal (output)	
	UART1_DSR	GPIO or Fast UART DSR signal (output)	
FEM controls	FEM_CTRL0	FEM control, GPIO or optional source for the RETLE_N_INPUT	8
	FEM_CTRL1	FEM control or GPIO	
	FEM_CTRL2	FEM control or GPIO	
	FEM_CTRL3	FEM control or GPIO	
	FEM_CTRL4	FEM control or GPIO	
	FEM_CTRL5	FEM control or GPIO	
	FEM_CTRL6	FEM control or GPIO	
	FEM_CTRL7	FEM control or GPIO	
Reserved pins	NC	These pins should be kept unconnected	11
RF	ANT	RF antenna for RX/TX	1
Ground		Ground	57
Total Functional			**137**

4. Operational Guidelines

4.1. Power Supplies Considerations

The ALT1210MOD-VZ-01 has 4 seperated power supply inputs in order to allow max flexibility to the developers at the application level, to design their products based on their unique requirements or tradeoffs such as cost, size or power consumption.

4.1.1. VBAT (pins #15,#16 and #70)

This is the main power supply to the integrated PMIC that produces all required supplies for the system. The allowed range for this supply is 3.4 to 4.2V.

It is designed to be connected directly to a Li-ion battery for the most simple devices, but can also be supplied from an external supply if the battery range is not in compatible to the VBAT allowed range or if further power optimization is required.

4.1.2. VPA (pins #46, #99)

This is a dedicated power supply for the RF PAs output stage. This supply max voltage can be 4.3V. The min voltage required in order to meet the TX conformance requirements (mainly ACLR and SEM) at the max TX output power (23dbm) is 3.0V.

There are several options to supply the RF PAs inside the module.

For simple applications wishing to optimize BOM cost or size (at the expense of power consumption), it is possible to supply this rail directly from the battery (Host needs to disable the Modem when the battery voltage drops towards 3.0V).

In applications wishing to optimize the power consumption (at the expense of BOM cost) it is possible to use an external DCDC converter (buck or buck-boost depending on the battery range) to supply the PAs.

It is very important to make sure this DCDC has a rating of more than 600mA output current, have an enable pin and is configured by default to 3.0V or higher.

The modem uses “FEM_CTRL2” pin#31 to enable the DCDC only during actual TX periods to reduce as much as possible power consumption.

4.1.3. 1V8_IO_IN (pin #61)

This is a dedicated power supply for the digital IOs interface. This is usually supplied from the same supply powering the host IOs. The allowed range for this supply is 1.71 to 1.89V.

4.1.4. VDD_RET_IN (pin #6)

This is a dedicated power supply for the DDR memory inside the module. The allowed range for this supply is 1.71 to 1.89V.

There are two options to supply the DDR.

The first one is using the integrated LDO output (“VO18R_OUT” pin #62) for that. This also requires connecting “RETLE_N_OUT” pin #21 to “RETLE_N_IN” pin #76, this configuration uses the relevant output control to put the DDR in retention state when the modem enters lite hibernation state. The advantage of this configuration

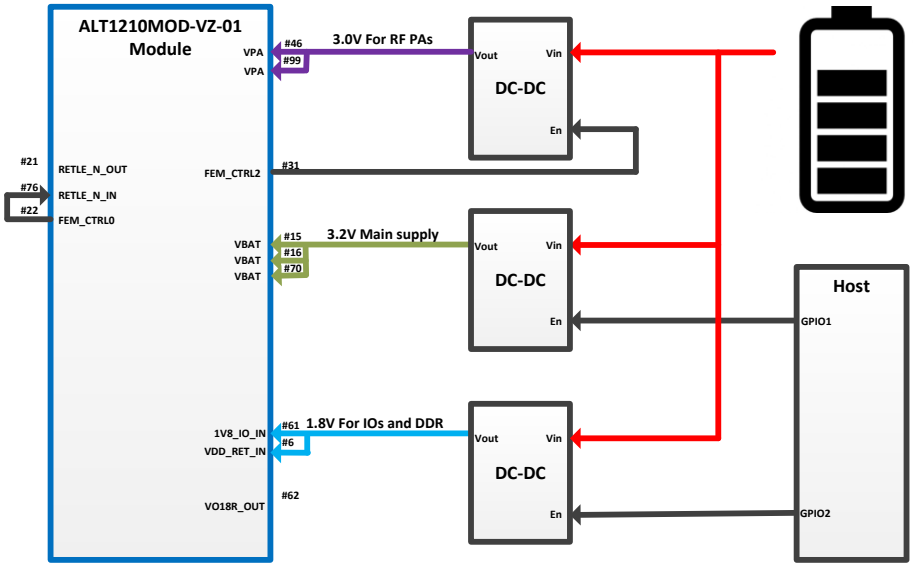
is that it does not require an external power supply for the saving possibly size and BOM cost on the application level.

The second option is using an external supply. The motivation is to allow shutting down additional circuits inside the Module in order to achieve an even lower floor power consumption in lite hibernation mode (~150uA instead of ~250uA). In order for this to be possible you should use an already available supply in the application board or add a dedicated low quiescent DCDC converter for this specific use.

4.1.5. General Power Related Guidelines

For wearable or battery sensitive IOT devices it is recommended to have the ability to completely disconnect all supplies to the module (controlled by the external host) to eliminate any leakage when the modem is not used and therefore optimizing battery life time.

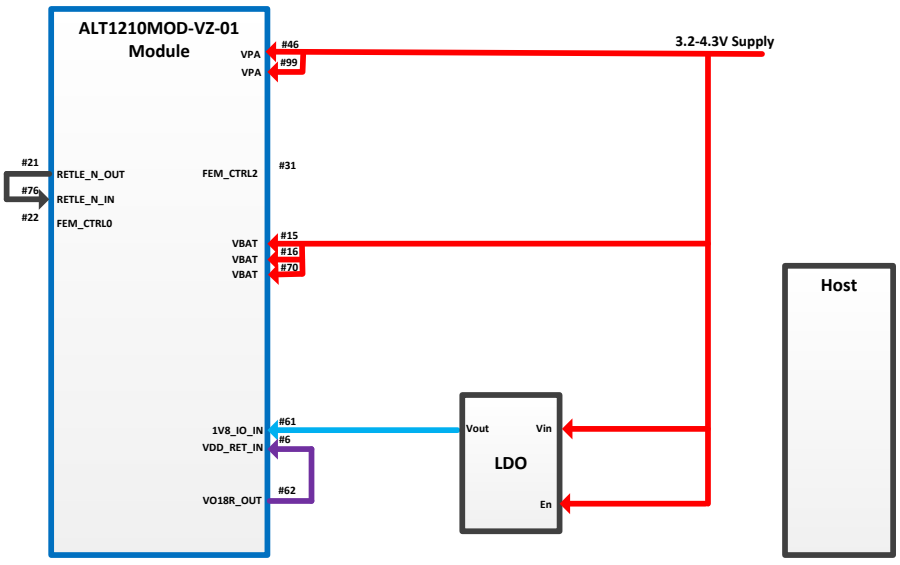
See below a diagram of a typical application aiming to optimize battery lifetime.



It requires additional supplies on application board, but allows shutting down the modem completely when not needed, therefore reducing the power consumption to minimum.

A simpler power supply network maybe used that only uses a single supply on the application board, but has higher power consumption due to leakage and efficiency losses.

See below a diagram of such system.



4.2. Power up and Power Down Sequences

The ALT1210MOD-VZ-01 module has a “Shutdown” control input (pin #81), that actually shutdowns the integrated supplies inside the module when asserted high.

The proper power up sequence would be:

- Shutdown pin is kept high (to prevent the system to boot up before the DDR voltage is available)
- 1.8V_IO_IN and VDD_RET_IN should be applied (1.8V_IN should be available before applying any external signal to the module pins (not including the shutdown pin)
- VBAT should be applied
- VPA is applied (if it is not controlled by the modem itself)
- Shutdown pin is set low

This Flow ensures that all power supplies are stable before the shutdown pin is set low and the system boots up.

The proper power down sequence would be the opposite:

- Shutdown pin is set high (shutting the modem internal supplies and modem)
- VPA shutdown (if it is not controlled by the modem itself)
- VBAT is shut down
- 1.8V_IO_IN and VDD_RET_IN are shut down

4.3. Specific Interfaces Guidelines

The module has multiple interfaces allowing it to be used for a very wide variety of applications. The following sections provide some detailed explanation on how to connect and use these interfaces.

4.3.1. RF (Pin #36)

The ALT1210MOD-VZ-01 has a single RX/TX antenna pad. This pad should be connected to the device antenna (dual band 4,13 antenna) through a 50ohm impedance trace.

It is very important to keep this trace as short as possible to reduce extra loss and away from any noisy circuits on the application board to avoid any degradation in the module sensitivity performance.

4.3.2. Host Interface (Pins #27 and #79)

This Interface allows both the Host and the modem to enter their power consumption savings states whenever possible, in order to optimize power consumption. The idea is to have a simple interface allowing the host and modem to wake each other up when required and to acknowledge once ready.

Due to the GPIOs quantity limitation in most Host processors this simple interface only uses two lines.

For a more detailed explanation on this interface implementation please check “Altair_SW_219_Rev2_host_interface_HL_design” application note.

4.3.3. UIM Interface (Pins #4, #59, #60, #5 and #7)

This Interface allows the use of an external 1.8V sim card on the application board.

The external SIM is powered from an internal 1.8V regulator (VSIM (pin# 7).

Please note the modem only supports 1.8V SIM/eSIM cards and requires the use of external pull up/down resistors to maintain the polarity of the SIM_CLK line for eSIM devices.

Regular SIM devices may be used externally to the module, but since all modem digital IOs are not maintained during hibernation states, if there is a need to maintain the SIM ON during modem hibernation states, it is necessary to add an external latch to keep the UIM_CLK value.

4.3.4. USB Interface (Pins #13 and #14)

The ALT1210MOD-VZ-01 module also supports USB 2.0 interface (primarily used for production and debug purposes due to the extra power consumption).

The USB interface requires proper SW drivers. For more information on the proper drivers to be used please contact Altair application team.

4.3.5. UART1 (Pins #11, #65, #10, #64 and optional #80, #26, #82, #25)

The UART1 interface is a 1mbps UART interface. It can be used as a two pin interface, 4 pin interface or even 8 pin interface.

4.3.6. UART2 (Pins #8 and #9)

The UART2 interface is a 1mbps UART interface. It can be used only as a simple two pin interface.

4.3.7. I2C (Pins #19 and #73)

The ALT1210MOD-VZ-01 module can also operate as the Master of an I2C bus to control external devices. These two signals require external 10k ohm pull-up resistors to 1V8_IO_IN rail.

4.3.8. Serial Flash Interface (Pins #17, #1, #3, #2, #57, #58 and #56)

The ALT1210MOD-VZ-01 module has an internal small flash memory to store the calibration and configuration files. The actual firmware is loaded from an external Flash located on the application board. The external and interna flash devices share the same interface bus, but have separated SF_nCSx lines. The boot is done from the external Flash controlled by SF_nCS1. Both the external and internal flash devices are powered by the internal regulator FLASH_1V8_OUT (Pin #17).

4.3.9. SAR_VAINPx (Pins #83, #29, #84 and #30)

The ALT1210MOD-VZ-01 has 4 ADC converters to measure external signals. The readings can be done by AT command or from the application layer.

4.3.10. SPI Master (Pins #107, #108, #54, #55 and #63)

This is a 4 wire bus, with two chip select lines in order to allow the module to be able to control two separate slave devices.

4.3.11. SPI Slave (Pins #66, #68, #69, #12 and #67)

This is the primary interface to the host. The Host is the Master on the bus.

4.3.12. PCM (Pins #53, #52, #105, and #106)

This is an AUDIO interface to be connected to voice hub or codec devices in order to enable voice enbled devices. Please contact Altair application team for specific requirements and availability of such options.

4.3.13. GPIOs

Digital IOs can be used by the application layer as general purpose IOs. Please see section 3.3 or contact Altair Application team for more information on how to use these pins for different purposes.

5. Regulatory Compliance

5.1.1. FCC

Please notice that if the FCC identification number is not visible when the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. This exterior label can use wording such as the following: “Contains FCC ID: 2AN5Z-001R1” any similar wording that expresses the same meaning may be used.

Manual Information to the End User:

1. The ALT1210MOD-VZ-01 module is limited to OEM installation ONLY.
2. The OEM integrator should provide a user manual that should clearly indicate the operating requirements and user guidelines.
3. The OEM is responsible for ensuring that the end-user has no manual instruction to remove or install the module.
4. This device complies with FCC radiation exposure limits set forth for an uncontrolled environment and it should be installed and operated with a minimum distance of 5.3 cm between the radiator and an extremity (such as an arm) or 7.9 cm between the radiator and the body. If an end product incorporates this module in a configuration where it would be closer to an extremity or the body (a portable/wearable device) then SAR testing would be required. The integrator is responsible for ensuring compliance in the host, which could involve power reduction control.
5. This transmitter module has not been evaluated for simultaneous operation with other transmitters. In a multi-transmitter integration scenario, an evaluation must be performed to ensure RF Exposure compliance. The integrator is responsible for ensuring compliance in the host.

5.1.2. GCF

This device complies with the 3GPP Rel 9 specification.

5.1.3. Verizon wireless conformance

This device complies with Verizon Wireless conformance