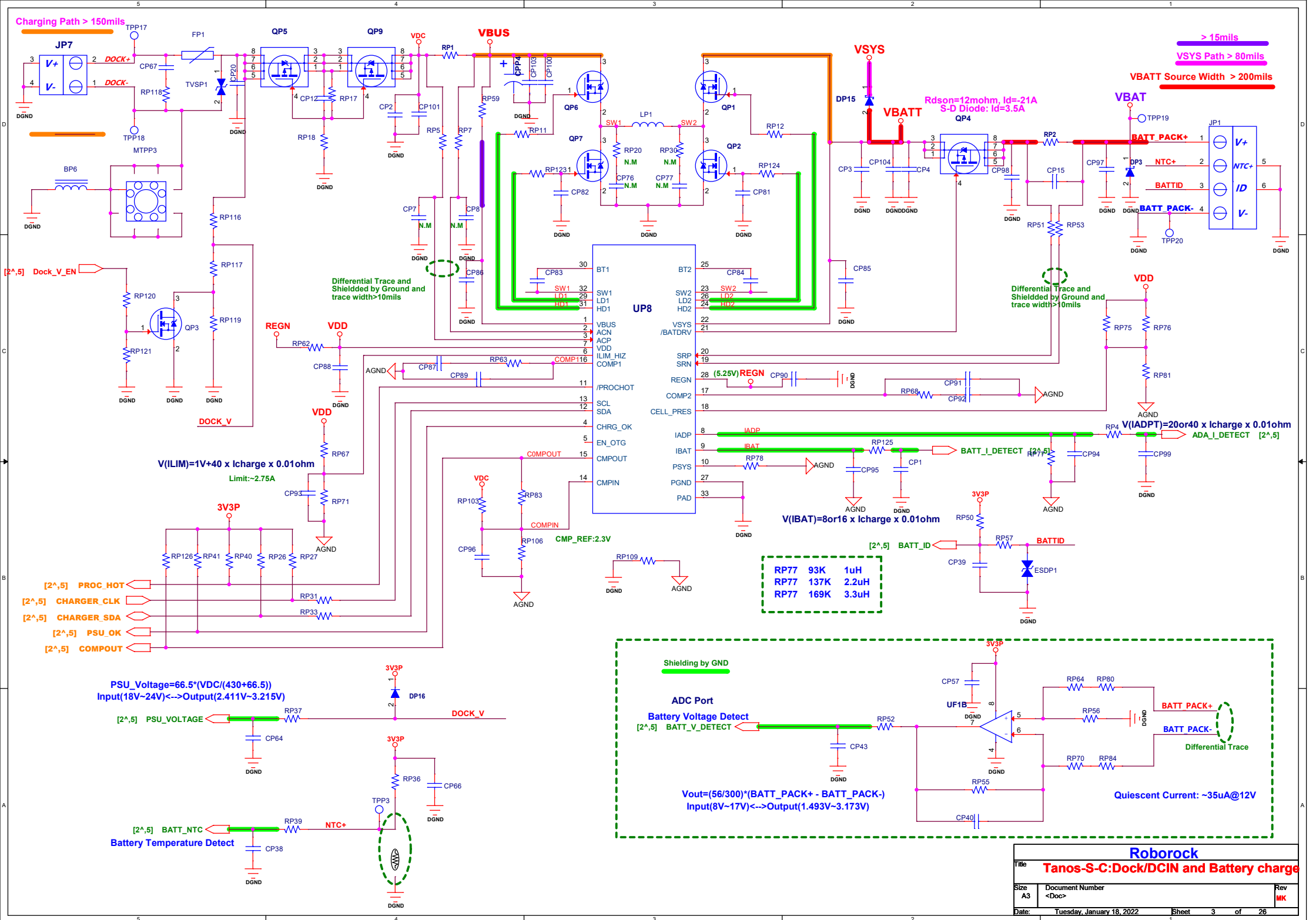
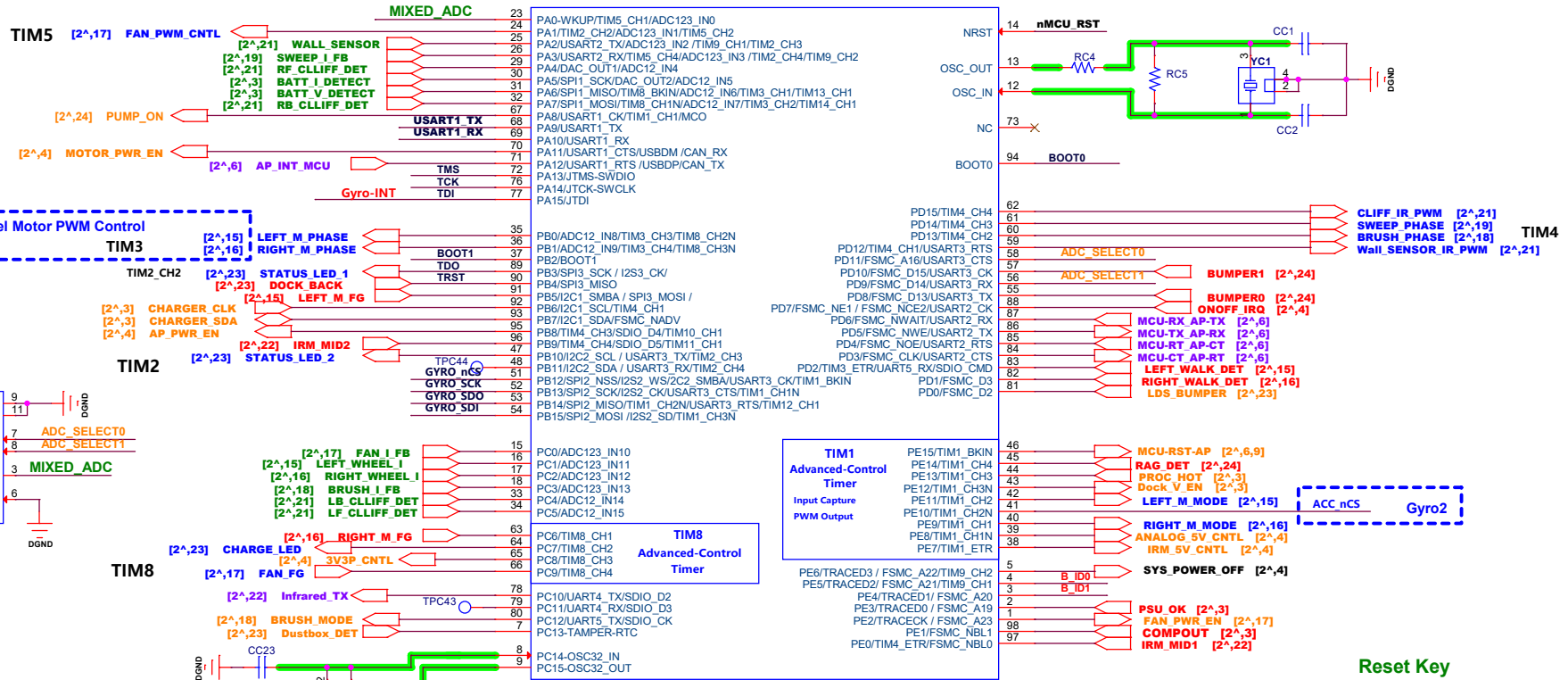




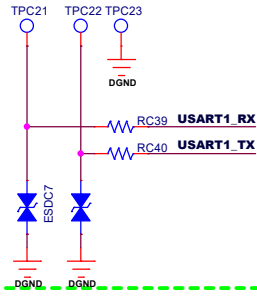
The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

UC1A

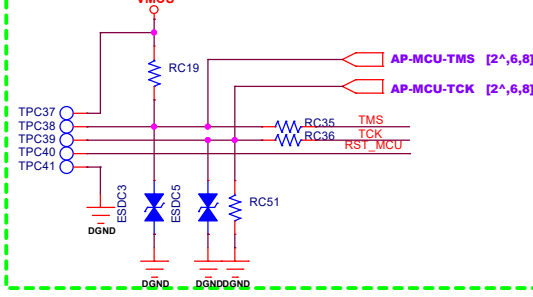


Font Color	Meaning
Blue	PWM Control Signal and high speed capture
Green	Analog: ADC/DAC
Red	Interrupt
Purple	Communication w/ AP
Orange	General GPIO

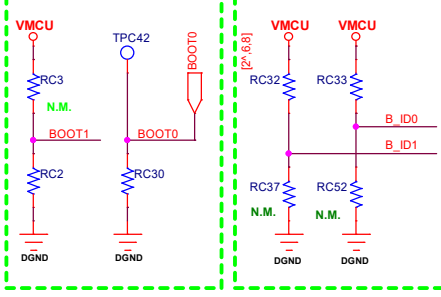
UART: for Debug and Download



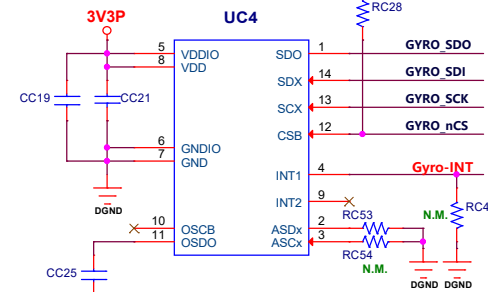
SWD Connector



Board Version

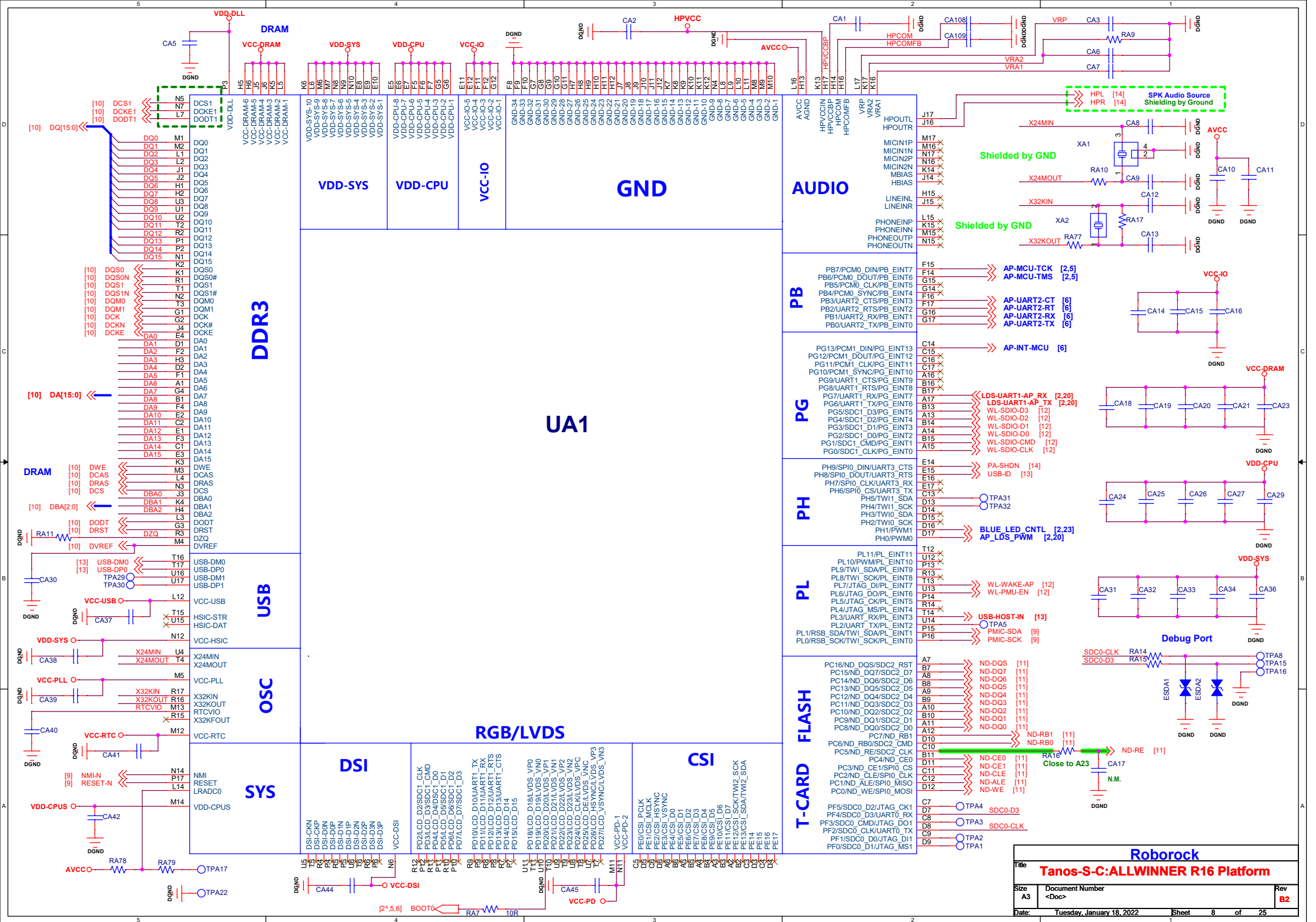


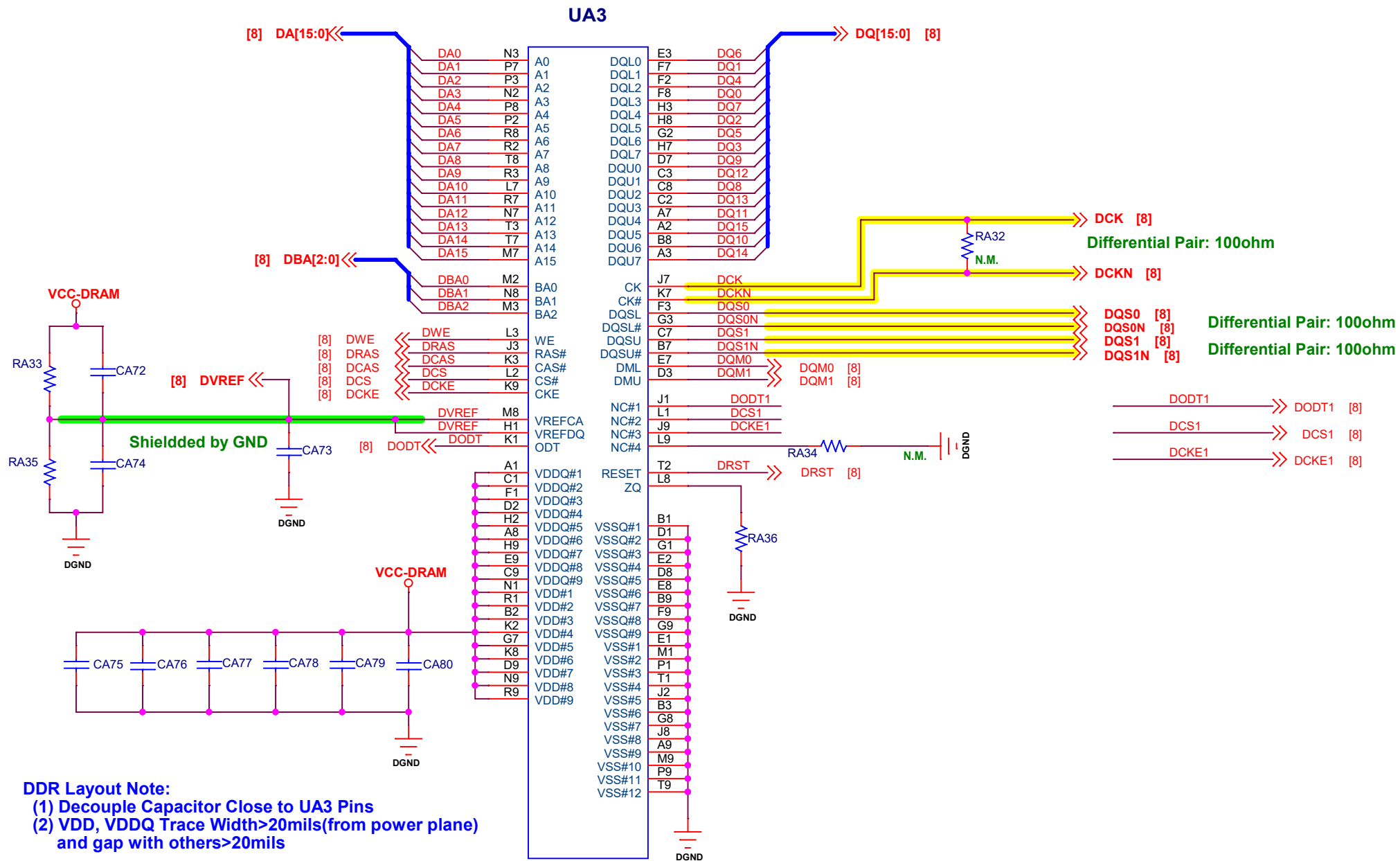
Gyro1



Roborock

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Tanos-S-C:MCU GD32F303VCT6		
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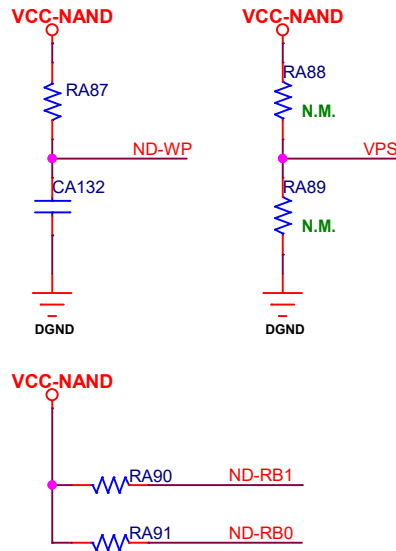
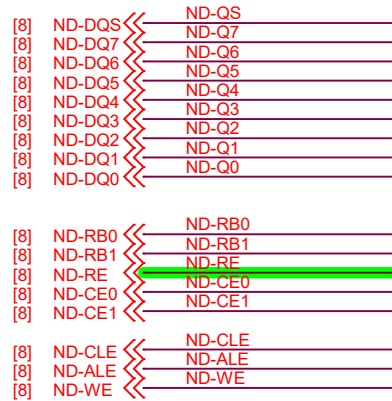




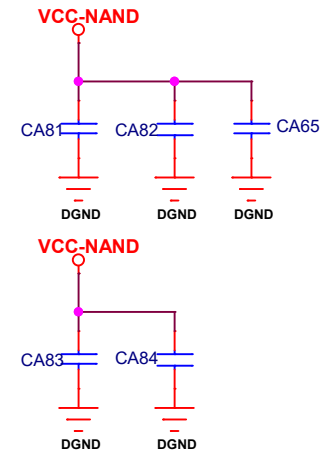
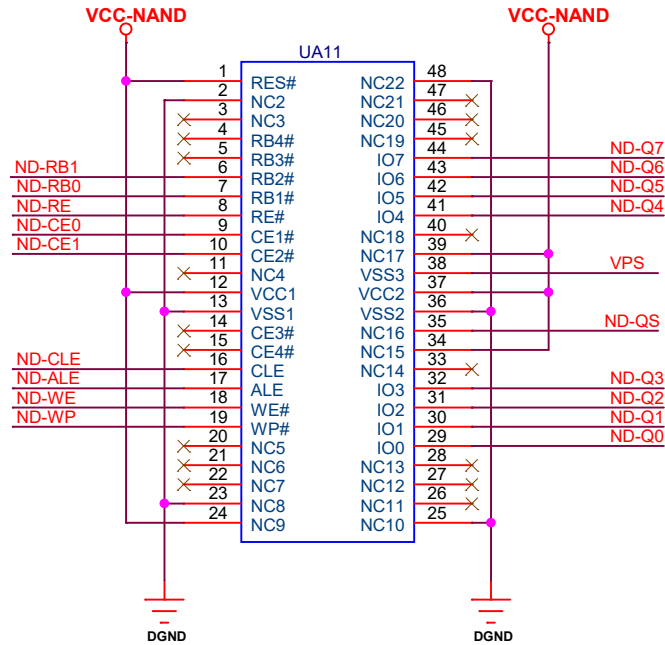
DDR Layout Note:

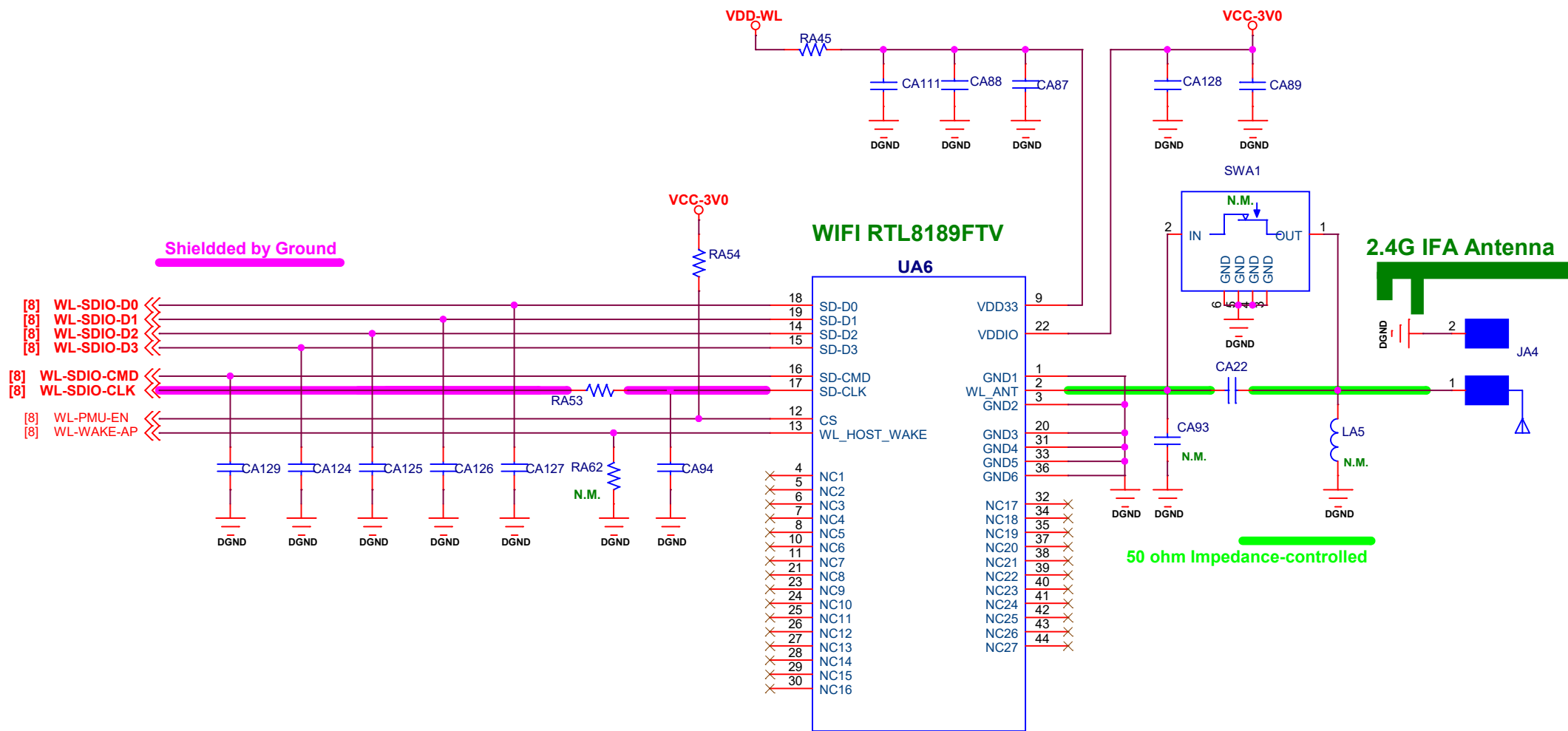
- (1) Decouple Capacitor Close to UA3 Pins
- (2) VDD, VDDQ Trace Width>20mils(from power plane) and gap with others>20mils
- (3) Trace Impedance:
 - (a) Single-ended signal trace are to be 50 ohm+-10%.
 - (b) Differential signal trace are to be 100 ohm +- 10%.
- (4) Differential clocks CK, CK#
 - (a) Differential line length match: within +- 25 mils;
 - (b) Trace length with DQS and DQS#: within +- 10 mils

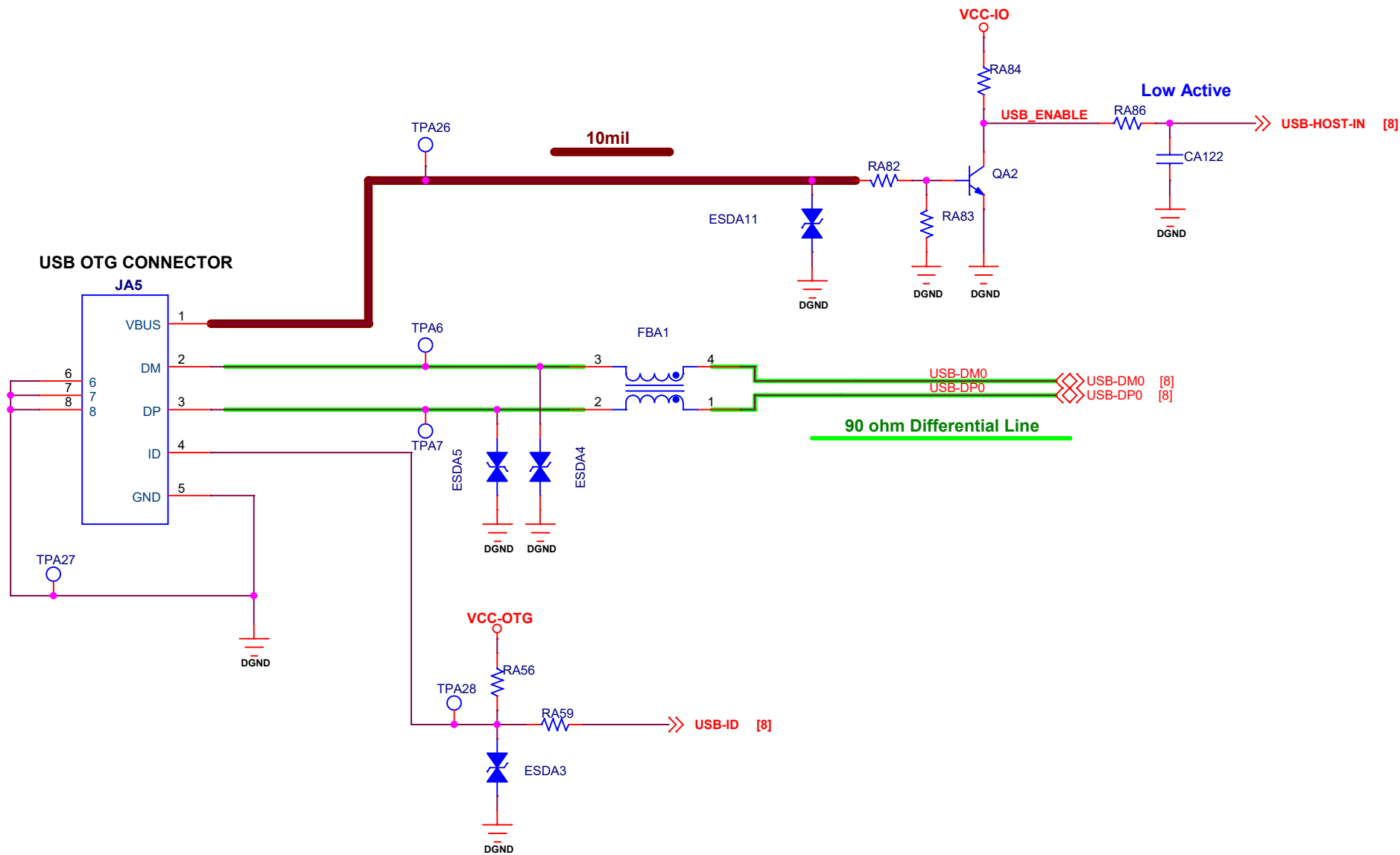
Roborock		
Title		
Tanos-S-C:DDR3		
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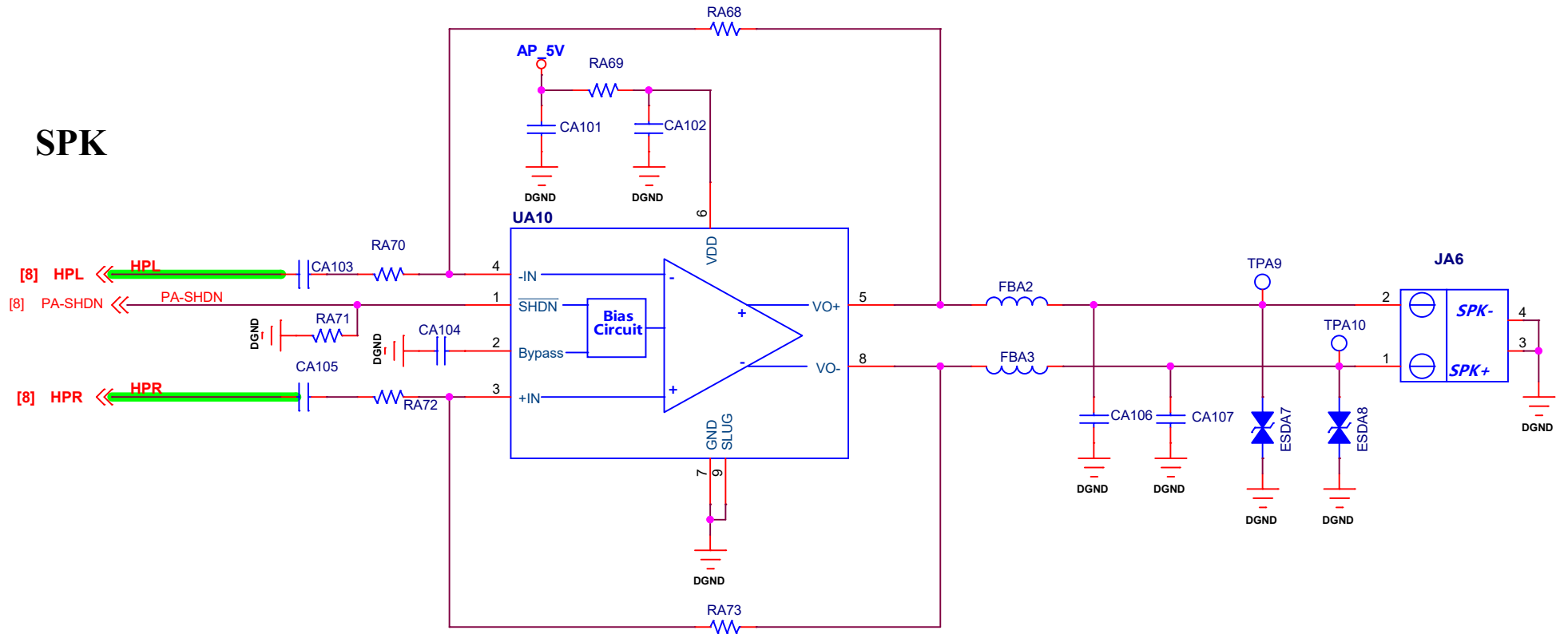
Nand Flash

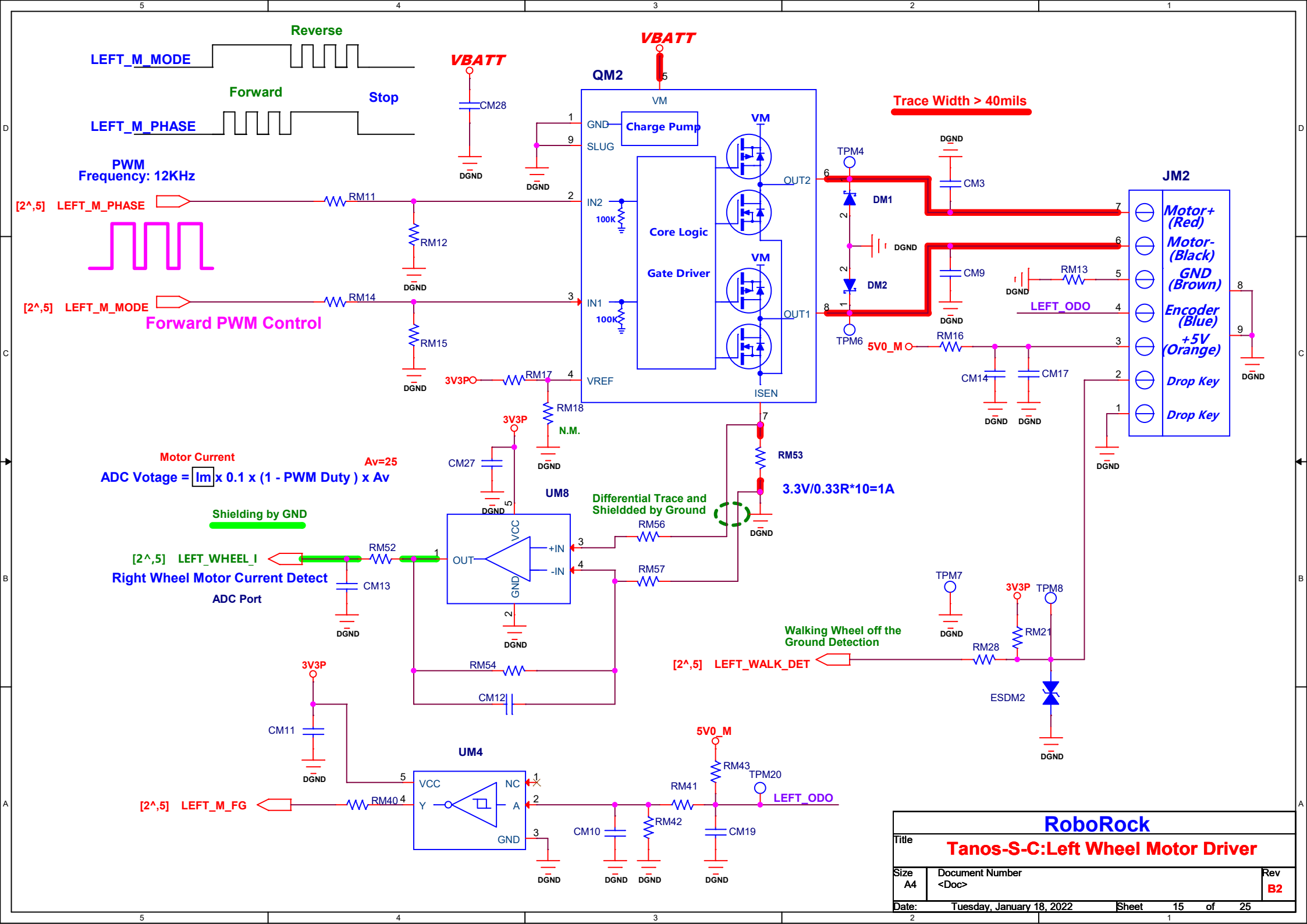


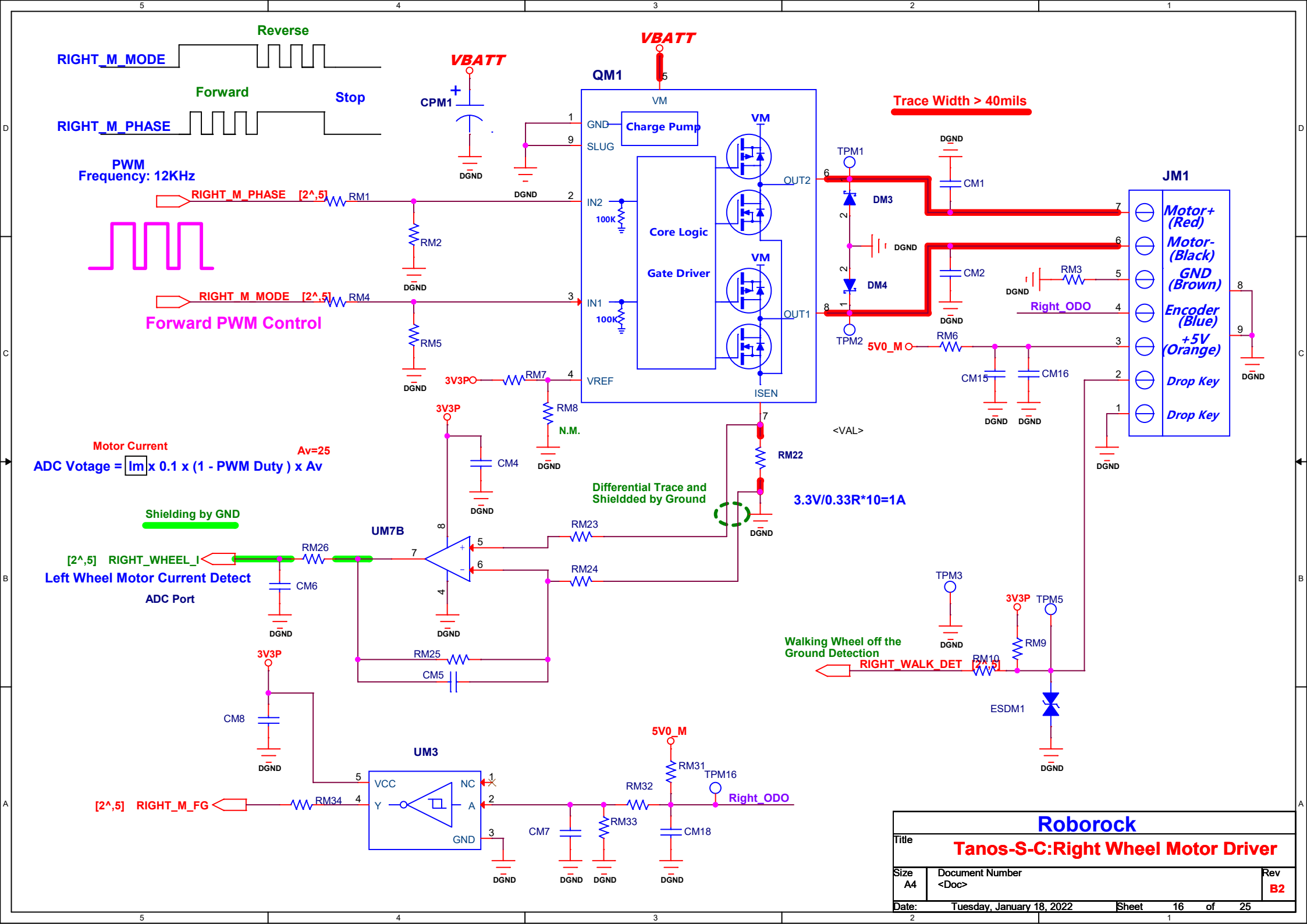


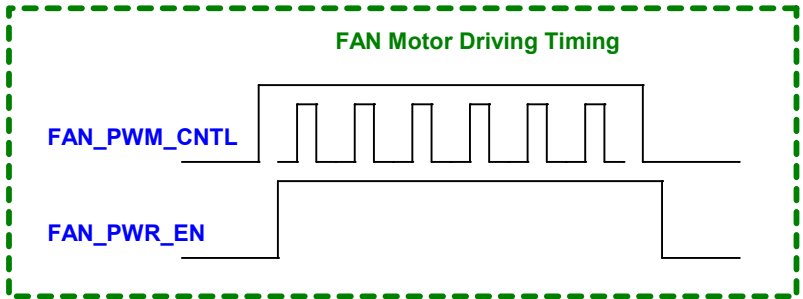
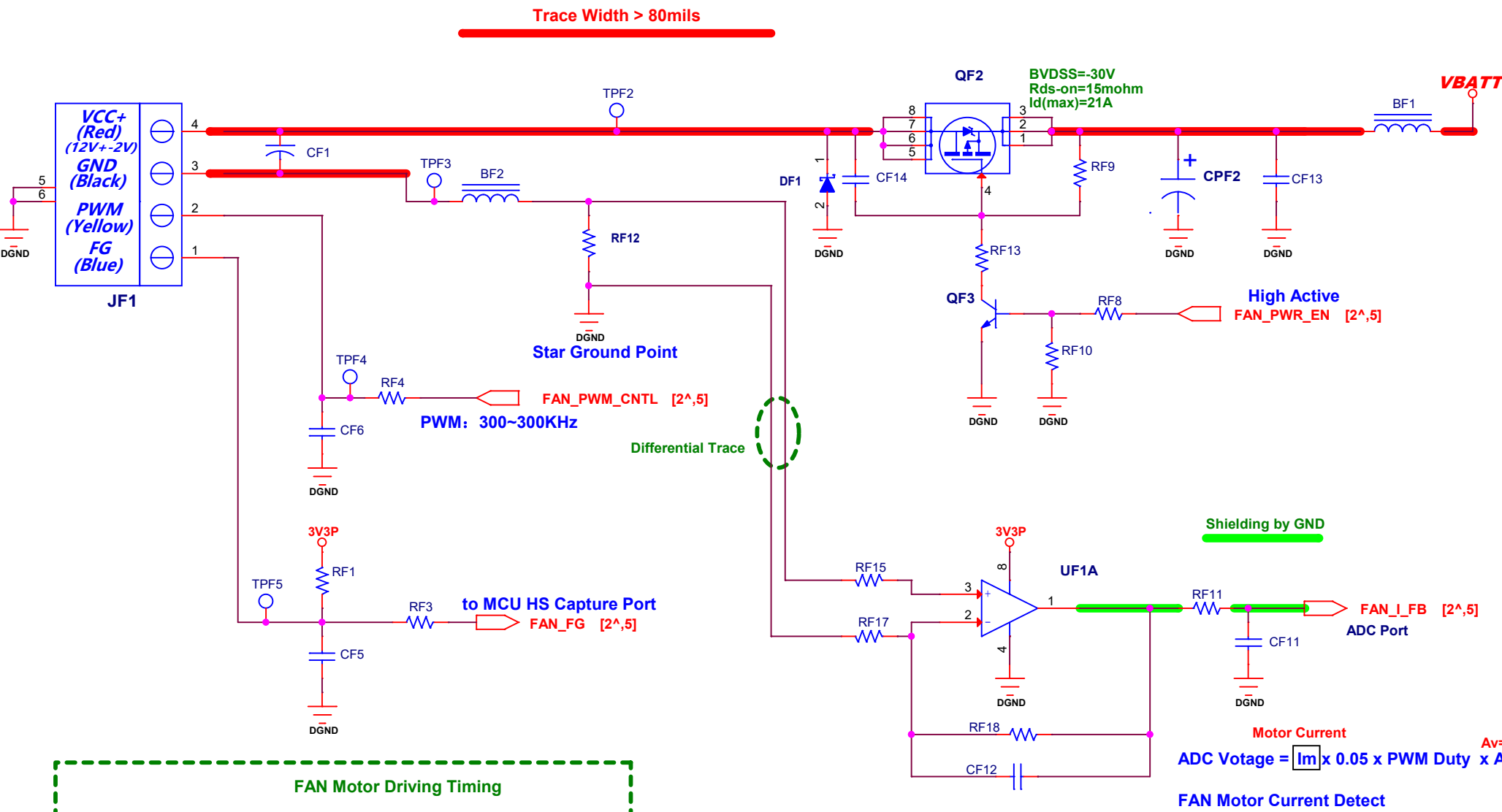


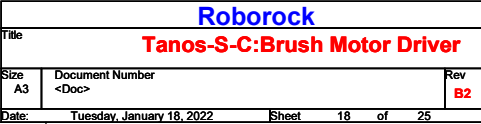
SPK

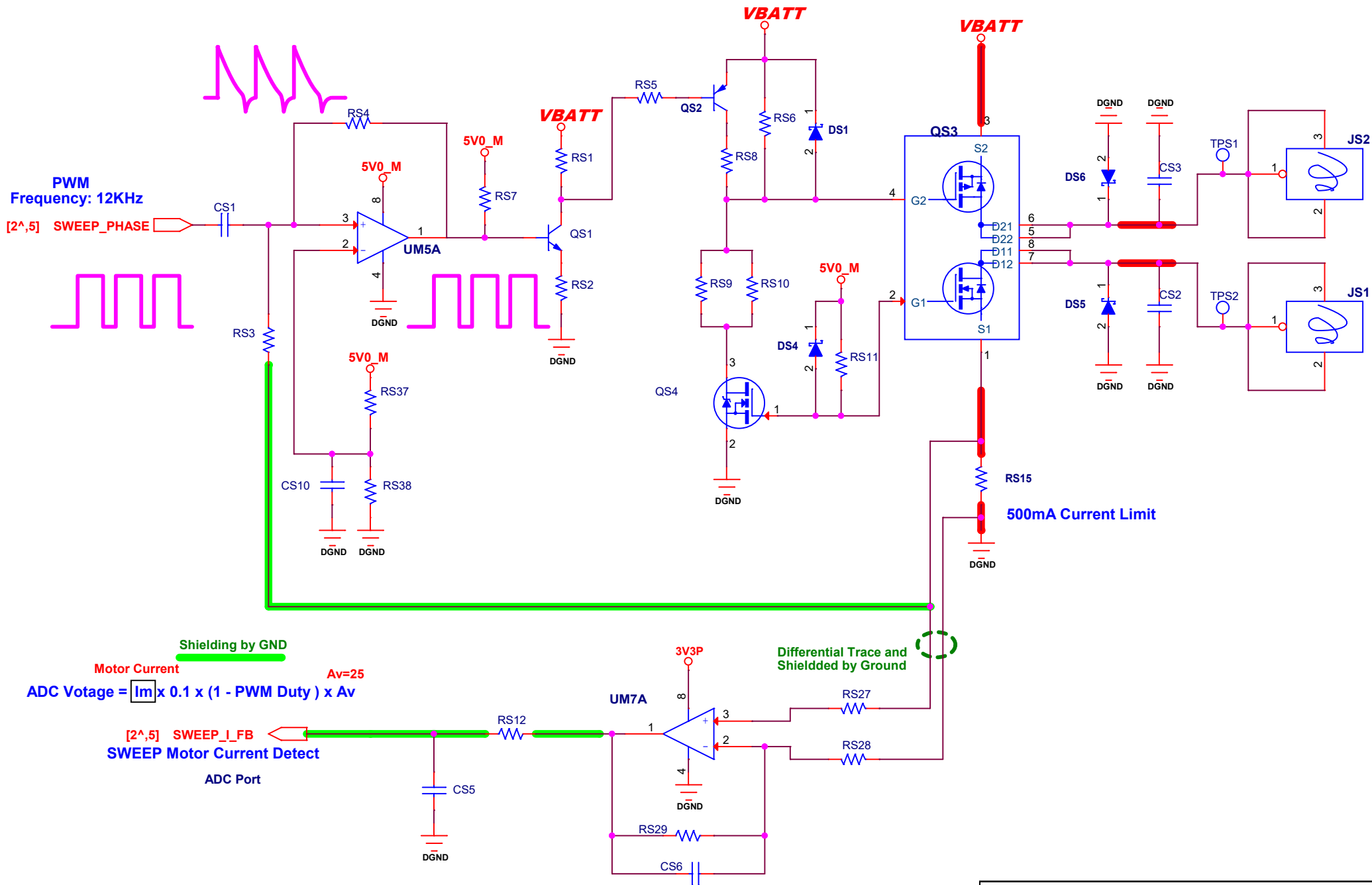




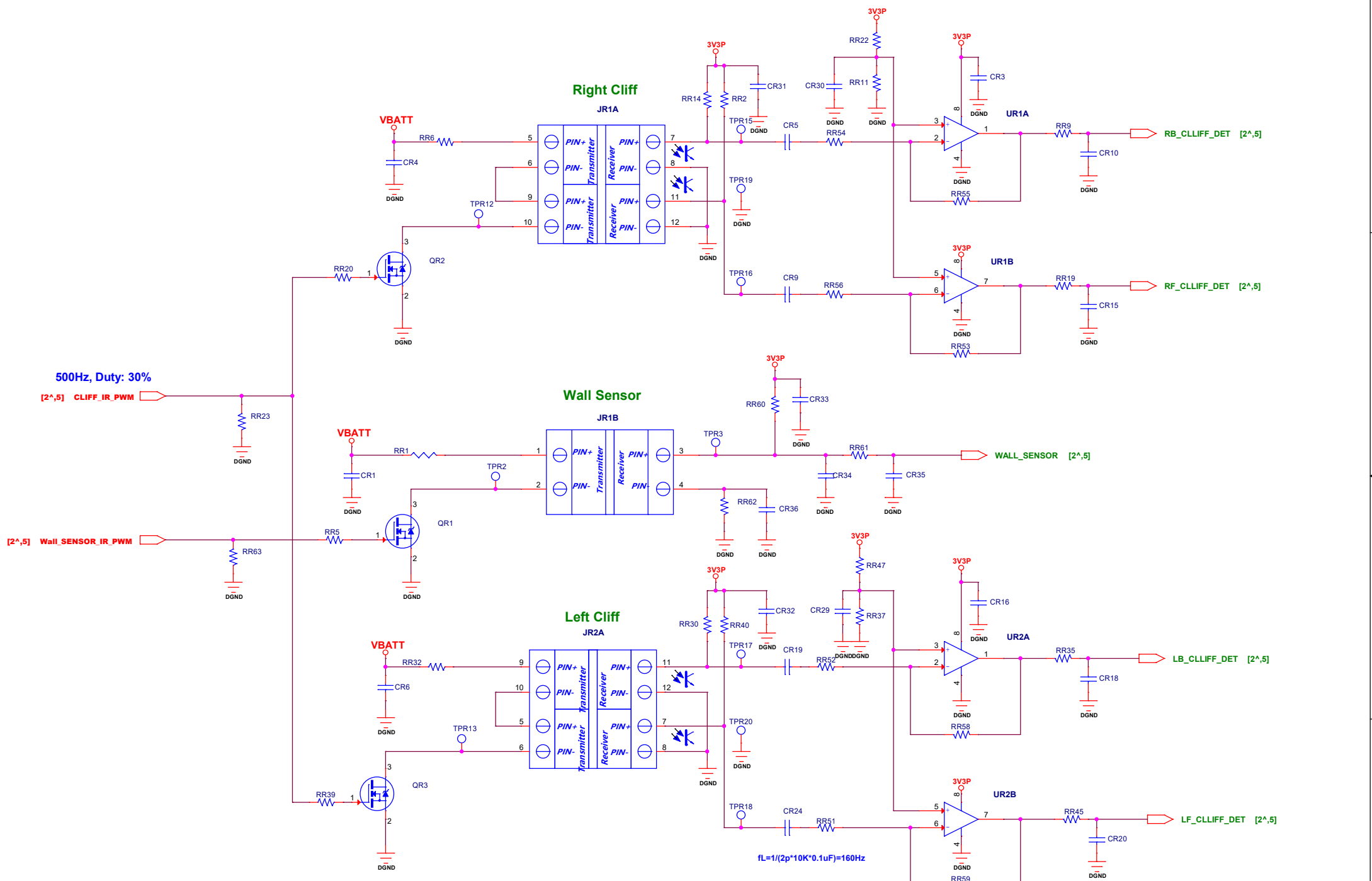


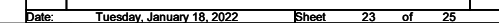






RoboRock			
Title			
Tanos-S-C:Sweep Motor Driver			
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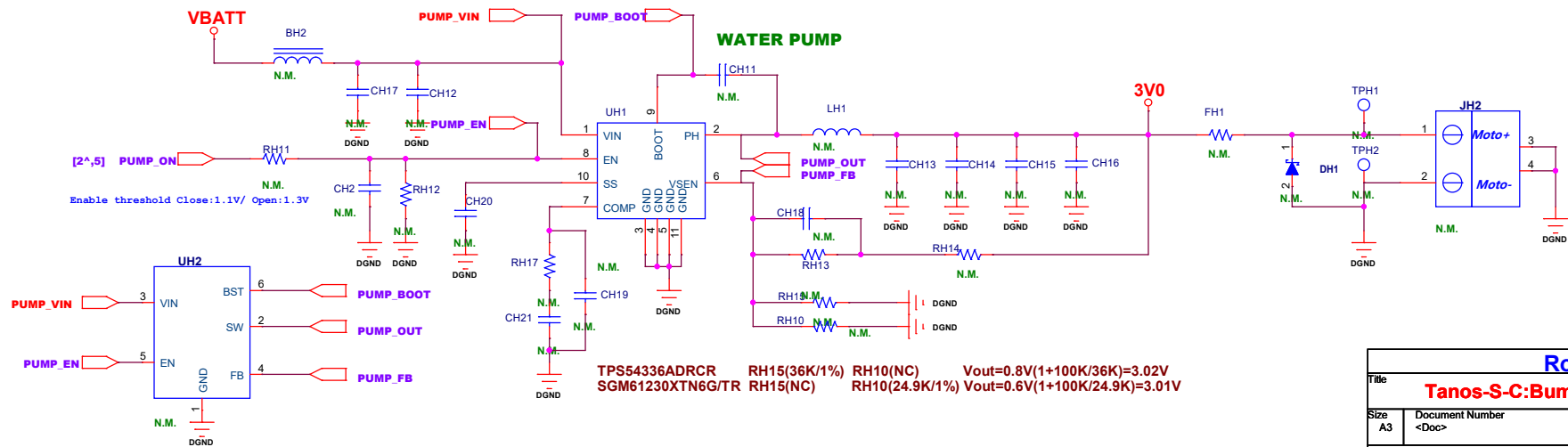
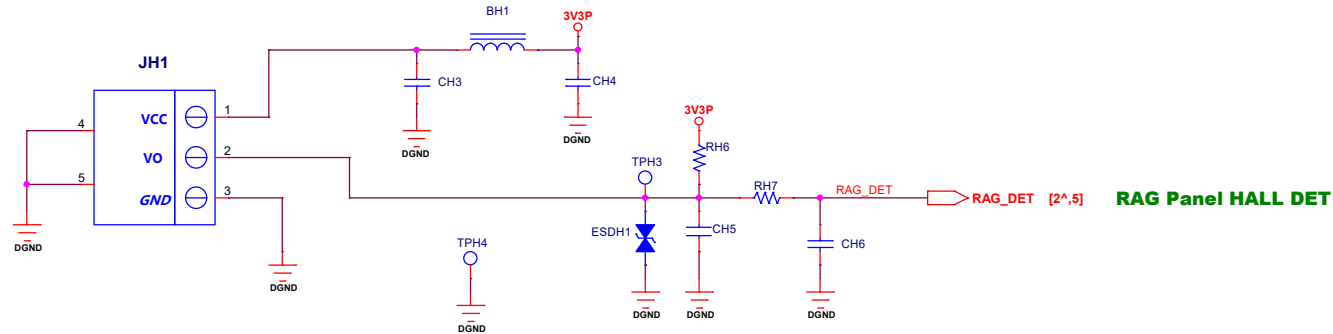




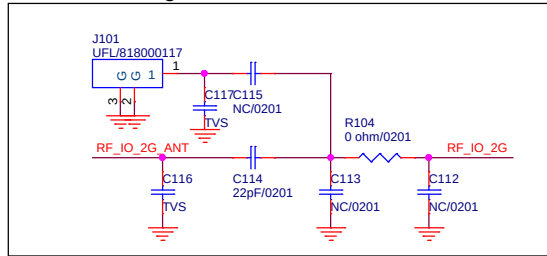
The image contains two circuit diagrams, one for the Left Bumper and one for the Right Bumper.

Left Bumper: This circuit uses a JR2B component. Pin 1 is connected to a 5V0A supply through a resistor RH3. Pin 2 is connected to DGND. Pin 3 is connected to a 3V3P supply through a resistor RH4, with a test point TPH13 located between the resistor and the component. Pin 4 is connected to DGND. Pin 13 is connected to DGND, and pin 14 is also connected to DGND. The output of the component is connected to a resistor RH16, which is then connected to a capacitor CH8 (connected to DGND) and a bumper input labeled BUMPER0 [2*,5].

Right Bumper: This circuit uses a JR1C component. Pin 15 is connected to a 3V3P supply through a resistor RH1, with a test point TPH15 located between the resistor and the component. Pin 16 is connected to DGND. Pin 13 is connected to a 5V0A supply through a resistor RH5. Pin 14 is connected to DGND. Pin 17 is connected to DGND, and pin 18 is also connected to DGND. The output of the component is connected to a resistor RH2, which is then connected to a capacitor CH1 (connected to DGND) and a bumper input labeled BUMPER1 [2*,5].



RF Matching



Boot strap	GPIO12
SDIO	0(default)
SPIDATA	1

VDDIO — R105 — NC/10K/5%/0201 — GPIO12

GPIO00/GPIO01 for UART_Debug_Log

LDO_EN

