# SUNRISE Technology

# SPECIFICATION

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**PRODUCT NAME :** AI00340

2.4G Wireless Transceiver Module

| | APPROVED | CHECKED | PREPARED | DCC ISSUE |
|---|---|---|---|---|
| NAME | | | | |

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# 2.4G Wireless Transceiver Module

## Key Features

- Worldwide 2.4GHz ISM band operation
- Up to 1Mbps on air data rate
- Ultra low power operation
- 11.3mA TX at 0dBm output power
- 12.3mA RX at 1Mbps air data rate
- 900nA in power down
- 22μA in standby-I
- On chip voltage regulator
- 1.9 to 3.6V supply range
- Enhanced ShockBurst™
- Automatic packet handling
- Auto packet transaction handling
- 6 data pipe MultiCeiver™
- Air compatible with Nordic nRF24L01+, nRF2401A, 02, E1 and E2
- Low cost BOM
- ±60ppm 16MHz crystal
- 5V tolerant inputs
- Compact 20-pin 4x4mm QFN package

### Power Supply

- VDD input is 1.9V to 3.6V

### Antenna

- Printed Antenna

### Temperature

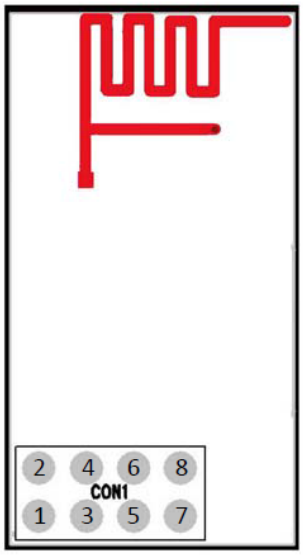
- Operating temperature: -40℃ to +85℃
- Storage temperature: -65℃ to +150℃

## Applications

- Wireless PC Peripherals
- Mouse, keyboards and remotes
- 3-in-one desktop bundles
- Advanced Media center remote controls
- VoIP headsets
- Game controllers
- Sports watches and sensors
- RF remote controls for consumer electronics
- Home and commercial automation
- Ultra low power sensor networks
- Active RFID
- Asset tracing systems
- Toys

# 1、Interface Description

## 1-1. PIN Diagram

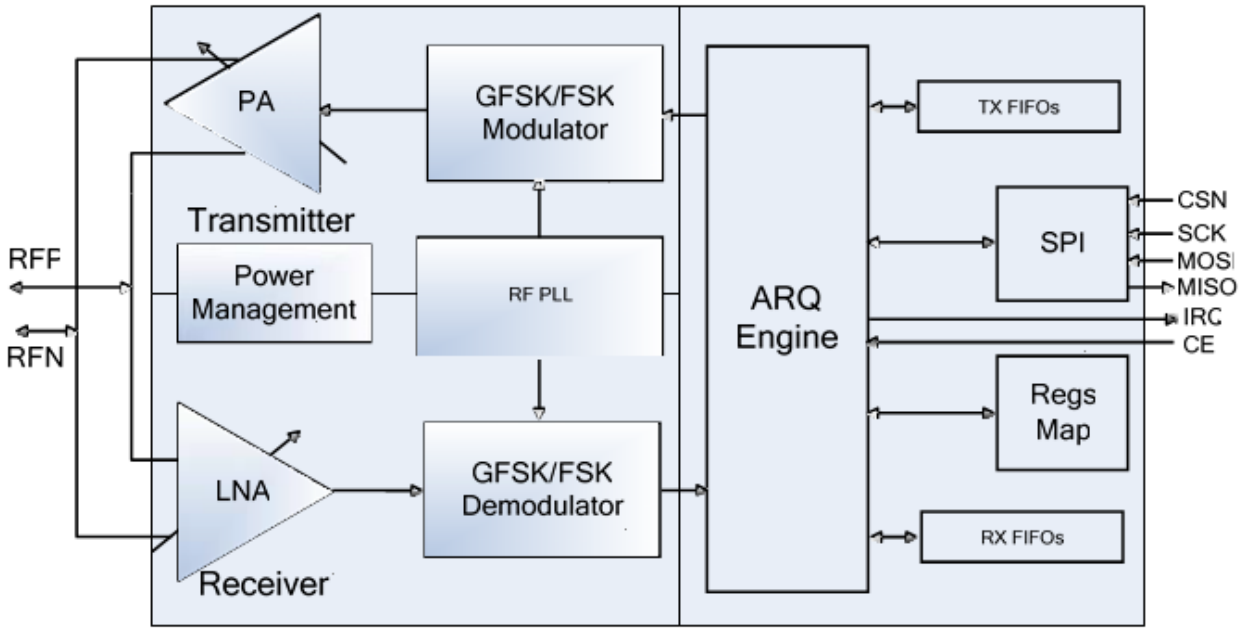



| PIN | Name |
|---|---|
| 1 | GND |
| 2 | VCC+3V |
| 3 | CE |
| 4 | CSN |
| 55 | SCK |
| 6 | MOSI |
| 7 | MISO |
| 8 | IRQ |

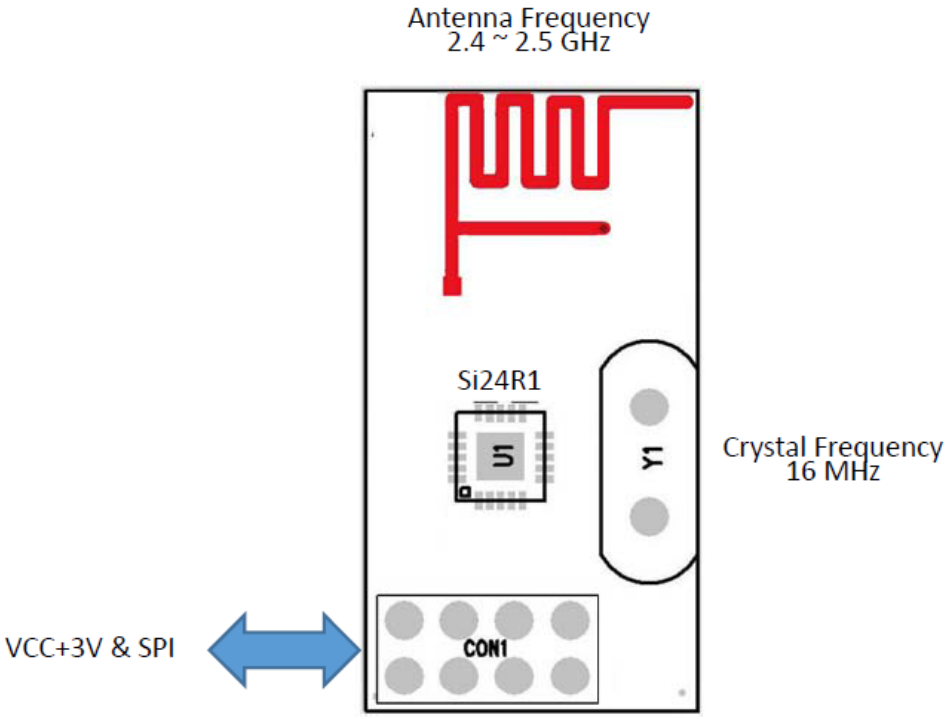
## 1-2. PIN Description

| PIN NO. | Name | I/O Type | Function Description | Other Function |
|---|---|---|---|---|
| 1 | GND | G | Power Supply (+1.9V - +3.6V DC) | |
| 2 | VCC+3V | P | Ground (0V) | |
| 3 | CE | I | Chip Enable Activates RX or TX mode | |
| 4 | CSN | I | Chip Select | |
| 5 | SCK | I | SPI Clock | |
| 6 | MOSI | I | SPI Slave Data Input | |
| 7 | MISO | O | SPI Slave Data Output, with tri-state option | |
| 8 | IRQ | O | Maskable interrupt pin. Active low | |

## 1-3. Chipset Block Diagram




## 1-4. Module Block Diagram



# 2、Electrical Specification

Conditions: VDD= +3V, VSS= 0V, $T_A$ = - 40ºC to + 85ºC

## 2-1. Absolute maximum ratings

**Note:** Exceeding one or more of the limiting values may cause permanent damage to AI00340.

| Operating conditions | Minimum | Maximum | Units |
|---|---|---|---|
| **Supply voltages** | | | |
| **VDD** | -0.3 | 3.6 | V |
| **VSS** | | 0 | V |
| **Input voltage** | | | |
| $V_I$ | -0.3 | 5.25 | V |
| **Output voltage** | | | |
| $V_O$ | **VSS** to **VDD** | **VSS** to **VDD** | |
| **Total Power Dissipation** | | | |
| $P_D$ ($T_A$=85°C) | | 60 | mW |
| **Temperatures** | | | |
| Operating Temperature | -40 | +85 | °C |
| Storage Temperature | -40 | +125 | °C |

## 2-2. Operation Condition

| Symbol | Parameter (condition) | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **VDD** | Supply voltage | | 1.9 | 3.0 | 3.6 | V |
| **VDD** | Supply voltage if input signals >3.6V | | 2.7 | 3.0 | 3.3 | V |
| TEMP | Operating Temperature | | -40 | +27 | +85 | ºC |

## 2-3. General Radio Characteristics

| Symbol | Parameter (condition) | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $f_{OP}$ | Operating frequency | a | 2400 | | 2525 | MHz |
| $PLL_{res}$ | PLL Programming resolution | | | 1 | | MHz |
| $f_{XTAL}$ | Crystal frequency | | | 16 | | MHz |
| $\triangle f_{1M}$ | Frequency deviation @ 1Mbps | | | ±160 | | kHz |
| $R_{GFSK}$ | Air Data rate | b | 1000 | | 2000 | kbps |
| $F_{CHAN-NEL\ 1M}$ | Non-overlapping channel spacing @ 1Mbps | c | | 1 | | MHz |

a. Usable band is determined by local regulations
b. Data rate in each burst on-air
c. The minimum channel spacing is 1Mhz

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## 2-4. Power consumption

| Symbol | Parameter (condition) | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| | **Idle modes** | | | | | |
| $I_{VDD\_PD}$ | Supply current in power down | | | 900 | | nA |
| $I_{VDD\_ST1}$ | Supply current in standby-I mode | a | | 22 | | µA |
| $I_{VDD\_ST2}$ | Supply current in standby-II mode | | | 320 | | µA |
| $I_{VDD\_SU}$ | Average current during 1.5ms crystal oscillator startup | | | 285 | | µA |
| | **Transmit** | | | | | |
| $I_{VDD\_TX0}$ | Supply current @ 0dBm output power | b | | 11.3 | | mA |
| $I_{VDD\_TX6}$ | Supply current @ -6dBm output power | b | | 9.0 | | mA |
| $I_{VDD\_TX12}$ | Supply current @ -12dBm output power | b | | 7.5 | | mA |
| $I_{VDD\_TX18}$ | Supply current @ -18dBm output power | b | | 7.0 | | mA |
| $I_{VDD\_AVG}$ | Average Supply current @ -6dBm output power, Enhanced ShockBurst™ | c | | 0.12 | | mA |
| $I_{VDD\_TXS}$ | Average current during TX settling | d | | 8.0 | | mA |
| | **Receive** | | | | | |
| $I_{VDD\_1M}$ | Supply current 1Mbps | | | 11.8 | | mA |
| $I_{VDD\_LC}$ | Supply current 1Mbps LNA low current | | | 11.1 | | mA |
| $I_{VDD\_RXS}$ | Average current during RX settling | e | | 8.4 | | mA |

a. Current is given for a 12pF crystal. Current when using external clock is dependent on signal swing.
b. Antenna load impedance = 15∧+j88∧.
c. Antenna load impedance = 15∧+j88∧. Average data rate 10kbps and full packets
d. Average current consumption for TX startup (130µs) and when changing mode from RX to TX (130µs).
e. Average current consumption for RX startup (130µs) and when changing mode from TX to RX (130µs).

## 2-5. Transmiter operation

| Symbol | Parameter (condition) | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $P_{RF}$ | Maximum Output Power | a | | 0 | +7 | dBm |
| $P_{RFC}$ | RF Power Control Range | | 16 | 18 | 20 | dB |
| $P_{RFCR}$ | RF Power Accuracy | | | | ±4 | dB |
| $P_{BW1}$ | 20dB Bandwidth for Modulated Carrier (1Mbps) | | | 900 | 1000 | kHz |
| $P_{RF1}$ | 1st Adjacent Channel Transmit Power 2MHz | | | | -20 | dBm |
| $P_{RF2}$ | 2nd Adjacent Channel Transmit Power 4MHz | | | | -50 | dBm |

a. Antenna load impedance = 15∧+j88∧

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## 2-6. Receiver operation

| Symbol | Parameter (condition) | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $RX_{max}$ | Maximum received signal at <0.1% BER | | | 0 | | dBm |
| $RX_{SENS}$ | Sensitivity at (0.1%BER) @1Mbps | | | -85 | | dBm |
| **RX selectivity according to ETSI EN 300 440-1 V1.3.1 (2001-09) page 27** | | | | | | |
| $C/I_{CO}$ | C/I Co-channel (@1Mbps) | a | | 9 | | dB |
| $C/I_{1ST}$ | $1^{st}$ Adjacent Channel Selectivity C/I 1MHz | | | 8 | | dB |
| $C/I_{2ND}$ | $2^{nd}$ Adjacent Channel Selectivity C/I 2MHz | | | -22 | | dB |
| $C/I_{3RD}$ | $3^{rd}$ Adjacent Channel Selectivity C/I 3MHz | | | -30 | | dB |
| **RX selectivity with AI00340 equal modulation on interfering signal** | | | | | | |
| $C/I_{CO}$ | C/I Co-channel (@1Mbps) | a | | 12 | | dB |
| $C/I_{1ST}$ | $1^{st}$ Adjacent Channel Selectivity C/I 1MHz | | | 8 | | dB |
| $C/I_{2ND}$ | $2^{nd}$ Adjacent Channel Selectivity C/I 2MHz | | | -21 | | dB |
| $C/I_{3RD}$ | $3^{rd}$ Adjacent Channel Selectivity C/I 3MHz | | | -30 | | dB |

a. Data rate is 1Mbps for the following C/I measurements

## 2-7. Crystal specifications

| Symbol | Parameter (condition) | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| Fxo | Crystal Frequency | | | 16 | | MHz |
| ⊗F | Tolerance | a b | | ±60 | | ppm |
| $C_0$ | Equivalent parallel capacitance | | | 1.5 | 7.0 | pF |
| $C_L$ | Load capacitance | | 8 | 12 | 16 | pF |
| ESR | Equivalent Series Resistance | | | | 100 | Λ |

a. Frequency accuracy including; tolerance at 25°C, temperature drift, aging and crystal loading.
b. Frequency regulations in certain regions sets tighter requirements to frequency tolerance (Ex: Japan and Korea max. +/- 50ppm)

## 2-8. DC characteristics

| Symbol | Parameter (condition) | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | HIGH level input voltage | | 0.7**VDD** | | 5.25[a] | V |
| $V_{IL}$ | LOW level input voltage | | **VSS** | | 0.3**VDD** | V |

a. If the input signal >3.6V, the **VDD** of the AI00340 must be between 2.7V and 3.3V (3.0V±10%)

| Symbol | Parameter (condition) | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | HIGH level output voltage ($I_{OH}$=-0.25mA) | | **VDD** -0.3 | | **VDD** | V |
| $V_{OL}$ | LOW level output voltage ($I_{OL}$=0.25mA) | | | | 0.3 | V |

## 2-9. Power on reset

| Symbol | Parameter (condition) | Notes | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $T_{PUP}$ | Power ramp up time | a | | | 100 | ms |
| $T_{POR}$ | Power on reset | b | 1.6 | 5.3 | 10.3 | ms |

a. From 0V to 1.9V
b. Measured when the **VDD** reaches 1.9V to when the reset finishes

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# 3、Radio Control

This chapter describes the different modes the AI00340 radio transceiver can operate in and the parameters used to control the radio.

The AI00340 has a built-in state machine that controls the transitions between the different operating modes of the chip. The state machine takes input from user defined register values and internal signals.

## 3-1. Operational Modes

The AI00340 can be configured in four main modes of operation. This section describes these modes.

### 3-1-1. State diagram

The state diagram Figure shows the modes the AI00340 can operate in and how they are accessed. The AI00340 is undefined until the VDDbecomes 1.9V or higher. When this happens AI00340 enters the Power on reset state where it remains in reset until it enters the Power Down mode. Even when the AI00340 enters Power Down mode the MCU can control the chip through the SPI and the Chip Enable (CE) pin Three types of states are used in the state diagram. “Recommended operating mode” is a state that is used during normal operation. “Possible operating mode” is a state that is allowed to use, but it is not used during normal operation. “Transition state” is a time limited state used during start up of the oscillator and settling of the PLL.

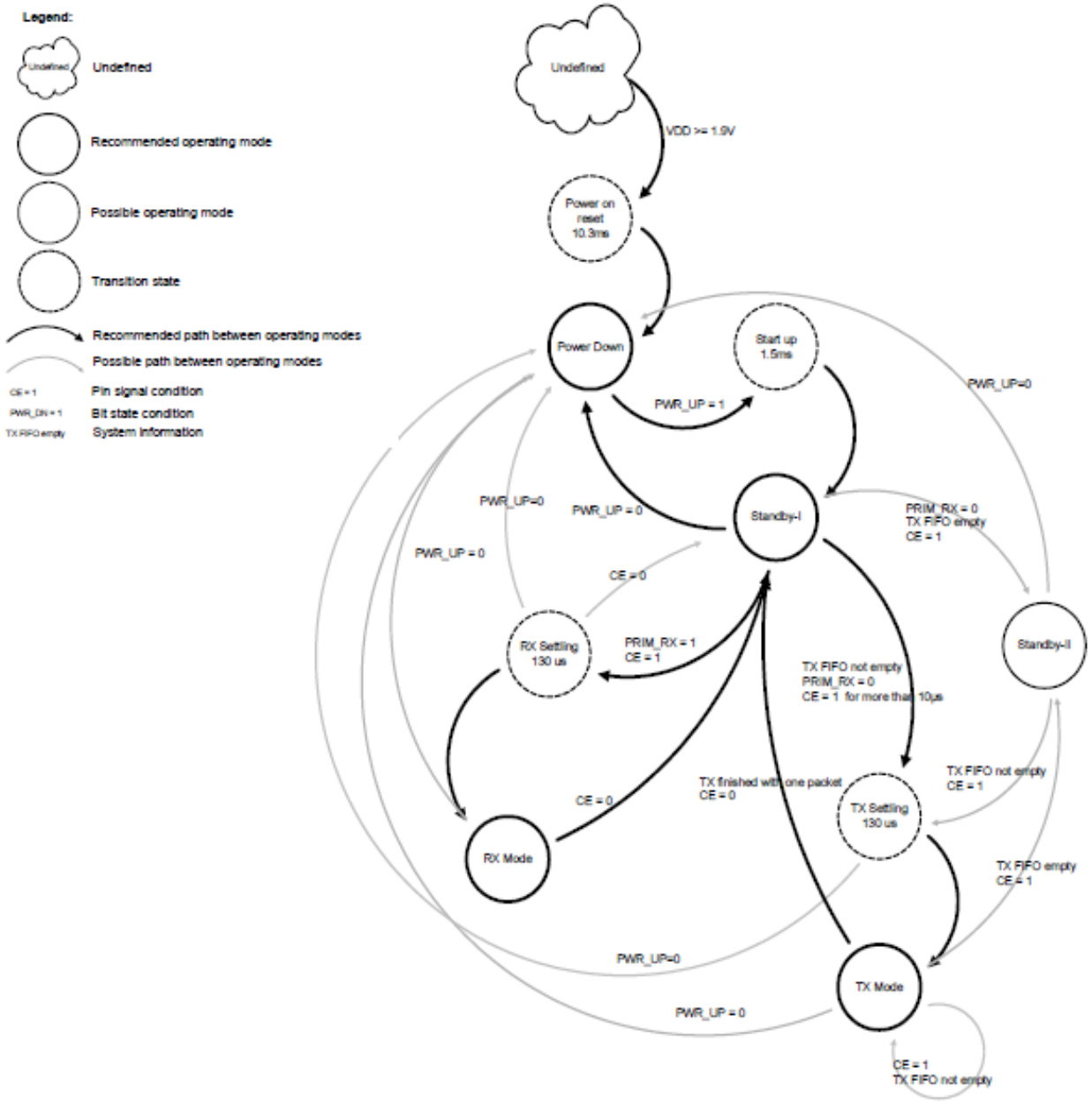


*Figure. Radio control state diagram*

### 3-1-2. Power Down Mode

In power down mode AI00340 is disabled with minimal current consumption. In power down mode all the register values available from the SPI are maintained and the SPI can be activated. Power down mode is entered by setting the PWR_UPbit in the CONFIGregister low.

### 3-1-3. Standby Modes

By settting the PWR_UP bit in the CONFIG register to 1, the device enters standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start up times. In this mode part of the crystal oscillator is active. This is the mode the AI00340 returns to from TX or RX mode when **CE** is set low.

In standby-II mode extra clock buffers are active compared to standby-I mode and much more current is used compared to standby-I mode. Standby-II occurs when **CE**is held high on

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a PTX device with empty TX FIFO. If a new packet is uploaded to the TX FIFO, the PLL starts and the packet is transmitted.

The register values are maintained during standby modes and the SPI may be activated.

### 3-1-4. RX mode

The RX mode is an active mode where the AI00340 radio is a receiver. To enter this mode, the AI00340 must have the PWR_UP bit set high, PRIM_RXbit set high and the **CE**pin set high.

In this mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the baseband protocol engine. The baseband protocol engine constantly searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFO. If the RX FIFO is full, the received packet is discarded.

The AI00340 remains in RX mode until the MCU configures it to standby-I mode or power down mode. If the automatic protocol features (Enhanced ShockBurst™) in the baseband protocol engine are enabled, the AI00340 can enter other modes in order to execute the protocol.

In RX mode a carrier detect signal is avaliable. The carrier detect is a signal that is set high when a RF sig- nal is detected inside the receiving frequency channel. The signal must be FSK modulated for a secure detection. Other signals can also be detected. The Carrier Detect (CD) is set high when an RF signal is detected in RX mode, otherwise CDis low. The internal CDsignal is filtered before presented to CDregister. The RF signal must be present for at least 128μs before the CDis set high.

### 3-1-5. TX mode

The TX mode is an active mode where the AI00340 transmits a packet. To enter this mode, the AI00340 must have the PWR_UP bit set high, PRIM_RXbit set low, a payload in the TX FIFO and, a high pulse on the **CE**for more than 10μs.

The AI00340 stays in TX mode until it finishes transmitting a current packet. If **CE**= 0 AI00340 returns to standby-I mode. If **CE**= 1, the next action is determined by the status of the TX FIFO. If the TX FIFO is not empty the AI00340 remains in TX mode, transmitting the next packet. If the TX FIFO is empty the AI00340 goes into standby-II mode. The AI00340 transmitter PLL operates in open loop when in TX mode. It is important to never keep the AI00340 in TX mode for more than 4ms at a time. If the auto retransmit is enabled, the AI00340 is never in TX mode long enough to disobey this rule.

### 3-1-6. Operational modes configuration

The following table describes how to configure the operational modes.

| Mode | PWR_UP register | PRIM_RX register | CE | FIFO state |
|---|---|---|---|---|
| RX mode | 1 | 1 | 1 | - |
| TX mode | 1 | 0 | 1 | Data in TX FIFO. Will empty all levels in TX FIFO[a]. |

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| | | | | |
|---|---|---|---|---|
| TX mode | 1 | 0 | minimum 10μs high pulse | Data in TX FIFO. Will empty one level in TX FIFO[b]. |
| Standby-II | 1 | 0 | 1 | TX FIFO empty |
| Standby-I | 1 | - | 0 | No ongoing packet transmission |
| Power Down | 0 | - | - | - |

a. In this operating mode if the **CE** is held high the TX FIFO is emptied and all necessary ACK and possible retransmits are carried out. The transmission continues as long as the TX FIFO is refilled. If the TX FIFO is empty when the **CE** is still high, AI00340 enters standby-II mode. In this mode the trans- mission of a packet is started as soon as the **CSN** is set high after a upload (UL) of a packet to TX FIFO.

b. This operating mode pulses the **CE** high for at least 10μs. This allows one packet to be transmitted. This is the normal operating mode. After the packet is transmitter, the AI00340 enters standby-I mode.

### 3-1-7. Timing Information

The timing information in this section is related to the transitions between modes and the timing for the **CE** pin. The transition from TX mode to RX mode or vice versa is the same as the transition from standby-I to TX mode or RX mode,Tstby2a.

| Name | AI00340 | Max. | Min. | Comments |
|---|---|---|---|---|
| Tpd2stby | Power Down ➔ Standby mode | 1.5ms | | Internal crystal oscillator |
| Tpd2stby | Power Down ➔ Standby mode | 150μs | | With external clock |
| Tstby2a | Standby modes ➔ TX/RX mode | 130μs | | |
| Thce | Minimum **CE** high | | 10μs | |
| Tpece2csn | Delay from **CE** pos. edge to **CSN** low | | 4μs | |

When AI00340 is in power down mode it must settle for 1.5ms before it can enter the TX or RX modes. If an *external clock* is used this delay is reduced to 150μs. The settling time must be controlled by the MCU.

**Note:** The register value is lost if **VDD**is turned off. In this case, AI00340 must be configured before entering the TX or RX modes.

## 3-2. Air data rate

The air data rate is the modulated signaling rate the AI00340 uses when transmitting and receiving data.

The air data rate up to 1Mbps gives better receiver sensitivity.

The air data rate is set by the RF_DR bit in the RF_SETUPregister.

## 3-3. RF channel frequency

The RF channel frequency determines the center of the channel used by the AI00340. The channel occupies a bandwidth of 1MHz at 1Mbps from 2.402GHz to 2.480GHz. The resolution of the RF channel frequency setting is 1MHz.

The RF channel frequency is set by the RF_CHregister according to the following formula: $F_0$= 2400 + RF_CH[MHz]
A transmitter and a receiver must be programmed with the same RF channel frequency to be able to communicate with each other.

## 3-4. PA control

The PA control is used to set the output power from the AI00340 power amplifier (PA). In TX mode PA control has four programmable steps.
The PA control is set by the RF_PWRbits in the RF_SETUPregister.

| SPI RF-SETUP (RF_PWR) | RF output power |
|---|---|
| 111 | 7dBm |
| 110 | 4dBm |
| 101 | 1dBm |
| 100 | 0dBm |
| 011 | -1dBm |
| 010 | -4dBm |
| 001 | -6dBm |
| 000 | -12dBm |

## 3-5. LNA gain

The gain in the Low Noise Amplifier (LNA) in the AI00340 receiver is controlled by the LNA gain setting. The LNA gain makes it possible to reduce the current consumption in RX mode with 0.8mA at the cost of 1.5dB reduction in receiver sensitivity.

The LNA gain has two steps and is set by the LNA_HCURRbit in the RF_SETUPregister.

## 3-6. RX/TX control

The RX/TX control is set by PRIM_RXbit in the CONFIGregister and sets the AI00340 in transmit/ receive.

# 4. Enhanced ShockBurst™

Enhanced ShockBurst™ is a packet based data link layer. It features automatic packet assembly and tim- ing, automatic acknowledgement and re-transmissions of packets. Enhanced ShockBurst™ enables the implementation of ultra low power, high performance communication with low cost host microcontrollers. The features enable significant improvements of power efficiency for bi-directional and uni-directional sys- tems, without adding complexity on the host controller side.

## 4-1. Features

The main features of Enhanced ShockBurst™ are:

- 1 to 32 bytes dynamic payload length
- Automatic packet handling
- Auto packet transaction handling
  - , Auto Acknowledgement
  - , Auto retransmit
- 6 data pipe MultiCeiver™ for 1:6 star networks

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## 4-2. Enhanced Shockburst™ packet format

The format of the Enhanced ShockBurst™ packet is described in this chapter. The Enhanced ShockBurst™ packet contains a preamble field, address field, packet control field, payload field and a CRC field.

| Preamble 1 byte | Address 3-5 byte | Packet Control Field 9 bit | Payload 0 - 32 byte | CRC 1-2 byte |
|---|---|---|---|---|

## 4-3. Automatic packet handling

Enhanced ShockBurst™ uses ShockBurst™ for automatic packet handling. The functions are static and dynamic payload length, automatic packet assembly, automatic packet validation and automatic packet disassembly.

## 4-4. Automatic packet transaction handling

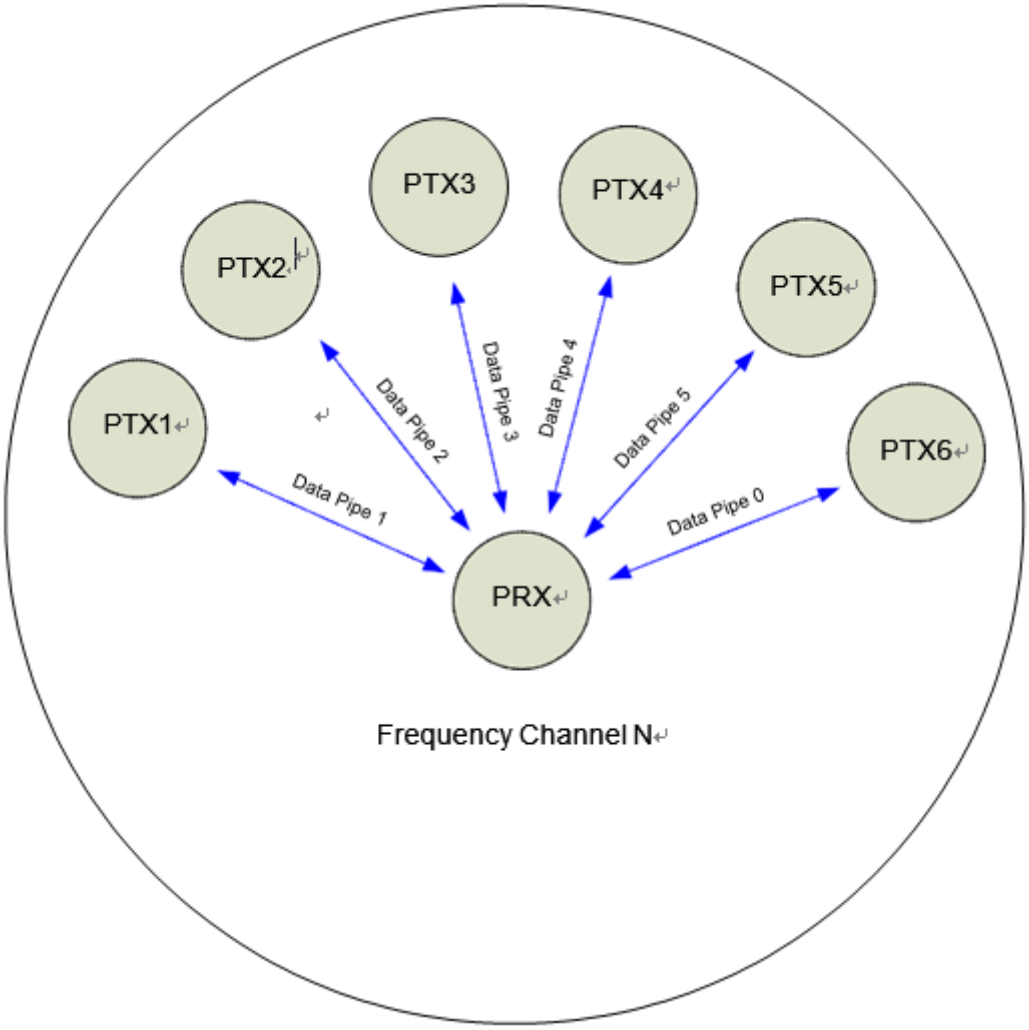
Enhanced ShockBurst™ features two functions for automatic packet transaction handling; auto acknowledgement and auto re-transmit.

## 4-5. Enhanced ShockBurst flowcharts

This section shows flowcharts for PTX and PRX operation in Enhanced ShockBurst™. ShockBurst™ operation is marked with a dashed square in the flow charts.

## 4-6. Multiceiver

Multiceiver is a feature used in RX mode that contains a set of 6 parallel data pipes with unique addresses. A data pipe is a logical channel in the physical RF channel. Each data pipe has its own physical address decoding in the AI00340.




AI00340 configured as PRX (primary receiver) can receive data addressed to six different data pipes in one frequency channel as shown in Figure 10. Each data pipe has its own unique address and can be con- figured for individual behavior.

Up to six AI00340s configured as PTX can communicate with one AI00340 configured as PRX. All data pipe addresses are searched for simultaneously. Only one data pipe can receive a packet at a time. All data pipes can perform Enhanced ShockBurst™ functionality.

The following settings are common to all data pipes:

- CRC enabled/disabled (CRC always enabled when Enhanced ShockBurst™ is enabled)
- CRC encoding scheme
- RX address width
- Frequency channel
- Air data rate
- LNA gain

The data pipes are enabled with the bits in the EN_RXADDRregister. By default only data pipe 0 and 1 are enabled.

Each data pipe address is configured in the RX_ADDR_PXregisters.

**Note:** Always ensure that none of the data pipes have the same address.

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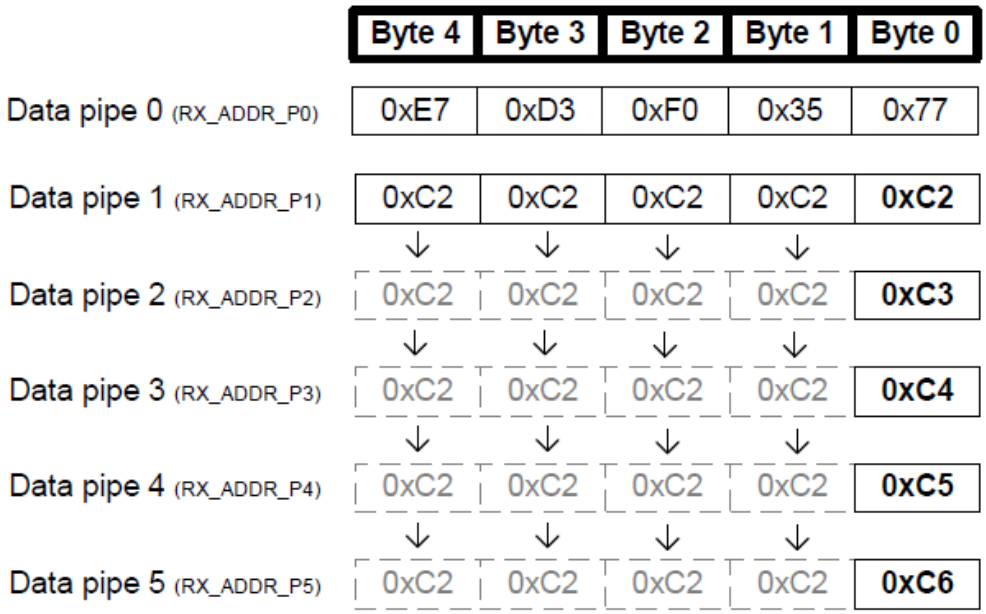
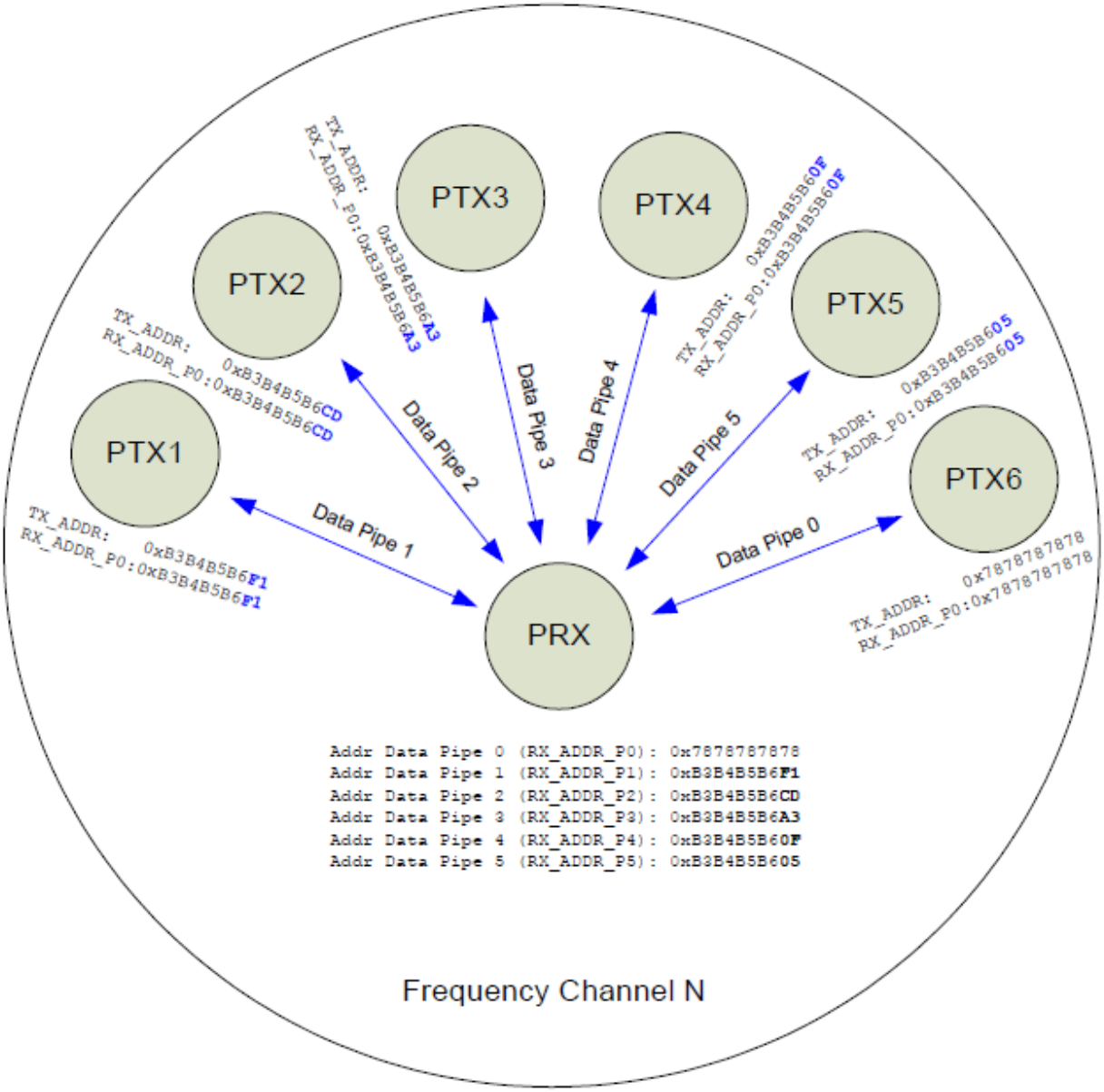
Each pipe can have up to 5 byte configurable address. Data pipe 0 has a unique 5 byte

address. Data pipes 1-5 share the 4 most significant address bytes. The LSByte must be unique for all 6 pipes. The Figure is an example of how data pipes 0-5 are addressed.



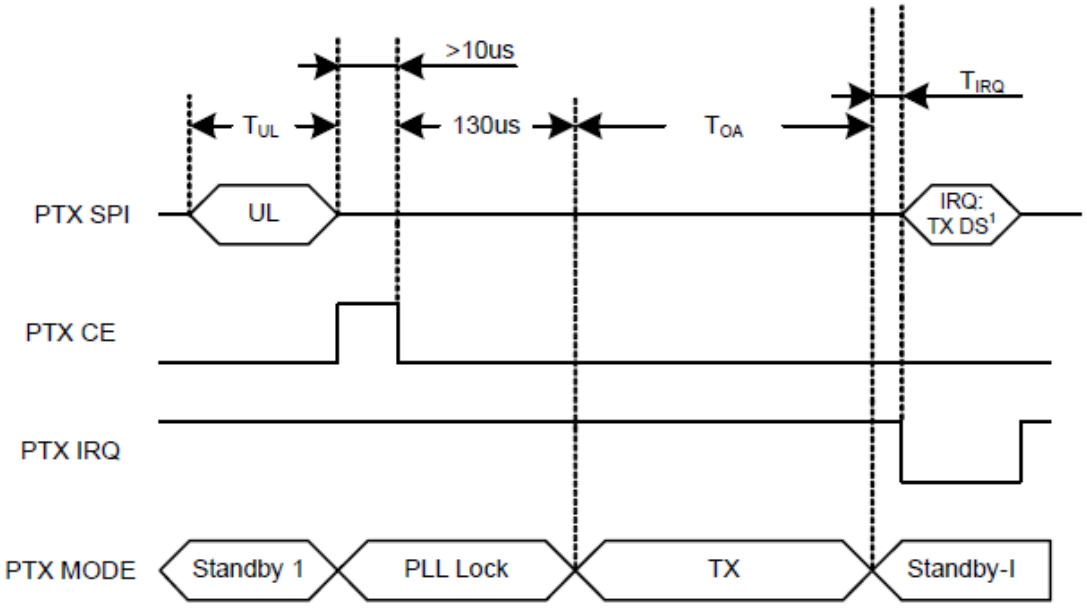

The PRX, using multiceiver and Enhanced ShockBurst™, receives packets from more than one PTX. To ensure that the ACK packet from the PRX is transmitted to the correct PTX, the PRX takes the data pipe address where it received the packet and uses it as the TX address when transmitting the ACK packet. Figure 12. is an example of how address configuration could be for the PRX and PTX. On the PRX the RX_ADDR_Pn, defined as the pipe address, must be unique. On the PTX the TX_ADDRmust be the same as the RX_ADDR_P0and as the pipe address for the designated pipe.




No other data pipe can receive data until a complete packet is received by a data pipe that has detected its address. When multiple PTXs are transmitting to a PRX, the ARD can be used to skew the auto retransmission so that they only block each other once.

## 4-7. Enhanced ShockBurst™ timing

This section describes the timing sequence of Enhanced ShockBurst™ and how all modes are initiated and operated. The Enhanced ShockBurst™ timing is controlled through the Data and Control interface. The AI00340 can be set to static modes or autonomous modes where the internal state machine con- trols the events. Each autonomous mode/sequence is ended with an interrupt at the **IRQ**pin. All the interrupts are indicated as IRQ events in the timing diagrams.

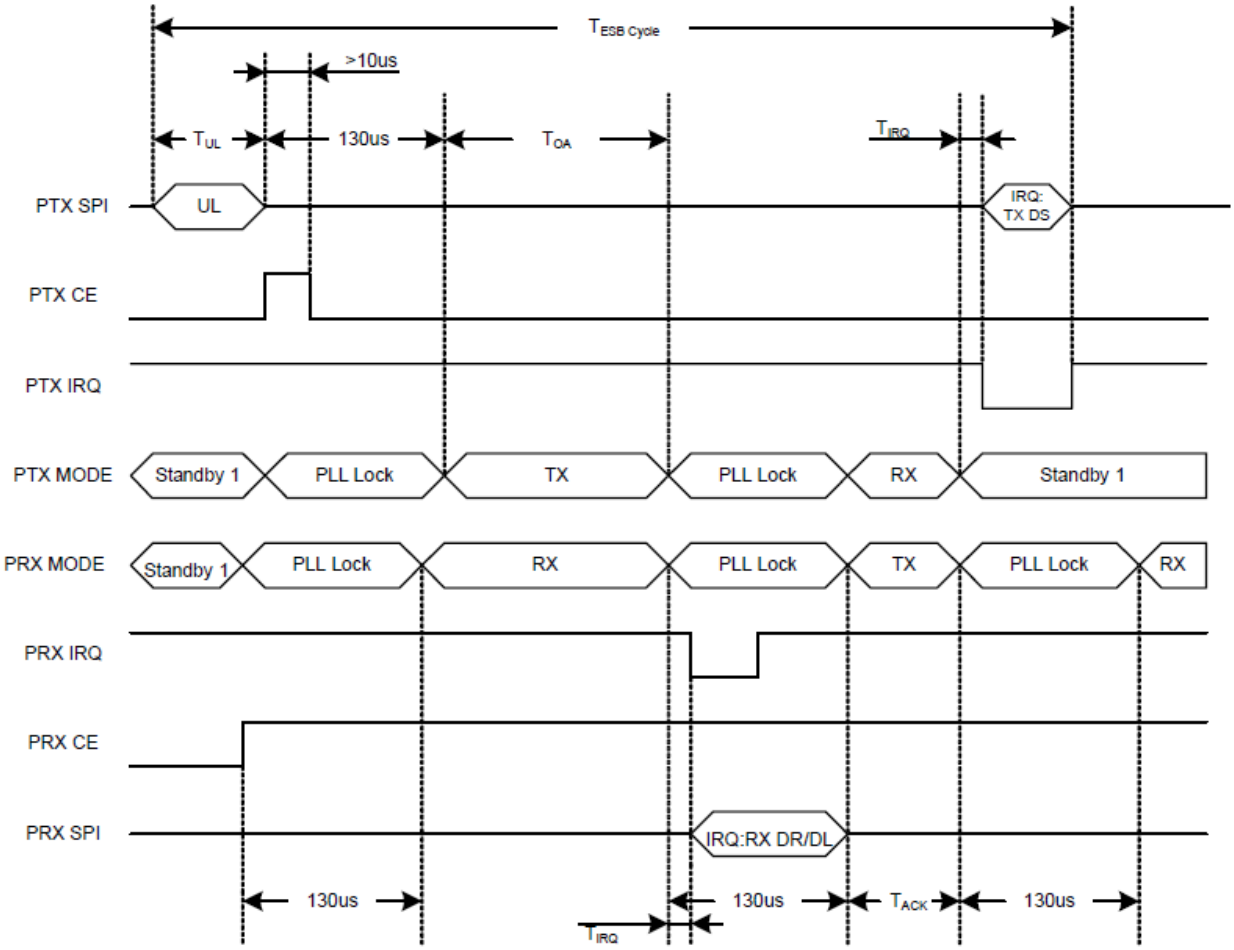



1 IRQ if No Ack is on.

$T_{IRQ}$ = 8.2ηs @ 1Mbps, $T_{IRQ}$ = 6.0ηs @ 2Mbps

The following equations calculate various timing measurements:

| Symbol | Description | Equation |
|---|---|---|
| $T_{OA}$ | Time on-air | $T_{OA} = \frac{packet\ length}{air\ data\ rate} = \frac{8\left[\frac{bit}{byte}\right]\cdot\left(1[byte]_{preamble}+3,4\ or\ 5[bytes]_{address}+N[bytes]_{payload}+1\ or\ 2[bytes]_{CRC}\right)+9[bit]_{packet\ control\ field}}{air\ data\ rate\left[\frac{bit}{s}\right]}$ |
| $T_{ACK}$ | Time on-air Ack | $T_{ACK} = \frac{packet\ length}{air\ data\ rate} = \frac{8\left[\frac{bit}{byte}\right]\cdot\left(1[byte]_{preamble}+3,4\ or\ 5[bytes]_{address}+N[bytes]_{payload}+1\ or\ 2[bytes]_{CRC}\right)+9[bit]_{packet\ control\ field}}{air\ data\ rate\left[\frac{bit}{s}\right]}$ |
| $T_{UL}$ | Time Upload | $T_{UL} = \frac{payload\ length}{SPI\ data\ rate} = \frac{8\left[\frac{bit}{byte}\right]\cdot N[bytes]_{payload}}{SPI\ data\ rate\left[\frac{bit}{s}\right]}$ |
| $T_{ESB}$ | Time Enhanced Shock-Burst™ cycle | $T_{ESB} = T_{UL} + 2\cdot T_{stby2a} + T_{ACK} + T_{IRQ}$ |




In Figure the transmission and acknowledgement of a packet are shown. The PRX device is turned into RX mode (**CE**=1), and the PTX device is set to TX mode (**CE**=1 for minimum 10 s). After 130 s the trans- mission starts and finishes after the elapse of $T_{OA}$.

When the transmission ends the PTX device automatically switches to RX mode to wait for the ACK packet from the PRX device. After the PTX device receives the ACK packet it responds with an interrupt to the MCU. When the PRX device receives the packet it responds with an interrupt to the MCU.

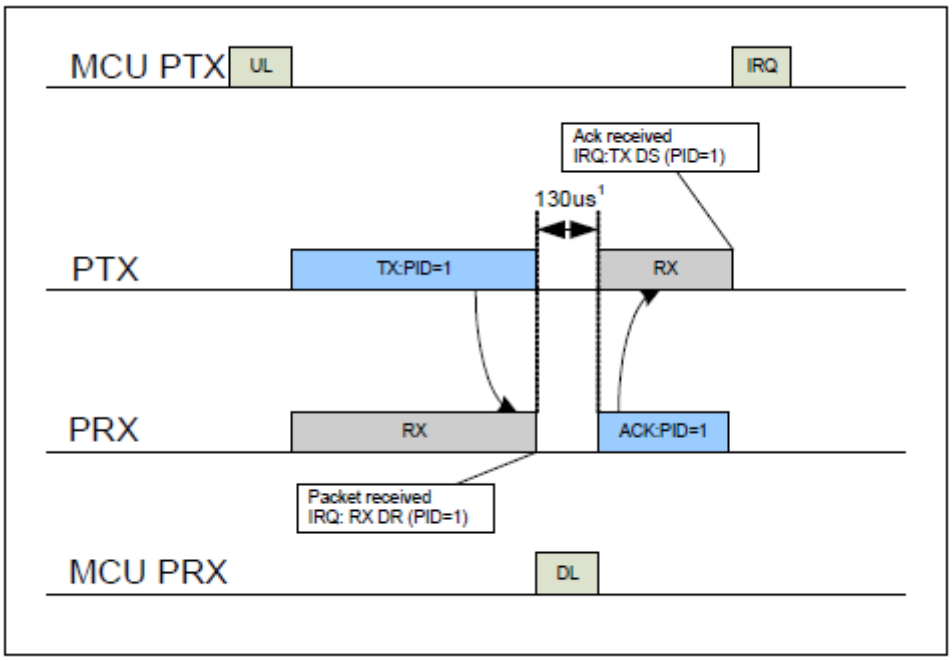
## 4-8. Enhanced ShockBurst™ transaction diagram

This section describes how several scenarios for the Enhanced ShockBurst™ automatic transaction handling. The call outs in this section's figures indicate the IRQs and other events. For MCU activity the event may be placed at a different timeframe.

**Note:** The figures in this section indicate the earliest possible download (DL) of the packet to the MCU and the latest possible upload (UL) of payload to the transmitter.

### 4-8-1. Single transaction with ACK packet and interrupts

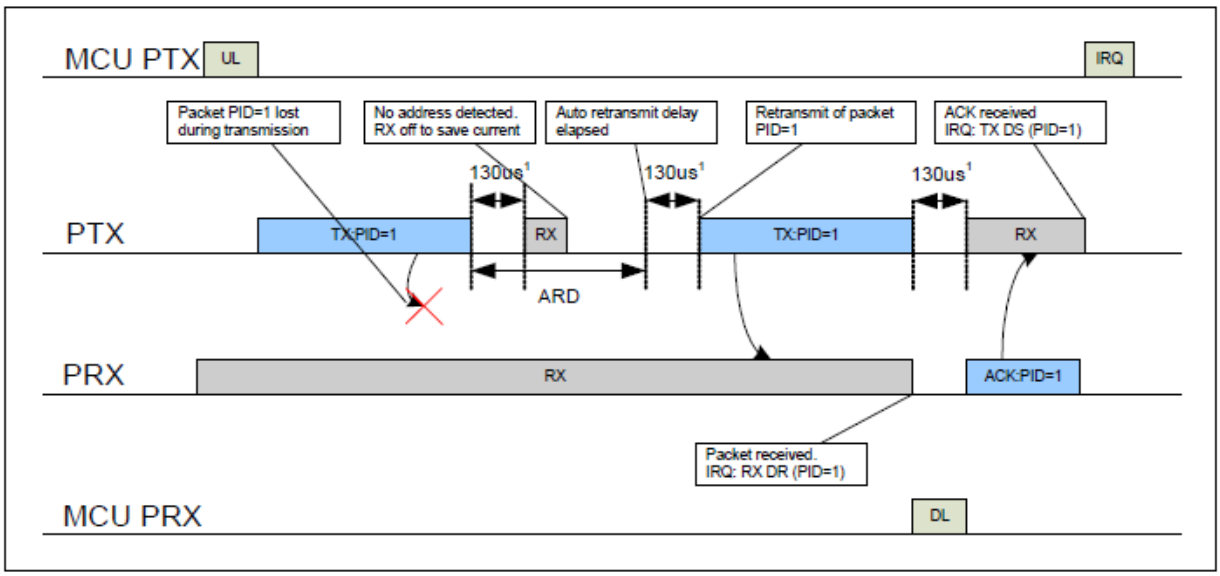
In Figure the basic auto acknowledgement is shown. After the packet is transmitted by the PTX and received by the PRX the ACK packet is transmitted from the PRX to the PTX. The RX_DR IRQ is asserted after the packet is received by the PRX, whereas the TX_DS IRQ is asserted when the packet is acknowledged and the ACK packet is received by the PTX.




1 Radio Turn Around Delay

### 4-8-2. Single transaction with a lost packet

In Figure is a scenario where a retransmission is needed due to loss of the first packet transmit. After the packet is transmitted, the PTX enters RX mode to receive the ACK packet. After the first transmission, the PTX waits a specified time for the ACK packet, if it is not in the specific time slot the PTX retransmits the packet.




1 Radio Turn Around Delay

When an address is detected the PTX stays in RX mode until the packet is received. When the retransmitted packet is received by the PRX, the RX_DR IRQ is asserted and an ACK is transmitted back to the PTX. When the ACK is received by the PTX, the TX_DS IRQ is asserted.

### 4-8-3. Single transaction with a lost ACK packet

In Figure is a scenario where a retransmission is needed after a loss of the ACK packet. The corresponding interrupts are also indicated.

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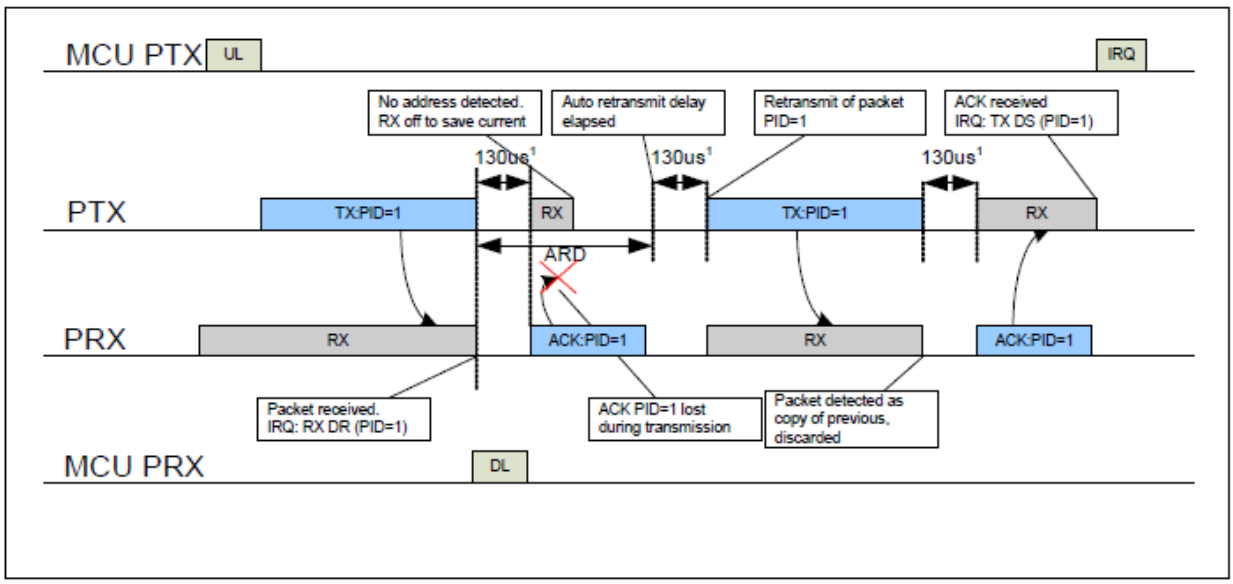
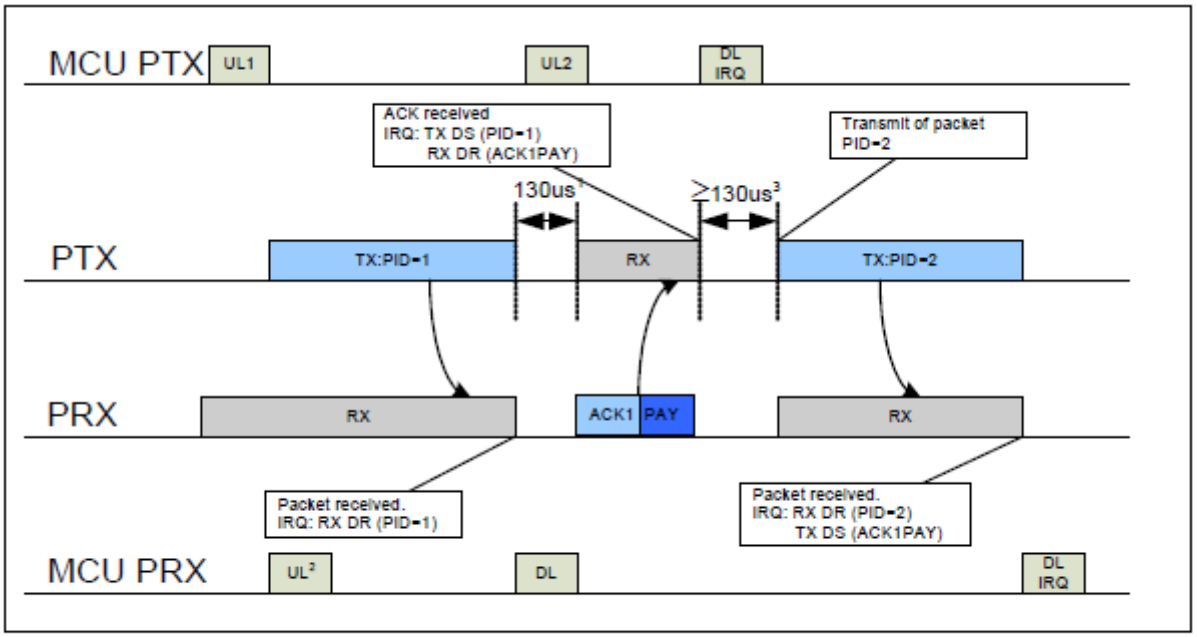



1 Radio Turn Around Delay

### 4-8-4. Single transaction with ACK payload packet

In Figure is a scenario of the basic auto acknowledgement with payload. After the packet is transmitted by the PTX and received by the PRX the ACK packet with payload is transmitted from the PRX to the PTX. The RX_DRIRQ is asserted after the packet is received by the PRX, whereas on the PTX side the TX_DS IRQ is asserted when the ACK packet is received by the PTX. On the PRX side, the TX_DSIRQ for the ACK packet payload is asserted after a new packet from PTX is received. The position of the IRQ in Figure shows where the MCU can respond to the interrupt.

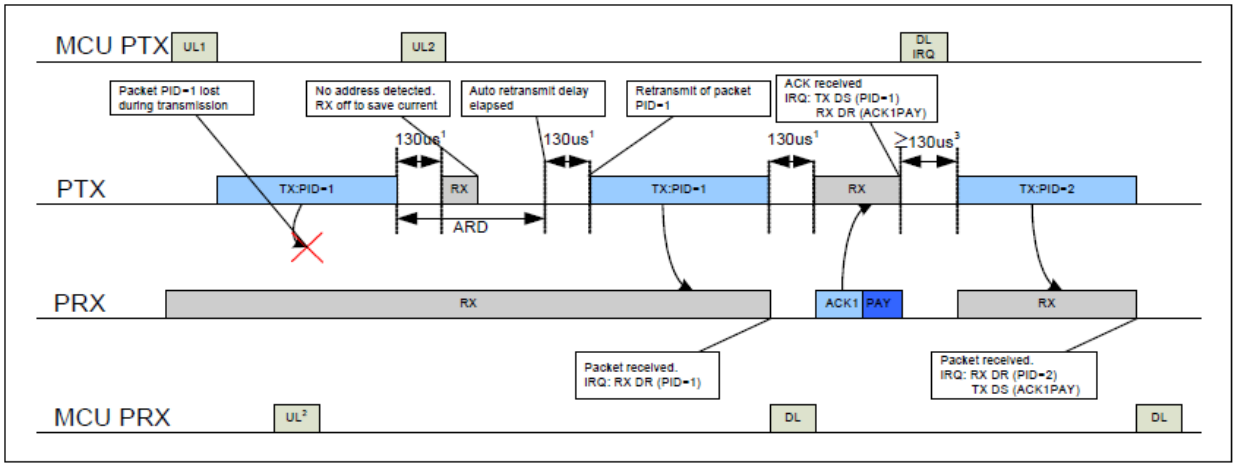



1 Radio Turn Around Delay
2 Uploading Paylod for Ack Packet
3 Delay defined by MCU on PTX side, ≥ 130us

### 4-8-5. Single transaction with ACK payload packet and lost packet

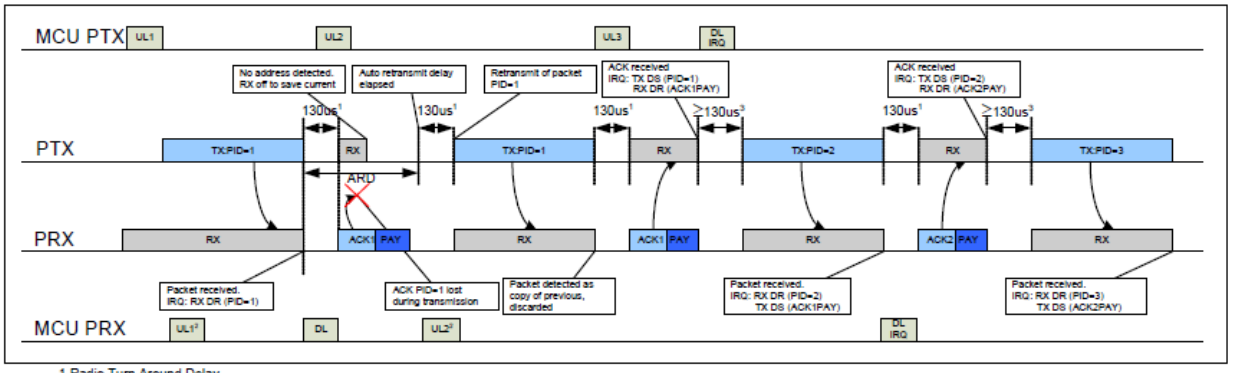
In Figure is a scenario where the first packet is lost and a retransmission is needed before the RX_DRIRQ on the PRX side is asserted. For the PTX both the TX_DSand RX_DRIRQ are asserted after the ACK packet is received. After the second packet (PID=2) is received

on the PRX side both the RX_DR(PID=2) and TX_DS(ACK packet payload) IRQ are asserted.




1 Radio Turn Around Delay
2 Uploading Paylod for Ack Packet
3 Delay defined by MCU on PTX side, ≥ 130us

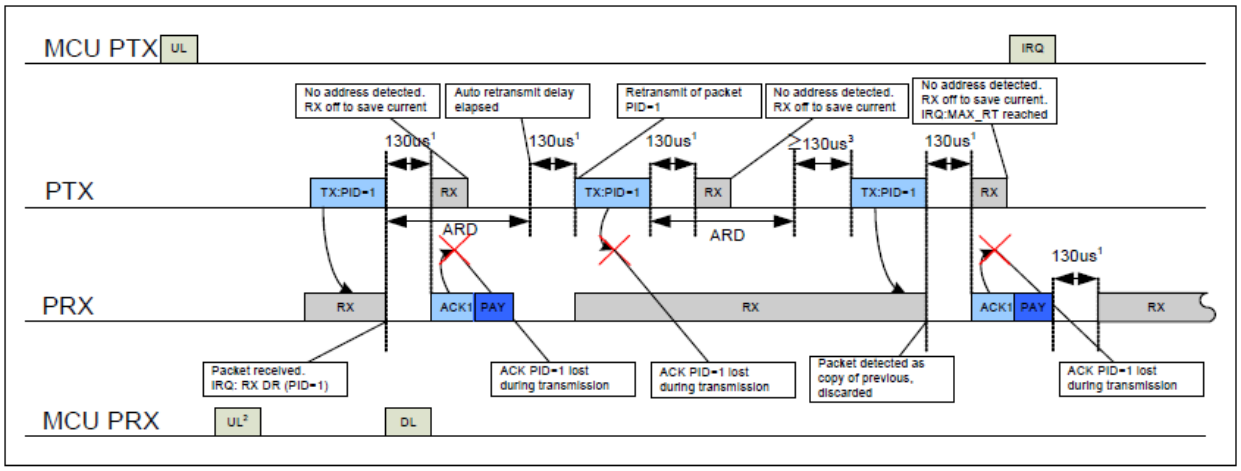
## 4-8-6. Two transactions with ACK payload packet and the first ACK packet lost.




1 Radio Turn Around Delay
2 Uploading Paylod for Ack Packet
3 Delay defined by MCU on PTX side, ≥ 130us

In Figure the ACK packet is lost and a retransmission is needed before the TX_DSIRQ is asserted, but the RX_DRIRQ is asserted immediately. The retransmission of the packet (PID=1) results in a discarded packet. For the PTX both the TX_DSand RX_DRIRQ are asserted after the second transmission of ACK, which is received. After the second packet (PID=2) is received on the PRX both the RX_DR(PID=2) and TX_DS(ACK1PAY) IRQ is asserted. The callouts explains the different events and interrupts.

## 4-8-7. Two transactions where max retransmissions is reached




1 Radio Turn Around Delay
2 Uploading Paylod for Ack Packet
3 Delay defined by MCU on PTX side, ≥ 130us

If the auto retransmit counter (ARC_CNT) exceeds the programmed maximum limit (ARC), the MAX_RTIRQ is asserted. In Figure the packet transmission ends with a MAX_RTIRQ. The payload in TX FIFO is NOT removed and the MCU decides the next step in the protocol. A toggle of the **CE**starts a new sequence of transmitting the same packet. The payload can be removed from the TX FIFO using the FLUSH_TXcommand.

# 5、SPI (Serial peripheral interface) —Data and Control

The data and control interface gives you access to all the features in the AI00340. The data and control interface consists of the following six 5Volt tolerant digital signals:

- **IRQ**(this signal is active low and is controlled by three maskable interrupt sources)
- **CE**(this signal is active high and is used to activate the chip in RX or TX mode)
- **CSN**(SPI signal)
- **SCK**(SPI signal)
- **MOSI**(SPI signal)
- **MISO**(SPI signal)

You can use the SPI to activate the AI00340 data FIFOs or the register map by 1 byte SPI commands during all modes of operation.

## 5-1. Features

- Special SPI commands for quick access to the most frequently used features
- 0-8Mbps 4-wire SPI serial interface
- 8 bit command set
- Easily configurable register map
- Full three level FIFO for both TX and RX direction

## 5-2. Functional description

The SPI is a standard SPI with a maximum data rate of 8Mbps.

## 5-3. SPI operation

This chapter describes the SPI commands and SPI timing.

### 5-3-1. SPI Commands

Every new command must be started by a high to low transi- tion on **CSN**.

In parallel to the SPI command word applied on the **MOSI**pin, the STATUSregister is shifted serially out on the **MISO**pin.

The serial shifting SPI commands is in the following format:

<**Command word**: MSBit to LSBit (one byte)>

<**Data bytes**: LSByte to MSByte, MSBit in each byte first>

| Command name | Command word (binary) | # Data bytes | Operation |
|---|---|---|---|
| R_REGISTER | 000A AAAA | 1 to 5 LSByte first | Read command and status registers. AAAAA = 5 bit Register Map Address |
| W_REGISTER | 001A AAAA | 1 to 5 LSByte first | Write command and status registers. AAAAA = 5 bit Register Map Address<br>Executable in power down or standby modes only. |
| R_RX_PAYLOAD | 0110 0001 | 1 to 32 LSByte first | Read RX-payload: 1 – 32 bytes. A read operation always starts at byte 0. Payload is deleted from FIFO after it is read. Used in RX mode. |
| W_TX_PAYLOAD | 1010 0000 | 1 to 32 LSByte first | Write TX-payload: 1 – 32 bytes. A write operation always starts at byte 0 used in TX payload. |
| FLUSH_TX | 1110 0001 | 0 | Flush TX FIFO, used in TX mode |
| FLUSH_RX | 1110 0010 | 0 | Flush RX FIFO, used in RX mode<br>Should not be executed during transmission of acknowledge, that is, acknowledge package will not be completed. |
| REUSE_TX_PL | 1110 0011 | 0 | Used for a PTX device<br>Reuse last transmitted payload. Packets are repeatedly retransmitted as long as **CE** is high. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX payload reuse must not be activated or deacti- vated during package transmission |
| ACTIVATE | 0101 0000 | 1 | This write command followed by data 0x73 acti- vates the following features:<br>• R_RX_PL_WID<br>• W_ACK_PAYLOAD<br>• W_TX_PAYLOAD_NOACK<br>A new ACTIVATE command with the same data deactivates them again. *This is executable in power down or stand by modes only.*<br><br>The R_RX_PL_WID, W_ACK_PAYLOAD, and W_TX_PAYLOAD_NOACK features registers are initially in a deactivated state; a write has no effect, a read only results in zeros on **MISO**. To activate these registers, use the ACTIVATE com- mand followed by data 0x73. Then they can be accessed as any other register in AI00340. Use the same command and data to deactivate the registers again. |
| R_RX_PL_WID[a] | 0110 0000 | | Read RX-payload width for the top R_RX_PAYLOAD in the RX FIFO. |

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| | | | |
|---|---|---|---|
| W_ACK_PAYLOAD[a] | 1010 1PPP | 1 to 32 LSByte first | Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled using first in - first out principle. Write payload: 1– 32 bytes. A write operation always starts at byte 0. |

a. To activate this feature use the ACTIVATE SPI command followed by data 0x73. The corresponding bits in the FEATURE register have to be set.

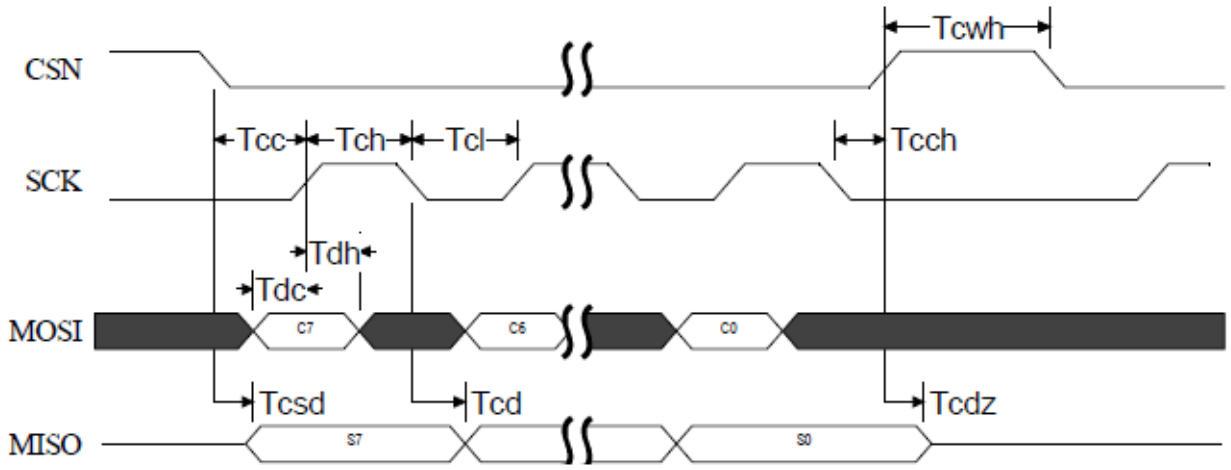
The W_REGISTERand R_REGISTERcommands can operate on single or multi-byte registers. When accessing multi-byte registers you read or write to the MSBit of LSByte first. You can terminate the writing before all bytes in a multi-byte register are written, leaving the unwritten MSByte(s) unchanged. For exam- ple, the LSByte of RX_ADDR_P0can be modified by writing only one byte to the RX_ADDR_P0register. The content of the status register is always read to **MISO**after a high to low transition on **CSN**.

**Note:** The 3 bit pipe information in the STATUSregister is updated during the **IRQ**pin high to low transition. If the STATUSregister is read during an **IRQ**pin high to low transition, the pipe information is unreliable.

### 5-3-2. SPI timing

In Tables and Figures shown SPI operation and timing. AI00340 must be in one of the standby modes or in power down mode before writing to the configuration registers.

| Abbreviation | Description |
|---|---|
| Cn | SPI command bit |
| Sn | STATUS register bit |
| Dn | Data Bit (**Note:** LSByte to MSByte, MSBit in each byte first) |




| Symbol | Parameters | Min | Max | Units |
|---|---|---|---|---|
| Tdc | Data to **SCK** Setup | 2 | | ns |
| Tdh | **SCK** to Data Hold | 2 | | ns |
| Tcsd | **CSN** to Data Valid | | 38 | ns |
| Tcd | **SCK** to Data Valid | | 55 | ns |
| Tcl | **SCK** Low Time | 40 | | ns |
| Tch | **SCK** High Time | 40 | | ns |
| Fsck | **SCK** Frequency | 0 | 8 | MHz |
| Tr,Tf | **SCK** Rise and Fall | | 100 | ns |
| Tcc | **CSN** to **SCK** Setup | 2 | | ns |
| Tcch | **SCK** to **CSN** Hold | 2 | | ns |
| Tcwh | **CSN** Inactive time | 50 | | ns |
| Tcdz | **CSN** to Output High Z | | 38 | ns |

| Symbol | Parameters | Min | Max | Units |
|---|---|---|---|---|
| Tdc | Data to **SCK** Setup | 2 | | ns |
| Tdh | **SCK** to Data Hold | 2 | | ns |
| Tcsd | **CSN** to Data Valid | | 42 | ns |
| Tcd | **SCK** to Data Valid | | 58 | ns |
| Tcl | **SCK** Low Time | 40 | | ns |
| Tch | **SCK** High Time | 40 | | ns |
| Fsck | **SCK** Frequency | 0 | 8 | MHz |
| Tr,Tf | **SCK** Rise and Fall | | 100 | ns |
| Tcc | **CSN** to **SCK** Setup | 2 | | ns |
| Tcch | **SCK** to **CSN** Hold | 2 | | ns |
| Tcwh | **CSN** Inactive time | 50 | | ns |
| Tcdz | **CSN** to Output High Z | | 42 | ns |

| Symbol | Parameters | Min | Max | Units |
|---|---|---|---|---|
| Tdc | Data to **SCK** Setup | 2 | | ns |
| Tdh | **SCK** to Data Hold | 2 | | ns |
| Tcsd | **CSN** to Data Valid | | 75 | ns |
| Tcd | **SCK** to Data Valid | | 86 | ns |
| Tcl | **SCK** Low Time | 40 | | ns |
| Tch | **SCK** High Time | 40 | | ns |
| Fsck | **SCK** Frequency | 0 | 5 | MHz |
| Tr,Tf | **SCK** Rise and Fall | | 100 | ns |
| Tcc | **CSN** to **SCK** Setup | 2 | | ns |
| Tcch | **SCK** to **CSN** Hold | 2 | | ns |
| Tcwh | **CSN** Inactive time | 50 | | ns |
| Tcdz | **CSN** to Output High Z | | 75 | ns |

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| Symbol | Parameters | Min | Max | Units |
|---|---|---|---|---|
| Tdc | Data to **SCK** Setup | 2 | | ns |
| Tdh | **SCK** to Data Hold | 2 | | ns |
| Tcsd | **CSN** to Data Valid | | 116 | ns |
| Tcd | **SCK** to Data Valid | | 123 | ns |
| Tcl | **SCK** Low Time | 40 | | ns |
| Tch | **SCK** High Time | 40 | | ns |
| Fsck | **SCK** Frequency | 0 | 4 | MHz |
| Tr,Tf | **SCK** Rise and Fall | | 100 | ns |
| Tcc | **CSN** to **SCK** Setup | 2 | | ns |
| Tcch | **SCK** to **CSN** Hold | 2 | | ns |
| Tcwh | **CSN** Inactive time | 50 | | ns |
| Tcdz | **CSN** to Output High Z | | 116 | ns |

| Symbol | Parameters | Min | Max | Units |
|---|---|---|---|---|
| Tdc | Data to **SCK** Setup | 2 | | ns |
| Tdh | **SCK** to Data Hold | 2 | | ns |
| Tcsd | **CSN** to Data Valid | | 75 | ns |
| Tcd | **SCK** to Data Valid | | 85 | ns |
| Tcl | **SCK** Low Time | 40 | | ns |
| Tch | **SCK** High Time | 40 | | ns |
| Fsck | **SCK** Frequency | 0 | 5 | MHz |
| Tr,Tf | **SCK** Rise and Fall | | 100 | ns |
| Tcc | **CSN** to **SCK** Setup | 2 | | ns |
| Tcch | **SCK** to **CSN** Hold | 2 | | ns |
| Tcwh | **CSN** Inactive time | 50 | | ns |
| Tcdz | **CSN** to Output High Z | | 75 | ns |

| Symbol | Parameters | Min | Max | Units |
|---|---|---|---|---|
| Tdc | Data to **SCK** Setup | 2 | | ns |
| Tdh | **SCK** to Data Hold | 2 | | ns |
| Tcsd | **CSN** to Data Valid | | 116 | ns |
| Tcd | **SCK** to Data Valid | | 121 | ns |
| Tcl | **SCK** Low Time | 40 | | ns |
| Tch | **SCK** High Time | 40 | | ns |
| Fsck | **SCK** Frequency | 0 | 4 | MHz |
| Tr,Tf | **SCK** Rise and Fall | | 100 | ns |
| Tcc | **CSN** to **SCK** Setup | 2 | | ns |
| Tcch | **SCK** to **CSN** Hold | 2 | | ns |
| Tcwh | **CSN** Inactive time | 50 | | ns |
| Tcdz | **CSN** to Output High Z | | 116 | ns |

## 5-4. Data FIFO

The data FIFOs are used to store payload that is transmitted (TX FIFO) or payload that is received and ready to be clocked out (RX FIFO). The FIFOs are accessible in both PTX mode and PRX mode.

The following FIFOs are present in AI00340:

- TX three level, 32 byte FIFO
- RX three level, 32 byte FIFO

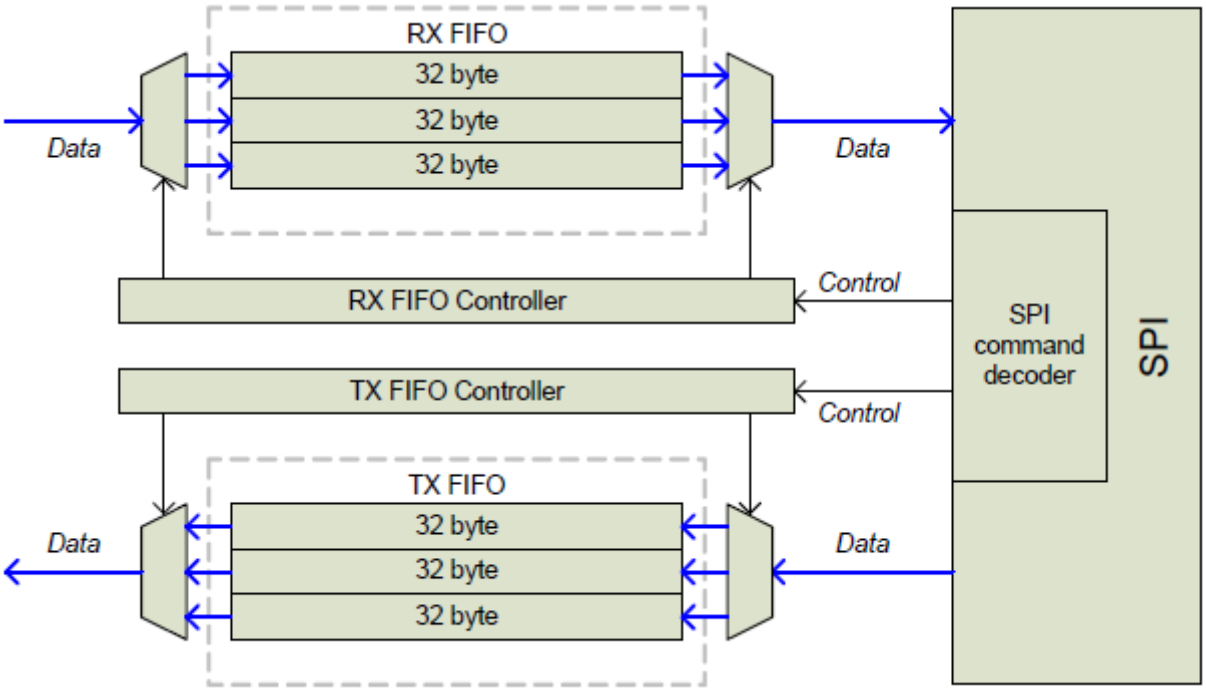
Both FIFOs have a controller and are accessible through the SPI by using dedicated SPI commands. A TX FIFO in PRX can store payload for ACK packets to three different PTX devices. If the TX FIFO contains more than one payload to a pipe, payloads are handled

using the first in - first out principle. The TX FIFO in a PRX is blocked if all pending payloads are addressed to pipes where the link to the PTX is lost. In this case, the MCU can flush the TX FIFO by using the FLUSH_TXcommand.

The RX FIFO in PRX may contain payload from up to three different PTX devices. A TX FIFO in PTX can have up to three payloads stored. The TX FIFO can be written to by three commands, W_TX_PAYLOADand W_TX_PAYLOAD_NO_ACKin PTX mode and W_ACK_PAYLOADin PRX mode. All three commands give access to the TX_PLDregister.

The RX FIFO can be read by the command R_RX_PAYLOADin both PTX and PRX mode. This command gives access to the RX_PLD register.

The payload in TX FIFO in a PTX is NOT removed if the MAX_RTIRQ is asserted. Figure 27. is a block dia- gram of the TX FIFO and the RX FIFO.




In the FIFO_STATUS register it is possible to read if the TX and RX FIFO is full or empty. The TX_REUSE bit is also available in the FIFO_STATUS register. TX_REUSE is set by the SPI command REUSE_TX_PL, and is reset by the SPI commands W_TX_PAYLOAD or FLUSH TX.

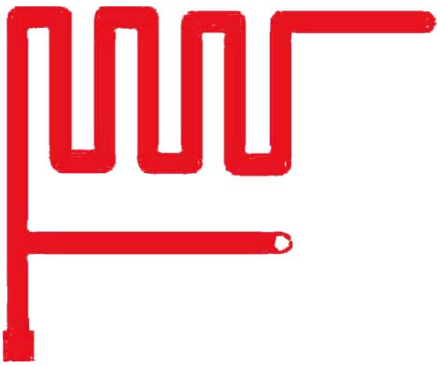
## 5-5. Interrupt

The AI00340 has an active low interrupt (**IRQ**) pin. The **IRQ**pin is activated when TX_DS IRQ, RX_DR IRQ or MAX_RT IRQ are set high by the state machine in the STATUS register. The **IRQ**pin resets when MCU writes '1' to the IRQ source bit in the STATUS register. The IRQ mask in the CONFIGregister is used to select the IRQ sources that are allowed to assert the **IRQ**pin. By setting one of the MASK bits high, the corresponding IRQ source is disabled. By default all IRQ sources are enabled.

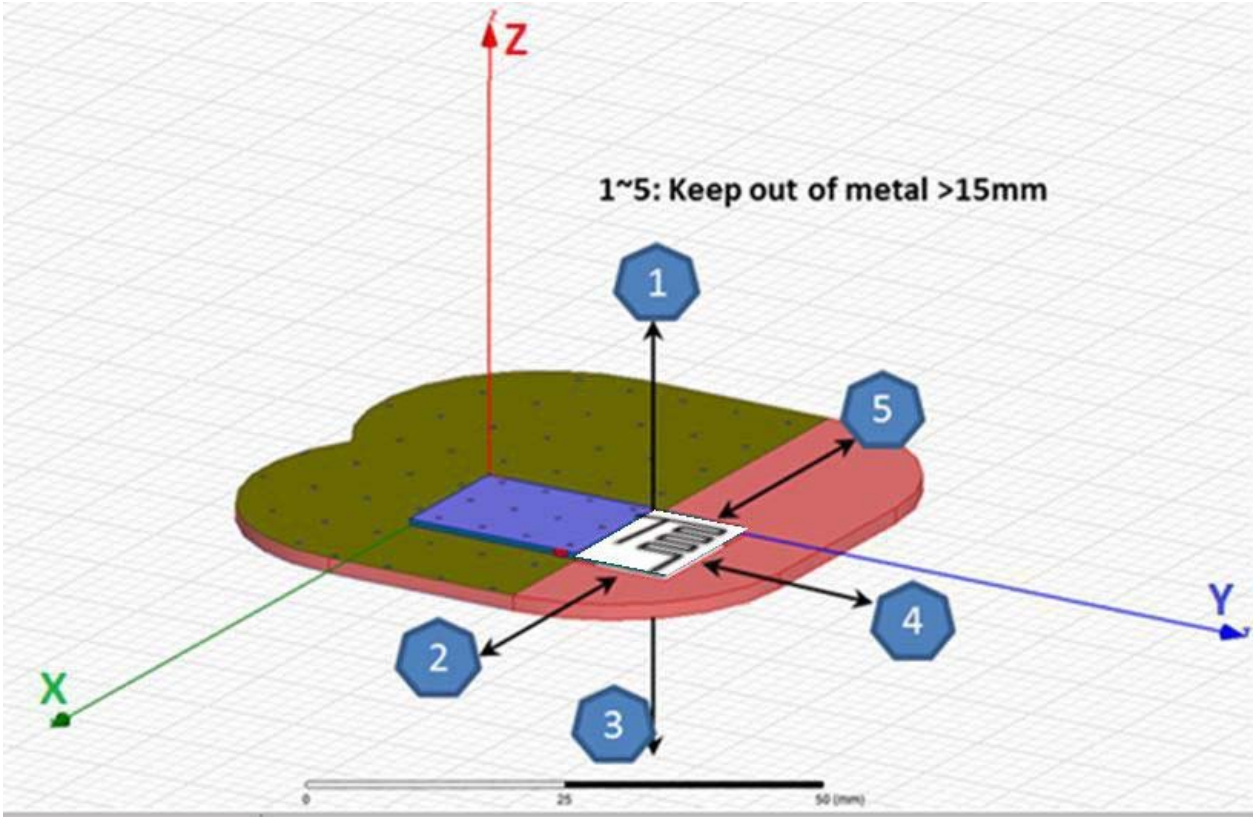
**Note:** The 3 bit pipe information in the STATUSregister is updated during the **IRQ**pin high to low transition. If the STATUSregister is read during an **IRQ**pin high to low transition, the pipe information is unreliable.

# 6、PCB Printed Antenna Information

## 6-1. PCB Printed Antenna Dimension



## 6-2. Antenna Keep Out Area Example



## 6-3. Module Radiation Pattern

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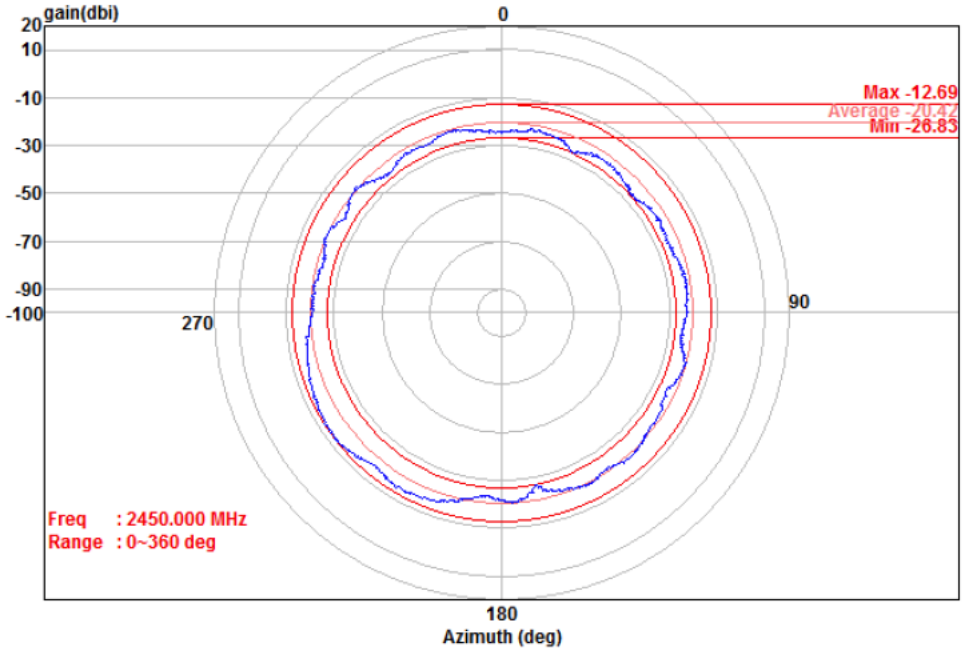
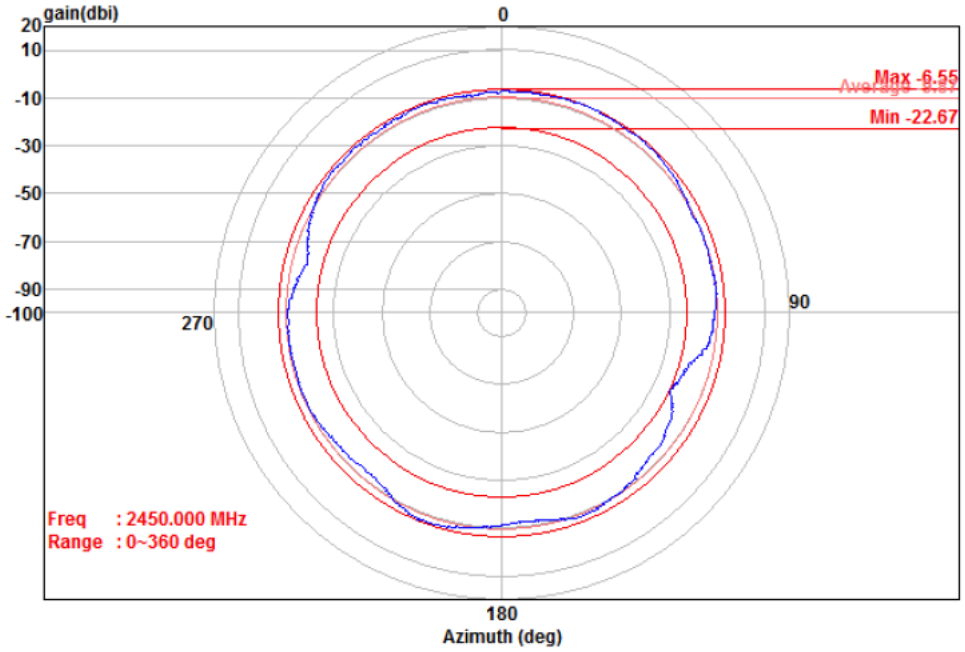
VERTICAL_Antenna 2D Radiation Pattern @2450 MHz




Condition : 3m VERTICAL
Project Number:
Compy :
Model : PCB
Test Mode : 2450
Test Site : Chamber 966
Temp/Humi : 25/60

HORIZONTAL_Antenna 2D Radiation Pattern @2450 MHz




Condition : 3m HORIZONTAL
Project Number:
Compy :
Model : PCB
Test Mode : 2450
Test Site : Chamber 966
Temp/Humi : 25/60

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# APPENDIX A:CERTIFICATION NOTICES

**Federal Communications Commission (FCC) Statement**

15.21
You are cautioned that changes or modifications not expressly approved by the part responsible for compliance could void the user's authority to operate the equipment.

15.105(b)
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.
However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.
-Increase the separation between the equipment and receiver.
-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:
1) this device may not cause harmful interference, and
2) this device must accept any interference received, including interference that may cause undesired operation
of the device.

**FCC RF Radiation Exposure Statement**

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.
This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.
This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
Note: The end product shall has the words "Contains Transmitter Module FCC ID: 2AMPP-AI00340

**Canada, Industry Canada (IC)**

This Class B digital apparatus complies with Canadian ICES-003
Cet appareil numérique de classe B est conforme à la norme NMB-003.

**Le present appareil est conforme aux CNR d'Industrie Canada applicables auxappareils radio exempts de licence.L'exploitation est autorisée aux deux conditions suivantes:**
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage adioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Déclaration d'exposition aux radiations:**
Cet équipement est conforme aux limites d'exposition au rayonnement ISED établies pour un environnement non contrôlé.
Cet équipement doit être installé et utilisé à une distance minimale de 20 cm entre le radiateur et votre corps.

Cet émetteur ne doit pas être co-localisé ou fonctionner en conjonction avec une autre antenne ou un autre émetteur.

**ICES-003 RF Radiation Exposure Statement**

This equipment complies with ICES-003 radiation exposure limits set forth for an uncontrolled environment.
This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.
This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
Note: The end product shall has the words “Contains Transmitter Module IC ID: 11471A-AI00340”

**(Modular approval) End Product Labeling:**

The final end product must be labeled in a visible area with the following: “Contains IC: 11471A-AI00340”.

**OEM statement**

The Original Equipment Manufacturer (OEM) must ensure that the OEM modular transmitter must be labeled with its own FCC ID number. This includes a clearly visible label on the outside of the final product enclosure that displays the contents shown below. If the FCC ID is not visible when the equipment is installed inside another device, then the outside of the device into which the equipment is installed must also display a label referring to the enclosed equipment

The end product with this module may subject to perform FCC part 15 unintentional emission test requirement and be properly authorized.
This device is intended for OEM integrator only This radio transmitter (192170139/AA/00) has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed Below, with the maximum permissible gain indicated. Antenna types not included in this list that Have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.
AI00340-1: PCB  Antenna, 1 dBi

# APPENDIX B: LABEL FOR FINISHED PRODUCT

Contains Transmitter Module FCC ID: 2AMPP-AI00340
and IC ID: 11471A-AI00340

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1) this device may not cause harmful interference, and
2) this device must accept any interference received, including interference that may cause the device undesired operation of.

# Version Information

| Date | number | Description |
|---|---|---|
| 2021.10.13 | V1.0 | Initial Version |
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