Technical Description

The Equipment Under Test (EUT) is a Smarter Coffee Model: SMC01-US, that equips with WiFi connectivity feature. The Smarter Coffee can be controlled by the corresponding smartphone apps to grind coffee bean and boil coffee. The EUT is powered 120VAC only.

Antenna Type: Internal, Integral
Antenna Gain: 2.24dBi

(Peak measurement)

Operating mode	Nominal Conducted Power	Production Tolerance	Modulation Type
802.11b	17.4 dBm	+3/- 3dB	DSSS
802.11g	18.5 dBm	+3/- 3dB	OFDM
802.11n (HT20)	17.3 dBm	+3/- 3dB	MCSn (n=1 to 7)

The main components are described below:

WLAN (WiFi) and Main Processor Unit

1. U101 (imp003) is integrated unit with Broadcom BCM43362 (2.4GHz radio core) and Main Processor (ST Micro STM32F405 MCU). The 2.4GHz RF radio core is for the WLAN (WiFi) IEEE 802.11 b/g/n(HT20).
2. U100 (S25FL116K0XMFI043) is 16Mb flash memory for U101 (imp003).

Other Unit

1. U1 (JLX12864G-332-BN) is LCD Display.
2. U3 (SLG41143V) is temperature sensing IC.

Channel Occupation

channel (b/g/n20)	frequency (MHz)
1	2412
2	2417
3	2422
4	2427
5	2432
6	2437
7	2442
8	2447
9	2452
10	2457
11	2462

n20 = 802.11n HT20 (20MHz bandwidth)

WiFi Module Data Sheet

Broadcom BCM43362 WiFi + ST Micro STM32F405 MCU

electric imp P/N : imp003

MURATA P/N : LBWA1ZV1CD-716

< Specification may be changed by Murata without notice >

Murata Manufacturing Co., Ltd.

The revision history of the product specification

Issued Date	**Revision Code**	**Revision Page**	**Changed Items**	**Change Reason**
Apr.11.2014			First issued	
May.23.2014	A	P4	3. Block Diagram, 2MBit -> 4MBi	
Jun.3.2014	B	P10 P17	7. Absolute Maximum Rating 8. Operating Condition 9. Electric characteristics 14. Recommended Components	
Jul.1.2014	C	P9 P11 P12 P18	5. LED Drive 6. Phototransistor Corrected reference paragraph 10. External clock source characteristics add 11. Power Up Sequence Changed "NRST" to "RESET_L" 15.4. Low Power Schematic -ABS07-120-32.768kHz-T add -Changed "ST3215SB32768B0HPWB1" to "ST3215SB32768B0HPWB3"	
Jul.31.2014	D	P10 P18	7. SPI Flash Requirements Added SPI Flash Requirements 16. Recommended Components Added SPI Flash	
Oct.14.2014	E	P18	16. Recommended Components -Changed APT2012P3BT with KDT00030TR -Changed S24FLxxx with S25FLxxx	
Jun.8.2015	F	P18	16.5. Low Power Schematic -Changed "AP2281" to " AP2281-1/AP2281-3" -Changed "ABS25-32.768KHZ-T" to "ABS25-32.768KHZ-6-T "	
Jan.21.2016	G	P5 P11 P13,14	4.1. Dimensions -add marking information 11. Electric characteristics -updated 13. RF Characteristics -updated current consumption	
Apr.26.2016	H	P16	15. Reference Circuit -Corrected	

TABLE OF CONTENTS

Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

1. Scope

This specification is for the LBWA1ZV1CD smart module that provides connectivity to the internet via WiFi with embedded OS that works with the Electric Imp cloud service.

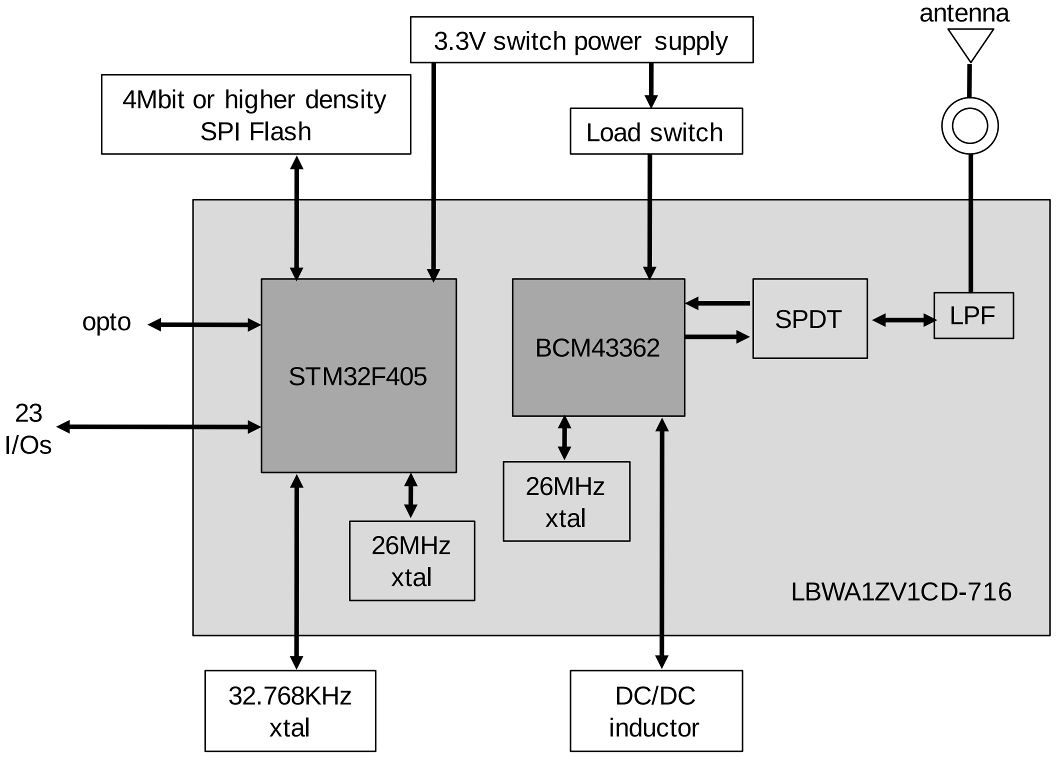
- 802.11 b/g/n WiFi
  - 20MHz 11n channels, 1 x 1
- 32-bit Cortex M4 processor
  - Robust embedded operating system with fail-safe firmware updates
  - Virtual machine for vendor firmware
- LED drive for red/green status LEDs
- Phototransistor input for Electric imp's patent-pending BlinkUp™ technology to provide optical configuration
- 23 user selectable I/Os
  - GPIO, PWM, Analog input & output, SPI, UART, I2C
  - Dedicated SPI bus for local storage
- Low power 4uA sleep mode (with external load switch)
  - Option for coin cell RTC battery backup
- Compliant with the RoHS directive

2. Part Number

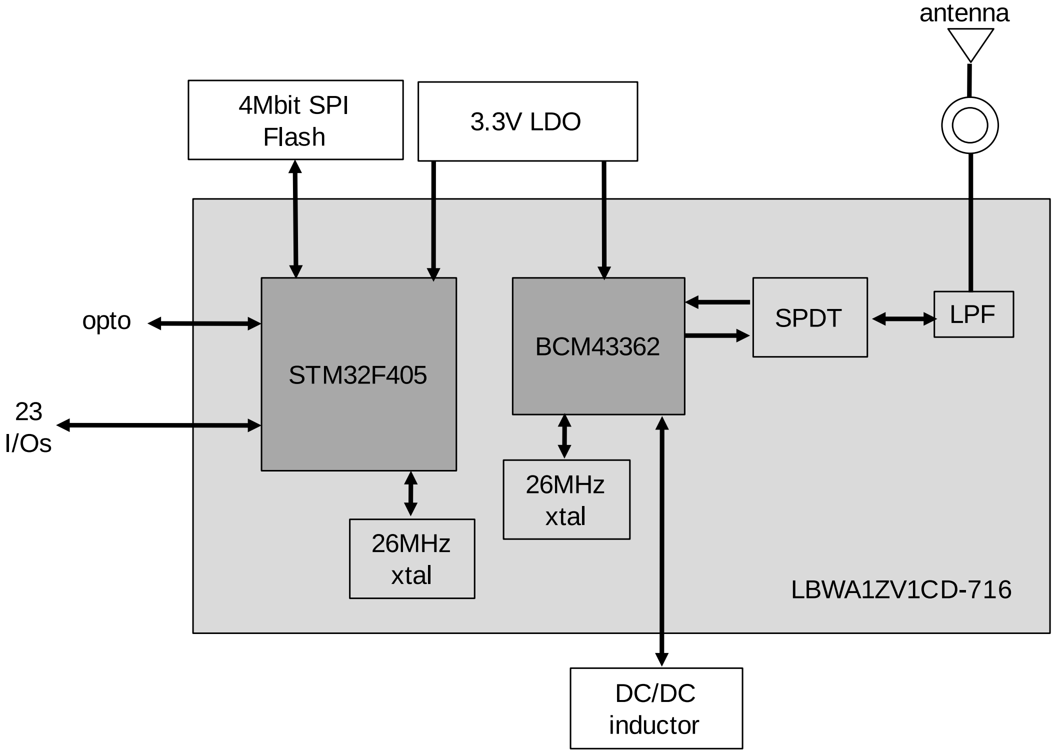
Sample Part Number
LBWA1ZV1CD-TEMP

Production Part Number
LBWA1ZV1CD-716

3. Block Diagram



<Low Power Block Diagram>

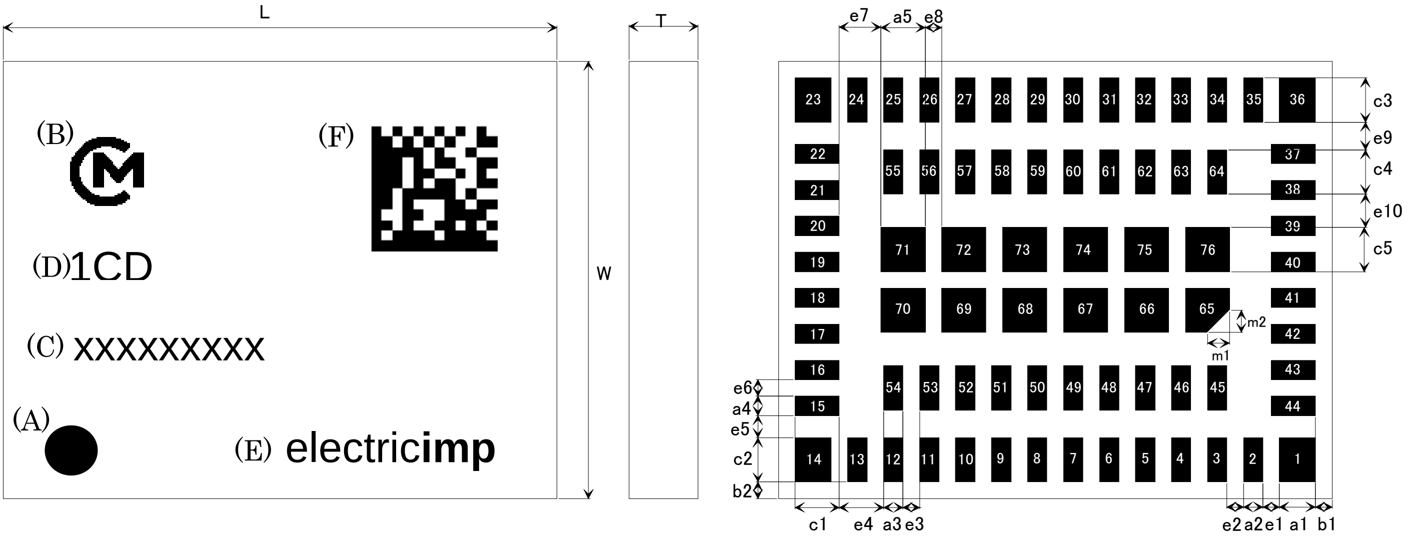


<Low Cost Block Diagram>

4. Dimensions, Marking and Terminal Configurations

4.1. Dimensions

< Top View > < Side View > < Bottom View >



Mark	Dimensions	Mark	Dimensions	Mark	Dimensions
L	10.0 +/- 0.2	W	7.9 +/- 0.2	T	1.25 max.
a1	0.65 +/- 0.1	a2	0.35 +/- 0.1	a3	0.35 +/- 0.1
a4	0.35 +/- 0.1	a5	0.80 +/- 0.1	b1	0.30 +/- 0.2
b2	0.30 +/- 0.2	c1	0.80 +/- 0.1	c2	0.80 +/- 0.1
c3	0.80 +/- 0.1	c4	0.80 +/- 0.1	c5	0.80 +/- 0.1
e1	0.30 +/- 0.1	e2	0.30 +/- 0.1	e3	0.30 +/- 0.1
e4	0.80 +/- 0.1	e5	0.40 +/- 0.1	e6	0.30 +/- 0.1
e7	0.75 +/- 0.1	e8	0.30 +/- 0.1	e9	0.50 +/- 0.1
e10	0.60 +/- 0.1	m1	0.40 +/- 0.1	m2	0.40 +/- 0.1

(unit : mm)

Marking

Marking	Meaning
(A)	Pin 1 Marking
(B)	Murata Logo
(C)	Inspection Number
(D)	Module Type
(E)	Electric Imp Logo
(F)	2D code

4.2. Terminal Configurations

No.	Terminal Name	Type	Description
1	GND	-	Ground
2	OPTO_Bias	O	Phototransistor bias voltage
3	OPTO_IN	I	Phototransistor input
4	PinW	I/O	I/O, please refer to Pin mux table
5	OSC32_IN	I	MCU sleep clock input
6	OSC32_OUT	O	MCU sleep clock output
7	PinN	I/O	I/O, please refer to Pin mux table
8	PSU_EN	O	External power supply enable
9	WLAN_POWER_EN	O	External power gate enable
10	GND	-	Ground
11	GND	-	Ground
12	ANT	-	Antenna
13	GND	-	Ground
14	GND	-	Ground
15	VDD	PI	Power supply for MCU VDD and WLAN Digital IO
16	WLAN_ANT_CTL2	O	Antenna switch control. Default is low. NC if not in use.
17	WLAN_ANT_CTL1	O	Antenna switch control. Default is high. NC if not in use.
18	VDD_PA	PI	Power supply for Internal Power Amplifier.
19	VDD_PA	PI	
20	VDD_WLAN	PI	Power supply for WLAN IC
21	VDD_WLAN	PI	
22	VDD_DCDC_IN	PI	Voltage input for core LDO, low noise LDO1 and VCO/LDO
23	GND	-	Ground
24	VDD_DCDC_OUT	PO	Voltage output for core LDO.
25	SPIFLASH_NCS	O	SPI flash nCS
26	SPIFLASH_MISO	I	SPI flash MISO

27	SPIFLASH_MOSI	O	SPI flash MOSI
28	SPIFLASH_SCK	O	SPI flash CLK
29	LED_RED	O	Must be connected to the Red terminal of the indicator LED
30	LED_GREEN	O	Must be connected to the Green terminal of the indicator LED
31	PinM	I/O	I/O, please refer to Pin mux table
32	PinL	I/O	I/O, please refer to Pin mux table
33	PinK	I/O	I/O, please refer to Pin mux table
34	PinJ	I/O	I/O, please refer to Pin mux table
35	PinH	I/O	I/O, please refer to Pin mux table
36	GND	-	Ground
37	PinG	I/O	I/O, please refer to Pin mux table
38	PinF	I/O	I/O, please refer to Pin mux table
39	PinE	I/O	I/O, please refer to Pin mux table
40	PinD	I/O	I/O, please refer to Pin mux table
41	PinC	I/O	I/O, please refer to Pin mux table
42	PinB	I/O	I/O, please refer to Pin mux table
43	PinA	I/O	I/O, please refer to Pin mux table
44	VDDA	PI	MCU analog power and reference, must be connected to VDD
45	VBAT	PI	MCU retention RAM and RTC backup supply
46	PinY	I/O	I/O, please refer to Pin mux table
47	GND	-	Ground
48	PinV	I/O	I/O, please refer to Pin mux table
49	GND	-	Ground
50	DNC	-	Do not connect
51	GND	-	Ground
52	RESET_L	I	MCU reset, internally pulled up
53	GND	-	Ground
54	GND	-	Ground

55	GND	-	Ground
56	GND	-	Ground
57	GND	-	Ground
58	PinQ	I/O	I/O, please refer to Pin mux table
59	PinR	I/O	I/O, please refer to Pin mux table
60	PinT	I/O	I/O, please refer to Pin mux table
61	PinP	I/O	I/O, please refer to Pin mux table
62	PinS	I/O	I/O, please refer to Pin mux table
63	PinU	I/O	I/O, please refer to Pin mux table
64	PinX	I/O	I/O, please refer to Pin mux table
65	VSSA	-	MCU analog ground, must be connected to GND
66-76	GND	-	Ground

4.3. Pin Mux Table

Pin	uartFG	uartQRPW	uartUVGD	uartWJ	uartDM	i2cFG	i2cAB	spiEBCA	spiLGDK	ADC	DAC	PWM	Wake from sleep	State change callback	Pin trig pulse gen
Pin A							SCL	nSS		yes	yes			yes	
Pin B							SDA	MISO		yes		yes		yes	
Pin C								SCLK		yes	yes	yes		yes	
Pin D			CTS		TX				SCLK					yes	
Pin E								MOSI		yes		yes		yes	for C
Pin F	TX					SCL				yes		yes			for K,X
Pin G	RX		RTS			SDA			MISO					yes	
Pin H										yes					
Pin J				RX						yes					
Pin K									nSS	yes		yes			
Pin L									MOSI			yes			for G
Pin M					RX							yes		yes	for D
Pin N										yes					
Pin P		RTS												yes	
Pin Q		TX												yes	
Pin R		RX												yes	
Pin S															
Pin T														yes	
Pin U			TX											yes	
Pin V			RX											yes	
Pin W		CTS		TX						yes			yes	yes	
Pin X														yes	
Pin Y															

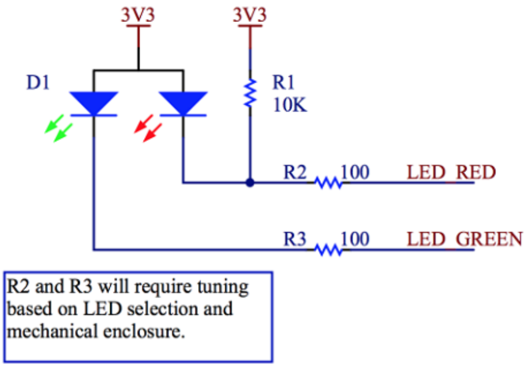
5. LED Drive

The indicator LED should be bicolor, because red, green and amber (red+green) are used to indicate status.

The LED drive pins will auto-detect common anode or common cathode parts. The detection is done by looking to see which way up the LED_RED pin is idling at boot; to ensure this works correctly, please place a 100k resistor in parallel with the red LED.

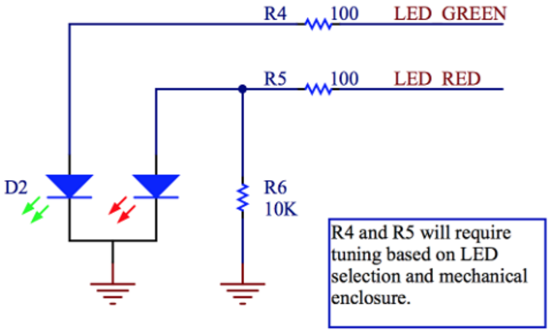
The current drive on these pins is 20mA maximum.
Please refer to paragraph 15 for the recommended LEDs.

<Common anode diagram>



R2 and R3 will require tuning based on LED selection and mechanical enclosure.

<Common cathode diagram>



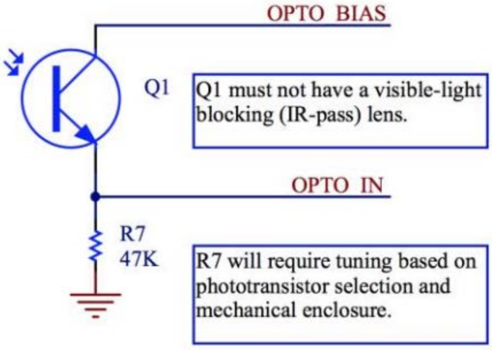
R4 and R5 will require tuning based on LED selection and mechanical enclosure.

6. Phototransistor

The phototransistor is used to receive BlinkUp configuration data. The bias resistor connected between OPTO_IN and GND may need to be adjusted to ensure adequate sensitivity and response time - in general you need at least 500mV swing on the OPTO_IN pin between black and white states, with the worst (dimmest) BlinkUp sender you can find.

End-user BlinkUp send data at between 30 and 60 bits per second, depending on the user's device. For factory configuration, data is typically sent at 142 bits per second using red LED(s) in a test fixture. If your application does not require optical configuration, config can be sent electrically at 120 bits per second from another micro using the OPTO_IN pin. Please contact us for more details.

Please refer to paragraph 15 for the recommended phototransistors.



Q1 must not have a visible-light blocking (IR-pass) lens.

R7 will require tuning based on phototransistor selection and mechanical enclosure.

7. SPI Flash Requirements

An external SPI Flash part is required. The minimum size of the SPI Flash is 4 Mbit (512 kByte). The area below address 0x70000 (448 kByte) is reserved for use by the OS. The remainder of the available space is made available to user code programmatically. Areas below address 0x70000 will be erased and reprogrammed by the OS; applications using pre-programmed SPI Flash components must not use space below this address.

Minimum Size	4 Mbit (512 kByte)
Reserved for OS (do not pre-program)	0x000000 to 0x70000 (448 kByte)

8. Absolute Maximum Rating

		min.	max.	unit
Storage Temperature		-40	+85	deg.C
Supply Voltage	VDD	-0.3	4	V
	VDD_PA	-0.3	6	V
	VDD_WLAN	-0.3	6	V

Caution! The absolute maximum ratings indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Opertation at absolute maximum conditions for extended periods can adversely affect long-term reliabilty of the device.

9. Operating Condition

		min.	typ.	max.	unit
Operating Temperature Range(*1)		-40		+85	deg.C
Specification Temperature Range		-20		+70	deg.C
Supply Voltage	VDD	1.8	3.3	3.6	V
	VDD_PA	2.3(*2)	3.3	4.8(*2) (*3)	V
	VDD_WLAN	2.3(*2)	3.3	4.8(*2) (*3)	V
Backup operating Voltage	VBAT	1.65	3.3	3.6	V

[Note] All RF characteristics in this datasheet are defined by Specification Temperature Range

(*1) Functionality is guaranteed but specifications require derating at extreme temperatures.

(*2)The BCM43362 is functional across this range of voltage. RF performance is guaranteed only 3.0V < VDD_PA/WLAN < 4.8V

(*3) The maximum continuous voltage is 4.8V. Voltages up to 5.5V for up to 10 seconds, cumulative duration, over the lifetime of the device are allowed voltages as high 5.0V for up to 250 seconds, cumulative duration, over the lifetime of the device are allowed.

10. Electric characteristics

Parameter	Description	Min	Typ	Max	Unit
I_{DDA}	Current input on VDDA		70	500	uA
V_{IH}	I/O input high level voltage	$0.7V_{dd}$		3.6	V
V_{IL}	I/O input low level voltage	$V_{ss}-0.3$		$0.3V_{dd}$	V
I_{OUT}	Output current on any single I/O pin	-8		8	mA
	Output current on LED_RED pin	-20		20	mA
	Output current on LED_GREEN pin	-20		20	mA
	Total output current on all I/O pins including LED_RED & LED_GREEN	-80		-80	mA
I/O input leakage current	VSS □ VIN □ VDD			6	uA
Load capacitance	Pins A to Y		15		pF

11. External clock source characteristics

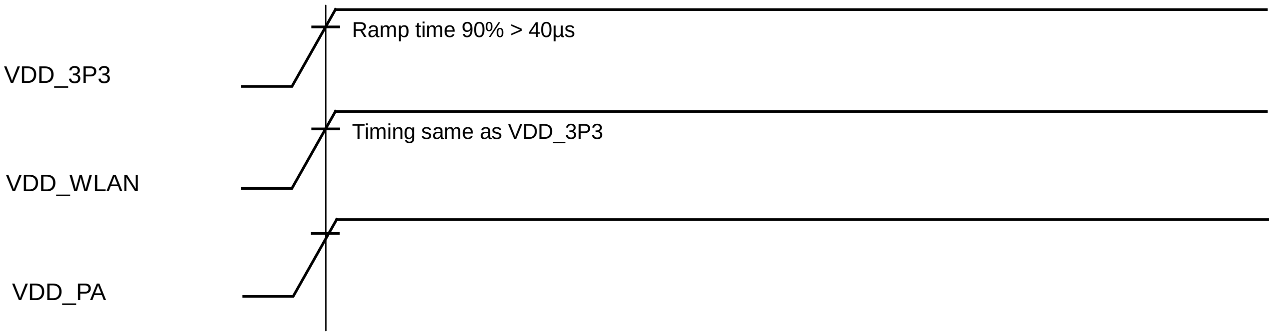
11.1. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(*1)		-	32.768	1,000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{W(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(*1)		450	-	-	ns
$t_{r(LSE)}$ $t_{r(LSE)}$	OSC32_IN rise or fall time(*1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(*1)		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	uA
ESR	Equivalent Series Resistance		-	-	60	kΩ
CL	Load Capacitance			6		pF
C0	Shunt Capacitance			1.5		pF

(*1) Guaranteed by design, not tested in production

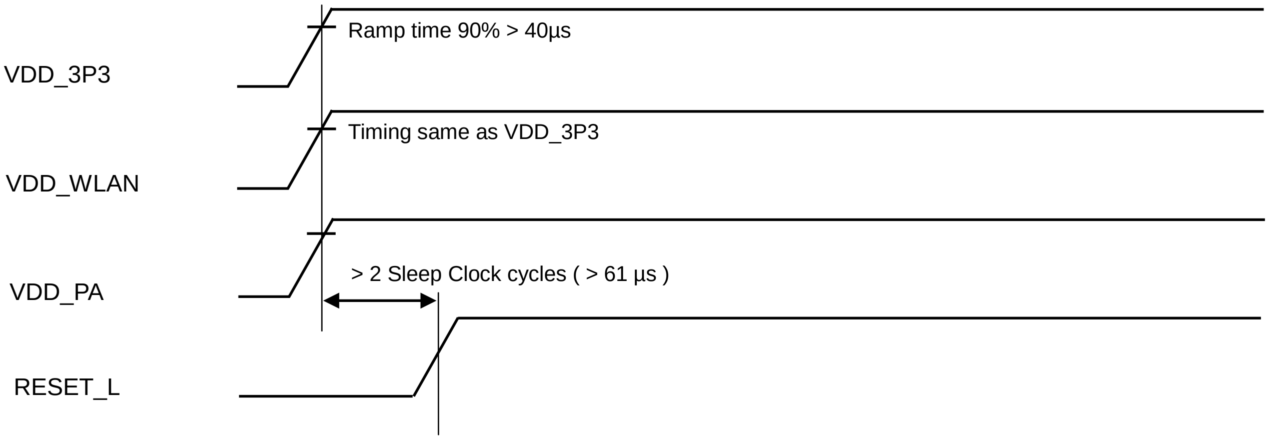
12. Power Up Sequence

12.1. Without RESET_L control



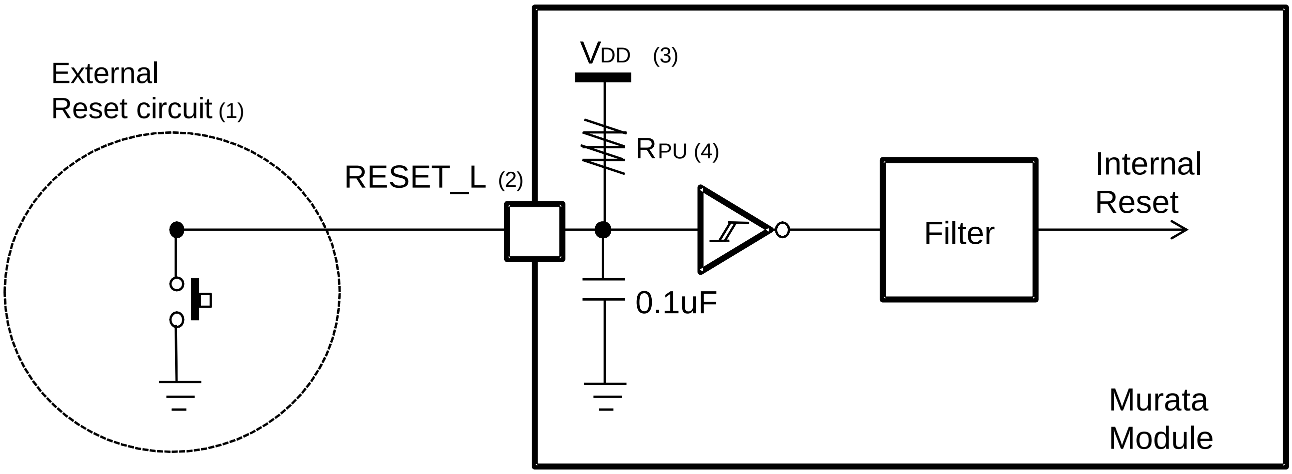
*Power down sequence is opposite sequence of power up.

12.2. With RESET_L control



*Power down sequence is opposite sequence of power up.

12.2.1. RESET_L Circuit



(1) The reset network protects the device against parasitic resets.
(2) The use must ensure that the level on the RESET_L pin can go below the 0.8V. Otherwise the reset is not taken into account by the device.
(3) Vdd=3.3V(for the 1.8□ Vdd□ 3.6 voltage range)
(4) RPU=40k ohm (for the 30□ RPU□ 50kohm range)

13. RF Characteristics

13.1. RF Characteristics for IEEE802.11b (11Mbps mode unless otherwise specified.)

Conditions: 25deg.C, VDD=VDD_WLAN=3.3V

Items	Contents			
Specification	IEEE802.11b			
Mode	DSSS / CCK			
Frequency	2400 - 2483.5MHz			
Data rate	1, 2, 5.5, 11Mbps			
Target Max Output Power	17.0			
- DC Characteristics -	min.	Typ.	max.	Unit
1. DC current				
1) Tx mode	-	350	450	mA
2) Rx mode	-	100	160	mA
- Tx Characteristics -	min.	Typ.	max.	Unit
2. Power Levels	15.0	17.0	19.0	dBm
- Rx Characteristics -	min.	typ.	max.	Unit
3. Minimum Input Level Sensitivity				
1) 11Mbps (FER ≤ 8%)	-	-87	-76	dBm
4. Maximum Input Level (FER ≤ 8%)	-10	-	-	dBm
5. Adjacent Channel Rejection (FER ≤ 8%)	35	-	-	dB

13.2. RF Characteristics for IEEE802.11g (54Mbps mode unless otherwise specified.)

Conditions: 25deg.C, VDD=VDD_WLAN=3.3V

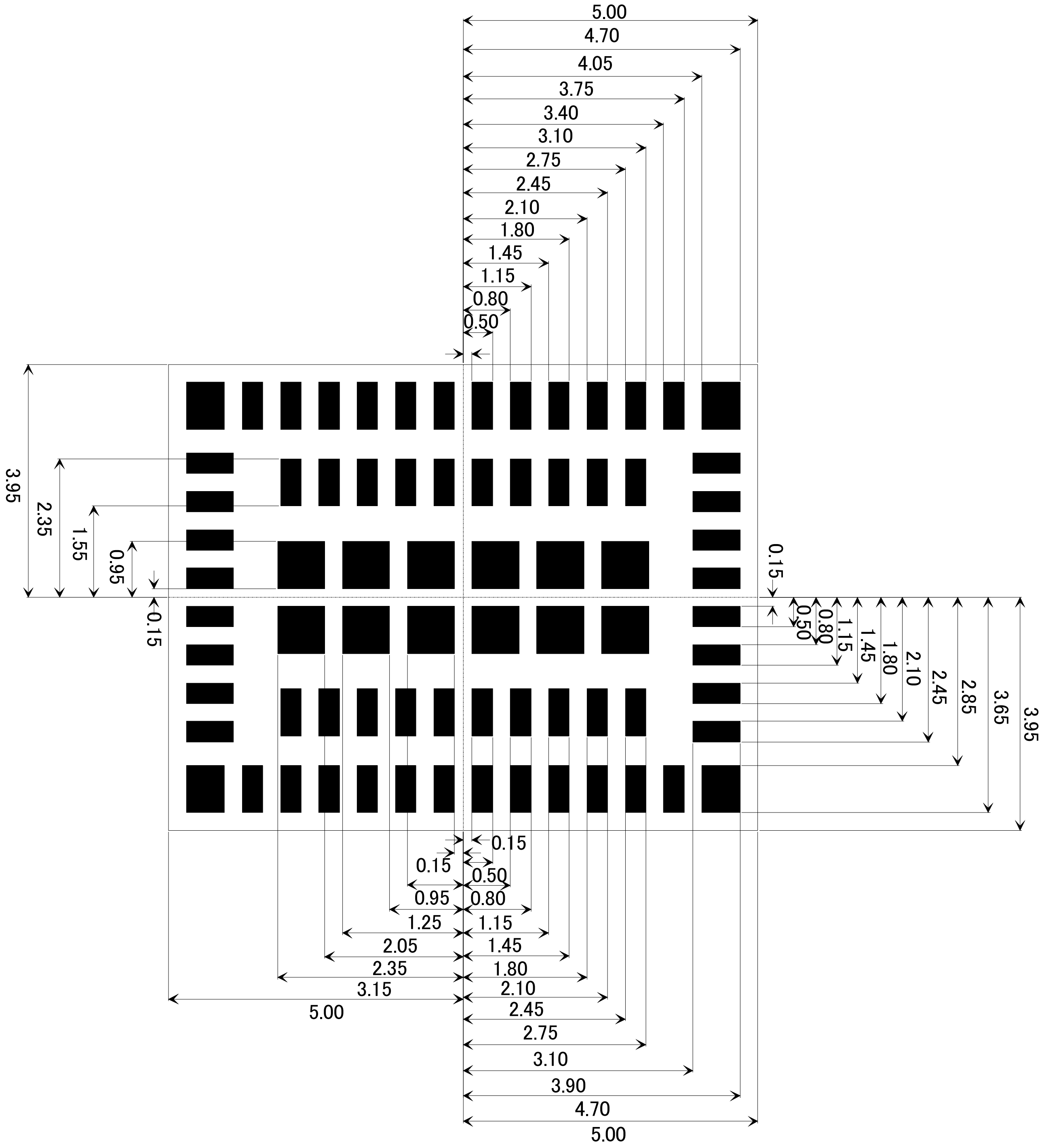
Items	Contents			
Specification	IEEE802.11g			
Mode	OFDM			
Frequency	2400 - 2483.5MHz			
Data rate	6, 9, 12, 18, 24, 36, 48, 54Mbps			
Target Max Output Power	13.0dBm			
- DC Characteristics -	min.	Typ.	max.	Unit
1. DC current				
1) Tx mode (1024byte, 20usec interval)	-	295	370	mA
2) Rx mode	-	100	160	mA
- Tx Characteristics -	min.	typ.	max.	unit
2. Power Levels	11.0	13.0	15.0	dBm
- Rx Characteristics -	min.	typ.	max.	Unit
3. Minimum Input Level Sensitivity				
1) 54Mbps (PER ≤ 10%)	-	-73	-65	dBm
4. Maximum Input Level (PER ≤ 10%)	-20	-	-	dBm
5. Adjacent Channel Rejection (PER ≤ 10%)	-1	-	-	dB

13.3. RF Characteristics for IEEE802.11n (65Mbps(MCS7) mode unless otherwise specified.)

Conditions: 25deg.C, VDD=VDD_WLAN=3.3V

Items	Contents			
Specification	IEEE802.11n			
Mode	OFDM			
Frequency	2400 - 2483.5MHz			
Data rate	6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps			
Target Max Output Power	12.0dBm			
- DC Characteristics -	min.	Typ.	max.	Unit
1. DC current				
1) Tx mode (1024byte, 20usec interval)	-	280	350	mA
2) Rx mode	-	100	160	mA
- Tx Characteristics -	min.	typ.	max.	Unit
2. Power Levels	10.0	12.0	14.0	dBm
- Rx Characteristics -	min.	typ.	max.	Unit
3. Minimum Input Level Sensitivity				
1) 65Mbps (PER ≦ 10%)	-	-70	-64	dBm
4. Maximum Input Level (PER ≦ 10%)	-20	-	-	dBm
5. Adjacent Channel Rejection (PER ≦ 10%)	-2	-	-	dB

14. Land Pattern (Top View)

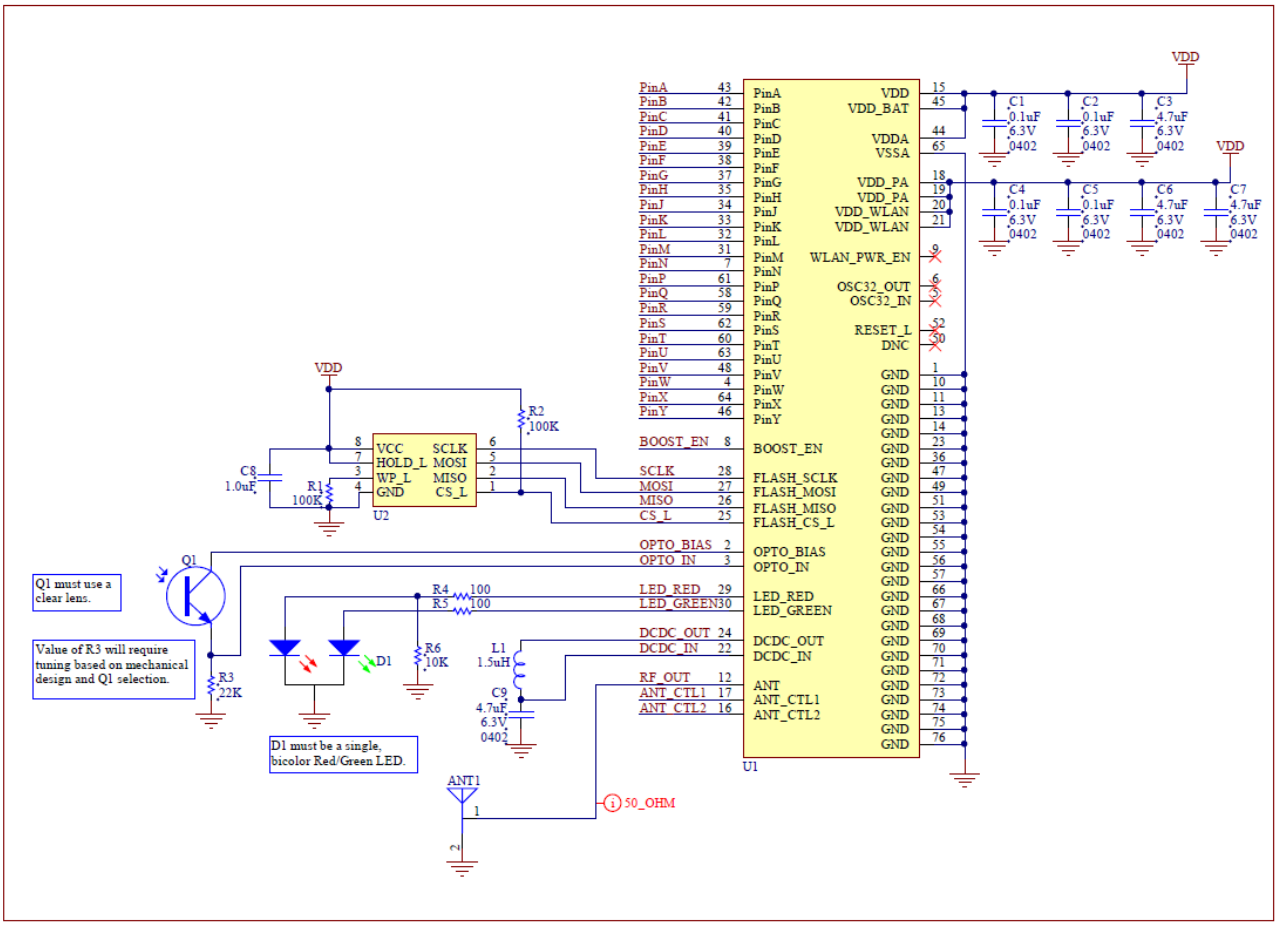


Unit : mm

15. Reference Circuit

15.1. Low Cost Schematic

Please refer to paragraph 16 for the low cost recommended components.



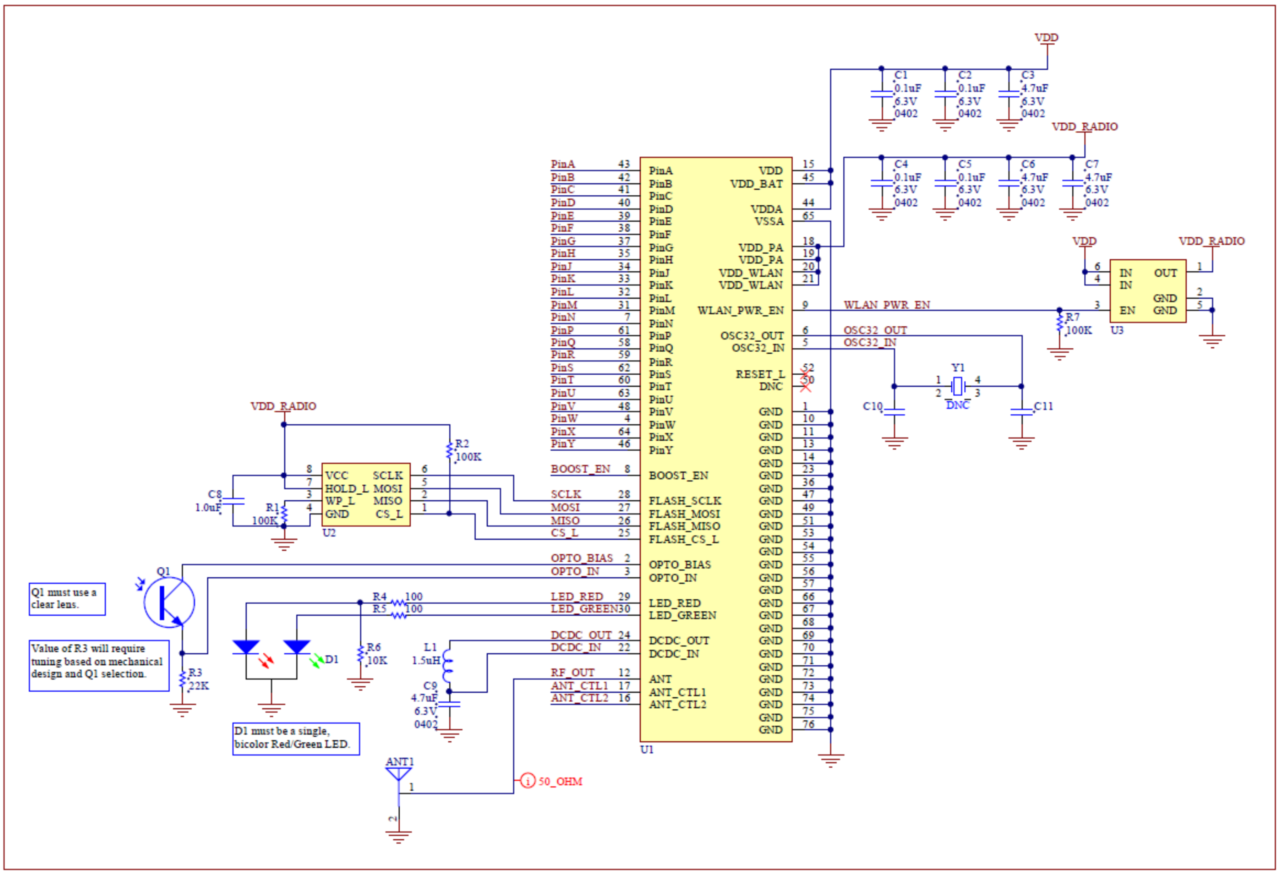
Q1 must use a clear lens.

Value of R3 will require tuning based on mechanical design and Q1 selection.

D1 must be a single, bicolor Red/Green LED.

15.2. Low Power Schematic

Please refer to paragraph 16 for the low power recommended components.



16. Recommended Components

16.1. Bi-color LED

	Manufacturer	Manufacturer’s part number
Surface mount		
top-view	SunLED	XZMDKVG59W-1
	Liteon	LTST-C195KGJRKT
side-view	SunLED	XZMDKVG88W
	Bivar	SM1204BC
Through-hole		
3mm	SunLED	XLMDKVG34M
	Liteon	LTL1BEKVJNN

16.2. Phototransistor

	Manufacturer	Manufacturer’s part number
Surface mount		
top-view	Everlight	PT17-21C/L41/TR8
	Fairchild	KDT00030TR
side-view	SunLED	XZRNI56W-1
	Everlight	PT12-21C/TR8
Through-hole		
3mm	SunLED	XRNI30W-1
	Honeywell	SDP8405-003

16.3. SPI Flash

Size	Manufacturer	Manufacturer’s part number
4 Mbit	Spansion	S25FL204K
4 Mbit	Macronix	MX25L4006E
32 Mbit	Spansion	S25FL132K
32 Mbit	Macronix	MX25L3206E

16.4. Low Cost Schematic

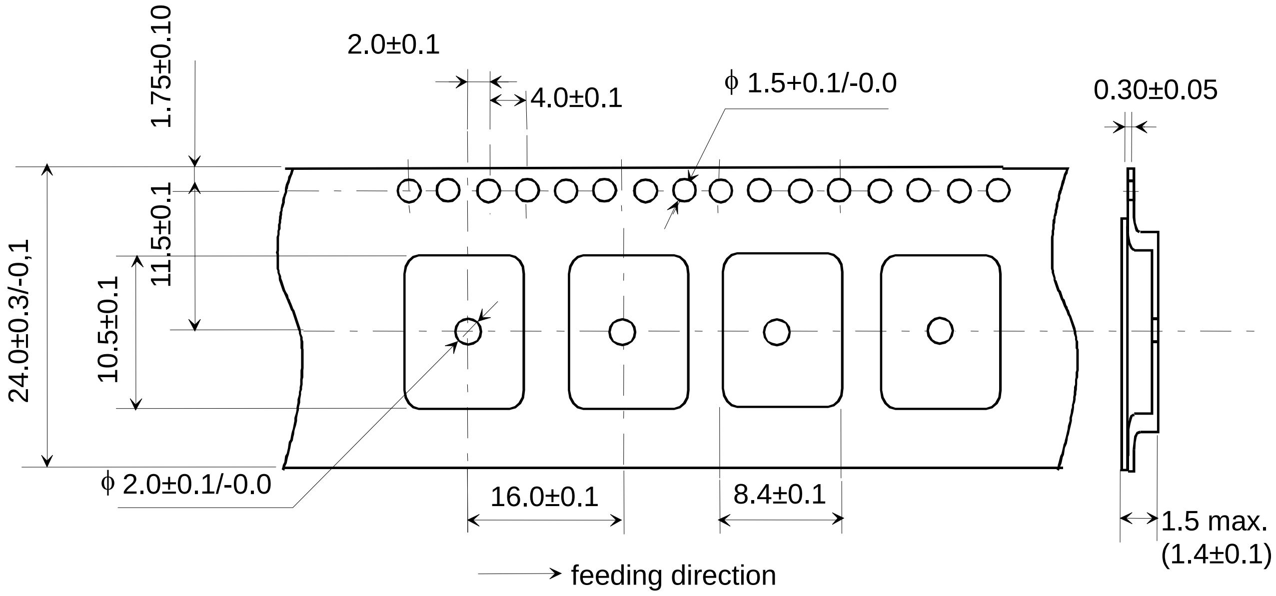
Size	Manufacturer	Manufacturer’s part number	Description
U2	please refer to paragraph 16.3		SPI Flash
Q1	please refer to paragraph 16.2		clear lens phototransistor
D1	please refer to paragraph 16.1		red/green bicolor LED
L1	Murata	LQM21PN1R5MC0	1.5uH inductor

16.5. Low Power Schematic

Ref Des	Manufacturer	Manufacturer’s part number	Description
U2	please refer to paragraph 16.3		SPI Flash
U3	Diodes Inc.	AP2281-1/AP2281-3	2A load switch
Q1	please refer to paragraph 16.2		clear lens phototransistor
D1	please refer to paragraph 16.1		red/green bicolor LED
L1	Murata	LQM21PN1R5MC0	1.5uH inductor
Y1	Kyocera	ST3215SB32768B0HPWB3	32.768kHz crystal
	Abracon	ABS25-32.768KHZ-6-T	
	Abracon	ABS07-120-32.768kHz-T	

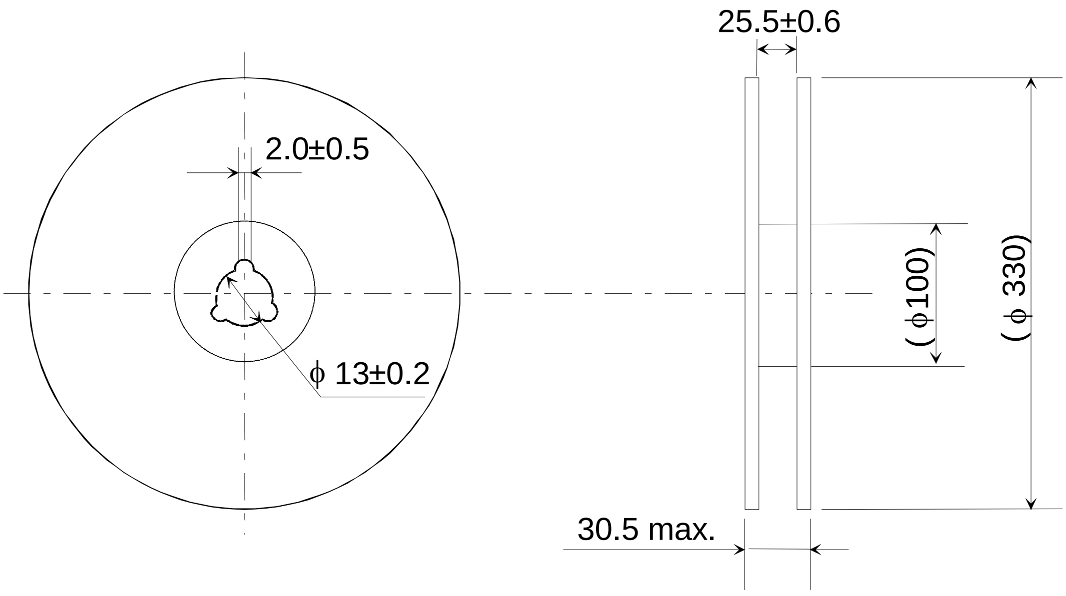
17. Tape and Reel Packing

(1) Dimensions of Tape (Plastic tape)



1) The corner and ridge radiuses (R) of inside cavity are 0.3mm max.
2) Cumulative tolerance of 10 pitches of the sprocket hole is +/-0.2mm
3) Measuring of cavity positioning is based on cavity center in accordance with JIS/IES standard.

(2) Dimensions of Reel



(unit : mm)

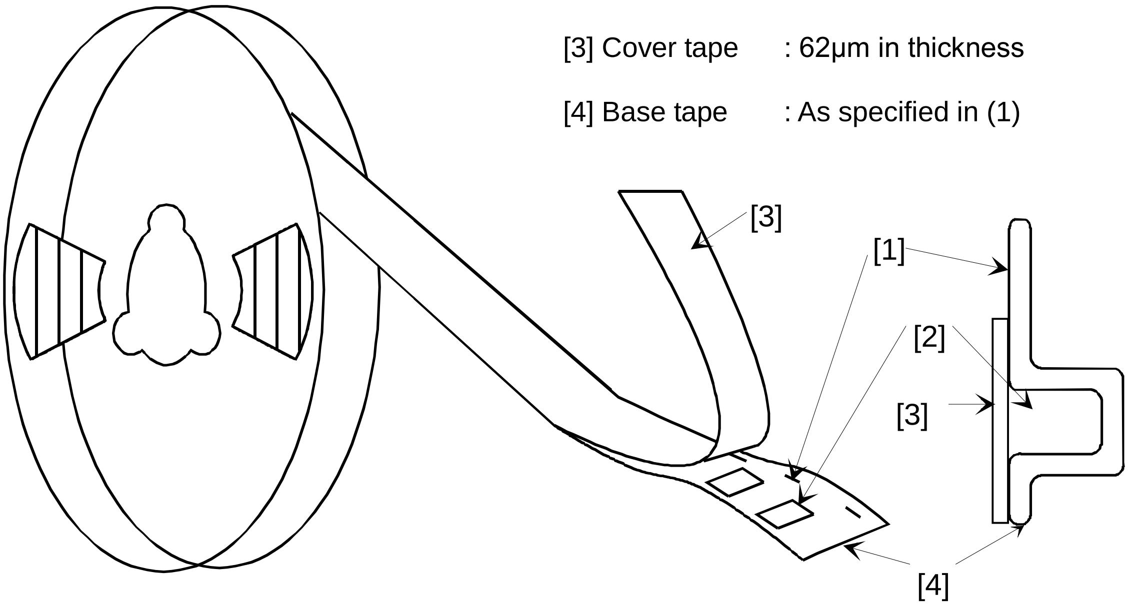
(3) Taping Diagrams

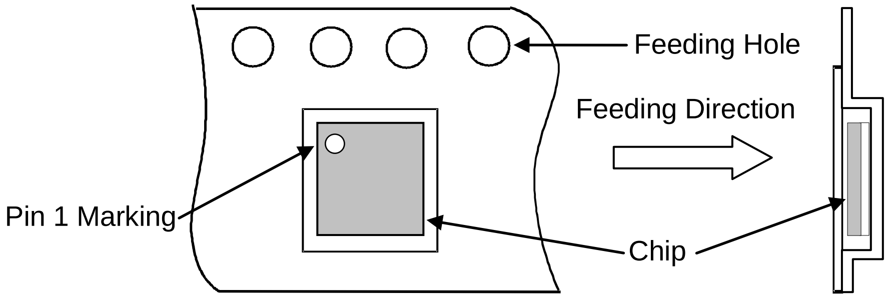
[1] Feeding Hole : As specified in (1)

[2] Hole for chip : As specified in (1)

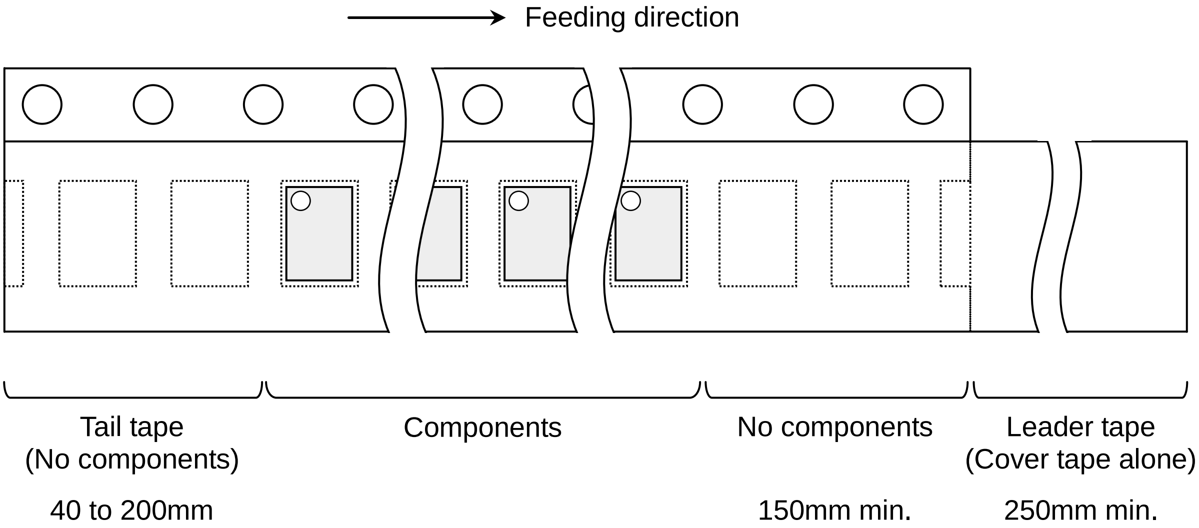
[3] Cover tape : 62μm in thickness

[4] Base tape : As specified in (1)





(4) Leader and Tail tape



(5) The tape for chips are wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.

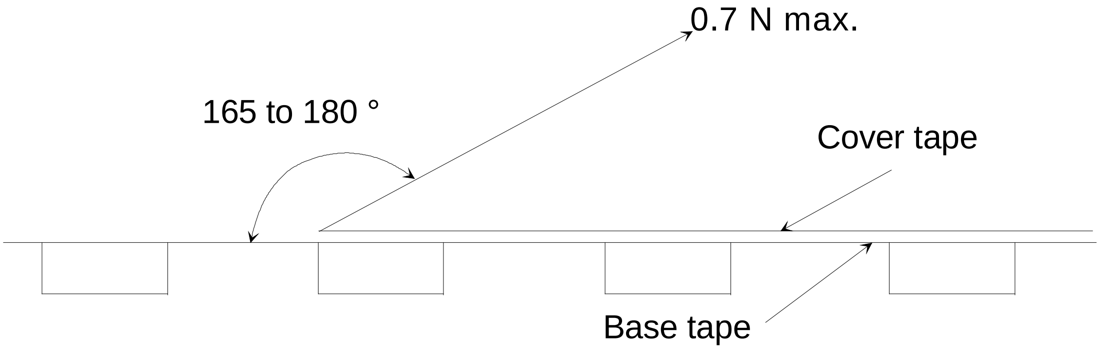
(6) The cover tape and base tape are not adhered at no components area for 250mm min.

(7) Tear off strength against pulling of cover tape : 5N min.

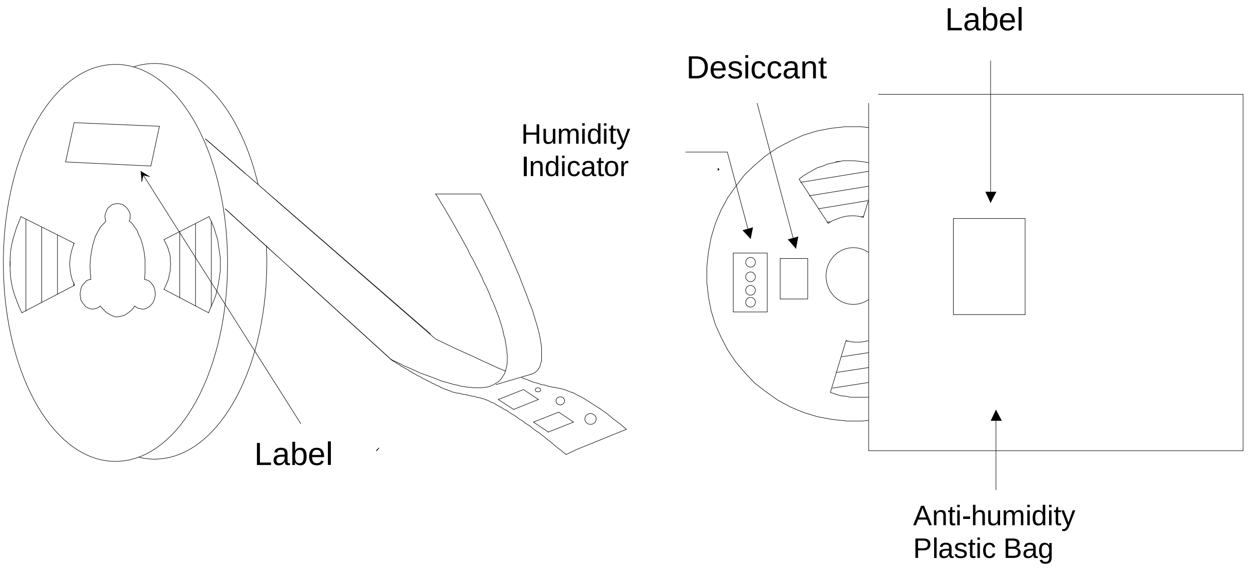
(8) Packaging unit : 1000pcs./ reel

(9) material : Base tape : Plastic
Real : Plastic
Cover tape, cavity tape and reel are made the anti-static processing.

(10) Peeling of force : 0.7N max. in the direction of peeling as shown below.



(11) Packaging (Humidity proof Packing)



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

18. NOTICE

18.1. Storage Conditions:

Please use this product within 6month after receipt.
- The product shall be stored without opening the packing under the ambient temperature from 5 to 35deg.C and humidity from 20 to 70%RH.
(Packing materials, in particular, may be deformed at the temperature over 40deg.C.)
- The product left more than 6months after reception, it needs to be confirmed the solderbility before used.
- The product shall be stored in non corrosive gas (Cl_2, NH_3, SO_2, No_x, etc.).
- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, shall not be applied in order not to damage the packing materials.

This product is applicable to MSL3 (Based on JEDEC Standard J-STD-020)
- After the packing opened, the product shall be stored at ≦30deg.C / ≦60%RH and the product shall be used within 168hours.
- When the color of the indicator in the packing changed, the product shall be baked before soldering.

Baking condition: 125+5/-0deg.C, 24hours, 1time

The products shall be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

18.2. Handling Conditions:

Be careful in handling or transporting products because excessive stress or mechanical shock may break products.

Handle with care if products may have cracks or damages on their terminals, the characteristics of products may change. Do not touch products with bear hands that may result in poor solder ability and destroy by static electrical charge.

18.3. Standard PCB Design (Land Pattern and Dimensions):

All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

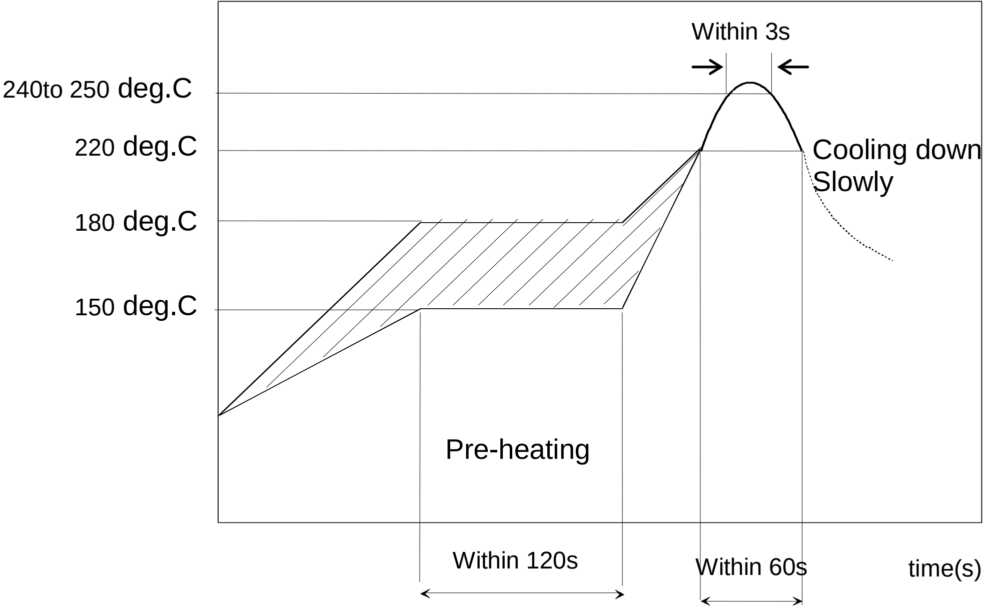
18.4. Notice for Chip Placer:

When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

18.5. Soldering Conditions:

The recommendation conditions of soldering are as in the following figure.
When products are immersed in solvent after mounting, pay special attention to maintain the temperature difference within 100 °C. Soldering must be carried out by the above mentioned conditions to prevent products from damage. Set up the highest temperature of reflow within 260 °C. Contact Murata before use if concerning other soldering conditions.

Reflow soldering standard conditions(Example)



Please use the reflow within 2 times.
Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt % or less.

18.6. Cleaning:

Since this Product is Moisture Sensitive, any cleaning is not permitted.

18.7. Operational Environment Conditions:

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (Cl_2, NH_3, SO_x, NO_x etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.
As it might be a cause of degradation or destruction to apply static electricity to products, do not apply static electricity or excessive voltage while assembling and measuring.

18.8. Input Power Capacity:

Products shall be used in the input power capacity as specified in this specifications.
Inform Murata beforehand, in case that the components are used beyond such input power capacity range.

19. PRECONDITION TO USE OUR PRODUCTS

PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.
All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.
Please note that the only warranty that we provide regarding the products is its conformance to the specifications provided herein. Accordingly, we shall not be responsible for any defects in products or equipment incorporating such products, which are caused under the conditions other than those specified in this specification.
WE HEREBY DISCLAIMS ALL OTHER WARRANTIES REGARDING THE PRODUCTS, EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION ANY WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE, THAT THEY ARE DEFECT-FREE, OR AGAINST INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS.
The product shall not be used in any application listed below which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property. You acknowledge and agree that, if you use our products in such applications, we will not be responsible for any failure to meet such requirements. Furthermore, YOU AGREE TO INDEMNIFY AND DEFEND US AND OUR AFFILIATES AGAINST ALL CLAIMS, DAMAGES, COSTS, AND EXPENSES THAT MAY BE INCURRED, INCLUDING WITHOUT LIMITATION, ATTORNEY FEES AND COSTS, DUE TO THE USE OF OUR PRODUCTS IN SUCH APPLICATIONS.

- Aircraft equipment. - Aerospace equipment - Undersea equipment.
- Power plant control equipment - Medical equipment.
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Traffic signal equipment. - Disaster prevention / crime prevention equipment.
- Burning / explosion control equipment
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.

We expressly prohibit you from analyzing, breaking, reverse-engineering, remodeling altering, and reproducing our product. Our product cannot be used for the product which is prohibited from being manufactured, used, and sold by the regulations and laws in the world.
We do not warrant or represent that any license, either express or implied, is granted under any our patent right, copyright, mask work right, or our other intellectual property right relating to any combination, machine, or process in which our products or services are used. Information provided by us regarding third-party products or services does not constitute a license from us to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from us under our patents or other intellectual property.
Please do not use our products, our technical information and other data provided by us for the purpose of developing of mass-destruction weapons and the purpose of military use.
Moreover, you must comply with "foreign exchange and foreign trade law", the "U.S. export administration regulations", etc.
Please note that we may discontinue the manufacture of our products, due to reasons such as end of supply of materials and/or components from our suppliers.
By signing on specification sheet or approval sheet, you acknowledge that you are the legal representative for your company and that you understand and accept the validity of the contents herein. When you are not able to return the signed version of specification sheet or approval sheet within 30 days from receiving date of specification sheet or approval sheet, it shall be deemed to be your consent on the content of specification sheet or approval sheet. Customer acknowledges that engineering samples may deviate from specifications and may contain defects due to their development status. We reject any liability or product warranty for engineering samples. In particular we disclaim liability for damages caused by

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- deviation or lapse in function of engineering sample,
- improper use of engineering samples.

We disclaim any liability for consequential and incidental damages.
If you can’t agree the above contents, you should inquire our sales.

Single-Chip IEEE 802.11™ b/g/n MAC/Baseband/Radio + SDIO

GENERAL DESCRIPTION

The Broadcom® BCM43362 single-chip device provides the highest level of integration for mobile and handheld wireless systems, featuring integrated IEEE 802.11™ b/g and handheld device class IEEE 802.11n. It includes a 2.4 GHz WLAN CMOS power amplifier (PA) that meets the output power requirements of most handheld systems. An optional external low-noise amplifier (LNA) and external PA are also supported.

Along with the integrated power amplifier, the BCM43362 also includes integrated transmit and receive baluns, further reducing the overall solution cost.

Host interface options include SDIO v2.0 that can operate in 4b or 1b modes, and a generic gSPI mode.

Utilizing advanced design techniques and process technology to reduce active and idle power, the BCM43362 is designed to address the needs of highly mobile devices that require minimal power consumption and compact size. It includes a power management unit that simplifies the system power topology and allows for operation directly from a rechargeable mobile platform battery while maximizing battery life.

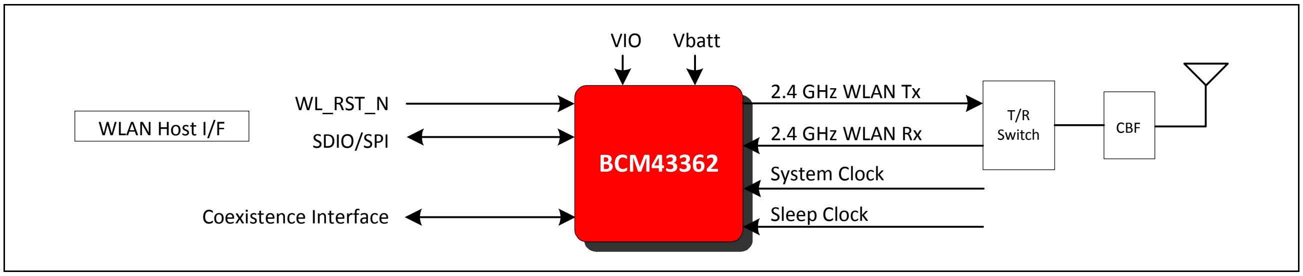
- Programmable dynamic power management
- Supports battery voltage range from 2.3V to 4.8V supplies with internal switching regulator
- 1 kbit One-Time Programmable (OTP) memory for storing board parameters

FEATURES

- Single-band 2.4 GHz IEEE 802.11 b/g/n
- Integrated WLAN CMOS power amplifier with internal power detector and closed-loop power control
- Internal fractional-N PLL enables the use of a wide range of reference clock frequencies
- Supports IEEE 802.15.2 external 3-wire and 4-wire coexistence schemes to optimize bandwidth utilization with other co-located wireless technologies such as Bluetooth, Zigbee, or BT Smart.
- Supports standard interfaces SDIO v2.0 (50 MHz, 4-bit and 1-bit) and generic SPI (up to 50 MHz)
- Integrated ARM Cortex™-M3 CPU with on-chip memory enables running IEEE 802.11 firmware that can be field-upgraded with future features.
- Supports WMM®, WMM-PS, and Wi-Fi Voice Personal (upgradable to Voice Enterprise in the future)
- Security:
  - Hardware WAPI acceleration engine
  - AES and TKIP in hardware for faster data encryption and IEEE 802.11i compatibility
  - WPA™- and WPA2™- (Personal) support for powerful encryption and authentication

- 69-bump WLBGA (4.52 mm x 2.92 mm, 0.4 mm pitch)

Figure 1: BCM43362 System Block Diagram



BROADCOM.
MASS MARKET
PLATFORM

MMP43362-DS100-D1

5300 California Avenue • Irvine, CA 92617 • Phone: 949-926-5000 • Fax: 949-926-5203

February 13, 2015

Revision History

Revision	*Date*	*Change Description*
MMP43362-DS101-R	02/13/15	**Updated:** • Removed “Preliminary” from the document type.
MMP43362-DS100-R	04/07/14	Initial release

Broadcom Corporation
5300 California Avenue
Irvine, CA 92617

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About This Document

Purpose and Audience

This document provides engineering design information for the BCM43362, a single chip with an integrated 2.4 GHz RF transceiver, MAC, and baseband processor that fully supports the IEEE 802.11™ b/g/n standards.

The information provided is intended for hardware design engineers who will be incorporating the BCM43362 into their designs.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

Document Conventions

The following conventions may be used in this document:

Convention	*Description*
Bold	User input and actions: for example, type **exit**, click **OK,** press **Alt+C**
`Monospace`	Code: `#include <iostream>` HTML: `<td rowspan = 3>` Command line commands and parameters: `wl [-l] <command>`
< >	Placeholders for *required* elements: enter your <username> or `wl <command>`
[ ]	Indicates *optional* command-line parameters: `wl [-l]` Indicates bit and byte ranges (inclusive): [0:3] or [7:0]

References

The references in this section may be used in conjunction with this document.

Note: Broadcom provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads & Support site (see Technical Support).

For Broadcom documents, replace the “xx” in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	*Number*	*Source*
Broadcom Items		
[1] BCM43362 reference board schematics	–	Broadcom Representative

Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (https://support.broadcom.com). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads & Support site (http://www.broadcom.com/support/).

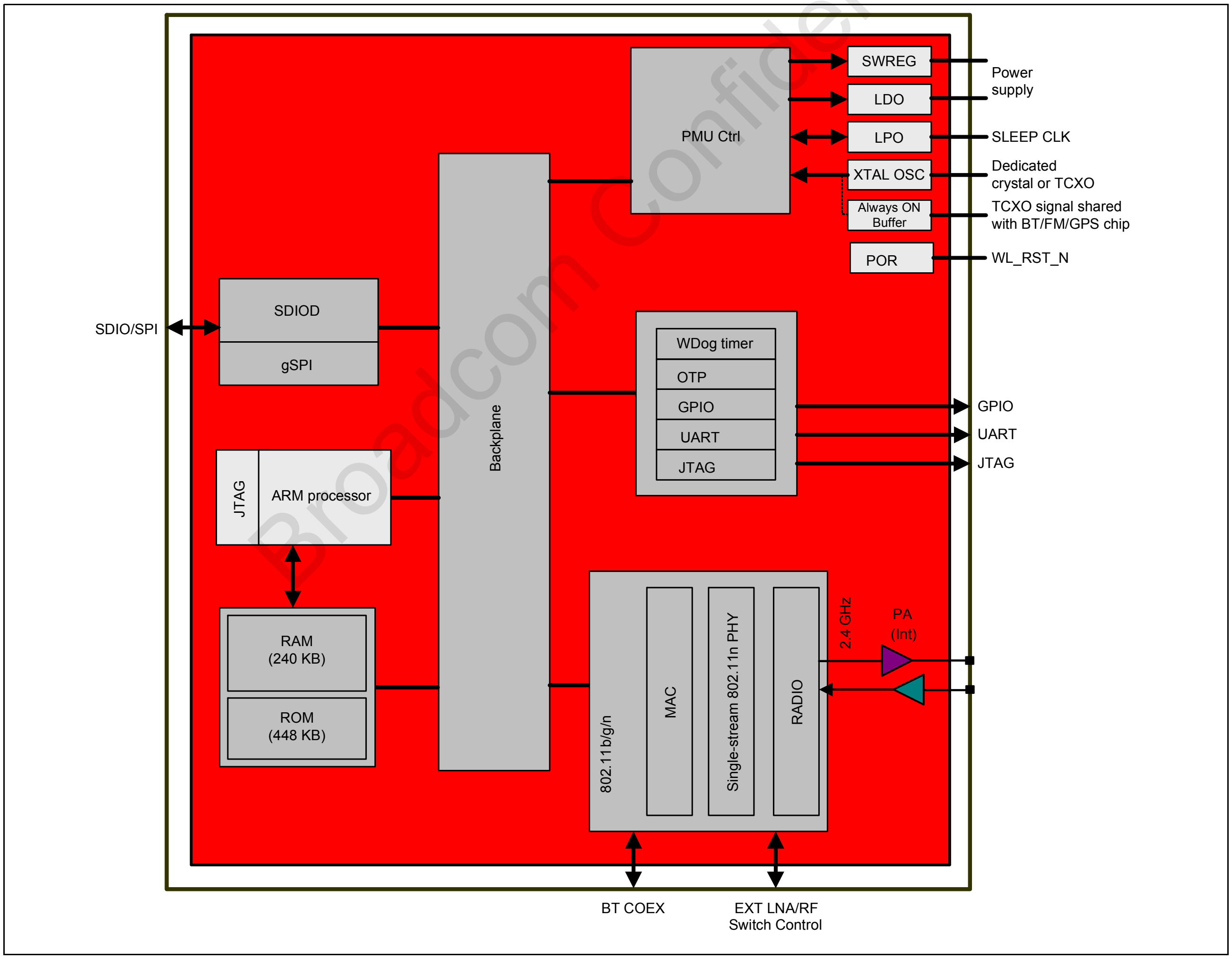
Section 1: Overview

Overview

The Broadcom® BCM43362 provides the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.11 b/g/n. It provides a small form-factor solution with minimal external components to drive down cost for mass volumes and allows for handheld device flexibility in size, form, and function. The BCM43362 is designed to address the needs of highly mobile devices that require minimal power consumption and reliable operation.

Figure 2 shows the interconnect of all the major physical blocks in the BCM43362 and their associated external interfaces, which are described in greater detail in the following sections.

Figure 2: BCM43362 Block Diagram



Standards Compliance

The BCM43362 supports the following standards:

- IEEE 802.11n
- 802.11b
- 802.11g
- 802.11d
- 802.11h
- 802.11i
- 802.11j

The BCM43362 will support the following future drafts/standards:

- 802.11w—Secure Management Frames
- 802.11 Extensions:
  - WMM®
  - 802.11i MAC Enhancements
  - 802.11r Fast Roaming Support (between APs)
  - 802.11k Radio Resource Measurement
- Security:
  - WEP
  - WAPI
  - WPA™ Personal
  - WPA2™ Personal
  - AES (Hardware Accelerator)
  - TKIP (HW Accelerator)
  - CKIP (SW Support)
- QOS Protocols:
  - WMM
  - WWM-PS (U-APSD)
  - WWM-SA
- Proprietary Protocols:
  - WFAEC
- Coexistence Interfaces:
  - Supports IEEE 802.15.2 external three-wire coexistence scheme to support additional wireless technologies, such as Bluetooth, Zigbee, or BT Smart.

Section 2: Power Supplies and Power Management

WLAN Power Management

The BCM43362 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the BCM43362 integrated RAM is a low-leakage memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only.

Additionally, the BCM43362 includes an advanced WLAN power management unit (PMU) sequencer. The PMU sequencer provides significant power savings by putting the BCM43362 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters, which run on the 32.768 kHz low-power oscillator (LPO) sleep clock in the PMU sequencer, are used to turn individual regulators and power switches on and off. Clock speeds are dynamically changed, or gated off, as appropriate for the current mode. Slower clock speeds are used wherever possible.

The BCM43362 power states are described as follows:

- Active mode—All components in the BCM43362 are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode (PWM or Burst) based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- Sleep mode—The radio, AFE, PLLs, and the crystal oscillator are powered down. The rest of the BCM43362 remains powered up in an IDLE state. All main clocks are shut down. The 32.768-kHz LPO sleep clock is available only for the PMU sequencer. This condition is necessary to allow the PMU sequencer to wake up the chip and transition to Active mode. In Sleep mode, the primary power consumed is due to leakage current.
- Power-down modes—The BCM43362 has a full power-down mode and a low-power shutdown mode. A full power-down occurs when there is no VIO voltage, and WL_RST_N and EXT_SMPRS_REQ are low. A low-power shutdown occurs when VIO is present, and WL_RST_N and EXT_SMPRS_REQ are low. In low-power shutdown, only the band gap and LDO3P3 are on. Both power-down modes are exited when the host asserts either WL_RST_N or EXT_SMPS_REQ high.
- External mode—In this mode, the following are true:
  - The assertion of EXT_SMPS_REQ turns only the Core Buck (CBUCK) regulator on.
  - The WLAN is in reset (WL_RST_N = low).
  - The state of LDO3P3 and the band gap are dependent on VBAT and VIO.

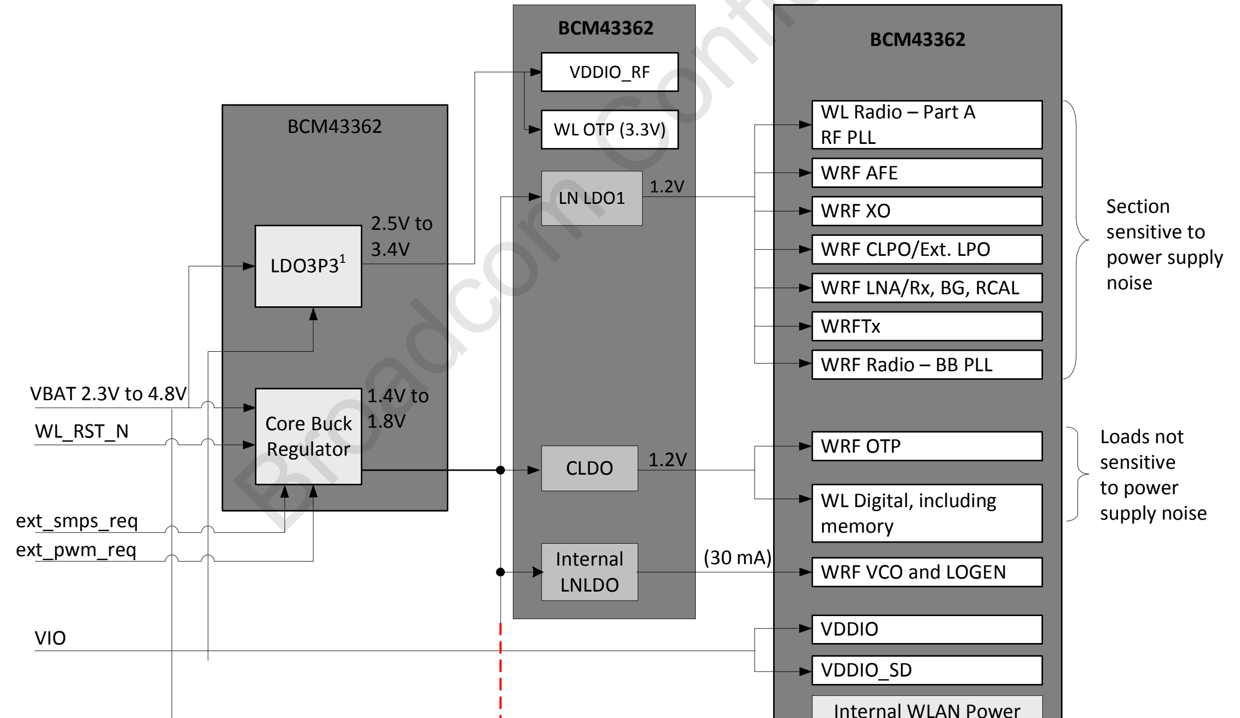
Power Supply Topology

The BCM43362 contains a Power Management Unit (PMU), a buck-mode switching regulator, and three low noise LDOs. These integrated regulators simplify power supply design in WLAN embedded designs. All regulator inputs and outputs are brought out to pins on the BCM43362, providing system designers with the flexibility to choose which of the BCM43362 integrated regulators to use. One option is to supply the PMU from a single, variable power supply, VBAT, which can range from 2.3V to 4.8V. Using this option, all of the required voltages are provided by BCM43362 regulators except for a low current rail, VIO, which must be provided by the host to power the I/O signal buffers when the chip is out of reset.

Alternately, if specific rails such as 3.3V, 1.8V, and 1.2V already exist in the system, appropriate regulators in the BCM43362 can be bypassed, thereby reducing the cost and board space associated with external regulator components such as inductors and large capacitors.

The CBUCK and CLDO get powered whenever the reset signal is deasserted. The CBUCK regulator can be turned ON by asserting EXT_SMPS_REQ high. Asserting EXT_PWM_REQ high will set CBUCK to PWM mode. Driving EXT_PWM_REQ low will put CBUCK in Burst mode. Optionally, LNLDO may also be powered. All regulators are powered down only when the reset signal is asserted.

Figure 3: Power Topology



Notes:
1. LDO3P3 is always enabled when VIO is present in order to provide bias for VDDIO_RF and the external RF switch.
2. Areas in dark gray are internal to the BCM43362.
3. VDDIO and VDDIO_SD can be powered from separate supplies if SDIO signaling needs to be at a different level than VDDIO. This diagram shows the more common case where VDDIO and VDDIO_SD are powered from the same supply.

Voltage Regulators

All BCM43362 regulator output voltages are PMU programmable and have the following nominal capabilities. The currents listed below indicate regulator capabilities. See "System Power Consumption" on page 73 for the actual expected loads.

- Core Buck switching regulator (CBUCK): 2.3–4.8V input, nominal 1.5V output (up to 500 mA).
- LDO3P3: 2.3–4.8V input, nominal 3.3V output (up to 40 mA)
- CLDO (for the core): 1.45–2.0V input, nominal 1.2V output (up to 150 mA)
- Low-noise LNLDO1: 1.45–2.0V input, nominal 1.2V output (up to 150 mA)

See "Internal Regulator Electrical Specifications" on page 67 for full regulator specifications.

PMU Sequencing

The WLAN PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Resource requests come from several sources: clock requests from cores, the minimum resources defined in the ResourceMin register, and the resources requested by any active resource request timers. The PMU sequencer maps clock requests into a set of resources required to produce the requested clocks.

Each resource is in one of four states: enabled, disabled, transition_on, and transition_off. Each resource has a timer that contains 0 when the resource is enabled or disabled and a nonzero value in the transition states. The timer is loaded with the resource's time_on or time_off value when the PMU determines that the resource must be enabled or disabled. That timer decrements on each LPO sleep clock. When it reaches 0, the state changes from transition_off to disabled or transition_on to enabled. If the time_on value is 0, the resource can go immediately from disabled to enabled. Similarly, a time_off value of 0 indicates that the resource can go immediately from enabled to disabled. The terms enable sequence and disable sequence refer to either the immediate transition or the timer load-decrement sequence.

During each clock cycle, the PMU sequencer performs the following actions:

1. Computes the required resource set based on requests and the resource dependency table.
2. Decrements all timers whose values are nonzero. If a timer reaches 0, the PMU clears the ResourcePending bit for the resource and inverts the ResourceState bit.
3. Compares the request with the current resource status and determines which resources must be enabled or disabled.
4. Initiates a disable sequence for each resource that is enabled, no longer being requested, and has no powered-up dependents.
5. Initiates an enable sequence for each resource that is disabled, is being requested, and has all of its dependencies enabled.

Low-Power Shutdown

The BCM43362 provides a low-power shutdown feature that allows the device to be turned off while the host, and any other device in the system, remain operational. When WLAN is not needed, the WLAN core can be put in reset by asserting WL_RST_N (logic LOW). VDDIO_RF and VDDIO remain powered while VIO and VBAT are both present, allowing the BCM43362 to be effectively off while keeping the I/O pins powered. During a low-power shut-down state, provided VIO continues to be supplied to the BCM43362, most outputs are tristated and most inputs are disabled. Input voltages must remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system, enabling the BCM43362 to be a fully integrated embedded device that takes full advantage of the lowest power-saving modes.

Two signals on the BCM43362, the system clock input (OSCIN) and sleep clock input (EXT_SLEEP_CLK), are designed to be high-impedance inputs that do not load down the driving signal even if the BCM43362 does not have VDDIO power applied to it. When the BCM43362 is powered on from this state, it is the same as a normal power-up, and the device does not contain any information about its state from before it was powered down.

CBUCK Regulator Features

The CBUCK regulator has several features that help make the BCM43362 ideal for mobile devices. First, the regulator uses 3.2 MHz as its PWM switching frequency for Buck regulation. This high frequency allows the use of small passive components for the switcher's external circuit, thereby saving PCB space in the design. In addition, the CBUCK regulator has three modes of operation: PWM mode for low-ripple output and for fast transient response and extended load ranges, Burst Mode for lower currents, and Low Power Burst Mode for higher efficiency when the load current is very low (Low Power Burst mode is not available for external devices).

The CBUCK supports external SMPS request to allow flexibility of supplying 1.8V to BCM43362, BCM2076, and other external devices when EXT_SMPS_REQ is asserted high. It also supports low ripple PWM mode (7 mVpp typical) for noise-sensitive applications when EXT_PWM_REQ is asserted high. A 100 µs wait/settling time from the assertion of EXT_PWM_REQ high before increasing the load current allows the internal integrator precharging to complete. This is not a requirement, but is preferred.

Table 1 lists the mode the CBUCK operates in (Burst or PWM), based on various external control signals and internal CBUCK mode register settings.

Table 1: CBUCK Operating Mode Selection

WL_RST_L	EXT_SMPS_REQ	EXT_PWM_REQ	Internal CBUCK Mode Required	CBUCK Mode
0	0	X	X	Off
0	1	0	X	BURST
0	1	1	X	PWM
1	0	X	BURST	BURST
1	0	X	PWM	PWM
1	1	0	BURST	BURST
1	1	0	PWM	PWM
1	1	1	X	PWM

For detailed CBUCK performance specifications, see "Core Buck Regulator" on page 67.

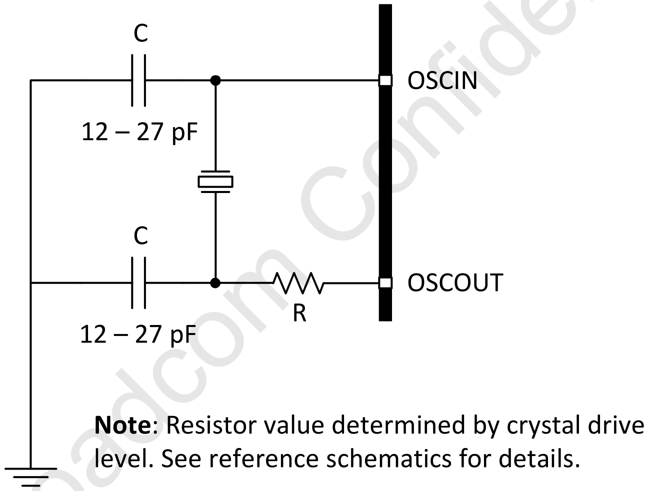
Section 3: Frequency References

An external crystal is used for generating all radio frequencies and normal operation clocking. As an alternative, an external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal may be used. No software settings are required to differentiate between the two. In addition, a low-power oscillator (LPO) is provided for lower power mode timing.

Crystal Interface and Clock Generation

The BCM43362 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator, including all external components, is shown in Figure 4. Consult the reference schematics for the latest configuration.

Figure 4: Recommended Oscillator Configuration



Note: Resistor value determined by crystal drive level. See reference schematics for details.

The BCM43362 uses a fractional-N synthesizer to generate the radio frequencies, clocks, and data/packet timing. This enables it to operate using numerous frequency references. This may either be an external source such as a TCXO or a crystal interfaced directly to the BCM43362.

The default frequency reference setting is a 26 MHz crystal or TCXO. The signal requirements and characteristics for the crystal interface are shown in Table 2 on page 19.

Note: Although the fractional-N synthesizer can support many reference frequencies, frequencies other than the default require support to be added in the driver, plus additional extensive system testing. Contact Broadcom for further details.

TCXO

As an alternative to a crystal, an external precision TCXO can be used as the frequency reference, provided that it meets the Phase Noise requirements listed in Table 2 on page 19. When the clock is provided by an external TCXO, there are two possible connection methods, as shown in Figure 5 and Figure 6:

1. If the TCXO is dedicated to driving the BCM43362, it should be connected to the OSC_IN pin through an external 1000 pF coupling capacitor, as shown in Figure 5. The internal clock buffer connected to this pin will be turned OFF when the BCM43362 goes into sleep mode. When the clock buffer turns ON and OFF, there will be a small impedance variation up to ±15%. Power must be supplied to the WRF_XTAL_VDD1P2 pin.
2. An alternative is to DC-couple the TCXO to the WRF_TCXO_IN pin, as shown in Figure 6. Use this method when the same TCXO is shared with other devices and a change in the input impedance is not acceptable because it may cause a frequency shift that cannot be tolerated by the other device sharing the TCXO. This pin is connected to a clock buffer powered from WRF_TCXO_VDD3P3. If the power supply to this buffer is always on (even in sleep mode), the clock buffer is always on, thereby ensuring a constant input impedance in all states of the device. The maximum current drawn from WRF_TCXO_VDD3P3 is approximately 500 µA.

Figure 5: Recommended Circuit to Use with an External Dedicated TCXO

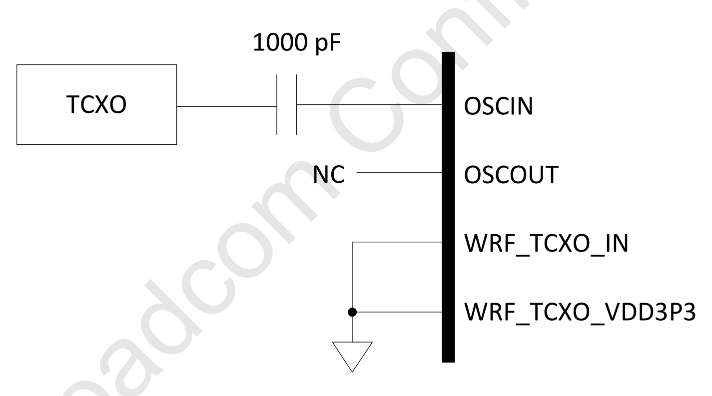


Figure 6: Recommended Circuit to Use with an External Shared TCXO

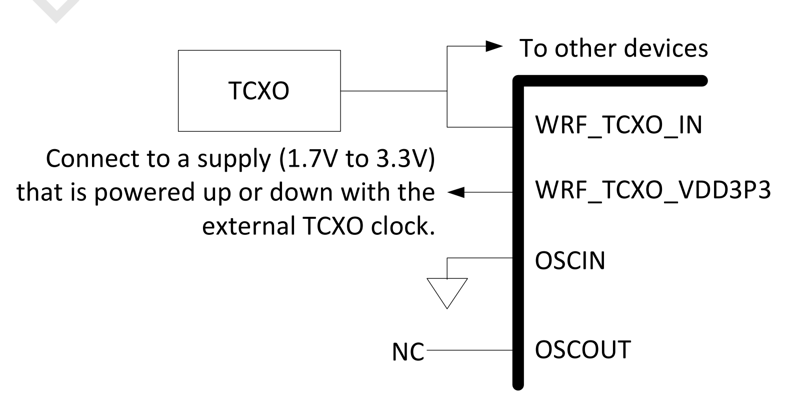


Table 2: Crystal Oscillator and External Clock Requirements and Performance

		Crystal			External Frequency Reference			
Parameter	**Conditions/Notes**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Frequency	–	Between 12 MHz and 52 MHz[a]						
Crystal load capacitance	–	–	12	–				pF
ESR	–	–	–	60				Ω
Input Impedance (OSCIN)[b]	Resistive				30k	100k	–	Ω
	Capacitive				–	–	7.5	pF
Input Impedance (WRF_TCXO_IN)	Resistive				30k	100k	–	Ω
	Capacitive				–	–	4	pF
OSCIN input voltage	AC-coupled analog signal				400	–	1200	mV_{p-p}
OSCIN input low level	DC-coupled digital signal				0	–	0.2	V
OSCIN input high level	DC-coupled digital signal				1.0	–	1.36	V
WRF_TCXO_IN input voltage	DC-coupled analog signal[c]				400	–	TCXO_ VDD[d]	mV_{p-p}
Frequency tolerance Initial + over temperature	–	–20	–	20	–20	–	20	ppm
Duty cycle	26 MHz clock				40	50	60	%
Phase Noise[e, f] (IEEE 802.11 b/g)	26 MHz clock at 1 kHz offset				–	–	–119	dBc/Hz
	26 MHz clock at 10 kHz offset				–	–	–129	dBc/Hz
	26 MHz clock at 100 kHz offset				–	–	–134	dBc/Hz
	26 MHz clock at 1 MHz offset				–	–	–139	dBc/Hz
Phase Noise[e, f] (IEEE 802.11n, 2.4 GHz)	26 MHz clock at 1 kHz offset				–	–	–124	dBc/Hz
	26 MHz clock at 10 kHz offset				–	–	–134	dBc/Hz
	26 MHz clock at 100 kHz offset				–	–	–139	dBc/Hz
	26 MHz clock at 1 MHz offset				–	–	–144	dBc/Hz

a. The frequency step size is approximately 80 Hz. The BCM43362 does not auto-detect the reference clock frequency; the frequency is specified in the software/NVRAM file.

b. The internal clock buffer connected to this pin will be turned off when the BCM43362 goes into Sleep mode. When the clock buffer turns on and off, there will be a small impedance variation up to ±15%.

c. This input has an internal DC blocking capacitor, so do not include an external DC blocking capacitor.

d. The maximum allowable voltage swing for the WRF_TCXO_IN input is equal to the WRF_TCX0_VDD3P3 supply voltage range, which is 1.7V to 3.3V.

e. For a clock reference other than 26 MHz, 20 × log10(f/26) dB should be added to the limits, where f = the reference clock frequency in MHz.

f. If the selected clock has a flat phase-noise response above 100 kHz, then it is acceptable to subtract 1 dB from all 1 kHz, 10 kHz, and 100 kHz values shown, and ignore the 1 MHz requirement.

External 32.768 kHz Low-Power Oscillator

The BCM43362 uses a secondary low-frequency sleep clock for low-power mode timing. Either the internal low-precision LPO or an external 32.768 kHz precision oscillator is required. The internal LPO frequency range is approximately 33 kHz ± 30% over process, voltage, and temperature, which is adequate for some applications. However, one trade-off caused by this wide LPO tolerance is a small current consumption increase during power save mode that is incurred by the need to wake up earlier to avoid missing beacons.

Whenever possible, the preferred approach is to use a precision external 32.768 kHz clock that meets the requirements listed in Table 3.

Note: The BCM43362 will auto-detect the LPO clock. If it senses a clock on the EXT_SLEEP_CLK pin, it will use that clock. If it doesn't sense a clock, it will use its own internal LPO.

- To use the internal LPO: Tie EXT_SLEEP_CLK to ground. Do not leave this pin floating.
- To use an external LPO: Connect the external 32.768 kHz clock to EXT_SLEEP_CLK.

Table 3: External 32.768 kHz Low-Power Oscillator Specifications

			Specification			
Symbol	***Parameter***	***Condition/Notes***	***Minimum***	***Typical***	***Maximum***	***Units***
Fr	Frequency	–	–	32768	–	Hz
∆f/fr	Frequency tolerance	At 25°C	–30	–	+30	ppm
		–20°C <Ta< +70°C	–150	–	+40	
		–30°C <Ta< +85°C	–220	–	+40	
Duty cycle	–	–	30	–	70	%
Vol	Output low voltage	–	0	–	0.2	V
Voh	Output high voltage	–	0.7 Vio	–	Vio	V
Tr/Tf	Rise and fall time	–	–	–	100	ns
–	Signal type	Digital	–	–	–	–
–	Clock jitter	Integrated over 300 Hz to 15 kHz	–	–	30	ns
–	Input impedance	Resistive	10	–	–	MΩ
		Capacitive	–	–	2	pF
–	Input amplitude	Fail safe, 3.3V digital I/O	–	–	3.63	V

Section 4: WLAN System Interfaces

SDIO v2.0

The BCM43362 WLAN section supports SDIO version 2.0. for both 1-bit (25 Mbps), 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks—200 Mbps). It has the ability to map the interrupt signal on a GPIO pin. This out-of-band interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force control of the gated clocks from within the WLAN chip is also provided.

SDIO mode is enabled using the strapping option pins. See Table 10 on page 55 for details.

Three functions are supported:

- Function 0 Standard SDIO function (Max BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize/ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount = 512B)

SDIO Pin Descriptions

Table 4: SDIO Pin Descriptions

SD 4-Bit Mode		SD 1-Bit Mode		gSPI Mode	
DATA0	Data line 0	DATA	Data line	DO	Data output
DATA1	Data line 1 or Interrupt	IRQ	Interrupt	IRQ	Interrupt
DATA2	Data line 2	NC	Not used	NC	Not used
DATA3	Data line 3	NC	Not used	CS	Card select
CLK	Clock	CLK	Clock	SCLK	Clock
CMD	Command line	CMD	Command line	DI	Data input

Figure 7: Signal Connections to SDIO Host (SD 4-Bit Mode)

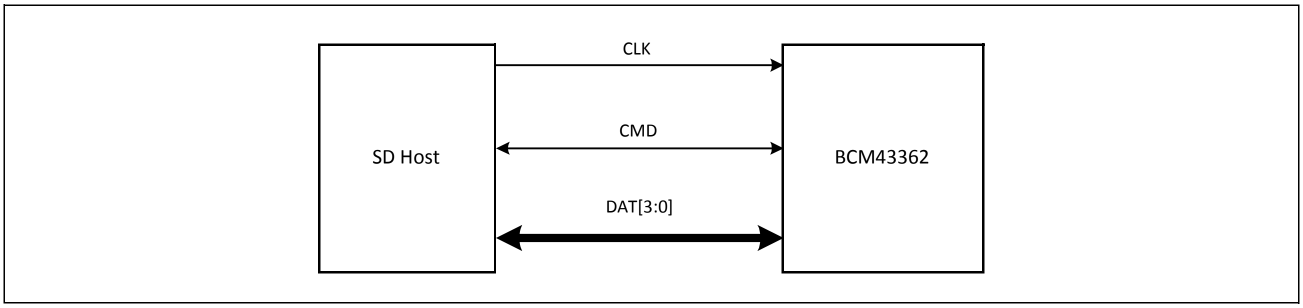
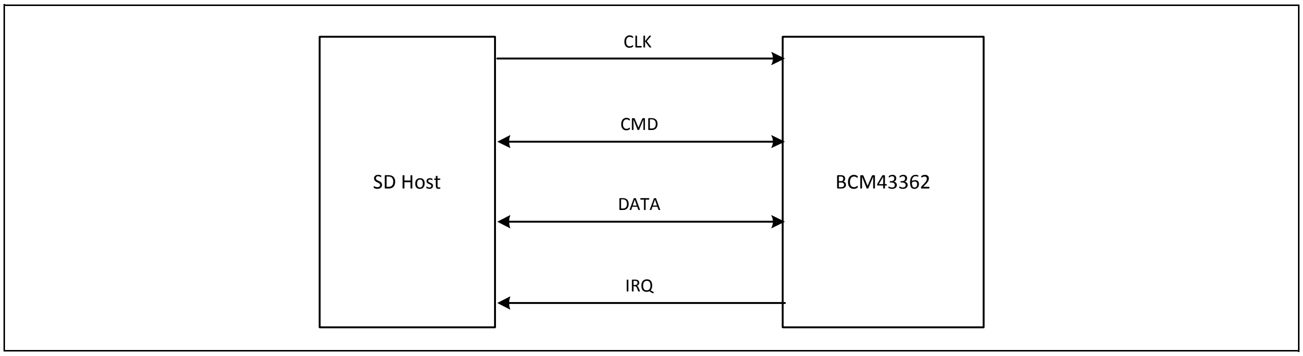


Figure 8: Signal Connections to SDIO Host (SD 1-Bit Mode)



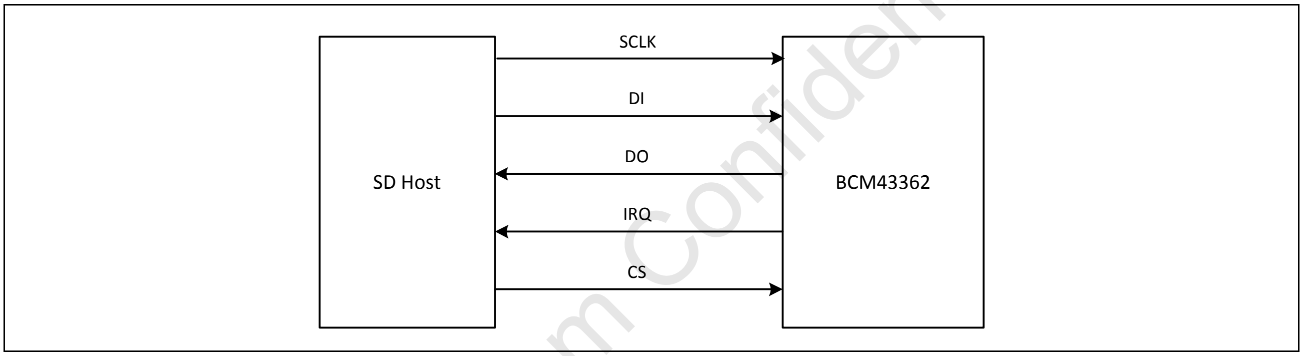
Generic SPI Mode

In addition to the full SDIO mode, the BCM43362 includes the option of using the simplified generic SPI (gSPI) interface/protocol. Characteristics of the gSPI mode include:

- Supports up to 50 MHz operation
- Supports fixed delays for responses and data from device
- Supports alignment to host gSPI frames (16 or 32 bits)
- Supports up to 2 KB frame size per transfer
- Supports little-endian and big-endian configurations
- Supports configurable active edge for shifting
- Supports packet transfer through DMA for WLAN

gSPI mode is enabled using the strapping option pins. See Table 10 on page 55 for details.

Figure 9: Signal Connections to SDIO Host (gSPI Mode)



SPI Protocol

The SPI protocol supports both 16-bit and 32-bit word operation. Byte endianess is supported in both modes. Figure 10 and Figure 11 show the basic write and write/read commands.

Figure 10: gSPI Write Protocol

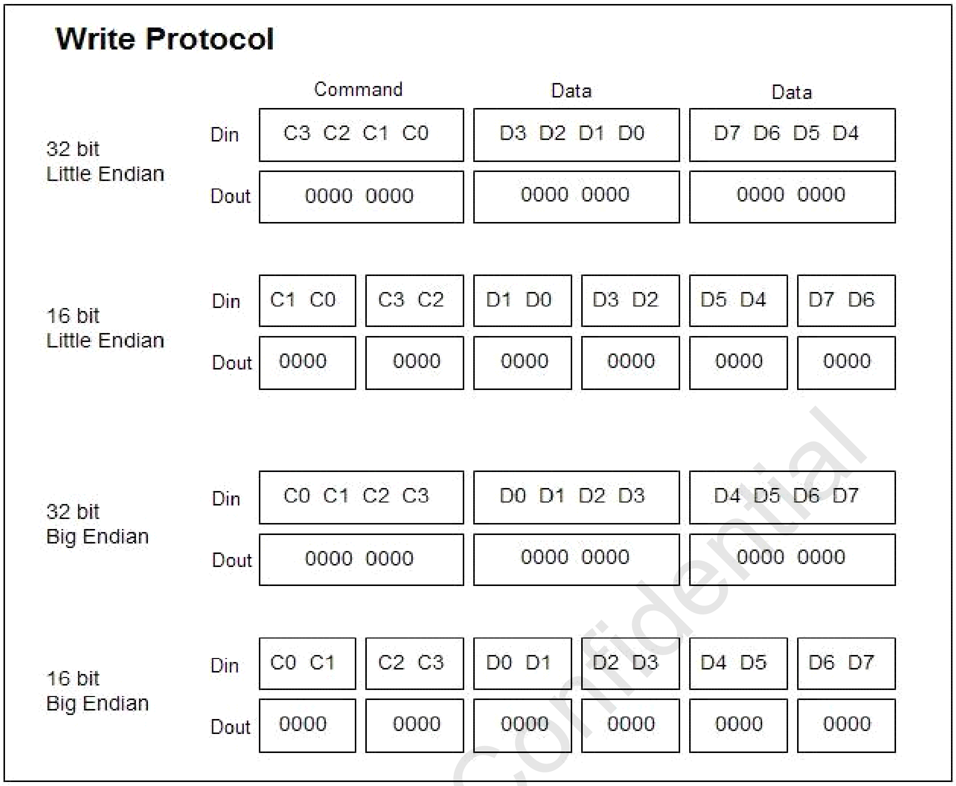
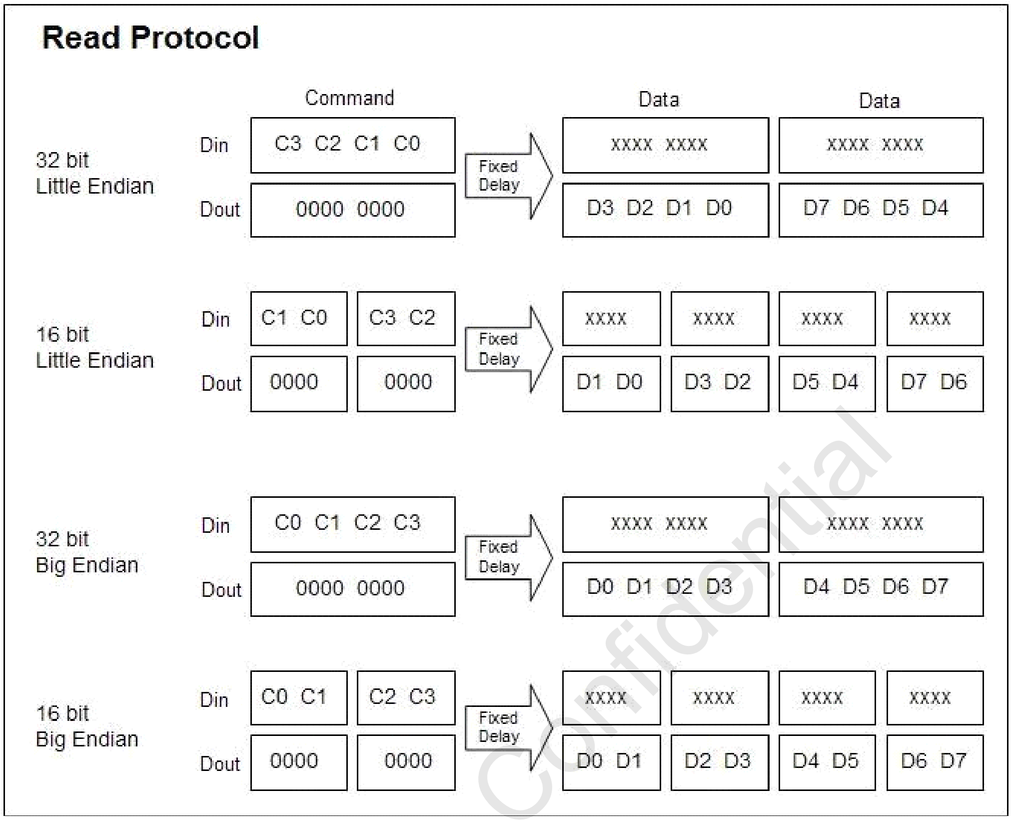


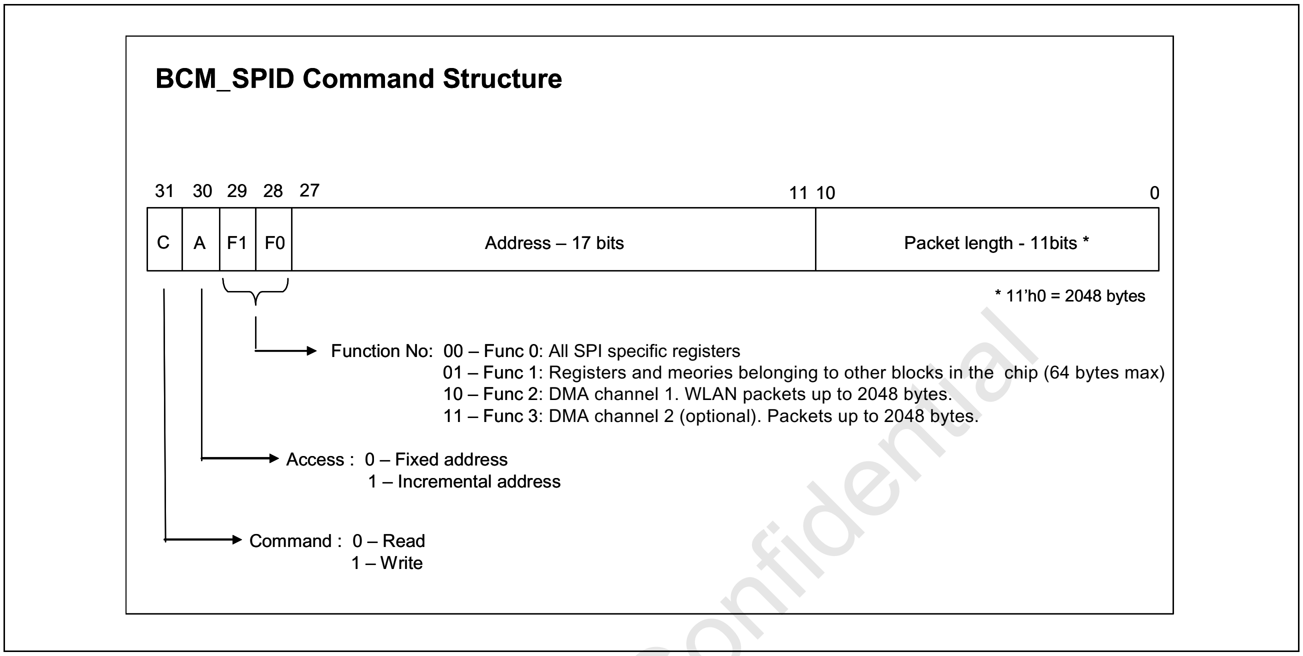
Figure 11: gSPI Read Protocol



Command Structure

The gSPI command structure is 32 bits. The bit positions and definitions are as shown in Figure 12.

Figure 12: gSPI Command Structure



Write

The host puts the first bit of the data onto the bus half a clock-cycle before the first active edge following the CS going low. The following bits are clocked out on the falling edge of the gSPI clock. The device samples the data on the active edge.

Write/Read

The host reads on the rising edge of the clock requiring data from the device to be made available before the first rising clock edge of the clock burst for the data. The last clock edge of the fixed delay word can be used to represent the first bit of the following data word. This allows data to be ready for the first clock edge without relying on asynchronous delays.

Read

The read command always follows a separate write to set up the WLAN device for a read. This command differs from the write/read command in the following respects: a) chip selects go high between the command/address and the data and b) the time interval between the command/address is not fixed.

Status

The gSPI interface supports status notification to the host after a read/write transaction. This status notification provides information about any packet errors, protocol errors, information about available packet in the RX queue, etc. The status information helps in reducing the number of interrupts to the host. The status-reporting feature can be switched off using a register bit, without any timing overhead. The gSPI bus timing for read/write transactions with and without status notification are as shown in Figure 13 below and Figure 14 on page 28. See Table 5 on page 28 for information on status field details.

Figure 13: gSPI Signal Timing Without Status

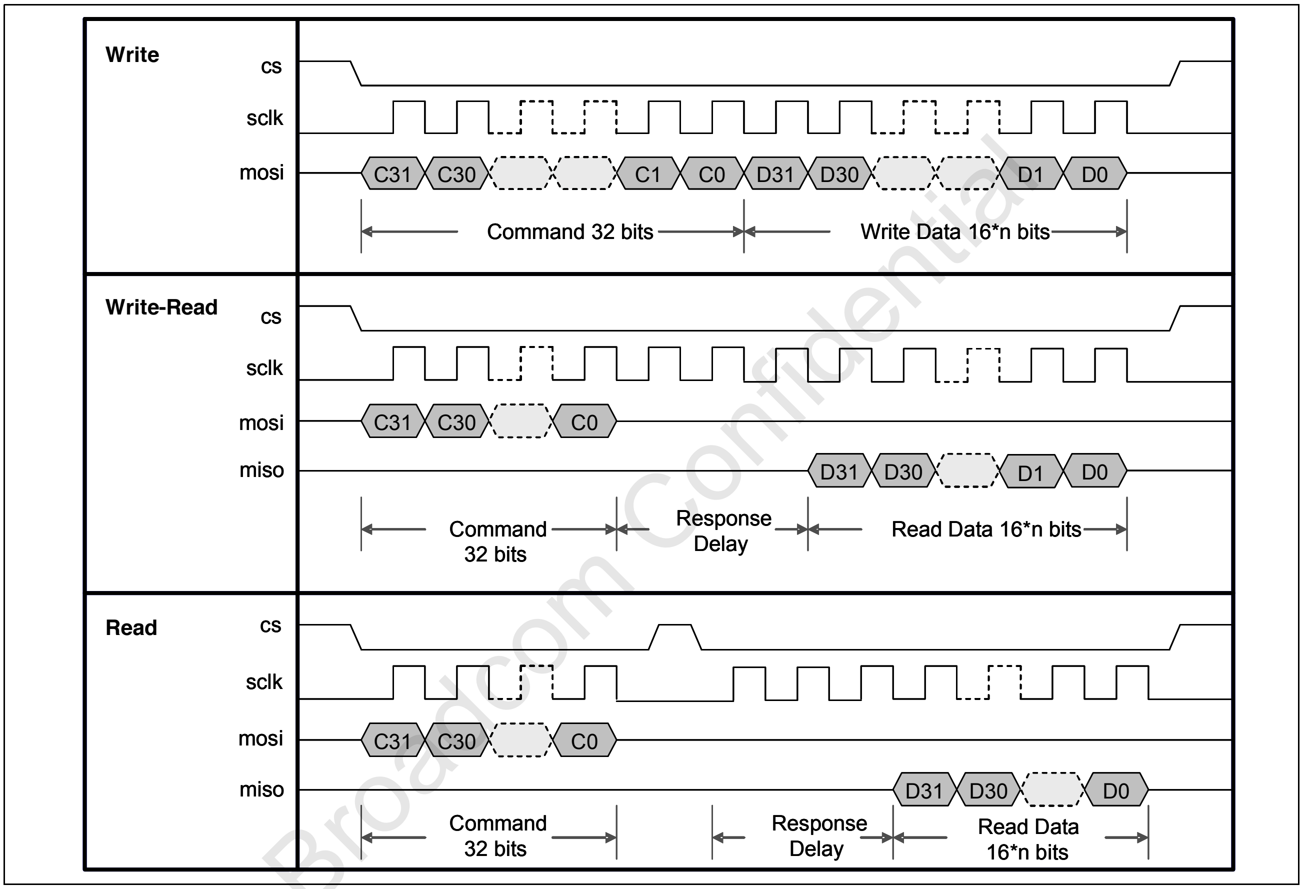


Figure 14: gSPI Signal Timing with Status (Response Delay = 0)

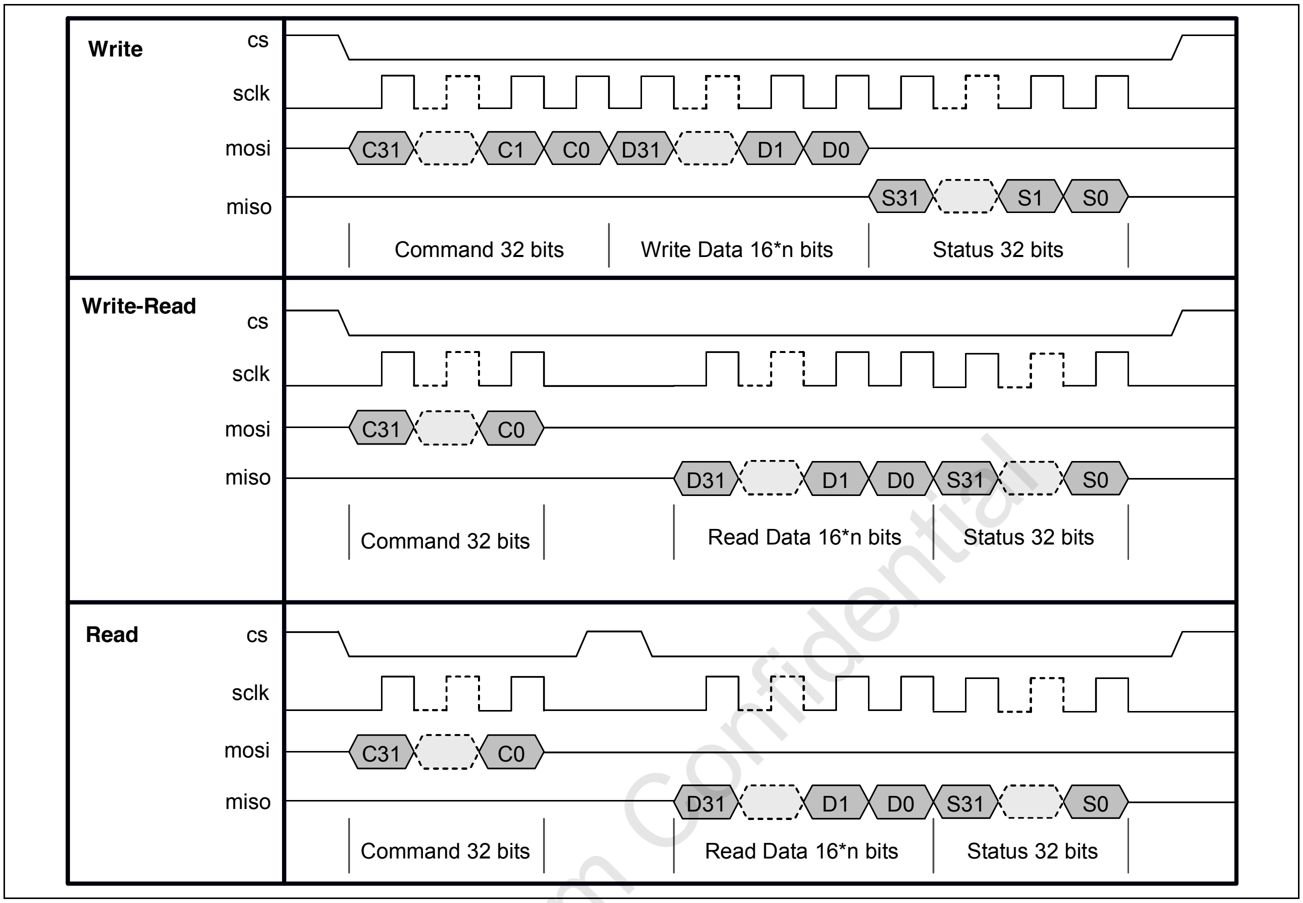


Table 5: gSPI Status Field Details

Bit	***Name***	***Description***
0	Data not available	The requested read data is not available.
1	Underflow	FIFO underflow occurred due to current (F2, F3) read command.
2	Overflow	FIFO overflow occurred due to current (F1, F2, F3) write command.
3	F2 interrupt	F2 channel interrupt
5	F2 RX Ready	F2 FIFO is ready to receive data (FIFO empty).
7	Reserved	–
8	F2 Packet Available	Packet is available/ready in F2 TX FIFO.
9:19	F2 Packet Length	Length of packet available in F2 FIFO

gSPI Host-Device Handshake

To initiate communication through the gSPI after power-up, the host needs to bring up the WLAN/Chip by writing to the wake-up WLAN register bit. Writing a 1 to this bit will start up the necessary crystals and PLLs so that the BCM43362 is ready for data transfer. The device can signal an interrupt to the host indicating that the device is awake and ready. This procedure also needs to be followed for waking up the device in sleep mode. The device can interrupt the host using the WLAN IRQ line whenever it has any information to pass to the host. On getting an interrupt, the host needs to read the interrupt and/or status register to determine the cause of interrupt and then take necessary actions.

Boot-Up Sequence

After power-up, the gSPI host needs to wait 50 ms for the device to be out of reset. For this, the host needs to poll with a read command to F0 addr 0x14. Address 0x14 contains a predefined bit pattern. As soon as the host gets a response back with the correct register content, it implies that the device has powered up and is out of reset. After that, the host needs to set the wakeup-WLAN bit (F0 reg 0x00 bit 7). Wakeup-WLAN turns the PLL on; however, the PLL doesn't lock until the host programs the PLL registers to set the crystal frequency.

For the first time after power-up, the host needs to wait for the availability of low-power clock inside the device. Once that is available, the host needs to write to a PMU register to set the crystal frequency. This will turn on the PLL. After the PLL is locked, the chipActive interrupt is issued to the host. This indicates device awake/ready status. See Table 6 for information on gSPI registers.

In Table 6, the following notation is used for register access:

- R: Readable from host and CPU
- W: Writable from host
- U: Writable from CPU

Table 6: gSPI Registers

Address	Register	Bit	Access	Default	Description
x0000	Word length	0	R/W/U	0	0: 16-bit word length 1: 32-bit word length
	Endianess	1	R/W/U	0	0: Little Endian 1: Big Endian
	High-speed mode	4	R/W/U	1	0: Normal mode. Sample on SPICLK rising edge, output on falling edge. 1: High-speed mode. Sample and output on rising edge of SPICLK (default).
	Interrupt polarity	5	R/W/U	1	0: Interrupt active polarity is low. 1: Interrupt active polarity is high (default).
	Wake-up	7	R/W	0	A write of 1 will denote wake-up command from host to device. This will be followed by a F2 Interrupt from gSPI device to host, indicating device awake status.

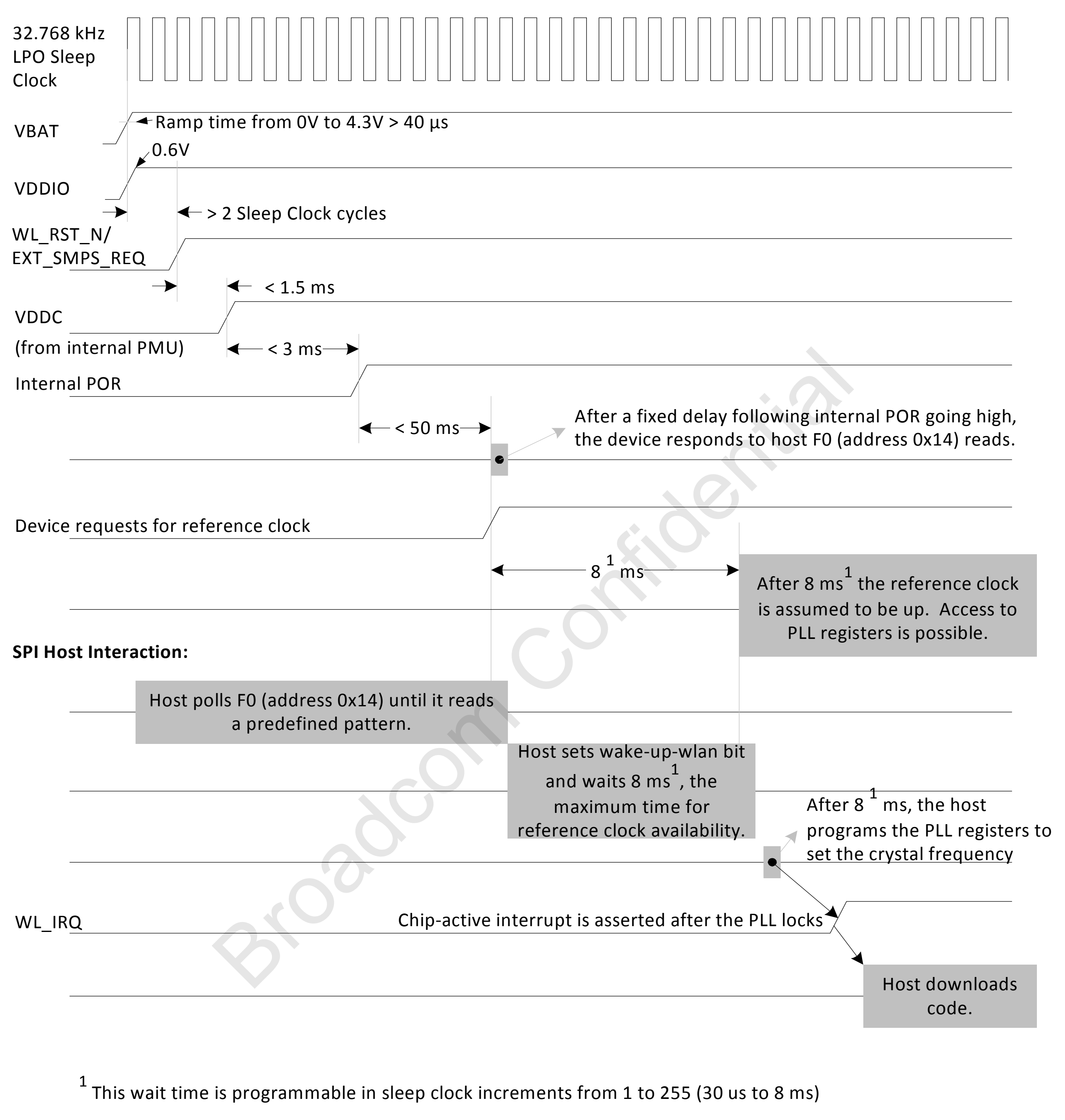
Table 6: gSPI Registers (Cont.)

Address	Register	Bit	Access	Default	Description
x0002	Status enable	0	R/W	1	0: no status sent to host after read/write 1: status sent to host after read/write
	Interrupt with status	1	R/W	0	0: do not interrupt if status is sent 1: interrupt host even if status is sent
x0003	Reserved	–	–	–	–
x0004	Interrupt register	0	R/W	0	Requested data not available; Cleared by writing a 1 to this location
		1	R	0	F2/F3 FIFO underflow due to last read
		2	R	0	F2/F3 FIFO overflow due to last write
		5	R	0	F2 packet available
		6	R	0	F3 packet available
		7	R	0	F1 overflow due to last write
x0005	Interrupt register	5	R	0	F1 Interrupt
		6	R	0	F2 Interrupt
		7	R	0	F3 Interrupt
x0006, x0007	Interrupt enable register	15:0	R/W/U	16'hE0E7	Particular Interrupt is enabled if a corresponding bit is set
x0008 to x000B	Status register	31:0	R	32'h0000	Same as status bit definitions
x000C, x000D	F1 info register	0	R	1	F1 enabled
		1	R	0	F1 ready for data transfer
		13:2	R/U	12'h40	F1 max packet size
x000E, x000F	F2 info register	0	R/U	1	F2 enabled
		1	R	0	F2 ready for data transfer
		15:2	R/U	14'h800	F2 max packet size
x0014 to x0017	Test–Read only register	31:0	R	32'hFEEDBEAD	This register contains a predefined pattern, which the host can read and determine if the gSPI interface is working properly.
x0018 to x001B	Test–R/W register	31:0	R/W/U	32'h00000000	This is a dummy register where the host can write some pattern and read it back to determine if the gSPI interface is working properly.
x001C to x001F	Response delay registers	7:0	R/W	0x1D = 4, other registers = 0	Individual response delays for F0, F1, F2, and F3. The value of the registers is the number of byte delays that are introduced before data is shifted out of the gSPI interface during host reads.

Figure 15 on page 31 shows the WLAN boot-up sequence from power-up to firmware download, including the initial device power-on reset (POR) evoked by the WL_RST_N signal. After initial power-up, the WL_RST_N signal can be held low to disable the BCM43362 or pulsed low to induce a subsequent reset.

Note: The BCM43362 has an internal power-on reset (POR) circuit. The device will be held in reset for a maximum of 3 ms after VDD and VDDIO have both passed the 0.6V threshold.

Figure 15: WLAN Boot-Up Sequence



External Coexistence Interface

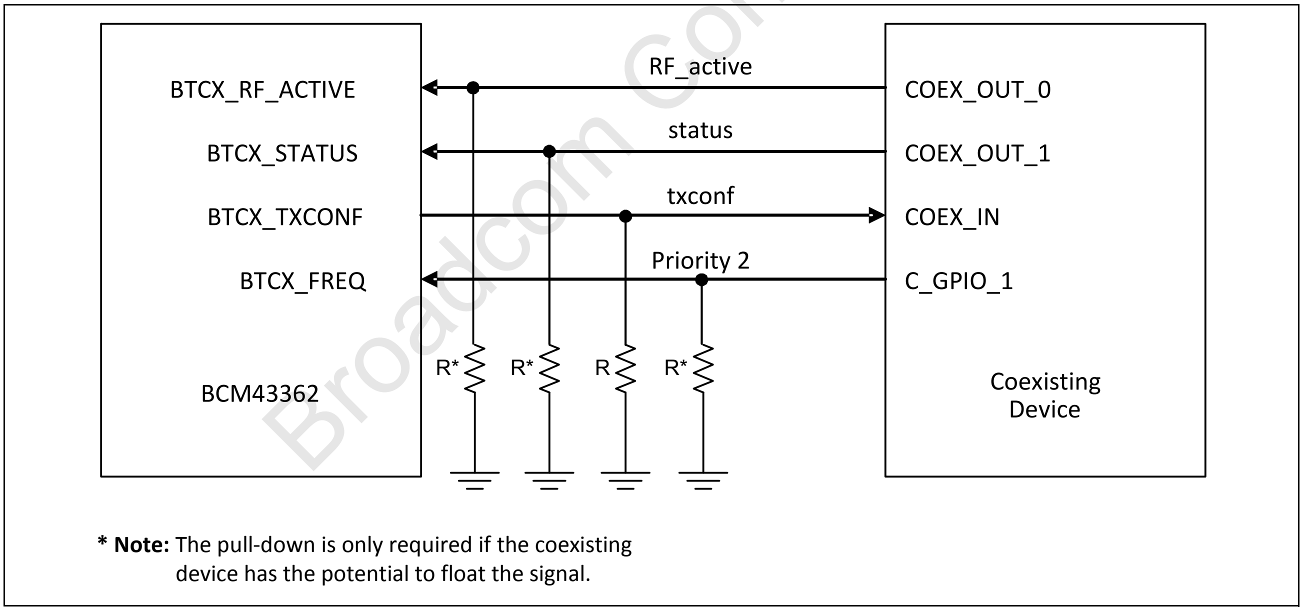
To manage wireless medium sharing for optimal performance, an external coexistence interface is provided that enables signaling between the BCM43362 and one or two external collocated wireless devices such as Bluetooth and/or WiMax. Note that three of the External Coexistence Interface pins are multiplexed with GPIOs. By default, the pins are BT_COEX pins. Through software they can be changed to GPIOs. The fourth BT_COEX signal is also multiplexed with a GPIO, but this one is a GPIO by default and can be changed via software to be BTCX_FREQ. See "Pinout and Signal Descriptions" on page 46 for more details.

The signals in Table 7 can be enabled by software.

Table 7: Coexistence Signals

Signal	***Description***
BTCX_STATUS	Coexistence signal indicating Bluetooth priority status and TX/RX direction.
BTCX_RF_ACTIVE	Coexistence signal indicating that Bluetooth is active.
BTCX_FREQ	Indicates that the coexisting Bluetooth is about to transmit on a restricted channel.
BTCX_TXCONF	Coexistence output giving Bluetooth permission to transmit.

Figure 16: 4-Wire Coexistence Wiring



*** Note:** The pull-down is only required if the coexisting device has the potential to float the signal.

Section 5: Wireless LAN MAC and PHY

MAC Features

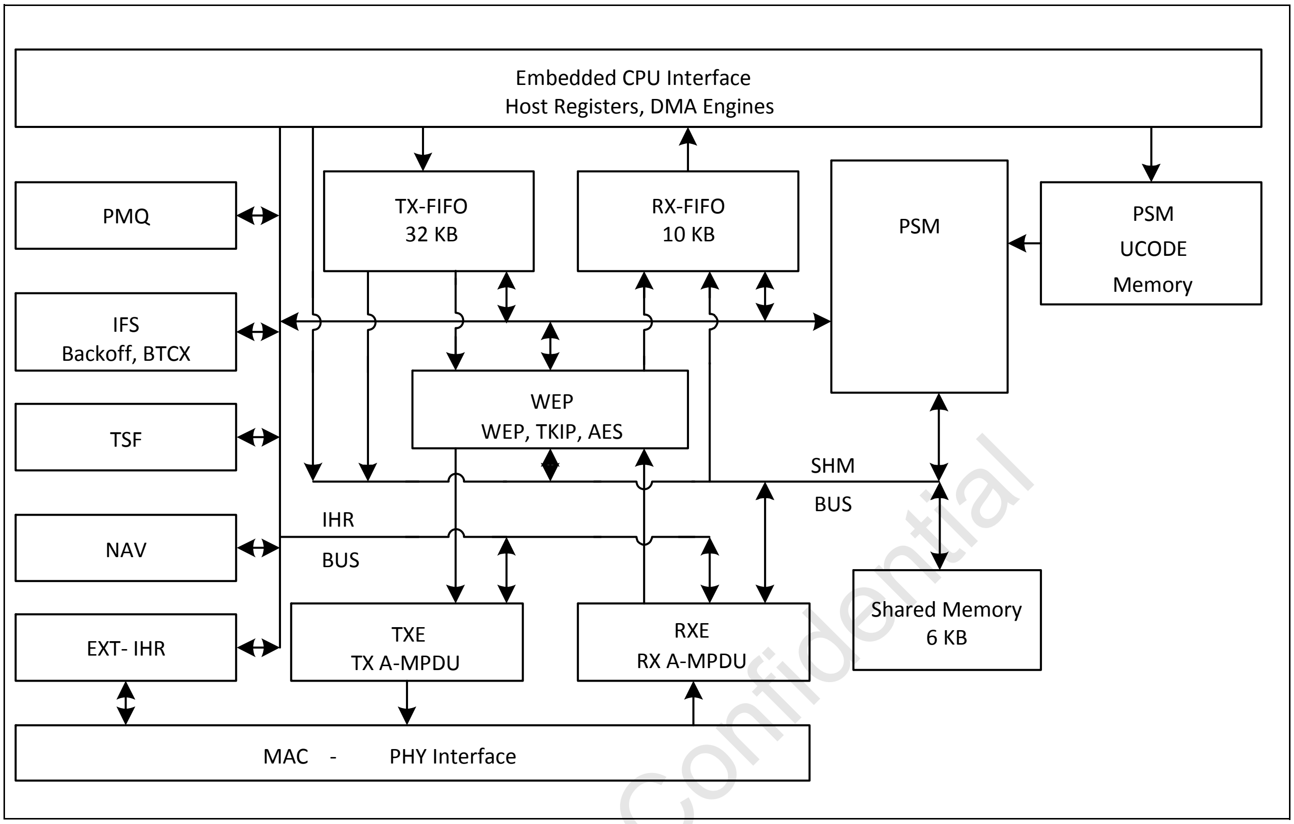
The BCM43362 WLAN MAC supports features specified in the IEEE 802.11 base standard, and amended by IEEE 802.11n. The salient features are listed below:

- Transmission and reception of aggregated MPDUs (A-MPDU)
- Support for power management schemes, including WMM power-save, power-save multipoll (PSMP) and multiphase PSMP operation.
- Support for immediate ACK and Block-ACK policies
- Interframe space timing support, including RIFS
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges
- Back-off counters in hardware for supporting multiple priorities as specified in the WMM specification
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware
- Hardware off-load for AES-CCMP, legacy WPA TKIP, legacy WEP ciphers, WAPI, and support for key management
- Support for coexistence with Bluetooth and other external radios
- Programmable independent basic service set (IBSS) or infrastructure basic service set functionality
- Statistics counters for MIB support

MAC Description

The BCM43362 WLAN MAC is designed to support high throughput operation with low-power consumption. It does so without compromising on Bluetooth coexistence policies, thereby enabling optimal performance over both networks. In addition, several power-saving modes that have been implemented allow the MAC to consume very little power while maintaining network-wide timing synchronization. The architecture diagram of the MAC is shown in Figure 17 on page 34.

Figure 17: WLAN MAC Architecture



The following sections provide an overview of the important modules in the MAC.

PSM

The programmable state machine (PSM) is a microcoded engine that provides most of the low-level control to the hardware to implement the IEEE 802.11 specification. It is a microcontroller that is highly optimized for flow control operations, which are predominant in implementations of communication protocols. The instruction set and fundamental operations are simple and general, which allows algorithms to be optimized until very late in the design process. It also allows for changes to the algorithms to track evolving IEEE 802.11 specifications.

The PSM fetches instructions from the microcode memory. It uses the shared memory to obtain operands for instructions, as a data store, and to exchange data between both the host and the MAC data pipeline (via the SHM bus). The PSM also uses a scratchpad memory (similar to a register bank) to store frequently accessed and temporary variables.

The PSM exercises fine-grained control over the hardware engines by programming internal hardware registers (IHR). These IHRs are collocated with the hardware functions they control and are accessed by the PSM via the IHR bus.

The PSM fetches instructions from the microcode memory using an address determined by the program counter, instruction literal, or a program stack. For ALU operations, the operands are obtained from shared memory, scratchpad, IHRs, or instruction literals, and the results are written into the shared memory, scratchpad, or IHRs.

There are two basic branch instructions: conditional branches and ALU based branches. To better support the many decision points in the IEEE 802.11 algorithms, branches can depend on either a readily available signals from the hardware modules (branch condition signals are available to the PSM without polling the IHRs), or on the results of ALU operations.

WEP

The wired equivalent privacy (WEP) engine encapsulates all the hardware accelerators to perform the encryption and decryption, as well as MIC computation and verification. The accelerators implement the following cipher algorithms: legacy WEP, WPA TKIP, WPA2 AES-CCMP.

Based on the frame type and association information, the PSM determines the appropriate cipher algorithm to be used. It supplies the keys to the hardware engines from an on-chip key table. The WEP interfaces with the TXE to encrypt and compute the MIC on transmit frames, and the RXE to decrypt and verify the MIC on receive frames. WAPI is also supported.

TXE

The transmit engine (TXE) constitutes the transmit data path of the MAC. It coordinates the DMA engines to store the transmit frames in the TXFIFO. It interfaces with WEP module to encrypt frames and transfers the frames across the MAC-PHY interface at the appropriate time determined by the channel access mechanisms.

The data received from the DMA engines are stored in transmit FIFOs. The MAC supports multiple logical queues to support traffic streams that have different QoS priority requirements. The PSM uses the channel access information from the IFS module to schedule a queue from which the next frame is transmitted. Once the frame is scheduled, the TXE hardware transmits the frame based on a precise timing trigger received from the IFS module.

The TXE module also contains the hardware that allows the rapid assembly of MPDUs into an A-MPDU for transmission. The hardware module aggregates the encrypted MPDUs by adding appropriate headers and pad delimiters as needed.

RXE

The receive engine (RXE) constitutes the receive data path of the MAC. It interfaces with the DMA engine to drain the received frames from the RXFIFO. It transfers bytes across the MAC-PHY interface and interfaces with the WEP module to decrypt frames. The decrypted data is stored in the RXFIFO.

The RXE module contains programmable filters that are programmed by the PSM to accept or filter frames based on several criteria such as receiver address, BSSID, and certain frame types.

The RXE module also contains the hardware required to detect A-MPDUs, parse the headers of the containers, and disaggregate them into component MPDUS.

IFS

The IFS module contains the timers required to determine interframe space timing including RIFS timing. It also contains multiple back-off engines required to support prioritized access to the medium as specified by WMM.

The interframe spacing timers are triggered by the cessation of channel activity on the medium, as indicated by the PHY. These timers provide precise timing to the TXE to begin frame transmission. The TXE uses this information to send response frames or perform transmit frame-bursting (RIFS or SIFS separated, as within a TXOP).

The back-off engines (for each access category) monitor channel activity, in each slot duration, to determine whether to continue or pause the back-off counters. When the back-off counters reach 0, the TXE gets notified, so that it may commence frame transmission. In the event of multiple back-off counters decrementing to 0 at the same time, the hardware resolves the conflict based on policies provided by the PSM.

The IFS module also incorporates hardware that allows the MAC to enter a low-power state when operating under the IEEE power-saving mode. In this mode, the MAC is in a suspended state with its clock turned off. A sleep timer, whose count value is initialized by the PSM, runs on a slow clock and determines the duration over which the MAC remains in this suspended state. Once the timer expires, the MAC is restored to its functional state. The PSM updates the TSF timer based on the sleep duration, ensuring that the TSF is synchronized to the network.

The IFS module also contains the PTA hardware that assists the PSM in Bluetooth coexistence functions.

TSF

The timing synchronization function (TSF) module maintains the TSF timer of the MAC. It also maintains the target beacon transmission time (TBTT). The TSF timer hardware, under the control of the PSM, is capable of adopting timestamps received from beacon and probe response frames in order to maintain synchronization with the network.

The TSF module also generates trigger signals for events that are specified as offsets from the TSF timer, such as uplink and downlink transmission times used in PSMP.

NAV

The network allocation vector (NAV) timer module is responsible for maintaining the NAV information conveyed through the duration field of MAC frames. This ensures that the MAC complies with the protection mechanisms specified in the standard.

The hardware, under the control of the PSM, maintains the NAV timer and updates the timer appropriately based on received frames. This timing information is provided to the IFS module, which uses it as a virtual carrier-sense indication.

MAC-PHY Interface

The MAC-PHY interface consists of a data path interface to exchange RX/TX data from/to the PHY. In addition, there is a programming interface, which can be controlled either by the host or the PSM to configure and control the PHY.

PHY Description

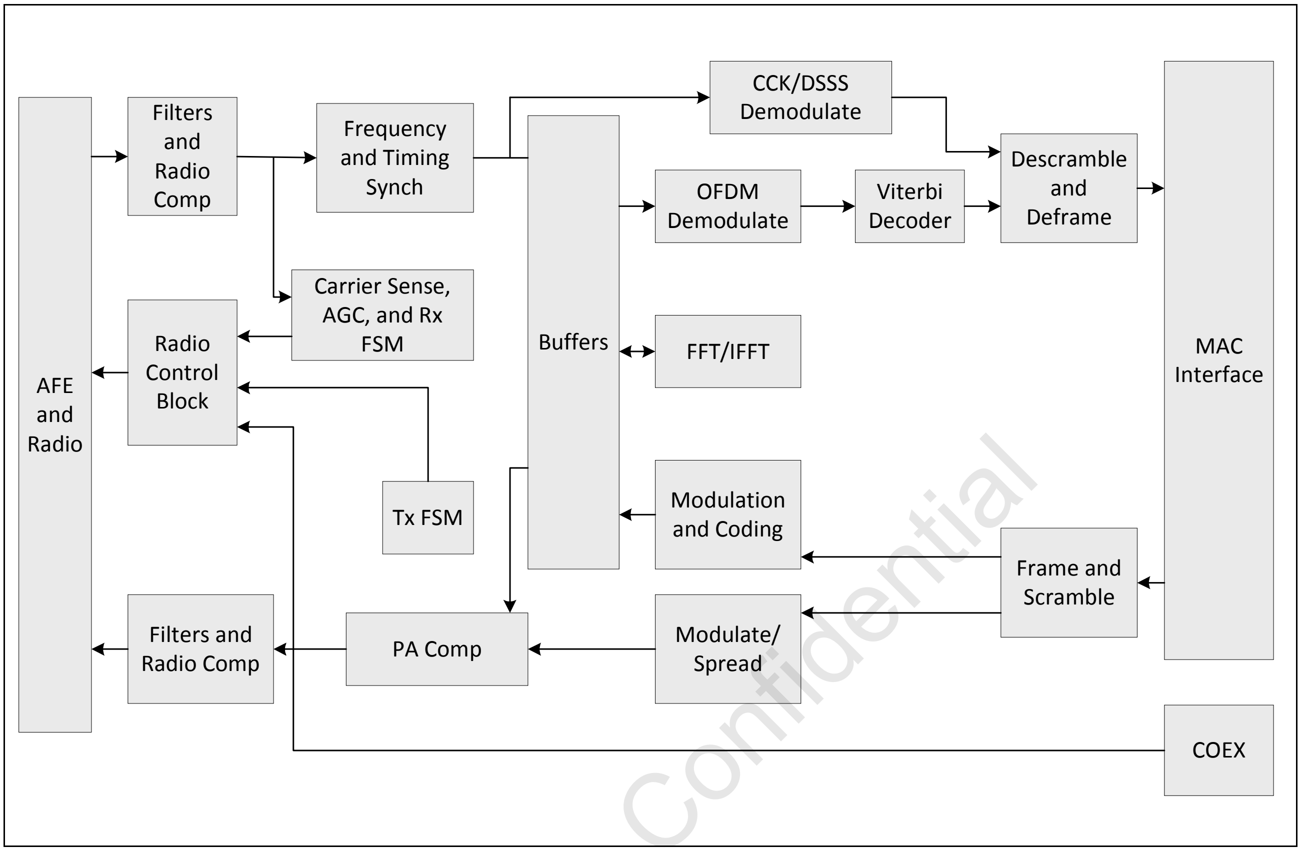
The BCM43362 WLAN Digital PHY is designed to comply with IEEE 802.11b/g/n single stream to provide wireless LAN connectivity supporting data rates from 1 Mbps to 72 Mbps for low-power, high-performance handheld applications.

The PHY has been designed to meet specification requirements in the presence of interference, radio nonlinearity, and impairments. It incorporates efficient implementations of the Filters, FFT and Viterbi decoder algorithms. Efficient algorithms have been designed to achieve maximum throughput and reliability, including algorithms for carrier sense/rejection, frequency/phase/timing acquisition and tracking, channel estimation and tracking. The PHY receiver also contains a robust 11b demodulator. The PHY carrier sense has been tuned to provide high throughput for IEEE 802.11g/11b hybrid networks with Bluetooth coexistence.

PHY Features

- Supports IEEE 802.11b, 11g, 11n single-stream standards.
- Supports Optional Greenfield mode in Tx and Rx.
- Supports optional STBC receive of two space-time stream.
- Supports IEEE 802.11h/d for worldwide operation.
- Algorithms achieving low power, enhanced sensitivity, range, and reliability
- Algorithms to maximize throughput performance in presence of Bluetooth
- Automatic gain control scheme for blocking and non blocking application scenario for cellular applications.
- Closed loop transmit power control
- Supports per packet Rx Antenna diversity.
- Designed to meet FCC and other regulatory requirements.

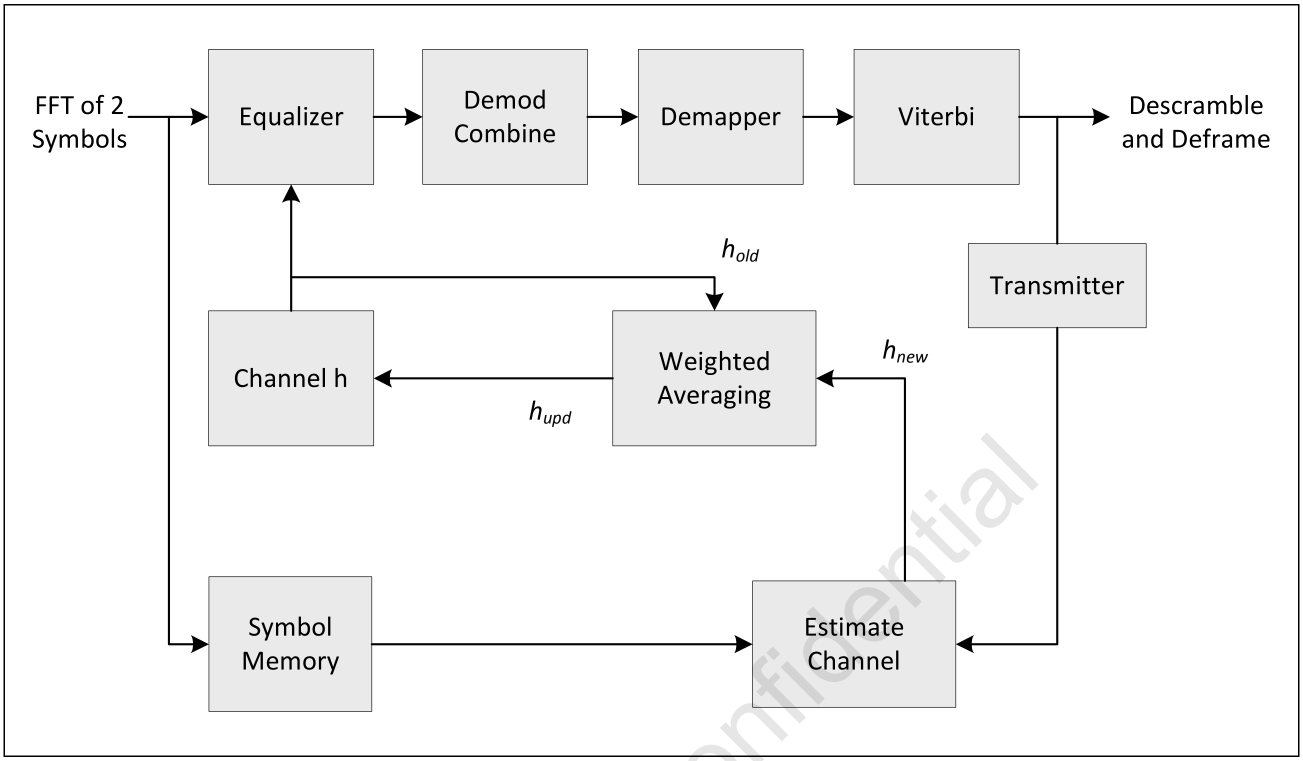
Figure 18: WLAN PHY Block Diagram



The PHY is capable of fully calibrating the RF front-end to extract the highest performance. On power-up, the PHY performs a full calibration suite to correct for IQ mismatch and local oscillator leakage. The PHY also performs periodic calibration to compensate for any temperature related drift, thus maintaining high-performance over time. A closed loop transmit control algorithm maintains the output power to required level with capability control Tx power on a per packet basis.

One of the key feature of the PHY is two space-time stream receive capability. The STBC scheme can obtain diversity gains by using multiple transmit antennas in AP (Access Point) in a fading channel environment, without increasing the complexity at the STA. Details of the STBC receive are shown in the block diagram in Figure 19 on page 39.

Figure 19: STBC Receive Block Diagram

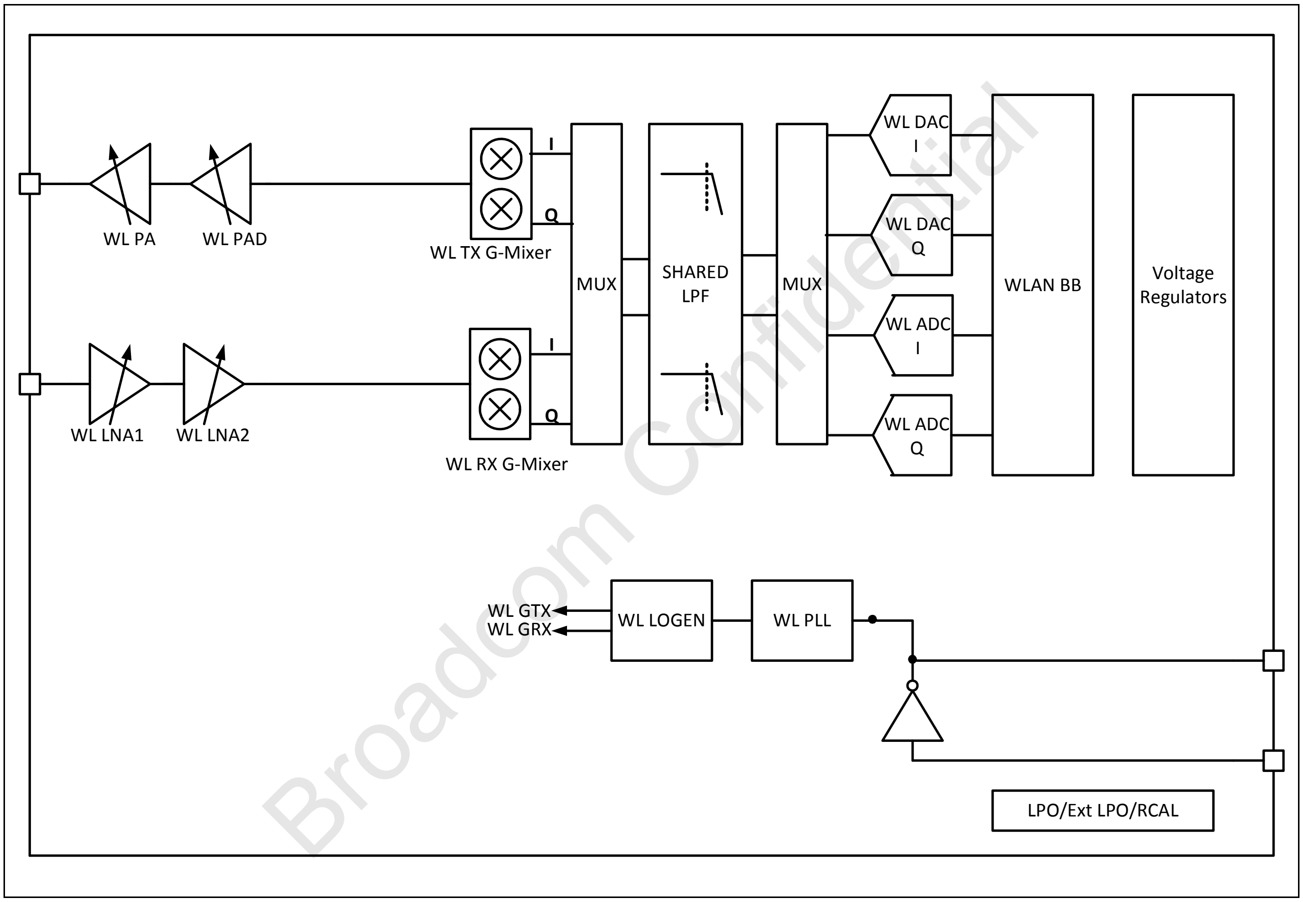


In STBC mode, symbols are processed in pairs. Equalized output symbols are linearly combined and decoded. Channel estimation is refined on every pair of symbols using the received symbols and reconstructed symbols.

Section 6: WLAN Radio Subsystem

The BCM43362 includes an integrated WLAN RF transceiver that has been optimized for use in 2.4 GHz Wireless LAN systems. It is designed to provide low power, low cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions. Improvements to the radio design include shared Tx/Rx baseband filters and high immunity to supply noise.

Figure 20: Radio Functional Block Diagram



Receive Path

The BCM43362 has a wide dynamic range, direct conversion receiver. It employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band.

Transmit Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM band. A linear on-chip power amplifier is included, which is capable of delivering high output powers while meeting IEEE 802.11b/g/n specifications without the need for an external PA. This PA can be powered directly from VBAT, thereby eliminating the need for a separate PALDO. Closed-loop output power control is completely integrated.

Calibration

The BCM43362 features dynamic on-chip calibration, eliminating process variation across components. This enables the BCM43362 to be used in high-volume applications, because calibration routines are not required during manufacturing testing. These calibration routines are performed periodically in the course of normal radio operation. Examples of this automatic calibration are baseband filter calibration for optimum transmit and receive performance and LOFT calibration for leakage reduction. In addition, I/Q Calibration, R Calibration, and VCO Calibration are performed on-chip.

Section 7: CPU and Global Functions

WLAN CPU and Memory Subsystem

The BCM43362 includes an integrated ARM Cortex™-M3 processor with internal RAM and ROM. The ARM Cortex-M3 processor is a low-power processor that features low gate count, low interrupt latency, and low-cost debugging. It is intended for deeply embedded applications that require fast interrupt response features. The processor implements the ARM® architecture v7-M with support for Thumb®-2 instruction set. ARM Cortex-M3 delivers 30% more performance gain over ARM7TDMI.

At 0.19 µW/MHz, the Cortex-M3 is the most power efficient general purpose microprocessor available, outperforming 8- and 16-bit devices on MIPS/µW. It supports integrated sleep modes.

ARM Cortex-M3 uses multiple technologies to reduce cost through improved memory utilization, reduced pin overhead, and reduced silicon area. ARM Cortex-M3 supports independent buses for Code and Data access (ICode/DCode and System buses). ARM Cortex-M3 supports extensive debug features including real time trace of program execution.

On-chip memory for the CPU includes 240 KB SRAM and 448 KB ROM.

One-Time Programmable Memory

Various hardware configuration parameters may be stored in an internal 1024-bit One-Time Programmable (OTP) memory, which is read by system software after device reset. In addition, customer-specific parameters, including the system vendor ID and the MAC address, can be stored, depending on the specific board design.

The initial state of all bits in an unprogrammed OTP device is 0. After any bit is programmed to a 1, it cannot be reprogrammed to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with the Broadcom WLAN manufacturing test tools. Alternatively, multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package. Documentation on the OTP development process is available on the Broadcom customer support portal (http://www.broadcom.com/support).

GPIO Interface

Five general purpose I/O (GPIO) pins are available on the BCM43362 that can be used to connect to various external devices.

GPIOs are tristated by default. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. They can also be programmed to have internal pull-up or pull-down resistors.

GPIO_0 is initially used as a strapping option to select between SDIO and SPI modes.

GPIOs 3, 4, and 5 are multiplexed with the Bluetooth Coexistence Interface. By default, these pins are BT_COEX pins. Software can reprogram these pins to behave as GPIOs.

GPIO_1 is a GPIO by default, but can be reprogrammed by software to become the BTCX_FREQ signal.

JTAG Interface

The BCM43362 supports the IEEE 1149.1 JTAG boundary scan standard for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Broadcom to assist customers by using proprietary debug and characterization test tools during board bring-up. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

UART Interface

One UART interface can be enabled by software as an alternate function on the JTAG pins. UART_RX is available on the JTAG_TDI pin, and UART_TX is available on the JTAG_TDO pin.

The UART is primarily for debugging during development. By adding an external RS-232 transceiver, this UART enables the BCM43362 to operate as RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. It is compatible with the industry standard 16550 UART, and it provides a FIFO size of 64 × 8 in each direction.

Section 8: WLAN Software Architecture

Host Software Architecture

The host driver (DHD) provides a transparent connection between the host operating system and the BCM43362 media (for example, WLAN) by presenting a network driver interface to the host operating system and communicating with the BCM43362 over an interface-specific bus (SPI, SDIO, and so on) to:

- Forward transmit and receive frames between the host network stack and the BCM43362 device, and
- Pass control requests from the host to the BCM43362 device, returning the BCM43362 device responses

The driver communicates with the BCM43362 over the bus using a control channel and a data channel to pass control messages and data messages. The actual message format is based on the BDC protocol.

Device Software Architecture

The wireless device, protocol, and bus drivers are run on the embedded ARM® processor using a Broadcom-defined operating system called HNDRTE, which transfers data over a propriety Broadcom format over the SDIO/SPI interface between the host and device (BDC/LMAC). The data portion of the format consists of IEEE 802.11 frames wrapped in a Broadcom encapsulation. The host side architecture provides all missing functionality between a network device and the Broadcom device interface. The host can also be customized to provide functionality between the Broadcom device interface and a full network device interface.

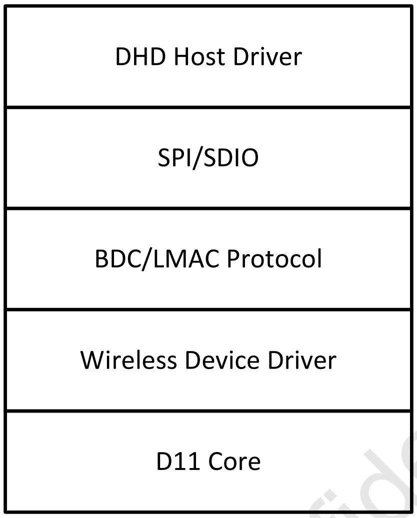
This transfer requires a message-oriented (framed) interconnect between the host and device. The SDIO bus is an addressed bus—each host-initiated bus operation contains an explicit device target address—and does not natively support a higher-level data frame concept. Broadcom has implemented a hardware/software message encapsulation scheme that ignores the bus operation code address and prefixes each frame with a 4-byte length tag for framing. The device presents a packet-level interface over which data, control, and asynchronous event (from the device) packets are supported.

The data and control packets received from the bus are initially processed by the bus driver and then passed on to the protocol driver. If the packets are data packets, they are transferred to the wireless device driver (and out through its medium), and a data packet received from the device medium follows the same path in the reverse direction. If the packets are control packets, the protocol header is decoded by the protocol driver. If the packets are wireless IOCTL packets, the IOCTL API of the wireless driver is called to configure the wireless device. The microcode running in the D11 core processes all time-critical tasks.

Remote Downloader

When the BCM43362 powers up, the DHD initializes and downloads the firmware to run in the device.

Figure 21: WLAN Software Architecture



Wireless Configuration Utility

The device driver that supports the Broadcom IEEE 802.11 family of wireless solutions provides an input/output control (IOCTL) interface for making advanced configuration settings. The IOCTL interface makes it possible to make settings that are normally not possible when using just the native operating system-specific IEEE 802.11 configuration mechanisms. The utility uses IOCTLs to query or set a number of different driver/chip operating properties.

Section 9: Pinout and Signal Descriptions

Signal Assignments

Figure 22 shows the 69-Ball WLBGA ball map.

Table 8 on page 47 shows the WLBGA signal descriptions.

Figure 22: 69-Ball WLBGA Ball Map

	A	B	C	D	E	F	G	H	J	K	L	
1	WRF_RFIN	WRF_RFOUT		WRF_PA_VDD	RF_SW_CTRL_0	RF_SW_CTRL_1	VDDIO_RF	VOUT_3P3	SR_VDDBAT1	SR_VDDBAT1	SR_VLX	1
2		WRF_PA_GND		WRF_PA_GND	WRF_PADRV_GND	RF_SW_CTRL_3	RF_SW_CTRL_2	VDD	SR_VDDBAT2	PMU_AVSS	SR_PVSS	2
3	WRF_LNA_VDD1P2			WRF_PADRV_VDD	VSS	VSS	VSS	VDD	EXT_SMPS_REQ	VOUT_LNLDO1	VDD_LDO	3
4	WRF_LNA_GND	WRF_ANA_VDD1P2	WRF_GPIO_OUT	WRF_ANA_GND	GPIO_0	VSS	VSS	VDDIO	WL_RST_N	EXT_PWM_REQ	VOUT_CLDO	4
5	WRF_VCO_LDO_IN_VDD1P8		WRF_VCO_LDO_OUT_VDD1P2	WRF_RES_EXT	GPIO_1 / BTCX_FREQ	SDIO_DATA_2	JTAG_TDO	BTCX_TXCONF/ GPIO_3	EXT_SLEEP_CLK	VDDIO_SD	SDIO_DATA_1	5
6	WRF_VCO_GND		WRF_XTAL_GND	OSCOUT	WRF_AFE_GND	XTAL_PU	JTAG_TMS	JTAG_TDI	BTCX_STATUS/ GPIO_4	SDIO_DATA_3	SDIO_DATA_0	6
7	WRF_TCXO_IN	WRF_TCXO_VDD3P3	WRF_XTAL_VDD1P2	OSCIN		WRF_AFE_VDD1P2	JTAG_TRST_L	JTAG_TCK	BTCX_RF_ACTIVE/ GPIO_5	SDIO_CMD	SDIO_CLK	7
	A	B	C	D	E	F	G	H	J	K	L	

Table 8: WLBGA Signal Descriptions

Ball #	Signal Name	Type	Description
WLAN RF Interface			
A1	WRF_RFIN	I	WLAN IEEE 802.11n RX input (50Ω)
B1	WRF_RFOUT	O	WLAN IEEE 802.11n internal power amplifier output (50Ω)
D5	WRF_RES_EXT	I	Connect to external 15 kΩ resistor (1%) to ground
RF Control Lines (IO Supply = VDDIO_RF)			
E1	RF_SW_CTRL0	O	RF switch control line. Default at this pin is high.
F1	RF_SW_CTRL1	O	RF switch control line. Default at this pin is low.
G2	RF_SW_CTRL2	O	RF switch control line. Default at this pin is low.
F2	RF_SW_CTRL3	O	RF switch control line. Default at this pin is low.

Note:

1. Use only RF_SW_CTRL1 and RF_SW_CTRL2 unless diversity is required, in which case RF_SW_CTRL0 and RF_SW_CTRL3 can also be used to select the antenna for a pair of SPDT switches.
2. For a transfer switch, use only RF_SW_CTRL1 and RF_SW_CTRL2 with the main antenna to Rx when RF_SW_CTRL1 is high.
3. For a diamond-type switch, do the following:
   - RF_SW_CTRL0 must select WLAN Tx, aux antenna.
   - RF_SW_CTRL1 must select WLAN Rx, main antenna.
   - RF_SW_CTRL2 must select WLAN Tx, main antenna.
   - RF_SW_CTRL2 must select WLAN Rx, aux antenna.
4. For cases where a shared antenna is used for WLAN and Bluetooth, RF_SW_CNTRL_0 defaults to HIGH when the BCM43362 is in reset. Use a switch topology in which the Bluetooth RF path is connected to the antenna when this signal is HIGH. This allows Bluetooth access to the antenna when WLAN is in reset.
5. The following is a list of the internal pull-up/pull-down resistor strengths for the RF switch control lines when the BCM43362 is in reset:

	Minimum	Typical	Maximum
– pup @ 3.3V	39K	58K	69K
– pdn @ 3.3V	39K	58K	67K

6. The default drive strength is 6.0 mA.

Table 8: WLBGA Signal Descriptions (Cont.)

Ball #	Signal Name	Type	Description
SDIO Interface			
F5	SDIO_DATA_2	I/O	SDIO data line 2. This pin has an internal weak pull-up resistor. ***Note:*** By default, the internal pull-up is enabled, but it can be disabled via software. The pull-up resistor is forced on for SPI mode since this pin is unused in that mode.
L6	SDIO_DATA_0/SPI_MISO	I/O	SDIO data line 0. This pin has an internal weak pull-up resistor. ***Note:*** By default, the internal pull-up is enabled, but it can be disabled via software.
L5	SDIO_DATA_1/SPI_IRQ	I/O	SDIO data line 1. This pin has an internal weak pull-up resistor. ***Note:*** By default, the internal pull-up is enabled, but it can be disabled via software.
L7	SDIO_CLK/SPI_CLK	I	SDIO clock.
K6	SDIO_DATA_3/SPI_CSX	I/O	SDIO data line 3. This pin has an internal weak pull-up resistor. ***Note:*** By default, the internal pull-up is enabled, but it can be disabled by software.
K7	SDIO_CMD/SPI_MOSI	I/O	SDIO command line. This pin has an internal weak pull-up resistor. ***Note:*** By default, the internal pull-up is enabled, but it can be disabled by software.
	SDIO/SPI weak internal pull-up resistances: For 1.8V (minimum, typical, maximum): 34 kΩ, 51 kΩ, 86 kΩ For 2.5V (minimum, typical, maximum): 21 kΩ, 32 kΩ, 54 kΩ For 3.3V (minimum, typical, maximum): 16 kΩ, 24 kΩ, 37 kΩ **Software programmable SDIO/SPI drive strength options**: For 1.8V: 0.5 mA, 1.0 mA, 1.5 mA, 2.0 mA, 2.5 mA (default), and 3.0 mA For 2.5V: 1.5 mA, 3.0 mA, 4.5 mA, 6.0 mA, 7.5 mA (default), and 9.0 mA For 3.3V: 2.0 mA, 4.0 mA, 6.0 mA, 8.0 mA, 10.0 mA (default), and 12.0 mA		
JTAG Interface			
G6	JTAG_TMS	I	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, this pin can be left unconnected (NC) as it has an internal weak pull-up resistor.
G5	JTAG_TDO	O	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, this pin can be left unconnected (NC). This pin is also muxed with UART_TX, which can be enabled by software.
H6	JTAG_TDI	I	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, this pin can be left unconnected (NC) as it has an internal weak pull-up resistor. This pin is also muxed with UART_RX, which can be enabled by software.
H7	JTAG_TCK	I	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, this pin can be left unconnected (NC) as it has an internal weak pull-up resistor.

Table 8: WLBGA Signal Descriptions (Cont.)

Ball #	*Signal Name*	*Type*	*Description*
G7	JTAG_TRST_L	I	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, this pin can be left unconnected (NC) as it has an internal weak pull-up resistor.
	JTAG drive strength: For 1.8V: 1.0 mA For 2.5V: 2.5 mA For 3.3V: 3.0 mA Output slewing can be enabled or disabled by software; it is enabled by default.		
Clocks			
A7	WRF_TCXO_IN	I	Reference clock input for use when sharing a TCXO with another chip, such as a BT/FM/GPS chip (see "Frequency References" on page 17). This input has an internal DC blocking capacitor, so do not include an external DC blocking capacitor. Connect directly to the external TCXO. This input pad is powered by the WRF_TCXO_VDD3P3 supply, which should be continually powered whenever the external TCXO is powered, even when the BCM43362 is in reset, thereby ensuring this input maintains a constant load on the TCXO signal in all device modes. If unused, ground this pin.
D6	OSCOUT	O	XTAL oscillator amplifier output. See "Frequency References" on page 17.
D7	OSCIN	I	XTAL oscillator amplifier input. This pin can also be used as the reference clock input from a dedicated (that is, not shared) TCXO.
F6	XTAL_PU	O	External reference clock enable (Clock_Request)
	Default mode (open source): XTAL_PU is driven HIGH when the clock is requested and pulled low with a weak internal pull-down resistor when the clock is not requested. **Push-Pull**: Always driven HIGH or LOW (no PU/PD). Push-Pull mode is enabled by software. **XTAL_PU internal pull-down (PD) resistances**: PD @ 1.8V (minimum, typical, maximum): 356 kΩ, 558 kΩ, 651 kΩ PD @ 2.5V (minimum, typical, maximum): 356 kΩ, 559 kΩ, 652 kΩ PD @ 3.3V (minimum, typical, maximum): 356 kΩ, 559 kΩ, 653 kΩ **XTAL_PU drive strength**: For 1.8V: 2.0 mA For 2.5V: 5.0 mA For 3.3V: 6.0 mA Output slewing can be enabled or disabled by software; it is enabled by default.		
J5	EXT_SLEEP_CLK	I	Input pin for optional high-precision 32.768 kHz Clock (Sleep Clock).

Table 8: WLBGA Signal Descriptions (Cont.)

Ball #	Signal Name	Type	Description
GPIO Interface			
E4	GPIO_0	I/O	This pin is used as a strapping option to select between SDIO mode (pull low) or SPI mode (pull high). It is strongly recommended to use GPIO_0 only as a host bus interface select. This pin has a weak internal pull-down resistor.
E5	GPIO_1/BTCX_FREQ	I/O	General-purpose interface pin. This pin is high impedance on power-up and reset. Subsequently, it becomes an input or output through software control. This pin has a programmable weak pull-up/down. This GPIO can be used as the out-of-band WLAN_IRQ signal for SDIO/SPI. This pin can also be programmed via software to behave as the BTCX_FREQ coexistence signal.
H5	BTCX_TXCONF/GPIO_3	–	Multiplexed BT_Coex/GPIO pins. When programmed as GPIOs, pins are high impedance on power-up and reset. Subsequently, they can be individually programmed to become inputs or outputs through software control. They can also be programmed to have internal pull-up or pull-down resistors. Only GPIO 1, 3, 4, and 5 (total 4) can be used as GPIOs. GPIO drive strength: For 1.8V: 1.0 mA For 2.5V: 2.5 mA For 3.3V: 3.0 mA Output slewing can be enabled or disabled by software; it is enabled by default.
J6	BTCX_STATUS/GPIO_4	–	
J7	BTCX_RF_ACTIVE/ GPIO_5	–	

Note:

The following is a list of the internal pull-up/pull-down resistor strengths for the default strapping options described in the GPIO section above:

	Minimum	Typical	Maximum
– pup @ 1.8V	40K	59K	70K
– pdn @ 1.8V	39K	58K	67K
– pup @ 2.5V	40K	58K	69K
– pdn @ 2.5V	39K	58K	67K
– pup @ 3.3V	39K	58K	69K
– pdn @ 3.3V	39K	58K	67K

Ball #	Signal Name	Type	Description
Miscellaneous Signals			
J4	WL_RST_N	I	Active low WLAN reset signal. Includes an internal 200 kΩ pull-down resistor. Within 1.5 ms of WL_RST_N being driven high, the PMU changes this from PD to High-Z. Software can optionally enable the pull-down resistor. VIH = 1.08V to 3.6V. VIL < 0.4V.
H5	BTCX_TXCONF/GPIO_3	O	Coexistence output giving Bluetooth permission to transmit. This pin is muxed and can be changed to a GPIO via software.

Table 8: WLBGA Signal Descriptions (Cont.)

Ball #	***Signal Name***	***Type***	***Description***
E5	GPIO_1/BTCX_FREQ	I	By default, this pin behaves as a GPIO. However, it can be programmed via software to behave as a coexistence signal that indicates that the coexisting BT is about to transmit on a restricted channel.
J6	BTCX_STATUS/GPIO_4	I	Coexistence signal indicating Bluetooth priority status and TX/RX direction. This pin is muxed and can be changed to a GPIO via software.
J7	BTCX_RF_ACTIVE/GPIO_5	I	Coexistence signal indicating that Bluetooth is active. This pin is muxed and can be changed to a GPIO via software.
Note: The above Bluetooth coexistence and GPIO signals have keepers that prevent them from floating when they aren't connected; however, when they are connected to another component, prevention from floating can't be assured by the keepers.			
Integrated Voltage Regulators			
H1	VOUT_3P3	O	3.3V low noise LDO output (40 mA)
K3	VOUT_LNLDO1	O	1.2V output for low noise LDO1, 150 mA
J1, K1	SR_VDDBAT1	I	Battery voltage input for CBUCK
J2	SR_VDDBAT2	I	Battery voltage input for band gap and LDOP3
J3	EXT_SMPS_REQ	I	Internal 200 kΩ pull-down resistor included. VIH = 1.08V to 3.6V, and VIL < 0.4V. **Note:** Driving this input high sets CBUCK to External mode, but it does not power down the rest of the PMU. The PMU powers down when WL_RST_N is low. **Note:** This pin is only used if the BCM43362 switching regulator is also used to power an external device. This pin should be connected to ground for applications that do not use this feature.
K4	EXT_PWM_REQ	I	Driving this input high forces CBUCK into PWM mode. Internal 200 kΩ pull-down resistor included. VIH = 1.08V to 3.6V, and VIL < 0.4V. **Note:** This pin is only used if the BCM43362 switching regulator is also used to power an external device. This pin should be connected to ground for applications that do not use this feature.
L1	SR_VLX	O	Core buck regulator: output to inductor
L3	VDD_LDO	I	Input supply pin for CLDO and LNLDO1 (also acts as the voltage feedback for CBUCK).
L4	VOUT_CLDO	O	1.2V output from the core LDO, 150 mA

Table 8: WLBGA Signal Descriptions (Cont.)

Ball #	Signal Name	Type	Description
Power Supplies			
B4	WRF_ANA_VDD1P2	I	1.2V analog power supply
A5	WRF_VCO_LDO_IN_ VDD1P8	I	1.4V to 1.8V VCO/LDO power supply input
B7	WRF_TCXO_VDD3P3	I	1.7V to 3.3V supply for the BCM43362 TCXO driver. To maintain a constant load on the TCXO_IN pin, even when power is removed from the BCM43362, connect this supply pin to a 1.7V to 3.3V supply that is present whenever the external TCXO is powered up. Note that this should be a clean supply (do not use VIO). If not used, this pin must be connected to ground.
C7	WRF_XTAL_VDD1P2	I	1.2V XTAL oscillator power supply. This supply is required for all clock options: crystal, dedicated TCXO, and shared TCXO (WRF_TCXO_IN).
D1	WRF_PA_VDD	I	Internal power amplifier power supply (VBAT supported), high current
D3	WRF_PADRV_VDD	I	Internal power amplifier driver power supply (VBAT supported)
F7	WRF_AFE_VDD1P2	I	1.2V AFE power supply
H2, H3	VDD	I	1.2V digital supply for the core
G1	VDDIO_RF	I	RF I/O and OTP supply (3.3V)
H4	VDDIO	I	Digital I/O supply.
K5	VDDIO_SD	I	Digital I/O supply for SDIO interface signals.
A3	WRF_LNA_VDD1P2	I	1.2V analog supply to the internal LNA.
C5	WRF_VCO_LDO_ OUT_VDD1P2	O	VCO LDO output. Some designs may require a decoupling capacitor (nominal 0.22 µF) for optimal WLAN performance. Broadcom recommends that a 0201 size footprint for this capacitor be included in all designs in case the capacitor is necessary.
Ground			
D4	WRF_ANA_GND	–	Analog ground
A6	WRF_VCO_GND	–	VCO ground
B2, D2	WRF_PA_GND	–	Internal power amplifier ground
C6	WRF_XTAL_GND	–	XTAL ground
E2	WRF_PADRV_GND	–	Internal power amplifier driver ground
E3, F3, F4, G3, G4	VSS	–	Ground
E6	WRF_AFE_GND	–	AFE ground
K2	PMU_AVSS	–	PMU analog ground
L2	SR_PVSS	–	Buck regulator: power switch ground
A4	WRF_LNA_GND	–	Internal Rx LNA ground
No Connects			
C4	WRF_GPIO_OUT	O	No Connect

Table 9: BCM43362 During Reset and After Reset or During Sleep

Signal Name/Group	I/O Type	During Reset		After Reset (and after firmware initialization) or During Sleep	
		Pull R	I/O	Pull R	I/O
Reset/Control					
WL_RST_N	Digital	PD	Input	High Z[a, b]	Input
EXT_SMPS_REQ	Digital	PD	Input	PD [c]	Input
EXT_PWM_REQ	Digital	PD	Input	PD [c]	Input
SPI Signals					
SPI_SDI	Digital	None	High Z	PU[d]	Input
SPI_SDO	Digital	None	High Z	PU[d]	Output
SPI_CLK	Digital	None	High Z	None	Input
SPI_CS	Digital	None	High Z	PU[d]	Input
SPI_IRQ	Digital	None	High Z	PU[d]	Output
SDIO Signals					
SDIO_CLK	Digital	None	High Z	None	Input
SDIO_CMD	Digital	None	High Z	PU[d]	Bidirectional
SDIO_DATA0	Digital	None	High Z	PU[d]	Bidirectional
SDIO_DATA1	Digital	None	High Z	PU[d]	Bidirectional
SDIO_DATA2	Digital	None	High Z	PU[d]	Bidirectional
SDIO_DATA3	Digital	None	High Z	PU[d]	Bidirectional
Clock					
XTAL_PU (CLK_REQ)	Digital	PD	High Z	PD[e]	Output (high)[e, f]
EXT_SLEEP_CLK (external 32.768 kHz clock)	Digital	None	High Z	None	Input
OSCIN (reference clock)	CLK	None	High Z	None	Input
Bluetooth Coexistence[g]					
btcx_txconf	Digital	None	High Z	Configurable	Output
btcx_freq	Digital	None	High Z	Configurable	Input
btcx_rf_actvive	Digital	None	High Z	Configurable	Input
btcx_status	Digital	None	High Z	Configurable	Input

Table 9: BCM43362 During Reset and After Reset or During Sleep (Cont.)

		During Reset		After Reset (and after firmware initialization) or During Sleep	
Signal Name/Group	**I/O Type**	**Pull R**	**I/O**	**Pull R**	**I/O**
RF Switch Control					
rf_sw_ctl_0	Digital	PU	High Z	None	Output
rf_sw_ctl_1	Digital	PD	High Z	None	Output
rf_sw_ctl_2	Digital	PD	High Z	None	Output
rf_sw_ctl_3	Digital	PD	High Z	None	Output
GPIOs[g]					
gpio_x	Digital	None	High Z	Configurable	Configurable

a. Within 1.5 ms of WL_RST_N being driven high, the PMU changes this from PD to High-Z.

b. Software can optionally enable a weak internal pull-down resistor.

c. Internal pull-down resistor can be disabled via software.

d. Software can optionally disable the weak internal pull-up for these signals.

e. Default mode (Open source): XTAL_PU is driven HIGH when a clock is requested, and pulled low with a weak internal pull-down resistor when a clock is not requested.
Push-Pull: Always driven HIGH or LOW (no PU/PD). Available via a strapping option for the FCFBGA and WLCSP packages.

f. The clock is not requested during Sleep mode.

g. The Bluetooth coexistence and GPIO signals have keepers that prevent them from floating when they aren't connected; however, when they are connected to another component, prevention from floating can't be assured by the keepers.

WLAN GPIO Signals and Strapping Options

The pins listed in Table 10 are sampled at power-on reset (POR) to determine the various operating modes. Sampling occurs a few milliseconds after an internal POR or deassertion of the external POR. After the POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 10: GPIO Functions and Strapping Options

Pin Name	*WLBGA Pin #*	*Default*	*Function*	*Description*
GPIO_0	E4	0	spimode_sel	This pin selects the host interface mode: • 0: SDIO • 1: gSPI

Section 10: DC Characteristics

Note: Values in this document are design goals and are subject to change based on the results of device characterization.

Absolute Maximum Ratings

Caution! The absolute maximum ratings in Table 11 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 11: Absolute Maximum Ratings

Rating	*Symbol*	*Value*	*Unit*
DC supply for VBAT	VBAT	–0.5 to 6.0	V
DC supply for WLAN power amplifier	VDDPA	–0.5 to 6.0	V
DC supply voltage for I/O	VDDIO, VDDIO_SD	–0.5 to 4.1	V
DC supply voltage for RF blocks in chip	VDDRF	–0.5 to 1.29	V
DC supply voltage for core	VDD	–0.5 to 1.29	V
DC supply voltage for RF I/Os	VDDIO_RF	–0.5 to 4.1	V
DC input supply voltage for CLDO and LNLDO	–	–0.5 to 2.1	V
WRF_VCO_LDO_IN_VDD1P8	–	–0.5 to 2.75	V
WRF_TCXO_VDD3P3	–	–0.5 to 3.63	V
WL_RST_N	–	–0.5 to 3.63	V
EXT_SMPS_REQ	–	–0.5 to 3.63	V
EXT_PWM_REQ	–	–0.5 to 3.63	V
Maximum undershoot voltage for I/O	$V_{undershoot}$	–0.5	V
Maximum overshoot voltage for I/O	$V_{overshoot}$	VDDIO + 0.5	V
Maximum Junction Temperature	T_j	125	°C

Environmental Ratings

The environmental ratings are shown in Table 12.

Table 12: Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient Temperature (T_A)	–30 to +85°C	°C	Operation
Storage Temperature	–40 to +125°C	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

Electrostatic Discharge Specifications

Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 13: ESD Specifications

Pin Type	Symbol	Condition	ESD Rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human Body Model Contact Discharge per JEDEC EID/ JESD22-A114	1250	V
Machine Model (MM)	ESD_HAND_MM	Machine Model Contact	50	V
CDM	ESD_HAND_CDM	Charged Device Model Contact Discharge per JEDEC EIA/ JESD22-C101	175	V

Recommended Operating Conditions and DC Characteristics

Functional operation is not guaranteed outside the limits shown in Table 14, and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 14: Recommended Operating Conditions and DC Characteristics

		Value			
Element	***Symbol***	***Minimum***	***Typical***	***Maximum***	***Unit***
DC supply voltage for VBAT	VBAT	2.3	–	4.8[a]	V
DC supply for WLAN power amplifier	VDDPA	2.3	3.3	4.8[a]	V
DC supply voltage for core	VDD	1.14	1.2	1.26	V
DC Supply voltage for RF blocks in chip	VDDRF	1.14	1.2	1.26	V
DC supply voltage for I/O	VDDIO, VDDIO_SD	1.71	–	3.63	V
DC supply voltage for RF I/Os	VDDIO_RF	3.13	3.3	3.46	V
WRF_VCO_LDO_IN_VDD1P8	–	1.4	1.8	1.9	V
WRF_TCXO_VDD3P3 (Icc = 500 µA max)[b,c]	–	1.7	1.8	3.3	V
Input high voltage (WL_RST_N, EXT_SMPS_REQ, EXT_PWM_REQ)	V_{IH}	1.08	–	3.6	V
Input low voltage (WL_RST_N, EXT_SMPS_REQ, EXT_PWM_REQ)	V_{IL}	–	–	0.4	V
Input high voltage (VDDIO = 1.8V)[d]	V_{IH}	1.1	–	VDDIO	V
Input low voltage (VDDIO = 1.8V)[c]	V_{IL}	–	–	0.7	V
Input high voltage (VDDIO = 2.5V)[c]	V_{IH}	1.7	–	VDDIO	V
Input low voltage (VDDIO = 2.5V)[c]	V_{IL}	–	–	0.8	V
Input high voltage (VDDIO = 3.3V)[c]	V_{IH}	2.0	–	VDDIO	V
Input low voltage (VDDIO = 3.3V)[c]	V_{IL}	–	–	0.8	V
SDIO input high voltage (VDDIO_SD = 1.8V)	V_{IH}	1.17	–	VDDIO_SD	V
SDIO input low voltage (VDDIO_SD = 1.8V)	V_{IL}	–	–	0.63	V
SDIO input high voltage (VDDIO_SD = 2.5V or 3.3V)	V_{IH}	2.0	–	VDDIO_SD	V
SDIO input low voltage (VDDIO_SD = 2.5V or 3.3V)	V_{IL}	–	–	0.8	V
Output low voltage[e]	V_{OL}	–	–	0.4	V
Output high voltage[d]	V_{OH}	VDDIO – 0.4V	–	–	V
Input low current	I_{IL}	–	0.3	–	µA
Input high current	I_{IH}	–	0.3	–	µA

a. The maximum continuous supply voltage is 4.8V. Brief spikes above this 4.8V can be tolerated. Specifically, voltages as high as 5.5V for up to 10 seconds cumulative duration over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds cumulative duration over the lifetime of the device are allowed.

b. The maximum limits for TCXO_VDD3P3 noise are:
20 kHz, 100 nV/sqrt(Hz); 100 kHz, 80 nV/sqrt(Hz); 1 MHz, 50 nV/sqrt(Hz); 2 MHz, 30 nV/sqrt (Hz)

c. Conditions for Icc = 500 µA maximum are: –30°C, 3.3V, 52 MHz.

d. For non-SDIO digital I/O only.

e. For SDIO and non-SDIO outputs.

Section 11: WLAN RF Specifications

The BCM43362 includes an integrated direct conversion radio that supports the 2.4 GHz band. This section describes the RF characteristics of the 2.4 GHz radio.

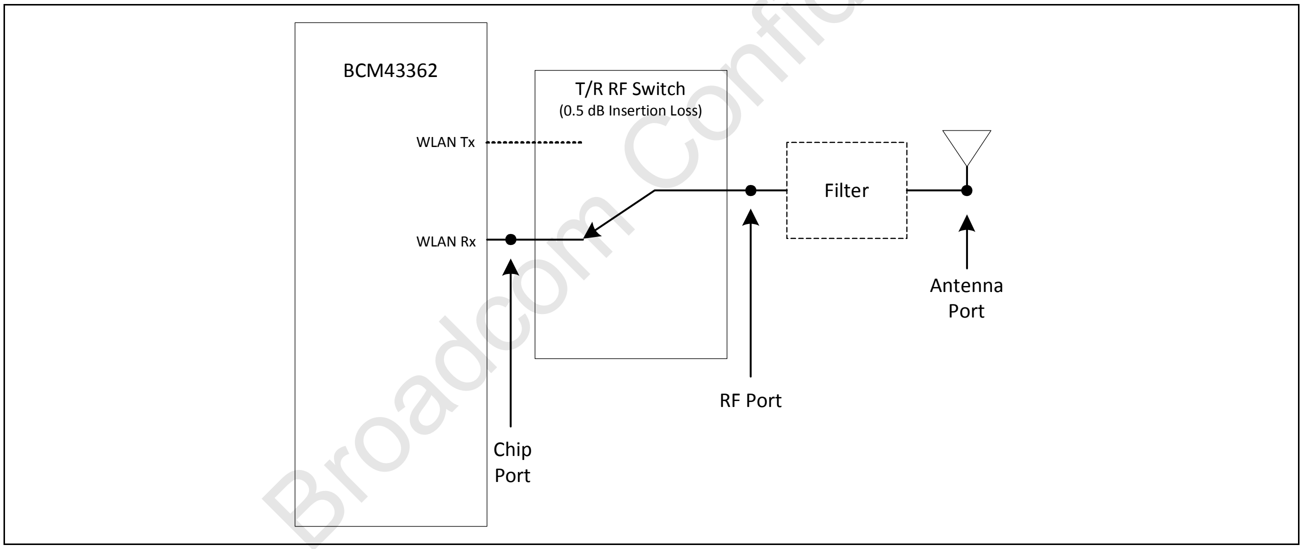
Note: Values in this document are design goals and may change based on device characterization results.

Unless otherwise stated, the specifications in this section apply when the operating conditions are within the limits specified in Table 12: “Environmental Ratings,” on page 57 and Table 14: “Recommended Operating Conditions and DC Characteristics,” on page 58. Functional operation outside these limits is not guaranteed.

Typical values apply for the following conditions:

- VBAT = 3.6V
- Ambient temperature +25°C

Figure 23: RF Port Location



Note: All specifications are measured at the RF port unless otherwise specified.

2.4 GHz Band General RF Specifications

Table 15: 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
Tx/Rx switch time	Including TX ramp down	–	–		μs
Rx/Tx switch time	Including TX ramp up	–	–		μs

WLAN 2.4 GHz Receiver Performance Specifications

Note: The specifications in Table 16 are measured at the RF port.

Table 16: WLAN 2.4 GHz Receiver Performance Specifications

Parameter	Condition/Notes	Minimum	Typical	Maximum	Unit
Frequency range	–	2400	–	2500	MHz
Operating temperature	–	–30	25	85	°C
RX sensitivity (8% PER for 1024 octet PSDU) at WLAN RF port[a]	1 Mbps DSSS	–95	–97	–	dBm
	2 Mbps DSSS	–92.5	–94.5	–	dBm
	5.5 Mbps DSSS	–90	–92	–	dBm
	11 Mbps DSSS	–87	–89	–	dBm
RX sensitivity (10% PER for 1000 octet PSDU) at WLAN RF port[a]	6 Mbps OFDM	–88	–90	–	dBm
	9 Mbps OFDM	–88	–90	–	dBm
	12 Mbps OFDM	–86	–88	–	dBm
	18 Mbps OFDM	–84	–86	–	dBm
	24 Mbps OFDM	–82	–84	–	dBm
	36 Mbps OFDM	–79	–81	–	dBm
	48 Mbps OFDM	–75	–77	–	dBm
	54 Mbps OFDM	–73	–75	–	dBm
RX sensitivity (10% PER for 4096 octet PSDU) at WLAN RF port[a]. Defined for default parameters: GF, 800 ns GI, and non-STBC.	20 MHz channel spacing for all MCS rates				
	MCS7	–70	–72	–	dBm
	MCS6	–72.5	–74.5	–	dBm
	MCS5	–74.5	–76.5	–	dBm
	MCS4	–78.5	–80.5	–	dBm
	MCS3	–82	–84	–	dBm
	MCS2	–84.5	–86.5	–	dBm
	MCS1	–86.5	–88.5	–	dBm
	MCS0	–88	–90	–	dBm

Table 16: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	*Condition/Notes*		*Minimum*	*Typical*	*Maximum*	*Unit*
Blocking level @ WLAN RF port for 1dB Rx sensitivity degradation (without external filtering).[b]	698–716 MHz	WCDMA, LTE	–28	–	–	dBm
	776–787 MHz	WCDMA, LTE	–28	–	–	dBm
	824–849 MHz	GSM850	–19[c]	–	–	dBm
	824–849 MHz	WCDMA, LTE	–28[d]	–	–	dBm
	880–915 MHz	GSM900	–19	–	–	dBm
	880–915 MHz	WCDMA, LTE	–28	–	–	dBm
	1710–1785 MHz	GSM1800	–22	–	–	dBm
	1710–1785 MHz	WCDMA, LTE	–28	–	–	dBm
	1850–1910 MHz	GSM1900	–22	–	–	dBm
	1850–1910 MHz	WCDMA, LTE	–28	–	–	dBm
	1880–1920 MHz	TD–SCDMA	–33	–	–	dBm
	1900–1920 MHz	LTE	–28	–	–	dBm
	1910–1930 MHz	LTE	–28	–	–	dBm
	1920–1980 MHz	WCDMA, LTE	–28	–	–	dBm
	1930–1990 MHz	LTE	–32	–	–	dBm
	2010–2025 MHz	TD–SCDMA	–31	–	–	dBm
	2500–2570 MHz	WCDMA, LTE	–50	–	–	dBm
	2570–2620 MHz	LTE	–50	–	–	dBm
	3168–4752 MHz	UWB	–28	–	–	dBm
	3402–3620 MHz	WiMAX	–23	–	–	dBm
	6336–8976 MHz	UWB	–21	–	–	dBm
Maximum Receive Level @ 2.4 GHz	@ 1, 2 Mbps (8% PER, 1024 octets)		–3.5	–	–	dBm
	@ 5.5, 11 Mbps (8% PER, 1024 octets)		–9.5	–	–	dBm
	@ 6–54 Mbps (10% PER, 1000 octets)		–13	–	–	dBm
LPF 3-dB Bandwidth	–	–	9	–	10	MHz
Adjacent channel rejection-DSSS (Difference between interfering and desired signal [25 MHz apart] at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	11 Mbps DSSS	–70 dBm	35	–	–	dB

Table 16: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Adjacent channel rejection-OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1000[e] octet PSDU with desired signal level as specified in Condition/Notes)	6 Mbps OFDM	–79 dBm	16	–	–	dB
	9 Mbps OFDM	–78 dBm	15	–	–	dB
	12 Mbps OFDM	–76 dBm	13	–	–	dB
	18 Mbps OFDM	–74 dBm	11	–	–	dB
	24 Mbps OFDM	–71 dBm	8	–	–	dB
	36 Mbps OFDM	–67 dBm	4	–	–	dB
	48 Mbps OFDM	–63 dBm	0	–	–	dB
	54 Mbps OFDM	–62 dBm	–1	–	–	dB
	65 Mbps OFDM	–61 dBm	–2	–	–	dB
Maximum receiver gain	–	–	–	90	–	dB
Gain control step	–	–	–	3	–	dB
RCPI accuracy[f]	Range −98 dBm to −75 dBm		−3	–	3	dB
	Range above −75 dBm		−5	–	5	dB
Return loss	Zo = 50 across the dynamic range.		10	–	–	dB

a. Derate by 1.5 dB for −30 °C to −10°C and 55°C to 85°C.
b. The cellular standard listed for each band indicates the type of modulation used to generate the interfering signal in that band for the purpose of this test. It is not intended to indicate any specific usage of each band in any specific country.
c. Min value is –23 dB for chan 11.
d. Min value is –36 dBm for chan 11.
e. For 65 Mbps, the size is 4096.
f. The minimum and maximum values shown have a 95% confidence level.

WLAN 2.4 GHz Transmitter Performance Specifications

Note: The specifications in Table 17 are measured at the RF port output.

Table 17: WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
Transmitted power in cellular and FM bands at RF port (at 18.5 dBm, 90% duty cycle, 1 Mbps CCK).[a]	76–108 MHz	FM RX	–	–161	–159	dBm/Hz
	170–240 MHz	DAB	–	–161	–159	dBm/Hz
	470–862 MHz	DVB-H	–	–161	–159	dBm/Hz
	728–746 MHz	WCDMA, LTE	–	–161	–159	dBm/Hz
	746–757 MHz	WCDMA, LTE	–	–161	–159	dBm/Hz
	869–894 MHz	WCDMA, LTE	–	–161	–159	dBm/Hz
	925–960 MHz	GSM, WCDMA, LTE	–	–161	–159	dBm/Hz
	1570–1580 MHz	GPS	–	–155	–153	dBm/Hz
	1592–1610 MHz	GLONASS	–	–155	–153	dBm/Hz
	1805–1880 MHz	GSM, WCDMA, LTE	–	–155	–153	dBm/Hz
	1880–1920 MHz	TD-SCDMA	–	–134	–132	dBm/Hz
	1850–1910 MHz	WCDMA, LTE	–	–134	–132	dBm/Hz
	1910–1930 MHz	WCDMA, LTE	–	–134	–132	dBm/Hz
	1900–1920 MHz	WCDMA, LTE	–	–134	–132	dBm/Hz
	1930–1990 MHz	GSM, WCDMA, LTE	–	–134	–132	dBm/Hz
	2010–2075 MHz	TD-SCDMA	–	–125.3	–123.3	dBm/Hz
	2110–2170 MHz	WCDMA, LTE	–	–125.3	–123.3	dBm/Hz
Harmonic level at RF port (at 18 dBm with 90% duty cycle, 1 Mbps CCK)	4.8–5.0 GHz	2nd harmonic	–	–19.5	–12.8	dBm/MHz
	7.2–7.5 GHz	3rd harmonic	–	–37.7	–26.7	dBm/MHz
Tx power at RF port for highest power level setting at 25°C, VBAT = 3.6V and spectral mask and EVM compliance[b, c]		**EVM Does Not Exceed**				
	IEEE 802.11b (DSSS/CCK)	–9 dB	18.5	–	–	dBm
	OFDM, BPSK	–8 dB	18	–	–	dBm
	OFDM, QPSK	–13 dB	18	–	–	dBm
	OFDM, 16-QAM	–19 dB	18	–	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	15.5	–	–	dBm
	OFDM, 64-QAM (R = 5/6)	–28 dB	14.5	–	–	dBm

Table 17: WLAN 2.4 GHz Transmitter Performance Specifications (Cont.)

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Tx power control dynamic range	–		9	–	–	dB
Closed loop Tx power variation at highest power level setting (at RF port)	Across full temperature and voltage range. Applies across 5 to 21 dBm output power range.		–	–	±1.5	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss	Zo = 50		4	6	–	dB
Load pull variation for output power, EVM, and Adjacent Channel Power Ratio (ACPR)	VSWR = 2:1.	EVM degradation	–	3.5	–	dB
		Output power variation	–	±2	–	dB
		ACPR-compliant power level	–	15	–	dBm
	VSWR = 3:1.	EVM degradation	–	4	–	dB
		Output power variation	–	±3	–	dB
		ACPR-compliant power level	–	15	–	dBm

a. The cellular standards listed indicate only typical usages of that band in some countries. Other standards may also be used within those bands.

b. Derate by 1.5 dB for temperatures less than –10°C or more than 55°C, or voltages less than 3.0V. Derate by 3.0 dB for voltages of less than 2.7V or voltages of less than 3.0V at temperatures less than –10°C or greater than 55°C.

c. Tx power for Ch 1 and Ch 11 is specified separately by nonvolatile memory parameters to ensure band-edge compliance.

General Spurious Emissions Specifications

Table 18: General Spurious Emissions Specifications

Parameter	Condition/Notes		Minimum	Typical	Maximum	Unit
Frequency range	–		2400	–	2500	MHz
General Spurious Emissions						
Tx Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–99	–96	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–44	–41	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–68	–65	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–88	–85	dBm
Rx/standby Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	–99	–96	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	–54	–51	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	–88	–85	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	–88	–85	dBm

Note: The specifications in this table are at the RF port.

Section 12: Internal Regulator Electrical Specifications

Note: Values in this document are design goals and are subject to change based on the results of device characterization.

Functional operation is not guaranteed outside the specification limits provided in this section.

Core Buck Regulator

The specifications for the Core Buck regulator (CBUCK) are provided in Table 19.

Table 19: Core Buck Regulator

Specification	*Notes*	*Minimum*	*Typical*	*Maximum*	*Units*
Input supply voltage	–	2.3	–	4.8[a]	Volts
PWM mode switching frequency	–	2.56	3.2	3.84	MHz
PWM output current	–	–	–	500	mA
Output current limit	–	–	700	–	mA
Output voltage range	Programmable, 33.33 mV steps default = 1.8V	1.2	–	1.833	Volts
Output voltage DC accuracy	Includes load and line regulation. VBAT = 2.7V to 4.8V, Load 0 to 500 mA, Inductor DCR < 137.5 mΩ	–5	–	5	%
PWM ripple voltage, static[b]	Measure with 20 MHz BW limit. Fixed load (0 to 500 mA). Max ripple based on VBAT < 4.3V, Vout = 1.833V, Fs = 3.2 MHz, 1.5 μH inductor L > 0.6144 μH, Cap+Board total-ESR < 10 mΩ, Cout > 1.9 μF	–	7	20	mVpp
PWM load step transient voltage error	VBAT = 2.7V to 4.8V, current step = 150 to 400 mA, 1 μsec rise-time based on 0402, 6.3V, X5R, and 4.7 μF[c] ceramic capacitor.	–	100	200	mV
PWM line step transient voltage error	VBAT step from 2.3 to 2.7V, 10 μsec rise-time, fixed 500 mA load based on 0402, 6.3V, X5R, and 4.7 μF[b] ceramic capacitor.	–	50	100	mV
PWM load regulation[a]	VBAT = 2.7V to 4.8V, 10 mA to 500 mA load. Inductor DCR < 137.5 mΩ	–	–	±30	mV

Table 19: Core Buck Regulator (Cont.)

Specification	Notes	Minimum	Typical	Maximum	Units
PWM line regulation[a]	VBAT = 2.7V to 4.8V, 500 mA load. Inductor DCR < 137.5 mΩ	–	–	±10	mV
Burst mode ripple voltage, static	Load < 30 mA. Measure with 20 MHz BW limit.	–	–	80	mVpp
	30 mA < Load < 200 mA. Measure with 20 MHz BW limit.	–	–	200	mVpp
Burst mode load step transient voltage error	VBAT = 2.7V to 4.8V, current step 10 to 200 mA, 1 µsec rise-time based on 0402, 6.3V, X5R, and 4.7 µF[b] ceramic capacitor.	–	60	120	mV
Burst mode line step transient voltage error	VBAT step from 2.3V to 2.7V, 10 µsec rise-time, fixed 200 mA load based on 0402, 6.3V, X5R, and 4.7 µF[b] ceramic capacitor.	–	50	100	mV
Burst mode load regulation	VBAT = 2.7V to 4.8V, 10 mA to 200 mA load	–	35	50	mV
Burst line regulation	Input voltage 2.7 to 4.8V, 200 mA load	–	44	70	mV
Peak PWM mode efficiency[d]	200 mA load current	80	90	–	%
	30 mA load current	60			%
Burst mode efficiency	5 mA load current	70	80	–	%
Start-up time from power down	–	–	1350	1500	µs
Burst to PWM mode transient voltage error	Ensure load current < 200 mA during a mode change	–	–	160	mV
External inductor	See preferred inductor list	–	1.5	–	µH
External output capacitor	Ceramic, X5R, 0402, Cap-ESR < 4 mΩ ESL < 700 pH at 3.2 MHz, ±20%, 6.3V	–	4.7	–	µF
External input capacitor	For SR_VDDBAT1 pins, ceramic, X5R, 0603, Cap-ESR < 4 mΩ at 3.2 MHz, ±10%, 6.3V	–	4.7	–	µF
Input supply voltage ramp-up time	0 to 4.3V	40	–	–	µs

[a] The maximum continuous supply voltage is 4.8V. Brief spikes above this 4.8V can be tolerated. Specifically, voltages as high as 5.5V for up to 10 seconds cumulative duration over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds cumulative duration over the lifetime of the device are allowed.

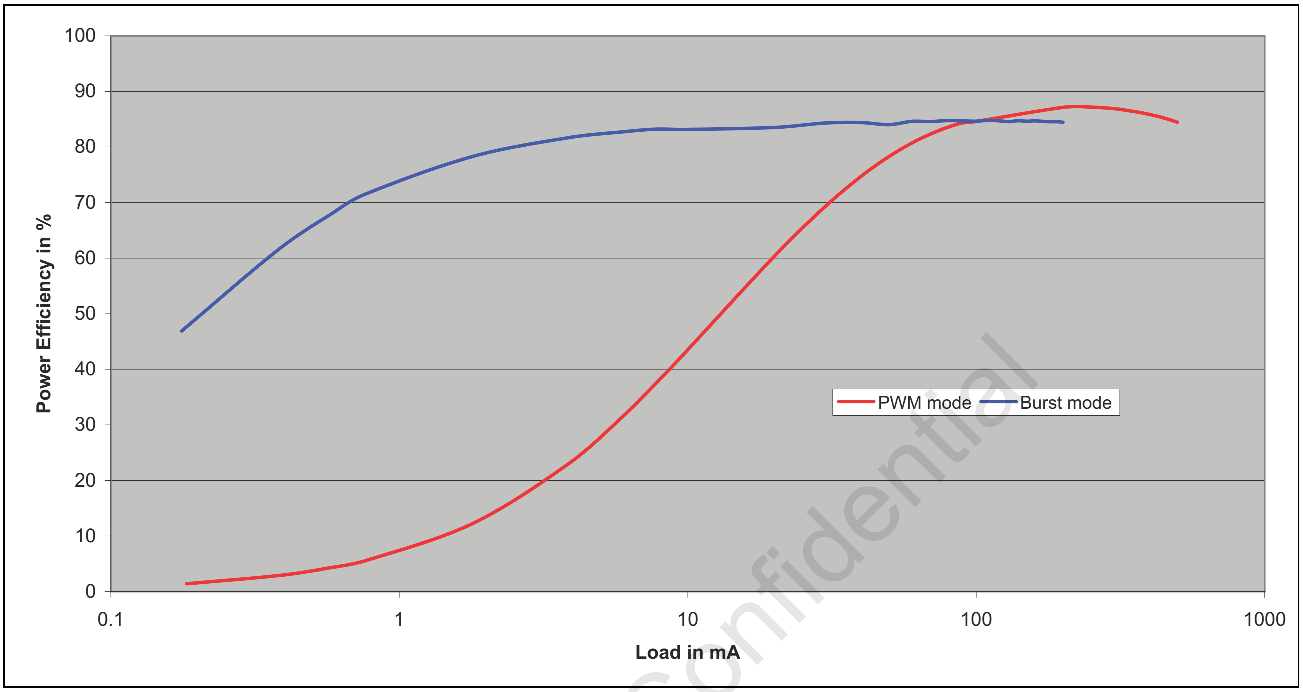
[b] These are not load or line step transient tests.

[c] More capacitance can be used to reduce the transient error at the output.

[d] VBAT < 4.3V. Inductor DCR < 137.5 mΩ, ACR < 1Ω.

An efficiency plot for the CBUCK regulator is shown in Figure 24. The plot shows typical performance for nominal process silicon, Vout = 1.8V, VBAT = 3.6V, and temperature = 25°C.

Figure 24: CBUCK Efficiency



3.3V LDO (LDO3P3)

Table 20: 3.3V LDO (LDO3P3)

Specification	Notes	Minimum	Typical	Maximum	Units
Input supply voltage	–	2.3	3.6	4.8[a]	Volts
Output current	–	–	–	40	mA
Output voltage, Vo	Step size 100 mV. Default = 3.3V.	2.4	3.3	3.4	Volts
Dropout voltage	At max load	–	–	200	mV
Output voltage DC accuracy	Include line/load regulation.	–5	–	+5	%
Quiescent current	No load	–	8	17	µA
Line regulation	Vin from (Vo + 0.2V) to 4.8V, maximum load	–0.2	–	+0.2	%Vo/V
Load regulation	Load from 1 mA to 40 mA	–	0.02	0.05	%Vo/ mA
Leakage current	Power-down mode	–	–	5	µA
PSRR	VBAT ≥ 3.6V, Vo = 2.5V, Co = 1 µF, max load, 100 Hz to 1 MHz	20	–	–	dB
Start-up time	From the rising edge of VIO as the chip powers up from a full power down (that is, band gap off)	–	1200	1400	µs
LDO turn-on time	LDO turn-on time when rest of chip is up	–	–	100	µs
In-rush current during turn-on	From its output capacitor in fully discharged state	–	–	135	mA
External output capacitor, Co	Ceramic, X5R, 0402, (ESR: 30 mΩ–200 mΩ), ±10%, 10V	–	1	–	µF
External input capacitor	For SR_VDDBAT2 pin (shared with Band gap) Ceramic, X5R, 0603, (ESR: 30 mΩ–200 mΩ), ±10%, 10V	–	1	–	µF

[a] The maximum continuous supply voltage is 4.8V. Brief spikes above this 4.8V can be tolerated. Specifically, voltages as high as 5.5V for up to 10 seconds cumulative duration over the lifetime of the device are allowed. Voltages as high as 5.0V for up to 250 seconds cumulative duration over the lifetime of the device are allowed.

CLDO

Table 21: CLDO

Specification	*Notes*	*Minimum*	*Typical*	*Maximum*	*Units*
Input supply voltage, Vin	Min = 1.25 + 0.2V = 1.45V. Dropout voltage requirement must be met under max load.	1.45	1.5	2.0	Volts
Output current	–	–	–	150	mA
Output voltage, Vo	Programmable in 25 mV steps	1.075	1.2	1.325	Volts
Dropout voltage	At max load	–	–	200	mV
Output voltage DC accuracy	Include line/load regulation Vin > Vo + 0.2V	–4	–	+4	%
Quiescent current	No-load	–	10	15	µA
Line regulation	Vin from (Vo + 0.2V) to 2V, max load	–0.2	–	+0.2	%Vo/V
Load regulation	Load from 1 mA to 150 mA	–	0.02	0.05	%Vo/mA
Leakage current	Power-down	–	–	10	µA
PSRR	@1 kHz, Vin ≥ 1.5V, Co = 1–2.2 µF	20	40	–	dB
Start-up time	From full-chip power down[a]	–	1250	1400	µs
LDO turn-on time	LDO turn-on time when rest of chip is up	–	–	180	µs
In-rush current during turn-on	From its output capacitor in fully discharged state	–	–	150	mA
External output capacitor, Co (nominal values)	Ceramic, X5R, 0402, (ESR: 30 mΩ–200 mΩ), ±10%, 10V	–	2.2	–	µF
External input capacitor (nominal values)	Only use an external input cap at VDD_LDO pin if it is not supplied from CBUCK output. Ceramic, X5R, 0402, (ESR: 30 mΩ–200 mΩ), ±10%, 10V	–	1	2.2	µF

[a] With CBUCK soft-starting concurrently.

LNLDO1

Table 22: LNLDO1

Specification	*Notes*	*Minimum*	*Typical*	*Maximum*	*Units*
Input supply voltage, Vin	Min = 1.25 + 0.2V = 1.45V Dropout voltage requirement must be met under max load.	1.45	1.5	2.0	Volts
Output current	–	–	–	150	mA
Output voltage, Vo	Programmable in 25 mV steps	1.075	1.2	1.325	Volts
Dropout voltage	At max load	–	–	200	mV
Output voltage DC accuracy	Include line/load regulation Vin > Vo+0.2V	–4	–	+4	%
Quiescent current	No-load	–	31	44	µA
Line regulation	Vin from (Vo+0.2V) to 2V, max load	–0.2	–	+0.2	%Vo/V
Load regulation	Load from 1 mA to 150 mA	–	0.02	0.05	%Vo/mA
Leakage current	Power-down	–	–	10	µA
Output noise	@30 kHz, 60 mA load Co = 2.2 µF @100 kHz, 60 mA load Co = 2.2 µF	–	–	60 30	nV/rt Hz nV/rt Hz
PSRR	@1 kHz, Vin ≥ 1.5V, Co = 2.2 µF	20	50	–	dB
LDO turn-on time	LDO turn-on time when rest of chip is up	–	–	180	µs
In-rush current during turn-on	From its output capacitor in fully discharged state	–	–	150	mA
External output capacitor, Co (nominal values)	Ceramic, X5R, 0402, (ESR: 30 mΩ–200 mΩ), ±10%, 10V	–	2.2	–	µF

Note: Recommended inductor for CBUCK: 1.5 µH ± 20%.
Murata® LQM21PN1R5MC0 2.0 × 1.25 × 0.55 mm DCR = 0.26Ω ± 25%.
Murata LQM2MPN1R5NG0 2.0 × 1.60 × 1.00 mm DCR = 0.11Ω ± 25%.

Section 13: System Power Consumption

Note: Table 23 shows typical values.

Power consumption referenced to VBAT @ 3.6V, 20°C, VDDIO = 1.8V, CBUCK out = 1.5V.

Table 23: System Power Consumption

WLAN Operational Modes	***Total (Ivbat)***
OFF[1]	11 µA
OFF[2]	40 µA
IDLE	185 µA
SLEEP[5]	200 µA
Rx (Listen)[3]	52 mA
Rx (Active)[4]	59 mA
Power Save[6, 9]	1.9 mA
Tx CCK (11 Mbps at 18.5 dBm)[7, 11]	320 mA
Tx OFDM (54 Mbps at 15.5 dBm)[8, 11]	270 mA
Tx OFDM (65 Mbps at 14.5 dBm)[10, 11]	260 mA

Note 1: WL_RST_N = Low, VDDIO is not present

Note 2: WL_RST_N = Low, VDDIO is present

Note 3: Carrier Sense (CCA) when no carrier present

Note 4: Carrier Sense (CS) detect/Packet Rx

Note 5: Intra-beacon Sleep

Note 6: Beacon Interval = 102.4 ms, DTIM = 1, Beacon duration = 1 ms @1 Mbps. Integrated Sleep + wakeup + Beacon Rx current over 1 DTIM interval.

Note 7: CCK power at chip port. Duty cycle is 100%. Includes PA contribution at 3.6V.

Note 8: OFDM power at chip port. Duty cycle is 100%. Includes PA contribution at 3.6V.

Note 9: In WLAN power-saving mode, the following blocks are powered down: Crystal oscillator, Baseband PLL, AFE, RF PLL, Radio

Note 10: OFDM power at chip port is 16 dBm, duty cycle is 100%, includes PA contribution at 3.6V.

The above blocks are turned ON in the required order with sufficient time for them to settle. This sequencing is done by the PMU controller that controls the settling time for each of the blocks. It also has information to determine the order in which the blocks should be turned ON. The settling times and the dependency order are programmable in the PMU controller. The default CLK settling time is set to 8 ms at power-up. It can be reduced after power-up.

Note 11: Absolute junction temperature limits maintained through active thermal monitoring and dynamic Tx duty cycle limiting.

Section 14: Interface Timing and AC Characteristics

Note: Values in this document are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, the specifications in this section apply when the operating conditions are within the limits specified in Table 12 on page 57 and Table 14 on page 58. Functional operation outside of these limits is not guaranteed.

SDIO Default Mode Timing

SDIO default mode timing is shown by the combination of Figure 25 and Table 24 on page 74.

Figure 25: SDIO Bus Timing (Default Mode)

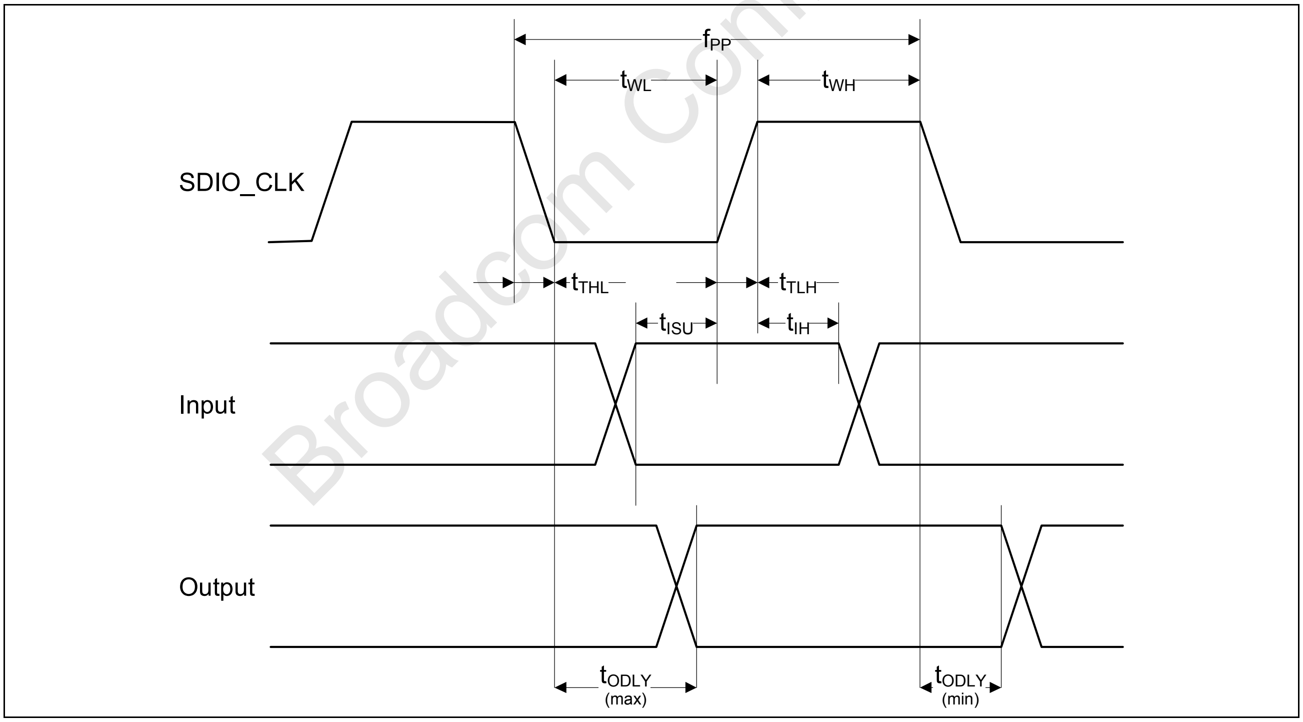


Table 24: SDIO Bus Timing [a] Parameters (Default Mode)

Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					

Table 24: SDIO Bus Timing [a] Parameters (Default Mode)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Frequency—Data Transfer mode	fPP	0	–	25	MHz
Frequency—Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock fall time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time—Data Transfer mode	tODLY	0	–	14	ns
Output delay time—Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40 pF load on CMD and Data.

b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

SDIO High-Speed Mode Timing

SDIO high-speed mode timing is shown by the combination of Figure 26 and Table 25.

Figure 26: SDIO Bus Timing (High-Speed Mode)

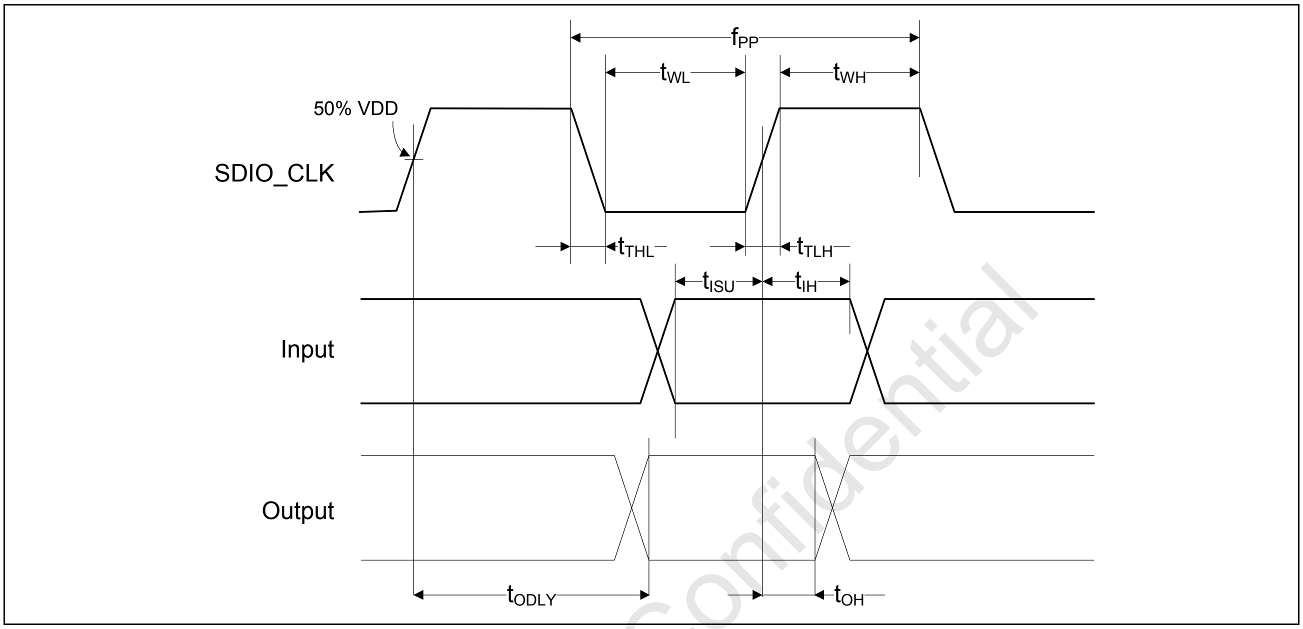


Table 25: SDIO Bus Timing [a] Parameters (High-Speed Mode)

Parameter	***Symbol***	***Minimum***	***Typical***	***Maximum***	***Unit***
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock fall time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

[a] Timing is based on CL ≤ 40pF load on CMD and Data.

[b] min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

gSPI Signal Timing

The gSPI device always samples data on the rising edge of the clock.

Figure 27: gSPI Timing

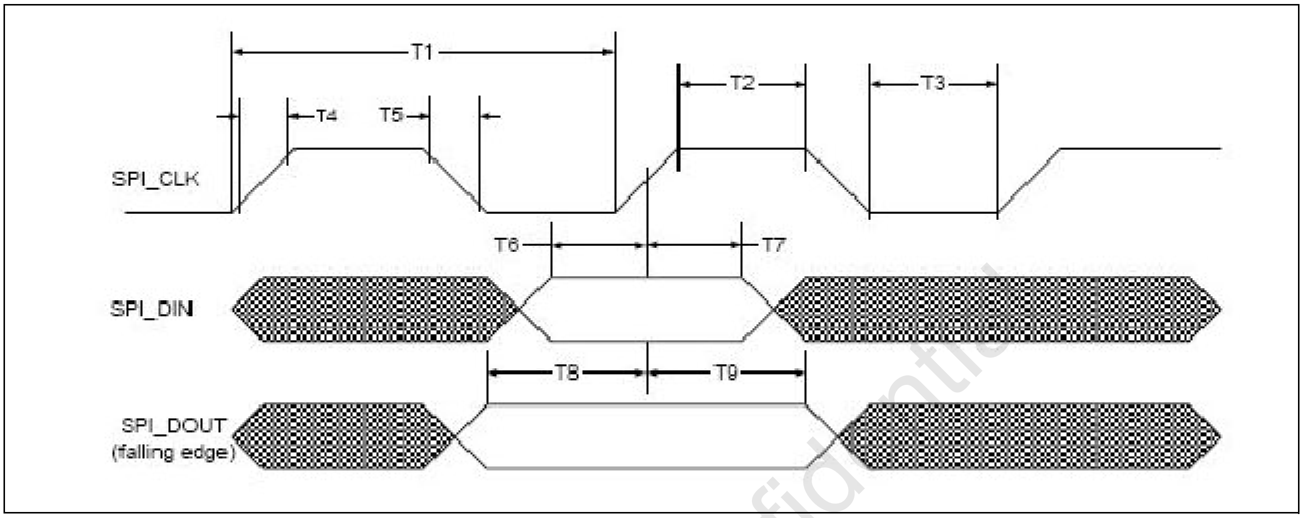


Table 26: gSPI Timing Parameters

Parameter	***Symbol***	***Minimum***	***Maximum***	***Units***	***Note***
Clock period	T1	20.8	–	ns	F_{max} = 48 MHz
Clock high/low	T2/T3	(0.45 × T1) – T4	(0.55 × T1) – T4	ns	–
Clock rise/fall time	T4/T5	–	2.5	ns	–
Input setup time	T6	5.0	–	ns	Setup time, SIMO valid to SPI_CLK active edge
Input hold time	T7	5.0	–	ns	Hold time, SPI_CLK active edge to SIMO invalid
Output setup time	T8	5.0	–	ns	Setup time, SOMI valid before SPI_CLK rising
Output hold time	T9	5.0	–	ns	Hold time, SPI_CLK active edge to SOMI invalid
CSX to clock[a]	–	7.86	–	ns	CSX fall to 1st rising edge
Clock to CSX[c]	–	–	–	ns	Last falling edge to CSX high

a. SPI_CSx remains active for entire duration of gSPI read/write/write_read transaction (i.e., overall words for multiple word transaction)

JTAG Timing

Table 27: JTAG Timing Characteristics

Signal Name	Period	Output Maximum	Output Minimum	Setup	Hold
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
$\overline{\text{JTAG\_TRST}}$	250 ns	–	–	–	–

Section 15: Package Information

Package Thermal Characteristics

Table 28: Package Thermal Characteristics[a]

Characteristic	*Value in Still Air*
θ_{JA} (°C/W)	44.88
θ_{JB} (°C/W)	1.20
θ_{JC} (°C/W)	0.20
Ψ_{JT} (°C/W)	0.04
Ψ_{JB} (°C/W)	14.21
Maximum Junction Temperature T_j (°C)[b]	125
Maximum Power Dissipation (W)	1.2

a. No heat sink, TA = 70°C. This is an estimate based on a 4-layer PCB that conforms to EIA/JESD51–7 (101.6 mm x 114.3 mm x 1.6 mm) and P = 1.2W continuous dissipation.

b. Absolute junction temperature limits maintained through active thermal monitoring and dynamic Tx duty cycle limiting.

Junction Temperature Estimation and PSI Versus Theta$_{jc}$

Package thermal characterization parameter PSI-JT (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta-J_C (θ_{JC}). The reason for this is θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is as follows:

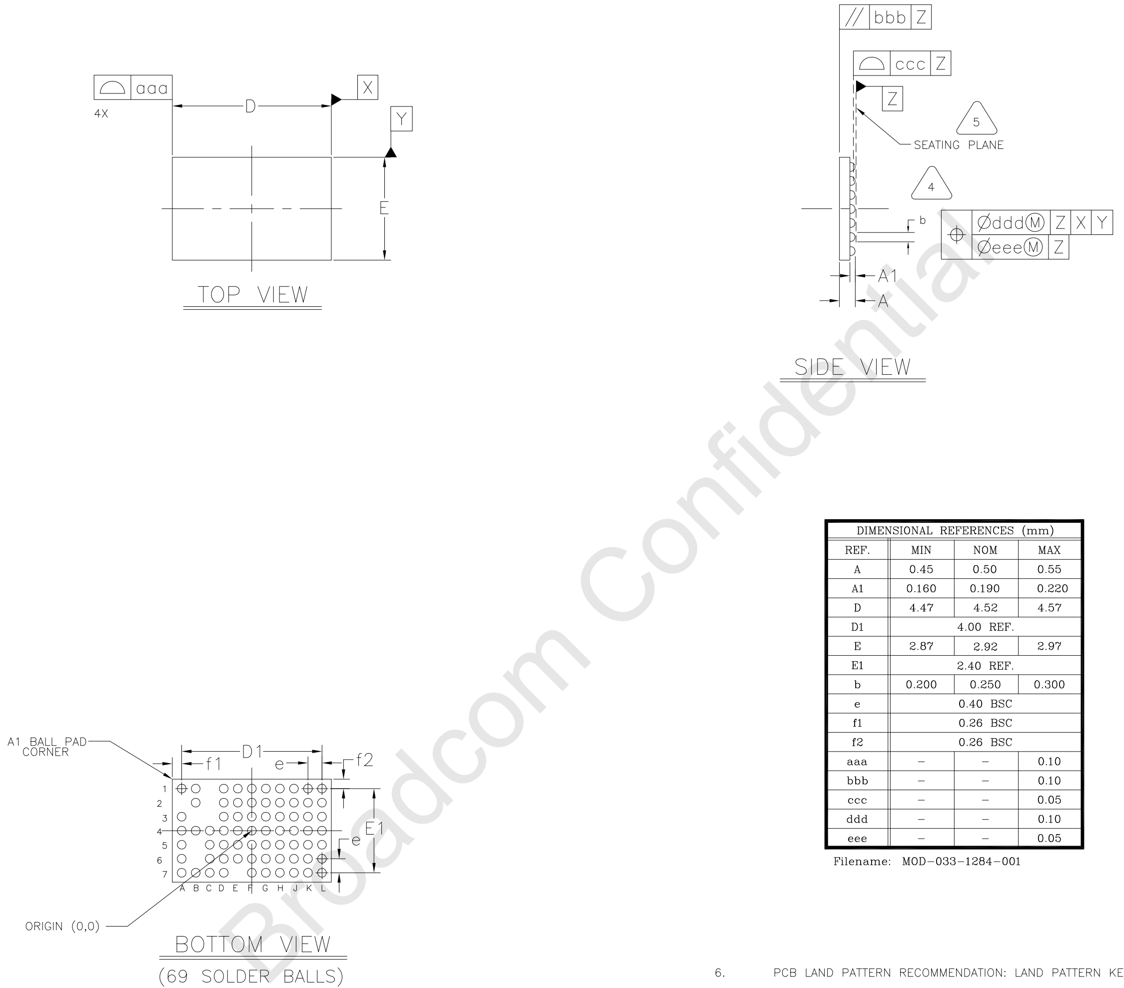
$$T_J = T_T + P \times \Psi_{JT}$$

Where:

- T_J = junction temperature at steady-state condition, °C
- T_T = package case top center temperature at steady-state condition, °C
- P = device power dissipation, Watts
- Ψ_{JT} = package thermal characteristics (no airflow), °C/W

Section 16: Mechanical Information

Figure 28: 69-Ball WLBGA Mechanical Information



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.160	0.190	0.220
D	4.47	4.52	4.57
D1	4.00 REF.		
E	2.87	2.92	2.97
E1	2.40 REF.		
b	0.200	0.250	0.300
e	0.40 BSC		
f1	0.26 BSC		
f2	0.26 BSC		
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

Filename: MOD–033–1284–001

6. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY A REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES."

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BUMP PITCH IS 0.40mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–225.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Section 17: Ordering Information

Part Number	***Package***	***Description***	***Operating Ambient Temperature***
BCM43362KUBG	69-ball WLBGA halogen-free package (4.52 mm x 2.92 mm, 0.40 pitch)	Single-band IEEE 802.11b/g/n 2.4 GHz WLAN	–30°C to +85°C

Note: Add a "T" to the end of the part number to specify "Tape and Reel".

Broadcom Corporation
5300 California Avenue
Irvine, CA 92617

Phone: 949-926-5000
Fax: 949-926-5203
E-mail: info@broadcom.com
Web: www.broadcom.com