

Technical Description

The Equipment Under Test (EUT) is a Bluetooth Speaker which equips with a 2.4GHz Bluetooth 4.2 Module. The EUT operates at frequency range of 2402MHz to 2480MHz. There are total 79 channels with 1MHz channel spacing. The EUT can accept wireless audio when paired with a Bluetooth devices. The audio signal is amplified and driving internal loudspeaker. The EUT is powered by a 12V internal rechargeable battery. The internal battery can be charged by 13.5V AC/DC adaptor (Model: YLS0301E-T135200. The applicant declared that the Bluetooth 4.0 BLE is not used.

2.4GHz Bluetooth Module:

Modulation Type: GFSK

Antenna Type: Integral, Internal (PCB Trace)

Frequency Range: 2402MHz - 2480MHz, 1MHz channel spacing, 79 channels

Nominal field strength is 97.6dB μ V/m @ 3m

Production Tolerance of field strength is +/- 3dB

Antenna gain is 0dBi

The functions of main ICs are mentioned below.

1. Bluetooth module BM6420 (IC1):

- 1) CSR64210 (U1) acts as the 2.4GHz radio core of Bluetooth module (IC1).
- 2) 26MHz crystal (Y1) provides clock for Bluetooth RF IC CSR64210 (U1).
- 3) U7 (KH25L8006) is flash memory for parameter storage.
- 4) F1 is 2.4GHz bandpass filter.

2. Regulator and LED strip control portion:

- 1) U7 (5802-3.3V) is 3.3V regulator.
- 2) U2 (24C02) is flash memory for controlling LED light strip.

3. Audio portion:

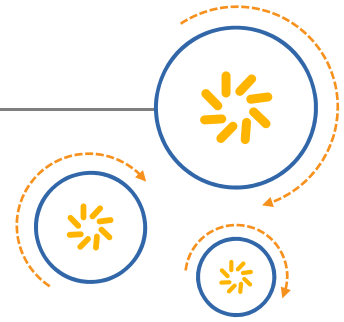
- 1) U3 (TDA3116) is stereo amplifier.

Bluetooth 3.0

CH. NO.	FRE.	Hex Value		CH. NO.	FRE.	Hex Value		CH. NO.	FRE.	Hex Value		CH. NO.	FRE.	Hex Value
CH0	2402MHz	0		CH26	2428MHz	1A		CH52	2454MHz	34		CH78	2480MHz	4E
CH1	2403MHz	1		CH27	2429MHz	1B		CH53	2455MHz	35				
CH2	2404MHz	2		CH28	2430MHz	1C		CH54	2456MHz	36				
CH3	2405MHz	3		CH29	2431MHz	1D		CH55	2457MHz	37				
CH4	2406MHz	4		CH30	2432MHz	1E		CH56	2458MHz	38				
CH5	2407MHz	5		CH31	2433MHz	1F		CH57	2459MHz	39				
CH6	2408MHz	6		CH32	2434MHz	20		CH58	2460MHz	3A				
CH7	2409MHz	7		CH33	2435MHz	21		CH59	2461MHz	3B				
CH8	2410MHz	8		CH34	2436MHz	22		CH60	2462MHz	3C				
CH9	2411MHz	9		CH35	2437MHz	23		CH61	2463MHz	3D				
CH10	2412MHz	A		CH36	2438MHz	24		CH62	2464MHz	3E				
CH11	2413MHz	B		CH37	2439MHz	25		CH63	2465MHz	3F				
CH12	2414MHz	C		CH38	2440MHz	26		CH64	2466MHz	40				
CH13	2415MHz	D		CH39	2441MHz	27		CH65	2467MHz	41				
CH14	2416MHz	E		CH40	2442MHz	28		CH66	2468MHz	42				
CH15	2417MHz	F		CH41	2443MHz	29		CH67	2469MHz	43				
CH16	2418MHz	10		CH42	2444MHz	2A		CH68	2470MHz	44				
CH17	2419MHz	11		CH43	2445MHz	2B		CH69	2471MHz	45				
CH18	2420MHz	12		CH44	2446MHz	2C		CH70	2472MHz	46				
CH19	2421MHz	13		CH45	2447MHz	2D		CH71	2473MHz	47				
CH20	2422MHz	14		CH46	2448MHz	2E		CH72	2474MHz	48				
CH21	2423MHz	15		CH47	2449MHz	2F		CH73	2475MHz	49				
CH22	2424MHz	16		CH48	2450MHz	30		CH74	2476MHz	4A				
CH23	2425MHz	17		CH49	2451MHz	31		CH75	2477MHz	4B				
CH24	2426MHz	18		CH50	2452MHz	32		CH76	2478MHz	4C				
CH25	2427MHz	19		CH51	2453MHz	33		CH77	2479MHz	4D				



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Features

- Bluetooth® v4.2 specification compliant
- 80 MHz RISC MCU and 80 MIPS Kalimba DSP
- High-performance stereo codec with 1 microphone input (shared with line input) and 1 digital microphone (MEMS) interface
- Internal ROM and serial flash memory
- Radio includes integrated balun with RF performance of 8 dBm (typ) transmit power and -89 dBm (typ) BDR receiver sensitivity
- AVRCP v1.5
- TrueWireless Stereo™ (TWS)
- User and manufacturer configurable EQs
- Wideband speech supported by HFP v1.6 and mSBC codec
- CSR's latest cVc technology for narrowband and wideband voice connections including wind noise reduction
- Multipoint support for A2DP connection to 2 A2DP sources for music playback
- Secure simple pairing, CSR's proximity pairing and CSR's proximity connections
- Stereo line-in
- Serial interfaces: USB 2.0, UART, I²C and SPI
- SBC and AAC decoder support
- Wired audio support
- Integrated dual switch-mode regulators, linear regulators and battery charger
- External crystal load capacitors not required for typical crystals
- 3 LED outputs (RGB)
- 68-lead QFN 8 x 8 x 0.9 mm 0.4 mm pitch
- Green (RoHS compliant and no antimony or halogenated flame retardants)

General Description

CSRA64210 QFN is a single-chip Bluetooth ROM audio solution for rapid evaluation and development of Bluetooth ROM stereo applications.

The CSRA64210 QFN consumer audio platform for wired and wireless applications using the QFN package integrates an ultra-low power DSP and application processor, high-performance stereo codec, a power management subsystem and LED drivers.

The CSR configuration tools and the development kit provide a flexible and powerful development platform to design advanced and high-quality Bluetooth stereo products using the CSRA64210 QFN single-chip Bluetooth audio solution.

BlueCore® CSRA64210 QFN

CSRA64210 Stereo ROM Solution

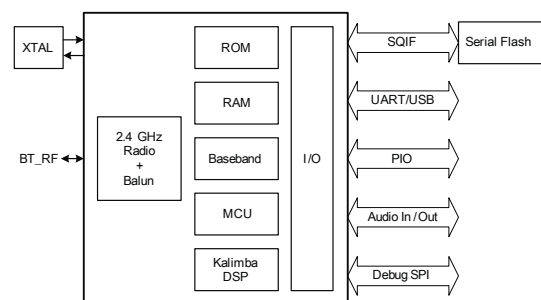
1-mic cVc® Hands-free Audio Enhancement

Fully Qualified Single-chip Bluetooth® v4.2 System

Engineering Sample

CSRA64210A11

Issue 1



Applications

- Stereo speakers
- Speakerphones

The enhanced Kalimba DSP coprocessor with 80 MIPS supports enhanced audio and DSP applications.

The integrated audio codec supports stereo input and output with 1-mic cVc hands-free input, 1 digital microphone (MEMS) interface, as well as a variety of audio standards.

See *CSR Glossary* at <https://www.csrsupport.com>

Ordering Information

Device	Package			Order Number
	Type	Size	Shipment Method	
CSRA64210 Stereo ROM Solution	QFN-68-lead (Pb free)	8 x 8 x 0.9 mm 0.4 mm pitch	Tape and reel	CSRA64210A11-IQQF-R

Note:

Until CSRA64210 QFN reaches **Production** status, engineering samples order number applies. This is ES-CSRA64210A11-IQQF, with no minimum order quantity.

CSRA64210 QFN is a ROM-based device where the product code has the form CSRA64210Axx. Axx is the specific ROM-variant, A11 is the ROM-variant for CSRA64210 Stereo ROM Solution.

At **Production** status minimum order quantity is 2kpcs taped and reeled.

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Supply chain: CSR's manufacturing policy is to multisource volume products. For further details, contact your local sales account manager or representative.

Contacts

General information

www.csr.com

Information on this product

sales@csr.com

Customer support for this product

www.csrsupport.com

Details of compliance and standards

product.compliance@csr.com

Help with this document

comments@csr.com

CSRA64210 Stereo ROM Solution Development Kit Ordering Information

Description	Order Number
CSRA64210 Stereo ROM Solution Audio Development Kit	DK-64210-TBD-TBD

Device Details

Bluetooth low energy

- Dual-mode Bluetooth low energy radio

Bluetooth Radio

- On-chip balun (50 Ω impedance)
- No production trimming of external components
- Bluetooth v4.2 specification compliant

Bluetooth Transmitter

- 8 dBm (typ) RF transmit power with level control
- Class 1, Class 2 and Class 3 support, no external PA or TX/RX switch required

Bluetooth Receiver

- -91 dBm (typ) $\pi/4$ DQPSK receiver sensitivity and -81 dBm (typ) 8DPSK receiver sensitivity
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Real-time digitised RSSI available to application
- Fast AGC for enhanced dynamic range
- Channel classification for AFH

Bluetooth Synthesiser

- Fully integrated synthesiser requires no external VCO, varactor diode, resonator or loop filter
- Compatible with crystals 16 MHz to 32 MHz

Kalimba DSP

- Enhanced Kalimba DSP coprocessor, 80 MIPS, 24-bit fixed point core
- 2 single-cycle MACs: 24 x 24-bit multiply and 56-bit accumulator
- 32-bit instruction word, dual 24-bit data memory
- 6K x 32-bit program RAM including 1K instruction cache for executing out of internal ROM
- 16K x 24-bit + 16K x 24-bit 2-bank data RAM

Audio Interfaces

- Stereo audio ADC with line input
- Stereo audio DAC
- Supported sample rates of 8, 11.025, 16, 22.05, 32, 44.1, 48 and 96 kHz (DAC only)

Auxiliary Features

- Crystal oscillator with built-in digital trimming

Package Option

- 68-lead QFN 8 x 8 x 0.9 mm 0.4 mm pitch

Physical Interfaces

- UART interface for debug
- USB 2.0 (full-speed) interface, including USB BC1.2 charger detection
- 4-bit SPI flash memory interface
- SPI interface for debug and programming
- I²C master for amp control
- Up to 14 general purpose PIOs with 3 extra open-drain PIOs available when LED not used
- PCM and I²S interfaces
- 3 LED drivers (includes RGB) with PWM flasher independent of MCU

Integrated Power Control and Regulation

- Automatic power switching to charger when present
- 2 high-efficiency switch-mode regulators with 1.8 V and 1.35 V outputs direct from battery supply
- 3.3 V linear regulator for USB supply
- Low-voltage linear regulator for internal digital circuits
- Low-voltage linear regulator for internal analogue circuits
- Power-on-reset detects low supply voltage
- Power management includes digital shutdown and wake-up commands for ultra-low power modes

Battery Charger

- Lithium ion / Lithium polymer battery charger
- Instant-on function automatically selects the power supply between battery and USB, which enables operation even if the battery is fully discharged
- Fast charging support up to 200 mA with no external components. Higher charge currents using external pass device.
- Supports USB charger detection
- Support for thermistor protection of battery pack
- Support to enable end product design to PSE law:
 - Design to JIS-C 8712/8714 (batteries)
 - Testing based on IEEE 1725

Baseband and Software

- Internal ROM
- Memory protection unit supporting accelerated VM
- 56 KB internal RAM, enables full-speed data transfer, and full piconet support
- Logic for forward error correction, header error control, access code correlation, CRC, demodulation, encryption bit stream generation, whitening and transmit pulse shaping

CSRA64210 Stereo ROM Solution Details

Bluetooth Profiles

- Bluetooth v4.2 specification support
- A2DP v1.3
- AVRCP v1.5
- HFP v1.6
- HSP v1.2
- DI v1.3

Music Enhancements

- SBC and AAC
- TrueWireless Stereo (TWS)
- Configurable Signal Detection to trigger events
- Up to 10 stages of Speaker Parametric EQ
- Up to 6 banks of 5 stages of User Parametric EQ for music playback (user, rock, pop, classical, jazz, etc)
- MeloD[®] Expansion 3D stereo widening and phase shifting effect
- Volume Control
- Comander to compress or expand the dynamic range of the audio
- Post Mastering to improve DAC fidelity
- Volume Boost

Additional Functionality

- Support for multi-language programmable audio prompts
- CSR's proximity pairing and CSR's proximity connection
- Multipoint support for A2DP connection to 2 A2DP sources for music playback
- Talk-time extension

CSRA64xxx ROM Series Configuration Tool

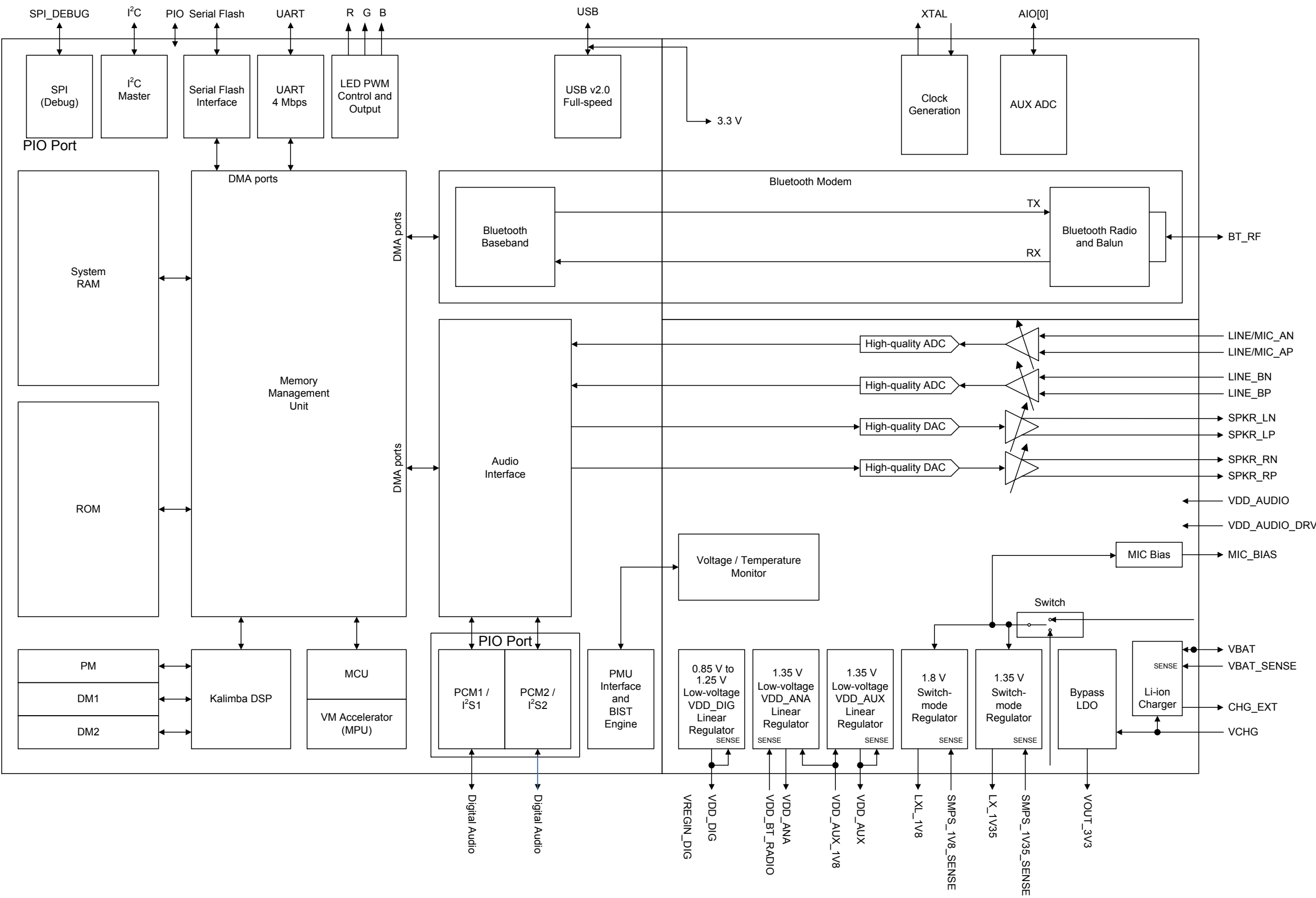
Configures the CSRA64210 stereo ROM solution software features:

- Bluetooth v4.2 specification features
- Reconnection policies, e.g. reconnect on power-on
- Audio features, including default volumes
- Button events: configuring button presses and durations for certain events, e.g. double press on PIO for last number redial
- LED indications for states, e.g. device connected, and events, e.g. power on
- Indication tones for events and ringtones
- Battery divider ratios and thresholds, e.g. thresholds for battery low indication, full battery etc.
- Advanced Multipoint settings

CSRA64210 Stereo ROM Solution Development Kit

- Example CSRA64210 QFN module design
- Carrier board
- Output stage: headphone amplifier
- Interface adapters and cables

Functional Block Diagram





Document History

Revision	Date	Change Reason
Issue 1	29 JUL 15	Original publication of this document.

Status Information

The status of this Data Sheet is **Engineering Sample**. CSR Product Data Sheets progress according to the following format:

- **Advance Information:**
 - Information for designers concerning CSR product in development. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.
- **Engineering Sample:**
 - Information about initial devices. Devices are untested or partially tested prototypes, their status is described in an Engineering Sample Release Note. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.
 - All detailed specifications including pinouts and electrical specifications may be changed by CSR without notice.
- **Pre-production Information:**
 - Pinout and mechanical dimension specifications finalised. All values specified are the target values of the design. Minimum and maximum values specified are only given as guidance to the final specification limits and must not be considered as the final values.
 - All electrical specifications may be changed by CSR without notice.
- **Production Information:**
 - Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.
 - Production Data Sheets supersede all previous document versions.

Device Implementation

Important Note:

As the feature-set of the CSRA64210 QFN is firmware build-specific, see the relevant software release note for the exact implementation of features on the CSRA64210 QFN.

Life Support Policy and Use in Safety-critical Applications

CSR's products are not authorised for use in life-support or safety-critical applications. Use in such applications is done at the sole discretion of the customer. CSR will not warrant the use of its devices in such applications.

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CSRA64210 QFN devices meet the requirements of Directive 2011/65/EU of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS). CSRA64210 QFN devices are free from halogenated or antimony trioxide-based flame retardants and other hazardous chemicals. For more information, see CSR's *Environmental Compliance Statement for CSR Green Semiconductor Products*.

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1 Package Information

1.1 Pinout Diagram

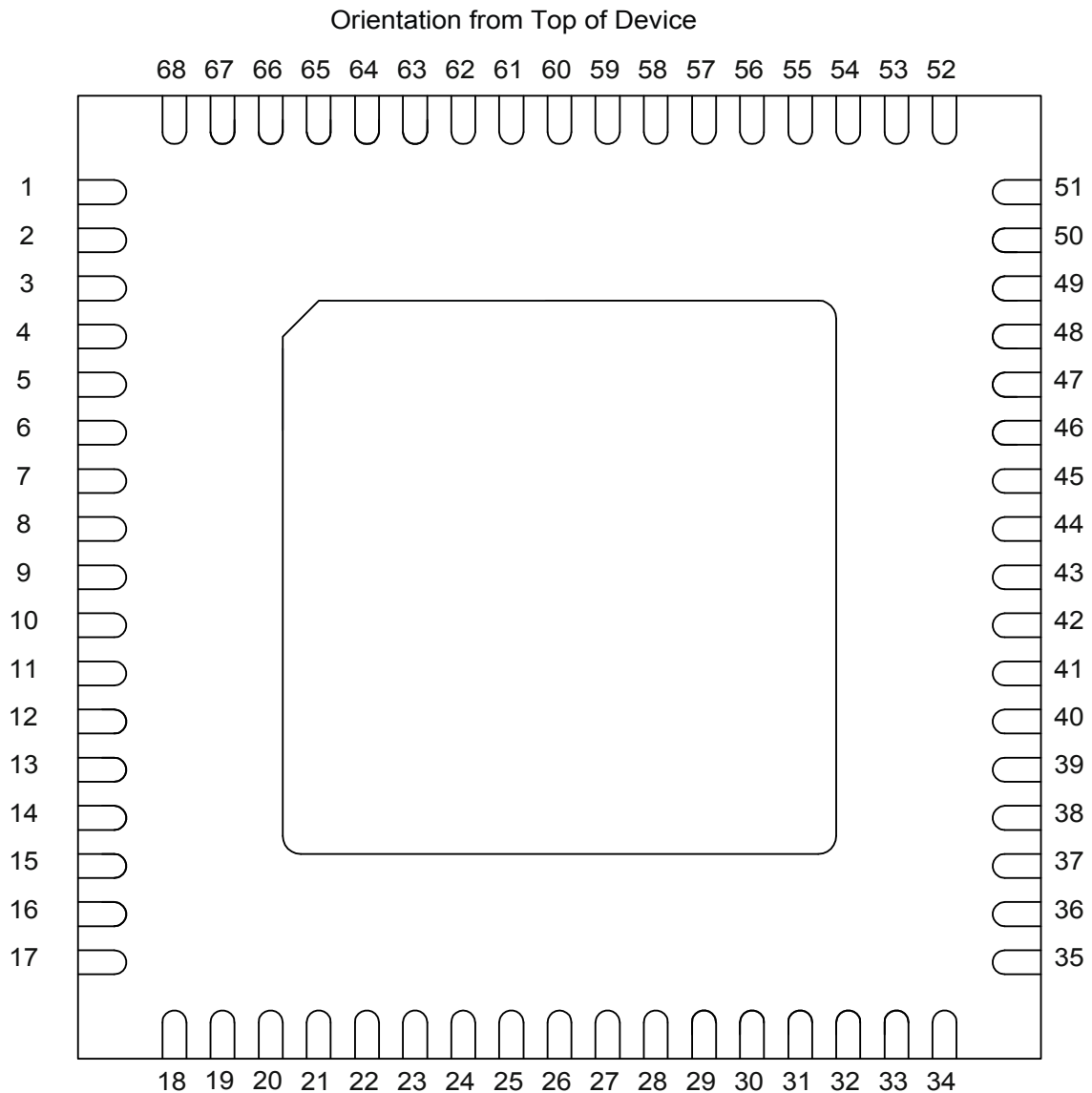


Figure 1.1: Device Pinout

1.2 Device Terminal Functions

Radio	Lead	Pad Type	Supply Domain	Description
BT_RF	12	RF	VDD_BT_RADIO	Bluetooth 50 Ω transmitter output / receiver input

Oscillator	Lead	Pad Type	Supply Domain	Description
XTAL_IN	19	Analogue	VDD_AUX	For crystal or external clock input
XTAL_OUT	18	Analogue	VDD_AUX	Drive for crystal

USB	Lead	Pad Type	Supply Domain	Description
USB_DP	56	Bidirectional	VDD_USB	USB data plus with selectable internal 1.5 k Ω pull-up resistor
USB_DN	55	Bidirectional	VDD_USB	USB data minus

SPI/PCM Interface	Lead	Pad Type	Supply Domain	Description
SPI_PCM#	29	Input with weak pull-down	VDD_PADS_1	SPI/PCM select input: <ul style="list-style-type: none"> ■ 0 = PCM/PIO interface ■ 1 = SPI

Note:

SPI and PCM1 interfaces are mapped as alternative functions on the PIO port.

SQIF	Lead	Pad Type	Supply Domain	Description
QSPI_FLASH_CLK	25	Bidirectional with strong pull-down	VDD_PADS_1	SPI flash clock
QSPI_FLASH_CS#	22	Bidirectional with strong pull-up	VDD_PADS_1	SPI flash chip select
QSPI_IO[3]	21	Bidirectional with strong pull-up	VDD_PADS_1	SPI flash data bit 3
QSPI_IO[2]	23	Bidirectional with strong pull-up	VDD_PADS_1	SPI flash data bit 2
QSPI_IO[1]	31	Bidirectional with strong pull-down	VDD_PADS_1	SPI flash data bit 1
QSPI_IO[0]	26	Bidirectional with strong pull-down	VDD_PADS_1	SPI flash data bit 0

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[21]	64	Bidirectional with weak pull-down	VDD_PADS_2	Programmable input / output line 21.
PIO[18]	65	Bidirectional with weak pull-down	VDD_PADS_2	Programmable input / output line 18.
PIO[17]	32	Bidirectional with strong pull-down	VDD_PADS_1	Programmable input / output line 17. Alternative function: <ul style="list-style-type: none"> UART_CTS: UART clear to send, active low
PIO[16]	27	Bidirectional with strong pull-up	VDD_PADS_1	Programmable input / output line 16. Alternative function: <ul style="list-style-type: none"> UART_RTS: UART request to send, active low
PIO[9]	58	Bidirectional with strong pull-down	VDD_PADS_2	Programmable input / output line 9. Alternative function: <ul style="list-style-type: none"> UART_CTS: UART clear to send, active low PCM2_CLK: PCM2 synchronous data clock I2S2_SCK: I2S2 synchronous data clock
PIO[8]	61	Bidirectional with strong pull-up	VDD_PADS_2	Programmable input / output line 8. Alternative function: <ul style="list-style-type: none"> UART_RTS: UART request to send, active low PCM2_IN: PCM2 synchronous data input I2S2_SD_IN: I2S2 synchronous data input
PIO[7]	57	Bidirectional with strong pull-down	VDD_PADS_2	Programmable input / output line 7. Alternative function: <ul style="list-style-type: none"> PCM2_SYNC: PCM2 synchronous data sync I2S2_WS: I2S2 word select
PIO[6]	62	Bidirectional with strong pull-down	VDD_PADS_2	Programmable input / output line 6. Alternative function: <ul style="list-style-type: none"> PCM2_OUT: PCM2 synchronous data output I2S2_SD_OUT: I2S2 synchronous data output
PIO[5]	34	Bidirectional with weak pull-down	VDD_PADS_1	Programmable input / output line 5. Alternative function: <ul style="list-style-type: none"> SPI_CLK: SPI clock PCM1_CLK: PCM1 synchronous data clock I2S1_SCK: I2S1 synchronous data clock

PIO Port	Lead	Pad Type	Supply Domain	Description
PIO[4]	24	Bidirectional with weak pull-down	VDD_PADS_1	Programmable input / output line 4. Alternative function: <ul style="list-style-type: none"> SPI_CS#: chip select for SPI, active low PCM1_SYNC: PCM1 synchronous data sync I2S1_WS: I²S1 word select
PIO[3]	28	Bidirectional with weak pull-down	VDD_PADS_1	Programmable input / output line 3. Alternative function: <ul style="list-style-type: none"> SPI_MISO: SPI data output PCM1_OUT: PCM1 synchronous data output I2S1_SD_OUT: I²S1 synchronous data output
PIO[2]	30	Bidirectional with weak pull-down	VDD_PADS_1	Programmable input / output line 2. Alternative function: <ul style="list-style-type: none"> SPI_MOSI: SPI data input PCM1_IN: PCM1 synchronous data input I2S1_SD_IN: I²S1 synchronous data input
PIO[1]	60	Bidirectional with strong pull-up	VDD_PADS_2	Programmable input / output line 1. Alternative function: <ul style="list-style-type: none"> UART_TX: UART data output AMP_I2C_SDA: I²C serial data line for external amplifier control
PIO[0]	59	Bidirectional with strong pull-up	VDD_PADS_2	Programmable input / output line 0. Alternative function: <ul style="list-style-type: none"> UART_RX: UART data input AMP_I2C_SCL: I²C serial clock line for external amplifier control
AIO[0]	20	Bidirectional	VDD_AUX	Analogue programmable input / output line 0.

Test and Debug	Lead	Pad Type	Supply Domain	Description
RST#	35	Input with strong pull-up	VDD_PADS_1	Reset if low. Pull low for minimum 5 ms to cause a reset.

Codec	Lead	Pad Type	Supply Domain	Description
MIC_BIAS	2	Analogue in	VDD_AUDIO	Microphone bias
AU_REF	1	Analogue in	VDD_AUDIO	Decoupling of audio reference (for high-quality audio)
SPKR_RN	6	Analogue out	VDD_AUDIO_DRV	Speaker output negative, right
SPKR_RP	7	Analogue out	VDD_AUDIO_DRV	Speaker output positive, right

Codec	Lead	Pad Type	Supply Domain	Description
SPKR_LN	9	Analogue out	VDD_AUDIO_DRV	Speaker output negative, left
SPKR_LP	10	Analogue out	VDD_AUDIO_DRV	Speaker output positive, left
LINE/MIC_AN	67	Analogue in	VDD_AUDIO	Line or microphone input negative, channel A
LINE/MIC_AP	68	Analogue in	VDD_AUDIO	Line or microphone input positive, channel A
LINE_BN	4	Analogue in	VDD_AUDIO	Line input negative, channel B
LINE_BP	5	Analogue in	VDD_AUDIO	Line input positive, channel B

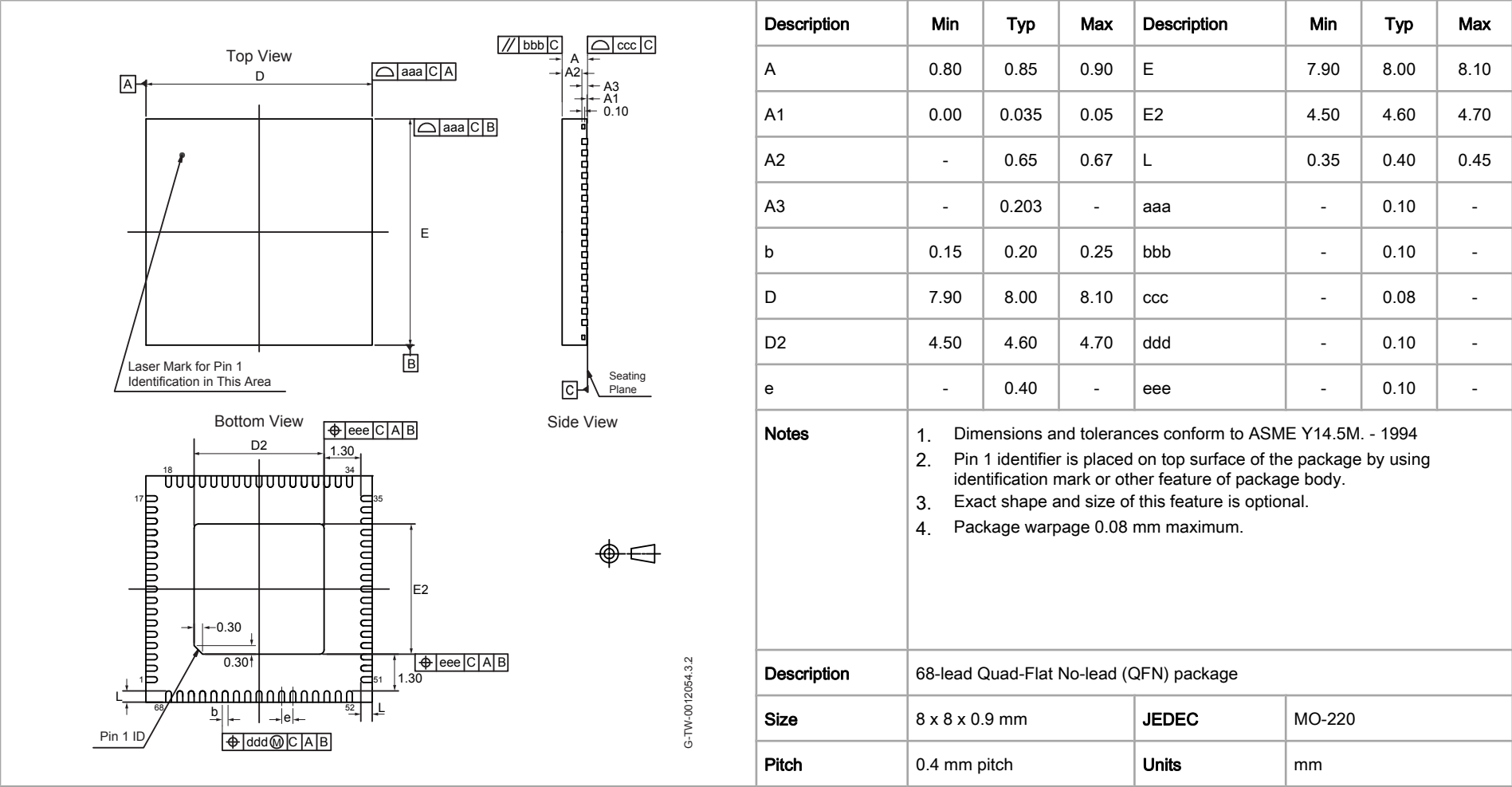
LED Drivers	Lead	Pad Type	Supply Domain	Description
LED[2]	66	Bidirectional	VDD_PADS_2	LED driver. Alternative function: programmable output PIO[31] Note: As output is open-drain, an external pull-up is required when PIO[31] is configured as a programmable output.
LED[1]	36	Bidirectional	VDD_PADS_1	LED driver. Alternative function: programmable output PIO[30]. Note: As output is open-drain, an external pull-up is required when PIO[30] is configured as a programmable output.
LED[0]	37	Bidirectional	VDD_PADS_1	LED driver. Alternative function: programmable output PIO[29]. Note: As output is open-drain, an external pull-up is required when PIO[29] is configured as a programmable output.

Power Supplies and Control	Lead	Description
CHG_EXT	43	External battery charger control. External battery charger transistor base control when using external charger boost. Otherwise leave unconnected.
LX_1V35	50	1.35 V switch-mode power regulator inductor connection.
LX_1V8	47	1.8 V switch-mode power regulator inductor connection.
SMPS_1V35_SENSE	52	1.35 V switch-mode power regulator sense input.
SMPS_1V8_SENSE	53	1.8 V switch-mode power regulator sense input.

Power Supplies and Control	Lead	Description
SMP_BYP	49	Supply via bypass regulator for 1.8 V and 1.35 V switch-mode power supply regulator inputs. Must be connected to the same potential as VOUT_3V3.
SMP_VBAT	48	1.8 V and 1.35 V switch-mode power supply regulator inputs. Must be at the same potential as VBAT.
VSS_SMPS_1V35	51	1.35 V switch-mode regulator ground.
VSS_SMPS_1V8	46	1.8 V switch-mode regulator ground.
VBAT	45	Battery positive terminal.
VBAT_SENSE	44	Battery charger sense input, connect as Section 11 shows.
VCHG	42	Charger input. Typically connected to VBUS (USB supply) as Section 11 shows.
VDD_ANA	17	Analogue LDO linear regulator output (1.35 V). Connect to 1.35 V supply, see Section 11 for connections.
VDD_AUDIO	3	Positive supply for audio. Connect to 1.35 V supply, see Section 11 for connections.
VDD_AUDIO_DRV	8	Positive supply for audio output amplifiers. Connect to 1.8 V supply, see Section 11 for connections.
VDD_AUX	14	Auxiliary supply. Connect to 1.35 V supply, see Section 11 for connections.
VDD_AUX_1V8	15, 16	Auxiliary LDO regulator input. Connect to 1.8 V supply, see Section 11 for connections.
VDD_BT_LO	13	Bluetooth radio local oscillator supply (1.35 V). Connect to 1.35 V supply, see Section 11 for connections.
VDD_BT_RADIO	11	Bluetooth radio supply. Connect to 1.35 V supply, see Section 11 for connections.
VDD_DIG	38	Digital LDO regulator output, see Section 11 for connections.
VDD_PADS_1	33	Positive supply input for input/output ports.

Power Supplies and Control	Lead	Description
VDD_PADS_2	63	Positive supply input for input/output ports.
VDD_USB	54	Positive supply for USB port.
VOUT_3V3	41	3.3 V bypass linear regulator output. Connect external minimum 2.2 μ F ceramic decoupling capacitor.
VREGENABLE	40	Regulator enable input. Can also be sensed as an input. Regulator enable and multifunction button. A high input (tolerant to VBAT) enables the on-chip regulators, which can then be latched on internally and the button used as a multifunction input.
VREGIN_DIG	39	Digital LDO regulator input, see Section 11 for connections. Typically connected to a 1.35 V supply.
VSS	Exposed pad	Ground connections.

1.3 Package Dimensions



1.4 PCB Design and Assembly Considerations

This section lists recommendations to achieve maximum board-level reliability of the 8 x 8 x 0.9 mm QFN 68-lead package:

- NSMD lands (lands smaller than the solder mask aperture) are preferred, because of the greater accuracy of the metal definition process compared to the solder mask process. With solder mask defined pads, the overlap of the solder mask on the land creates a step in the solder at the land interface, which can cause stress concentration and act as a point for crack initiation.
- CSR recommends that the PCB land pattern is in accordance with IPC standard IPC-7351.
- Solder paste must be used during the assembly process.

1.5 Typical Solder Reflow Profile

For information, see *Typical Solder Reflow Profile for Lead-free Devices Information Note*.

2 Bluetooth Modem

The Bluetooth modem includes:

- RF ports
- RF receiver
- RF transmitter
- Bluetooth radio synthesiser
- Baseband

2.1 RF Ports (BT_RF)

CSRA64210 QFN contains an on-chip balun which combines the balanced outputs of the PA on transmit and produces the balanced input signals for the LNA required on receive. No matching components are needed as the receive mode impedance is $50\ \Omega$ and the transmitter has been optimised to deliver power into a $50\ \Omega$ load.

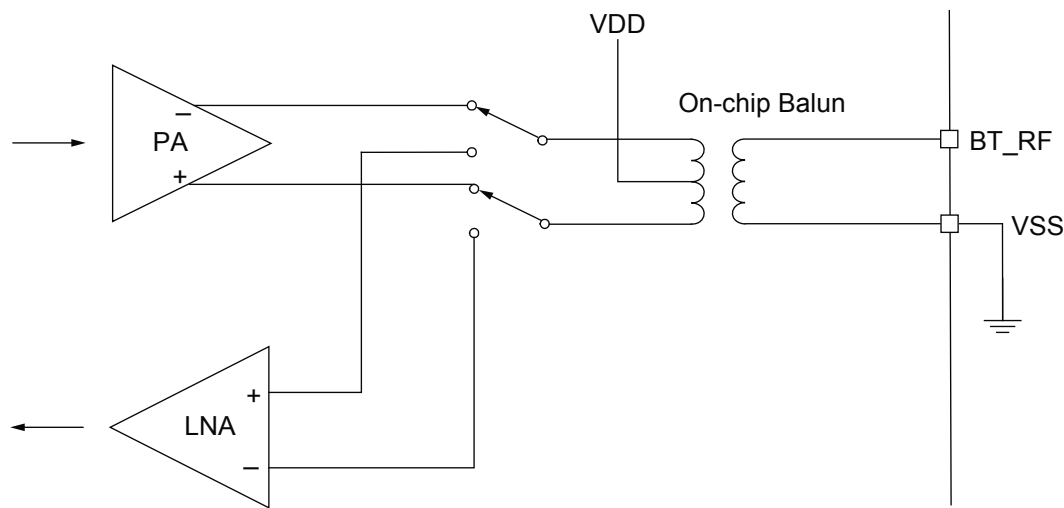


Figure 2.1: Simplified Circuit BT_RF

2.2 RF Receiver

The receiver features a near-zero IF architecture that enables the channel filters to be integrated onto the die. Sufficient out-of-band blocking specification at the LNA input enables the receiver to operate in close proximity to GSM and W-CDMA cellular phone transmitters without being desensitised. A digital FSK discriminator means that no discriminator tank is needed and its excellent performance in the presence of noise enables CSRA64210 QFN to exceed the Bluetooth requirements for co-channel and adjacent channel rejection.

2.2.1 Low Noise Amplifier

The LNA operates in differential mode and takes its input from the balanced port of the on-chip balun.

2.2.2 RSSI Analogue to Digital Converter

The ADC implements fast AGC. The ADC samples the RSSI voltage on a slot-by-slot basis. The front-end LNA gain is changed according to the measured RSSI value, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference-limited environments.

2.3 RF Transmitter

2.3.1 IQ Modulator

The transmitter features a direct IQ modulator to minimise frequency drift during a transmit timeslot, which results in a controlled modulation index. Digital baseband transmit circuitry provides the required spectral shaping.

2.3.2 Power Amplifier

The internal PA output power is software controlled and configured through a PS Key. The internal PA on the CSRA64210 QFN has a maximum output power that enables it to operate as a Class 1, Class 2 and Class 3 Bluetooth radio without requiring an external RF PA.

2.4 Bluetooth Radio Synthesiser

The Bluetooth radio synthesiser is fully integrated onto the die with no requirement for an external VCO screening can, varactor tuning diodes, LC resonators or loop filter. The synthesiser is guaranteed to lock in sufficient time across the guaranteed temperature range to meet the Bluetooth v4.2 specification.

2.5 Baseband

The baseband handles the digital functions of the Bluetooth modem, for example the Burst Mode Controller and Physical Layer Hardware Engine.

3 Clock Generation

CSRA64210 QFN accepts a reference clock input from either a crystal or an external clock source, e.g. a TCXO.

The external reference clock is required in active and deep sleep modes and must be present when CSRA64210 QFN is enabled.

3.1 Crystal

Figure 3.1 shows the CSRA64210 QFN contains a crystal driver circuit that acts as a transconductance amplifier that drives an external crystal connected between XTAL_IN and XTAL_OUT. The crystal driver circuit forms a Pierce oscillator with the external crystal. External capacitors are not required for standard crystals that require a load capacitance of around 9pF. CSR recommends this option.

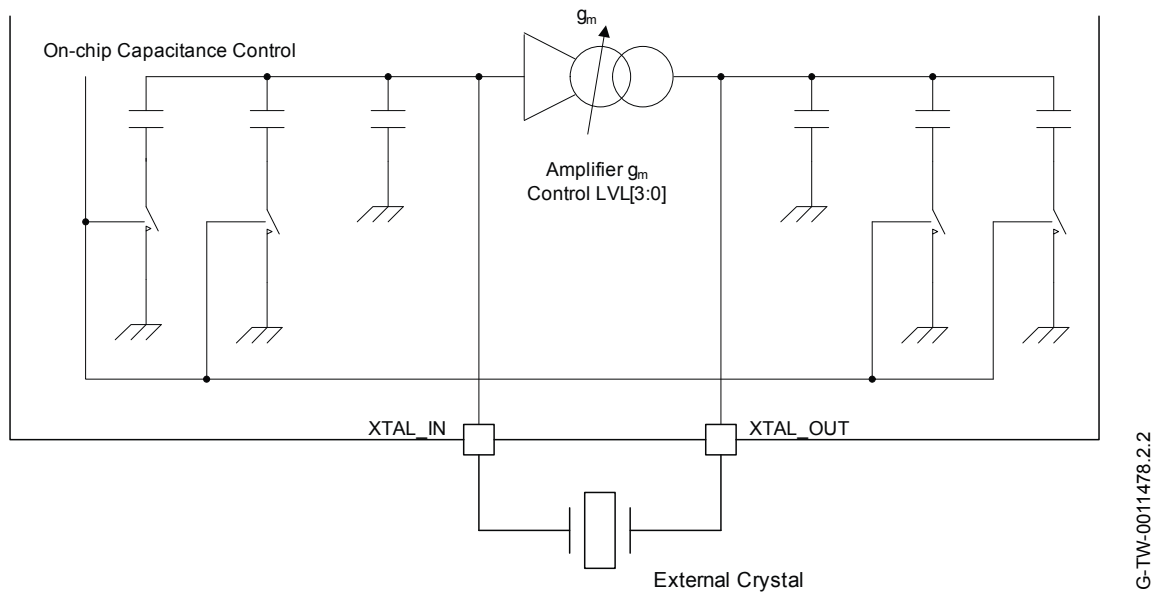


Figure 3.1: Crystal Oscillator Overview

The on-chip capacitance is adjusted using PSKEY_XTAL_OSC_CONFIG, see Table 3.1. The default values suit a typical crystal requiring a 9 pF load capacitance. In deep sleep mode, the crystal oscillation is maintained, but at a lower drive strength to reduce power consumption. The drive strength and load capacitance are configured with a PS Key.

	Normal Mode PSKEY_XTAL_OSC_CONFIG [3:2]				Low Power Mode PSKEY_XTAL_OSC_CONFIG [1:0]			
Value	00	01	10	11	00	01	10	11
XTAL_IN (Typical)	15.6 pF	10.8 pF	6.0 pF	1.1 pF	15.6 pF	10.8 pF	6.0 pF	1.1 pF
XTAL_OUT (Typical)	20.8 pF	16.0 pF	11.2 pF	6.4 pF	16.0 pF	11.2 pF	6.4 pF	1.5 pF

Table 3.1: Typical On-chip Capacitance Values

The drive strength is configured with PSKEY_XTAL_LVL. The default level for this PS Key is sufficient for typical crystals. The level control is set in the range 0 to 15, where 15 is the maximum drive level.

Increasing the crystal amplifier drive level increases the transconductance of the crystal amplifier, which creates an increase in the oscillator margin (ratio of oscillator amplifiers is equivalent to the negative resistance of the crystal ESR).

Note:

Excessive amplifier transconductance can lead to an increase in the oscillator phase noise if the oscillator amplifier is excessively overdriven. Set the transconductance to the minimum level to give the desired oscillation ratio. Higher values can increase power consumption. Also, insufficient drive strength can prevent the the crystal from starting to oscillate.

3.1.1 Negative Resistance Model

The crystal and its load capacitor can be modelled as a frequency dependant resistive element. Consider the driver amplifier as a circuit that provides negative resistance. For oscillation, the value of the negative resistance should be greater than that of the crystal circuit equivalence resistance. Equation 3.1 shows how to calculate the equivalent negative resistance.

$$R_{neg} = -\frac{g_m C_{in} C_{out}}{2\pi f^2 (C_{out} C_{in} + (C_0 + C_{int})(C_{out} + C_{in}))^2}$$

Equation 3.1: Negative Resistance

Where:

- g_m = Transconductance of the crystal oscillator amplifier
- C_0 = Static capacitance of the crystal, which is sometimes referred to as the shunt or case capacitance
- C_{int} = On-chip parasitic capacitance between input and output of XTAL amplifier.
- C_{in} = Internal capacitance on XTAL_IN, see Table 3.1
- C_{out} = Internal capacitance on XTAL_OUT, see Table 3.1

Parameter	Min	Typ	Max	Unit
Transconductance	2	-	-	mS
C_{int}	-	1.5	-	pF

Table 3.2: Transconductance and On-chip Parasitic Capacitance

3.1.2 Crystal Specification

Table 3.3 shows the specification for an external crystal.

Parameter	Min	Typ	Max	Unit
Frequency	16	26	32	MHz
Initial Frequency error from nominal frequency which can be compensated for	-	-	±285	ppm
Frequency Stability	-	-	±20	ppm
Crystal ESR	-	-	60	Ω

Table 3.3: Crystal Specification

3.1.3 Crystal Calibration

The actual crystal frequency depends on the capacitance of XTAL_IN and XTAL_OUT on the PCB and the CSRA64210 QFN, as well as the capacitance of the crystal.

The Bluetooth specification requires ± 20 ppm clock accuracy. The actual frequency at which a crystal oscillates contains two error terms, which are typically mentioned in the crystal device datasheets:

- Initial Frequency Error: The difference between the desired frequency and the actual oscillating frequency caused by the crystal itself and its PCB connections. It is also called as Calibration Tolerance or Frequency Tolerance.
- Frequency Stability: The total of how far the crystal can move off frequency with temperature, aging or other effects. It is also called as Temperature Stability, Frequency Stability or Aging.

CSRA64210 QFN has the capability to compensate for Initial Frequency errors by a simple per-device basis on the production line, with the trim value stored in the non-volatile memory (PS Key). However, it is not possible to compensate for frequency stability, therefore a crystal must be chosen with a Frequency Stability that is better than ± 20 ppm clock accuracy.

Some crystal datasheets combine both these terms into one tolerance value. This causes a problem because only the initial frequency error can be compensated for and CSRA64210 QFN cannot compensate for the temperature or aging performance. If frequency stability is not explicitly stated, CSR cannot guarantee remaining within the Bluetooth's ± 20 ppm frequency accuracy specification.

Crystal calibration uses a single measurement of RF output frequency and can be performed quickly as part of the product final test. Typically, a TXSTART radio command is sent and then a measurement of the output RF frequency is read. From this, the calibration factor to correct actual offset from the desired frequency can be calculated. This offset value is stored in PSKEY_ANA_FTRIM_OFFSET. CSRA64210 QFN then compensates for the initial frequency offset of the crystal.

The value in PSKEY_ANA_FTRIM_OFFSET is a 16-bit 2's complement signed integer which specifies the fractional part of the ratio between the true crystal frequency, f_{actual} , and the value set in PSKEY_ANA_FREQ, f_{nominal} . Equation 3.2 shows the value of PSKEY_ANA_FTRIM_OFFSET in parts per 2^{20} rounded to the nearest integer.

$$\text{PSKEY_ANA_FTRIM_OFFSET} = \left(\frac{f_{\text{actual}}}{f_{\text{nominal}}} - 1 \right) \times 2^{20}$$

Equation 3.2: Crystal Calibration Using PSKEY_ANA_FTRIM_OFFSET

For more information on TXSTART radio test see *BlueTest User Guide*.

3.2 Non-crystal Oscillator

Apply the external reference clock to the CSRA64210 QFN XTAL_IN input. Connect XTAL_OUT to ground.

The external clock is either a low-level sinusoid, or a digital-level square wave. The clock must meet the specification in Table 3.4. The external reference clock is required in active and deep sleep modes, it must be present when CSRA64210 QFN is enabled.

		Min	Typ	Max	Unit
Frequency ^(a)		19.2	26	40	MHz
Duty cycle		40:60	50:50	60:40	-
Edge jitter (at zero crossing)		-	-	10	ps _{rms} ^(b)
Signal level	AC coupled sinusoid amplitude	0.2	0.4	VDD_AUX ^(c)	V
	DC coupled digital extremes	0	-	VDD_AUX ^(c)	V
	DC coupled digital digital amplitude	0.4	-	1.2	V pk-pk
XTAL_IN input impedance		30	-	-	kΩ
XTAL_IN input capacitance		-	-	1	pF

Table 3.4: External Clock Specifications

^(a) The frequency should be an integer multiple of 250 kHz except for the CDMA/3G frequencies

^(b) 100 Hz to 1 MHz

^(c) VDD_AUX is 1.35 V nominal

3.2.1 XTAL_IN Impedance in Non-crystal Mode

The impedance of XTAL_IN does not change significantly between operating modes. When transitioning from deep sleep to active states, the capacitive load can change. For this reason, CSR recommends using a buffered clock input.

4 Processors

4.1 Bluetooth Stack Microcontroller

The CSRA64210 QFN uses a 16-bit RISC 80 MHz MCU for low power consumption and efficient use of memory. It contains a single-cycle multiplier and a memory protection unit.

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and host interfaces.

4.2 Kalimba DSP

The Kalimba DSP performs signal processing functions on over-air data or codec data to enhance audio applications. The key features of the DSP include:

- 80 MIPS performance, 24-bit fixed point DSP core
- Single-cycle MAC; 24 x 24-bit multiply and 56-bit accumulate includes 2 rMAC registers and new instructions for improved performance over previous architecture
- 32-bit instruction word
- Separate program memory and dual data memory, enabling an ALU operation and up to 2 memory accesses in a single cycle
- Zero overhead looping, including a very low-power 32-instruction cache
- Zero overhead circular buffer indexing
- Single cycle barrel shifter with up to 56-bit input and 56-bit output
- Multiple cycle divide (performed in the background)
- Bit reversed addressing
- Orthogonal instruction set
- Low overhead interrupt

5 Memory Interface and Management

5.1 Memory Management Unit

The MMU provides buffers that hold the data in transit between the host, the air or the Kalimba DSP. The use of DMA ports also helps with efficient transfer of data to other peripherals.

5.2 System RAM

56 KB of integrated RAM supports the RISC MCU.

5.3 Kalimba DSP RAM

Additional integrated RAM provides support for the Kalimba DSP:

- 16K x 24-bit for data memory 1 (DM1)
- 16K x 24-bit for data memory 2 (DM2)
- 6K x 32-bit for program memory (PM)

5.4 Internal ROM

Internal ROM is provided for system firmware implementation.

5.5 Serial Quad I/O Flash Interface (SQIF)

The CSRA64210 QFN uses external serial flash ICs for storage of device-specific data. The CSRA64210 QFN supports a 4-bit I/O flash-memory interface. Figure 5.1 shows a typical connection between the CSRA64210 QFN and a serial flash IC.

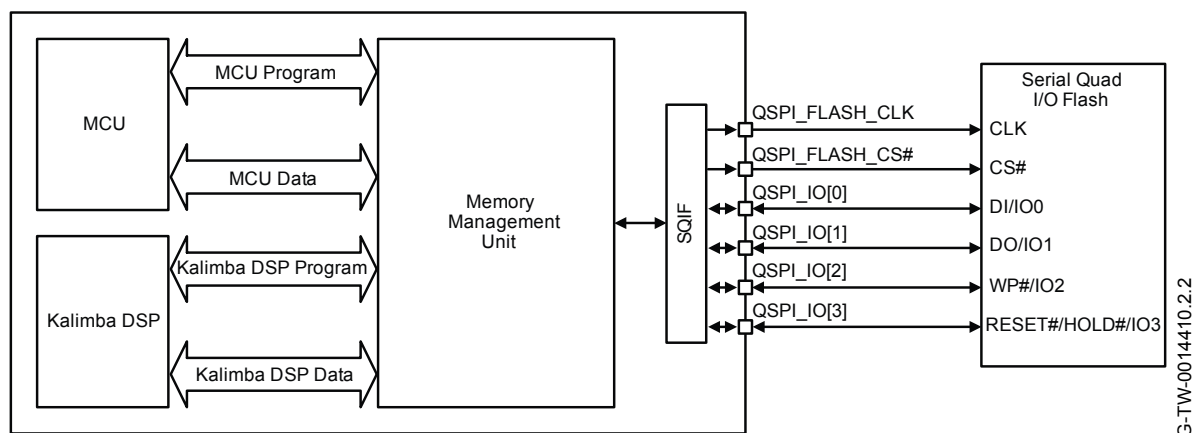


Figure 5.1: Serial Quad I/O Flash Interface

The SQIF interface on the CSRA64210 QFN supports:

- Flash serial memory, which is also visible in the MCU and Kalimba DSP program address space
- MCU and Kalimba DSP data access through a generic window
- Concurrent program and / or data accesses from the MCU and / or Kalimba DSP (although efficiency suffers)
- Separate prefetch buffers for MCU program, MCU data, Kalimba DSP program, Kalimba DSP data:
 - Each buffer is 4 x 16-bit
 - Defined minimum length prefetch
 - Prefetch continues if accesses are contiguous (and buffer not full)
 - Prefetch does not automatically restart as buffer empties
 - Prefetch is enabled and disabled by software control, which enables optimisation of sequential / random data access patterns
- Serial flash devices up to 64 Mb with 4-bit wide transfers, see firmware release note for up-to-date device support
- Flash performance:

- Clocks up to 80/16 MHz
- The control and address overhead is 14/24 cycles per burst read, with support for Word Read Quad Continuous (Winbond) and High Speed Read Quad (Microchip (SST)). Microchip (SST) indexed instructions are not supported.
- Data transfer is 4/16 cycles per 16-bits.
- Flash instruction sequences:
 - Requires considerable (run-time) programmable configuration
 - Set up for either read, or write (not both)
 - Software configures SQIF for specific flash attached
- All other management of serial flash via software:
 - Memory mapped registers support transfers of data to and from the flash
 - Software needs to read the serial flash JEDEC ID in order to index a table of flash characteristics
 - Software driven sequence to enable, e.g. the Winbond Continuous Read Mode

6 Serial Interfaces

6.1 USB Interface

CSRA64210 QFN has a full-speed (12 Mbps) USB interface for communicating with other compatible digital devices. The USB interface on CSRA64210 QFN acts as a USB peripheral, responding to requests from a master host controller.

CSRA64210 QFN contains internal USB termination resistors and requires no external resistor matching.

CSRA64210 QFN supports the *Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification)*, supports USB standard charger detection and fully supports the *USB Battery Charging Specification*, available from <http://www.usb.org>. For more information on how to integrate the USB interface on CSRA64210 QFN, see the *Bluetooth and USB Design Considerations Application Note*.

As well as describing USB basics and architecture, the application note describes:

- Power distribution for high and low bus-powered configurations
- Power distribution for self-powered configuration, which includes USB VBUS monitoring
- USB enumeration
- Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads
- USB suspend modes and Bluetooth low-power modes:
 - Global suspend
 - Selective suspend, includes remote wake
 - Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend
 - Suspend mode current draw
 - PIO status in suspend mode
 - Resume, detach and wake PIOs
- Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS voltage consideration
- USB termination when interface is not in use
- Internal modules, certification and non-specification compliant operation

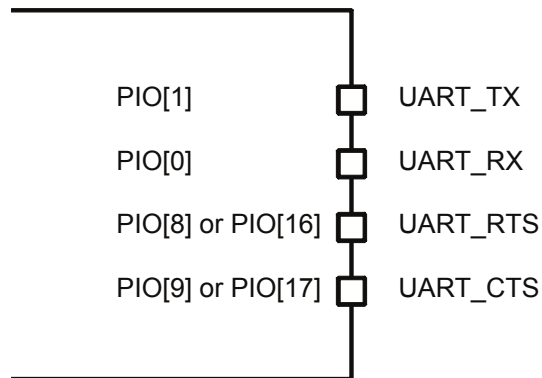
6.2 UART Interface

CSRA64210 QFN has an optional UART serial interface that provides a simple mechanism for communicating with other serial devices using the RS232 protocol, including for test and debug. The UART interface is multiplexed with PIOs and other functions, and hardware flow control is optional. Table 6.1 shows the PS Keys for configuring this multiplexing.

PS Key	PIO Location Option
PSKEY_UART_RX_PIO	PIO[0]
PSKEY_UART_TX_PIO	PIO[1]
PSKEY_UART_RTS_PIO	PIO[8] (default) or PIO[16]
PSKEY_UART_CTS_PIO	PIO[9] (default) or PIO[17]

Table 6.1: PS Keys for UART/PIO Multiplexing

Figure 6.1 shows the 4 signals that implement the UART function.



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Figure 6.1: Universal Asynchronous Receiver

When CSRA64210 QFN is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. The remaining 2 signals, UART_CTS and UART_RTS, implement optional RS232 hardware flow control where both are active low indicators.

UART configuration parameters, such as baud rate and packet format, are set using CSRA64210 QFN firmware.

Note:

To communicate with the UART at its maximum data rate using a standard PC, the PC requires an accelerated serial port adapter card.

Table 6.2 shows the possible UART settings.

Parameter		Possible Values
Baud rate	Minimum	1200 baud ($\leq 2\%$ Error)
		9600 baud ($\leq 1\%$ Error)
	Maximum	4 Mbaud ($\leq 1\%$ Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 6.2: Possible UART Settings

Table 6.3 lists common baud rates and their associated error values for PSKEY_UART_BITRATE. To set the UART baud rate, load PSKEY_UART_BITRATE with the number of bits per second.

Baud Rate	PS Key Value (Bits Per Second)	Error
1200	1200	1.73%
2400	2400	1.73%
4800	4800	1.73%

Baud Rate	PS Key Value (Bits Per Second)	Error
9600	9600	-0.82%
19200	19200	0.45%
38400	38400	-0.18%
57600	57600	0.03%
76800	76800	0.14%
115200	115200	0.03%
230400	230400	0.03%
460800	460800	-0.02%
921600	921600	0.00%
1382400	1382400	-0.01%
1843200	1843200	0.00%
2764800	2764800	0.00%
3686400	3686400	0.00%

Table 6.3: Standard Baud Rates

6.3 Programming and Debug Interface

CSRA64210 QFN provides a debug SPI interface for programming, configuring (PS Keys) and debugging the CSRA64210 QFN. Access to this interface is required in production. Ensure the 4 SPI signals and the SPI_PCM# line are brought out to either test points or a header. To use the SPI interface, the SPI_PCM# line requires the option of being pulled high externally.

CSR provides development and production tools to communicate over the SPI from a PC, although a level translator circuit is often required. All are available from CSR.

6.3.1 Multi-slave Operation

Avoid connecting CSRA64210 QFN in a multi-slave arrangement by simple parallel connection of slave MISO lines. When CSRA64210 QFN is deselected (SPI_CS# = 1), the SPI_MISO line does not float. Instead, CSRA64210 QFN outputs 0 if the processor is running or 1 if it is stopped.

6.4 I²C Interface

The CSRA64210 QFN supports an I²C interface for I/O port expansion. Its primary function is to control an external audio power amplifier. The I²C interface is multiplexed onto the PIOs on the CSRA64210 QFN as follows:

- PIO[0] is the I²C interface SCL line (AMP_I2C_SCL)
- PIO[1] is the I²C interface SDA line (AMP_I2C_SDA)

PIOs used for I²C can be configured by PS Keys.

Note:

The I²C interface requires external pull-up resistors. Ensure that external pull-up resistors are suitably sized for the I²C interface speed and PCB track capacitance.

7 Interfaces

7.1 Programmable I/O Ports, PIO

CSRA64210 QFN provides up to 14 lines of programmable bidirectional I/O, PIO[21,18:16,9:0]. Table 7.1 lists the PIOs on the CSRA64210 QFN that have alternative functions.

PIO	Function					
	Debug SPI	SPI Flash	UART	I ² C	PCM	I ² S
PIO[0]	-	-	UART_RX	AMP_I2C_SCL	-	-
PIO[1]	-	-	UART_TX	AMP_I2C_SDA	-	-
PIO[2]	SPI_MOSI	-	-	-	PCM1_IN	I2S1_SD_IN
PIO[3]	SPI_MISO	-	-	-	PCM1_OUT	I2S1_SD_OUT
PIO[4]	SPI_CS#	-	-	-	PCM1_SYNC	I2S1_WS
PIO[5]	SPI_CLK	-	-	-	PCM1_CLK	I2S1_SCK
PIO[6]	-	-	-	-	PCM2_OUT	I2S2_SD_OUT
PIO[7]	-	-	-	-	PCM2_SYNC	I2S2_WS
PIO[8]	-	-	UART_RTS	-	PCM2_IN	I2S2_SD_IN
PIO[9]	-	-	UART_CTS	-	PCM2_CLK	I2S2_SCK
PIO[16]	-	-	UART_RTS	-	-	-
PIO[17]	-	-	UART_CTS	-	-	-
PIO[18]	-	-	-	-	-	-
PIO[21]	-	-	-	-	-	-

Table 7.1: Alternative PIO Functions

Note:

See the relevant software release note for the implementation of these PIO lines, as they are firmware build-specific.

To change the default assignment shown for some alternative functions, use PS Keys.

7.2 Analogue I/O Ports, AIO

CSRA64210 QFN has 1 general-purpose analogue interface pin, AIO[0]. Typically, this connects to a thermistor for battery pack temperature measurements during charge control. See Section 11 for typical connections.

7.3 LED Drivers

The CSRA64210 QFN includes a 3-pad synchronised PWM LED driver for driving RGB LEDs for producing a wide range of colours. All LEDs are controlled by firmware.

The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.

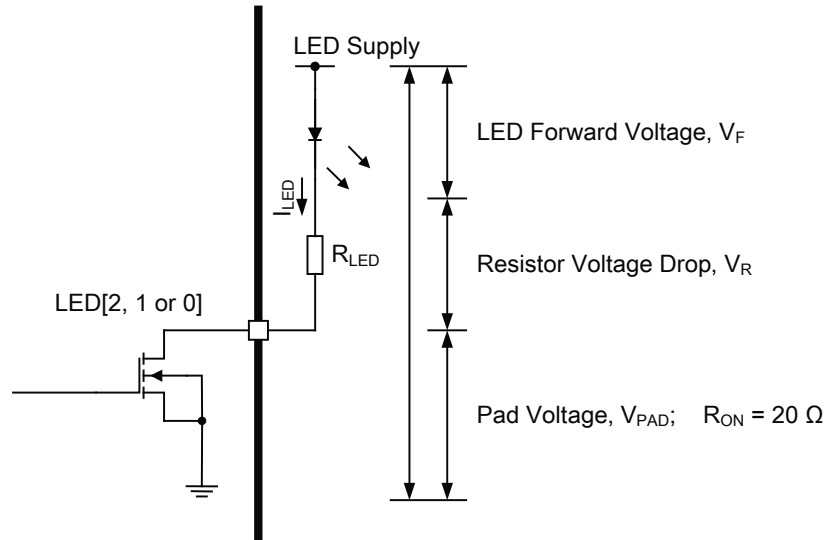


Figure 7.1: LED Equivalent Circuit

From Figure 7.1 it is possible to derive Equation 7.1 to calculate I_{LED} . If a known value of current is required through the LED to give a specific luminous intensity, then the value of R_{LED} is calculated.

$$I_{LED} = \frac{V_{DD} - V_F}{R_{LED} + R_{ON}}$$

Equation 7.1: LED Current

For the LED pads to act as resistance, the external series resistor, R_{LED} , needs to be such that the voltage drop across it, V_R , keeps V_{PAD} below 0.5 V. Equation 7.2 also applies.

$$V_{DD} = V_F + V_R + V_{PAD}$$

Equation 7.2: LED PAD Voltage

Note:

The supply domain for LED[2:0] must remain powered for LED functions to operate.

The LED current adds to the overall current. Conservative LED selection extends battery life.

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8 Audio Interface

The audio interface circuit consists of:

- Stereo/dual-mono audio codec.
- Dual analogue audio inputs.
- Dual analogue audio outputs.
- Configurable PCM and I²S interfaces. For configuration information, contact CSR.

Figure 8.1 shows the functional blocks of the interface. The codec supports stereo/dual-mono playback and recording of audio signals at multiple sample rates with a 16-bit resolution. The ADC and the DAC of the codec each contain 2 independent high-quality channels. Any ADC or DAC channel runs at its own independent sample rate.

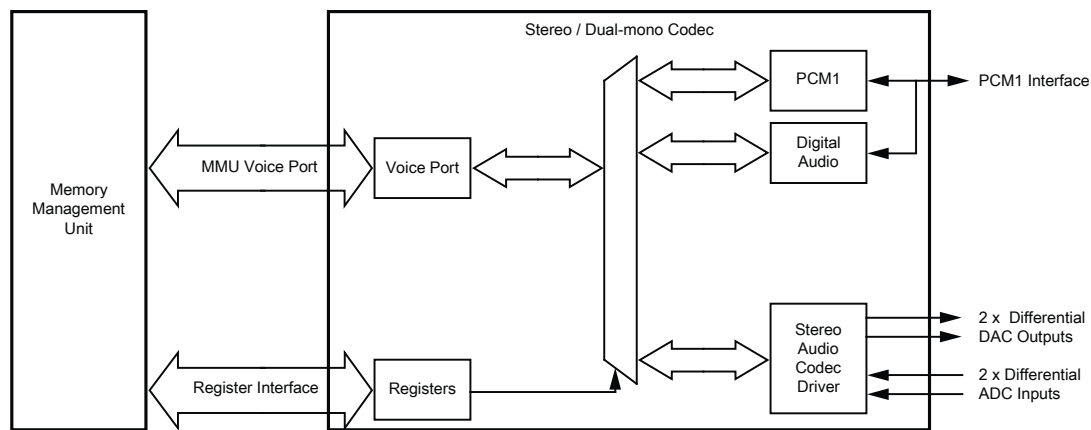


Figure 8.1: Audio Interface

The interface for the digital audio bus shares the same pins as the PCM codec interface. Table 8.1 lists the alternative functions.

PCM Interface	I ² S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 8.1: Alternative Functions of the Digital Audio Bus Interface on the PCM1 and PCM2 Interface

Important Note:

The term *PCM* in Table 8.1 and its subsections refers to the PCM1 and PCM2 interface.

8.1 Audio Input and Output

The audio input circuitry consists of 2 independent 16-bit high-quality ADC channels:

- Programmable as either stereo or dual-mono inputs
- 1 input programmable as either microphone or line input, the other as line input only
- Each channel is independently configurable to be either single-ended or fully differential
- Each channel has an analogue and digital programmable gain stage, this also aids optimisation of different microphones

The audio output circuitry consists of a dual differential class A-B output stage.

Note:

CSRA64210 QFN is designed for a differential audio output. If a single-ended audio output is required, use an external differential to single-ended converter.

8.2 Audio Codec Interface

The main features of the interface are:

- Stereo and mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band
- Support for I²S stereo digital audio bus standard
- Support for PCM interface including PCM master codecs that require an external system clock

Important Note:

To avoid any confusion regarding stereo operation this data sheet explicitly states which is the left and right channel for audio output. With respect to audio input, software and any registers, channel 0 or channel A represents the left channel and channel 1 or channel B represents the right channel.

8.2.1 Audio Codec Block Diagram

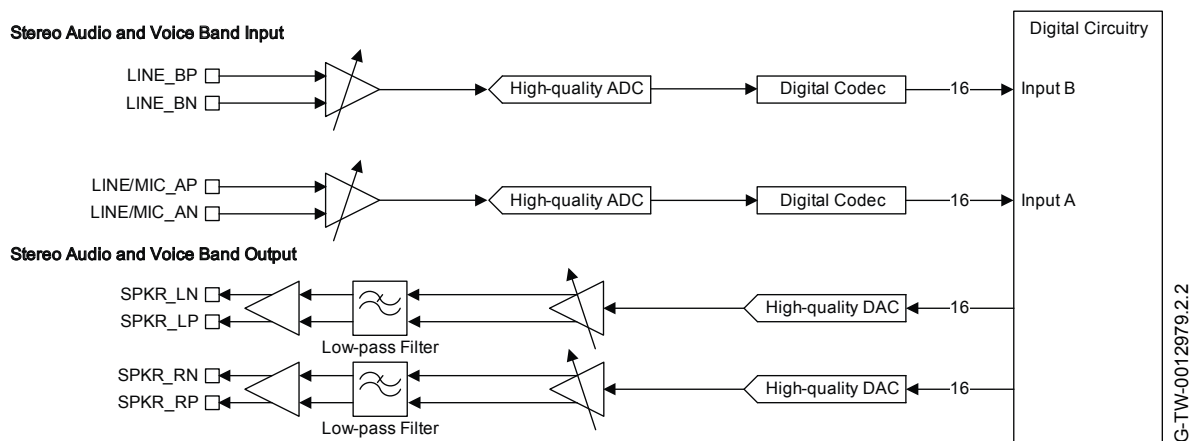


Figure 8.2: Audio Codec Input and Output Stages

The CSRA64210 QFN audio codec uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude. It operates from a dual power supply, VDD_AUDIO for the audio circuits and VDD_AUDIO_DRV for the audio driver circuits.

8.2.2 ADC

The CSRA64210 QFN consists of 2 high-quality ADCs:

- Each ADC has a second-order Sigma-Delta converter
- Each ADC is a separate channel with identical functionality
- There are 2 gain stages for each channel, 1 of which is an analogue gain stage and the other is a digital gain stage

8.2.3 ADC Sample Rate Selection

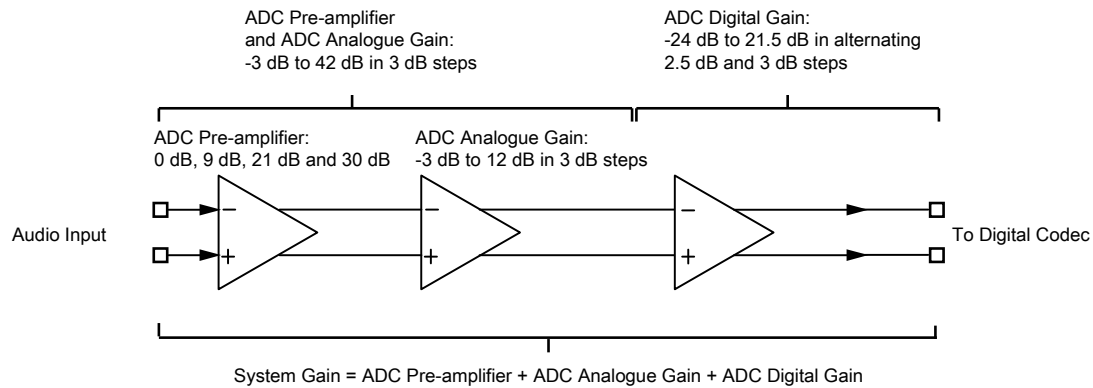
Each ADC supports the following pre-defined sample rates, although other rates are programmable, e.g. 40 kHz:

- 8 kHz
- 11.025 kHz
- 16 kHz
- 22.050 kHz
- 24 kHz
- 32 kHz
- 44.1 kHz
- 48 kHz

8.2.4 ADC Audio Input Gain

Figure 8.3 shows that the CSRA64210 QFN audio input gain consists of:

- An analogue gain stage based on a pre-amplifier and an analogue gain amplifier
- A digital gain stage



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Figure 8.3: Audio Input Gain

8.2.5 ADC Pre-amplifier and ADC Analogue Gain

CSRA64210 QFN has an analogue gain stage based on an ADC pre-amplifier and ADC analogue amplifier:

- The ADC pre-amplifier has 4 gain settings: 0 dB, 9 dB, 21 dB and 30 dB
- The ADC analogue amplifier gain is -3 dB to 12 dB in 3 dB steps
- The overall analogue gain for the pre-amplifier and analogue amplifier is -3 dB to 42 dB in 3 dB steps
- At mid to high gain levels it acts as a microphone pre-amplifier
- At low gain levels it acts as an audio line level amplifier

8.2.6 ADC Digital Gain

Table 8.2 shows that a digital gain stage inside the ADC varies between -24 dB to 21.5 dB. There is also a *fine gain interface* with a 9-bit gain setting enabling gain changes in 1/32 steps. For more information, contact CSR.

Digital Gain Selection Value	ADC Digital Gain Setting (dB)	Digital Gain Selection Value	ADC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 8.2: ADC Audio Input Gain Rate

The firmware controls the audio input gain.

8.2.7 ADC Digital IIR Filter

The ADC contains 2 integrated anti-aliasing filters:

- A *long* IIR filter suitable for music (>44.1 kHz)
- G.722 filter is a digital IIR filter that improves the stop-band attenuation required for G.722 compliance (which is the best selection for 8 kHz / 16 kHz / voice)

For more information, contact CSR.

8.2.8 DAC

The DAC consists of:

- 2 fourth-order Sigma-Delta converters enabling 2 separate channels that are identical in functionality
- 2 gain stages for each channel, 1 of which is an analogue gain stage and the other is a digital gain stage

8.2.9 DAC Sample Rate Selection

Each DAC supports the following sample rates:

- 8 kHz
- 11.025 kHz
- 16 kHz
- 22.050 kHz
- 32 kHz
- 40 kHz
- 44.1 kHz
- 48 kHz
- 96 kHz

8.2.10 DAC Digital Gain

Table 8.3 shows that a digital gain stage inside the DAC varies between -24 dB to 21.5 dB. There is also a *fine gain interface* with a 9-bit gain setting enabling gain changes in 1/32 steps, for more information contact CSR.

Digital Gain Selection Value	DAC Digital Gain Setting (dB)	Digital Gain Selection Value	DAC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

Table 8.3: DAC Digital Gain Rate Selection

The overall gain control of the DAC is controlled by the firmware. Its setting is a combined function of the digital and analogue amplifier settings.

8.2.11 DAC Analogue Gain

Table 8.4 shows the DAC analogue gain stage consists of 8 gain selection values that represent seven 3 dB steps.

Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)	Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)
7	0	3	-12
6	-3	2	-15
5	-6	1	-18
4	-9	0	-21

Table 8.4: DAC Analogue Gain Rate Selection

The firmware controls the overall gain control of the DAC. Its setting is a combined function of the digital and analogue amplifier settings.

8.2.12 DAC Digital FIR Filter

The DAC contains an integrated digital FIR filter with the following modes:

- A default *long* FIR filter for best performance at ≥ 44.1 kHz.
- A *short* FIR to reduce latency.
- A *narrow* FIR (a very sharp roll-off at Nyquist) for G.722 compliance. Best for 8 kHz / 16 kHz.

8.2.13 Microphone Input

CSRA64210 QFN contains an independent low-noise microphone bias generator. The microphone bias generator is recommended for biasing electret condenser microphones. Figure 8.4 shows a biasing circuit for microphones with a sensitivity between about -40 to -60 dB (0 dB = 1 V/Pa).

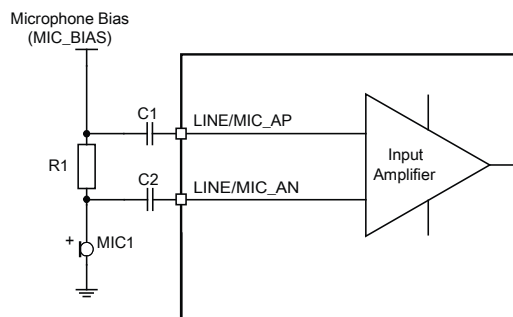


Figure 8.4: Microphone Biasing

Where:

- The microphone bias generator derives its power from VBAT or VOUT_3V3 and requires no capacitor on its output.
- The microphone bias generator maintains regulation within the limits 70 μ A to 2.8 mA, supporting a 2 mA source typically required by 2 electret condenser microphones. If the microphone sits below these limits, then the microphone output must be pre-loaded with a large value resistor to ground.
- Biasing resistors R1 is 2.2 k Ω .
- The input impedance at LINE/MIC_AN and LINE/MIC_AP is typically 6 k Ω .
- C1 and C2 are 100/150 nF if bass roll-off is required to limit wind noise on the microphone.
- R1 sets the microphone load impedance and are normally around 2.2 k Ω .

The microphone bias characteristics include:

- Power supply:
 - CSRA64210 QFN microphone supply is VBAT or VOUT_3V3
 - Minimum input voltage = Output voltage + drop-out voltage
 - Maximum input voltage is 4.3 V
- Drop-out voltage:
 - 300 mV maximum
- Output voltage:
 - 1.8 V or 2.6 V
 - Tolerance 90% to 110%
- Output current:
 - 70 μ A to 2.8 mA
- No load capacitor required

8.2.14 Line Input

Figure 8.5 and Figure 8.6 show 2 circuits for line input operation and show connections for either differential or single-ended inputs.

In line input mode, the input impedance of the pins to ground varies from 6 k Ω to 34 k Ω depending on input gain setting.

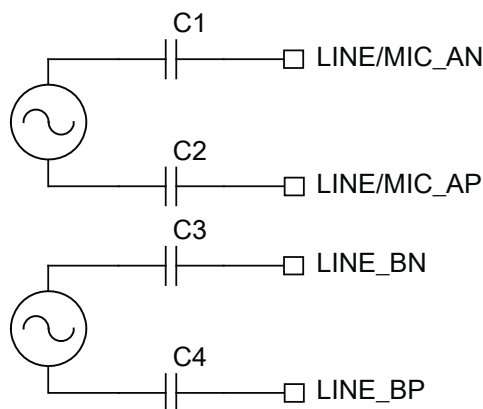


Figure 8.5: Differential Input

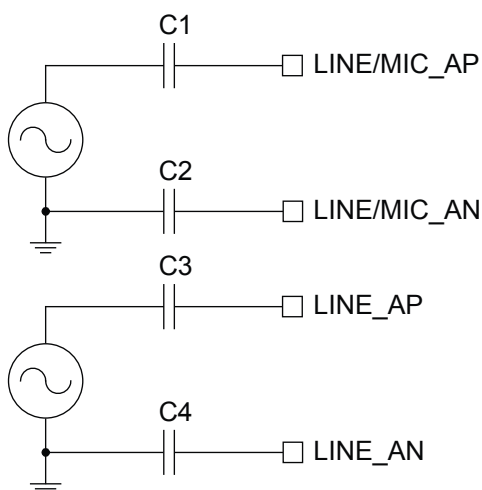


Figure 8.6: Single-ended Input

8.2.15 Output Stage

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to bit stream, which is fed into the analogue output circuitry.

The analogue output circuit comprises a DAC, a buffer with gain-setting, a low-pass filter and a class AB output stage amplifier. Figure 8.7 shows that the output is available as a differential signal between SPKR_LN and SPKR_LP for the left channel, and between SPKR_RN and SPKR_RP for the right channel.

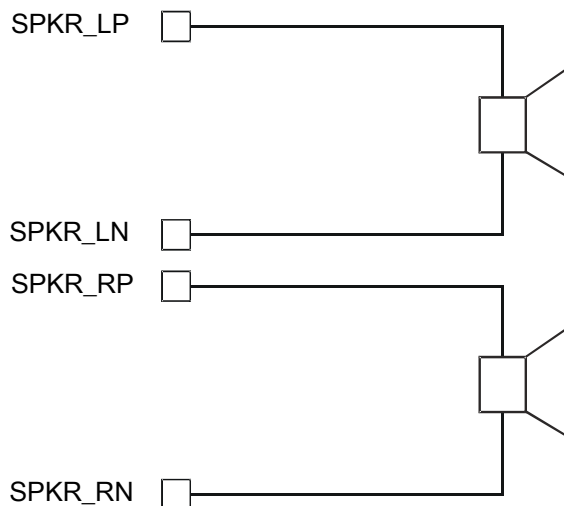


Figure 8.7: Speaker Output

8.2.16 Mono Operation

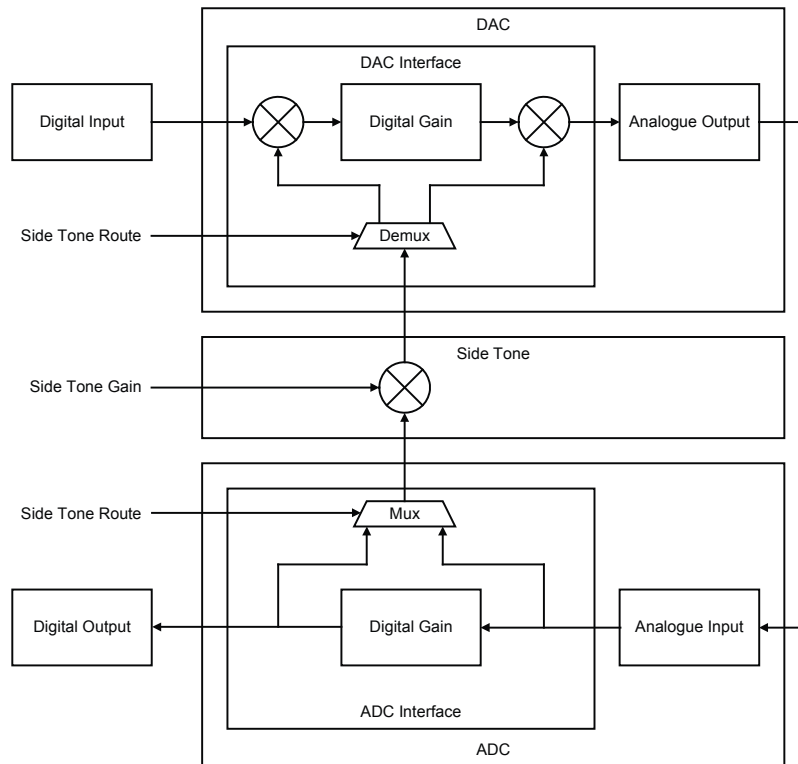
Mono operation is a single-channel operation of the stereo codec. The left channel represents the single mono channel for audio in and audio out. In mono operation, the right channel is the auxiliary mono channel for dual-mono channel operation.

In single channel mono operation, disable the other channel to reduce power consumption.

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8.2.17 Side Tone

In some applications it is necessary to implement side tone. This side tone function involves feeding a properly gained microphone signal in to the DAC stream, e.g. earpiece. The side tone routing selects the version of the microphone signal from before or after the digital gain in the ADC interface and adds it to the output signal before or after the digital gain of the DAC interface, see Figure 8.8.



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Figure 8.8: Side Tone

The ADC provides simple gain to the side tone data. The gain values range from -32.6 dB to 12.0 dB in alternating steps of 2.5 dB and 3.5 dB, see Table 8.5.

Value	Side Tone Gain	Value	Side Tone Gain
0	-32.6 dB	8	-8.5 dB
1	-30.1 dB	9	-6.0 dB
2	-26.6 dB	10	-2.5 dB
3	-24.1 dB	11	0 dB
4	-20.6 dB	12	3.5 dB
5	-18.1 dB	13	6.0 dB
6	-14.5 dB	14	9.5 dB
7	-12.0 dB	15	12.0 dB

Table 8.5: Side Tone Gain

Note:

The values of side tone are shown for information only. During standard operation, the application software controls the side tone gain.

The following PS Keys configure the side tone hardware:

- PSKEY_SIDE_TONE_ENABLE
- PSKEY_SIDE_TONE_GAIN
- PSKEY_SIDE_TONE_AFTER_ADC
- PSKEY_SIDE_TONE_AFTER_DAC

8.2.18 Integrated Digital IIR Filter

CSRA64210 QFN has a programmable digital filter integrated into the ADC channel of the codec. The filter is a 2-stage, second order IIR and is for functions such as custom wind noise reduction. The filter also has optional DC blocking.

The filter has 10 configuration words:

- 1 for gain value
- 8 for coefficient values
- 1 for enabling and disabling the DC blocking

The gain and coefficients are all 12-bit 2's complement signed integer with the format NN.NNNNNNNNNN.

Note:

The position of the binary point is between bit[10] and bit[9], where bit[11] is the most significant bit.

For example:

```
01.1111111111 = most positive number, close to 2
01.0000000000 = 1
00.0000000000 = 0
11.0000000000 = -1
10.0000000000 = -2, most negative number
```

The filter is configured, enabled and disabled from the VM via the `CodecSetIIRFilterA` and `CodecSetIIRFilterB` traps. This requires firmware support. The configuration function takes 10 variables in the following order:

- 0 : Gain
- 1 : b_{01}
- 2 : b_{02}
- 3 : a_{01}
- 4 : a_{02}
- 5 : b_{11}
- 6 : b_{12}
- 7 : a_{11}
- 8 : a_{12}
- 9 : DC Block (1 = enable, 0 = disable)

Equation 8.1 shows the equation for the IIR filter.

$$\text{Filter, } H(z) = \text{Gain} \times \frac{(1 + b_{01} z^{-1} + b_{02} z^{-2})}{(1 + a_{01} z^{-1} + a_{02} z^{-2})} \times \frac{(1 + b_{11} z^{-1} + b_{12} z^{-2})}{(1 + a_{11} z^{-1} + a_{12} z^{-2})}$$

Equation 8.1: IIR Filter Transfer Function, $H(z)$

Equation 8.2 shows the equation for when the DC blocking is enabled.

$$\text{Filter with DC Blocking, } H_{DC}(z) = H(z) \times (1 - z^{-1})$$

Equation 8.2: IIR Filter Plus DC Blocking Transfer Function, $H_{DC}(z)$

8.3 PCM1 and PCM2 Interface

This section describes the digital audio interfaces for the PCM1 and PCM2 interfaces.

The PCM1 interface shares the same physical set of pins with the SPI interface. Either interface is selected using SPI_PCM#:

- SPI_PCM# = 1 selects SPI
- SPI_PCM# = 0 selects PCM/PPIO

The PCM2 interface shares 2 of its pins with the UART interface hardware flow control:

- PCM2_IN = UART_RTS
- PCM2_CLK = UART_CTS

Important Note:

The term *PCM* refers to PCM1 and PCM2.

The audio PCM interface on the CSRA64210 QFN supports:

- Continuous transmission and reception of PCM encoded audio data over Bluetooth.
- Processor overhead reduction through hardware support for continual transmission and reception of PCM data.
- A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not pass through the HCI protocol layer.
- Hardware on the CSRA64210 QFN for sending data to and from a SCO connection.
- Up to 3 SCO connections on the PCM interface at any one time.
- PCM interface master, generating PCM_SYNC and PCM_CLK.
- PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK.
- Various clock formats including:
 - Long Frame Sync
 - Short Frame Sync
 - GCI timing environments
- 13-bit or 16-bit linear, 8-bit μ -law or A-law companded sample formats.
- Receives and transmits on any selection of 3 of the first 4 slots following PCM_SYNC.

The PCM configuration options are enabled by setting PSKEY_PCM_CONFIG32.

8.3.1 PCM Interface Master/Slave

When configured as the master of the PCM interface, CSRA64210 QFN generates PCM_CLK and PCM_SYNC.

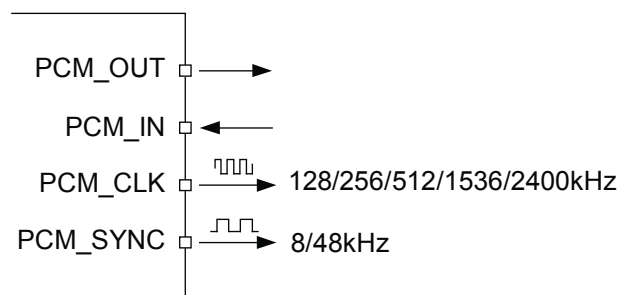
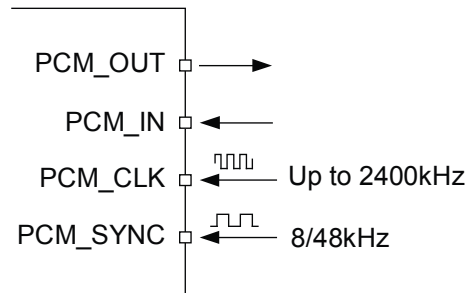


Figure 8.9: PCM Interface Master

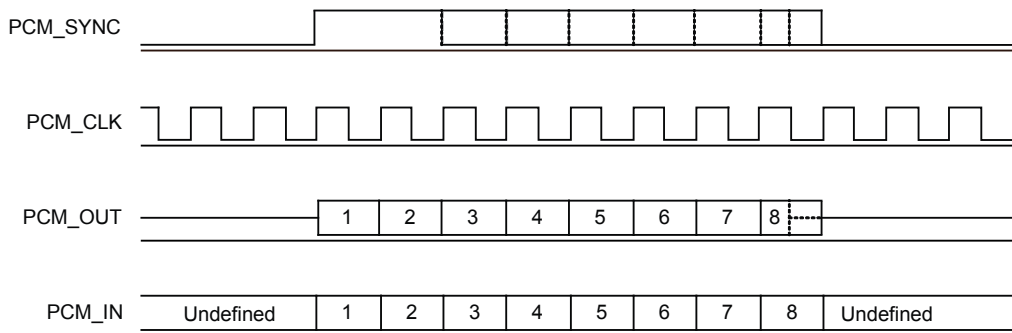


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Figure 8.10: PCM Interface Slave

8.3.2 Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When CSRA64210 QFN is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8 bits long. When CSRA64210 QFN is configured as PCM Slave, PCM_SYNC pulse length may vary from 1 PCM_CLK cycle to half the PCM_SYNC rate.



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Figure 8.11: Long Frame Sync (Shown with 8-bit Companded Sample)

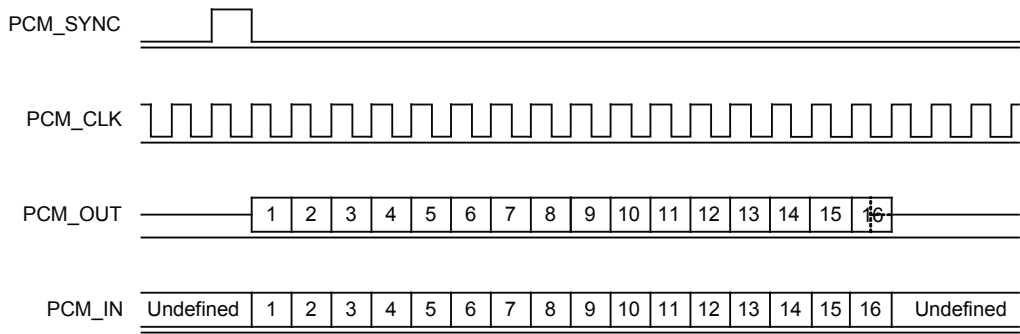
CSRA64210 QFN samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable to switch to high impedance on the falling edge of PCM_CLK of the last data bit or on the rising edge.

Note:

PCM_OUT only goes tristate if TX_TRISTATE_EN = 1 and the next slot is unused.

8.3.3 Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always 1 clock cycle long.



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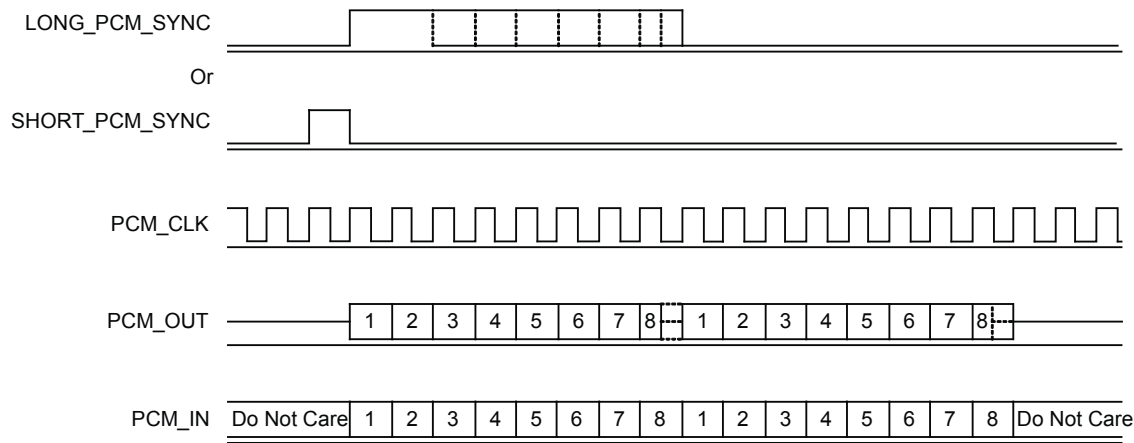
Figure 8.12: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, CSRA64210 QFN samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT is configurable to switch to high impedance on the falling edge of PCM_CLK of the last data bit or on the rising edge.

Note:
PCM_OUT only goes tristate if TX_TRISTATE_EN = 1 and the next slot is unused.

8.3.4 Multi-slot Operation

More than 1 SCO connection over the PCM interface is supported using multiple slots. Up to 3 SCO connections are carried over any set of the first 4 slots.

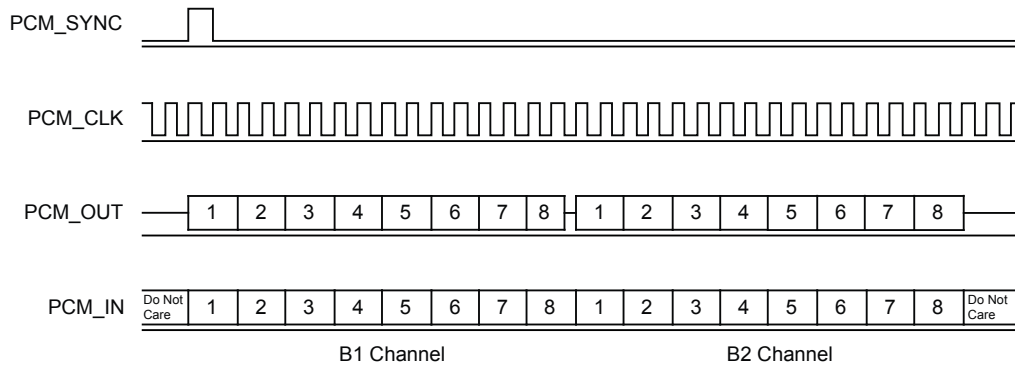


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Figure 8.13: Multi-slot Operation with 2 Slots and 8-bit Companded Samples

8.3.5 GCI Interface

CSRA64210 QFN is compatible with the GCI, a standard synchronous 2B+D ISDN timing interface. The two 64 kbps B channels are accessed when this mode is configured.



G-TW-0000222.2.3

Figure 8.14: GCI Interface

The start of frame is indicated by the rising edge of PCM_SYNC, which runs at 8 kHz.

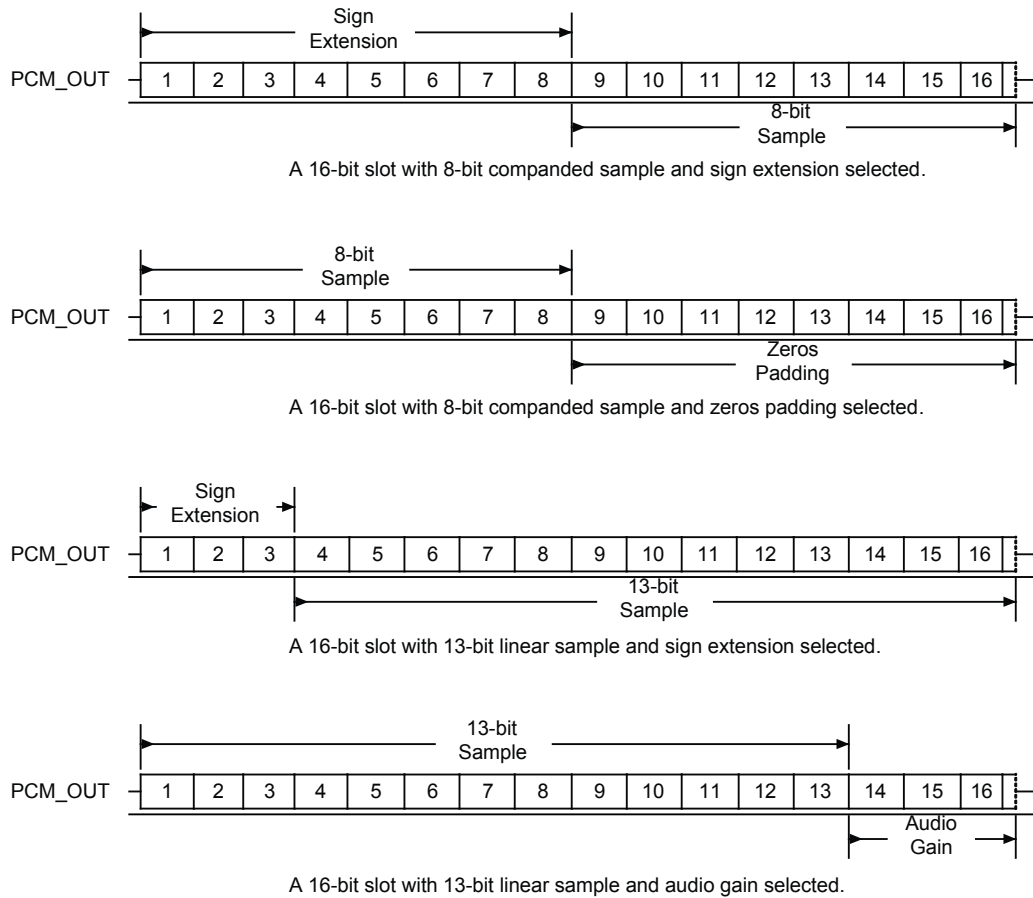
8.3.6 Slots and Sample Formats

CSRA64210 QFN receives and transmits on any selection of the first 4 slots following each sync pulse. Slot durations are either 8 or 16 clock cycles:

- 8 clock cycles for 8-bit sample formats.
- 16 clock cycles for 8-bit, 13-bit or 16-bit sample formats.

CSRA64210 QFN supports:

- 13-bit linear, 16-bit linear and 8-bit μ -law or A-law sample formats.
- A sample rate of 8ksps.
- Little or big endian bit order.
- For 16-bit slots, the 3 or 8 unused bits in each slot are filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some codecs.



G-TW-0000223.2.3

Figure 8.15: 16-bit Slot Length and Sample Formats

8.3.7 Additional Features

CSRA64210 QFN has a mute facility that forces PCM_OUT to be 0. In master mode, CSRA64210 QFN is compatible with some codecs which control power down by forcing PCM_SYNC to 0 while keeping PCM_CLK running.

8.3.8 PCM Timing Information

Symbol	Parameter		Min	Typ	Max	Unit
f _{mclk}	PCM_CLK frequency	4 MHz DDS generation.	-	128	-	kHz
				256		
				512		
		48 MHz DDS generation.	2.9	-	-	kHz
-	PCM_SYNC frequency for SCO connection		-	8	-	kHz
t _{mclkh} ^(a)	PCM_CLK high	4 MHz DDS generation	980	-	-	ns
t _{mckl} ^(a)	PCM_CLK low	4 MHz DDS generation	730	-	-	ns

Symbol	Parameter		Min	Typ	Max	Unit
-	PCM_CLK jitter	48 MHz DDS generation	-	-	21	ns pk-pk
$t_{dmclkssynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclkssyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclkpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinckl}$	Set-up time for PCM_IN valid to PCM_CLK low		20	-	-	ns
$t_{hpinckl}$	Hold time for PCM_CLK low to PCM_IN invalid		0	-	-	ns

Table 8.6: PCM Master Timing

(a) Assumes normal system clock operation. Figures vary during low-power modes, when system clock speeds are reduced.

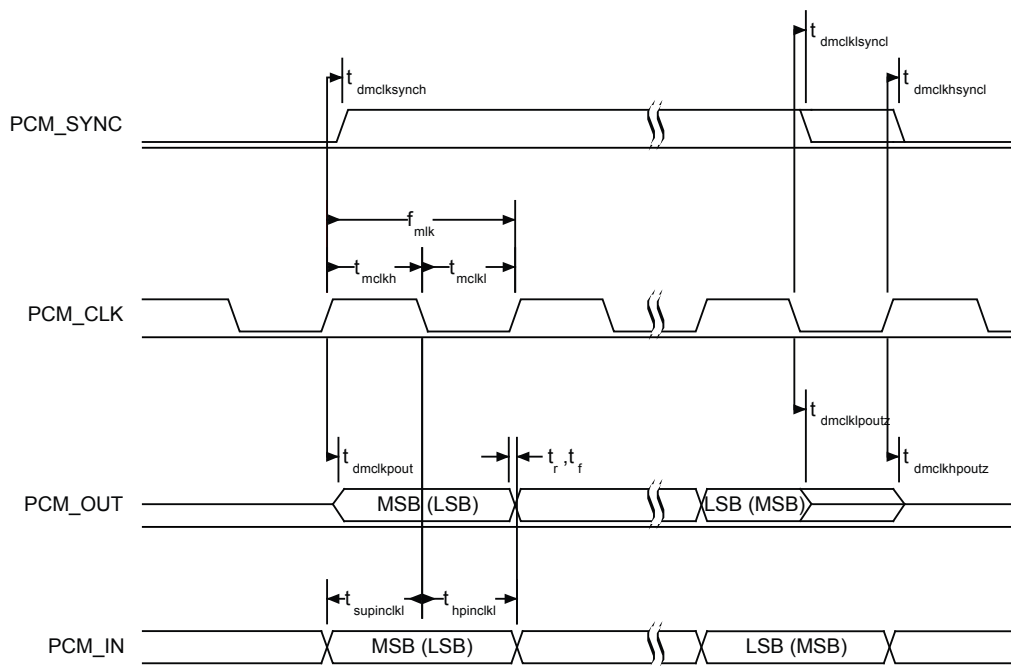


Figure 8.16: PCM Master Timing Long Frame Sync

G-TW-0000224.2.3

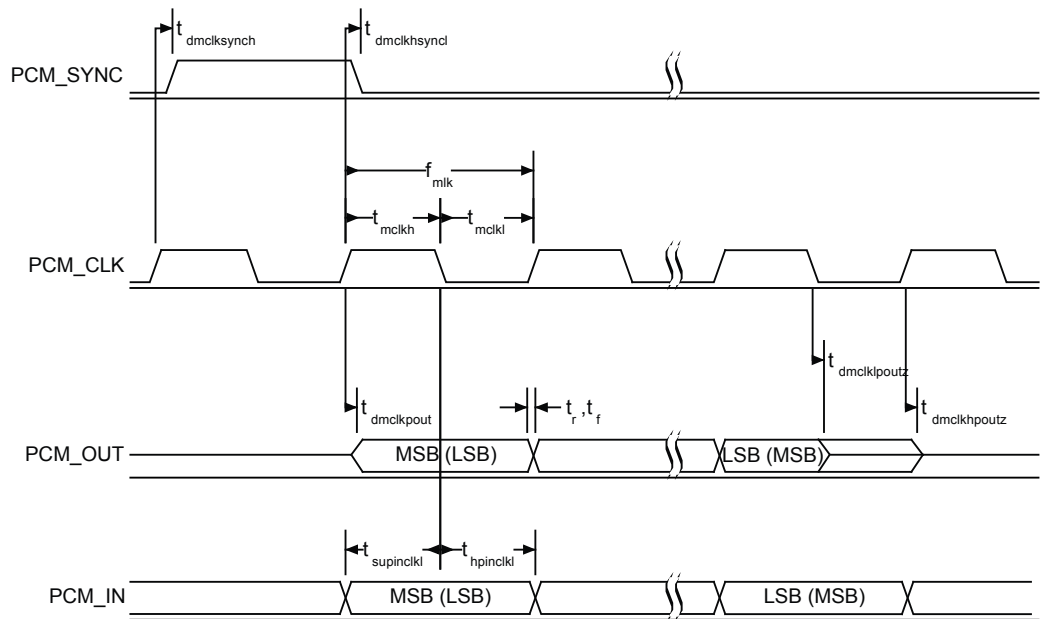


Figure 8.17: PCM Master Timing Short Frame Sync

G-TW-0000225 3.3

Symbol	Parameter	Min	Typ	Max	Unit
f_{sclk}	PCM clock frequency (Slave mode: input)	64	-	(a)	kHz
f_{sclk}	PCM clock frequency (GCI mode)	128	-	(b)	kHz
t_{sckl}	PCM_CLK low time	200	-	-	ns
t_{sclkh}	PCM_CLK high time	200	-	-	ns
$t_{\text{hsclksynch}}$	Hold time from PCM_CLK low to PCM_SYNC high	2	-	-	ns
$t_{\text{susclksynch}}$	Set-up time for PCM_SYNC high to PCM_CLK low	20	-	-	ns
t_{dpout}	Delay time from PCM_SYNC or PCM_CLK, whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
$t_{\text{dsclkhout}}$	Delay time from CLK high to PCM_OUT valid data	-	-	15	ns
t_{dpoutz}	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	15	ns
$t_{\text{supinsckl}}$	Set-up time for PCM_IN valid to CLK low	20	-	-	ns
t_{hpinsckl}	Hold time for PCM_CLK low to PCM_IN invalid	2	-	-	ns

Table 8.7: PCM Slave Timing

(a) Max frequency is the frequency defined by PSKEY_PCM_MIN_CPU_CLOCK

(b) Max frequency is twice the frequency defined by PSKEY_PCM_MIN_CPU_CLOCK

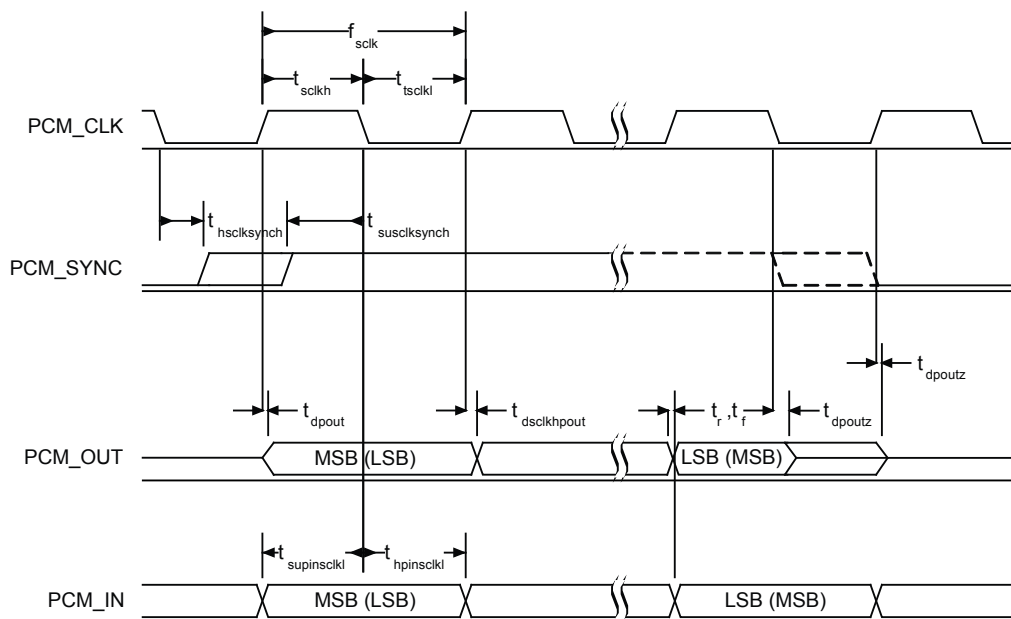


Figure 8.18: PCM Slave Timing Long Frame Sync

G-TW-0000226.3.2

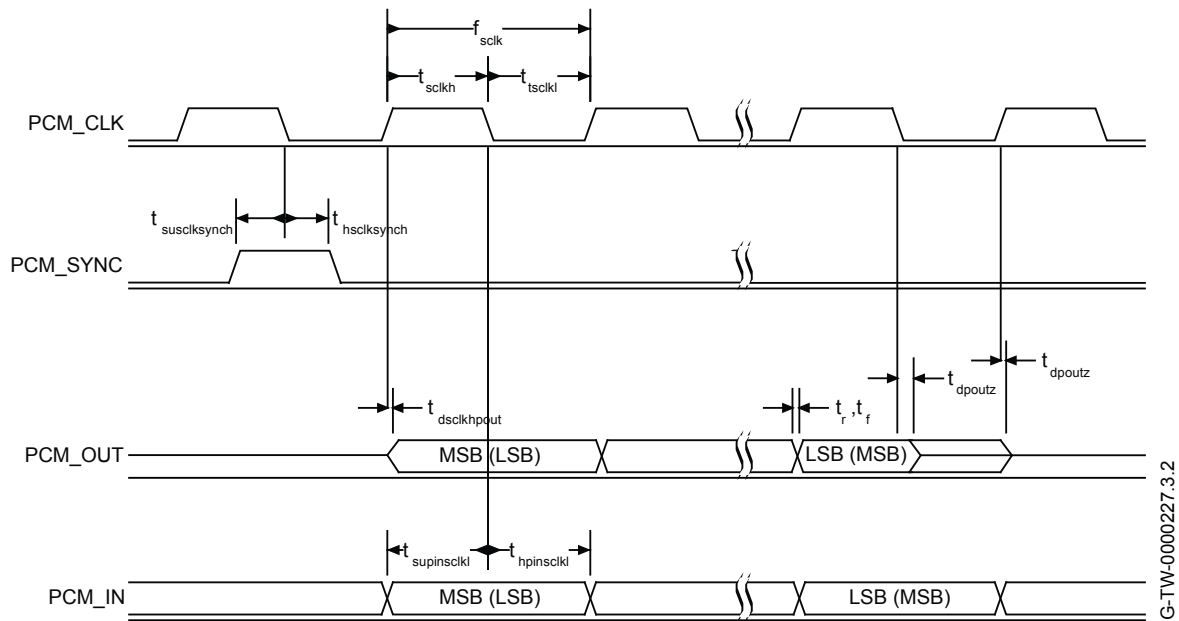


Figure 8.19: PCM Slave Timing Short Frame Sync

8.3.9 PCM_CLK and PCM_SYNC Generation

CSRA64210 QFN has 2 methods of generating PCM_CLK and PCM_SYNC in master mode:

- Generating these signals by DDS from CSRA64210 QFN internal 4 MHz clock. Using this mode limits PCM_CLK to 128, 256 or 512 kHz and PCM_SYNC to 8 kHz.
- Generating these signals by DDS from an internal 48 MHz clock, which enables a greater range of frequencies to be generated with low jitter but consumes more power. To select this second method set bit 48M_PCM_CLK_GEN_EN in PSKEY_PCM_CONFIG32. When in this mode and with long frame sync, the length of PCM_SYNC is either 8 or 16 cycles of PCM_CLK, determined by LONG_LENGTH_SYNC_EN in PSKEY_PCM_CONFIG32.

PSKEY_PCM_USE_LOW_JITTER_MODE sets the low jitter mode when the sync rate is 8 kHz and the PCM clock is set either by PSKEY_PCM_CLOCK_RATE or through the audio API, see *BlueCore Audio API Specification*.

8.3.10 PCM Configuration

Configure the PCM by using PSKEY_PCM_CONFIG32 or through the audio API, see *BlueCore Audio API Specification*. The default for PSKEY_PCM_CONFIG32 is 0x00800000, i.e. first slot following sync is active, 13-bit linear voice format, long frame sync and interface master generating 256 kHz PCM_CLK from 4 MHz internal clock with no tristate of PCM_OUT.

8.4 I²S1 and I²S2 Interface

The CSRA64210 QFN supports 2 industry-standard I²S digital audio interfaces, left-justified or right-justified. The interfaces (I²S1 and I²S2) share the same pins as their equivalent number PCM interface (PCM1 and PCM2), which means each audio bus is mutually exclusive in its usage. Table 8.8 lists these alternative functions.

PCM Interface	I ² S Interface
PCM1_OUT	I2S1_SD_OUT
PCM1_IN	I2S1_SD_IN
PCM1_SYNC	I2S1_WS
PCM1_CLK	I2S1_SCK
PCM2_OUT	I2S2_SD_OUT
PCM2_IN	I2S2_SD_IN
PCM2_SYNC	I2S2_WS
PCM2_CLK	I2S2_SCK

Table 8.8: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

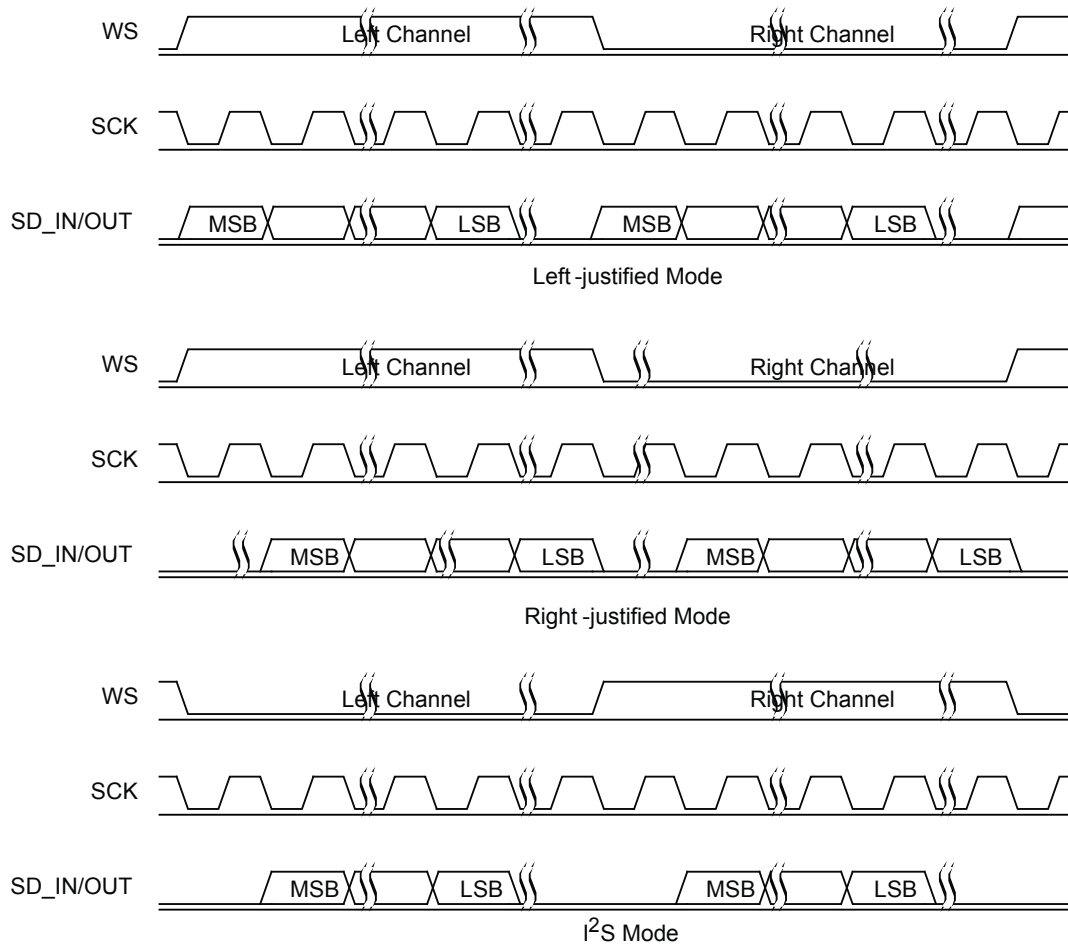
Important Note:

In this section the terms:

- *I²S* refers to the I²S1 and I²S2 interfaces.
- *SD_IN* refers to I2S1_SD_IN or I2S1_SD_IN.
- *SD_OUT* refers to I2S1_SD_OUT or I2S1_SD_OUT.
- *WS* refers to I2S1_WS or I2S1_WS.
- *SCK* refers to I2S1_SCK or I2S1_SCK.

Configure the digital audio interface using PSKEY_DIGITAL_AUDIO_CONFIG, see the PS Key file for more details.

Figure 8.20 shows the timing diagram for the I²S interface.



G-TW-0000230.3.2

Figure 8.20: Digital Audio Interface Modes

The internal representation of audio samples within the CSRA64210 QFN is 16-bit and data on SD_OUT is limited to 16-bit per channel.

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t _{ch}	SCK high time	80	-	-	ns
t _{cl}	SCK low time	80	-	-	ns

Table 8.9: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{ssu}	WS valid to SCK high set-up time	20	-	-	ns
t_{sh}	SCK high to WS invalid hold time	2.5	-	-	ns
t_{opd}	SCK low to SD_OUT valid delay time	-	-	20	ns
t_{isu}	SD_IN valid to SCK high set-up time	20	-	-	ns
t_{ih}	SCK high to SD_IN invalid hold time	2.5	-	-	ns

Table 8.10: I²S Slave Mode Timing

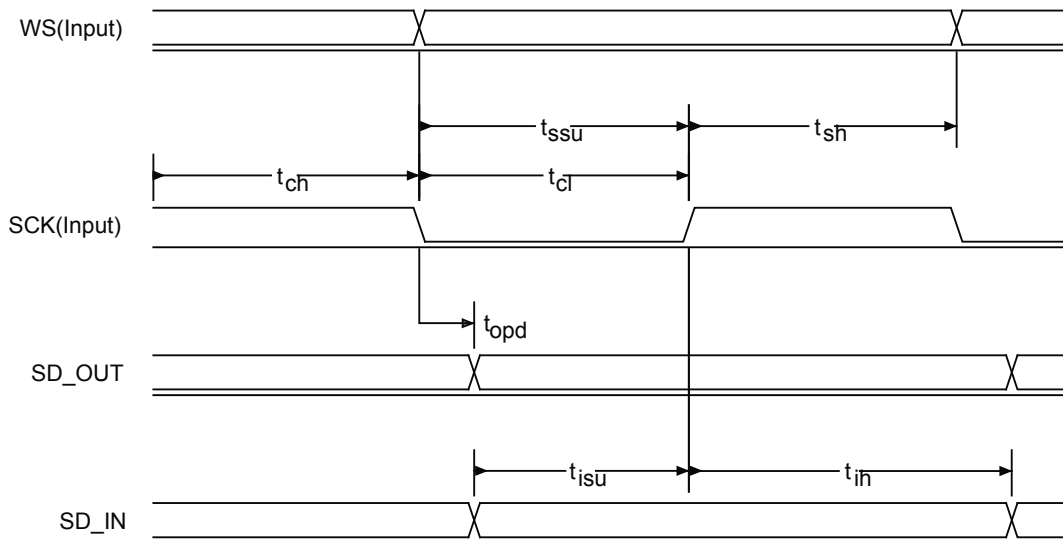


Figure 8.21: Digital Audio Interface Slave Timing

G-TW-0000231.2.2

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz

Table 8.11: Digital Audio Interface Master Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_{spd}	SCK low to WS valid delay time	-	-	39.27	ns
t_{opd}	SCK low to SD_OUT valid delay time	-	-	18.44	ns
t_{isu}	SD_IN valid to SCK high set-up time	18.44	-	-	ns
t_{ih}	SCK high to SD_IN invalid hold time	0	-	-	ns

Table 8.12: I²S Master Mode Timing Parameters, WS and SCK as Outputs

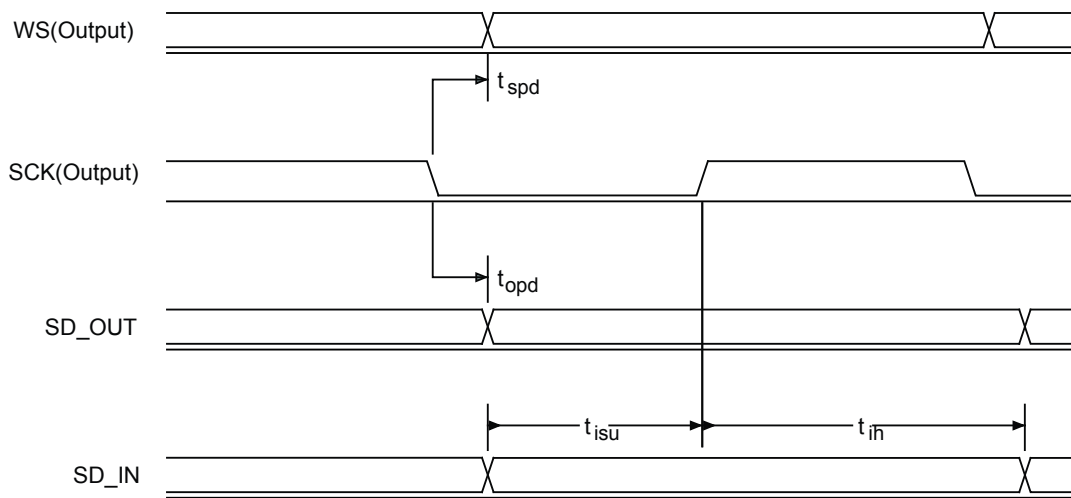


Figure 8.22: Digital Audio Interface Master Timing

9 Power Control and Regulation

For greater power efficiency the CSRA64210 QFN contains 2 switch-mode regulators:

- 1 generates a 1.80 V supply rail with an output current of 185 mA, see Section 9.1.
- 1 generates a 1.35 V supply rail with an output current of 160 mA, see Section 9.2.
- Combining the 2 switch-mode regulators in parallel generates a single 1.80 V supply rail with an output current of 340 mA, see Section 9.3.

CSRA64210 QFN contains 4 LDO linear regulators:

- 3.30 V bypass regulator, see Section 9.4.
- 0.85 V to 1.20 V VDD_DIG linear regulator, see Section 9.5.
- 1.35 V VDD_AUX linear regulator, see Section 9.6.
- 1.35 V VDD_ANA linear regulator, see Section 9.7.

The recommended configurations for power control and regulation on the CSRA64210 QFN are:

- 3 switch-mode configurations:
 - A 1.80 V and 1.35 V dual-supply rail system using the 1.80 V and 1.35 V switch-mode regulators, see Figure 9.1. This is the default power control and regulation configuration for the CSRA64210 QFN.
 - A 1.80 V single-supply rail system using the 1.80 V switch-mode regulator.
 - A 1.80 V parallel-supply rail system for higher currents using the 1.80 V and 1.35 V switch-mode regulators with combined outputs, see Figure 9.2.
- A linear configuration using an external 1.8 V rail omitting all regulators

Table 9.1 shows settings for the recommended configurations for power control and regulation on the CSRA64210 QFN.

Supply Configuration	Regulators				Supply Rail	
	Switch-mode		VDD_AUX Linear Regulator	VDD_ANA Linear Regulator		
	1.8 V	1.35 V			1.8 V	1.35 V
Dual-supply SMPS	ON	ON	OFF	OFF	SMPS	SMPS
Single-supply SMPS	ON	OFF	ON	ON	SMPS	LDO
Parallel-supply SMPS	ON	ON	ON	ON	SMPS	LDO
Linear supply	OFF	OFF	ON	ON	External	LDO

Table 9.1: Recommended Configurations for Power Control and Regulation

For more information on CSRA64210 QFN power supply configuration, see the *Configuring the Power Supplies on CSR8670* application note.



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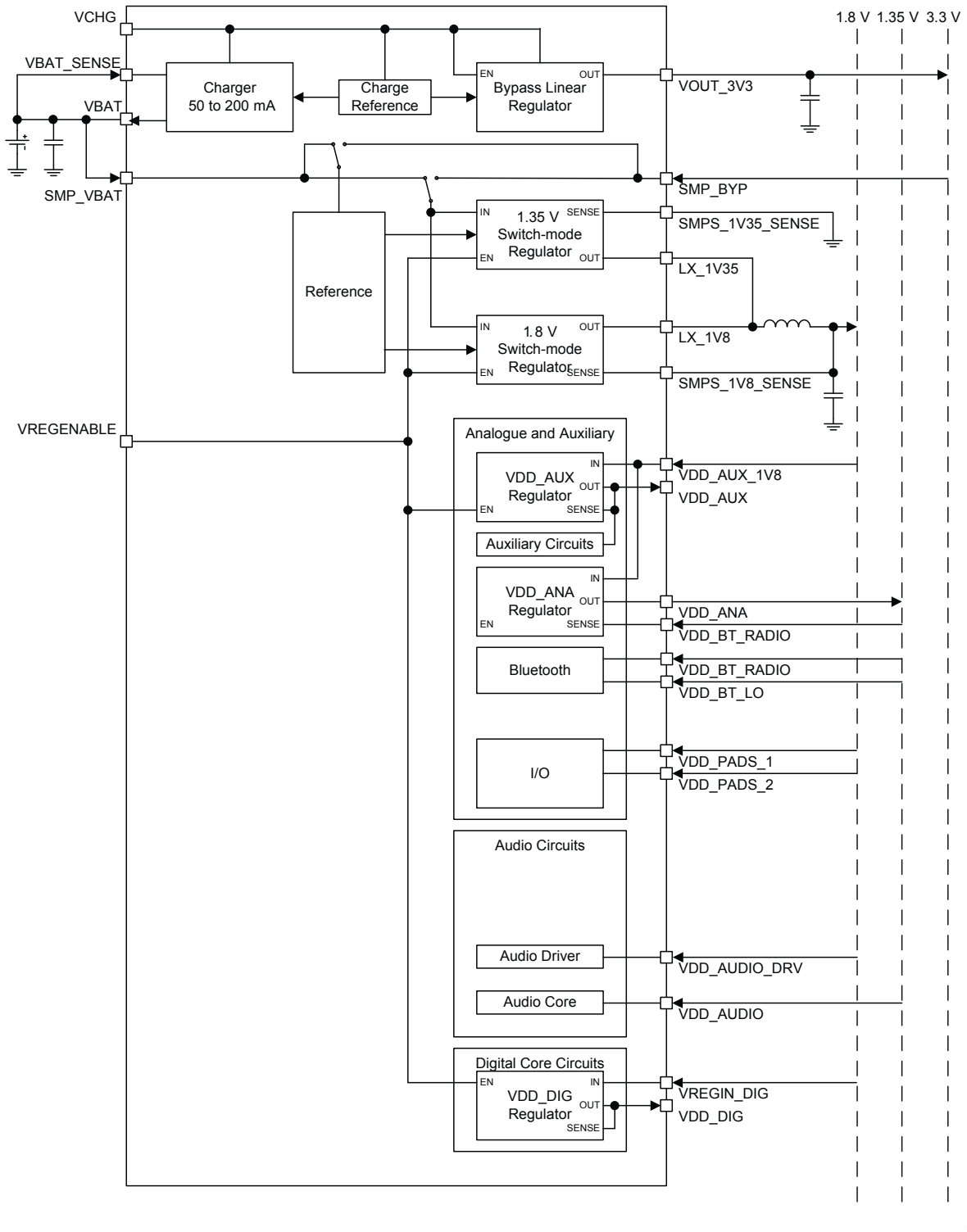


Figure 9.2: 1.80 V Parallel-supply Switch-mode System Configuration

9.1 1.8 V Switch-mode Regulator

CSR recommends using the integrated switch-mode regulator to power the 1.80 V supply rail.

Figure 9.3 shows that an external LC filter circuit of a low-resistance series inductor, L1 (4.7 μ H), followed by a low ESR shunt capacitor, C3 (2.2 μ F), is required between the LX_1V8 terminal and the 1.80 V supply rail. Connect the 1.80 V supply rail and the SMPS_1V8_SENSE pin.

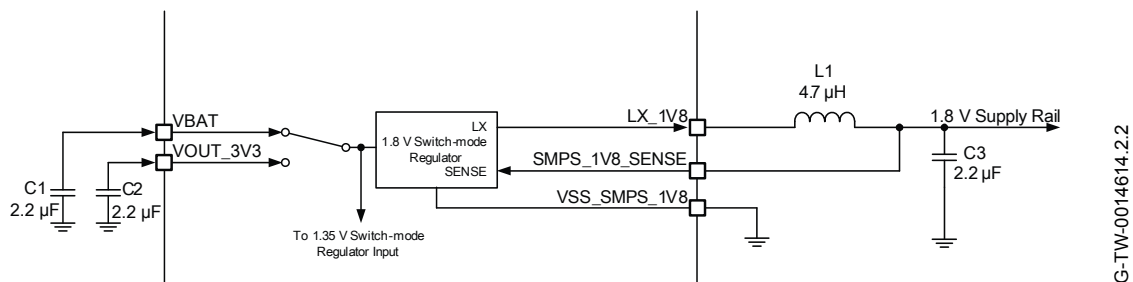


Figure 9.3: 1.8 V Switch-mode Regulator Output Configuration

Minimise the series resistance of the tracks between the regulator input, VBAT and VOUT_3V3, ground terminals, the filter and decoupling components, and the external voltage source to maintain high-efficiency power conversion and low supply ripple.

Ensure a solid ground plane between C1, C2, C3 and VSS_SMPS_1V8.

Also minimise the collective parasitic capacitance on the track between LX_1V8 and the inductor L1, to maximise efficiency.

For the regulator to meet its specifications it requires a total resistance of $<1.0 \Omega$ ($<0.5 \Omega$ recommended) for the following:

- The track between the battery and VBAT.
- The track between LX_1V8 and the inductor.
- The inductor, L1, ESR.
- The track between the inductor, L1, and the sense point on the 1.80 V supply rail.

The following enable the 1.80 V switch-mode regulator:

- VREGENABLE pin
- The CSRA64210 QFN firmware with reference to PSKEY_PSU_ENABLES
- VCHG pin

The switching frequency is adjustable by setting an offset from 4.00 MHz using PSKEY_SMPS_FREQ_OFFSET, which also affects the 1.35 V switch-mode regulator.

When the 1.80 V switch-mode regulator is not required, leave unconnected:

- The regulator input VBAT and VOUT_3V3
- The regulator output LX_1V8

9.2 1.35 V Switch-mode Regulator

CSR recommends using the integrated switch-mode regulator to power the 1.35 V supply rail.

Figure 9.4 shows that an external LC filter circuit of a low-resistance series inductor L1 (4.7 μ H), followed by a low ESR shunt capacitor, C3 (4.7 μ F), is required between the LX_1V35 terminal and the 1.35 V supply rail. Connect the 1.35 V supply rail and the SMPS_1V35_SENSE pin.

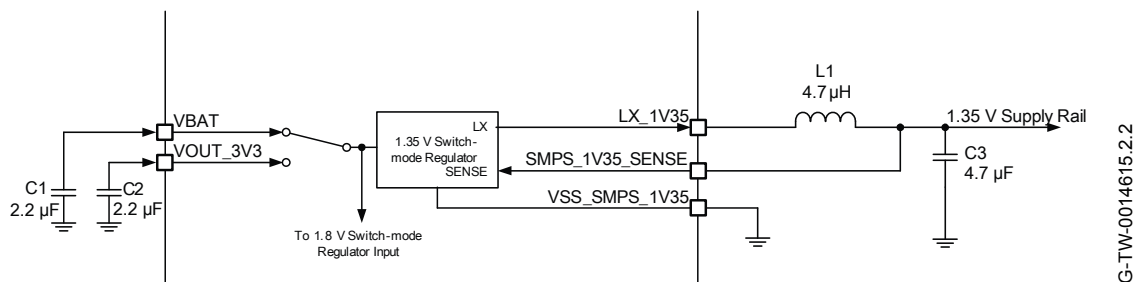


Figure 9.4: 1.35 V Switch-mode Regulator Output Configuration

Minimise the series resistance of the tracks between the regulator input, VBAT and VOUT_3V3, ground terminals, the filter and decoupling components, and the external voltage source to maintain high-efficiency power conversion and low supply ripple.

Ensure a solid ground plane between C1, C2, C3 and VSS_SMPS_1V35.

Also minimise the collective parasitic capacitance on the track between LX_1V35 and the inductor L1, to maximise efficiency.

For the regulator to meet its specifications it requires a total resistance of $<1.0 \Omega$ ($<0.5 \Omega$ recommended) for the following:

- The track between the battery and VBAT.
- The track between LX_1V35 and the inductor.
- The inductor, L1, ESR.
- The track between the inductor, L1, and the sense point on the 1.35 V supply rail.

The following enable the 1.35 V switch-mode regulator:

- VREGENABLE pin
- The CSRA64210 QFN firmware with reference to PSKEY_PSU_ENABLES
- VCHG pin

The switching frequency is adjustable by setting an offset from 4.00 MHz using PSKEY_SMPS_FREQ_OFFSET, which also affects the 1.80 V switch-mode regulator.

When the 1.35 V switch-mode regulator is not required, leave unconnected:

- The regulator input VBAT and VOUT_3V3
- The regulator output LX_1V35

9.3 1.8 V and 1.35 V Switch-mode Regulators Combined

For applications that require a single 1.80 V supply rail with higher currents CSR recommends combining the outputs of the integrated 1.80 V and 1.35 V switch-mode regulators in parallel to power a single 1.80 V supply rail, see Figure 9.5.

Figure 9.5 shows that an external LC filter circuit of a low-resistance series inductor L1 (4.7 μ H), followed by a low ESR shunt capacitor, C3 (2.2 μ F), is required between the LX_1V8 terminal and the 1.80 V supply rail. Connect the 1.80 V supply rail and the SMPS_1V8_SENSE pin and ground the SMPS_1V35_SENSE pin.

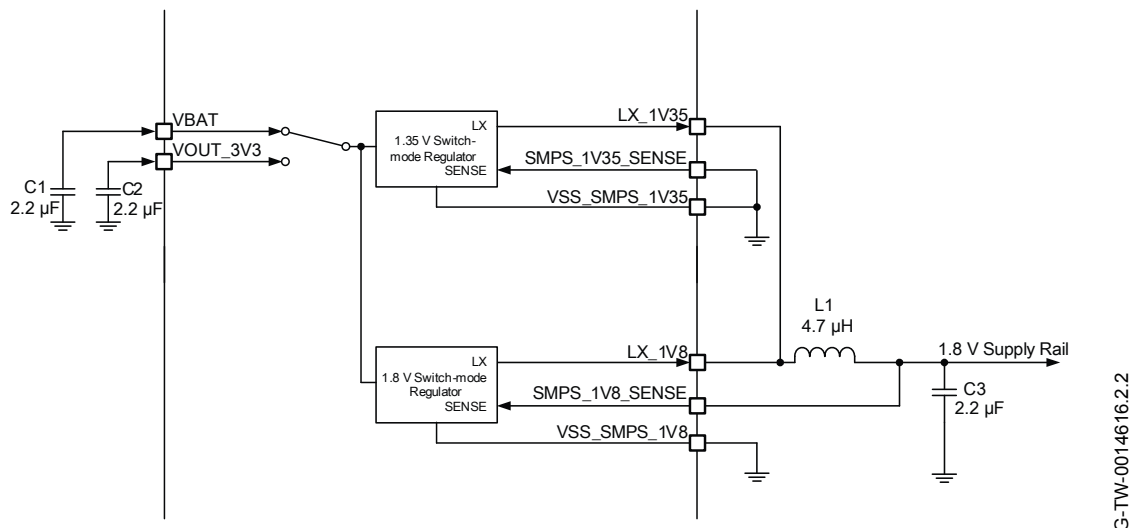


Figure 9.5: 1.8 V and 1.35 V Switch-mode Regulators Outputs Parallel Configuration

Minimise the series resistance of the tracks between the regulator input VBAT and VOUT_3V3, ground terminals, the filter and decoupling components, and the external voltage source to maintain high-efficiency power conversion and low supply ripple.

Ensure a solid ground plane between C1, C2, C3, VSS_SMPS_1V8 and VSS_SMPS_1V35.

Also minimise the collective parasitic capacitance on the track between LX_1V8, LX_1V35 and the inductor L1, to maximise efficiency.

For the regulator to meet its specifications it requires a total resistance of $<1.0 \Omega$ ($<0.5 \Omega$ recommended) for the following:

- The track between the battery and VBAT.
- The track between LX_1V8, LX_1V35 and the inductor.
- The inductor L1, ESR.
- The track between the inductor, L1, and the sense point on the 1.80 V supply rail.

The following enable the 1.80 V switch-mode regulator:

- VREGENABLE pin
- The CSRA64210 QFN firmware with reference to PSKEY_PSU_ENABLES
- VCHG pin

The switching frequency is adjustable by setting an offset from 4.00 MHz using PSKEY_SMPS_FREQ_OFFSET.

When the 1.80 V switch-mode regulator is not required, leave unconnected:

- The regulator input VBAT and VOUT_3V3
- The regulator output LX_1V8

9.3.1 Inductor Choice

Correct switch-mode power supply performance depends on inductor choice. A key parameter is the saturation current of the inductor. As an inductor saturates, its effective inductance decreases significantly, leading to the switching currents increasing further. This can eventually lead to:

- Poor regulator performance
- RF interference
- Possible instability

CSR recommends inductor selection ensures that the inductance reduction at 250 mA is less than 30% of nominal inductance. This is often stated as the inductor parameter *Rated Current (L change) Max* and the value is the current at which the rated inductance has fallen by a specified percentage.

Note:

Some inductor manufacturers state the inductor's rated current as the temperature rise (DC current at which the inductor temperature increases by a specified temperature). This is not the same as saturation current.

The saturation performance can be particularly poor with small package inductors.

Another key inductor parameter is the DC resistance, because high DC resistance in the inductor decreases switch-mode power supply efficiency.

Note:

Pay attention to the frequency for the inductor specified parameters. The switch-mode power supply operates at 4 MHz, so inductor parameters should be stated at 4 MHz or higher.

Table 9.2 shows CSR's testing and characterisation carried out on boards using Taiyo-Yuden CB2012T4R7M parts (0805 (2012 metric) package).

Parameter	Min	Typ	Max	Unit
Nominal inductance value ($\pm 20\%$ tolerance)	3.84	4.7	5.64	μH
Inductor R_{dc} for SMPS stability	0.1	0.25	1	Ω
Inductor R_{dc} for SMPS efficiency	0.1	0.25	0.4	Ω
Inductor saturation current (-30% reduction from the nominal inductor value)	250	-	-	mA
Inductor self-resonant frequency	10	-	-	MHz
Direct capacitance on SMPS output (including tolerance and de-rating)	1.5	2.2 / 4.7	10	μF

Table 9.2: Inductor Choice, CSR's Testing and Characterisation

9.4 Bypass LDO Linear Regulator

The integrated bypass LDO linear regulator is available as a 3.30 V supply rail and is an alternative supply rail to the battery supply. This is especially useful when the battery has no charge and the CSRA64210 QFN needs to power up. The input voltage should be between 4.25 V to 6.50 V.

Note:

The integrated bypass LDO linear regulator can operate down to 3.1 V with a reduced performance.

Externally decouple the output of this regulator using a low ESR MLC capacitor of a minimum 2.2 μF to the VOUT_3V3 pin.

The output voltage is switched on when VCHG gets above 3.0 V.

9.5 Low-voltage VDD_DIG Linear Regulator

The integrated low-voltage VDD_DIG linear regulator powers the digital circuits on CSRA64210 QFN. Externally decouple the output of this regulator using a low ESR MLC capacitor of 470 nF.

9.6 Low-voltage VDD_AUX Linear Regulator

The integrated low-voltage VDD_AUX linear regulator is optionally available to provide a 1.35 V auxiliary supply rail when the 1.35 V switch-mode regulator is not used. When using the integrated low-voltage VDD_AUX linear regulator, externally decouple the output of this regulator using a low ESR MLC capacitor of a minimum 470 nF to the VDD_AUX pin.

9.7 Low-voltage VDD_ANA Linear Regulator

The integrated low-voltage VDD_ANA linear regulator is optionally available to power the 1.35 V analogue supply rail when the 1.35 V switch-mode regulator is not used. When using the integrated low-voltage VDD_ANA linear regulator, externally decouple the output of this regulator using a 2.2 μ F low ESR MLC capacitor to the VDD_ANA pin.

9.8 Voltage Regulator Enable

When using the integrated regulators the voltage regulator enable pin, VREGENABLE, enables the CSRA64210 QFN and the following regulators:

- 1.8 V switch-mode regulator
- 1.35 V switch-mode regulator
- Low-voltage VDD_DIG linear regulator
- Low-voltage VDD_AUX linear regulator

The VREGENABLE pin is active high, with a pull-down, typical 100 k Ω , which is disabled by PSKEY_VREG_ENABLE_STRONG_PULL.

CSRA64210 QFN boots-up when the voltage regulator enable pin is pulled high typically for 10 to 15 ms, enabling the regulators. The firmware then latches the regulators on. The voltage regulator enable pin can then be released.

The status of the VREGENABLE pin is available to firmware through an internal connection. VREGENABLE also works as an input line.

Note:

VREGENABLE should be asserted after the VBAT supply when VREGENABLE is not used as a power-on button.

9.9 External Regulators and Power Sequencing

CSR recommends that the integrated regulators supply the CSRA64210 QFN and it is configured based on the information in this data sheet.

If any of the supply rails for the CSRA64210 QFN are supplied from an external regulator, then it should match or be better than the internal regulator available on CSRA64210 QFN. For more information see regulator characteristics in Section 12.

Note:

The internal regulators described in Section 9.1 to Section 9.7 are not recommended for external circuitry other than that shown in Section 11.

For information about power sequencing of external regulators to supply the CSRA64210 QFN contact CSR.

9.10 Reset, RST#

CSRA64210 QFN is reset from several sources:

- RST# pin
- Power-on reset
- USB charger attach reset
- Software configured watchdog timer

The RST# pin is an active low reset. Assert the reset signal for a period >5 ms to ensure a full reset.

At reset the digital I/O pins are set to inputs for bidirectional pins and outputs are set to tristate.

Note:

Reset can also be triggered by a UART break symbol if:

- Host interface is any UART transport and
- PSKEY_HOSTIO_UART_RESET_TIMEOUT is set to a non-zero value (>1000)

A warm reset function is also available under software control. After a warm reset RAM data remains available.

9.10.1 Digital Pin States on Reset

Table 9.3 shows the pin states of CSRA64210 QFN on reset.

Pin Name	I/O Type	Full Chip Reset	Pin Name	I/O Type	Full Chip Reset
USB_DP	Digital bidirectional	N/A	PIO[6]	Digital bidirectional	PDS
USB_DN	Digital bidirectional	N/A	PIO[7]	Digital bidirectional	PDS
PIO[0]	Digital bidirectional	PUS	PIO[8]	Digital bidirectional	PUS
PIO[1]	Digital bidirectional	PUS	PIO[9]	Digital bidirectional	PDS
PIO[2]	Digital bidirectional	PDW	PIO[16]	Digital bidirectional	PUS
PIO[3]	Digital bidirectional	PDW	PIO[17]	Digital bidirectional	PDS
PIO[4]	Digital bidirectional	PDW	PIO[18]	Digital bidirectional	PDW
PIO[5]	Digital bidirectional	PDW	PIO[21]	Digital bidirectional	PDW

Table 9.3: Pin States on Reset

Note:

PUS = Strong pull-up

PDS = Strong pull-down

PUW = Weak pull-up

PDW = Weak pull-down

9.10.2 Status After Reset

The status of CSRA64210 QFN after a reset is:

- Warm reset: baud rate and RAM data remain available
- Cold reset: baud rate and RAM data not available

9.11 Automatic Reset Protection

CSRA64210 QFN includes an automatic reset protection circuit which restarts/resets CSRA64210 QFN when an unexpected reset occurs, e.g. ESD strike or lowering of RST#. The automatic reset protection circuit enables resets from the VM without the requirement for external circuitry.

Note:

The reset protection is cleared after typically 2 s (1.6 s min to 2.4 s max).

If RST# is held low for >2.4 s CSRA64210 QFN turns off. A rising edge on VREGENABLE or VCHG is required to power on CSRA64210 QFN.

10 Battery Charger

10.1 Battery Charger Hardware Operating Modes

The battery charger hardware is controlled by the VM. The battery charger has 5 modes:

- Disabled
- Trickle charge
- Fast charge
- Standby: fully charged or float charge
- Error: charging input voltage, VCHG, is too low

The battery charger operating mode is determined by the battery voltage and current, see Table 10.1 and Figure 10.1.

Mode	Battery Charger Enabled	VBAT_SENSE
Disabled	No	X
Trickle charge	Yes	>0 and $<V_{fast}$
Fast charge	Yes	$>V_{fast}$ and $<V_{float}$
Standby	Yes	$I_{term}^{(a)}$ and $>(V_{float} - V_{hyst})$
Error	Yes	$>(VCHG - 50mV)$

Table 10.1: Battery Charger Operating Modes Determined by Battery Voltage and Current

^(a) I_{term} is approximately 10% of I_{fast} for a given I_{fast} setting

Figure 10.1 shows the mode-to-mode transition voltages. These voltages are fixed and calibrated by CSR. The transition between modes can occur at any time.

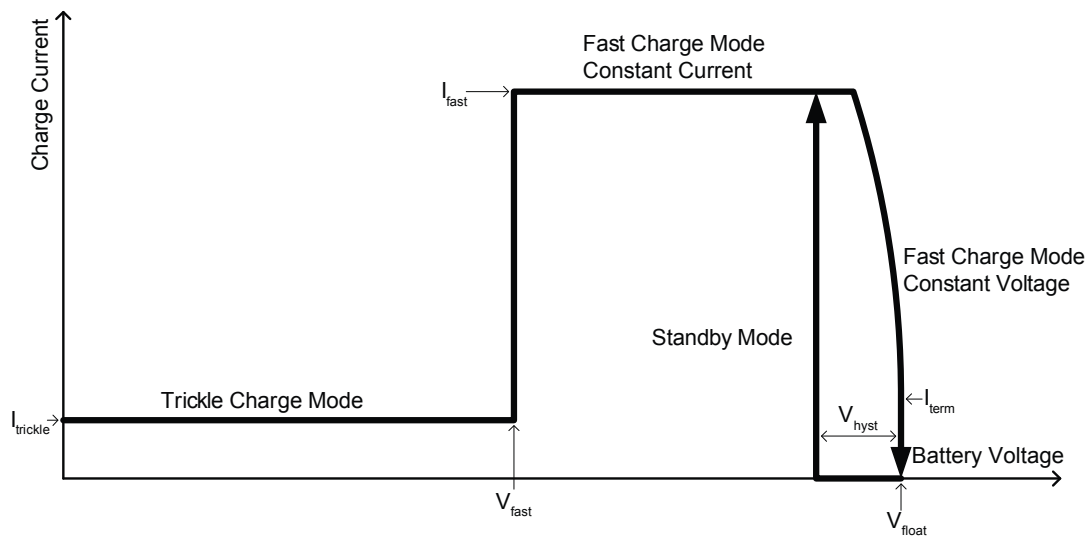


Figure 10.1: Battery Charger Mode-to-Mode Transition Diagram

Note:

The battery voltage remains constant in Fast Charge Constant Voltage Mode, the curved line on Figure 10.1 is for clarity only.

The internal charger circuit can provide up to 200 mA of charge current, for currents higher than this the CSRA64210 QFN can control an external pass transistor.

10.1.1 Disabled Mode

In the disabled mode the battery charger is fully disabled and draws no active current on any of its terminals.

10.1.2 Trickle Charge Mode

In the trickle charge mode, when the voltage on VBAT_SENSE is lower than the V_{fast} threshold, a current of approximately 10% of the fast charge current, I_{fast} , is sourced from the VBAT pin.

The V_{fast} threshold detection has hysteresis to prevent the charger from oscillating between modes.

10.1.3 Fast Charge Mode

When the voltage on VBAT_SENSE is greater than V_{fast} , the current sourced from the VBAT pin increases to I_{fast} . I_{fast} is between 10 mA and 200 mA set by PS Key or a VM trap. In addition, I_{fast} is calibrated in production test to correct for process variation in the charger circuit.

The current is held constant at I_{fast} until the voltage at VBAT_SENSE reaches V_{float} , then the charger reduces the current sourced to maintain a constant voltage on the VBAT_SENSE pin.

When the current sourced is below the termination current, I_{term} , the charging stops and the charger enters standby mode. I_{term} is typically 10% of the fast charge current.

10.1.4 Standby Mode

When the battery is fully charged, the charger enters standby mode, and battery charging stops. The battery voltage on the VBAT_SENSE pin is monitored, and when it drops below a threshold set at V_{hyst} below the final charging voltage, V_{float} , the charger re-enters fast charge mode.

10.1.5 Error Mode

The charger enters the error mode if the voltage on the VCHG pin is too low to operate the charger correctly (VBAT_SENSE is greater than VCHG - 50 mV (typical)).

In this mode, charging is stopped. The battery charger does not require a reset to resume normal operation.

10.2 Battery Charger Trimming and Calibration

The battery charger default trim values are written by CSR into non-volatile memory when each IC is characterised. CSR provides various PS Keys for overriding the default trims.

10.3 VM Battery Charger Control

The VM charger code has overall supervisory control of the battery charger and is responsible for:

- Responding to charger power connection/disconnection events
- Monitoring the temperature of the battery
- Monitoring the temperature of the die to protect against silicon damage
- Monitoring the time spent in the various charge states
- Enabling/disabling the charger circuitry based on the monitored information
- Driving the user visible charger status LED(s)

10.4 Battery Charger Firmware and PS Keys

The battery charger firmware sets up the charger hardware based on the PS Key settings and traps called from the VM charger code. It also performs the initial analogue trimming. Settings for the charger current depend on the battery capacity and type, which are set by the user in the PS Keys.

For more information on the CSRA64210 QFN, including details on setting up, calibrating, trimming and the PS Keys, see *Lithium Polymer Battery Charger Calibration and Operation for CSR8670* application note.

10.5 External Mode

The external mode is for charging higher capacity batteries using an external pass device. The current is controlled by sinking a varying current into the CHG_EXT pin, and the current is determined by measuring the voltage drop across a resistor, R_{sense} , connected in series with the external pass device, see Figure 10.2. The voltage drop is determined by looking at the difference between the VBAT_SENSE and VBAT pins. The voltage drop across R_{sense} is typically 200 mV. The value of the external series resistor determines the charger current. This current can be trimmed with a PS Key.

Figure 10.2 shows R1 (220 m Ω) and C1 (4.7 μ F) form an RC snubber that is required to maintain stability across all battery ESRs. The battery ESR must be <1.0 Ω .

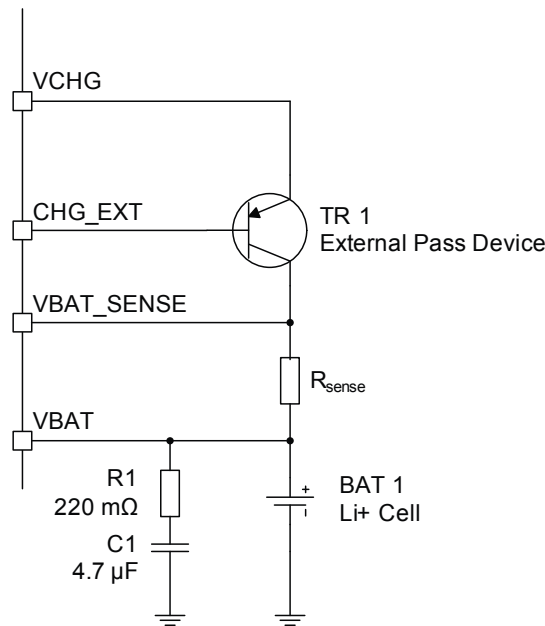


Figure 10.2: Battery Charger External Mode Typical Configuration

G-TW-0005585 3.2

11 Example Application Schematic

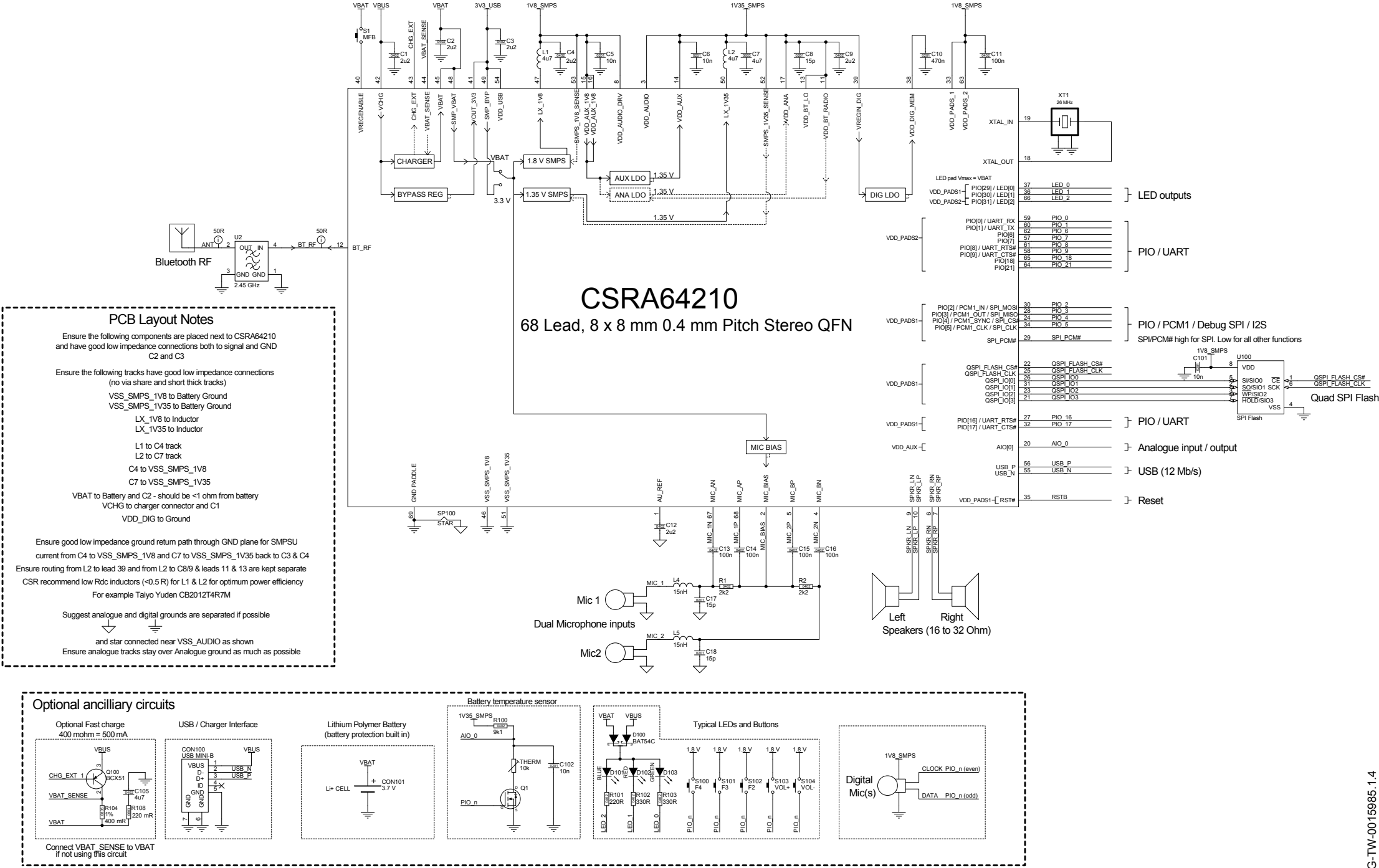


Figure 11.1: Example Application Schematic

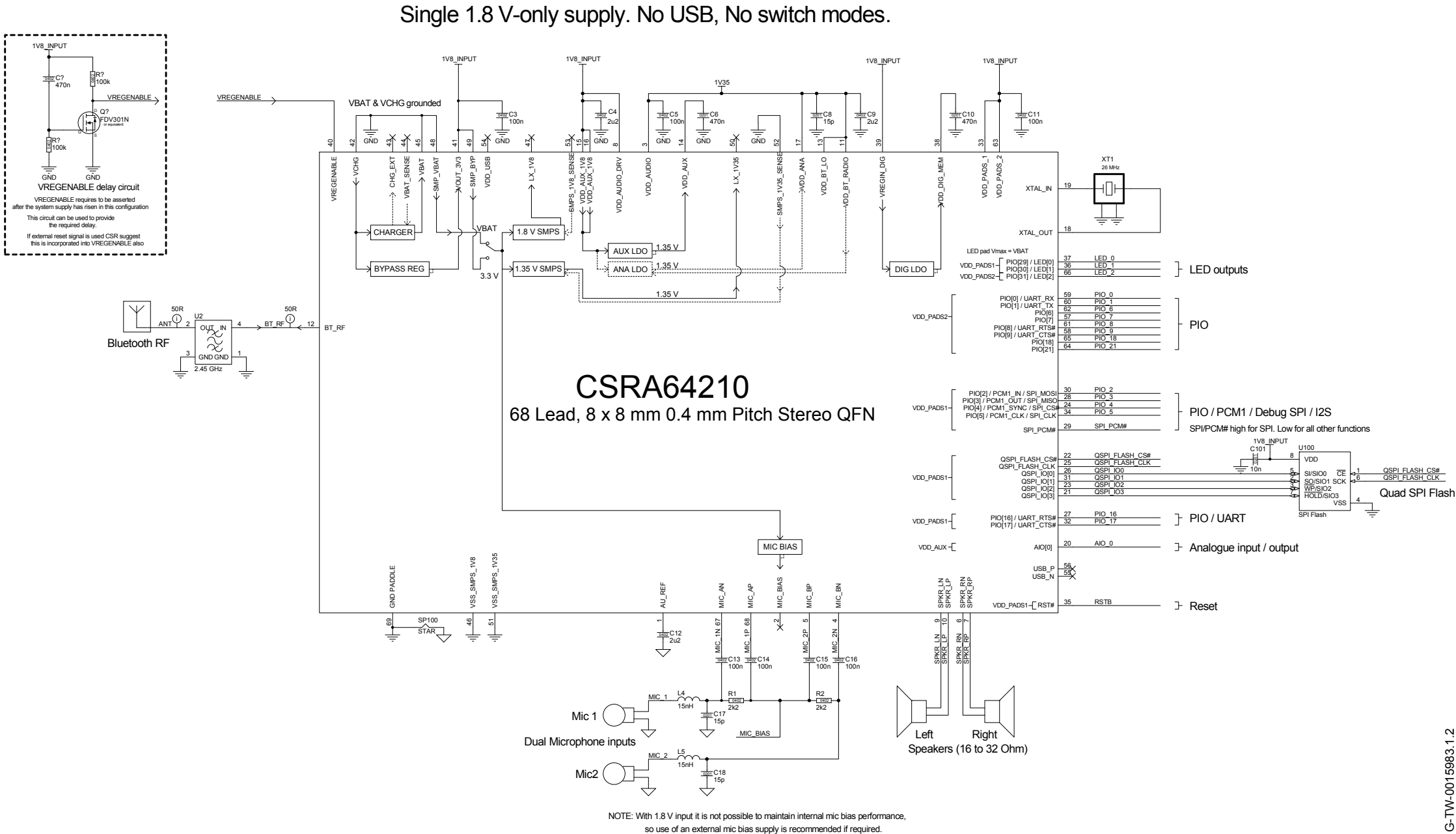


Figure 11.2: Single 1.8 V-only Supply, with no USB or SMPSS

G-TW-0015984.1.2



12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Rating		Min	Max	Unit
Storage temperature		-40	105	°C
Supply Voltage				
5 V (USB VBUS)	VCHG	-0.4	6.50	V
3.3 V	SMP_BYP	-0.4	3.60	V
	VDD_USB	-0.4	3.60	V
Battery	LED[2:0]	-0.4	4.40	V
	SMP_VBAT	-0.4	4.25	V
	VBAT_SENSE	-0.4	4.40	V
	VREGENABLE	-0.4	4.40	V
PIO	VDD_PADS_1	-0.4	3.60	V
	VDD_PADS_2	-0.4	3.60	V
1.8 V	SMPS_1V8_SENSE	-0.4	1.95	V
	VDD_AUDIO_DRV	-0.4	1.95	V
	VDD_AUX_1V8	-0.4	1.95	V
1.35 V	SMPS_1V35_SENSE	-0.4	1.45	V
	VDD_AUDIO	-0.4	1.45	V
	VREGIN_DIG	-0.4	1.95	V
Other terminal voltages		VSS - 0.4	VDD + 0.4 ≤ 3.60 ^(a)	V

^(a) VDD is the VDD_PADS supply domain for this I/O. For more information, see Section 1.2. Voltage should not exceed 3.6 V on any I/O.

12.2 Recommended Operating Conditions

Rating		Min	Typ	Max	Unit
Operating temperature range		-40	20	85	°C
Supply Voltage					
5 V (USB VBUS)	VCHG	4.75 / 3.10 ^(a)	5.00	6.50	V
3.3 V	SMP_BYP	3.10	3.30	3.60	V
	VDD_USB	3.10	3.30	3.60	V
Battery	LED[2:0]	1.10	3.70	4.30	V
	SMP_VBAT	2.50	3.70	4.30	V
	VBAT_SENSE	0	3.70	4.25	V
	VREGENABLE	0	3.70	4.25	V
PIO	VDD_PADS_1	1.70	1.80	3.60	V
	VDD_PADS_2	1.70	1.80	3.60	V
1.8 V	SMPS_1V8_SENSE	1.70	1.80	1.95	V
	VDD_AUDIO_DRV	1.70	1.80	1.95	V
	VDD_AUX_1V8	1.70	1.80	1.95	V
1.35 V	SMPS_1V35_SENSE	1.30	1.35	1.45	V
	VDD_AUDIO	1.30	1.35	1.45	V
	VREGIN_DIG	1.30	1.35 or 1.80 ^(b)	1.95	V

^(a) Minimum input voltage of 4.75 V is required for full specification. Regulator operates at reduced load current from 3.1 V.

^(b) Typical value depends on output required by the low-voltage VDD_DIG linear regulator, see Section 12.3.2.2

12.3 Input/Output Terminal Characteristics

Note:

For all I/O terminal characteristics:

- Current drawn into a pin is defined as positive. Current supplied out of a pin is defined as negative.

12.3.1 Regulators: Available For External Use

12.3.1.1 1.8 V Switch-mode Regulator

1.8 V Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	2.80	3.70	4.25	V
Output voltage	1.70	1.80	1.90	V
Normal Operation				
Transient settling time	-	30	-	μs
Load current	-	-	185	mA
Current available for external use, audio with 16 Ω load ^(a)	-	-	25	mA
Peak conversion efficiency ^(b)	-	90	-	%
Switching frequency	3.63	4.00	4.00	MHz
Inductor saturation current (-30% reduction from the nominal inductor value)	250	-	-	mA
Inductor ESR	0.1	0.3	0.8	Ω
Low-power Mode, Automatically Entered in Deep Sleep				
Transient settling time	-	200	-	μs
Load current	0.005	-	5	mA
Current available for external use	-	-	5	mA
Peak conversion efficiency	-	85	-	%
Switching frequency	100	-	200	kHz

^(a) More current available for audio loads above 16 Ω.

^(b) Conversion efficiency depends on inductor selection.

12.3.1.2 Combined 1.8 V and 1.35 V Switch-mode Regulator

Combined 1.8 V and 1.35 V Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	2.80	3.60	4.25	V
Output voltage	1.70	1.80	1.90	V
Normal Operation				
Transient settling time	-	30	-	μs
Load current	-	-	340	mA
Current available for external use, audio with 16 Ω load ^(a)	-	-	25	mA
Peak conversion efficiency ^(b)	-	90	-	%
Switching frequency	3.63	4.00	4.00	MHz
Inductor saturation current (-30% reduction from the nominal inductor value)	250	-	-	mA
Inductor ESR	0.1	0.3	0.8	Ω
Low-power Mode, Automatically Entered in Deep Sleep				
Transient settling time	-	200	-	μs
Load current	0.005	-	5	mA
Current available for external use	-	-	5	mA
Peak conversion efficiency	-	85	-	%
Switching frequency	100	-	200	kHz

^(a) More current available for audio loads above 16 Ω.

^(b) Conversion efficiency depends on inductor selection.

12.3.1.3 Bypass LDO Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	4.25 / 3.10 ^(a)	5.00	5.75 / 6.50 ^(b)	V
Output voltage ($V_{in} > 4.75$ V)	3.00	3.30	3.60	V
Output current ($V_{in} > 4.75$ V)	-	-	250	mA

^(a) Minimum input voltage of 4.25 V is required for full specification, regulator operates at reduced load current from 3.1 V.

^(b) Standard maximum input voltage is 5.75 V, a 6.50 V maximum requires a correct patch bundle. For more information, contact CSR.

12.3.2 Regulators: For Internal Use Only

12.3.2.1 1.35 V Switch-mode Regulator

1.35 V Switch-mode Regulator	Min	Typ	Max	Unit
Input voltage	2.80	3.60	4.25	V
Output voltage	1.30	1.35	1.40	V
Normal Operation				
Transient settling time	-	30	-	μs
Load current	-	-	160	mA
Current available for external use	-	-	0	mA
Peak conversion efficiency ^(a)	-	88	-	%
Switching frequency	3.63	4.00	4.00	MHz
Inductor saturation current (-30% reduction from the nominal inductor value)	250	-	-	mA
Inductor ESR	0.1	0.3	0.8	Ω
Low-power Mode, Automatically Entered in Deep Sleep				
Transient settling time	-	200	-	μs
Load current	0.005	-	5	mA
Current available for external use	-	-	0	mA
Peak conversion efficiency	-	85	-	%
Switching frequency	100	-	200	kHz

^(a) Conversion efficiency depends on inductor selection.

12.3.2.2 Low-voltage VDD_DIG Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.30	1.35 or 1.80	1.95	V
Output voltage ^(a)	0.80	0.90 / 1.20	1.25	V
Internal load current	-	-	80	mA

^(a) Output voltage level is software controlled.

12.3.2.3 Low-voltage VDD_AUX Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.70	1.80	1.95	V
Output voltage	1.30	1.35	1.45	V
Internal load current	-	-	5	mA

12.3.2.4 Low-voltage VDD_ANA Linear Regulator

Normal Operation	Min	Typ	Max	Unit
Input voltage	1.70	1.80	1.95	V
Output voltage	1.30	1.35	1.45	V
Load current	-	-	60	mA

12.3.3 Regulator Enable

VREGENABLE, Switching Threshold	Min	Typ	Max	Unit
Rising threshold	-	-	1.0	V

12.3.4 Battery Charger

Battery Charger	Min	Typ	Max	Unit
Input voltage, VCHG	4.75 / 3.10 ^(a)	5.00	6.50 ^(b)	V

^(a) Reduced specification from 3.1 V to 4.75 V. Full specification >4.75 V.

^(b) Standard maximum input voltage is 5.75 V, a 6.50 V maximum requires a correct patch bundle. For more information, contact CSR.

Trickle Charge Mode	Min	Typ	Max	Unit
Charge current I_{trickle} , as percentage of fast charge current	8	10	12	%
V_{fast} rising threshold	-	2.9	-	V
V_{fast} rising threshold trim step size	-	0.1	-	V
V_{fast} falling threshold	-	2.8	-	V

Fast Charge Mode		Min	Typ	Max	Unit
Charge current during constant current mode, I _{fast}	Maximum charge setting (VCHG-VBAT > 0.55 V)	194	200	206	mA
	Minimum charge setting (VCHG-VBAT > 0.55 V)	-	10	-	mA
Reduced headroom charge current, as a percentage of I _{fast}	(VCHG-VBAT < 0.55 V)	50	-	100	%
Charge current step size		-	10	-	mA
V _{float} threshold, calibrated		4.16	4.20	4.24	V
Charge termination current I _{term} , as percentage of I _{fast}		7	10	20	%

Standby Mode	Min	Typ	Max	Unit
Voltage hysteresis on VBAT, V_{hyst}	100	-	150	mV

Error Charge Mode	Min	Typ	Max	Unit
Headroom ^(a) error falling threshold	-	50	-	mV

^(a) Headroom = VCHG - VBAT

External Charge Mode ^(a)	Min	Typ	Max	Unit
Fast charge current, I_{fast}	200	-	500	mA
Control current into CHG_EXT	0	-	20	mA
Voltage on CHG_EXT	0	-	5.75 / 6.50 ^(b)	V
External pass device h_{fe}	-	50	-	-
Sense voltage, between VBAT_SENSE and VBAT at maximum current	195	200	205	mV

^(a) In the external mode, the battery charger meets all the previous charger electrical characteristics and the additional or superseded electrical characteristics are listed in this table.

^(b) Standard maximum input voltage is 5.75 V, a 6.50 V maximum requires a correct patch bundle. For more information, contact CSR.

12.3.5 USB

USB	Min	Typ	Max	Unit
VDD_USB for correct USB operation	3.1	3.3	3.6	V
Input Threshold				
V _{IL} input logic level low	-	-	0.3 x VDD_USB	V
V _{IH} input logic level high	0.7 x VDD_USB	-	-	V
Output Voltage Levels to Correctly Terminated USB Cable				
V _{OL} output logic level low	0	-	0.2	V
V _{OH} output logic level high	2.8	-	VDD_USB	V

12.3.6 Stereo Codec: Analogue to Digital Converter

Analogue to Digital Converter						
Parameter	Conditions		Min	Typ	Max	Unit
Resolution	-		-	-	16	Bits
Input Sample Rate, F_{sample}	-		8	-	48	kHz
Maximum ADC Input Signal Amplitude	0 dB = 1600 mV _{pk-pk}		13	-	2260	mV _{pk-pk}
SNR	f _{in} = 1 kHz B/W = 20 Hz→F _{sample} /2 (20 kHz max) A-Weighted THD+N < 0.1% 1.6 V _{pk-pk} input	F _{sample}				
		8 kHz	-	94.4	-	dB
		16 kHz	-	92.4	-	dB
		32 kHz	-	92.5	-	dB
		44.1 kHz	-	93.2	-	dB
		48 kHz	-	91.9	-	dB
THD+N	f _{in} = 1 kHz B/W = 20 Hz→F _{sample} /2 (20 kHz max) 1.6 V _{pk-pk} input	F _{sample}				
		8 kHz	-	0.004	-	%
		48 kHz	-	0.016	-	%
Digital gain	Digital gain resolution = 1/32		-24	-	21.5	dB
Analogue gain	Pre-amplifier setting = 0 dB, 9 dB, 21 dB or 30 dB Analogue setting = -3 dB to 12 dB in 3 dB steps		-3	-	42	dB
Stereo separation (crosstalk)			-	-89.9	-	dB

12.3.7 Stereo Codec: Digital to Analogue Converter

Digital to Analogue Converter							
Parameter	Conditions			Min	Typ	Max	Unit
Resolution	-			-	-	16	Bits
Output Sample Rate, F _{sample}	-			8	-	96	kHz
SNR	f _{in} = 1 kHz B/W = 20 Hz→20 kHz A-Weighted THD+N < 0.1% 0 dBFS input	F _{sample}	Load				
		48 kHz	100 kΩ	-	95.4	-	dB
		48 kHz	32 Ω	-	96.5	-	dB
		48 kHz	16 Ω	-	95.8	-	dB
THD+N	f _{in} = 1 kHz B/W = 20 Hz→20 kHz 0 dBFS input	F _{sample}	Load				
		8 kHz	100 kΩ	-	0.0021	-	%
		8 kHz	32 Ω	-	0.0031	-	%
		8 kHz	16 Ω	-	0.0034	-	%
		48 kHz	100 kΩ	-	0.0037	-	%
		48 kHz	32 Ω	-	0.0029	-	%
		48 kHz	16 Ω	-	0.0042	-	%
Digital Gain	Digital Gain Resolution = 1/32			-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3 dB			-21	-	0	dB
Output voltage	Full-scale swing (differential)			-	-	778	mV rms
Stereo separation (crosstalk)				-	-90.5	-	dB

12.3.8 Digital

Digital Terminals	Min	Typ	Max	Unit
Input Voltage				
V_{IL} input logic level low	-0.4	-	0.4	V
V_{IH} input logic level high	$0.7 \times V_{DD}$	-	$V_{DD} + 0.4$	V
T_r/T_f	-	-	25	ns
Output Voltage				
V_{OL} output logic level low, $I_{OL} = 4.0$ mA	-	-	0.4	V
V_{OH} output logic level high, $I_{OH} = -4.0$ mA	$0.75 \times V_{DD}$	-	-	V
T_r/T_f	-	-	5	ns
Input and Tristate Currents				
Strong pull-up	-150	-40	-10	μ A
Strong pull-down	10	40	150	μ A
Weak pull-up	-5	-1.0	-0.33	μ A
Weak pull-down	0.33	1.0	5.0	μ A
C_I Input Capacitance	1.0	-	5.0	pF

12.3.9 LED Driver Pads

LED Driver Pads		Min	Typ	Max	Unit
Current, I_{PAD}	High impedance state	-	-	5	μ A
	Current sink state	-	-	10	mA
LED pad voltage, V_{PAD}	$I_{PAD} = 10$ mA	-	-	0.55	V
LED pad resistance	$V_{PAD} < 0.5$ V	-	-	40	Ω
V_{OL} output logic level low ^(a)		-	0	-	V
V_{OH} output logic level high ^(a)		-	0.8	-	V
V_{IL} input logic level low		-	0	-	V
V_{IH} input logic level high		-	0.8	-	V

^(a) LED output port is open-drain and requires a pull-up

12.3.10 Auxiliary ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	10	Bits
Input voltage range ^(a)		0	-	VDD_AUX	V
Accuracy (Guaranteed monotonic)	INL	-1	-	1	LSB
	DNL	0	-	1	LSB
Offset		-1	-	1	LSB
Gain error		-0.8	-	0.8	%
Input bandwidth		-	100	-	kHz
Conversion time		1.38	1.69	2.75	µs
Sample rate ^(b)		-	-	700	Samples/s

^(a) LSB size = VDD_AUX/1023

^(b) The auxiliary ADC is accessed through a VM function. The sample rate given is achieved as part of this function.

12.3.11 Auxiliary DAC

Auxiliary DAC		Min	Typ	Max	Unit
Resolution		-	-	10	Bits
Supply voltage, VDD_AUX		1.30	1.35	1.40	V
Output voltage range		0	-	VDD_AUX	V
Full-scale output voltage		1.30	1.35	1.40	V
LSB size		0	1.32	2.64	mV
Offset		-1.32	0	1.32	mV
Integral non-linearity		-1	0	1	LSB
Settling time ^(a)		-	-	250	ns

^(a) The settling time does not include any capacitive load

Important Note:

Access to the auxiliary DAC is firmware-dependent. For more information about its availability, contact CSR.

12.4 ESD Protection

Apply ESD static handling precautions during manufacturing.

Table 12.1 shows the ESD handling maximum ratings.

Condition	Class	Max Rating
Human Body Model Contact Discharge per ANSI/ESDA/JEDEC JS-001	2	2 kV (all pins except CHG_EXT. CHG_EXT is rated at 1 kV)
Charged Device Model Contact Discharge per JEDEC/EIA JESD22-C101	III	500 V (all pins)

Table 12.1: ESD Handling Ratings

12.4.1 USB Electrostatic Discharge Immunity

CSRA64210 QFN has integrated ESD protection on the USB_DP and USB_DN pins as detailed in IEC 61000-4-2.

CSR has tested CSRA64210 QFN assembled in development kits to assess the Electrostatic Discharge Immunity. The tests were based on IEC 61000-4-2 requirements. Tests were performed up to level 4 (8 kV contact discharge / 15 kV air discharge).

CSR can demonstrate normal performance up to level 2 (4 kV contact discharge / 4 kV air discharge) as per IEC 6100-4-2 classification 1. Above level 2, temporary degradation is seen (classification 2).

CSRA64210 QFN contains a reset protection circuit and software, which will attempt to re-make any connections lost in a ESD event. If the device at the far end permits this, self-recovery of the Bluetooth link is possible if CSRA64210 QFN resets on an ESD strike. This classes CSRA64210 QFN as IEC 61000-4-2 classification 2 to level 4 (8 kV contact discharge / 15 kV air discharge). If self-recovery is not implemented, CSRA64210 QFN is IEC 61000-4-2 classification 3 to level 4.

Note:

Any test detailed in the IEC-61000-4-2 level 4 test specification does not damage CSRA64210 QFN.

The CSRA64210 QFN USB VBUS pin is protected to level 4 using an external 2.2 μ F decoupling capacitor on VCHG.

Important Note:

CSR recommends correct PCB routing and to route the VBUS track through a decoupling capacitor pad.

When the USB connector is a long way from CSRA64210 QFN, place an extra 1 μ F or 2.2 μ F capacitor near the USB connector.

No components (including 22 Ω series resistors) are required between CSRA64210 QFN and the USB_DP and USB_DN lines.

To recover from an unintended reset, e.g. a large ESD strike, the watchdog and reset protection feature can restart CSRA64210 QFN and signal the unintended reset to the VM.

Table 12.2 summarises the level of protection.

IEC 61000-4-2 Level	ESD Test Voltage (Positive and Negative)	IEC 61000-4-2 Classification	Comments
1	2 kV contact / 2 kV air	Class 1	Normal performance within specification limits
2	4 kV contact / 4 kV air	Class 1	Normal performance within specification limits
3	6 kV contact / 8 kV air	Class 2 or class 3	Temporary degradation or operator intervention required
4	8 kV contact / 15 kV air	Class 2 or class 3	Temporary degradation or operator intervention required

Table 12.2: USB Electrostatic Discharge Protection Level

For more information contact CSR.

13 Power Consumption

DUT Role	Connection		Packet Type	Packet Size	Average Current	Unit
Slave	SCO		HV3	30	TBD	mA
Slave	eSCO		EV3	30	TBD	mA
Slave	eSCO		3EV3	60	TBD	mA
Slave	SCO	1-mic cVc hands-free: <ul style="list-style-type: none"> 8 kHz sampling Narrowband 	HV3	30	TBD	mA
Slave	eSCO	1-mic cVc hands-free: <ul style="list-style-type: none"> 8 kHz sampling Narrowband 	2EV3	60	TBD	mA
Slave	eSCO	1-mic cVc hands-free: <ul style="list-style-type: none"> 16 kHz sampling Wideband 	2EV3	60	TBD	mA
Slave	eSCO	1-mic cVc hands-free: <ul style="list-style-type: none"> 16 kHz sampling FESI 	2EV3	60	TBD	mA
Slave	A2DP Stereo streaming SBC high quality: <ul style="list-style-type: none"> Bit-Pool = 50, 16 blocks and 8 sub-bands 48 kHz sampling No sniff White noise 		-	-	TBD	mA
Slave	A2DP Stereo streaming SBC low quality: <ul style="list-style-type: none"> Bit-Pool = 20, 16 blocks and 8 sub-bands 48 kHz sampling No sniff White noise 		-	-	TBD	mA
Slave	ACL	Sniff = 500 ms	-	-	TBD	μA
Slave	ACL	Sniff = 1280 ms	-	-	TBD	μA
Master	SCO		HV3	30	TBD	mA
Master	eSCO		EV3	30	TBD	mA
Master	eSCO		3EV3	60	TBD	mA
Master	SCO	1-mic cVc hands-free: <ul style="list-style-type: none"> 8 kHz sampling Narrowband 	HV3	30	TBD	mA

DUT Role	Connection		Packet Type	Packet Size	Average Current	Unit
Master	eSCO	1-mic cVc hands-free: <ul style="list-style-type: none"> 8 kHz sampling Narrowband 	2EV3	60	TBD	mA
Master	eSCO	1-mic cVc hands-free: <ul style="list-style-type: none"> 16 kHz sampling Wideband 	2EV3	60	TBD	mA
Master	eSCO	1-mic cVc hands-free: <ul style="list-style-type: none"> 16 kHz sampling FESI 	2EV3	60	TBD	mA
Master	A2DP Stereo streaming SBC high quality: <ul style="list-style-type: none"> Bit-Pool = 50, 16 blocks and 8 sub-bands 48 kHz sampling No sniff White noise 		-	-	TBD	mA
Master	A2DP Stereo streaming SBC low quality: <ul style="list-style-type: none"> Bit-Pool = 20, 16 blocks and 8 sub-bands 48 kHz sampling No sniff White noise 		-	-	TBD	mA
Master	ACL	Sniff = 500 ms	-	-	TBD	μA
Master	ACL	Sniff = 1280 ms	-	-	TBD	μA

Note:

Current consumption values are taken with:

- VBAT pin = 3.7 V
- RF TX power set to 0 dBm
- No RF retransmissions in case of eSCO
- Microphones and speakers disconnected
- Audio gateway transmits silence when SCO/eSCO channel is open
- LEDs disconnected
- AFH classification master disabled

14 CSR Green Semiconductor Products and RoHS Compliance

CSR confirms that CSR Green semiconductor products comply with the following regulatory requirements:

- Restriction of Hazardous Substances directive guidelines in the EU RoHS Directive 2011/65/EU¹.
- EU REACH, Regulation (EC) No 1907/2006¹:
 - List of substances subject to authorisation (Annex XIV)
 - Restrictions on the manufacture, placing on the market and use of certain dangerous substances, preparations and articles (Annex XVII). This Annex now includes requirements that were contained within EU Directive, 76/769/EEC. There are many substance restrictions within this Annex, including, but not limited to, the control of use of Perfluorooctane sulfonates (PFOS).
 - When requested by customers, notification of substances identified on the Candidate List as Substances of Very High Concern (SVHC)¹.
- POP regulation (EC) No 850/2004¹
- EU Packaging and Packaging Waste, Directive 94/62/EC¹
- Montreal Protocol on substances that deplete the ozone layer.
- Conflict minerals, Section 1502, Dodd-Frank Wall Street Reform and Consumer Protection act, which affects columbite-tantalite (coltan / tantalum), cassiterite (tin), gold, wolframite (tungsten) or their derivatives. CSR is a fabless semiconductor company: all manufacturing is performed by key suppliers. CSR have mandated that the suppliers shall not use materials that are sourced from "conflict zone mines" but understand that this requires accurate data from the EICC programme. CSR shall provide a complete EICC / GeSI template upon request.

CSR has defined the "CSR Green" standard based on current regulatory and customer requirements including free from bromine, chlorine and antimony trioxide.

Products and shipment packaging are marked and labelled with applicable environmental marking symbols in accordance with relevant regulatory requirements.

This identifies the main environmental compliance regulatory restrictions CSR specify. For more information on the full "CSR Green" standard, contact product.compliance@csr.com.

¹ Including applicable amendments to EU law which are published in the EU Official Journal, or SVHC Candidate List updates published by the European Chemicals Agency (ECHA).

15 Software

CSRA64210 QFN:

- Includes integrated Bluetooth v4.2 specification qualified HCI stack firmware
- Includes integrated CSRA64210 Stereo ROM Solution, with 8th generation 1-mic cVc hands-free audio enhancements and a configurable EQ
- Can be shipped with CSR's CSRA64210 stereo ROM solution development kit for CSRA64210 QFN, order code DK-64210-TBD-TBD

The CSRA64210 QFN software architecture enables Bluetooth processing and the application program to run on the internal RISC MCU and the audio enhancements on the Kalimba DSP.

15.1 CSRA64210 Stereo ROM Solution

The CSRA64210 stereo ROM solution software supports:

- 8th generation 1-mic cVc hands-free audio enhancements
- WNR
- PLC / BEC
- mSBC wideband speech codec
- A2DP v1.3
- HFP v1.6 and HSP v1.2
- SCMS-T
- Bluetooth v4.2 specification is supported in the ROM software
- Secure simple pairing
- Proximity pairing (device-initiated pairing) for greatly simplifying the out-of-box pairing process
- For connection to more than 1 mobile phone, Advanced Multipoint is supported. This enables a user to take calls from a work and personal phone or a work phone and a VoIP dongle for Skype users. This has minimal impact on power consumption and is easy to configure.
- Most of the CSRA64210 stereo ROM solution ROM software features are configured on the CSRA64210 QFN using the CSRA64xxx ROM Series Configuration Tool. The tool reads and writes device configurations directly to the serial flash or alternatively to a PSR file. Configurable device features include:
 - Bluetooth v4.2 specification features
 - Reconnection policies, e.g. reconnect on power-on
 - Audio features, including default volumes
 - Button events: configuring button presses and durations for certain events, e.g. double press on PIO[1] for last number redial
 - LED indications for states, e.g. device connected, and events, e.g. power on
 - Indication tones for events and ringtones
 - HFP v1.6 supported features
 - Battery divider ratios and thresholds, e.g. thresholds for battery low indication, full battery etc.
 - Advanced Multipoint settings
- User configurable EQ for music playback (rock, pop, classical, jazz, dance etc)
- Manufacturer configurable Speaker EQ with 10 stages
- AAC and SBC
- TrueWireless Stereo (TWS)
- Stereo widening (S3D)
- MeloD Expansion 3D stereo widening and phase shifting effect
- Volume Boost
- USB audio mode for streaming high-quality music from a PC whilst charging, enables the device to:
 - Play back high-quality stereo music, e.g. iTunes
 - Use bidirectional audio in conversation mode, e.g. for Skype
- Wired audio mode for pendant-style devices supports music playback using a line-in jack. Enables non Bluetooth operation in low battery modes or when using the device in an airplane-mode.
- Support for smartphone applications (apps)
- The CSRA64210 stereo ROM solution has undergone extensive interoperability testing to ensure it works with the majority of phones on the market

15.1.1 Advanced Multipoint Support

Advanced Multipoint enables the connection of 2 devices to a CSRA64210 QFN device at the same time, examples include:

- 2 phones connected to a CSRA64210 QFN device
- Phone and a VoIP dongle connected to a CSRA64210 QFN device
- Phone and tablet

The CSRA64210 stereo ROM solution:

- Supports up to 2 simultaneous connections (either HFP or HSP)
- Enables multiple-call handling from both devices at the same time
- Treats all device buttons:
 - During a call from one device, as if there is 1 device connected
 - During multiple calls (1 on each device), as if there is a single AG with multiple calls in progress (three-way calling)
 - During multiple calls (more than 1 on each device), as if there are multiple calls on a single device enabling the user to switch between the active and held calls

15.1.2 A2DP Multipoint Support

A2DP Multipoint support enables the connection of 2 A2DP source devices to CSRA64210 QFN at the same time, examples include:

- 2 A2DP-capable phones connected to a CSRA64210 QFN device
- A2DP-capable phone and an A2DP-only source device, e.g. a PC or an iPod touch

The CSRA64210 stereo ROM solution enables:

- Music streaming from either of the connected A2DP source devices where the music player is controlled on the source device
- Advanced HFP Multipoint functions to interrupt music streaming for calls, and resume music streaming on the completion of the calls
- AVRCP v1.5 connections to both connected devices, enabling the device to remotely control the primary device, i.e. the device currently streaming audio

15.1.3 Wired Audio Mode

CSRA64210 QFN supports a wired audio mode for playing music over a wired connection.

If CSRA64210 QFN is powered, the audio path is routed through CSRA64210 QFN, including via the DSP, this enables the CSRA64210 QFN to:

- Mix audio sources, e.g. tones and programmable audio prompts
- Control the volume of the audio, i.e. volume up and volume down
- Utilise the 10-band Speaker EQ

In wired audio mode, if required, the CSRA64210 QFN is still available for Bluetooth audio. This enables seamless transition from wired audio mode to Bluetooth audio mode and back again. This transition is configurable to occur automatically as the battery voltage of the device reduces to a point at which Bluetooth audio is no longer possible.

The carrier board features a stereo line-in with detect.

15.1.4 USB Modes Including USB Audio Mode

CSRA64210 QFN supports a variety of USB modes which enables the USB interface to extend the functionality of a CSRA64210 QFN based stereo device.

CSRA64210 QFN supports:

- USB charger enumeration
- USB soundcard enumeration (USB audio mode)
- USB mass storage enumeration

USB audio mode enables the device to enumerate as a soundcard while charging from a USB master device, e.g. a PC. In this mode, the device enumerates as either a stereo music soundcard (for high quality music playback) or a bidirectional voice quality soundcard. This enables the device for either listening to music streaming from the USB host device or for voice applications, e.g. Skype.

The USB audio mode operates at the same time as the wired audio mode and the USB audio interrupts the wired audio mode if USB audio is attached. This enables a device to have both wired audio and USB modes connected at the same time.

In USB audio mode, if required, the device is still available for Bluetooth audio.

15.1.5 Smartphone Applications (Apps)

CSRA64210 QFN includes CSR's proprietary mechanism for communicating with smartphone apps, it enables full UI control of the device from within the application running on a smartphone, e.g. Google Android OS-based handset. For more information on this feature contact CSR.

15.1.6 Programmable Audio Prompts

The CSRA64210 QFN enables a user to configure and load pre-programmed audio prompts from an external SPI flash.

The programmable audio prompts provide a mechanism for higher-quality audio indications to replace standard tone indications. A programmable audio prompt is assigned to any user event in place of a standard tone.

Programmable audio prompts contain either voice prompts to indicate that events have occurred or provide user-defined higher quality ring tones/indications, e.g. custom power on/off tones.

The CSRA64xxx ROM Series Configuration Tool can generate the content for the programmable audio prompts from standard WAV audio files. The tool also enables the user to configure which prompts are assigned to which user events.

Figure 15.1 shows the SPI flash interface.

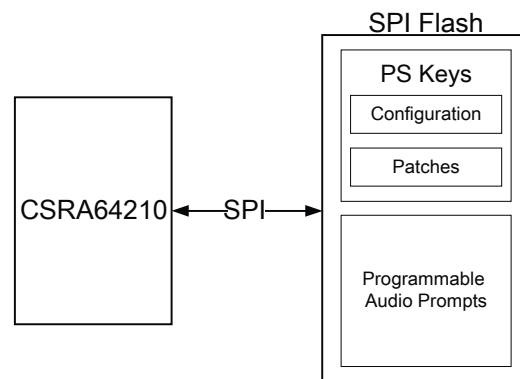


Figure 15.1: Programmable Audio Prompts in External SPI Flash

15.1.7 CSR's Intelligent Power Management

IPM extends the available talk time of a CSRA64210 QFN-based device, by automatically reducing the audio processing performed by cVc at a series of low battery capacity thresholds.

Configurable IPM features include:

- IPM enable/disable
- The battery capacity that engages IPM
- A user-action to enable or disable the IPM

If engaged, cVc processing reduces automatically on reaching the preset battery capacity. Once the audio is terminated, the DSP shuts down to achieve maximum power savings before the next call.

IPM resets when recharging the device. The talk time extension depends on:

- The battery size
- The battery condition
- The threshold capacity configured for the IPM to engage

15.1.8 Proximity Pairing

Proximity pairing is device-initiated pairing and it simplifies the out-of-box pairing process. Proximity pairing enables the device to find the closest discoverable phone. The device then initiates the pairing activity and the user simply has to accept the incoming pairing invitation on the phone.

This means that the phone-user does not have to hunt through phone menus to pair with the new device.

Depending on the phone UI:

- For a Bluetooth v2.0 phone the device pairing is with a PIN code
- For a Bluetooth v2.1 (or above) phone the device pairing is without a PIN code

Proximity pairing is based on finding and pairing with the closest phone. To do this, the device finds the loudest phone by carrying out RSSI power threshold measurements. The loudest phone is the one with the largest RSSI power threshold measurement, and it is defined as the closest device. The device then attempts to pair with and connect to this device.

Proximity pairing is configurable using the CSRA64xxx ROM Series Configuration Tool available from www.csrsupport.com.

15.1.9 Proximity Connection

Proximity connection is an extension to proximity pairing. It enables the device-user to take advantage of the proximity of devices each time the device powers up and not just during a first time pairing event.

Proximity connection enables a user with multiple handsets to easily connect to the closest discoverable phone by comparing the proximity of devices to the device at power-on to the list of previously paired devices.

Proximity connection speeds up the device connection process. It requires the device to initiate a SLC connection to the nearest device first and combines this with the device's storage of the last 8 paired/connected devices. Using proximity connection means functions operate equally well for the most or least recently paired or connected device.

15.2 8th Generation 1-mic cVc ENR Technology for Hands-free and Audio Enhancements

1-mic cVc hands-free full-duplex voice processing software is a fully integrated and highly optimised set of DSP algorithms developed to ensure easy design and build of hands-free products.

cVc enables greater acoustic design flexibility for a wide variety of environments and configurations as a result of sophisticated noise and echo suppression technology. cVc reduces the affects of noise on both sides of the conversation and smartly adjusts the receive volume levels and dynamically frequency shapes the voice to achieve optimal intelligibility and comfort for the hands-free user.

The 8th generation cVc features include:

- Full-duplex AEC
- Bit error and packet loss concealment
- Transmit and receive noise suppression including WNR
- Transmit and receive Parametric Equalisation
- Transmit and receive AGC
- Noise dependent volume control
- Receive frequency enhanced speech intelligibility using adaptive equaliser
- Narrowband, wideband and frequency expansion operations

1-mic cVc hands-free includes a tuning tool enabling the developer to easily adapt cVc with different audio configurations and tuning parameters. The tool provides real-time system statistics with immediate feedback enabling designers to quickly investigate the effect of changes.

Figure 15.2 shows the functional block diagram of CSR's proprietary 1-mic cVc hands-free DSP solution.

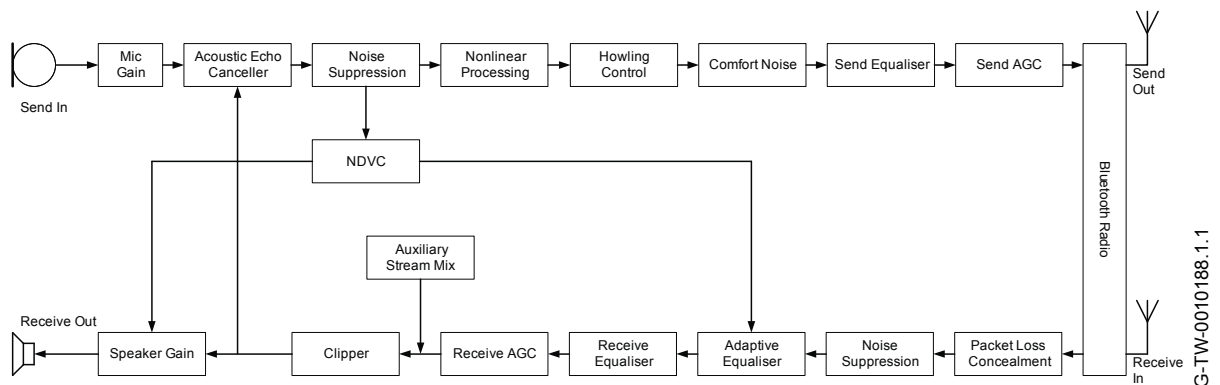


Figure 15.2: 1-mic cVc Hands-free Block Diagram

Section 15.2.1 to Section 15.2.13 describe the audio processing functions provided within cVc.

15.2.1 Acoustic Echo Cancellation

The AEC includes:

- A referenced sub-band adaptive linear filter that models the acoustic path from the receive reference point to the microphone input
- A non-linear processing function that applies narrowband and wideband attenuation adaptively as a result of residual echo present after the linear filter.

15.2.2 Noise Suppression with Wind Noise Reduction

The signal-channel noise suppression block is implemented in both signal paths. They are completely independent and individually tuned. Noise suppression is a sub-band stationary / quasi-stationary noise suppression algorithm that uses the temporal characteristics of speech and noise to remove the noise from the composite signal while maximising speech quality. The current implementation can improve the SNR by up to 20 dB.

In the transmit path, noise suppression aggressiveness is typically 95% improving SNR by 15 to 19 dB to compensate for the upstream processing and to maintain superior voice quality, while the Rx is typically tuned down to 80% improving SNR by 8 to 12 dB because of the cellular network processing. The user can parametrically adjust these default settings.

The noise suppression block contains a WNR feature (send path only). The WNR removes unwanted noise during a hands-free conversation, cleaning the audio for the far-end listener. It detects and tackle winds of various intensities and durations. Once the wind is detected, a good balance between voice quality and WNR is achieved.

15.2.3 Non-linear Processing

The non-linear processing module detects the presence of echo after the primary sub-band linear filter and adaptively applies attenuation at frequencies where echo is identified. It is used to minimise echo due to non-linearity caused by the system, for example, from the loudspeaker, microphone, amplifiers or electronics. CSR recommends minimal use of non-linear processing due to the inherent distortion that it introduces.

15.2.4 Howling Control

The Howling Control is a programmable coupling threshold that when triggered applies attenuation to the send path. This control enables cVc to operate in car-to-car calls without experiencing echo events during very high volume situations.

15.2.5 Comfort Noise Generator

The CNG:

- Creates a spectrally and temporally consistent noise floor for the far-end listener.
- Adaptively inserts noise modelled from the noise present at the microphone into gaps introduced when the non-linear processing of the AEC applies attenuation. The noise level applied is user-controllable.
- Allows selectable coloured noise.

15.2.6 Equalisation

The equalisation filters:

- Are independent in the send and receive signal channels
- Are independently enabled
- Are configurable to achieve the required frequency response
- Each channel comprises of 5 stages of cascaded 2nd order IIR filters
- Compensate for the frequency response of transducers in the system, i.e. the microphone and loud speaker

15.2.7 Automatic Gain Control

The AGC block attempts to:

- Normalise the amplitude of the incoming audio signal to a desired range to increase perceived loudness
- Reduce distortion due to clipping
- Reduce amplitude variance observed from different users, phones and networks

Maintaining a consistent long-term loudness for the speech ensures it is more easily heard by the listener and it also provides the subsequent processing block a larger amplitude signal to process. The behaviour of the AGC differs from a dynamic range audio compressor. The convergence time for the AGC is much slower to reduce the non-linear distortion.

15.2.8 Packet Loss Concealment

Bit errors and packet loss can occur in the Bluetooth transmission due to a variety of reasons, e.g. Wi-Fi interference or RF signal degradation due to distance or physical objects. As a result of these errors, the user hears glitches referred to as *pops* and *clicks* in the audio stream. The PLC block improves the receive path audio quality in the presence of bit and packet errors within the Bluetooth link by using a variety of techniques such as pitch-based waveform substitution.

The PLC tries to re-synthesise the lost packet from the history buffer with the same pitch period. The PLC uses a highly efficient 3-phase pitch estimator and performs cross-fading at the concatenation boundaries, i.e. the PLC attempts to clean up the audio signal by removing the *pops* and *clicks* and smoothing out gaps. This improves the audio quality for the user and the improved signal enables preceding processing blocks to perform better.

The PLC significantly improves dealing with bit errors, using the BFI output from the firmware. The DSP calculates an average BER and selectively applies the PLC to the incoming data. This optimises audio quality for a variety of bit errors and packet loss conditions. The PLC is enabled in all modes.

Note:

The PLC is enabled in all modes, HFK (full processing), pass-through and loopback by default.

15.2.9 Adaptive Equalisation

The adaptive equalisation block improves the intelligibility of the receive path voice signal in the presence of near end noise by altering the spectral shape of the receive path signal while maintaining the overall power level. It has been empirically observed that consonants, which are dominantly high-frequency based and much lower in amplitude than vowels, significantly contribute to the intelligibility of the voice signal. In the presence of noise, the lower amplitude consonants are masked by this noise. Therefore, by increasing the frequency of components that contribute to the consonants while in the presence of noise, the intelligibility can be improved. To maintain a consistent amplitude level, the adaptive equalisation block adaptively increases the high frequencies relative to the middle frequencies and also reduces the low frequencies accordingly. The adaptive equaliser also has the capability to compensate for variations in voice transmission channels, which include far-end devices and telecommunication channels.

The Frequency Emphasis feature can be used with any standard narrow band call, when the DAC is operating at a sample rate of 8 kHz. To complement the AEQ, High Frequency Emphasis can be added to improve the intelligibility of the far-end caller. The emphasis feature repairs frequencies (3469 Hz to 4000 Hz) that were lost due to the filters of the cellular network and Bluetooth link. Information contained in the original speech from 281 Hz to 3469 Hz is used to reconstruct the lost high frequency content.

The Frequency Expansion feature can be used with any standard narrow band call, but a special mode is invoked when the DAC operates at a sample rate of 16 kHz. The frequency expansion allows users to add in frequencies far beyond the band limits caused by the cellular network and Bluetooth link. These expansion frequencies are added between 3469 Hz and 6156 Hz. As in frequency emphasis, it uses the information contained in the original speech from 281 Hz to 3469 Hz to reconstruct the lost high frequency content.

15.2.10 Auxiliary Stream Mix

The auxiliary stream mixer enables the system to seamlessly mix audio signals such as tones, beeps and voice prompts with the incoming SCO stream. This avoids any interruption to the SCO stream and as a result prevents any speech from being lost.

15.2.11 Clipper

The clipper block intentionally distorts or *clips* the receive signal prior to the reference input of the AEC to more accurately model the behaviour of the post reference input blocks such as the DAC, power amplifier and the loudspeaker. The AEC attempts to correlate the signal received at the reference input and the microphone input. Any non-linearities introduced that are not accounted for after the reference input significantly degrade the AEC performance. This processing block can significantly improve the echo performance in cheap non-linear system designs.

15.2.12 Noise Dependent Volume Control

The NDVC block improves the intelligibility of the receive path signal by increasing the analogue DAC gain value based on the send noise estimate from the send path noise suppression block. As the send noise estimate increases, the NDVC algorithm increases the analogue DAC gain value. The NDVC uses hysteresis to minimise the artefacts generated by rapidly adjusting the DAC gain due to the fluctuation in the environmental noise.

15.2.13 Input Output Gains

Fixed gain controls are provided at the input to the cVc system. The mic gain is used set the ADC level so that proper levels can be set according to hardware constraints, industry standards and the digital resolution of the DSP fixed point processor. The speaker gain represents the output DAC which drive the speaker. The DAC level varies under software control for events such as the Bluetooth volume, NDVC, tone mixing and other volume based activities.

15.3 Music Enhancements

15.3.1 Audio Decoders

CSRA64210 QFN supports:

- SBC
- AAC
- Jitter handling and high quality sample rate matching
- Low power consumption

15.3.2 Configurable EQ

CSRA64210 QFN has 2 forms of EQ:

- User configurable EQ: Made up of up to 6 banks of 5 stages. Contains tiering for multiple customer presets, e.g. user, rock, pop, classical, jazz, etc. This enables the device user to select between the EQ bank presets through button presses.
- Manufacturer configurable speaker EQ: Made up of 1 bank of 0 to 10 stages. Contains an easy to use GUI, with drag points, see Figure 15.3.

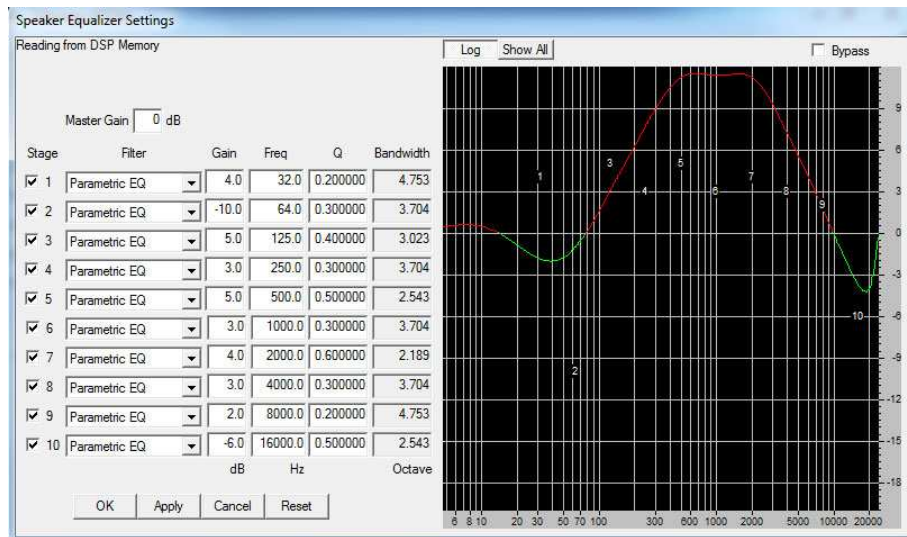


Figure 15.3: Configurable EQ GUI with Drag Points

15.3.3 Stereo Widening (S3D)

The stereo widening feature on CSRA64210 QFN:

- Simulates loudspeaker listening to provide 3D listening experience
- Is highly optimised at <1 MIPS of the Kalimba DSP
- Reduces listener fatigue for headphone listening

15.3.4 Volume Boost

The volume boost feature on the CSRA64210 QFN is a dynamic range compander and provides:

- Additional loudness without clipping
- Multi-stage compression and expansion
- Processing modules for dynamic bass boost
- Includes new optional volume control hard limiter
- Louder audio output without distortion
- Easy to use GUI, with drag points, see Figure 15.4

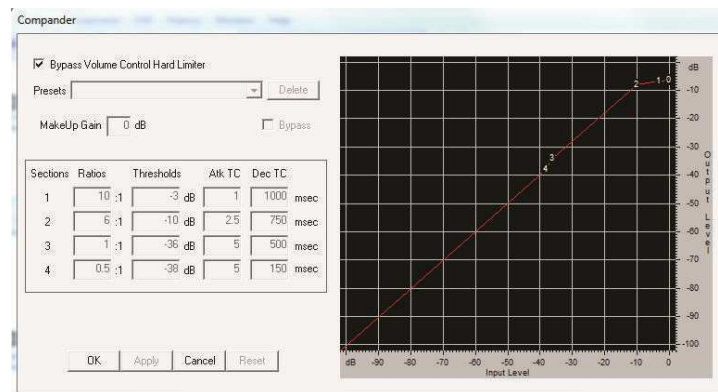


Figure 15.4: Volume Boost GUI with Drag Points

15.4 CSRA64210 Stereo ROM Solution Development Kit

CSR's audio development kit for the CSRA64210 QFN, order code DK-64210-TBD-TBD, includes a CSRA64210 stereo ROM solution demonstrator board and necessary interface adapters and cables are available. In conjunction with the CSRA64xxx ROM Series Configuration Tool and other supporting utilities the development kit provides the best environment for designing audio solutions with the CSRA64210 QFN.

Important Note:

The CSRA64210 Stereo ROM Solution audio development kit is subject to change and updates, for up-to-date information see www.csrsupport.com.

16 Tape and Reel Information

For tape and reel packing and labelling see *IC Packing and Labelling Specification*.

16.1 Tape Orientation

Figure 16.1 shows the CSRA64210 QFN packing tape orientation.

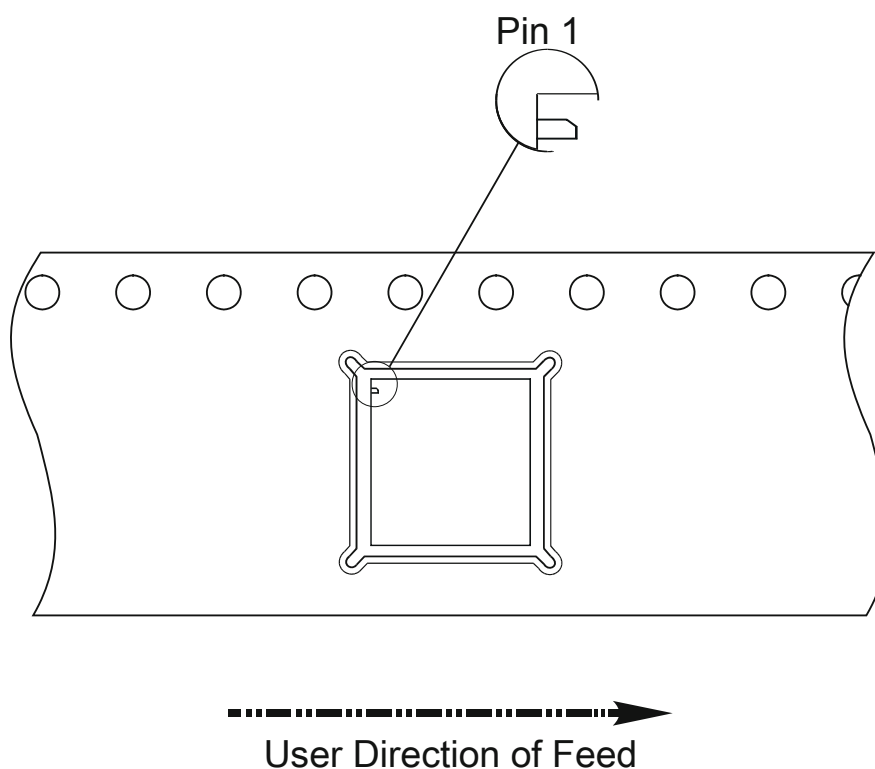
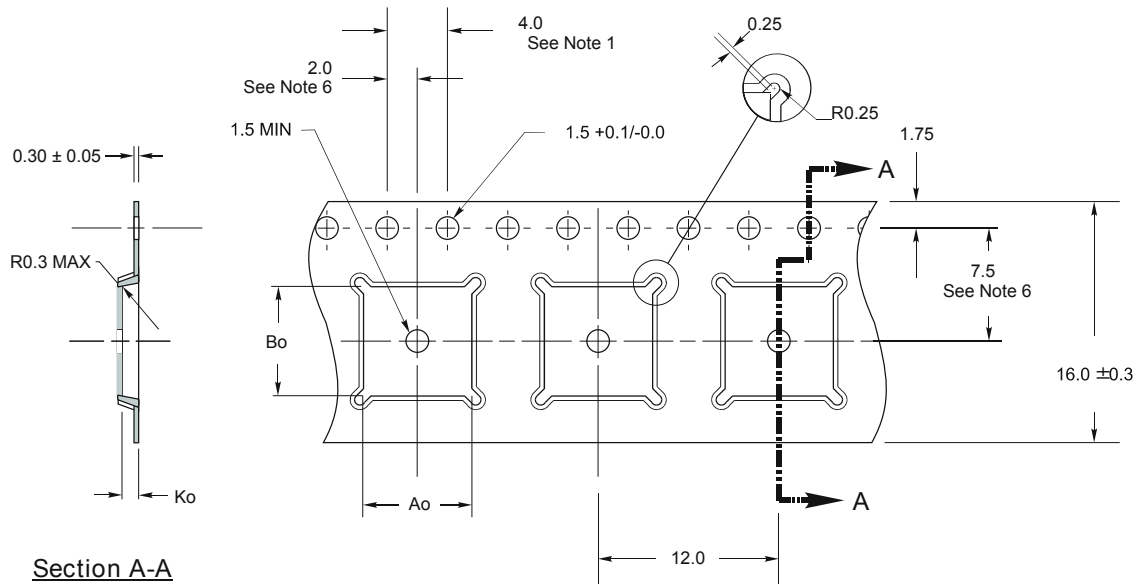


Figure 16.1: CSRA64210 QFN Tape Orientation

G-TW-0002812.2.2

16.2 Tape Dimensions



G-TW-0002811.3.2

CSRA64210 QFN Data Sheet

A ₀	B ₀	K ₀	Unit	Notes
8.30	8.30	1.10	mm	<ol style="list-style-type: none"> 10 sprocket hole pitch cumulative tolerance ±0.2 Camber not to exceed 1 mm in 100 mm Material: PS + C A₀ and B₀ measured as indicated K₀ measured from a plane on the inside bottom of the pocket to the top surface of the carrier Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

16.3 Reel Information

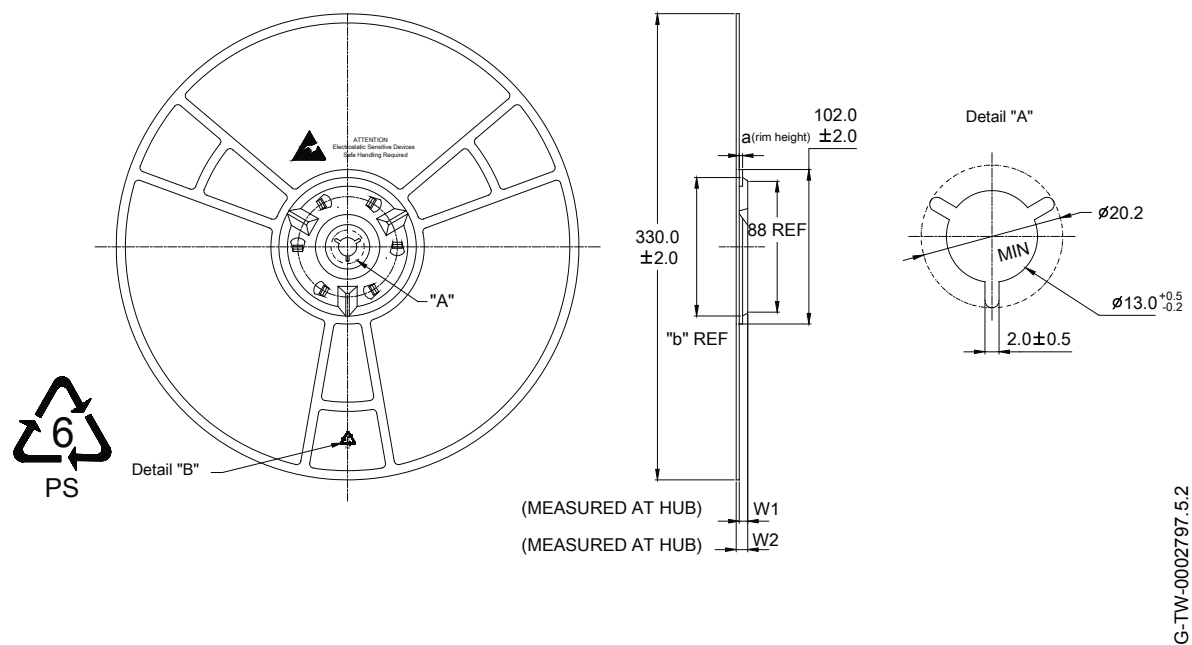


Figure 16.2: Reel Dimensions

Package Type	Nominal Hub Width (Tape Width)	a	b	W1	W2 Max	Units
8 x 8 x 0.9 mm QFN	16	4.5	98.0	16.4 (3.0/-0.2)	19.1	mm

16.4 Moisture Sensitivity Level

CSRA64210 QFN is qualified to moisture sensitivity level MSL3 in accordance with JEDEC J-STD-020.

17 Document References

Document	Reference, Date
<i>BlueCore Audio API Specification</i>	CS-209064-SP
<i>BlueTest User Guide</i>	CS-102736-UG
<i>Bluetooth and USB Design Considerations</i>	CS-101412-AN
<i>Core Specification of the Bluetooth System</i>	Bluetooth Specification Version 4.2, 02 December 2014
<i>CSRA64210 QFN Performance Specification</i>	CS-334656-SP
<i>ESDA/JEDEC Joint Standard For Electrostatic Discharge Sensitivity Testing Human Body Model (HBM) - Component Level</i>	ANSI/ESDA/JEDEC JS-001-201
<i>Field-Induced Charged-Device Model Test Method for Electrostatic- Discharge-Withstand Thresholds of Microelectronic Components</i>	JESD22-C101E
<i>IC Packing and Labelling Specification</i>	CS-112584-SP
<i>IEC 61000-4-2 Electromagnetic compatibility (EMC) – Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test</i>	IEC 61000-4-2, Edition 2.0, 2008-12
<i>Kalimba Architecture 3 DSP User Guide</i>	CS-202067-UG
<i>Lithium Polymer Battery Charger Calibration and Operation for CSR8670</i>	CS-204572-AN
<i>Moisture / Reflow Sensitivity Classification for Nonhermitic Solid State Surface Mount Devices</i>	IPC / JEDEC J-STD-020
<i>Optimising BlueCore5-Multimedia ADC Performance Application Note</i>	CS-120059-AN
<i>Typical Solder Reflow Profile for Lead-free Device</i>	CS-116434-AN
<i>Universal Serial Bus Specification</i>	v2.0, 27 April 2000
<i>USB Battery Charging Specification</i>	v1.2 December 7 th 2010, also errata and ECNs through March 15 th 2012

Terms and Definitions

Term	Definition
3G	3 rd Generation of mobile communications technology
8DPSK	8-phase Differential Phase Shift Keying
$\pi/4$ DQPSK	$\pi/4$ rotated Differential Quaternary Phase Shift Keying
μ -law	Audio companding standard (G.711)
A-law	Audio companding standard (G.711)
A2DP	Advanced Audio Distribution Profile
AAC	Advanced Audio Coding
AC	Alternating Current
ACL	Asynchronous Connection-oriented Logical (Transport)
ADC	Analogue to Digital Converter
AEC	Acoustic Echo Cancellation
AEQ	Adaptive EQualiser
AFH	Adaptive Frequency Hopping
AG	Audio Gateway
AGC	Automatic Gain Control
AIO	Analogue Input/Output
ALU	Arithmetic Logic Unit
API	Application Programming Interface
AUX	Auxiliary
AVRCP	Audio/Video Remote Control Profile
BCCMD	BlueCore CoMmanD
BCSP	BlueCore Serial Protocol
BDR	Basic Data Rate
BEC	Bit Error Concealment
BER	Bit Error Rate
BFI	Bad Frame Indicator
BIST	Built-In Self-Test
BlueCore®	Group term for CSR's range of Bluetooth wireless technology ICs
Bluetooth®	Set of technologies providing audio and data transfer over short-range radio connections
CNG	Comfort Noise Generation
codec	Coder decoder

Term	Definition
CRC	Cyclic Redundancy Check
CSR	Cambridge Silicon Radio
CTS	Clear To Send
cVc	Clear Voice Capture
CVSD	Continuously Variable Slope Delta Modulation
DAC	Digital to Analogue Converter
DC	Direct Current
DDS	Direct Digital Synthesis
DI	Device Id profile
DMA	Direct Memory Access
DNL	Differential Non Linearity (ADC accuracy parameter)
DSP	Digital Signal Processor (or Processing)
DUT	Device Under Test
e.g.	<i>exempli gratia</i> , for example
EIA	Electronic Industries Alliance
EMC	ElectroMagnetic Compatibility
EQ	EQualiser
eSCO	extended SCO
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
etc	<i>et cetera</i> , and the rest, and so forth
FIR	Finite Impulse Response (filter)
FSK	Frequency Shift Keying
G.722	An ITU-T standard wideband speech codec operating at 48, 56 and 64 kbps
GCI	General Circuit Interface
GSM	Global System for Mobile communications
GUI	Graphical User Interface
H4DS	H4 Deep Sleep
HBM	Human Body Model
HCI	Host Controller Interface
HFP	Hands-Free Profile
HSP	HeadSet Profile
I ² C	Inter-Integrated Circuit Interface

Term	Definition
I ² S	Inter-Integrated Circuit Sound
i.e.	<i>Id est</i> , that is
I/O	Input/Output
IC	Integrated Circuit
ID	IDentifier
IEC	International Electrotechnical Commission
IEEE	Institute of Electronic and Electrical Engineers
IF	Intermediate Frequency
IIR	Infinite Impulse Response (filter)
INL	Integral Non-Linearity (ADC accuracy parameter)
IPC	See www.ipc.org
IPM	Intelligent Power Management
IQ	In-Phase and Quadrature
ISDN	Integrated Services Digital Network
JEDEC	Joint Electron Device Engineering Council (now the JEDEC Solid State Technology Association)
Kalimba	An open platform DSP co-processor, enabling support of enhanced audio applications, such as echo and noise suppression and file compression / decompression
LC	An inductor (L) and capacitor (C) network
LDO	Low (voltage) Drop-Out
LED	Light-Emitting Diode
LM	Link Manager
LNA	Low Noise Amplifier
LSB	Least Significant Bit (or Byte)
MAC	Multiplier and ACcumulator
Mb	Megabit
MCU	MicroController Unit
MIPS	Million Instructions Per Second
MISO	Master In Slave Out
MLC	MultiLayer Ceramic
MMU	Memory Management Unit
mSBC	modified Sub-Band Coding
N/A	Not Applicable
NDVC	Noise Dependent Volume Control
NSMD	Non-Solder Mask Defined

Term	Definition
PA	Power Amplifier
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PIN	Personal Identification Number
PIO	Programmable Input/Output, also known as general purpose I/O
PLC	Packet Loss Concealment
plc	public limited company
PM	Physical Memory
ppm	parts per million
PS Key	Persistent Store Key
PWM	Pulse Width Modulation
QFN	Quad-Flat No-lead
RAM	Random Access Memory
RC	A Resistor and Capacitor network
RF	Radio Frequency
RGB	Red Green Blue
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive (2002/95/EC)
ROM	Read Only Memory
RS-232	Recommended Standard-232, a TIA/EIA standard for serial transmission between computers and peripheral devices (modem, mouse, etc.)
RSSI	Received Signal Strength Indication
RST	ReSeT
RTS	Request To Send
RX	Receive or Receiver
SBC	Sub-Band Coding
SCL	Serial Clock Line
SCMS	Serial Copy Management System (SCMS-T). A content protection scheme for secure transport and use of compressed digital music
SCO	Synchronous Connection-Oriented
SDA	Serial DAta (line)
SIG	(Bluetooth) Special Interest Group
SLC	Service Level Connection

Term	Definition
SMPS	Switch-Mode Power Supply
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
SQIF	Serial Quad I/O Flash (interface)
TBD	To Be Defined
TCXO	Temperature Compensated crystal Oscillator
THD+N	Total Harmonic Distortion and Noise
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
UI	User Interface
USB	Universal Serial Bus
VCO	Voltage Controlled Oscillator
VM	Virtual Machine
VoIP	Voice over Internet Protocol
W-CDMA	Wideband Code Division Multiple Access
Wi-Fi®	Wireless Fidelity (IEEE 802.11 wireless networking)
WNR	Wind Noise Reduction
XTAL	Crystal