VIBRSB 030-00885 Module Radio Board

The VIBRSB (030-00885) Module Radio Board can be used, but not limited to, the ZigBee 3.0 wireless Smart Bulb lighting platform. The module is designed and built to meet the performance, security, and reliability requirements of line-powered, smart LED lighting products and more. It is based on the Silicon Labs EFR32MG24 SoC, it includes a Bluetooth® Low Energy 5.4 implementation and 802.15.4-based full stacks to enable applications using industry-standard wireless protocols such as Zigbee® and Thread® for multiprotocol connectivity and for Matter-ready Smart Home connectivity, delivering best-in-class RF performance, CA Title 20 energy consumption compliance, future-proof capability for feature and OTA firmware updates, enhanced security, and a form factor and temperature rating suited for enclosed operation in lightbulb housings. The VIBRSB (030-00885) is designed as an FCC-certified ZigBee module. The PCA is approximately 22.5 mm x 15.50 mm x 1.35 mm. The end product will be placed in different configurations of Smart bulbs and other products.

The VIBRSB (030-00885) Module Radio Board has a single chip 802.15.4 2.4GHz Radio ZigBee transceiver/ microprocessor. It's using the 802.15.2GHz modulation scheme that is supported and provided by SiLabs for this SoC. The crystal on this transceiver/ microprocessor is driven by a 39.0 MHz crystal, which is used to produce all system internal clock signals. The core of the microprocessor runs at 78MHz, while the GPIO supports up to 10kHz PWM signal for the Smart Bulb application. The modules include a meandered inverted-F antenna (MIFA). When the device is installed in smart bulbs, there are no user accessible I/Os.

The RF transmit power level of the ZigBee transceiver is programmed into the firmware from values used during regulatory testing. These levels cannot be changed by the user. During manufacturing testing, the level of the RF power is measured to verify that the level is within the level of tolerance level of +/- 0.5dB.

The VIBRSB (030-00885) Module board gets its power from the separate PCBA, which has an onboard AC/DC switching power supply. The switching power supply provides +3.3VDC. The microprocessor requires +3.3VDC.

System Overview

Block Diagram

The 030-00885 module is a highly-integrated, high-performance system with all the hardware components needed to enable 2.4 GHz wireless connectivity and support robust networking capabilities via multiple protocols.

Built around the EFR32MG24 Wireless SoC, the 030-00885 includes a built-in PCB trace antenna, an RF matching network (optimized for transmit power efficiency), supply decoupling and filtering components, a 39 MHz reference crystal, and an RF shield.

EFR32MG24 SoC

The EFR32MG24 SoC is a Cortex®-M33 running up to 78.0 MHz and up to 1536 kB of Flash and 160 kB of RAM provides resources for demanding applications while leaving room for future growth, a rich set of MCU peripherals, and various clock management and serial interfacing options. See the EFR32xG24 Wireless Reference Manual and the EFR32MG24 Data Sheet for details.

Antenna

030-00885 modules include a meandered inverted-F antenna (MIFA) with the characteristics seen below.

Antenna Efficiency and Peak Gain

Parameter	With optimal layout	Note
Efficiency	–2.8 dB to –2.21 dB	Antenna efficiency, gain and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to Design Guidelines for PCB layout and antenna inte-gration guidelines to achieve optimal performance.
Peak gain	0.64 dBi	

Electrical Specifications

Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and VDD = 3.0 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	+125	°C
Voltage on any supply pin	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V / µs
DC voltage on any GPIO pin	V_{DIGPIN}		-0.3	—	V_{VDD} + 0.3	V
DC voltage on RESETn pin[1]	V_{RESETn}		-0.3	—	3.8	V
Total current into VDD pin	I_{VDDMAX}	Source	—	—	200	mA
Total current into GND pin	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA
Junction Temperature	T_{JMAX}		—	—	+125	°C

Note:

1. The RESETn pin has a pull-up device to the internal VDD supply. For minimum leakage, RESETn should not exceed the voltage at VDD.

Power Supply

The 030-00885 requires a single nominal supply level of 3.0 V. All the necessary decoupling and filtering components are included in the module. The module can tolerate supply voltage noise of up to 700 mVpp.

The supply voltage is filtered internally in the module with a 100 kHz low-pass filter to guarantee operation across the full supply range of 1.8 to 3.8 V. Additional external filtering is neither required nor recommended as it may cause voltage drops below the minimum level tolerable by the SoC (1.71 V) during transmit bursts.

For typical use cases, the decouple pin (DEC) should be left disconnected.

General Operating Conditions

This table specifies the general operating temperature range and supply voltage range for all supplies. The minimum and maximum values of all other tables are specifed over this operating range, unless otherwise noted.

General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A		-40	—	125	°C
VDD operating supply voltage	V_{VDD}		1.8	3.0	3.8	V
HCLK and SYSCLK frequency	f_{HCLK}	VSCALE2, MODE = WS1	—	—	78	MHz
		VSCALE2, MODE = WS0	—	—	40	MHz
		VSCALE1, MODE = WS1	—	—	40	MHz
		VSCALE1, MODE = WS0	—	—	20	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE2	—	—	78	MHz
		VSCALE1	—	—	40	MHz
EM01 Group C clock frequency	$f_{EM01GRPCCLK}$	VSCALE2	—	—	78	MHz
		VSCALE1	—	—	40	MHz
Radio HCLK frequency	f_{RHCLK}	VSCALE2 or VSCALE1	—	39.0	—	MHz

Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance, Junction to Ambient	$THETA_{JA}$	2-Layer PCB, Natural Convection[1]	—	56.6	—	°C/W
		4-Layer PCB, Natural Convection[1]	—	40.3	—	°C/W
Junction to board	Psi_{JB}	2-Layer PCB, Natural Convection[1]	—	38.5	—	°C/W
		4-Layer PCB, Natural Convection[1]	—	25.3	—	°C/W

Note:

1. Measured according to JEDEC standard JESD51-2A. Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air).
2. The device may operate continuously at the maximum allowable ambient T_A rating as long as the absolute maximum T_{JMAX} is not exceeded. For an application with significant power dissipation, the allowable T_A may be lower than the maximum T_A rating. T_A = T_{JMAX} - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_{JMAX} and $THETA_{JA}$.

RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: VDD = 3.0 V. RF center frequency 2.45 GHz. T_A = 25 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2402	—	2480	MHz

RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: VDD = 3.0 V. RF center frequency 2.45 GHz. T_A = 25 °C.

RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2402	—	2480	MHz

High-Frequency Crystal

High-Frequency Crystal

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXTAL}		—	39	—	MHz
Initial calibrated accuracy	ACC_{HFXTAL}		—	+/-5	—	ppm
Temperature drift	$DRIFT_{HFXTAL}$	Across specified temperature range	-30	—	30	ppm

GPIO Pins

Unless otherwise indicated, typical conditions are: VDD = 3.0 V.

GPIO Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, VDD = 3.0 V	—	2.5	—	nA
Input low voltage	V_{IL}	Any GPIO pin	—	—	0.3*VDD	V
		RESETn	—	—	0.3*VDD	V
Input high voltage	V_{IH}	Any GPIO pin	0.7*VDD	—	—	V
		RESETn	0.7*VDD	—	—	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05*VDD	—	—	V
		RESETn	0.05*VDD	—	—	V
Output high voltage	V_{OH}	Sourcing 20 mA, VDD = 3.0 V	0.8 * VDD	—	—	V
Output low voltage	V_{OL}	Sinking 20 mA, VDD = 3.0 V	—	—	0.2 * VDD	V
GPIO rise time	T_{GPIO_RISE}	VDD = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns
GPIO fall time	T_{GPIO_FALL}	VDD = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
Pull up/down resistance	R_{PULL}	Any GPIO pin. Pull-up to VDD: MODEn = DISABLE DOUT=1. Pull-down to GND: MODEn = WIREDORPULLDOWN DOUT = 0.	—	44	—	kΩ
		RESETn pin. Pull-up to VDD	—	44	—	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	27	—	ns

Microcontroller Peripherals

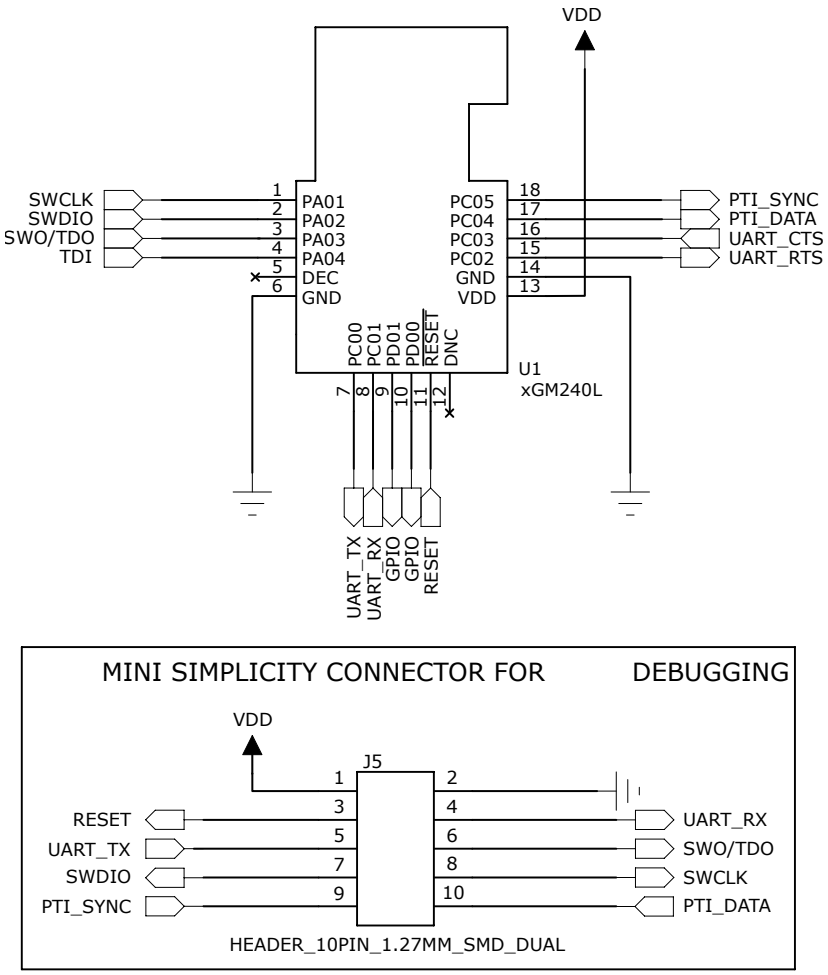
The MCU peripherals set available in 030-00885 modules

includes:

- 12-bit 1 Msps ADC
- Analog Comparators
- 16-bit and 32-bit Timers/Counters
- 24-bit Low Energy Timer for waveform generation
- 32-bit Real Time Counter
- USART (UART/SPI/SmartCards/IrDA/I2S)
- I^2C peripheral interfaces
- 12 Channel Peripheral Reflex System

Reference Diagrams

A typical application circuit for the 030-00885 module is shown below.



030-00885 Application Schematic

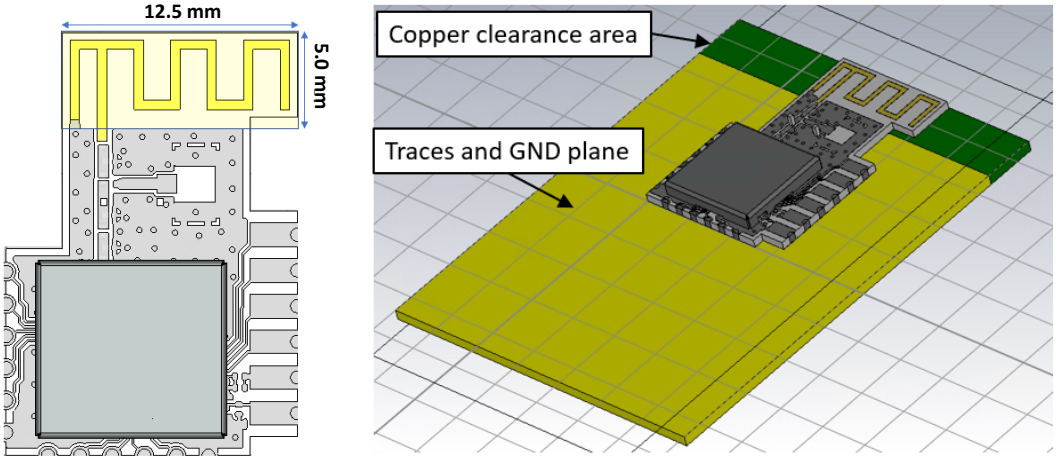
Interconnection labels correspond to supported pin functions described in Debug section.

Placing the module horizontally on the end-application board permits access to all module pins. Placing it vertically restricts access to pins 13 through 18 only. The reference schematic above is applicable for the former case only. Refer to Design Guidelines for more details.

Design Guidelines

Module Placement

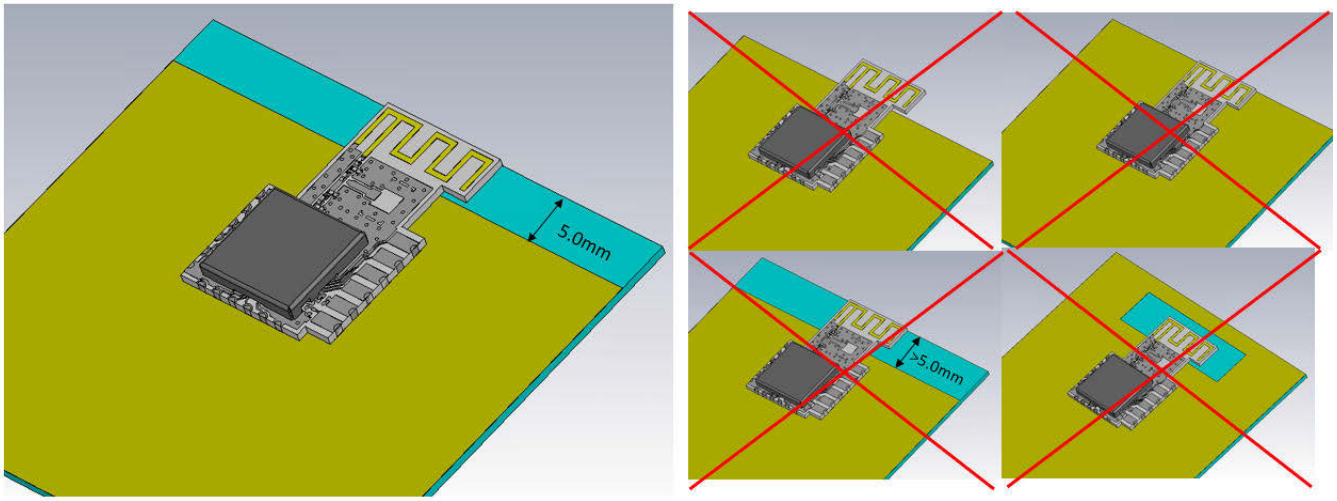
The 030-00885 should be placed at the edge of the end-application PCB as seen below. The copper clearance area under the antenna must be void of traces or components to prevent parasitic loading or undesired coupling of signals or noise to the antenna. The width of the GND pour on the end-application PCB should match at least the width of the antenna (e.g. 12.5 mm or greater) to have negligible effect on antenna performance.



Inverted-F Antenna Clearance

030-00885 modules do not support the use of an external, alternative antenna. The U.FL connector land pattern on the top layer of the module should not be used, populated or tampered with.

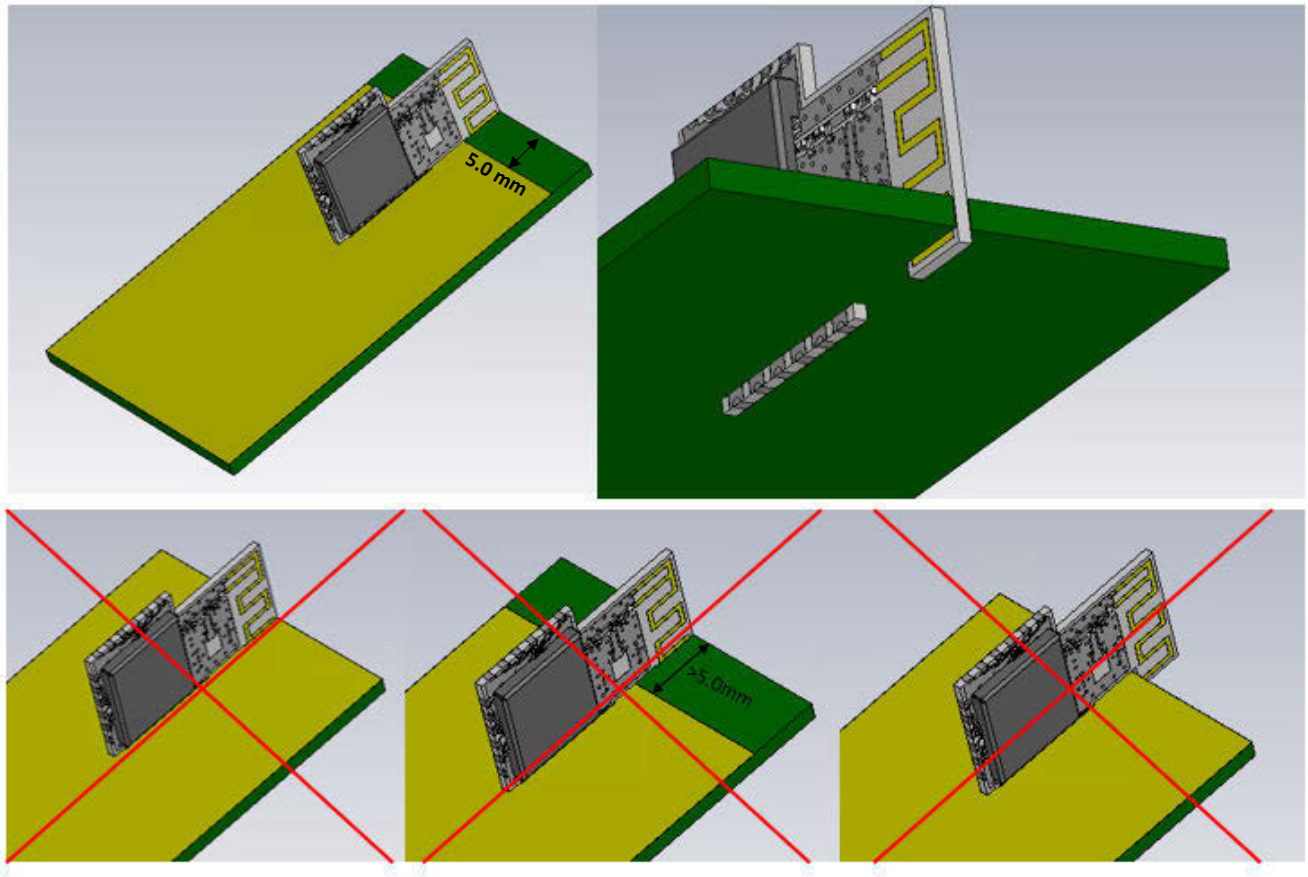
Horizontal Mounting illustrates the placement recommended when mounting the module horizontally to an end-application PCB. It also shows examples of layout cases that will result in severe RF performance degradation for the module.



Horizontal Mounting

Vertical mounting provides mechanical design flexibility that could be advantageous for certain applications. Vertical Mounting illustrates the placement recommended when mounting the module vertically to an end-application PCB. It also shows layout examples that will result in severe RF performance degradation for the module.

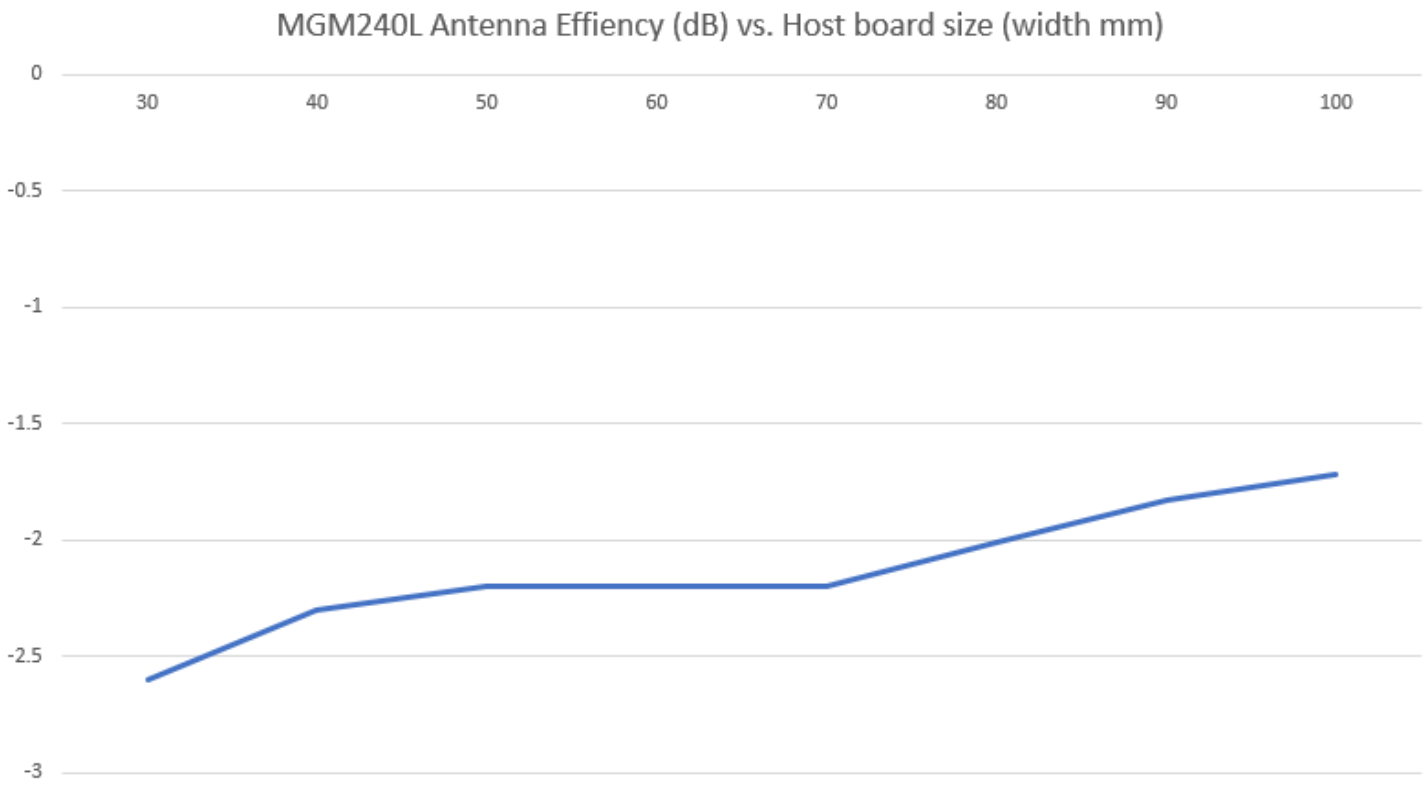
Notice that vertical mounting limits the number of pins available to interact with the module to six (VDD, GND and four GPIOs) which may be suitable for specific use cases only (e.g. to generate PWM outputs for LED control). The trade offs of vertical mounting should be carefully considered prior to choosing such arrangement.



Vertical Mounting

Antenna Optimization

Due to the nature of PCB trace antennas, the 030-00885 is sensitive to the thickness of the application PCB on which it is mounted, as well as to any plastics, metal or dielectric materials in close proximity to the antenna. The layout guide shown in Horizontal Mounting is optimal for an application board thickness of 0.8 mm. The figure below shows antenna efficiency vs. host board size.



Antenna Efficiency vs. Host Board Size

For cases where the application board is of a thickness different than the optimal, the impedance and performance of the antenna may be experimentally adjusted by

1. Cutting out the end-application PCB's FR4 material that is under the antenna, or by
2. Adjusting the separation between the lower side of the antenna and the edge of the application board's GND plane underneath the module

Impedance and performance optimization can be verified by measuring RSSI or radiated output power until either is maximized.

Reset

The 030-00885 can be reset by pulling the RESET line low, by the internal watchdog timer, or by software command. All three methods are applicable when the module is mounted horizontally on a given end-application board and, hence, all module pins are accessible. When mounted vertically, however, only the second and third methods apply.

The reset state does not provide power saving functionality and it is not recommended as a means to conserve power.

Debug

The 030-00885 supports hardware debugging via 4-pin JTAG or 2-pin serial-wire debug (SWD) interfaces. It is recommended to expose the debug pins in your own hardware design for firmware update and debug purposes.

If JTAG interfacing is enabled, the module must be power cycled to return to a SWD debug configuration if necessary.

Debug Pins

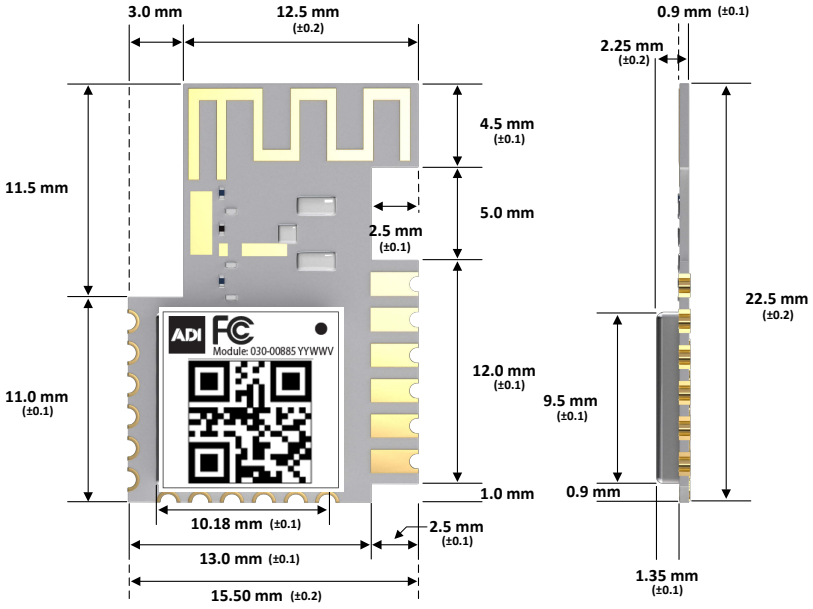
Pin Name	Pin Number	JTAG Signal	SWD Signal	Comments
PA04	4	TDI	N/A	This pin is disabled after reset. Once enabled the pin has a built-in pull-up.
PA03	3	TDO	N/A	This pin is disabled after reset.
PA02	2	TMS	SWDIO	Pin is enabled after reset and has a built-in pull-up.
PA01	1	TCK	SWCLK	Pin is enabled after reset and has a built-in pull-down.

Packet Trace Interface (PTI)

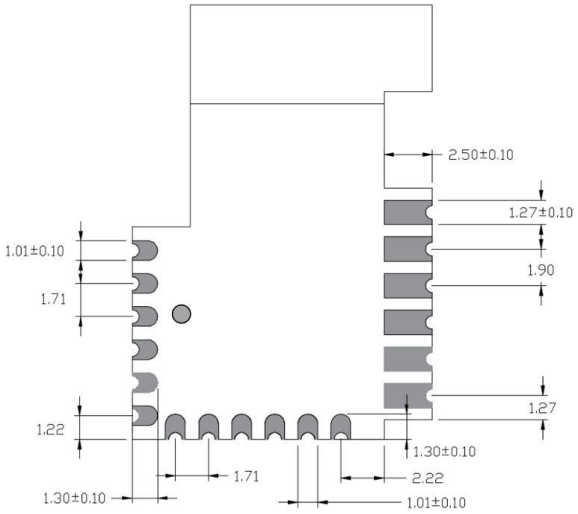
The 030-00885 integrates a true PHY-level packet trace interface (PTI) peripheral that can capture packets non-intrusively to monitor and log device and network traffic without burdening processing resources in the module's SoC. The PTI generates two output signals that can serve as a powerful debugging tool, especially in conjunction with other hardware and software development tools available from Silicon Labs. The PTI_DATA and PTI_SYNC signals can be accessed through any GPIO on ports C and D.

Package Specifications

Package Outline



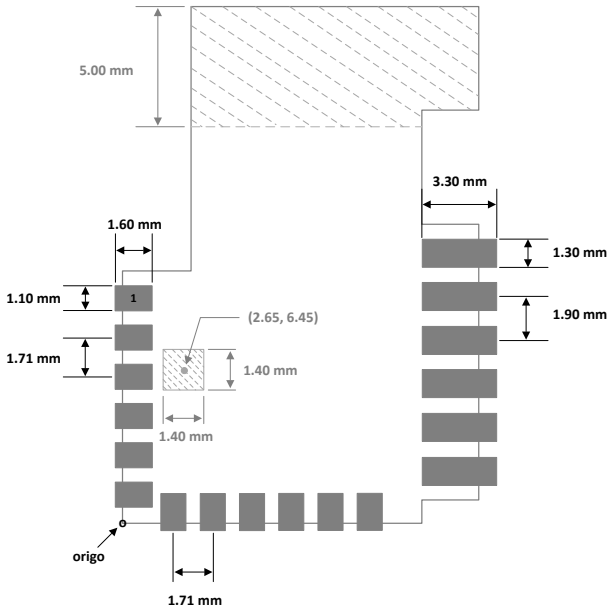
Top and Side Views



Bottom View

NOTE: Solder paste thickness adds 0.1 ± 0.05 mm to overall module height

PCB Land Pattern



Recommended Module PCB Land Pattern

Pad Sizing and Location

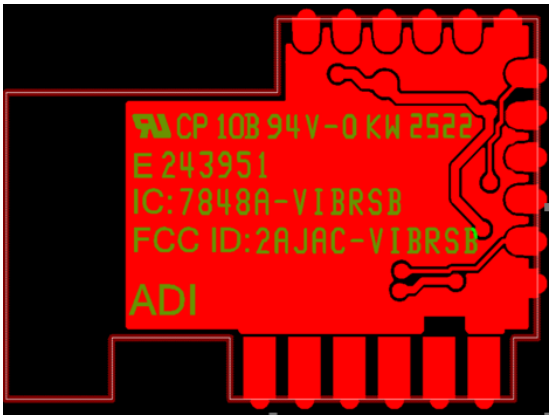
Pad Number	X Coordinate	Y Coordinate	Pad Dimensions
1	0.5	9.78	1.1 x 1.6
6	0.5	1.23	1.1 x 1.6
7	2.23	0.5	1.1 x 1.6
12	10.78	0.5	1.1 x 1.6
13	14.67	2.25	1.3 x 3.3
18	14.67	11.75	1.3 x 3.3

Note:

1. All dimensions in mm unless otherwise stated.
2. X and Y coordinates are specified relative to origo at indicated package corner in the figure above.
3. The module has a test point for VDD on the bottom layer at (X=2.65, Y=6.45). A keep-out area of 1.4 mm x 1.4 mm around this point is recommended to prevent the possibility of a short circuit.

Marking

The figure below shows the module markings engraved on the RF shield and the back of the PCB.



Mark Description

The package marking consists of:

- Module: 030-00885 - Part number/Model number designation
- QR Code: YYWWV
  - YY – Last two digits of the assembly year.
  - WW – Two-digit workweek when the device was assembled.
  - V – Version.
- Certification-related information (such as the FCC and etc.) is being engraved on the grayed out area, or printed on the back side of the module (silkscreen), according to regulatory body requirements.

Soldering Recommendations

It is recommended that final PCB assembly of the 030-00885 follows the industry standard as identified by the Institute for Printed Circuits (IPC). This product is assembled in compliance with the J-STD-001 requirements and the guidelines of IPC-AJ-820. Surface mounting of this product by the end user is recommended to follow IPC-A-610 to meet or exceed class 2 requirements.

CLASS 1 General Electronic Products

Includes products suitable for applications where the major requirement is function of the completed assembly.

CLASS 2 Dedicated Service Electronic Products

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically the end-use environment would not cause failures.

CLASS 3 High Performance/Harsh Environment Electronic Products

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

Certifications

This section details the certification status of the module with regards to regional regulatory radio approvals. Where applicable, the status with the industrial qualifications against the specifications of the supported wireless standards is given too.

The address of the module manufacturer (technology owner) and certification applicant is:

Snap One LLC.
1355 W Innovation Way Suite 125
Lehi, UT | 84043

The 030-00885 modules have brand name of “ADI”.

FCC - USA

This device complies with FCC's e-CFR Title 47, Part 15, Subpart C, Section 15.247 (and related relevant parts of the ANSI C63.10 standard) when operating with the built-in integral antenna.

Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

OEM Responsibilities to comply with FCC Regulations

This module has been tested for compliance to FCC Part 15.

OEM integrators are responsible for testing their end-product for any additional compliance requirements needed with this module installed (for example, digital device emissions, PC peripheral requirements, etc.). Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. (Part 15.21 in 47 CFR)

End Product Labeling

The 030-00885 modules are labeled with their own FCC ID. In all those cases when the FCC ID is not visible after the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final product must be labeled in a visible area with the following:

"Contains Transmitter Module FCC ID: 2AJAC-VIBRSB"

or

"Contains FCC ID: 2AJAC-VIBRSB"

Final note: As long as all the conditions in this and all the above chapters are met, further RF testing of the transmitter will not be strictly required. However, still consider the good practice and the FCC strong recommendation to ensure the compliance of the host by spot-checking. Nevertheless, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements which might be mandatory with this module installed.

ISED - Canada

This radio transmitter (**IC: 7848A-VIBRSB**) has been approved by *Innovation, Science and Economic Development Canada (ISED Canada, formerly Industry Canada*) to operate with the built-in integral antenna.

This radio-equipped device complies with ISED's license-exempt RSS standards. Operation is subject to the following two conditions:

1. This device may not cause interference; and
2. This device must accept any interference, including interference that may cause undesired operation of the device

ISED - Canada (French)

Ce transmetteur radio (**IC : 7848A-VIBRSB**) a été approuvé par Innovation, Sciences et Développement économique Canada (ISDE Canada, anciennement Industrie Canada) pour fonctionner avec l’antenne intégrée.

Cet appareil équipé d’un émetteur radio est conforme aux normes RSS exemptes de licence d’ISDE. Son fonctionnement est soumis aux deux conditions suivantes :

1. Cet appareil ne doit pas provoquer d’interférences;
2. Cet appareil doit accepter toute interférence reçue, y compris celles pouvant provoquer un fonctionnement indésirable.

RF Exposure Statement

Exception from routine SAR evaluation limits are given in RSS-102 Issue 5.

The module meets the requirements for Mobile use cases when the minimum separation distance from the human body is 20 cm or greater, in accordance to the limit(s) exposed in the RF Exposure Analysis.

For Portable use cases, RF Exposure or SAR evaluation is not required when the separation distances from the human body are equal or above 15.0 mm in the case of 802.15.4, and 15.0 mm in the case of Bluetooth Low Energy.

If the separation distance from the human body is less than the values stated above, the OEM integrator is responsible for evaluat-ing the SAR with the end-product, or for the re-configuration of the radio module in the host in terms of lowering the max RF TX power and/or the duty-cycle. A permissive change would be required too, under the responsibility of the host manufacturer, following a Multiple Listing authorization by the original module's certificate holder.

OEM Responsibilities to comply with IC Regulations

The 030-00885 modules have been certified for integration into products only by OEM integrators under the following conditions:

- The antenna must be installed such that a minimum separation distance as stated above is maintained between the radiator (antenna) and all persons at all times.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

Important Note: In the event that the above conditions cannot be met, the final product will have to undergo additional testing to evaluate the RF Exposure, or go through some re-configuration of the max output power and/or duty-cycle in order for the ISED authorization to remain valid; a permissive change will have to be applied too**.** The RF Exposure evaluation (SAR, or possibly a re-configuration) is in the responsibility of the end-product's manufacturer, as well as the permissive change that can be carried out with the help of the customer's own Telecommunication Certification Body, following a Multiple Listing authorization by the module's original grant holder.

End Product Labeling

The 030-00885 modules are labeled with their own IC ID. In all those cases when the IC ID is not visible after a module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final product must be labeled in a visible area with the following:

“**Contains Transmitter Module IC: 2AJAC-VIBRSB**”

or

“**Contains IC: 2AJAC-VIBRSB”**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end-product.

As long as all the conditions above are met, further RF testing of the transmitter will not be required. However, the OEM integrators are still responsible for testing their end-products for the fulfillment of any additional compliance requirements (for example, digital device emissions, PC peripheral requirements, etc.)

Notice that the information that is contained in this document is referenced from the Silicon Labs MGM240L document, which the product was designed by Silicon Labs for ADI.