Zhejiang Topso Technology Co., Ltd.

A3-LYAA01 user Manual

FEATURES

External Memory Interface

- Integrated 4Mbit(or 512KByte) Flash on chip
- Power efficient using retention technology to avoid floating lines
- Flexible IO voltage

Power Management

- Power On reset control
- Internal 32K OSC for standby/ shutoff/ sleep
- Battery charger (from USB or AC charger) Integrated all internal voltages from VBAT
- Provide all LDOs for external components

User Interface

ADC serial interface Keypad

Connectivity

- USB 1.1 Device
- **UART** interface
- 1 SD controller
- I2C controller
- 12S controller
- General Purpose I/Os
- 1 GPADC, 10bits, 2 channels

Audio

- 1 channel voice ADC, 8kHz, 13 bits/sample for microphone
- Voice DAC, 8kHz, 13 bits/sample for receiver
- High fidelity Stereo DAC, up to 48kHz, 16 bits per sample
- Stereo analog audio line input

Debug

- Host debug interface allowing non intrusive in depth investigation
- GDB debugger
- Execution logger and profiling through debug
- High level text based debugging using Host debug or USB

FΜ

Integrated Broadcast FM tuner which can be tuned world-wide frequency band

Bluetooth

Integrated Bluetooth SoC complaint with 2.1 + EDR standard

GENERAL DESCRIPTION

A high performance, high integrated multi-media system-on-chip solution with Bluetooth connectivity.

RDA5851S is a high performance, highly integrated multi-media system-on-chip solution with bluetooth connectivity. This is a newer generation than 5851, which specialized in music and audio applications, such as bluetooth music boom box, bluetooth stereo headset, etc.

Integrating all essential electronic components, including baseband, bluetooth transceiver, power management, FM receiver onto a single system on chip, RDA5851S offers best in class bill of material, space requirement and cost/feature ratio for bluetooth music and audio application.

Built around a cost effective 32-bit XCPU RISC core running at up to 312MHz with 4k of Instruction cache and 4k of Data cache, RDA5851S offers plenty of processing power for multimedia applications. A high performance proprietary 16/32-bit digital signal processing engine can further improve overall performance and user experience when performing complex multimedia tasks.

It is also packed with impressive connectivity for easy scalability of the system, allowing glue less interfaces to SDMMC Memory Cards and USB (slave, full speed).

Additionally, RDA5851S integrates a FM tuner and a Bluetooth module which completely include digital, analogue and RF function. And they can easily work only with a few passive components as filter or matching network

RDA5851S is available in a small footprint, fine pitch, 6.5 X 6.5, 81 ball TFBGA package.

Voice Coprocessor (VoC)

The Voice Co-Processor (VoC) is designed to process different Vocoders (FR, HR, EFR, AMR)It is developed as a target-specific DSP core, including basic function-call support, able to execute the code with very little (or no) control intervention from the CPU. It is controlled and configured by the CPU through the AMBA bus.

Features

- Bi-MAC, single test/logic Computational Unit with two 16x16 -> 32-bit multipliers
- · Eight 16-bit general purpose registers, that can be combined in four 32-bit general purpose registers.
- · All 16-bit registers can be used as pointers, four of them are incremental (for easy array addressing).
- · Four 32-bit general purpose registers.
- 2 x 20 Kbytes data RAM + 32 Kbytes instruction RAM.
- . Double stack with random access: for 32-bit & 16-bit values (push, pop).
- · Function call support (jal, return).
- · Two zero-cycle loop counters.
- · Pointer & Direct addressing modes.
- DMA sub-module for block transfers between external memory and VoC memories.
- Simple DAI Interface for Analog test Audio Loop (Loop between DAI interface and Analog Interface designed to test the Audio Filters implemented by VoC)
- Clock speed: 26MHz, 39MHz, 52MHz, 78MHz, 89MHz, 104MHz, 113MHz, 125MHz, 139MHz, 156MHz, 178MHz, 208MHz, 250MHz, 312MHz.

SPI Interface for Analog IP control

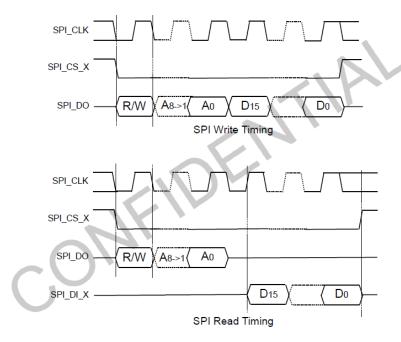
All the IPs connected to DBB feature an SPI interface dedicated to IP control.

The Power Management Unit(PMU) and the Analog module(ABB) are controlled by the same SPI of DBB (with different chip-select).

For simplicity sake and ease of use, the SPI protocol settings for PMU and ABB.

The chosen SPI setting is the following:

- Data from DBB are issued on falling edge of clock and can be latched on rising edge by the slave. Data from the slave are issued on rising edge of the clock and will be latched on falling edge of
- the SPI frame is 26 bits long: first bit is the R/W selection, then 9 bits of address A₈ to A₀, then 16 bits of data D₁₅ to D₀.
- Maximum SPI_CLK frequency: 26 MHz

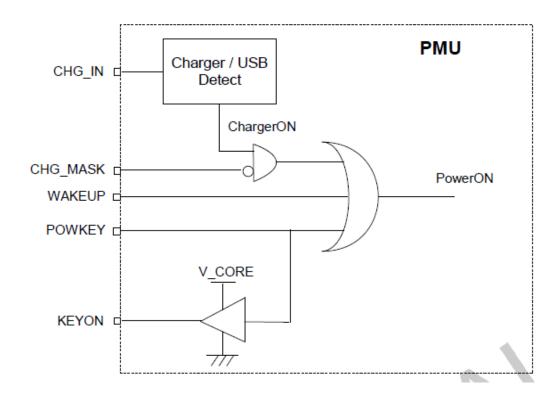


Power Management Unit

The PMU is controlled from the DBB through SPI.

Power System Management

The PMU performs a POR either when POWKEY is asserted (i.e. Power-ON/OFF button pressed) or when then WAKEUP line is raised (RTC Alarm) or when the charger (or USB) is plugged.



PMU Power ON

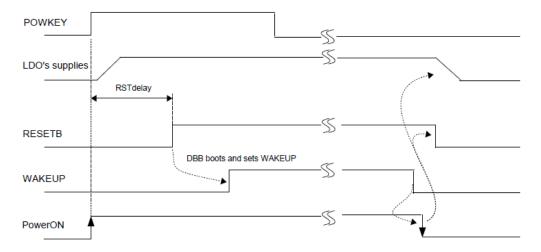
In the presented principle schematic, PowerON is an internal signal of the PMU that reflects that the system needs power. It can either be raised when the Power-ON key is pressed, when the WAKEUP line from DBB is raised or when the charger (or USB) is plugged. When a rising edge of PowerON is detected, the PMU should go through its POR sequence.

The POR sequence consists in turning ON the relevant power supplies then wait for RST delay that is be long enough to ensure that all LDOs are in steady state and that all the chip is correctly powered, then raise the RESETB signal.

In case the POR is trigged by POWKEY, It's DBB responsibility to set the WAKEUP line high when it considers that POWKEY has been pressed long enough. As POWKEY is a VBAT level input, a V_CORE version of POWKEY (named KEYON) is generated for DBB.

POR can also be initiated when the WAKEUP line is being raised directly because of an RTC Alarm (the POWKEY is not pressed).

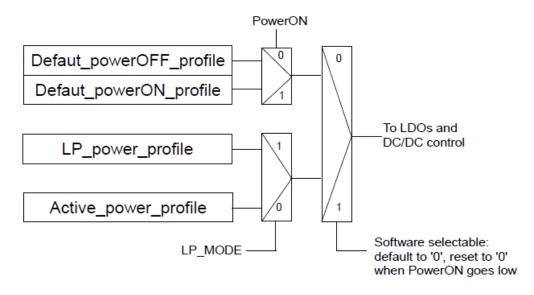
As long as PowerON is high, the PMU provides voltages supplies that are specified by the current Power-Profile that describes the LDO and DC/DC settings.



OR triggered by POWKEY press

The PMU implements multiple power profiles defining the LDOs and DC/DC activation in various modes.

- 1. Default_powerOFF_profile: used when the system is OFF(system has been shut-off or first time battery is plugged...). In this case only V_RTC is provided.
- 2. Default_powerON_profile: used when PowerON is asserted and the POR is trigged, all LDOs that have "reset state ON" are activated.
- 3. Active_power_profile: used once system has booted and decided to switch from Default_powerON_profile. This profile is programmable.
- 4. LP_power_profile: used when the system goes to low-power mode (switch from Active to Low-power through LP_MODE line). This profile is programmable.



Principle schematic for Power-Profiles usage

If the PowerON line goes low, the RESETB signal will be set to Low level then all power supplies excepted V_RTC are switched OFF

It can be useful to be able to go back to Default_powerOFF_profile (i.e. shut-off all supplies

except RTC) even when a charger is plugged. The CHG_MASK (RTC domain) line is used for this purpose, by masking the ChargerON line.

V_USB is not power-on automatically when USB is detected. The USB PHY remains OFF until the software decides to turn it ON.

LDOs

Name	Туре	Voltage	Max Current	Usage (power domain)
V_CORE	DC-DC	1.2V	300mA	Core
V_CORE	LDO	1.2V	20mA	Core
V_PAD	LDO	1.8V / 2.8V	200mA	Digital IO
V_ANA	LDO		200mA	Analog module
V_MEM	LDO	1.8V / 2.8V	200mA	External Combo flash / ram
V_SPIMEM	LDO	1.8V / 2.8V	200mA	External SPI Memory
V_MMC	LDO	2.8V / 3.2V	150mA	Memory Card
V_USB	LDO	3.3V	300mA	USB PHY
V_MIC	LDO	1.4V/1.75V	200mA	Microphone
V_RTC	LDO	1.2V	0.6mA	Real time clock

AUDIO

The Audio part includes ADC, DAC, Audio Amplifiers and Audio Muxes. The following diagram provides a global view of audio blocks. Voice data can be input from microphone. Voice and audio data can be output to a stereo DAC and connected to peripherals such as receiver, headset and loudspeaker. It is able to support multiple sample rate audio data including 8 kHz, 11.025 kHz, 12kHz, 16 kHz, 22,05 kHz, 24kHz, 32kHz, 44,1 kHz, 48kHz.

General Description

RDA5851S Integrates a broadcast FM stereo radio tuner with fully integrated synthesizer, IF selectivity and MPX decoder. The tuner requires the least external component. It has a powerful low-IF digital audio processor, this make it have optimum sound quality with varying reception conditions. It can be tuned to the worldwide frequency band.

Features

- Low Power Consumption
 - Total Current consumption Lower than 22 mA at 3.0 V power supply
- Support worldwide frequency band
 - ➤ 65-108MHz
- Digital low-IF tuner
 - Image-reject down-converter
 - High performance A/D converter
 - IF selectivity performed internally
- Fully integrated digital frequency synthesizer
 - > Fully integrated on-chip RF and IF VCO
 - Fully integrated on-chip loop filter
- Autonomous search tuning
- Support 32.768KHz crystal oscillator
- Digital auto gain control (AGC)
- Digital adaptive noise cancellation
 - Mono/stereo switch
 - Soft mute
 - High cut
- Programmable de-emphasis (50/75 ms)
- Receive signal strength indicator (RSSI)
- Bass boost
- Volume control
- FM Record through digital audio interface
- Line-level analog output voltage
- 32.768 KHz 12M,24M,13M,26M,19.2M,38.4MHz Reference Clock
- SPI control bus interface
- Directly support 32Ω resistance loading

Bluetooth:

General DescriptionRDA5851S Integrates a highly integrated Bluetooth SoC with radio transceiver and baseband processor, which is compliant with Bluetooth 2.1 + EDR specification and provides an optimal solution for data and voice application. It has been designed on highest level of integration to extremely reduce the number of external component.

Features

- CMOS single-chip fully-integrated radio and baseband
- Compliant with Bluetooth 2.1 + EDR specification
- Bluetooth Piconet and Scatternet support
- Support AFH
- Meet class1, class2 and class3 transmitting power requirement
- Provides +4dbm transmitting power
- NZIF receiver with -90dBm sensitivity
- Up to 4Mbps high speed UART HCI support
- Low power consumption
- Minimum external component

FCC Statement

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception,

- —Reorient or relocate the receiving antenna.
- —Increase the separation between the equipment and receiver.
- —Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- —Consult the dealer or an experienced radio/TV technician for help.

FCC RF Radiation Exposure Statement

This equipment complies with FCC RF radiation exposure limits set forth for an uncontrolled environment.