Technical Description

The brief circuit description is listed as below:

1) **U1 acts as a Bluetooth Module (NRF51822).**
2) **U2 acts as a 24-Bits ADC (HY3116).**
3) **U3 acts as a LDO Regulator (RT9193).**
4) **MFRC522 acts as a NFC Reader.**
5) **X1 acts as a Crystal for U1.**
6) **X2 acts as a Crystal for NFC Reader.**

NFC Reader:
Antenna Type: Internal antenna
Antenna Gain: 0dBi
Nominal rated field strength: 59.7 dBμV/m at 3m
Maximum allowed field strength of production tolerance: +/- 3dB

Bluetooth Module:
Antenna Type: Internal antenna
Antenna Gain: 0dBi
Nominal rated field strength: 87.2 dBμV/m at 3m
Maximum allowed field strength of production tolerance: +/- 3dB

MFRC522

Contactless reader IC

Rev. 3.3 — 26 October 2009
112133

Product data sheet
PUBLIC

1. Introduction

This document describes the functionality and electrical specifications of the contactless reader/writer MFRC522.

2. General description

The MFRC522 is a highly integrated reader/writer IC for contactless communication at 13.56 MHz. The MFRC522 reader supports ISO/IEC 14443 A/MIFARE mode.

The MFRC522's internal transmitter is able to drive a reader/writer antenna designed to communicate with ISO/IEC 14443 A/MIFARE cards and transponders without additional active circuitry. The receiver module provides a robust and efficient implementation for demodulating and decoding signals from ISO/IEC 14443 A/MIFARE compatible cards and transponders. The digital module manages the complete ISO/IEC 14443 A framing and error detection (parity and CRC) functionality.

The MFRC522 supports MF1xxS20, MF1xxS70 and MF1xxS50 products. The MFRC522 supports contactless communication and uses MIFARE higher transfer speeds up to 848 kBd in both directions.

The following host interfaces are provided:

- Serial Peripheral Interface (SPI)
- Serial UART (similar to RS232 with voltage levels dependant on pin voltage supply)
- I^2C-bus interface

3. Features

- Highly integrated analog circuitry to demodulate and decode responses
- Buffered output drivers for connecting an antenna with the minimum number of external components
- Supports ISO/IEC 14443 A/MIFARE
- Typical operating distance in Read/Write mode up to 50 mm depending on the antenna size and tuning
- Supports MF1xxS20, MF1xxS70 and MF1xxS50 encryption in Read/Write mode
- Supports ISO/IEC 14443 A higher transfer speed communication up to 848 kBd
- Supports MFIN/MFOUT
- Additional internal power supply to the smart card IC connected via MFIN/MFOUT
- Supported host interfaces

- SPI up to 10 Mbit/s
- I^2C-bus interface up to 400 kBd in Fast mode, up to 3400 kBd in High-speed mode
- RS232 Serial UART up to 1228.8 kBd, with voltage levels dependant on pin voltage supply

- FIFO buffer handles 64 byte send and receive
- Flexible interrupt modes
- Hard reset with low power function
- Power-down by software mode
- Programmable timer
- Internal oscillator for connection to 27.12 MHz quartz crystal
- 2.5 V to 3.3 V power supply
- CRC coprocessor
- Programmable I/O pins
- Internal self-test

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	analog supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
V_{DDD}	digital supply voltage			2.5	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage			2.5	3.3	3.6	V
$V_{DD(PVDD)}$	PVDD supply voltage		[3]	1.6	1.8	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V		1.6	-	3.6	V
I_{pd}	power-down current	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)} = 3$ V					
		hard power-down; pin NRSTPD set LOW	[4]	-	-	5	µA
		soft power-down; RF level detector on	[4]	-	-	10	µA
I_{DDD}	digital supply current	pin DVDD; $V_{DDD} = 3$ V		-	6.5	9	mA
I_{DDA}	analog supply current	pin AVDD; $V_{DDA} = 3$ V, CommandReg register's RcvOff bit = 0		-	7	10	mA
		pin AVDD; receiver switched off; $V_{DDA} = 3$ V, CommandReg register's RcvOff bit = 1		-	3	5	mA
$I_{DD(PVDD)}$	PVDD supply current	pin PVDD	[5]	-	-	40	mA
$I_{DD(TVDD)}$	TVDD supply current	pin TVDD; continuous wave	[6][7][8]	-	60	100	mA
T_{amb}	ambient temperature	HVQFN32		–25	-	+85	°C

[1] Supply voltages below 3 V reduce the performance in, for example, the achievable operating distance.

[2] V_{DDA}, V_{DDD} and $V_{DD(TVDD)}$ must always be the same voltage.

[3] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DDD}.

[4] I_{pd} is the total current for all supplies.

[5] $I_{DD(PVDD)}$ depends on the overall load at the digital pins.

[6] $I_{DD(TVDD)}$ depends on $V_{DD(TVDD)}$ and the external circuit connected to pins TX1 and TX2.

[7] During typical circuit operation, the overall current is below 100 mA.

[8] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
MFRC52201HN1/TRAYB[1]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1
MFRC52201HN1/TRAYBM[2]	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminal; body 5 × 5 × 0.85 mm	SOT617-1

[1] Delivered in one tray.

[2] Delivered in five trays.

6. Block diagram

The analog interface handles the modulation and demodulation of the analog signals.

The contactless UART manages the protocol requirements for the communication protocols in cooperation with the host. The FIFO buffer ensures fast and convenient data transfer to and from the host and the contactless UART and vice versa.

Various host interfaces are implemented to meet different customer requirements.

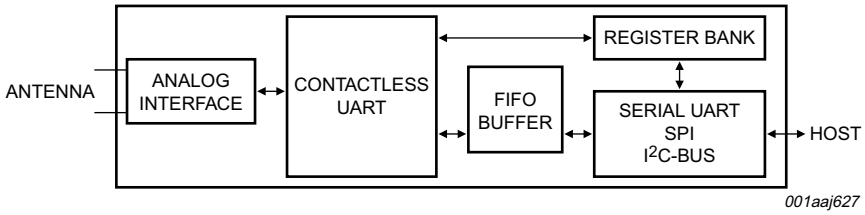


Fig 1. Simplified block diagram of the MFRC522

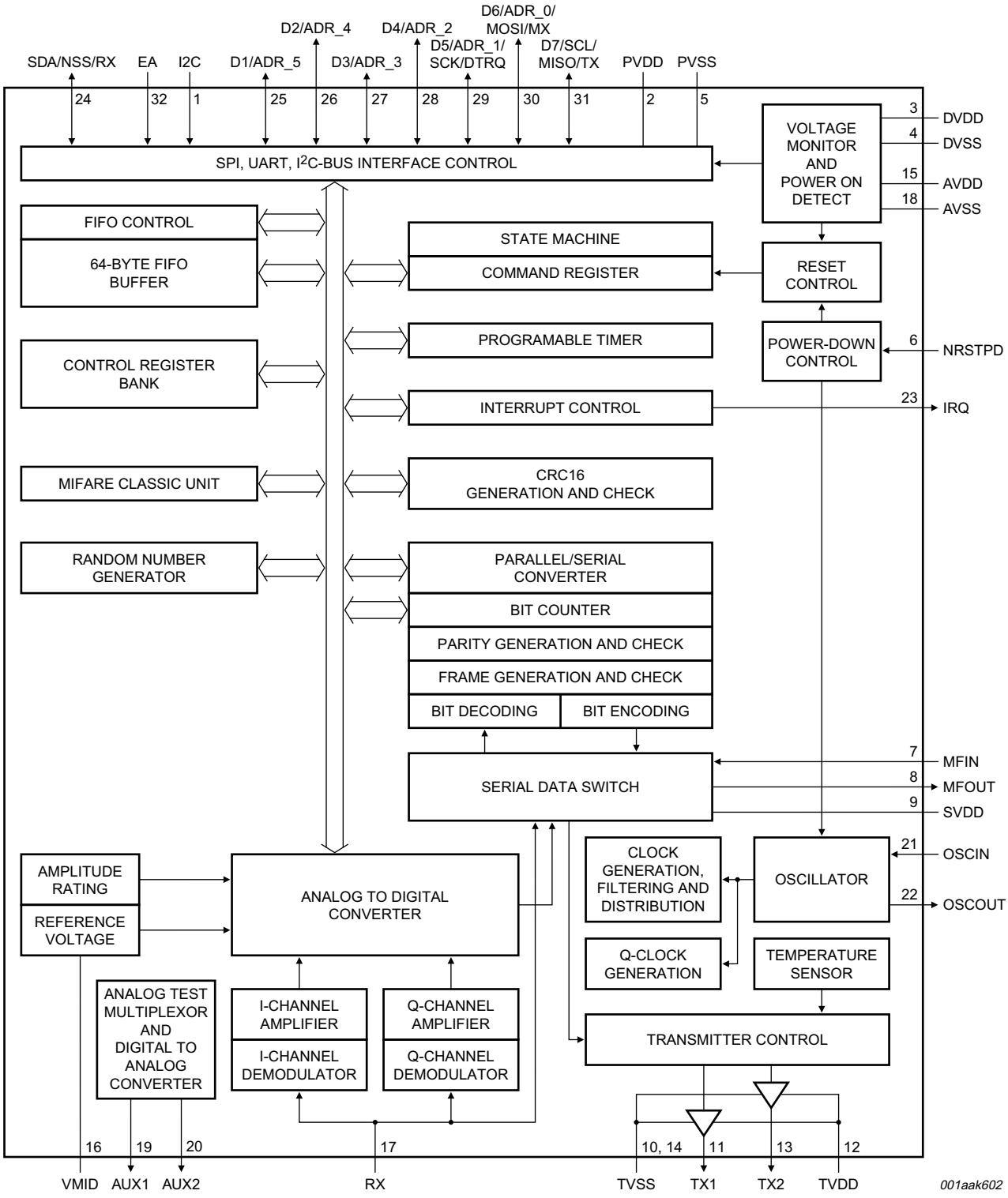


Fig 2. Detailed block diagram of the MFRC522

7. Pinning information

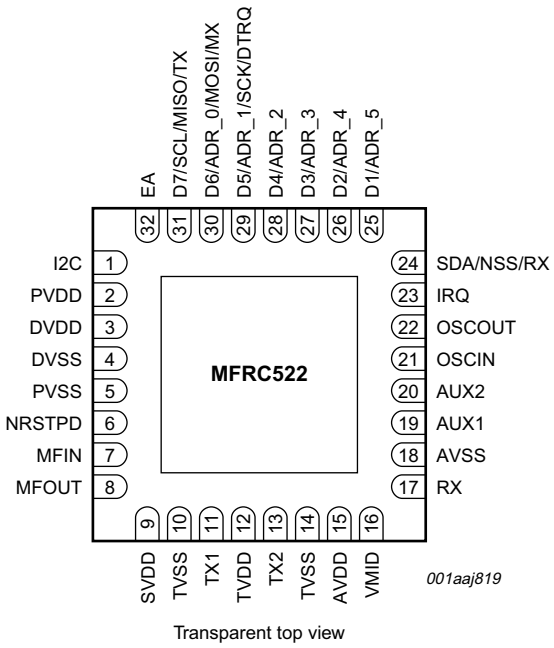


Fig 3. Pinning configuration HVQFN32 (SOT617-1)

7.1 Pin description

Table 3. Pin description

Pin	Symbol	Type[1]	Description
1	I2C	I	I^2C-bus enable input[2]
2	PVDD	P	pin power supply
3	DVDD	P	digital power supply
4	DVSS	G	digital ground[3]
5	PVSS	G	pin power supply ground
6	NRSTPD	I	reset and power-down input: power-down: enabled when LOW; internal current sinks are switched off, the oscillator is inhibited and the input pins are disconnected from the outside world reset: enabled by a positive edge
7	MFIN	I	MIFARE signal input
8	MFOUT	O	MIFARE signal output
9	SVDD	P	MFIN and MFOUT pin power supply
10	TVSS	G	transmitter output stage 1 ground
11	TX1	O	transmitter 1 modulated 13.56 MHz energy carrier output
12	TVDD	P	transmitter power supply: supplies the output stage of transmitters 1 and 2
13	TX2	O	transmitter 2 modulated 13.56 MHz energy carrier output
14	TVSS	G	transmitter output stage 2 ground
15	AVDD	P	analog power supply

Table 3. Pin description *...continued*

Pin	Symbol	Type[1]	Description
16	VMID	P	internal reference voltage
17	RX	I	RF signal input
18	AVSS	G	analog ground
19	AUX1	O	auxiliary outputs for test purposes
20	AUX2	O	auxiliary outputs for test purposes
21	OSCIN	I	crystal oscillator inverting amplifier input; also the input for an externally generated clock (f_{clk} = 27.12 MHz)
22	OSCOUT	O	crystal oscillator inverting amplifier output
23	IRQ	O	interrupt request output: indicates an interrupt event
24	SDA	I/O	I^2C-bus serial data line input/output[2]
	NSS	I	SPI signal input[2]
	RX	I	UART address input[2]
25	D1	I/O	test port[2]
	ADR_5	I/O	I^2C-bus address 5 input[2]
26	D2	I/O	test port
	ADR_4	I	I^2C-bus address 4 input[2]
27	D3	I/O	test port
	ADR_3	I	I^2C-bus address 3 input[2]
28	D4	I/O	test port
	ADR_2	I	I^2C-bus address 2 input[2]
29	D5	I/O	test port
	ADR_1	I	I^2C-bus address 1 input[2]
	SCK	I	SPI serial clock input[2]
	DTRQ	O	UART request to send output to microcontroller[2]
30	D6	I/O	test port
	ADR_0	I	I^2C-bus address 0 input[2]
	MOSI	I/O	SPI master out, slave in[2]
	MX	O	UART output to microcontroller[2]
31	D7	I/O	test port
	SCL	I/O	I^2C-bus clock input/output[2]
	MISO	I/O	SPI master in, slave out[2]
	TX	O	UART data output to microcontroller[2]
32	EA	I	external address input for coding I^2C-bus address[2]

[1] Pin types: I = Input, O = Output, I/O = Input/Output, P = Power and G = Ground.

[2] The pin functionality of these pins is explained in Section 8.1 “Digital interfaces”.

[3] Connection of heatsink pad on package bottom side is not necessary. Optional connection to pin DVSS is possible.

8. Functional description

The MFRC522 transmission module supports the Read/Write mode for ISO/IEC 14443 A/MIFARE using various transfer speeds and modulation protocols.

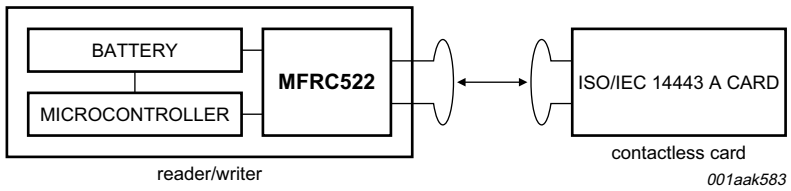
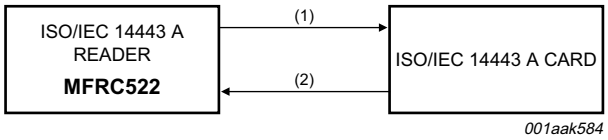


Fig 4. MFRC522 Read/Write mode

The physical level communication is shown in Figure 5.



(1) Reader to card 100 % ASK, Miller encoded, transfer speed 106 kBd to 848 kBd.

(2) Card to reader subcarrier load modulation, Manchester encoded or BPSK, transfer speed 106 kBd to 848 kBd.

Fig 5. ISO/IEC 14443 A/MIFARE Read/Write mode communication diagram

The physical parameters are described in Table 4.

Table 4. Communication overview for ISO/IEC 14443 A/MIFARE reader/writer

Communication direction	Signal type	Transfer speed			
		106 kBd	212 kBd	424 kBd	848 kBd
Reader to card (send data from the MFRC522 to a card)	reader side modulation	100 % ASK	100 % ASK	100 % ASK	100 % ASK
	bit encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding	modified Miller encoding
	bit length	128 (13.56 µs)	64 (13.56 µs)	32 (13.56 µs)	16 (13.56 µs)
Card to reader (MFRC522 receives data from a card)	card side modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation	subcarrier load modulation
	subcarrier frequency	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16	13.56 MHz/16
	bit encoding	Manchester encoding	BPSK	BPSK	BPSK

The MFRC522's contactless UART and dedicated external host must manage the complete ISO/IEC 14443 A/MIFARE protocol. Figure 6 shows the data coding and framing according to ISO/IEC 14443 A/MIFARE.

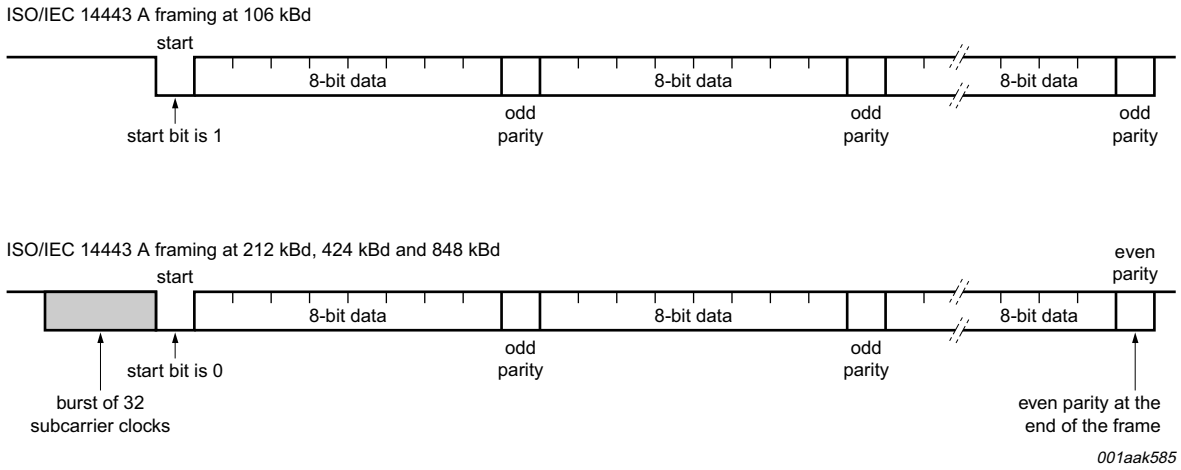


Fig 6. Data coding and framing according to ISO/IEC 14443 A

The internal CRC coprocessor calculates the CRC value based on ISO/IEC 14443 A part 3 and handles parity generation internally according to the transfer speed. Automatic parity generation can be switched off using the MfRxReg register's ParityDisable bit.

8.1 Digital interfaces

8.1.1 Automatic microcontroller interface detection

The MFRC522 supports direct interfacing of hosts using SPI, I^2C-bus or serial UART interfaces. The MFRC522 resets its interface and checks the current host interface type automatically after performing a power-on or hard reset. The MFRC522 identifies the host interface by sensing the logic levels on the control pins after the reset phase. This is done using a combination of fixed pin connections. Table 5 shows the different connection configurations.

Table 5. Connection protocol for detecting different interface types

Pin	Interface type		
	UART (input)	SPI (output)	I^2C-bus (I/O)
SDA	RX	NSS	SDA
I2C	0	0	1
EA	0	1	EA
D7	TX	MISO	SCL
D6	MX	MOSI	ADR_0
D5	DTRQ	SCK	ADR_1
D4	-	-	ADR_2
D3	-	-	ADR_3
D2	-	-	ADR_4
D1	-	-	ADR_5

8.1.2 Serial Peripheral Interface

A serial peripheral interface (SPI compatible) is supported to enable high-speed communication to the host. The interface can handle data speeds up to 10 Mbit/s. When communicating with a host, the MFRC522 acts as a slave, receiving data from the external host for register settings, sending and receiving data relevant for RF interface communication.

An interface compatible with SPI enables high-speed serial communication between the MFRC522 and a microcontroller. The implemented interface is in accordance with the SPI standard.

The timing specification is given in Section 14.1 on page 75.

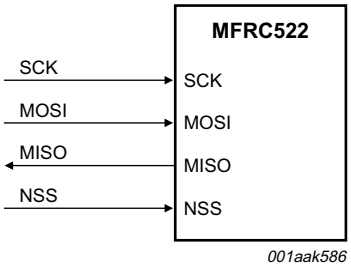


Fig 7. SPI connection to host

The MFRC522 acts as a slave during SPI communication. The SPI clock signal SCK must be generated by the master. Data communication from the master to the slave uses the MOSI line. The MISO line is used to send data from the MFRC522 to the master.

Data bytes on both MOSI and MISO lines are sent with the MSB first. Data on both MOSI and MISO lines must be stable on the rising edge of the clock and can be changed on the falling edge. Data is provided by the MFRC522 on the falling clock edge and is stable during the rising clock edge.

8.1.2.1 SPI read data

Reading data using SPI requires the byte order shown in Table 6 to be used. It is possible to read out up to n-data bytes.

The first byte sent defines both the mode and the address.

Table 6. MOSI and MISO byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	address 1	address 2	...	address n	00
MISO	X[1]	data 0	data 1	...	data n – 1	data n

[1] X = Do not care.

Remark: The MSB must be sent first.

8.1.2.2 SPI write data

To write data to the MFRC522 using SPI requires the byte order shown in Table 7. It is possible to write up to n data bytes by only sending one address byte.

The first send byte defines both the mode and the address byte.

Table 7. MOSI and MISO byte order

Line	Byte 0	Byte 1	Byte 2	To	Byte n	Byte n + 1
MOSI	address 0	data 0	data 1	...	data n – 1	data n
MISO	X[1]	X[1]	X[1]	...	X[1]	X[1]

[1] X = Do not care.

Remark: The MSB must be sent first.

8.1.2.3 SPI address byte

The address byte must meet the following format.

The MSB of the first byte defines the mode used. To read data from the MFRC522 the MSB is set to logic 1. To write data to the MFRC522 the MSB must be set to logic 0. Bits 6 to 1 define the address and the LSB is set to logic 0.

Table 8. Address byte 0 register; address MOSI

7 (MSB)	6	5	4	3	2	1	0 (LSB)
1 = read 0 = write	address						0

8.1.3 UART interface

8.1.3.1 Connection to a host

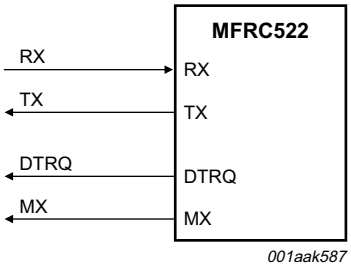


Fig 8. UART connection to microcontrollers

Remark: Signals DTRQ and MX can be disabled by clearing TestPinEnReg register's RS232LineEn bit.

8.1.3.2 Selectable UART transfer speeds

The internal UART interface is compatible with an RS232 serial interface.

The default transfer speed is 9.6 kBd. To change the transfer speed, the host controller must write a value for the new transfer speed to the SerialSpeedReg register. Bits BR_T0[2:0] and BR_T1[4:0] define the factors for setting the transfer speed in the SerialSpeedReg register.

The BR_T0[2:0] and BR_T1[4:0] settings are described in Table 9. Examples of different transfer speeds and the relevant register settings are given in Table 10.

Table 9. BR_T0 and BR_T1 settings

BR_Tn	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
BR_T0 factor	1	1	2	4	8	16	32	64
BR_T1 range	1 to 32	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64	33 to 64

Table 10. Selectable UART transfer speeds

Transfer speed (kBd)	SerialSpeedReg value		Transfer speed accuracy (%)[1]
	Decimal	Hexadecimal	
7.2	250	FAh	–0.25
9.6	235	EBh	0.32
14.4	218	DAh	–0.25
19.2	203	CBh	0.32
38.4	171	ABh	0.32
57.6	154	9Ah	–0.25
115.2	122	7Ah	–0.25
128	116	74h	–0.06
230.4	90	5Ah	–0.25
460.8	58	3Ah	–0.25
921.6	28	1Ch	1.45
1228.8	21	15h	0.32

[1] The resulting transfer speed error is less than 1.5 % for all described transfer speeds.

The selectable transfer speeds shown in Table 10 are calculated according to the following equations:

If BR_T0[2:0] = 0:

$$transfer\ speed = \frac{27.12 \times 10^6}{(BR\_T0 + 1)} \quad (1)$$

If BR_T0[2:0] > 0:

$$transfer\ speed = \left(\frac{27.12 \times 10^6}{\frac{(BR\_T1 + 33)}{2^{(BR\_T0 - 1)}}} \right) \quad (2)$$

Remark: Transfer speeds above 1228.8 kBd are not supported.

8.1.3.3 UART framing

Table 11. UART framing

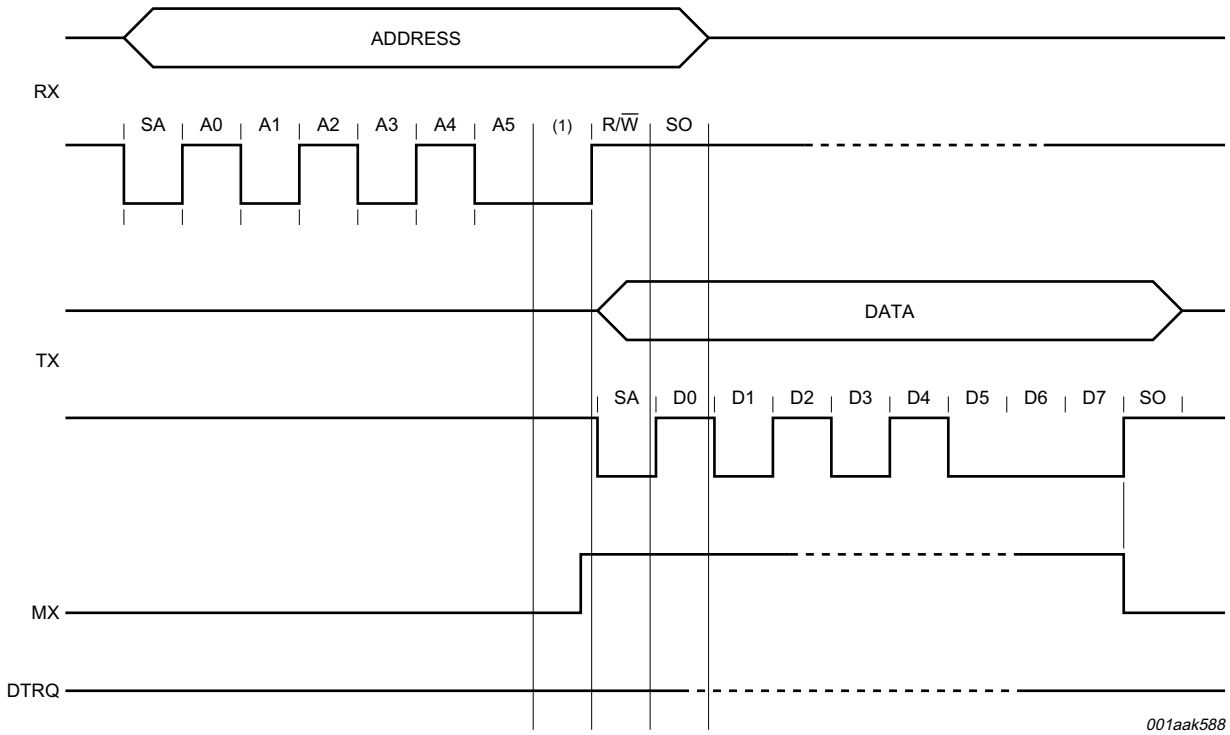
Bit	Length	Value
Start	1-bit	0
Data	8 bits	data
Stop	1-bit	1

Remark: The LSB for data and address bytes must be sent first. No parity bit is used during transmission.

Read data: To read data using the UART interface, the flow shown in Table 12 must be used. The first byte sent defines both the mode and the address.

Table 12. Read data byte order

Pin	Byte 0	Byte 1
RX (pin 24)	address	-
TX (pin 31)	-	data 0



(1) Reserved.

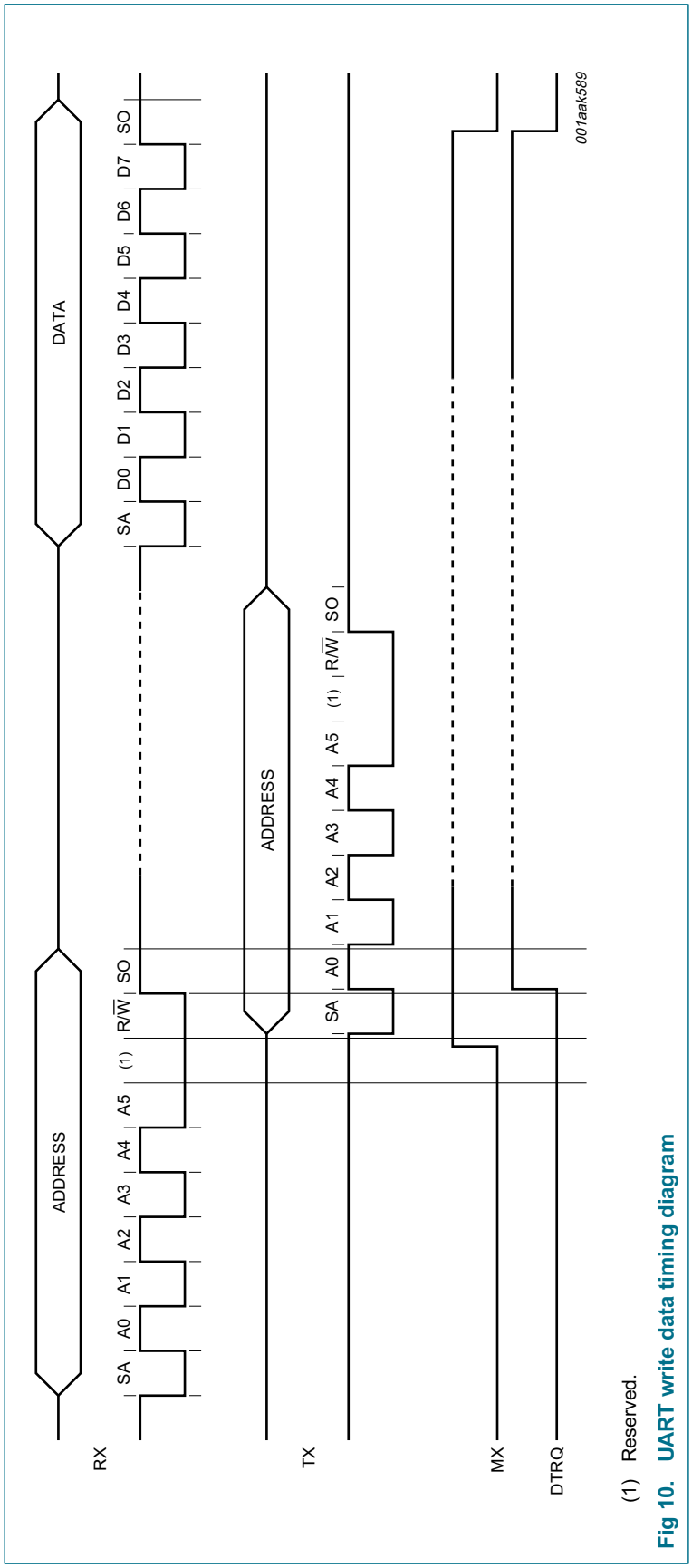
Fig 9. UART read data timing diagram

Write data: To write data to the MFRC522 using the UART interface, the structure shown in Table 13 must be used.

The first byte sent defines both the mode and the address.

Table 13. Write data byte order

Pin	Byte 0	Byte 1
RX (pin 24)	address 0	data 0
TX (pin 31)	-	address 0



(1) Reserved.

Fig 10. UART write data timing diagram

Remark: The data byte can be sent directly after the address byte on pin RX.

Address byte: The address byte has to meet the following format:

The MSB of the first byte sets the mode used. To read data from the MFRC522, the MSB is set to logic 1. To write data to the MFRC522 the MSB is set to logic 0. Bit 6 is reserved for future use, and bits 5 to 0 define the address; see Table 14.

Table 14. Address byte 0 register; address MOSI

7 (MSB)	6	5	4	3	2	1	0 (LSB)
1 = read 0 = write	reserved	address					

8.1.4 I²C-bus interface

An I²C-bus (Inter-IC) interface is supported to enable a low-cost, low pin count serial bus interface to the host. The I²C-bus interface is implemented according to NXP Semiconductors' *I²C-bus interface specification, rev. 2.1, January 2000*. The interface can only act in Slave mode. Therefore the MFRC522 does not implement clock generation or access arbitration.

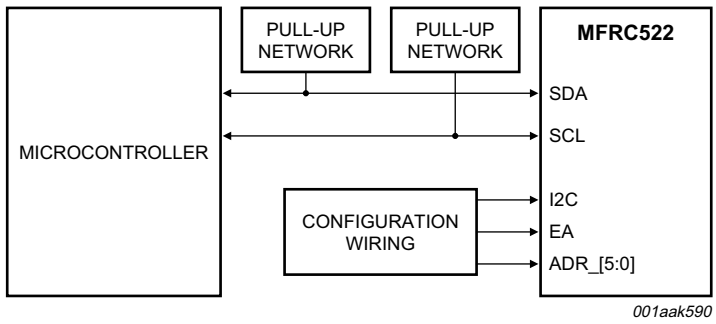


Fig 11. I²C-bus interface

The MFRC522 can act either as a slave receiver or slave transmitter in Standard mode, Fast mode and High-speed mode.

SDA is a bidirectional line connected to a positive supply voltage using a current source or a pull-up resistor. Both SDA and SCL lines are set HIGH when data is not transmitted. The MFRC522 has a 3-state output stage to perform the wired-AND function. Data on the I²C-bus can be transferred at data rates of up to 100 kBd in Standard mode, up to 400 kBd in Fast mode or up to 3.4 Mbit/s in High-speed mode.

If the I²C-bus interface is selected, spike suppression is activated on lines SCL and SDA as defined in the I²C-bus interface specification.

See Table 155 on page 76 for timing requirements.

8.1.4.1 Data validity

Data on the SDA line must be stable during the HIGH clock period. The HIGH or LOW state of the data line must only change when the clock signal on SCL is LOW.

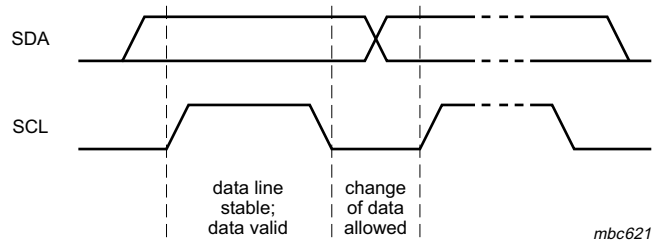


Fig 12. Bit transfer on the I²C-bus

8.1.4.2 START and STOP conditions

To manage the data transfer on the I²C-bus, unique START (S) and STOP (P) conditions are defined.

- A START condition is defined with a HIGH-to-LOW transition on the SDA line while SCL is HIGH.
- A STOP condition is defined with a LOW-to-HIGH transition on the SDA line while SCL is HIGH.

The I²C-bus master always generates the START and STOP conditions. The bus is busy after the START condition. The bus is free again a certain time after the STOP condition.

The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. The START (S) and repeated START (Sr) conditions are functionally identical. Therefore, S is used as a generic term to represent both the START (S) and repeated START (Sr) conditions.

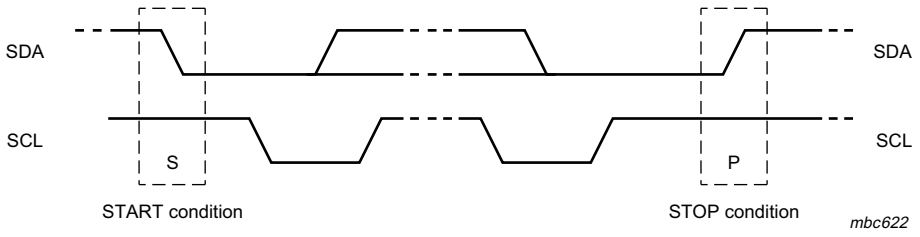


Fig 13. START and STOP conditions

8.1.4.3 Byte format

Each byte must be followed by an acknowledge bit. Data is transferred with the MSB first; see Figure 16. The number of transmitted bytes during one data transfer is unrestricted but must meet the read/write cycle format.

8.1.4.4 Acknowledge

An acknowledge must be sent at the end of one data byte. The acknowledge-related clock pulse is generated by the master. The transmitter of data, either master or slave, releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver pulls down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

The master can then generate either a STOP (P) condition to stop the transfer or a repeated START (Sr) condition to start a new transfer.

A master-receiver indicates the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out by the slave. The slave-transmitter releases the data line to allow the master to generate a STOP (P) or repeated START (Sr) condition.

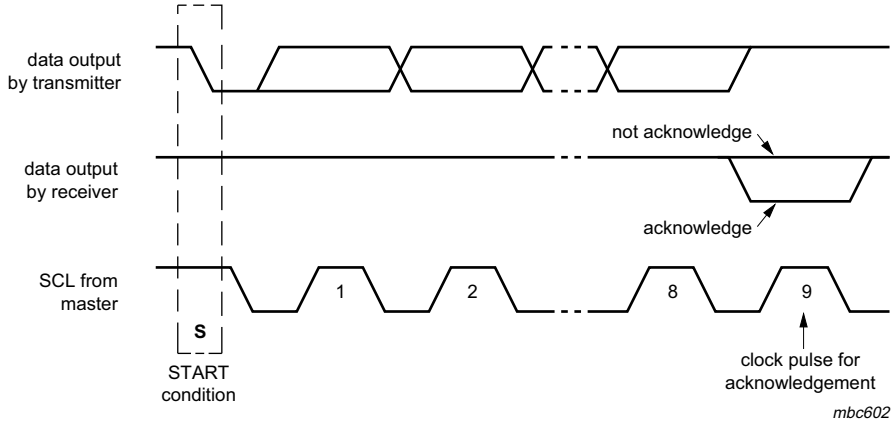


Fig 14. Acknowledge on the I²C-bus

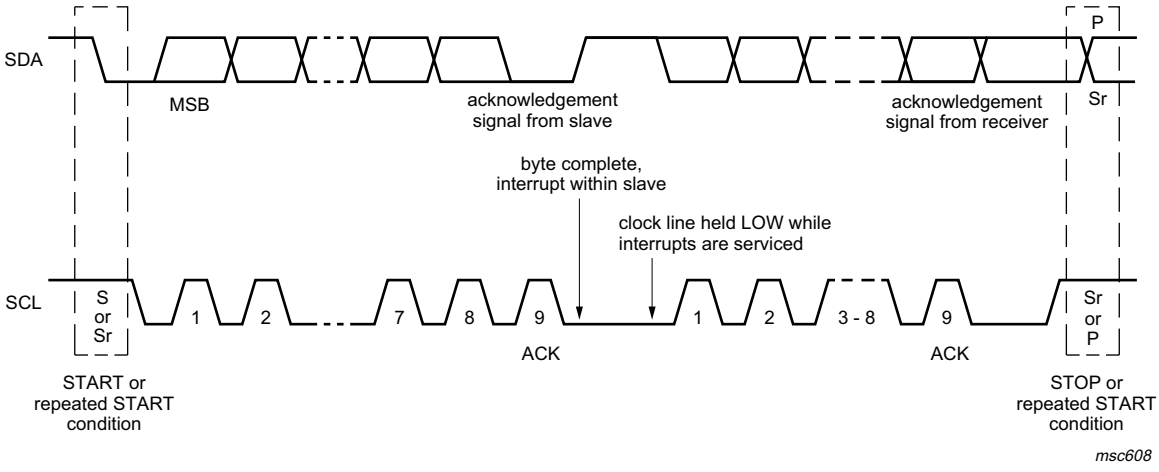


Fig 15. Data transfer on the I²C-bus

8.1.4.5 7-Bit addressing

During the I²C-bus address procedure, the first byte after the START condition is used to determine which slave will be selected by the master.

Several address numbers are reserved. During device configuration, the designer must ensure that collisions with these reserved addresses cannot occur. Check the *I²C-bus specification* for a complete list of reserved addresses.

The I²C-bus address specification is dependent on the definition of pin EA. Immediately after releasing pin NRSTPD or after a power-on reset, the device defines the I²C-bus address according to pin EA.

If pin EA is set LOW, the upper 4 bits of the device bus address are reserved by NXP Semiconductors and set to 0101b for all MFRC522 devices. The remaining 3 bits (ADR_0, ADR_1, ADR_2) of the slave address can be freely configured by the customer to prevent collisions with other I²C-bus devices.

If pin EA is set HIGH, ADR_0 to ADR_5 can be completely specified at the external pins according to Table 5 on page 8. ADR_6 is always set to logic 0.

In both modes, the external address coding is latched immediately after releasing the reset condition. Further changes at the used pins are not taken into consideration. Depending on the external wiring, the I²C-bus address pins can be used for test signal outputs.

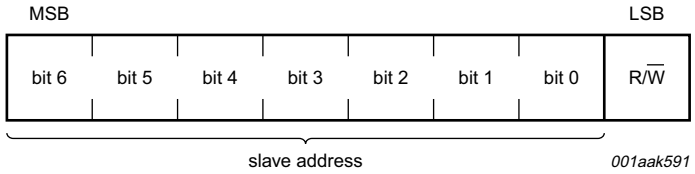


Fig 16. First byte following the START procedure

8.1.4.6 Register write access

To write data from the host controller using the I²C-bus to a specific register in the MFRC522 the following frame format must be used.

- The first byte of a frame indicates the device address according to the I²C-bus rules.
- The second byte indicates the register address followed by up to n-data bytes.

In one frame all data bytes are written to the same register address. This enables fast FIFO buffer access. The Read/Write (R/$\overline{W}$) bit is set to logic 0.

8.1.4.7 Register read access

To read out data from a specific register address in the MFRC522, the host controller must use the following procedure:

- Firstly, a write access to the specific register address must be performed as indicated in the frame that follows
- The first byte of a frame indicates the device address according to the I^2C-bus rules
- The second byte indicates the register address. No data bytes are added
- The Read/Write bit is 0

After the write access, read access can start. The host sends the device address of the MFRC522. In response, the MFRC522 sends the content of the read access register. In one frame all data bytes can be read from the same register address. This enables fast FIFO buffer access or register polling.

The Read/Write (R/W) bit is set to logic 1.

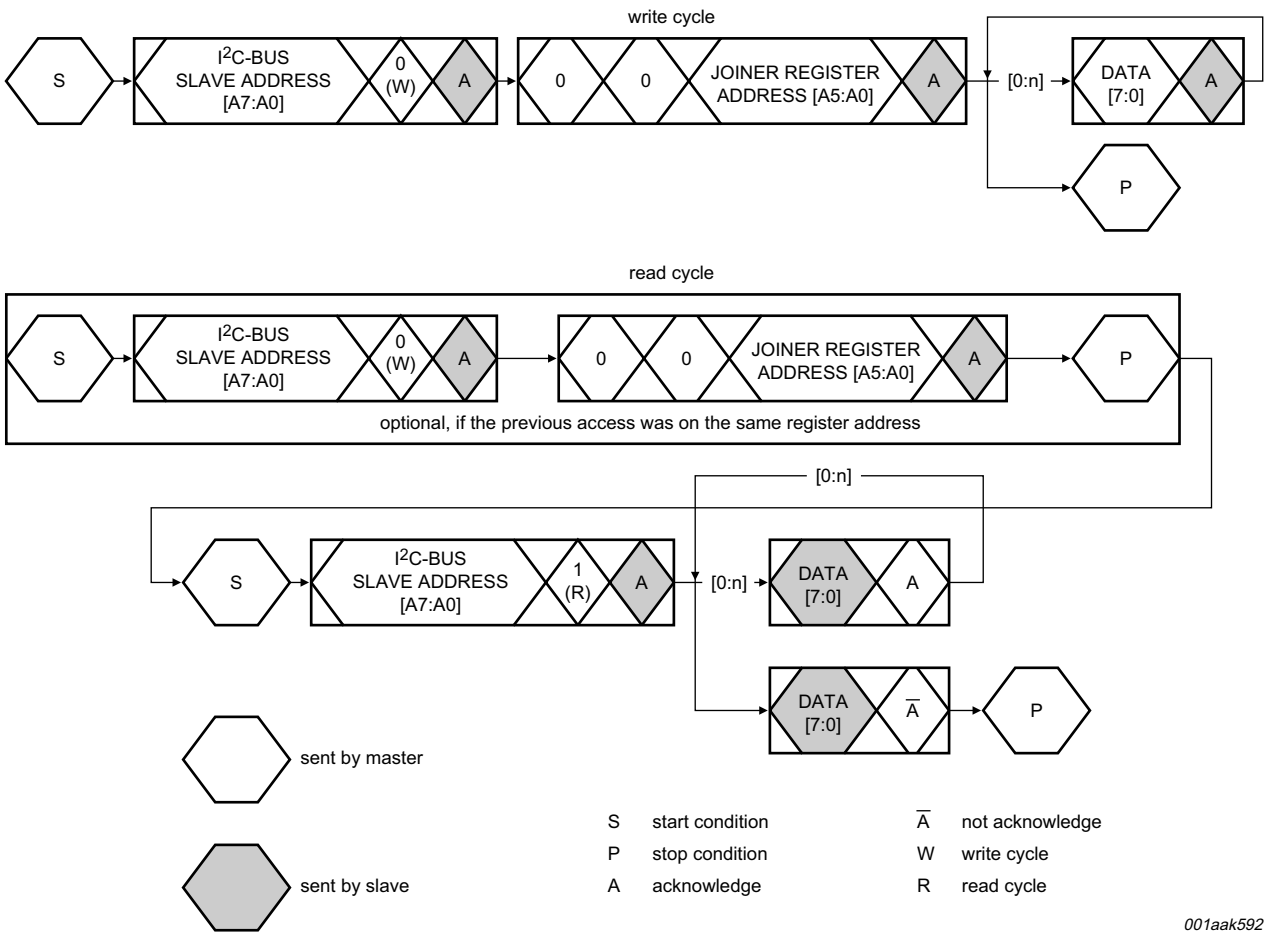


Fig 17. Register read and write access

8.1.4.8 High-speed mode

In High-speed mode (HS mode), the device can transfer information at data rates of up to 3.4 Mbit/s, while remaining fully downward-compatible with Fast or Standard mode (F/S mode) for bidirectional communication in a mixed-speed bus system.

8.1.4.9 High-speed transfer

To achieve data rates of up to 3.4 Mbit/s the following improvements have been made to I^2C-bus operation.

- The inputs of the device in HS mode incorporate spike suppression, a Schmitt trigger on the SDA and SCL inputs and different timing constants when compared to F/S mode
- The output buffers of the device in HS mode incorporate slope control of the falling edges of the SDA and SCL signals with different fall times compared to F/S mode

8.1.4.10 Serial data transfer format in HS mode

The HS mode serial data transfer format meets the Standard mode I^2C-bus specification. HS mode can only start after all of the following conditions (all of which are in F/S mode):

1. START condition (S)
2. 8-bit master code (00001XXXb)
3. Not-acknowledge bit ($\overline{A}$)

When HS mode starts, the active master sends a repeated START condition (Sr) followed by a 7-bit slave address with a R/W bit address and receives an acknowledge bit (A) from the selected MFRC522.

Data transfer continues in HS mode after the next repeated START (Sr), only switching back to F/S mode after a STOP condition (P). To reduce the overhead of the master code, a master links a number of HS mode transfers, separated by repeated START conditions (Sr).

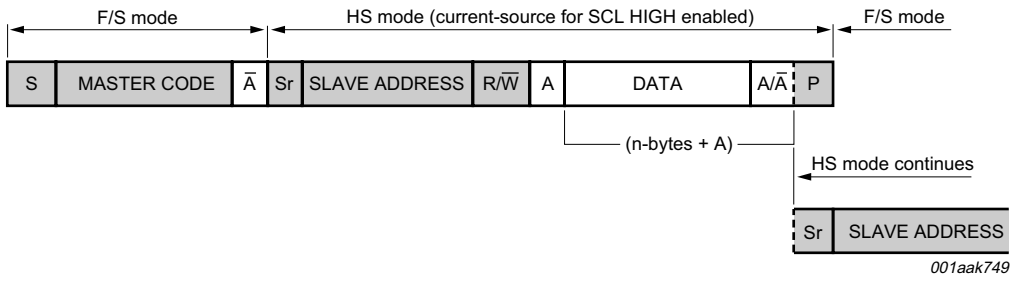


Fig 18. I^2C-bus HS mode protocol switch

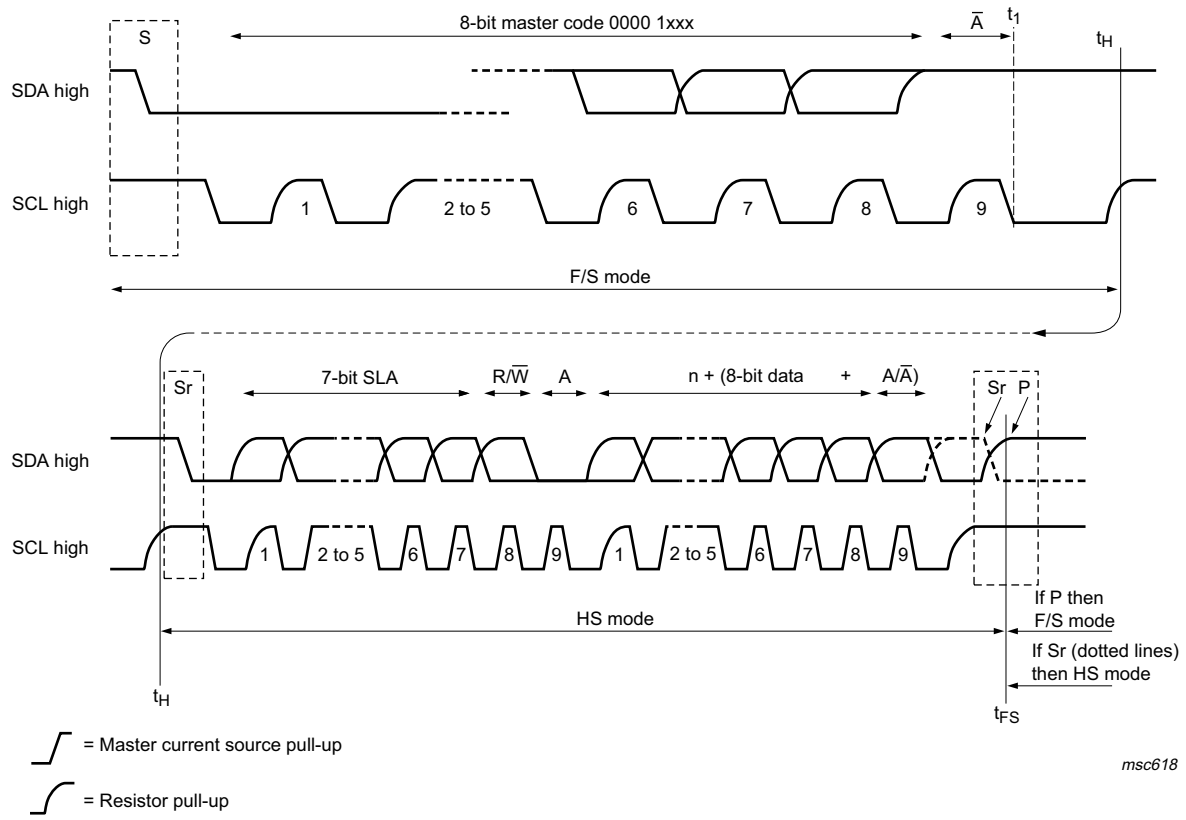


Fig 19. I²C-bus HS mode protocol frame

8.1.4.11 Switching between F/S mode and HS mode

After reset and initialization, the MFRC522 is in Fast mode (which is in effect F/S mode as Fast mode is downward-compatible with Standard mode). The connected MFRC522 recognizes the “S 00001XXX A” sequence and switches its internal circuitry from the Fast mode setting to the HS mode setting.

The following actions are taken:

1. Adapt the SDA and SCL input filters according to the spike suppression requirement in HS mode.
2. Adapt the slope control of the SDA output stages.

It is possible for system configurations that do not have other I^2C-bus devices involved in the communication to switch to HS mode permanently. This is implemented by setting Status2Reg register’s I^2CForceHS bit to logic 1. In permanent HS mode, the master code is not required to be sent. This is not defined in the specification and must only be used when no other devices are connected on the bus. In addition, spikes on the I^2C-bus lines must be avoided because of the reduced spike suppression.

8.1.4.12 MFRC522 at lower speed modes

MFRC522 is fully downward-compatible and can be connected to an F/S mode I^2C-bus system. The device stays in F/S mode and communicates at F/S mode speeds because a master code is not transmitted in this configuration.

8.2 Analog interface and contactless UART

8.2.1 General

The integrated contactless UART supports the external host online with framing and error checking of the protocol requirements up to 848 kBd. An external circuit can be connected to the communication interface pins MFIN and MFOUT to modulate and demodulate the data.

The contactless UART handles the protocol requirements for the communication protocols in cooperation with the host. Protocol handling generates bit and byte-oriented framing. In addition, it handles error detection such as parity and CRC, based on the various supported contactless communication protocols.

Remark: The size and tuning of the antenna and the power supply voltage have an important impact on the achievable operating distance.

8.2.2 TX p-driver

The signal on pins TX1 and TX2 is the 13.56 MHz energy carrier modulated by an envelope signal. It can be used to drive an antenna directly using a few passive components for matching and filtering; see Section 15 on page 78. The signal on pins TX1 and TX2 can be configured using the TxControlReg register; see Section 9.3.2.5 on page 48.

The modulation index can be set by adjusting the impedance of the drivers. The impedance of the p-driver can be configured using registers CWGsPReg and ModGsPReg. The impedance of the n-driver can be configured using the GsNReg register. The modulation index also depends on the antenna design and tuning.

The TxModeReg and TxSelReg registers control the data rate and framing during transmission and the antenna driver setting to support the different requirements at the different modes and transfer speeds.

Table 15. Register and bit settings controlling the signal on pin TX1

Bit Tx1RFEn	Bit Force 100ASK	Bit InvTx1RFOn	Bit InvTx1RFOff	Envelope	Pin TX1	GSPMos	GSNMos	Remarks
0	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	not specified if RF is switched off
1	0	0	X[1]	0	RF	pMod	nMod	100 % ASK: pin TX1 pulled to logic 0, independent of the InvTx1RFOff bit
				1	RF	pCW	nCW	
	0	1	X[1]	0	RF	pMod	nMod	
				1	RF	pCW	nCW	
	1	1	X[1]	0	0	pMod	nMod	
				1	RF_n	pCW	nCW	

[1] X = Do not care.

Table 16. Register and bit settings controlling the signal on pin TX2

Bit Tx1RFEn	Bit Force 100ASK	Bit Tx2CW	Bit InvTx2RFOn	Bit InvTx2RFOff	Envelope	Pin TX2	GSPMos	GSNMos	Remarks
0	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	X[1]	not specified if RF is switched off
1	0	0	0	X[1]	0	RF	pMod	nMod	-
					1	RF	pCW	nCW	
			1	X[1]	0	RF_n	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	X[1]	X[1]	RF	pCW	nCW	conductance always CW for the Tx2CW bit
			1	X[1]	X[1]	RF_n	pCW	nCW	
	1	0	0	X[1]	0	0	pMod	nMod	100 % ASK: pin TX2 pulled to logic 0 (independent of the InvTx2RFOn/InvTx2RFOff bits)
					1	RF	pCW	nCW	
			1	X[1]	0	0	pMod	nMod	
					1	RF_n	pCW	nCW	
		1	0	X[1]	X[1]	RF	pCW	nCW	
			1	X[1]	X[1]	RF_n	pCW	nCW	

[1] X = Do not care.

The following abbreviations have been used in Table 15 and Table 16:

- RF: 13.56 MHz clock derived from 27.12 MHz quartz crystal oscillator divided by 2
- RF_n: inverted 13.56 MHz clock
- GSPMos: conductance, configuration of the PMOS array
- GSNMos: conductance, configuration of the NMOS array
- pCW: PMOS conductance value for continuous wave defined by the CWGsPReg register
- pMod: PMOS conductance value for modulation defined by the ModGsPReg register
- nCW: NMOS conductance value for continuous wave defined by the GsNReg register's CWGsN[3:0] bits
- nMod: NMOS conductance value for modulation defined by the GsNReg register's ModGsN[3:0] bits
- X = do not care.

Remark: If only one driver is switched on, the values for CWGsPReg, ModGsPReg and GsNReg registers are used for both drivers.

8.2.3 Serial data switch

Two main blocks are implemented in the MFRC522. The digital block comprises the state machines, encoder/decoder logic. The analog block comprises the modulator and antenna drivers, the receiver and amplifiers. It is possible for the interface between these two blocks to be configured so that the interfacing signals are routed to pins MFIN and MFOUT.

This topology allows the analog block of the MFRC522 to be connected to the digital block of another device.

The serial signal switch is controlled by the TxSelReg and RxSelReg registers.

Figure 20 shows the serial data switch for p-driver TX1 and TX2.

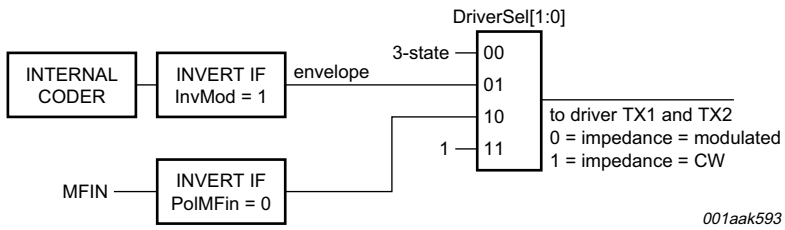


Fig 20. Serial data switch for p-driver TX1 and TX2

8.2.4 MFIN and MFOUT interface support

The MFRC522 is divided into a digital circuit block and an analog circuit block. The digital block contains state machines, encoder and decoder logic and so on. The analog block contains the modulator and antenna drivers, receiver and amplifiers. The interface between these two blocks can be configured so that the interfacing signals can be routed to pins MFIN and MFOUT; see Figure 21 on page 26. This configuration is implemented using TxSelReg register's MFOutSel[3:0] and DriverSel[1:0] bits and RxSelReg register's UARTSel[1:0] bits.

This topology allows some parts of the analog block to be connected to the digital block of another device.

Switch MFOutSel in the TxSelReg register can be used to measure MIFARE and ISO/IEC14443 A related signals. This is especially important during the design-in phase or for test purposes as it enables checking of the transmitted and received data.

The most important use of pins MFIN and MFOUT is found in the active antenna concept. An external active antenna circuit can be connected to the MFRC522's digital block. Switch MFOutSel must be configured so that the internal Miller encoded signal is sent to pin MFOUT (MFOutSel = 100b). UARTSel[1:0] must be configured to receive a Manchester signal with subcarrier from pin MFIN (UARTSel[1:0] = 01).

It is possible to connect a passive antenna to pins TX1, TX2 and RX (using the appropriate filter and matching circuit) and an active antenna to pins MFOUT and MFIN at the same time. In this configuration, two RF circuits can be driven (one after another) by a single host processor.

Remark: Pins MFIN and MFOUT have a dedicated supply on pin SVDD with the ground on pin PVSS. If pin MFIN is not used it must be connected to either pin SVDD or pin PVSS. If pin SVDD is not used it must be connected to either pin DVDD, pin PVDD or any other voltage supply pin.

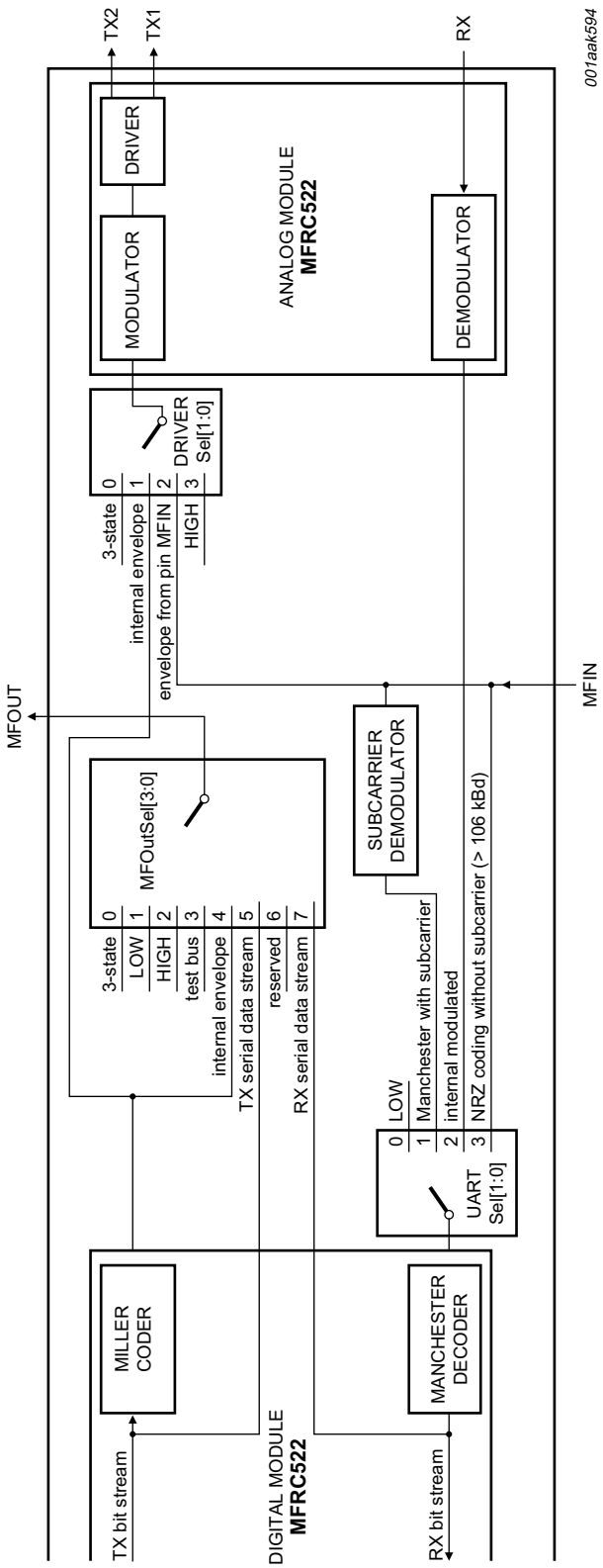


Fig 21. Overview of MFIN and MFOUT signal routing

8.2.5 CRC coprocessor

The following CRC coprocessor parameters can be configured:

- The CRC preset value can be either 0000h, 6363h, A671h or FFFFh depending on the ModeReg register's CRCPreset[1:0] bits setting
- The CRC polynomial for the 16-bit CRC is fixed to $x^{16} + x^{12} + x^5 + 1$
- The CRCResultReg register indicates the result of the CRC calculation. This register is split into two 8-bit registers representing the higher and lower bytes.
- The ModeReg register's MSBFirst bit indicates that data will be loaded with the MSB first.

Table 17. CRC coprocessor parameters

Parameter	Value
CRC register length	16-bit CRC
CRC algorithm	algorithm according to ISO/IEC 14443 A and ITU-T
CRC preset value	0000h, 6363h, A671h or FFFFh depending on the setting of the ModeReg register's CRCPreset[1:0] bits

8.3 FIFO buffer

An 8×64 bit FIFO buffer is used in the MFRC522. It buffers the input and output data stream between the host and the MFRC522's internal state machine. This makes it possible to manage data streams up to 64 bytes long without the need to take timing constraints into account.

8.3.1 Accessing the FIFO buffer

The FIFO buffer input and output data bus is connected to the FIFODataReg register. Writing to this register stores one byte in the FIFO buffer and increments the internal FIFO buffer write pointer. Reading from this register shows the FIFO buffer contents stored in the FIFO buffer read pointer and decrements the FIFO buffer read pointer. The distance between the write and read pointer can be obtained by reading the FIFOLevelReg register.

When the microcontroller starts a command, the MFRC522 can, while the command is in progress, access the FIFO buffer according to that command. Only one FIFO buffer has been implemented which can be used for input and output. The microcontroller must ensure that there are not any unintentional FIFO buffer accesses.

8.3.2 Controlling the FIFO buffer

The FIFO buffer pointers can be reset by setting FIFOLevelReg register's FlushBuffer bit to logic 1. Consequently, the FIFOLevel[6:0] bits are all set to logic 0 and the ErrorReg register's BufferOvfl bit is cleared. The bytes stored in the FIFO buffer are no longer accessible allowing the FIFO buffer to be filled with another 64 bytes.

8.3.3 FIFO buffer status information

The host can get the following FIFO buffer status information:

- Number of bytes stored in the FIFO buffer: FIFOLevelReg register's FIFOLevel[6:0]
- FIFO buffer almost full warning: Status1Reg register's HiAlert bit

- FIFO buffer almost empty warning: Status1Reg register's LoAlert bit
- FIFO buffer overflow warning: ErrorReg register's BufferOvfl bit. The BufferOvfl bit can only be cleared by setting the FIFOLevelReg register's FlushBuffer bit.

The MFRC522 can generate an interrupt signal when:

- ComIEnReg register's LoAlertIEn bit is set to logic 1. It activates pin IRQ when Status1Reg register's LoAlert bit changes to logic 1.
- ComIEnReg register's HiAlertIEn bit is set to logic 1. It activates pin IRQ when Status1Reg register's HiAlert bit changes to logic 1.

If the maximum number of WaterLevel bytes (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the HiAlert bit is set to logic 1. It is generated according to Equation 3:

$$HiAlert = (64 - FIFOLength) \leq WaterLevel \quad (3)$$

If the number of WaterLevel bytes (as set in the WaterLevelReg register) or less are stored in the FIFO buffer, the LoAlert bit is set to logic 1. It is generated according to Equation 4:

$$LoAlert = FIFOLength \leq WaterLevel \quad (4)$$

8.4 Interrupt request system

The MFRC522 indicates certain events by setting the Status1Reg register's IRq bit and, if activated, by pin IRQ. The signal on pin IRQ can be used to interrupt the host using its interrupt handling capabilities. This allows the implementation of efficient host software.

8.4.1 Interrupt sources overview

Table 18 shows the available interrupt bits, the corresponding source and the condition for its activation. The ComIrqReg register's TimerIRq interrupt bit indicates an interrupt set by the timer unit which is set when the timer decrements from 1 to 0.

The ComIrqReg register's TxIRq bit indicates that the transmitter has finished. If the state changes from sending data to transmitting the end of the frame pattern, the transmitter unit automatically sets the interrupt bit. The CRC coprocessor sets the DivIrqReg register's CRCIRq bit after processing all the FIFO buffer data which is indicated by CRCReady bit = 1.

The ComIrqReg register's RxIRq bit indicates an interrupt when the end of the received data is detected. The ComIrqReg register's IdleIRq bit is set if a command finishes and the Command[3:0] value in the CommandReg register changes to idle (see Table 149 on page 67).

The ComIrqReg register's HiAlertIRq bit is set to logic 1 when the Status1Reg register's HiAlert bit is set to logic 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

The ComIrqReg register's LoAlertIRq bit is set to logic 1 when the Status1Reg register's LoAlert bit is set to logic 1 which means that the FIFO buffer has reached the level indicated by the WaterLevel[5:0] bits.

The ComIrqReg register's ErrIRq bit indicates an error detected by the contactless UART during send or receive. This is indicated when any bit is set to logic 1 in register ErrorReg.

Table 18. Interrupt sources

Interrupt flag	Interrupt source	Trigger action
TimerIRq	timer unit	the timer counts from 1 to 0
TxIRq	transmitter	a transmitted data stream ends
CRCIRq	CRC coprocessor	all data from the FIFO buffer has been processed
RxIRq	receiver	a received data stream ends
IdleIRq	ComIrqReg register	command execution finishes
HiAlertIRq	FIFO buffer	the FIFO buffer is almost full
LoAlertIRq	FIFO buffer	the FIFO buffer is almost empty
ErrIRq	contactless UART	an error is detected

8.5 Timer unit

The MFRC522A has a timer unit which the external host can use to manage timing tasks. The timer unit can be used in one of the following timer/counter configurations:

- Timeout counter
- Watchdog counter
- Stop watch
- Programmable one shot
- Periodical trigger

The timer unit can be used to measure the time interval between two events or to indicate that a specific event occurred after a specific time. The timer can be triggered by events explained in the paragraphs below. The timer does not influence any internal events, for example, a time-out during data reception does not automatically influence the reception process. Furthermore, several timer-related bits can be used to generate an interrupt.

The timer has an input clock of 6.78 MHz derived from the 27.12 MHz quartz crystal oscillator. The timer consists of two stages: prescaler and counter.

The prescaler (TPrescaler) is a 12-bit counter. The reload values (TReloadVal_Hi[7:0] and TReloadVal_Lo[7:0]) for TPrescaler can be set between 0 and 4095 in the TModeReg register's TPrescaler_Hi[3:0] bits and TPrescalerReg register's TPrescaler_Lo[7:0] bits.

The reload value for the counter is defined by 16 bits between 0 and 65535 in the TReloadReg register.

The current value of the timer is indicated in the TCounterValReg register.

When the counter reaches 0, an interrupt is automatically generated, indicated by the ComIrqReg register's TimerIRq bit setting. If enabled, this event can be indicated on pin IRQ. The TimerIRq bit can be set and reset by the host. Depending on the configuration, the timer will stop at 0 or restart with the value set in the TReloadReg register.

The timer status is indicated by the Status1Reg register's TRunning bit.

The timer can be started manually using the ControlReg register's TStartNow bit and stopped using the ControlReg register's TStopNow bit.

The timer can also be activated automatically to meet any dedicated protocol requirements, by setting the TModeReg register's TAuto bit to logic 1.

The time delay of a timer stage is calculated with Equation 5 adding 1 to the reload values below:

- TPrescaler reload value = 4095
- TReloadVal reload value = 65535

$$Maximum\ time = 4096 \times \frac{65536}{6.78\ MHz} = 39.59\ s \quad (5)$$

Example: To indicate 100 µs, 678 clock cycles must be counted, so the TPrescaler value must be set to 677 using register TModeReg bits TPrescaler_Hi[3:0] and TPrescalerReg bits TPrescaler_Lo[7:0]. This gives the timer an input clock of 100 µs that enables it to count up to 65535 time slots for each 100 µs.

8.6 Power reduction modes

8.6.1 Hard power-down

Hard power-down is enabled when pin NRSTPD is LOW. This turns off all internal current sinks including the oscillator. All digital input buffers are separated from the input pins and clamped internally (except pin NRSTPD). The output pins are frozen at either a HIGH or LOW level.

8.6.2 Soft power-down mode

Soft Power-down mode is entered immediately after the CommandReg register's PowerDown bit is set to logic 1. All internal current sinks are switched off, including the oscillator buffer. However, the digital input buffers are not separated from the input pins and keep their functionality. The digital output pins do not change their state.

During soft power-down, all register values, the FIFO buffer content and the configuration keep their current contents.

After setting the PowerDown bit to logic 0, it takes 1024 clocks until the Soft power-down mode is exited indicated by the PowerDown bit. Setting it to logic 0 does not immediately clear it. It is cleared automatically by the MFRC522 when Soft power-down mode is exited.

Remark: If the internal oscillator is used, you must take into account that it is supplied by pin AVDD and it will take a certain time (t_{osc}) until the oscillator is stable and the clock cycles can be detected by the internal logic. It is recommended for the serial UART, to first send the value 55h to the MFRC522. The oscillator must be stable for further access to the registers. To ensure this, perform a read access to address 0 until the MFRC522 answers to the last read command with the register content of address 0. This indicates that the MFRC522 is ready.

8.6.3 Transmitter power-down mode

The Transmitter Power-down mode switches off the internal antenna drivers thereby, turning off the RF field. Transmitter power-down mode is entered by setting either the TxControlReg register's Tx1RFEn bit or Tx2RFEn bit to logic 0.

8.7 Oscillator circuit

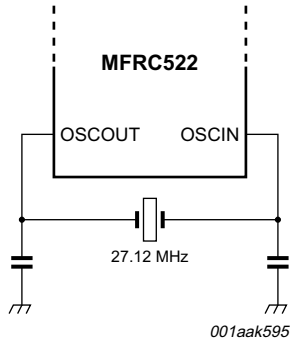


Fig 22. Quartz crystal connection

The clock applied to the MFRC522 provides a time basis for the synchronous system's encoder and decoder. The stability of the clock frequency, therefore, is an important factor for correct operation. To obtain optimum performance, clock jitter must be reduced as much as possible. This is best achieved using the internal oscillator buffer with the recommended circuitry.

If an external clock source is used, the clock signal must be applied to pin OSCIN. In this case, special care must be taken with the clock duty cycle and clock jitter and the clock quality must be verified.

8.8 Reset and oscillator start-up time

8.8.1 Reset timing requirements

The reset signal is filtered by a hysteresis circuit and a spike filter before it enters the digital circuit. The spike filter rejects signals shorter than 10 ns. In order to perform a reset, the signal must be LOW for at least 100 ns.

8.8.2 Oscillator start-up time

If the MFRC522 has been set to a Power-down mode or is powered by a V_{DDX} supply, the start-up time for the MFRC522 depends on the oscillator used and is shown in Figure 23.

The time ($t_{startup}$) is the start-up time of the crystal oscillator circuit. The crystal oscillator start-up time is defined by the crystal.

The time (t_d) is the internal delay time of the MFRC522 when the clock signal is stable before the MFRC522 can be addressed.

The delay time is calculated by:

$$t_d = \frac{1024}{27\ \mu s} = 37.74\ \mu s \quad (6)$$

The time (t_{osc}) is the sum of t_d and $t_{startup}$.

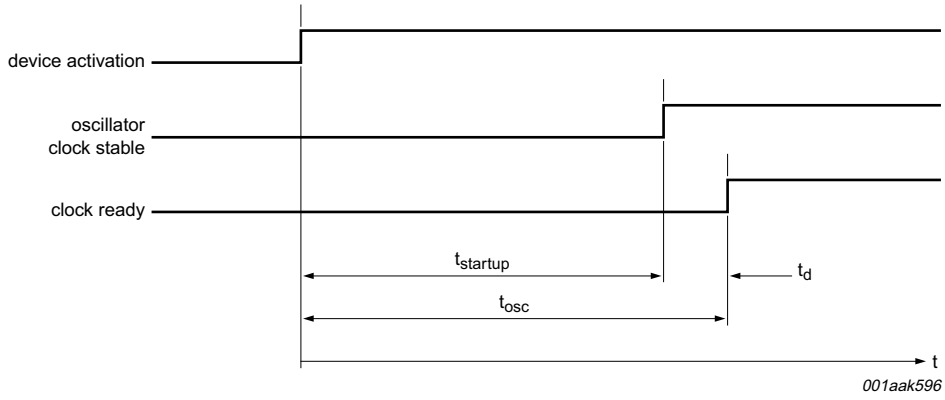


Fig 23. Oscillator start-up time

9. MFRC522 registers

9.1 Register bit behavior

Depending on the functionality of a register, the access conditions to the register can vary. In principle, bits with same behavior are grouped in common registers. The access conditions are described in Table 19.

Table 19. Behavior of register bits and their designation

Abbreviation	Behavior	Description
R/W	read and write	These bits can be written and read by the microcontroller. Since they are used only for control purposes, their content is not influenced by internal state machines, for example the ComIEnReg register can be written and read by the microcontroller. It will also be read by internal state machines but never changed by them.
D	dynamic	These bits can be written and read by the microcontroller. Nevertheless, they can also be written automatically by internal state machines, for example the CommandReg register changes its value automatically after the execution of the command.
R	read only	These register bits hold values which are determined by internal states only, for example the CRCReady bit cannot be written externally but shows internal states.
W	write only	Reading these register bits always returns zero.
reserved	-	These registers are reserved for future use and must not be changed. In case of a write access, it is recommended to always write the value “0”.
RFT	-	These register bits are reserved for future use or are for production tests and must not be changed.

9.2 Register overview

Table 20. MFRC522 register overview

Address (hex)	Register name	Function	Refer to
Page 0: Command and status			
00h	Reserved	reserved for future use	Table 21 on page 36
01h	CommandReg	starts and stops command execution	Table 23 on page 36
02h	ComlEnReg	enable and disable interrupt request control bits	Table 25 on page 36
03h	DivlEnReg	enable and disable interrupt request control bits	Table 27 on page 37
04h	ComIrqReg	interrupt request bits	Table 29 on page 37
05h	DivIrqReg	interrupt request bits	Table 31 on page 38
06h	ErrorReg	error bits showing the error status of the last command executed	Table 33 on page 39
07h	Status1Reg	communication status bits	Table 35 on page 40
08h	Status2Reg	receiver and transmitter status bits	Table 37 on page 41
09h	FIFODataReg	input and output of 64 byte FIFO buffer	Table 39 on page 42
0Ah	FIFOLevelReg	number of bytes stored in the FIFO buffer	Table 41 on page 42
0Bh	WaterLevelReg	level for FIFO underflow and overflow warning	Table 43 on page 42
0Ch	ControlReg	miscellaneous control registers	Table 45 on page 43
0Dh	BitFramingReg	adjustments for bit-oriented frames	Table 47 on page 44
0Eh	CollReg	bit position of the first bit-collision detected on the RF interface	Table 49 on page 44
0Fh	Reserved	reserved for future use	Table 51 on page 45
Page 1: Command			
10h	Reserved	reserved for future use	Table 53 on page 45
11h	ModeReg	defines general modes for transmitting and receiving	Table 55 on page 46
12h	TxModeReg	defines transmission data rate and framing	Table 57 on page 46
13h	RxModeReg	defines reception data rate and framing	Table 59 on page 47
14h	TxControlReg	controls the logical behavior of the antenna driver pins TX1 and TX2	Table 61 on page 48
15h	TxASKReg	controls the setting of the transmission modulation	Table 63 on page 49
16h	TxSelReg	selects the internal sources for the antenna driver	Table 65 on page 49
17h	RxSelReg	selects internal receiver settings	Table 67 on page 50
18h	RxThresholdReg	selects thresholds for the bit decoder	Table 69 on page 51
19h	DemodReg	defines demodulator settings	Table 71 on page 51
1Ah	Reserved	reserved for future use	Table 73 on page 52
1Bh	Reserved	reserved for future use	Table 75 on page 52
1Ch	MfTxReg	controls some MIFARE communication transmit parameters	Table 77 on page 52
1Dh	MfRxReg	controls some MIFARE communication receive parameters	Table 79 on page 53
1Eh	Reserved	reserved for future use	Table 81 on page 53
1Fh	SerialSpeedReg	selects the speed of the serial UART interface	Table 83 on page 53
Page 2: Configuration			
20h	Reserved	reserved for future use	Table 85 on page 54

Table 20. MFRC522 register overview *...continued*

Address (hex)	Register name	Function	Refer to
21h	CRCResultReg	shows the MSB and LSB values of the CRC calculation	Table 87 on page 54
22h			Table 89 on page 54
23h	Reserved	reserved for future use	Table 91 on page 55
24h	ModWidthReg	controls the ModWidth setting	Table 93 on page 55
25h	Reserved	reserved for future use	Table 95 on page 55
26h	RFCfgReg	configures the receiver gain	Table 97 on page 56
27h	GsNReg	selects the conductance of the antenna driver pins TX1 and TX2 for modulation	Table 99 on page 56
28h	CWGsPReg	defines the conductance of the p-driver output during periods of no modulation	Table 101 on page 57
29h	ModGsPReg	defines the conductance of the p-driver output during periods of modulation	Table 103 on page 57
2Ah	TModeReg	defines settings for the internal timer	Table 105 on page 57
2Bh	TPrescalerReg		Table 107 on page 58
2Ch	TReloadReg	defines the 16-bit timer reload value	Table 109 on page 59
2Dh			Table 111 on page 59
2Eh	TCounterValReg	shows the 16-bit timer value	Table 113 on page 59
2Fh			Table 115 on page 59
Page 3: Test register			
30h	Reserved	reserved for future use	Table 117 on page 60
31h	TestSel1Reg	general test signal configuration	Table 119 on page 60
32h	TestSel2Reg	general test signal configuration and PRBS control	Table 121 on page 60
33h	TestPinEnReg	enables pin output driver on pins D1 to D7	Table 123 on page 61
34h	TestPinValueReg	defines the values for D1 to D7 when it is used as an I/O bus	Table 125 on page 61
35h	TestBusReg	shows the status of the internal test bus	Table 127 on page 62
36h	AutoTestReg	controls the digital self test	Table 129 on page 62
37h	VersionReg	shows the software version	Table 131 on page 63
38h	AnalogTestReg	controls the pins AUX1 and AUX2	Table 133 on page 63
39h	TestDAC1Reg	defines the test value for TestDAC1	Table 135 on page 65
3Ah	TestDAC2Reg	defines the test value for TestDAC2	Table 137 on page 65
3Bh	TestADCReg	shows the value of ADC I and Q channels	Table 139 on page 65
3Ch to 3Fh	Reserved	reserved for production tests	Table 141 to Table 147 on page 66

9.3 Register descriptions

9.3.1 Page 0: Command and status

9.3.1.1 Reserved register 00h

Functionality is reserved for future use.

Table 21. Reserved register (address 00h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 22. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	-	reserved

9.3.1.2 CommandReg register

Starts and stops command execution.

Table 23. CommandReg register (address 01h); reset value: 20h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol:	reserved		RcvOff	PowerDown	Command[3:0]			
Access:	-		R/W	D	D			

Table 24. CommandReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	reserved	-	reserved for future use
5	RcvOff	1	analog part of the receiver is switched off
4	PowerDown	1	Soft power-down mode entered
		0	MFRC522 starts the wake up procedure during which this bit is read as a logic 1; it is read as a logic 0 when the MFRC522 is ready; see Section 8.6.2 on page 31 **Remark:** The PowerDown bit cannot be set when the SoftReset command is activated
3 to 0	Command[3:0]	-	activates a command based on the Command value; reading this register shows which command is executed; see Section 10.3 on page 67

9.3.1.3 ComIEnReg register

Control bits to enable and disable the passing of interrupt requests.

Table 25. ComIEnReg register (address 02h); reset value: 80h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IRqInv	TxIEn	RxIEn	IdleIEn	HiAlertIEn	LoAlertIEn	ErrIEn	TimerIEn
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 26. ComIEnReg register bit descriptions

Bit	Symbol	Value	Description
7	IRqInv	1	signal on pin IRQ is inverted with respect to the Status1Reg register's IRq bit
		0	signal on pin IRQ is equal to the IRq bit; in combination with the DivIEnReg register's IRqPushPull bit, the default value of logic 1 ensures that the output level on pin IRQ is 3-state
6	TxIEn	-	allows the transmitter interrupt request (TxIRq bit) to be propagated to pin IRQ
5	RxIEn	-	allows the receiver interrupt request (RxIRq bit) to be propagated to pin IRQ
4	IdleIEn	-	allows the idle interrupt request (IdleIRq bit) to be propagated to pin IRQ
3	HiAlertIEn	-	allows the high alert interrupt request (HiAlertIRq bit) to be propagated to pin IRQ
2	LoAlertIEn	-	allows the low alert interrupt request (LoAlertIRq bit) to be propagated to pin IRQ
1	ErrIEn	-	allows the error interrupt request (ErrIRq bit) to be propagated to pin IRQ
0	TimerIEn	-	allows the timer interrupt request (TimerIRq bit) to be propagated to pin IRQ

9.3.1.4 DivIEnReg register

Control bits to enable and disable the passing of interrupt requests.

Table 27. DivIEnReg register (address 03h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IRQPushPull	reserved		MfinActIEn	reserved	CRCIEn	reserved	
Access	R/W	-		R/W	-	R/W	-	

Table 28. DivIEnReg register bit descriptions

Bit	Symbol	Value	Description
7	IRQPushPull	1	pin IRQ is a standard CMOS output pin
		0	pin IRQ is an open-drain output pin
6 to 5	reserved	-	reserved for future use
4	MfinActIEn	-	allows the MFIN active interrupt request to be propagated to pin IRQ
3	reserved	-	reserved for future use
2	CRCIEn	-	allows the CRC interrupt request, indicated by the DivIrqReg register's CRCIRq bit, to be propagated to pin IRQ
1 to 0	reserved	-	reserved for future use

9.3.1.5 ComIrqReg register

Interrupt request bits.

Table 29. ComIrqReg register (address 04h); reset value: 14h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Set1	TxIRq	RxIRq	IdleIRq	HiAlertIRq	LoAlertIRq	ErrIRq	TimerIRq
Access	W	D	D	D	D	D	D	D

Table 30. ComIrqReg register bit descriptions

All bits in the ComIrqReg register are cleared by software.

Bit	Symbol	Value	Description
7	Set1	1	indicates that the marked bits in the ComIrqReg register are set
		0	indicates that the marked bits in the ComIrqReg register are cleared
6	TxIRq	1	set immediately after the last bit of the transmitted data was sent out
5	RxIRq	1	receiver has detected the end of a valid data stream if the RxModeReg register's RxNoErr bit is set to logic 1, the RxIRq bit is only set to logic 1 when data bytes are available in the FIFO
4	IdleIRq	1	If a command terminates, for example, when the CommandReg changes its value from any command to the Idle command (see Table 149 on page 67) if an unknown command is started, the CommandReg register Command[3:0] value changes to the idle state and the IdleIRq bit is set The microcontroller starting the Idle command does not set the IdleIRq bit
3	HiAlertIRq	1	the Status1Reg register's HiAlert bit is set in opposition to the HiAlert bit, the HiAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register
2	LoAlertIRq	1	Status1Reg register's LoAlert bit is set in opposition to the LoAlert bit, the LoAlertIRq bit stores this event and can only be reset as indicated by the Set1 bit in this register
1	ErrIRq	1	any error bit in the ErrorReg register is set
0	TimerIRq	1	the timer decrements the timer value in register TCounterValReg to zero

9.3.1.6 DivIrqReg register

Interrupt request bits.

Table 31. DivIrqReg register (address 05h); reset value: x0h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Set2	reserved		MfinActIRq	reserved	CRCIRq	reserved	
Access	W	-		D	-	D	-	

Table 32. DivIrqReg register bit descriptions

All bits in the DivIrqReg register are cleared by software.

Bit	Symbol	Value	Description
7	Set2	1	indicates that the marked bits in the DivIrqReg register are set
		0	indicates that the marked bits in the DivIrqReg register are cleared
6 to 5	reserved	-	reserved for future use
4	MfinActIRq	1	MFIN is active this interrupt is set when either a rising or falling signal edge is detected
3	reserved	-	reserved for future use
2	CRCIRq	1	the CalcCRC command is active and all data is processed
1 to 0	reserved	-	reserved for future use

9.3.1.7 ErrorReg register

Error bit register showing the error status of the last command executed.

Table 33. ErrorReg register (address 06h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WrErr	TempErr	reserved	BufferOvfl	CollErr	CRCErr	ParityErr	ProtocolErr
Access	R	R	-	R	R	R	R	R

Table 34: ErrorReg register bit descriptions

Bit	Symbol	Value	Description
7	WrErr	1	data is written into the FIFO buffer by the host during the MFAuthent command or if data is written into the FIFO buffer by the host during the time between sending the last bit on the RF interface and receiving the last bit on the RF interface
6	TempErr[1]	1	internal temperature sensor detects overheating, in which case the antenna drivers are automatically switched off
5	reserved	-	reserved for future use
4	BufferOvfl	1	the host or a MFRC522's internal state machine (e.g. receiver) tries to write data to the FIFO buffer even though it is already full
3	CollErr	1	a bit-collision is detected cleared automatically at receiver start-up phase only valid during the bitwise anticollision at 106 kBd always set to logic 0 during communication protocols at 212 kBd, 424 kBd and 848 kBd
2	CRCErr	1	the RxModeReg register's RxCRCEn bit is set and the CRC calculation fails automatically cleared to logic 0 during receiver start-up phase
1	ParityErr	1	parity check failed automatically cleared during receiver start-up phase only valid for ISO/IEC 14443 A/MIFARE communication at 106 kBd
0	ProtocolErr	1	set to logic 1 if the SOF is incorrect automatically cleared during receiver start-up phase bit is only valid for 106 kBd during the MFAuthent command, the ProtocolErr bit is set to logic 1 if the number of bytes received in one data stream is incorrect

[1] Command execution clears all error bits except the TempErr bit. Cannot be set by software.

9.3.1.8 Status1Reg register

Contains status bits of the CRC, interrupt and FIFO buffer.

Table 35. Status1Reg register (address 07h); reset value: 21h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	CRCOk	CRCReady	IRq	TRunning	reserved	HiAlert	LoAlert
Access	-	R	R	R	R	-	R	R

Table 36. Status1Reg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6	CRCOk	1	the CRC result is zero for data transmission and reception, the CRCOk bit is undefined: use the ErrorReg register's CRCErr bit indicates the status of the CRC coprocessor, during calculation the value changes to logic 0, when the calculation is done correctly the value changes to logic 1
5	CRCReady	1	the CRC calculation has finished only valid for the CRC coprocessor calculation using the CalcCRC command
4	IRq	-	indicates if any interrupt source requests attention with respect to the setting of the interrupt enable bits: see the ComIEnReg and DivIEnReg registers
3	TRunning	1	MFRC522's timer unit is running, i.e. the timer will decrement the TCounterValReg register with the next timer clock **Remark:** in gated mode, the TRunning bit is set to logic 1 when the timer is enabled by TModeReg register's TGated[1:0] bits; this bit is not influenced by the gated signal
2	reserved	-	reserved for future use
1	HiAlert	1	the number of bytes stored in the FIFO buffer corresponds to equation: $HiAlert = (64 - FIFOLength) \leq WaterLevel$ example: FIFO length = 60, WaterLevel = 4 → HiAlert = 1 FIFO length = 59, WaterLevel = 4 → HiAlert = 0
0	LoAlert	1	the number of bytes stored in the FIFO buffer corresponds to equation: $LoAlert = FIFOLength \leq WaterLevel$ example: FIFO length = 4, WaterLevel = 4 → LoAlert = 1 FIFO length = 5, WaterLevel = 4 → LoAlert = 0

9.3.1.9 Status2Reg register

Contains status bits of the receiver, transmitter and data mode detector.

Table 37. Status2Reg register (address 08h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TempSensClear	I²CForceHS	reserved		MFCrypto1On	ModemState[2:0]		
Access	R/W	R/W	-		D	R		

Table 38. Status2Reg register bit descriptions

Bit	Symbol	Value	Description
7	TempSensClear	1	clears the temperature error if the temperature is below the alarm limit of 125 °C
6	I²CForceHS		I²C-bus input filter settings:
		1	the I²C-bus input filter is set to the High-speed mode independent of the I²C-bus protocol
		0	the I²C-bus input filter is set to the I²C-bus protocol used
5 to 4	reserved	-	reserved
3	MFCrypto1On	-	indicates that the MIFARE Crypto1 unit is switched on and therefore all data communication with the card is encrypted can only be set to logic 1 by a successful execution of the MFAuthent command only valid in Read/Write mode for MIFARE standard cards this bit is cleared by software
2 to 0	ModemState[2:0]	-	shows the state of the transmitter and receiver state machines:
		000	idle
		001	wait for the BitFramingReg register's StartSend bit
		010	TxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1 the minimum time for TxWait is defined by the TxWaitReg register
		011	transmitting
		100	RxWait: wait until RF field is present if the TModeReg register's TxWaitRF bit is set to logic 1 the minimum time for RxWait is defined by the RxWaitReg register
		101	wait for data
		110	receiving

9.3.1.10 FIFODataReg register

Input and output of 64 byte FIFO buffer.

Table 39. FIFODataReg register (address 09h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FIFOData[7:0]							
Access	D							

Table 40. FIFODataReg register bit descriptions

Bit	Symbol	Description
7 to 0	FIFOData[7:0]	data input and output port for the internal 64-byte FIFO buffer FIFO buffer acts as parallel in/parallel out converter for all serial data stream inputs and outputs

9.3.1.11 FIFOLevelReg register

Indicates the number of bytes stored in the FIFO.

Table 41. FIFOLevelReg register (address 0Ah); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FlushBuffer	FIFOLevel[6:0]						
Access	W	R						

Table 42. FIFOLevelReg register bit descriptions

Bit	Symbol	Value	Description
7	FlushBuffer	1	immediately clears the internal FIFO buffer's read and write pointer and ErrorReg register's BufferOvfl bit reading this bit always returns 0
6 to 0	FIFOLevel [6:0]	-	indicates the number of bytes stored in the FIFO buffer writing to the FIFODataReg register increments and reading decrements the FIFOLevel value

9.3.1.12 WaterLevelReg register

Defines the level for FIFO under- and overflow warning.

Table 43. WaterLevelReg register (address 0Bh); reset value: 08h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		WaterLevel[5:0]					
Access	-		R/W					

Table 44. WaterLevelReg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	WaterLevel [5:0]	defines a warning level to indicate a FIFO buffer overflow or underflow: Status1Reg register's HiAlert bit is set to logic 1 if the remaining number of bytes in the FIFO buffer space is equal to, or less than the defined number of WaterLevel bytes Status1Reg register's LoAlert bit is set to logic 1 if equal to, or less than the WaterLevel bytes in the FIFO buffer **Remark:** to calculate values for HiAlert and LoAlert see Section 9.3.1.8 on page 40.

9.3.1.13 ControlReg register

Miscellaneous control bits.

Table 45. ControlReg register (address 0Ch); reset value: 10h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TStopNow	TStartNow	reserved			RxLastBits[2:0]		
Access	W	W	-			R		

Table 46. ControlReg register bit descriptions

Bit	Symbol	Value	Description
7	TStopNow	1	timer stops immediately reading this bit always returns it to 0
6	TStartNow	1	timer starts immediately reading this bit always returns it to 0
5 to 3	reserved	-	reserved for future use
2 to 0	RxLastBits[2:0]	-	indicates the number of valid bits in the last received byte if this value is zero, the whole byte is valid

9.3.1.14 BitFramingReg register

Adjustments for bit-oriented frames.

Table 47. BitFramingReg register (address 0Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	StartSend	RxAlign[2:0]			reserved	TxLastBits[2:0]		
Access	W	R/W			-	R/W		

Table 48. BitFramingReg register bit descriptions

Bit	Symbol	Value	Description
7	StartSend	1	starts the transmission of data only valid in combination with the Transceive command
6 to 4	RxAlign[2:0]		used for reception of bit-oriented frames: defines the bit position for the first bit received to be stored in the FIFO buffer example:
		0	LSB of the received bit is stored at bit position 0, the second received bit is stored at bit position 1
		1	LSB of the received bit is stored at bit position 1, the second received bit is stored at bit position 2
		7	LSB of the received bit is stored at bit position 7, the second received bit is stored in the next byte that follows at bit position 0
			These bits are only to be used for bitwise anticollision at 106 kBd, for all other modes they are set to 0
3	reserved	-	reserved for future use
2 to 0	TxLastBits[2:0]	-	used for transmission of bit oriented frames: defines the number of bits of the last byte that will be transmitted 000b indicates that all bits of the last byte will be transmitted

9.3.1.15 CollReg register

Defines the first bit-collision detected on the RF interface.

Table 49. CollReg register (address 0Eh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ValuesAfterColl	reserved	CollPosNotValid	CollPos[4:0]				
Access	R/W	-	R	R				

Table 50. CollReg register bit descriptions

Bit	Symbol	Value	Description
7	ValuesAfterColl	0	all received bits will be cleared after a collision only used during bitwise anticollision at 106 kBd, otherwise it is set to logic 1
6	reserved	-	reserved for future use
5	CollPosNotValid	1	no collision detected or the position of the collision is out of the range of CollPos[4:0]

Table 50. CollReg register bit descriptions …continued

Bit	Symbol	Value	Description
4 to 0	CollPos[4:0]	-	shows the bit position of the first detected collision in a received frame
			only data bits are interpreted
			example:
		00h	indicates a bit-collision in the 32nd bit
		01h	indicates a bit-collision in the 1st bit
		08h	indicates a bit-collision in the 8th bit
			These bits will only be interpreted if the CollPosNotValid bit is set to logic 0

9.3.1.16 Reserved register 0Fh

Functionality is reserved for future use.

Table 51. Reserved register (address 0Fh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 52. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.2 Page 1: Communication

9.3.2.1 Reserved register 10h

Functionality is reserved for future use.

Table 53. Reserved register (address 10h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 54. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.2.2 ModeReg register

Defines general mode settings for transmitting and receiving.

Table 55. ModeReg register (address 11h); reset value: 3Fh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MSBFirst	reserved	TxWaitRF	reserved	PolMFin	reserved	CRCPreset[1:0]	
Access	R/W	-	R/W	-	R/W	-	R/W	

Table 56. ModeReg register bit descriptions

Bit	Symbol	Value	Description
7	MSBFirst	1	CRC coprocessor calculates the CRC with MSB first in the CRCResultReg register the values for the CRCResultMSB[7:0] bits and the CRCResultLSB[7:0] bits are bit reversed **Remark:** during RF communication this bit is ignored
6	reserved	-	reserved for future use
5	TxWaitRF	1	transmitter can only be started if an RF field is generated
4	reserved	-	reserved for future use
3	PolMFin		defines the polarity of pin MFIN **Remark:** the internal envelope signal is encoded active LOW, changing this bit generates a MFinActIRq event
		1	polarity of pin MFIN is active HIGH
		0	polarity of pin MFIN is active LOW
2	reserved	-	reserved for future use
1 to 0	CRCPreset [1:0]		defines the preset value for the CRC coprocessor for the CalcCRC command **Remark:** during any communication, the preset values are selected automatically according to the definition of bits in the RxModeReg and TxModeReg registers
		00	0000h
		01	6363h
		10	A671h
		11	FFFFh

9.3.2.3 TxModeReg register

Defines the data rate during transmission.

Table 57. TxModeReg register (address 12h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TxCRCEn	TxSpeed[2:0]			InvMod	reserved		
Access	R/W	D			R/W	-		

Table 58. TxModeReg register bit descriptions

Bit	Symbol	Value	Description
7	TxCRCEn	1	enables CRC generation during data transmission **Remark:** can only be set to logic 0 at 106 kBd
6 to 4	TxSpeed[2:0]		defines the bit rate during data transmission the MFRC522 handles transfer speeds up to 848 kBd
		000	106 kBd
		001	212 kBd
		010	424 kBd
		011	848 kBd
		100	reserved
		101	reserved
		110	reserved
		111	reserved
3	InvMod	1	modulation of transmitted data is inverted
2 to 0	reserved	-	reserved for future use

9.3.2.4 RxModeReg register

Defines the data rate during reception.

Table 59. RxModeReg register (address 13h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RxCRCEn	RxSpeed[2:0]			RxNoErr	RxMultiple	reserved	
Access	R/W	D			R/W	R/W	-	

Table 60. RxModeReg register bit descriptions

Bit	Symbol	Value	Description
7	RxCRCEn	1	enables the CRC calculation during reception **Remark:** can only be set to logic 0 at 106 kBd
6 to 4	RxSpeed[2:0]		defines the bit rate while receiving data the MFRC522 handles transfer speeds up to 848 kBd
		000	106 kBd
		001	212 kBd
		010	424 kBd
		011	848 kBd
		100	reserved
		101	reserved
		110	reserved
		111	reserved
3	RxNoErr	1	an invalid received data stream (less than 4 bits received) will be ignored and the receiver remains active

Table 60. RxModeReg register bit descriptions …continued

Bit	Symbol	Value	Description
2	RxMultiple	0	receiver is deactivated after receiving a data frame
		1	able to receive more than one data frame only valid for data rates above 106 kBd in order to handle the polling command after setting this bit the Receive and Transceive commands will not terminate automatically. Multiple reception can only be deactivated by writing any command (except the Receive command) to the CommandReg register, or by the host clearing the bit if set to logic 1, an error byte is added to the FIFO buffer at the end of a received data stream which is a copy of the ErrorReg register value
1 to 0	reserved	-	reserved for future use

9.3.2.5 TxControlReg register

Controls the logical behavior of the antenna driver pins TX1 and TX2.

Table 61. TxControlReg register (address 14h); reset value: 80h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	InvTx2RFOn	InvTx1RFOn	InvTx2RFOff	InvTx1RFOff	Tx2CW	reserved	Tx2RFEn	Tx1RFEn
Access	R/W	R/W	R/W	R/W	R/W	-	R/W	R/W

Table 62. TxControlReg register bit descriptions

Bit	Symbol	Value	Description
7	InvTx2RFOn	1	output signal on pin TX2 inverted when driver TX2 is enabled
6	InvTx1RFOn	1	output signal on pin TX1 inverted when driver TX1 is enabled
5	InvTx2RFOff	1	output signal on pin TX2 inverted when driver TX2 is disabled
4	InvTx1RFOff	1	output signal on pin TX1 inverted when driver TX1 is disabled
3	Tx2CW	1	output signal on pin TX2 continuously delivers the unmodulated 13.56 MHz energy carrier
		0	Tx2CW bit is enabled to modulate the 13.56 MHz energy carrier
2	reserved	-	reserved for future use
1	Tx2RFEn	1	output signal on pin TX2 delivers the 13.56 MHz energy carrier modulated by the transmission data
0	Tx1RFEn	1	output signal on pin TX1 delivers the 13.56 MHz energy carrier modulated by the transmission data

9.3.2.6 TxASKReg register

Controls transmit modulation settings.

Table 63. TxASKReg register (address 15h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	Force100ASK	reserved					
Access	-	R/W	-					

Table 64. TxASKReg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6	Force100ASK	1	forces a 100 % ASK modulation independent of the ModGsPReg register setting
5 to 0	reserved	-	reserved for future use

9.3.2.7 TxSelReg register

Selects the internal sources for the analog module.

Table 65. TxSelReg register (address 16h); reset value: 10h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol:	reserved		DriverSel[1:0]		MFOutSel[3:0]			
Access:	-		R/W		R/W			

Table 66. TxSelReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	reserved	-	reserved for future use
5 to 4	DriverSel[1:0]	-	selects the input of drivers TX1 and TX2
		00	3-state; in soft power-down the drivers are only in 3-state mode if the DriverSel[1:0] value is set to 3-state mode
		01	modulation signal (envelope) from the internal encoder, Miller pulse encoded
		10	modulation signal (envelope) from pin MIFIN
		11	HIGH; the HIGH level depends on the setting of bits InvTx1RFOn/InvTx1RFOff and InvTx2RFOn/InvTx2RFOff

Table 66. TxSelReg register bit descriptions …continued

Bit	Symbol	Value	Description
3 to 0	MFOutSel [3:0]		selects the input for pin MFOUT
		0000	3-state
		0001	LOW
		0010	HIGH
		0011	test bus signal as defined by the TestSel1Reg register's TstBusBitSel[2:0] value
		0100	modulation signal (envelope) from the internal encoder, Miller pulse encoded
		0101	serial data stream to be transmitted, data stream before Miller encoder
		0110	reserved
		0111	serial data stream received, data stream after Manchester decoder
		1000 to 1111	reserved

9.3.2.8 RxSelReg register

Selects internal receiver settings.

Table 67. RxSelReg register (address 17h); reset value: 84h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	UARTSel[1:0]		RxWait[5:0]					
Access	R/W		R/W					

Table 68. RxSelReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	UARTSel [1:0]		selects the input of the contactless UART
		00	constant LOW
		01	Manchester with subcarrier from pin MFIN
		10	modulated signal from the internal analog module, default
		11	NRZ coding without subcarrier from pin MFIN which is only valid for transfer speeds above 106 kBd
5 to 0	RxWait [5:0]	-	after data transmission the activation of the receiver is delayed for RxWait bit-clocks, during this 'frame guard time' any signal on pin RX is ignored this parameter is ignored by the Receive command all other commands, such as Transceive, MFAuthent use this parameter the counter starts immediately after the external RF field is switched on

9.3.2.9 RxThresholdReg register

Selects thresholds for the bit decoder.

Table 69. RxThresholdReg register (address 18h); reset value: 84h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MinLevel[3:0]				reserved	CollLevel[2:0]		
Access	R/W				-	R/W		

Table 70. RxThresholdReg register bit descriptions

Bit	Symbol	Description
7 to 4	MinLevel [3:0]	defines the minimum signal strength at the decoder input that will be accepted if the signal strength is below this level it is not evaluated
3	reserved	reserved for future use
2 to 0	CollLevel [2:0]	defines the minimum signal strength at the decoder input that must be reached by the weaker half-bit of the Manchester encoded signal to generate a bit-collision relative to the amplitude of the stronger half-bit

9.3.2.10 DemodReg register

Defines demodulator settings.

Table 71. DemodReg register (address 19h); reset value: 4Dh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	AddIQ[1:0]		FixIQ	reserved	TauRcv[1:0]		TauSync[1:0]	
Access	R/W		R/W	-	R/W		R/W	

Table 72. DemodReg register bit descriptions

Bit	Symbol	Value	Description
7 to 6	AddIQ [1:0]	-	defines the use of I and Q channel during reception **Remark:** the FixIQ bit must be set to logic 0 to enable the following settings:
		00	selects the stronger channel
		01	selects the stronger channel and freezes the selected channel during communication
		10	reserved
		11	reserved
5	FixIQ	1	if AddIQ[1:0] are set to X0b, the reception is fixed to I channel if AddIQ[1:0] are set to X1b, the reception is fixed to Q channel
4	reserved	-	reserved for future use
3 to 2	TauRcv [1:0]	-	changes the time-constant of the internal PLL during data reception **Remark:** if set to 00b the PLL is frozen during data reception
1 to 0	TauSync [1:0]	-	changes the time constant of the internal PLL during burst

9.3.2.11 Reserved register 1Ah

Functionality is reserved for future use.

Table 73. Reserved register (address 1Ah); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 74. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.2.12 Reserved register 1Bh

Functionality is reserved for future use.

Table 75. Reserved register (address 1Bh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 76. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.2.13 MfTxReg register

Controls some MIFARE communication transmit parameters.

Table 77. MfTxReg register (address 1Ch); reset value: 62h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						TxWait[1:0]	
Access	-						R/W	

Table 78. MfTxReg register bit descriptions

Bit	Symbol	Description
7 to 2	reserved	reserved for future use
1 to 0	TxWait	defines the additional response time 7 bits are added to the value of the register bit by default

9.3.2.14 MfRxReg register

Table 79. MfRxReg register (address 1Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			ParityDisable	reserved			
Access	-			R/W	-			

Table 80. MfRxReg register bit descriptions

Bit	Symbol	Value	Description
7 to 5	reserved	-	reserved for future use
4	ParityDisable	1	generation of the parity bit for transmission and the parity check for receiving is switched off the received parity bit is handled like a data bit
3 to 0	reserved	-	reserved for future use

9.3.2.15 Reserved register 1Eh

Functionality is reserved for future use.

Table 81. Reserved register (address 1Eh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 82. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.2.16 SerialSpeedReg register

Selects the speed of the serial UART interface.

Table 83. SerialSpeedReg register (address 1Fh); reset value: EBh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	BR_T0[2:0]			BR_T1[4:0]				
Access	R/W			R/W				

Table 84. SerialSpeedReg register bit descriptions

Bit	Symbol	Description
7 to 5	BR_T0[2:0]	factor BR_T0 adjusts the transfer speed: for description, see Section 8.1.3.2 on page 11
4 to 0	BR_T1[4:0]	factor BR_T1 adjusts the transfer speed: for description, see Section 8.1.3.2 on page 11

9.3.3 Page 2: Configuration

9.3.3.1 Reserved register 20h

Functionality is reserved for future use.

Table 85. Reserved register (address 20h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-							
Access	reserved							

Table 86. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.3.2 CRCResultReg registers

Shows the MSB and LSB values of the CRC calculation.

Remark: The CRC is split into two 8-bit registers.

Table 87. CRCResultReg (higher bits) register (address 21h); reset value: FFh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultMSB[7:0]							
Access	R							

Table 88. CRCResultReg register higher bit descriptions

Bit	Symbol	Description
7 to 0	CRCResultMSB [7:0]	shows the value of the CRCResultReg register's most significant byte only valid if Status1Reg register's CRCReady bit is set to logic 1

Table 89. CRCResultReg (lower bits) register (address 22h); reset value: FFh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CRCResultLSB[7:0]							
Access	R							

Table 90. CRCResultReg register lower bit descriptions

Bit	Symbol	Description
7 to 0	CRCResultLSB [7:0]	shows the value of the least significant byte of the CRCResultReg register only valid if Status1Reg register's CRCReady bit is set to logic 1

9.3.3.3 Reserved register 23h

Functionality is reserved for future use.

Table 91. Reserved register (address 23h); reset value: 88h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 92. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.3.4 ModWidthReg register

Sets the modulation width.

Table 93. ModWidthReg register (address 24h); reset value: 26h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ModWidth[7:0]							
Access	R/W							

Table 94. ModWidthReg register bit descriptions

Bit	Symbol	Description
7 to 0	ModWidth[7:0]	defines the width of the Miller modulation as multiples of the carrier frequency (ModWidth + 1 / f_{clk}) the maximum value is half the bit period

9.3.3.5 Reserved register 25h

Functionality is reserved for future use.

Table 95. Reserved register (address 25h); reset value: 87h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 96. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.3.6 RFCfgReg register

Configures the receiver gain.

Table 97. RFCfgReg register (address 26h); reset value: 48h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	RxGain[2:0]			reserved			
Access	-	R/W			-			

Table 98. RFCfgReg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for future use
6 to 4	RxGain [2:0]		defines the receiver's signal voltage gain factor:
		000	18 dB
		001	23 dB
		010	18 dB
		011	23 dB
		100	33 dB
		101	38 dB
		110	43 dB
		111	48 dB
3 to 0	reserved	-	reserved for future use

9.3.3.7 GsNReg register

Defines the conductance of the antenna driver pins TX1 and TX2 for the n-driver when the driver is switched on.

Table 99. GsNReg register (address 27h); reset value: 88h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CWGsN[3:0]				ModGsN[3:0]			
Access	R/W				R/W			

Table 100. GsNReg register bit descriptions

Bit	Symbol	Description
7 to 4	CWGsN [3:0]	defines the conductance of the output n-driver during periods without modulation which can be used to regulate the output power and subsequently current consumption and operating distance **Remark:** the conductance value is binary-weighted during soft Power-down mode the highest bit is forced to logic 1 value is only used if driver TX1 or TX2 is switched on
3 to 0	ModGsN [3:0]	defines the conductance of the output n-driver during periods without modulation which can be used to regulate the modulation index **Remark:** the conductance value is binary weighted during soft Power-down mode the highest bit is forced to logic 1 value is only used if driver TX1 or TX2 is switched on

9.3.3.8 CWGsPReg register

Defines the conductance of the p-driver output during periods of no modulation.

Table 101. CWGsPReg register (address 28h); reset value: 20h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		CWGsP[5:0]					
Access	-		R/W					

Table 102. CWGsPReg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	CWGsP[5:0]	defines the conductance of the p-driver output which can be used to regulate the output power and subsequently current consumption and operating distance **Remark:** the conductance value is binary weighted during soft Power-down mode the highest bit is forced to logic 1

9.3.3.9 ModGsPReg register

Defines the conductance of the p-driver output during modulation.

Table 103. ModGsPReg register (address 29h); reset value: 20h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		ModGsP[5:0]					
Access	-		R/W					

Table 104. ModGsPReg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	ModGsP[5:0]	defines the conductance of the p-driver output during modulation which can be used to regulate the modulation index **Remark:** the conductance value is binary weighted during soft Power-down mode the highest bit is forced to logic 1 if the TxASKReg register's Force100ASK bit is set to logic 1 the value of ModGsP has no effect

9.3.3.10 TModeReg and TPrescalerReg registers

These registers define the timer settings.

Remark: The TPrescaler setting higher 4 bits are in the TModeReg register and the lower 8 bits are in the TPrescalerReg register.

Table 105. TModeReg register (address 2Ah); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TAuto	TGated[1:0]		TAutoRestart	TPrescaler_Hi[3:0]			
Access	R/W	R/W		R/W	R/W			

Table 106. TModeReg register bit descriptions

Bit	Symbol	Value	Description
7	TAuto	1	timer starts automatically at the end of the transmission in all communication modes at all speeds if the RxModeReg register's RxMultiple bit is not set, timer stops immediately after receiving the first data bit if the RxMultiple bit is set to logic 1 the timer never stops, in which case the timer can be stopped by setting the ControlReg register's TStopNow bit to logic 1
		0	indicates that the timer is not influenced by the protocol
6 to 5	TGated[1:0]		internal timer is running in gated mode **Remark:** in gated mode, the Status1Reg register's TRunning bit is logic 1 when the timer is enabled by the TModeReg register bits this bit does not influence the gating signal
		00	non-gated mode
		01	gated by pin MFIN
		10	gated by pin AUX1
		11	-
4	TAutoRestart	1	timer automatically restarts its count-down from the 16-bit timer reload value instead of counting down to zero
		0	timer decrements to 0 and the ComIrqReg register's TimerIRq bit is set to logic 1
3 to 0	TPrescaler_Hi [3:0]	-	defines the higher 4 bits of the TPrescaler value the following formula is used to calculate f_{timer}: $f_{timer} = \frac{13.56 \times 10^6}{TPrescaler + 1}$ where 13.56 is the carrier frequency in MHz; for detailed description, see Section 8.5 "Timer unit"

Table 107. TPrescalerReg register (address 2Bh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TPrescaler_Lo[7:0]							
Access	R/W							

Table 108. TPrescalerReg register bit descriptions

Bit	Symbol	Description
7 to 0	TPrescaler_Lo[7:0]	defines the lower 8 bits of the TPrescaler value the following formula is used to calculate f_{timer}: $f_{timer} = \frac{13.56 \times 10^6}{TPrescaler + 1}$ where 13.56 is the carrier frequency in MHz; for detailed description, see Section 8.5 "Timer unit"

9.3.3.11 TReloadReg register

Defines the 16-bit timer reload value.

Remark: The reload value bits are contained in two 8-bit registers.

Table 109. TReloadReg (higher bits) register (address 2Ch); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TReloadVal_Hi[7:0]							
Access	R/W							

Table 110. TReloadReg register higher bit descriptions

Bit	Symbol	Description
7 to 0	TReloadVal_Hi [7:0]	defines the higher 8 bits of the 16-bit timer reload value on a start event, the timer loads the timer reload value changing this register affects the timer only at the next start event

Table 111. TReloadReg (lower bits) register (address 2Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TReloadVal_Lo[7:0]							
Access	R/W							

Table 112. TReloadReg register lower bit descriptions

Bit	Symbol	Description
7 to 0	TReloadVal_Lo [7:0]	defines the lower 8 bits of the 16-bit timer reload value on a start event, the timer loads the timer reload value changing this register affects the timer only at the next start event

9.3.3.12 TCounterValReg register

Contains the timer value.

Remark: The timer value bits are contained in two 8-bit registers.

Table 113. TCounterValReg (higher bits) register (address 2Eh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TCounterVal_Hi[7:0]							
Access	R							

Table 114. TCounterValReg register higher bit descriptions

Bit	Symbol	Description
7 to 0	TCounterVal_Hi [7:0]	timer value higher 8 bits

Table 115. TCounterValReg (lower bits) register (address 2Fh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TCounterVal_Lo[7:0]							
Access	R							

Table 116. TCounterValReg register lower bit descriptions

Bit	Symbol	Description
7 to 0	TCounterVal_Lo [7:0]	timer value lower 8 bits

9.3.4 Page 3: Test

9.3.4.1 Reserved register 30h

Functionality is reserved for future use.

Table 117. Reserved register (address 30h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 118. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for future use

9.3.4.2 TestSel1Reg register

General test signal configuration.

Table 119. TestSel1Reg register (address 31h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved					TstBusBitSel[2:0]		
Access	-					R/W		

Table 120. TestSel1Reg register bit descriptions

Bit	Symbol	Description
7 to 3	reserved	reserved for future use
2 to 0	TstBusBitSel [2:0]	selects a test bus signal which is output at pin MFOUT if AnalogSelAux2[3:0] = FFh in AnalogTestReg register, test bus signal is also output at pins AUX1 or AUX2

9.3.4.3 TestSel2Reg register

General test signal configuration and PRBS control.

Table 121. TestSel2Reg register (address 32h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TstBusFlip	PRBS9	PRBS15	TestBusSel[4:0]				
Access	R/W	R/W	R/W	R/W				

Table 122. TestSel2Reg register bit descriptions

Bit	Symbol	Value	Description
7	TstBusFlip	1	test bus is mapped to the parallel port in the following order: TstBusBit4,TstBusBit3, TstBusBit2, TstBusBit6, TstBusBit5, TstBusBit0; see Section 16.1 on page 79
6	PRBS9	-	starts and enables the PRBS9 sequence according to ITU-TO150 **Remark:** all relevant registers to transmit data must be configured before entering PRBS9 mode the data transmission of the defined sequence is started by the Transmit command
5	PRBS15	-	starts and enables the PRBS15 sequence according to ITU-TO150 **Remark:** all relevant registers to transmit data must be configured before entering PRBS15 mode the data transmission of the defined sequence is started by the Transmit command
4 to 0	TestBusSel [4:0]	-	selects the test bus; see Section 16.1 “Test signals”

9.3.4.4 TestPinEnReg register

Enables the test bus pin output driver.

Table 123. TestPinEnReg register (address 33h); reset value: 80h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RS232LineEn	TestPinEn[5:0]						reserved
Access	R/W	R/W						-

Table 124. TestPinEnReg register bit descriptions

Bit	Symbol	Value	Description
7	RS232LineEn	0	serial UART lines MX and DTRQ are disabled
6 to 1	TestPinEn [5:0]	-	enables the output driver on one of the data pins D1 to D7 which outputs a test signal **Example:** setting bit 1 to logic 1 enables pin D1 output setting bit 5 to logic 1 enables pin D5 output **Remark:** If the SPI is used, only pins D1 to D4 can be used. If the serial UART interface is used and the RS232LineEn bit is set to logic 1 only pins D1 to D4 can be used.
0	reserved	-	reserved for future use

9.3.4.5 TestPinValueReg register

Defines the HIGH and LOW values for the test port D1 to D7 when it is used as I/O.

Table 125. TestPinValueReg register (address 34h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	UseIO	TestPinValue[5:0]						reserved
Access	R/W	R/W						-

Table 126. TestPinValueReg register bit descriptions

Bit	Symbol	Value	Description
7	UseIO	1	enables the I/O functionality for the test port when one of the serial interfaces is used the input/output behavior is defined by value TestPinEn[5:0] in the TestPinEnReg register the value for the output behavior is defined by TestPinValue[5:0]
6 to 1	TestPinValue [5:0]	-	defines the value of the test port when it is used as I/O and each output must be enabled by TestPinEn[5:0] in the TestPinEnReg register **Remark:** Reading the register indicates the status of pins D6 to D1 if the UseIO bit is set to logic 1. If the UseIO bit is set to logic 0, the value of the TestPinValueReg register is read back.
0	reserved	-	reserved for future use

9.3.4.6 TestBusReg register

Shows the status of the internal test bus.

Table 127. TestBusReg register (address 35h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TestBus[7:0]							
Access	R							

Table 128. TestBusReg register bit descriptions

Bit	Symbol	Description
7 to 0	TestBus[7:0]	shows the status of the internal test bus the test bus is selected using the TestSel2Reg register; see Section 16.1 on page 79

9.3.4.7 AutoTestReg register

Controls the digital self-test.

Table 129. AutoTestReg register (address 36h); reset value: 40h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	AmpRcv	RFT		SelfTest[3:0]			
Access	-	R/W	-		R/W			

Table 130. AutoTestReg register bit descriptions

Bit	Symbol	Value	Description
7	reserved	-	reserved for production tests
6	AmpRcv	1	internal signal processing in the receiver chain is performed non-linearly which increases the operating distance in communication modes at 106 kBd **Remark:** due to non-linearity, the effect of the RxThresholdReg register's MinLevel[3:0] and the CollLevel[2:0] values is also non-linear
5 to 4	RFT	-	reserved for production tests
3 to 0	SelfTest [3:0]	-	enables the digital self test the self test can also be started by the CalcCRC command; see Section 10.3.1.4 on page 68 the self test is enabled by 1001b **Remark:** for default operation the self test must be disabled by 0000b

9.3.4.8 VersionReg register

Shows the MFRC522 software version.

Table 131. VersionReg register (address 37h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	Version[7:0]							
Access	R							

Table 132. VersionReg register bit descriptions

Bit	Symbol	Description
7 to 0	Version[7:0]	indicates current software version of the MFRC522 **Remark:** the current version of the MFRC522 is 90h or 91h

9.3.4.9 AnalogTestReg register

Determines the analog output test signal at, and status of, pins AUX1 and AUX2.

Table 133. AnalogTestReg register (address 38h); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	AnalogSelAux1[3:0]				AnalogSelAux2[3:0]			
Access	R/W				R/W			

Table 134. AnalogTestReg register bit descriptions

Bit	Symbol	Value	Description
7 to 4	AnalogSelAux1 [3:0]		controls pin AUX1
		0000	3-state
		0001	output of TestDAC1 (AUX1), output of TestDAC2 (AUX2)[1]
		0010	test signal Corr1[1]
		0011	reserved
		0100	DAC: test signal MinLevel[1]
		0101	DAC: test signal ADC_I[1]
		0110	DAC: test signal ADC_Q[1]
		0111	reserved
		1000	reserved, test signal for production test[1]
		1001	reserved
		1010	HIGH
		1011	LOW
		1100	TxActive: at 106 kBd: HIGH during Start bit, Data bit, Parity and CRC at 212 kBd: 424 kBd and 848 kBd: HIGH during data and CRC
		1101	RxActive: at 106 kBd: HIGH during Data bit, Parity and CRC at 212 kBd: 424 kBd and 848 kBd: HIGH during data and CRC
		1110	subcarrier detected: 106 kBd: not applicable 212 kBd: 424 kBd and 848 kBd: HIGH during last part of data and CRC
		1111	test bus bit as defined by the TestSel1Reg register's TstBusBitSel[2:0] bits **Remark:** all test signals are described in Section 16.1 on page 79
3 to 0	AnalogSelAux2 [3:0]	-	controls pin AUX2 (see bit descriptions for AUX1)

[1] **Remark:** Current source output; the use of 1 kΩ pull-down resistor on AUXn is recommended.

9.3.4.10 TestDAC1Reg register

Defines the test value for TestDAC1.

Table 135. TestDAC1Reg register (address 39h); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		TestDAC1[5:0]					
Access	-		R/W					

Table 136. TestDAC1Reg register bit descriptions

Bit	Symbol	Description
7	reserved	reserved for production tests
6	reserved	reserved for future use
5 to 0	TestDAC1[5:0]	defines the test value for TestDAC1 output of DAC1 can be routed to AUX1 by setting value AnalogSelAux1[3:0] to 0001b in the AnalogTestReg register

9.3.4.11 TestDAC2Reg register

Defines the test value for TestDAC2.

Table 137. TestDAC2Reg register (address 3Ah); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		TestDAC2[5:0]					
Access	-		R/W					

Table 138. TestDAC2Reg register bit descriptions

Bit	Symbol	Description
7 to 6	reserved	reserved for future use
5 to 0	TestDAC2[5:0]	defines the test value for TestDAC2 output of DAC2 can be routed to AUX2 by setting value AnalogSelAux2[3:0] to 0001b in the AnalogTestReg register

9.3.4.12 TestADCReg register

Shows the values of ADC I and Q channels.

Table 139. TestADCReg register (address 3Bh); reset value: xxh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ADC_I[3:0]				ADC_Q[3:0]			
Access	R				R			

Table 140. TestADCReg register bit descriptions

Bit	Symbol	Description
7 to 4	ADC_I[3:0]	ADC I channel value
3 to 0	ADC_Q[3:0]	ADC Q channel value

9.3.4.13 Reserved register 3Ch

Functionality reserved for production test.

Table 141. Reserved register (address 3Ch); reset value: FFh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RFT							
Access	-							

Table 142. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

Table 143. Reserved register (address 3Dh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RFT							
Access	-							

Table 144. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

Table 145. Reserved register (address 3Eh); reset value: 03h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RFT							
Access	-							

Table 146. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

Table 147. Reserved register (address 3Fh); reset value: 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Access	-							

Table 148. Reserved register bit descriptions

Bit	Symbol	Description
7 to 0	reserved	reserved for production tests

10. MFRC522 command set

10.1 General description

The MFRC522 operation is determined by a state machine capable of performing a set of commands. A command is executed by writing a command code (see Table 149) to the CommandReg register.

Arguments and/or data necessary to process a command are exchanged via the FIFO buffer.

10.2 General behavior

- Each command that needs a data bit stream (or data byte stream) as an input immediately processes any data in the FIFO buffer. An exception to this rule is the Transceive command. Using this command, transmission is started with the BitFramingReg register's StartSend bit.
- Each command that needs a certain number of arguments, starts processing only when it has received the correct number of arguments from the FIFO buffer.
- The FIFO buffer is not automatically cleared when commands start. This makes it possible to write command arguments and/or the data bytes to the FIFO buffer and then start the command.
- Each command can be interrupted by the host writing a new command code to the CommandReg register, for example, the Idle command.

10.3 MFRC522 command overview

Table 149. Command overview

Command	Command code	Action
Idle	0000	no action, cancels current command execution
Mem	0001	stores 25 bytes into the internal buffer
Generate RandomID	0010	generates a 10-byte random ID number
CalcCRC	0011	activates the CRC coprocessor or performs a self test
Transmit	0100	transmits data from the FIFO buffer
NoCmdChange	0111	no command change, can be used to modify the CommandReg register bits without affecting the command, for example, the PowerDown bit
Receive	1000	activates the receiver circuits
Transceive	1100	transmits data from FIFO buffer to antenna and automatically activates the receiver after transmission
-	1101	reserved for future use
MFAuthent	1110	performs the MIFARE standard authentication as a reader
SoftReset	1111	resets the MFRC522

10.3.1 MFRC522 command descriptions

10.3.1.1 Idle

Places the MFRC522 in Idle mode. The Idle command also terminates itself.

10.3.1.2 Mem

Transfers 25 bytes from the FIFO buffer to the internal buffer.

To read out the 25 bytes from the internal buffer the Mem command must be started with an empty FIFO buffer. In this case, the 25 bytes are transferred from the internal buffer to the FIFO.

During a hard power-down (using pin NRSTPD), the 25 bytes in the internal buffer remain unchanged and are only lost if the power supply is removed from the MFRC522.

This command automatically terminates when finished and the Idle command becomes active.

10.3.1.3 Generate RandomID

This command generates a 10-byte random number which is initially stored in the internal buffer. This then overwrites the 10 bytes in the internal 25-byte buffer. This command automatically terminates when finished and the MFRC522 returns to Idle mode.

10.3.1.4 CalcCRC

The FIFO buffer content is transferred to the CRC coprocessor and the CRC calculation is started. The calculation result is stored in the CRCResultReg register. The CRC calculation is not limited to a dedicated number of bytes. The calculation is not stopped when the FIFO buffer is empty during the data stream. The next byte written to the FIFO buffer is added to the calculation.

The CRC preset value is controlled by the ModeReg register's CRCPreset[1:0] bits. The value is loaded in to the CRC coprocessor when the command starts.

This command must be terminated by writing a command to the CommandReg register, such as, the Idle command.

If the AutoTestReg register's SelfTest[3:0] bits are set correctly, the MFRC522 enters Self Test mode. Starting the CalcCRC command initiates a digital self test. The result of the self test is written to the FIFO buffer.

10.3.1.5 Transmit

The FIFO buffer content is immediately transmitted after starting this command. Before transmitting the FIFO buffer content, all relevant registers must be set for data transmission.

This command automatically terminates when the FIFO buffer is empty. It can be terminated by another command written to the CommandReg register.

10.3.1.6 NoCmdChange

This command does not influence any running command in the CommandReg register. It can be used to manipulate any bit except the CommandReg register Command[3:0] bits, for example, the RcvOff bit or the PowerDown bit.

10.3.1.7 Receive

The MFRC522 activates the receiver path and waits for a data stream to be received. The correct settings must be chosen before starting this command.

This command automatically terminates when the data stream ends. This is indicated either by the end of frame pattern or by the length byte depending on the selected frame type and speed.

Remark: If the RxModeReg register's RxMultiple bit is set to logic 1, the Receive command will not automatically terminate. It must be terminated by starting another command in the CommandReg register.

10.3.1.8 Transceive

This command continuously repeats the transmission of data from the FIFO buffer and the reception of data from the RF field. The first action is transmit and after transmission the command is changed to receive a data stream.

Each transmit process must be started by setting the BitFramingReg register's StartSend bit to logic 1. This command must be cleared by writing any command to the CommandReg register.

Remark: If the RxModeReg register's RxMultiple bit is set to logic 1, the Transceive command never leaves the receive state because this state cannot be cancelled automatically.

10.3.1.9 MFAuthent

This command manages MIFARE authentication to enable a secure communication to any MIFARE Mini, MIFARE 1K and MIFARE 4K card. The following data is written to the FIFO buffer before the command can be activated:

- Authentication command code (60h, 61h)
- Block address
- Sector key byte 0
- Sector key byte 1
- Sector key byte 2
- Sector key byte 3
- Sector key byte 4
- Sector key byte 5
- Card serial number byte 0
- Card serial number byte 1
- Card serial number byte 2
- Card serial number byte 3

In total 12 bytes are written to the FIFO.

Remark: When the MFAuthent command is active all access to the FIFO buffer is blocked. However, if there is access to the FIFO buffer, the ErrorReg register's WrErr bit is set.

This command automatically terminates when the MIFARE card is authenticated and the Status2Reg register's MFCrypto1On bit is set to logic 1.

This command does not terminate automatically if the card does not answer, so the timer must be initialized to automatic mode. In this case, in addition to the IdleIRq bit, the TimerIRq bit can be used as the termination criteria. During authentication processing, the RxIRq bit and TxIRq bit are blocked. The Crypto1On bit is only valid after termination of the MFAuthent command, either after processing the protocol or writing Idle to the CommandReg register.

If an error occurs during authentication, the ErrorReg register's ProtocolErr bit is set to logic 1 and the Status2Reg register's Crypto1On bit is set to logic 0.

10.3.1.10 SoftReset

This command performs a reset of the device. The configuration data of the internal buffer remains unchanged. All registers are set to the reset values. This command automatically terminates when finished.

Remark: The SerialSpeedReg register is reset and therefore the serial data rate is set to 9.6 kBd.

11. Limiting values

Table 150. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage		–0.5	+4.0	V
V_{DDD}	digital supply voltage		–0.5	+4.0	V
$V_{DD(PVDD)}$	PVDD supply voltage		–0.5	+4.0	V
$V_{DD(TVDD)}$	TVDD supply voltage		–0.5	+4.0	V
$V_{DD(SVDD)}$	SVDD supply voltage		–0.5	+4.0	V
V_I	input voltage	all input pins except pins MFIN and RX	$V_{SS(PVSS)}$ – 0.5	$V_{DD(PVDD)}$ + 0.5	V
		pin MFIN	$V_{SS(PVSS)}$ – 0.5	$V_{DD(SVDD)}$ + 0.5	V
P_{tot}	total power dissipation	per package; and V_{DDD} in shortcut mode	-	200	mW
T_j	junction temperature		-	100	°C
V_{ESD}	electrostatic discharge voltage	HBM; 1500 Ω, 100 pF; JESD22-A114-B	-	2000	V
		MM; 0.75 µH, 200 pF; JESD22-A114-A	-	200	V

12. Recommended operating conditions

Table 151. Operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	analog supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
V_{DDD}	digital supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
$V_{DD(TVDD)}$	TVDD supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[1][2]	2.5	3.3	3.6	V
$V_{DD(PVDD)}$	PVDD supply voltage	$V_{DD(PVDD)} \leq V_{DDA} = V_{DDD} = V_{DD(TVDD)}$; $V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V	[3]	1.6	1.8	3.6	V
$V_{DD(SVDD)}$	SVDD supply voltage	$V_{SSA} = V_{SSD} = V_{SS(PVSS)} = V_{SS(TVSS)} = 0$ V		1.6	-	3.6	V
T_{amb}	ambient temperature	HVQFN32		–25	-	+85	°C

[1] Supply voltages below 3 V reduce the performance (the achievable operating distance).

[2] V_{DDA}, V_{DDD} and $V_{DD(TVDD)}$ must always be the same voltage.

[3] $V_{DD(PVDD)}$ must always be the same or lower voltage than V_{DDD}.

13. Thermal characteristics

Table 152. Thermal characteristics

Symbol	Parameter	Conditions	Package	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in still air with exposed pin soldered on a 4 layer JEDEC PCB	HVQFN32	40	K/W

14. Characteristics

Table 153. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input characteristics						
Pins EA, I2C and NRSTPD						
I_{LI}	input leakage current		−1	-	+1	µA
V_{IH}	HIGH-level input voltage		$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(PVDD)}$	V
Pin MFIN						
I_{LI}	input leakage current		−1	-	+1	µA
V_{IH}	HIGH-level input voltage		$0.7V_{DD(SVDD)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(SVDD)}$	V
Pin SDA						
I_{LI}	input leakage current		−1	-	+1	µA
V_{IH}	HIGH-level input voltage		$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(PVDD)}$	V
Pin RX[1]						
V_i	input voltage		−1	-	V_{DDA} +1	V
C_i	input capacitance	V_{DDA} = 3 V; receiver active; $V_{RX(p-p)}$ = 1 V; 1.5 V (DC) offset	-	10	-	pF
R_i	input resistance	V_{DDA} = 3 V; receiver active; $V_{RX(p-p)}$ = 1 V; 1.5 V (DC) offset	-	350	-	Ω
Input voltage range; see Figure 24						
$V_{i(p-p)(min)}$	minimum peak-to-peak input voltage	Manchester encoded; V_{DDA} = 3 V	-	100	-	mV
$V_{i(p-p)(max)}$	maximum peak-to-peak input voltage	Manchester encoded; V_{DDA} = 3 V	-	4	-	V
Input sensitivity; see Figure 24						
V_{mod}	modulation voltage	minimum Manchester encoded; V_{DDA} = 3 V; RxGain[2:0] = 111b (48 dB)	-	5	-	mV
Pin OSCIN						
I_{LI}	input leakage current		−1	-	+1	µA
V_{IH}	HIGH-level input voltage		$0.7V_{DDA}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DDA}$	V
C_i	input capacitance	V_{DDA} = 2.8 V; DC = 0.65 V; AC = 1 V (p-p)	-	2	-	pF
Input/output characteristics						
pins D1, D2, D3, D4, D5, D6 and D7						
I_{LI}	input leakage current		−1	-	+1	µA
V_{IH}	HIGH-level input voltage		$0.7V_{DD(PVDD)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD(PVDD)}$	V

Table 153. Characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA	$V_{DD(PVDD)}$ − 0.4	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA	$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$ = 3 V	-	-	4	mA
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$ = 3 V	-	-	4	mA
Output characteristics						
Pin MFOUT						
V_{OH}	HIGH-level output voltage	$V_{DD(SVDD)}$ = 3 V; I_O = 4 mA	$V_{DD(SVDD)}$ − 0.4	-	$V_{DD(SVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(SVDD)}$ = 3 V; I_O = 4 mA	$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OL}	LOW-level output current	$V_{DD(SVDD)}$ = 3 V	-	-	4	mA
I_{OH}	HIGH-level output current	$V_{DD(SVDD)}$ = 3 V	-	-	4	mA
Pin IRQ						
V_{OH}	HIGH-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA	$V_{DD(PVDD)}$ − 0.4	-	$V_{DD(PVDD)}$	V
V_{OL}	LOW-level output voltage	$V_{DD(PVDD)}$ = 3 V; I_O = 4 mA	$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OL}	LOW-level output current	$V_{DD(PVDD)}$ = 3 V	-	-	4	mA
I_{OH}	HIGH-level output current	$V_{DD(PVDD)}$ = 3 V	-	-	4	mA
Pins AUX1 and AUX2						
V_{OH}	HIGH-level output voltage	V_{DDD} = 3 V; I_O = 4 mA	V_{DDD} − 0.4	-	V_{DDD}	V
V_{OL}	LOW-level output voltage	V_{DDD} = 3 V; I_O = 4 mA	$V_{SS(PVSS)}$	-	$V_{SS(PVSS)}$ + 0.4	V
I_{OL}	LOW-level output current	V_{DDD} = 3 V	-	-	4	mA
I_{OH}	HIGH-level output current	V_{DDD} = 3 V	-	-	4	mA
Pins TX1 and TX2						
V_{OH}	HIGH-level output voltage	$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 3Fh	$V_{DD(TVDD)}$ − 0.15	-	-	V
		$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 3Fh	$V_{DD(TVDD)}$ − 0.4	-	-	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 3Fh	$V_{DD(TVDD)}$ − 0.24	-	-	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 3Fh	$V_{DD(TVDD)}$ − 0.64	-	-	V

Table 153. Characteristics *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 0Fh		-	-	0.15	V
		$V_{DD(TVDD)}$ = 3 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 0Fh		-	-	0.4	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 32 mA; CWGsP[5:0] = 0Fh		-	-	0.24	V
		$V_{DD(TVDD)}$ = 2.5 V; $I_{DD(TVDD)}$ = 80 mA; CWGsP[5:0] = 0Fh		-	-	0.64	V
Current consumption							
I_{pd}	power-down current	$V_{DDA} = V_{DDD} = V_{DD(TVDD)} = V_{DD(PVDD)}$ = 3 V					
		hard power-down; pin NRSTPD set LOW	[2]	-	-	5	µA
		soft power-down; RF level detector on	[2]	-	-	10	µA
I_{DDD}	digital supply current	pin DVDD; V_{DDD} = 3 V		-	6.5	9	mA
I_{DDA}	analog supply current	pin AVDD; V_{DDA} = 3 V; bit RcvOff = 0		-	7	10	mA
		pin AVDD; receiver switched off; V_{DDA} = 3 V; bit RcvOff = 1		-	3	5	mA
$I_{DD(PVDD)}$	PVDD supply current	pin PVDD	[3]	-	-	40	mA
$I_{DD(TVDD)}$	TVDD supply current	pin TVDD; continuous wave	[4][5][6]	-	60	100	mA
$I_{DD(SVDD)}$	SVDD supply current	pin SVDD	[7]	-	-	4	mA
Clock frequency							
f_{clk}	clock frequency			-	27.12	-	MHz
δ_{clk}	clock duty cycle			40	50	60	%
t_{jit}	jitter time	RMS		-	-	10	ps
Crystal oscillator							
V_{OH}	HIGH-level output voltage	pin OSCOUT		-	1.1	-	V
V_{OL}	LOW-level output voltage	pin OSCOUT		-	0.2	-	V
C_i	input capacitance	pin OSCOUT		-	2	-	pF
		pin OSCIN		-	2	-	pF
Typical input requirements							
f_{xtal}	crystal frequency			-	27.12	-	MHz
ESR	equivalent series resistance			-	-	100	Ω
C_L	load capacitance			-	10	-	pF
P_{xtal}	crystal power dissipation			-	50	100	mW

[1] The voltage on pin RX is clamped by internal diodes to pins AVSS and AVDD.

[2] I_{pd} is the total current for all supplies.

[3] $I_{DD(PVDD)}$ depends on the overall load at the digital pins.

[4] $I_{DD(TVDD)}$ depends on $V_{DD(TVDD)}$ and the external circuit connected to pins TX1 and TX2.

[5] During typical circuit operation, the overall current is below 100 mA.

[6] Typical value using a complementary driver configuration and an antenna matched to 40 Ω between pins TX1 and TX2 at 13.56 MHz.

[7] $I_{DD(SVDD)}$ depends on the load at pin MFOUT.

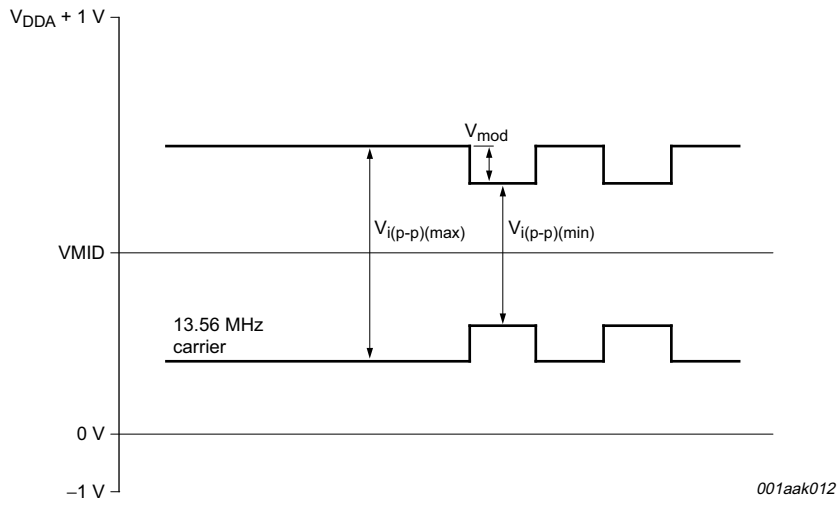


Fig 24. Pin RX input voltage range

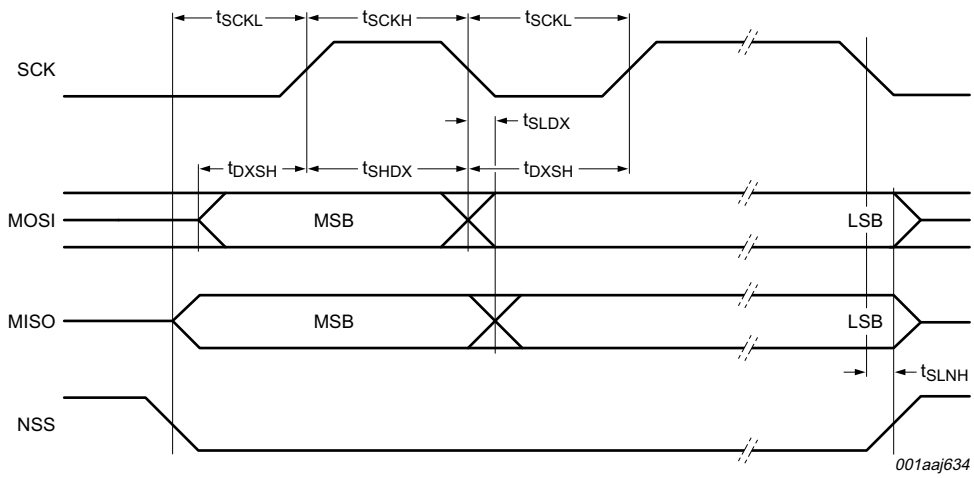
14.1 Timing characteristics

Table 154. SPI timing characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WL}	pulse width LOW	line SCK	50	-	-	ns
t_{WH}	pulse width HIGH	line SCK	50	-	-	ns
$t_{h(SCKH-D)}$	SCK HIGH to data input hold time	SCK to changing MOSI	25	-	-	ns
$t_{su(D-SCKH)}$	data input to SCK HIGH set-up time	changing MOSI to SCK	25	-	-	ns
$t_{h(SCKL-Q)}$	SCK LOW to data output hold time	SCK to changing MISO	-	-	25	ns
$t_{(SCKL-NSSH)}$	SCK LOW to NSS HIGH time		0	-	-	ns

Table 155. I^2C-bus timing in Fast mode

Symbol	Parameter	Conditions	Fast mode		High-speed mode		Unit
			Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	400	0	3400	kHz
$t_{HD;STA}$	hold time (repeated) START condition	after this period, the first clock pulse is generated	600	-	160	-	ns
$t_{SU;STA}$	set-up time for a repeated START condition		600	-	160	-	ns
$t_{SU;STO}$	set-up time for STOP condition		600	-	160	-	ns
t_{LOW}	LOW period of the SCL clock		1300	-	160	-	ns
t_{HIGH}	HIGH period of the SCL clock		600	-	60	-	ns
$t_{HD;DAT}$	data hold time		0	900	0	70	ns
$t_{SU;DAT}$	data set-up time		100	-	10	-	ns
t_r	rise time	SCL signal	20	300	10	40	ns
t_f	fall time	SCL signal	20	300	10	40	ns
t_r	rise time	SDA and SCL signals	20	300	10	80	ns
t_f	fall time	SDA and SCL signals	20	300	10	80	ns
t_{BUF}	bus free time between a STOP and START condition		1.3	-	1.3	-	µs



Remark: The signal NSS must be LOW to be able to send several bytes in one data stream. To send more than one data stream NSS must be set HIGH between the data streams.

Fig 25. Timing diagram for SPI

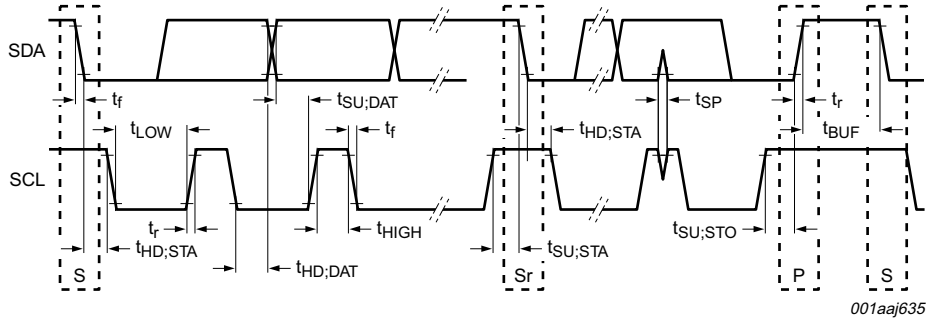


Fig 26. Timing for Fast and Standard mode devices on the I^2C-bus

15. Application information

A typical application diagram using a complementary antenna connection to the MFRC522 is shown in Figure 27.

The antenna tuning and RF part matching is described in the application note Ref. 1 and Ref. 2.

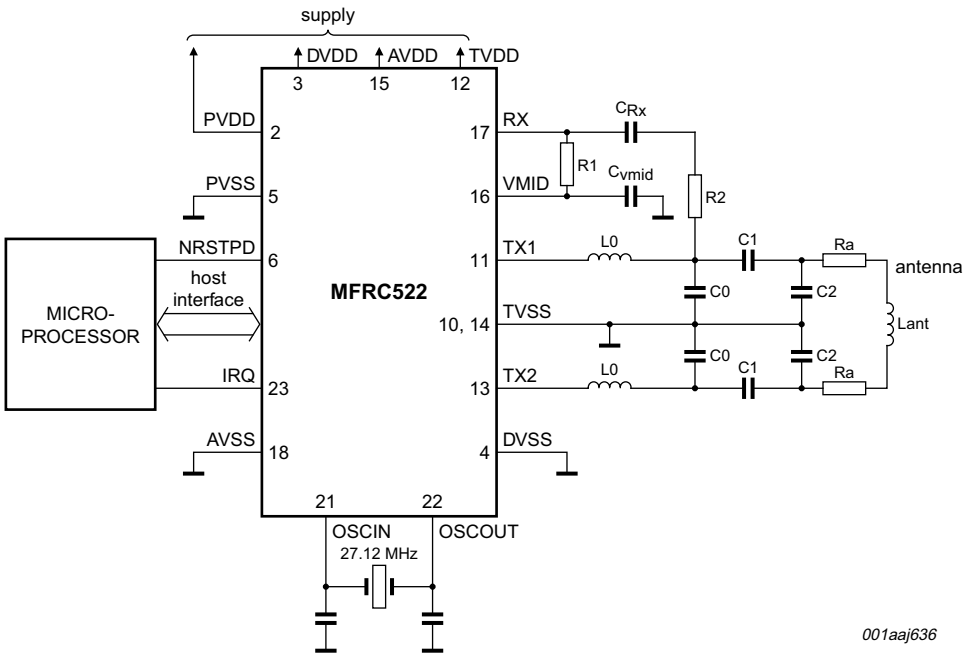


Fig 27. Typical application diagram

16. Test information

16.1 Test signals

16.1.1 Self test

The MFRC522 has the capability to perform a digital self test. The self test is started by using the following procedure:

1. Perform a soft reset.
2. Clear the internal buffer by writing 25 bytes of 00h and implement the Config command.
3. Enable the self test by writing 09h to the AutoTestReg register.
4. Write 00h to the FIFO buffer.
5. Start the self test with the CalcCRC command.
6. The self test is initiated.
7. When the self test has completed, the FIFO buffer contains the following 64 bytes:

FIFO buffer byte values for version 90h:

```
00h, 87h, 98h, 0fh, 49h, FFh, 07h, 19h
BFh, 22h, 30h, 49h, 59h, 63h, ADh, CAh
7Fh, E3h, 4Eh, 03h, 5Ch, 4Eh, 49h, 50h
47h, 9Ah, 37h, 61h, E7h, E2h, C6h, 2Eh
75h, 5Ah, EDh, 04h, 3Dh, 02h, 4Bh, 78h
32h, FFh, 58h, 3Bh, 7Ch, E9h, 00h, 94h
B4h, 4Ah, 59h, 5Bh, FDh, U9h, 29h, DFh
35h, 96h, 98h, 9Eh, 4Fh, 30h, 32h, 8Dh
```

FIFO buffer byte values for version 91h:

```
00h, C6h, 37h, D5h, 32h, B7h, 57h, 5Ch
C2h, D8h, 7Ch, 4Dh, D9h, 70h, C7h, 73h
10h, E6h, D2h, AAh, 5Eh, A1h, 3Eh, 5Ah
14h, AFh, 30h, 61h, C9h, 70h, DBh, 2Eh
64h, 22h, 72h, B5h, BDh, 65h, F4h, ECh
22h, BCh, D3h, 72h, 35h, CDh, AAh, 41h
1Fh, A7h, F3h, 53h, 14h, DEh, 7Eh, 02h
D9h, 0Fh, B5h, 5Eh, 25h, 1Dh, 29h, 79h
```

16.1.2 Test bus

The test bus is used for production tests. The following configuration can be used to improve the design of a system using the MFRC522. The test bus allows internal signals to be routed to the digital interface. The test bus comprises two sets of test signals which are selected using their subaddress specified in the TestSel2Reg register's TestBusSel[4:0] bits. The test signals and their related digital output pins are described in Table 156 and Table 157.

Table 156. Test bus signals: TestBusSel[4:0] = 07h

Pins	Internal signal name	Description
D6	s_data	received data stream
D5	s_coll	bit-collision detected (106 kBd only)
D4	s_valid	s_data and s_coll signals are valid
D3	s_over	receiver has detected a stop condition
D2	RCV_reset	receiver is reset
D1	-	reserved

Table 157. Test bus signals: TestBusSel[4:0] = 0Dh

Pins	Internal test signal name	Description
D6	clkstable	oscillator output signal
D5	clk27/8	oscillator output signal divided by 8
D4 to D3	-	reserved
D2	clk27	oscillator output signal
D1	-	reserved

16.1.3 Test signals on pins AUX1 or AUX2

The MFRC522 allows the user to select internal signals for measurement on pins AUX1 or AUX2. These measurements can be helpful during the design-in phase to optimize the design or used for test purposes.

Table 158 shows the signals that can be switched to pin AUX1 or AUX2 by setting AnalogSelAux1[3:0] or AnalogSelAux2[3:0] in the AnalogTestReg register.

Remark: The DAC has a current output, therefore it is recommended that a 1 kΩ pull-down resistor is connected to pin AUX1 or AUX2.

Table 158. Test signal descriptions

AnalogSelAux1[3:0] or AnalogSelAux2[3:0] value	Signal on pin AUX1 or pin AUX2
0000	3-state
0001	DAC: register TestDAC1 or TestDAC2
0010	DAC: test signal Corr1
0011	reserved
0100	DAC: test signal MinLevel
0101	DAC: test signal ADC_I
0110	DAC: test signal ADC_Q
0111 to 1001	reserved
1010	HIGH
1011	LOW
1100	TxActive

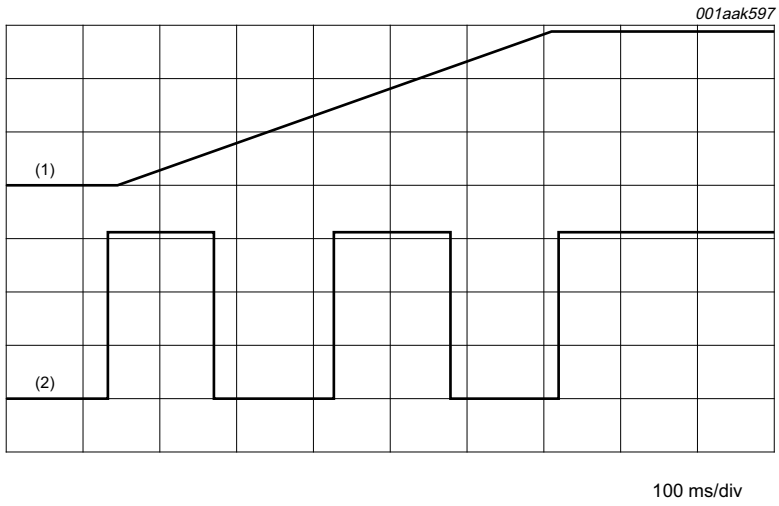
Table 158. Test signal descriptions …continued

AnalogSelAux1[3:0] or AnalogSelAux2[3:0] value	Signal on pin AUX1 or pin AUX2
1101	RxActive
1110	subcarrier detected
1111	TstBusBit

16.1.3.1 Example: Output test signals TestDAC1 and TestDAC2

The AnalogTestReg register is set to 11h. The output on pin AUX1 has the test signal TestDAC1 and the output on pin AUX2 has the test signal TestDAC2. The signal values of TestDAC1 and TestDAC2 are controlled by the TestDAC1Reg and TestDAC2Reg registers.

Figure 28 shows test signal TestDAC1 on pin AUX1 and TestDAC2 on pin AUX2 when the TestDAC1Reg register is programmed with a slope defined by values 00h to 3Fh and the TestDAC2Reg register is programmed with a rectangular signal defined by values 00h and 3Fh.



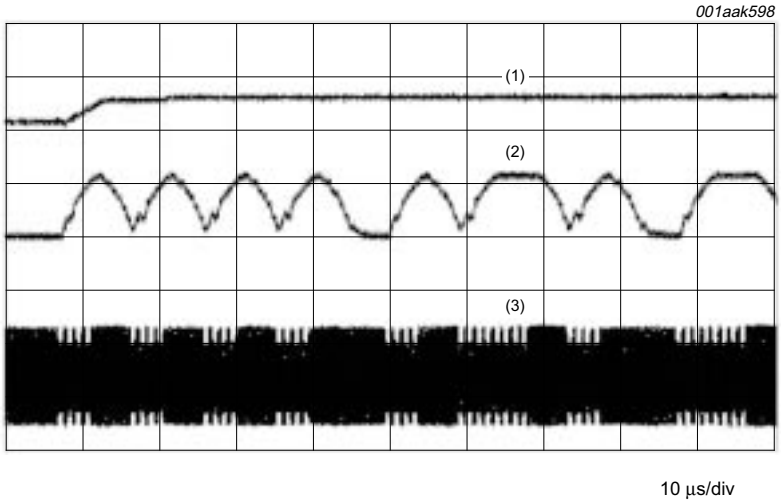
(1) TestDAC1 (500 mV/div) on pin AUX1.

(2) TestDAC2 (500 mV/div) on pin AUX2.

Fig 28. Output test signals TestDAC1 on pin AUX1 and TestDAC2 on pin AUX2

16.1.3.2 Example: Output test signals Corr1 and MinLevel

Figure 29 shows test signals Corr1 and MinLevel on pins AUX1 and AUX2, respectively. The AnalogTestReg register is set to 24h.

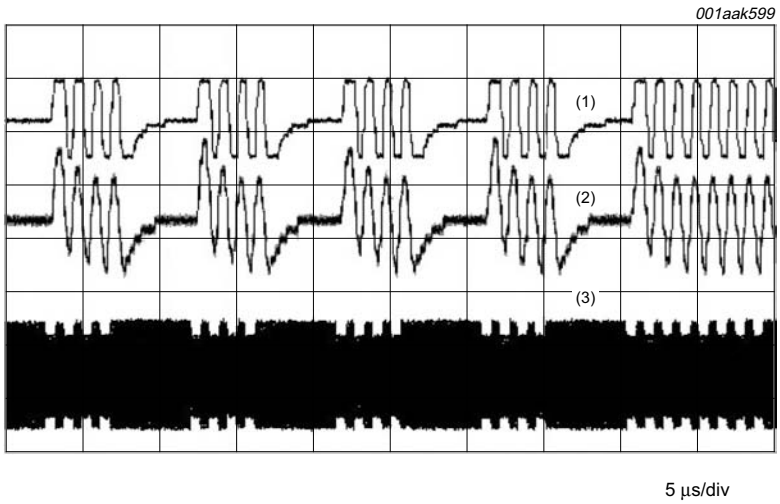


(1) MinLevel (1 V/div) on pin AUX2.
(2) Corr1 (1 V/div) on pin AUX1.
(3) RF field.

Fig 29. Output test signals Corr1 on pin AUX1 and MinLevel on pin AUX2

16.1.3.3 Example: Output test signals ADC channel I and ADC channel Q

Figure 30 shows the channel behavior test signals ADC_I and ADC_Q on pins AUX1 and AUX2, respectively. The AnalogTestReg register is set to 56h.



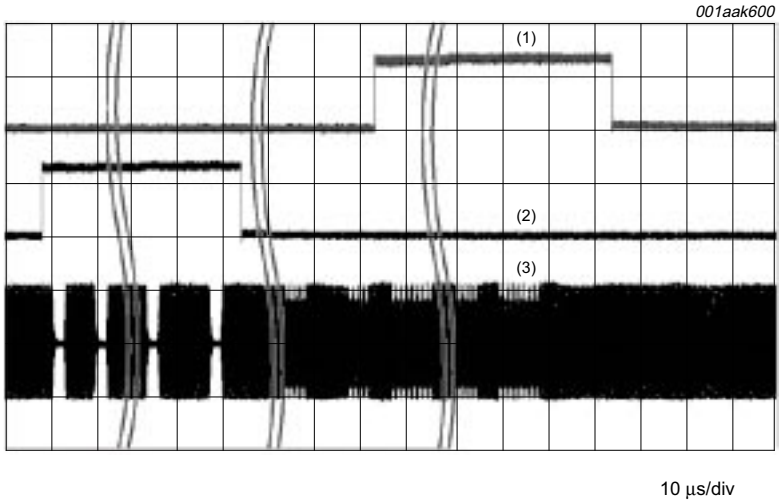
(1) ADC_I (1 V/div) on pin AUX1.
(2) ADC_Q (500 mV/div) on pin AUX2.
(3) RF field.

Fig 30. Output ADC channel I on pin AUX1 and ADC channel Q on pin AUX2

16.1.3.4 Example: Output test signals RxActive and TxActive

Figure 31 shows the RxActive and TxActive test signals relating to RF communication. The AnalogTestReg register is set to CDh.

- At 106 kBd, RxActive is HIGH during data bits, parity and CRC reception. Start bits are not included
- At 106 kBd, TxActive is HIGH during start bits, data bits, parity and CRC transmission
- At 212 kBd, 424 kBd and 848 kBd, RxActive is HIGH during data bits and CRC reception. Start bits are not included
- At 212 kBd, 424 kBd and 848 kBd, TxActive is HIGH during data bits and CRC transmission

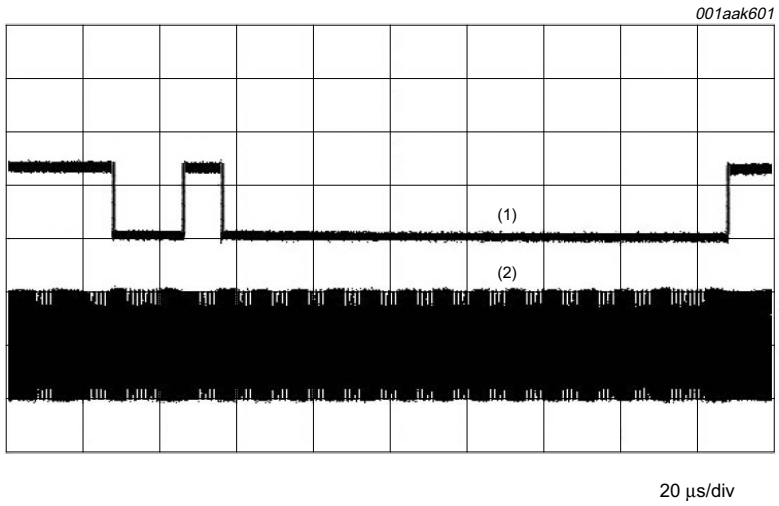


(1) RxActive (2 V/div) on pin AUX1.
(2) TxActive (2 V/div) on pin AUX2.
(3) RF field.

Fig 31. Output RxActive on pin AUX1 and TxActive on pin AUX2

16.1.3.5 Example: Output test signal RX data stream

Figure 32 shows the data stream that is currently being received. The TestSel2Reg register's TestBusSel[4:0] bits are set to 07h to enable test bus signals on pins D1 to D6; see Section 16.1.2 on page 79. The TestSel1Reg register's TstBusBitSel[2:0] bits are set 06h (pin D6 = s_data) and AnalogTestReg register is set to FFh (TstBusBit) which outputs the received data stream on pins AUX1 and AUX2.



(1) s_data (received data stream) (2 V/div).

(2) RF field.

Fig 32. Received data stream on pins AUX1 and AUX2

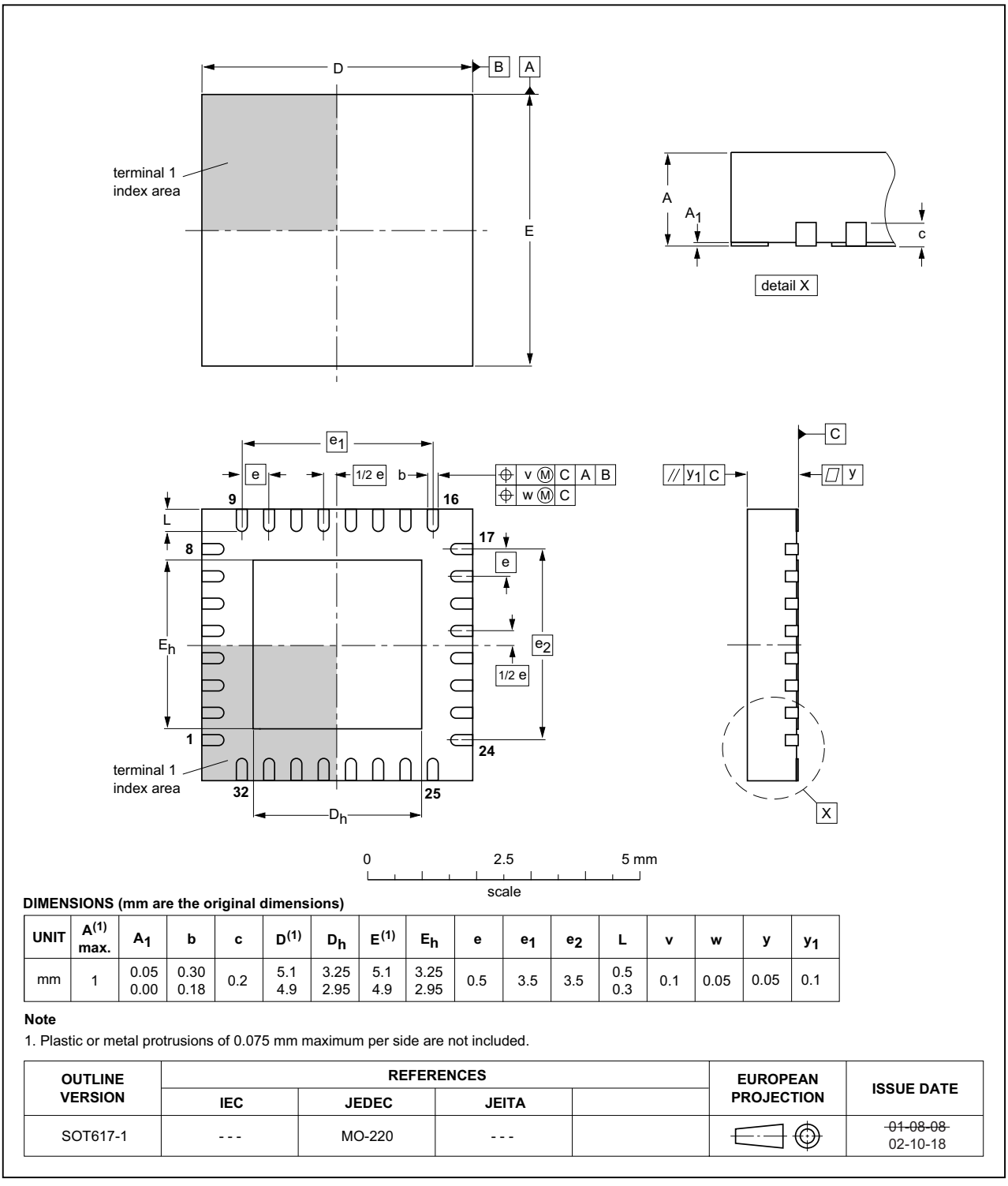
16.1.3.6 PRBS

The pseudo-random binary sequences PRBS9 and PRBS15 are based on ITU-TO150 and are defined with the TestSel2Reg register. Transmission of either data stream is started by the Transmit command. The preamble/sync byte/start bit/parity bit are automatically generated depending on the mode selected.

Remark: All relevant registers for transmitting data must be configured in accordance with ITU-TO150 before selecting PRBS transmission.

17. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 33. Package outline SOT617-1 (HVQFN32)

Detailed package information can be found at:
http://www.nxp.com/package/SOT617-1.html.

18. Handling information

Moisture Sensitivity Level (MSL) evaluation has been performed according to *SNW-FQ-225B rev.04/07/07 (JEDEC J-STD-020C)*. MSL for this package is level 1 which means 260 °C convection reflow temperature.

Dry pack is not required.

Unlimited out-of-pack floor life at maximum ambient 30 °C/85 % RH.

19. Packing information

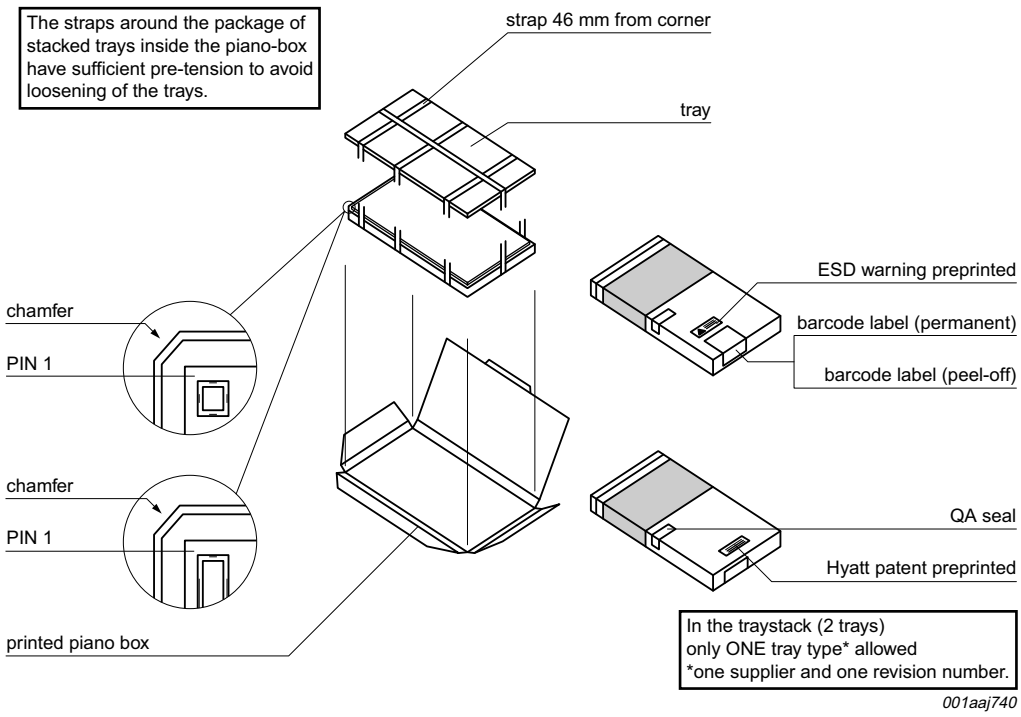


Fig 34. Packing information 1 tray

20. Abbreviations

Table 159. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
BPSK	Binary Phase Shift Keying
CRC	Cyclic Redundancy Check
CW	Continuous Wave
DAC	Digital-to-Analog Converter
HBM	Human Body Model
I^2C	Inter-integrated Circuit
LSB	Least Significant Bit
MISO	Master In Slave Out
MM	Machine Model
MOSI	Master Out Slave In
MSB	Most Significant Bit
NRZ	Not Return to Zero
NSS	Not Slave Select
PLL	Phase-Locked Loop
PRBS	Pseudo-Random Bit Sequence
RX	Receiver
SOF	Start Of Frame
SPI	Serial Peripheral Interface
TX	Transmitter
UART	Universal Asynchronous Receiver Transmitter

21. References

[1] **Application note** — *MFRC52x Reader IC Family Directly Matched Antenna Design*

[2] **Application note** — *MIFARE (ISO/IEC 14443 A) 13.56 MHz RFID Proximity Antennas*

22. Revision history

Table 160. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MFRC522_33	20091026	Product data sheet	-	112132
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • General re-wording of MIFARE designation and commercial conditions. • Table 106 “TModeReg register bit descriptions” and Table 108 “TPrescalerReg register bit descriptions”: changed value "f_{Timer} = 13.56 MHz / (TPreScaler + 1)" • Graphics: updated to latest standard • Descriptive text: updated • Register and bit names: updated • Register tables: presentation updated • Parameter symbols: updated • Section 9 “MFRC522 registers” now follows Section 8 “Functional description” • Section 16 “Test information” added, incorporating Section 16.1 “Test signals”			
112132	May 2007	Product data sheet	200705005F	112131
112131	September 2006	Product data sheet	-	112130
112130	December 2005	Product data sheet PUBLIC	-	112121
112121	September 2005	Product data sheet	-	112120
112120	July 2005	Preliminary data sheet	-	112110
112110	July 2005	Objective data sheet	-	112104
112104	November 2004	Objective data sheet	-	112103
112103	October 2004	Objective data sheet	-	-

23. Legal information

23.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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RATP/Innovatron Technology

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25. Tables

continued >>

continued >>

continued >>

26. Figures

continued >>

27. Contents

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Date of release: 26 October 2009
112133
Document identifier: MFRC522_33

nRF51822

Multiprotocol *Bluetooth*® low energy/2.4 GHz RF System on Chip

Product Specification v3.1

Key Features

- 2.4 GHz transceiver
  - -93 dBm sensitivity in *Bluetooth*® low energy mode
  - 250 kbps, 1 Mbps, 2 Mbps supported data rates
  - TX Power -20 to +4 dBm in 4 dB steps
  - TX Power -30 dBm Whisper mode
  - 13 mA peak RX, 10.5 mA peak TX (0 dBm)
  - 9.7 mA peak RX, 8 mA peak TX (0 dBm) with DC/DC
  - RSSI (1 dB resolution)
- ARM® Cortex™-M0 32 bit processor
  - 275 µA/MHz running from flash memory
  - 150 µA/MHz running from RAM
  - Serial Wire Debug (SWD)
- S100 series SoftDevice ready
- Memory
  - 256 kB or 128 kB embedded flash program memory
  - 16 kB or 32 kB RAM
- On-air compatibility with nRF24L series
- Flexible Power Management
  - Supply voltage range 1.8 V to 3.6 V
  - 4.2 µs wake-up using 16 MHz RCOSC
  - 0.6 µA at 3 V OFF mode
  - 1.2 µA at 3 V in OFF mode + 1 region RAM retention
  - 2.6 µA at 3 V ON mode, all blocks IDLE
- 8/9/10 bit ADC - 8 configurable channels
- 31 General Purpose I/O Pins
- One 32 bit and two 16 bit timers with counter mode
- SPI Master/Slave
- Low power comparator
- Temperature sensor
- Two-wire Master (I2C compatible)
- UART (CTS/RTS)
- CPU independent Programmable Peripheral Interconnect (PPI)
- Quadrature Decoder (QDEC)
- AES HW encryption
- Real Timer Counter (RTC)
- Package variants
  - QFN48 package, 6 x 6 mm
  - WLCSP package, 3.50 x 3.83 mm
  - WLCSP package, 3.83 x 3.83 mm
  - WLCSP package, 3.50 x 3.33 mm

Applications

- Computer peripherals and I/O devices
  - Mouse
  - Keyboard
  - Multi-touch trackpad
- Interactive entertainment devices
  - Remote control
  - Gaming controller
- Beacons
- Personal Area Networks
  - Health/fitness sensor and monitor devices
  - Medical devices
  - Key-fobs + wrist watches
- Remote control toys

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Datasheet Status

Status	Description
Objective Product Specification (OPS)	This product specification contains target specifications for product development.
Preliminary Product Specification (PPS)	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product Specification (PS)	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Revision History

Date	Version	Description
October 2014	3.1	Added documentation for the following versions of the chip: • nRF51822-QFAC AA0 • nRF51822-QFAC Ax0 • nRF51822-CDAB AA0 • nRF51822-CDAB Ax0 • nRF51822-CFAC AA0 • nRF51822-CFAC Ax0 (The x in the build codes can be any number between 0 and 9.) **Added content:** • ***Section 2.2.2 "CDAB WLCSP ball assignment and functions"*** on page 13 • ***Section 9.2 "CDAB WLCSP package"*** on page 67 • ***Section 9.4 "CFAC WLCSP package"*** on page 69 **Updated content:** • Feature list on the front page. • ***Section 2.2.3 "CEAA and CFAC WLCSP ball assignment and functions"*** on page 16 • ***Section 3.2.1 "Code organization"*** on page 21 • ***Section 3.2.2 "RAM organization"*** on page 21 • ***Section 3.3 "Memory Protection Unit (MPU)"*** on page 22 • ***Section 8.2 "Power management"*** on page 44 • ***Section 8.3 "Block resource requirements"*** on page 48 • ***Section 8.12 "Analog to Digital Converter (ADC) specifications"*** on page 60 • ***Section 10.6 "Code ranges and values"*** on page 73 • ***Section 10.7 "Product options"*** on page 75

Date	Version	Description
August 2014	3.0	Update to reflect the changes in build code: • nRF51822-QFAA Hx0 • nRF51822-CEAA Ex0 • nRF51822-QFAB Cx0 (The x in the build codes can be any number between 0 and 9.) If you are working with a previous revision of the chip, read version 2.x of the document. **Added content:** • ***Section 8.5.3 "Radio current consumption with DC/DC enabled"*** on page 50 • ***Section 11.1.1 "PCB layout example"*** on page 77 **Updated content:** • Feature list on the front page. • ***Section 2.1 "Block diagram"*** on page 10 • ***Section 3.2.1 "Code organization"*** on page 21 • ***Section 3.2.2 "RAM organization"*** on page 21 • ***Section 3.3 "Memory Protection Unit (MPU)"*** on page 22 • ***Section 3.4 "Power management (POWER)"*** on page 23 • ***Section 3.6 "Clock management (CLOCK)"*** on page 27 • ***Section 3.8 "Debugger support"*** on page 30 • ***Section 4.2 "Timer/counters (TIMER)"*** on page 32 • ***Chapter 5 "Instance table"*** on page 36 • ***Chapter 7 "Operating conditions"*** on page 38 • ***Section 8.1.2 "16 MHz crystal oscillator (16M XOSC)"*** on page 40 • ***Section 8.1.3 "32 MHz crystal oscillator (32M XOSC)"*** on page 41 • ***Section 8.1.4 "16 MHz RC oscillator (16M RCOSC)"*** on page 42 • ***Section 8.1.6 "32.768 kHz RC oscillator (32k RCOSC)"*** on page 43 • ***Section 8.1.7 "32.768 kHz Synthesized oscillator (32k SYNT)"*** on page 43 • ***Section 8.2 "Power management"*** on page 44 • ***Section 8.3 "Block resource requirements"*** on page 48 • ***Section 8.4 "CPU"*** on page 48 • ***Section 8.5.6 "Radio timing parameters"*** on page 54 • ***Section 8.5.7 "Antenna matching network requirements"*** on page 54 • ***Section 8.7 "Universal Asynchronous Receiver/Transmitter (UART) specifications"*** on page 55 • ***Section 8.8 "Serial Peripheral Interface Slave (SPIS) specifications"*** on page 56 • ***Section 8.12 "Analog to Digital Converter (ADC) specifications"*** on page 60 • ***Section 8.13 "Timer (TIMER) specifications"*** on page 61 • ***Section 8.15 "Temperature sensor (TEMP)"*** on page 61 • ***Section 8.22 "Non-Volatile Memory Controller (NVMC) specifications"*** on page 64 • ***Section 8.24 "Low Power Comparator (LPCOMP) specifications"*** on page 65 • ***Section 9.2 "CDAB WLCSP package"*** on page 67 • ***Section 10.7.2 "Development tools"*** on page 75 • ***Chapter 11 "Reference circuitry"*** on page 76

Date	Version	Description
October 2013	2.0	This version of the document will target the nRF51822 QFAA G0 revision of the chip. If you are working with a previous revision of the chip, read version 1.3 or earlier of the document. **Updated** the following sections: Key Feature list on the front page, ***Chapter 1 "Introduction"*** on page 9, ***Section 2.1 "Block diagram"*** on page 10, ***Section 2.2 "Pin assignments and functions"*** on page 11, ***Section 3.2 "Memory"*** on page 20, ***Section 3.5 "Programmable Peripheral Interconnect (PPI)"*** on page 26, ***Section 3.7 "GPIO"*** on page 30, ***Section 4.1 "2.4 GHz radio (RADIO)"*** on page 31, ***Section 4.2 "Timer/counters (TIMER)"*** on page 32, ***Section 4.3 "Real Time Counter (RTC)"*** on page 32, ***Section 4.10 "Serial Peripheral Interface (SPI/SPIS)"*** on page 34, ***Section 4.12 "Universal Asynchronous Receiver/Transmitter (UART)"*** on page 35, ***Section 4.14 "Analog to Digital Converter (ADC)"*** on page 35, ***Section 4.15 "GPIO Task Event blocks (GPIOTE)"*** on page 35, ***Chapter 5 "Instance table"*** on page 36, ***Chapter 6 "Absolute maximum ratings"*** on page 37, ***Chapter 8 "Electrical specifications"*** on page 39, ***Section 8.1 "Clock sources"*** on page 39, ***Section 8.1.2 "16 MHz crystal oscillator (16M XOSC)"*** on page 40, ***Section 8.1.3 "32 MHz crystal oscillator (32M XOSC)"*** on page 41, ***Section 8.2 "Power management"*** on page 44, ***Section 8.3 "Block resource requirements"*** on page 48, ***Section 8.7 "Universal Asynchronous Receiver/Transmitter (UART) specifications"*** on page 55, ***Section 8.9 "Serial Peripheral Interface (SPI) Master specifications"*** on page 57, ***Section 8.11 "GPIO Tasks and Events (GPIOTE) specifications"*** on page 59, ***Section 8.13 "Timer (TIMER) specifications"*** on page 61, ***Section 8.16 "Random Number Generator (RNG) specifications"*** on page 62, ***Section 8.17 "AES Electronic Codebook Mode Encryption (ECB) specifications"*** on page 62, ***Section 8.18 "AES CCM Mode Encryption (CCM) specifications"*** on page 62, ***Section 8.19 "Accelerated Address Resolver (AAR) specifications"*** on page 62, ***Section 8.21 "Quadrature Decoder (QDEC) specifications"*** on page 63, ***Section 11.1 "PCB guidelines"*** on page 76, ***Section 11.3 "QFAA QFN48 package"*** on page 79, and ***Section 11.7 "CEAA WLCSP package"*** on page 103. **Added** the following sections: ***Section 3.3 "Memory Protection Unit (MPU)"*** on page 22, ***Section 4.5 "AES CCM Mode Encryption (CCM)"*** on page 33, ***Section 4.6 "Accelerated Address Resolver (AAR)"*** on page 33, ***Section 4.16 "Low Power Comparator (LPCOMP)"*** on page 35, ***Section 8.5.7 "Antenna matching network requirements"*** on page 54, ***Section 8.8 "Serial Peripheral Interface Slave (SPIS) specifications"*** on page 56, ***Section 8.18 "AES CCM Mode Encryption (CCM) specifications"*** on page 62, ***Section 8.19 "Accelerated Address Resolver (AAR) specifications"*** on page 62, and ***Section 8.24 "Low Power Comparator (LPCOMP) specifications"*** on page 65.
May 2013	1.3	Updated schematics and BOMs in section 11.3 on page 61.

Date	Version	Description
April 2013	1.2	Added chip variant nRF51822-CEAA. Updated feature list on front page. **Updated** Section 3.2.1 on page 15, Section 3.2.2 on page 15, Chapter 6 on page 28, Section 10.4 on page 52, and Section 10.5.1 on page 53. **Added** Section 2.2.2 on page 10, Section 7.1 on page 29, Section 9.2 on page 50, and Section 11.3 on page 61. **Removed** PCB layouts in Chapter 11 on page 54.
March 2013	1.1	Added chip variant nRF51822-QFAB. Added 32 MHz crystal oscillator feature. Updated feature list on front page. Moved subsection 'Calculating current when the DC/DC converter is enabled' from chapter 8 to the *nRF51 Series Reference Manual*. **Updated** Chapter 1 on page 6, Section 2.2 on page 8, Section 3.2 on page 12, Section 3.5 on page 16, Section 3.5.1 on page 17, Section 4.2 on page 21, Chapter 5 on page 24, Section 8.1 on page 27, Section 8.1.2 on page 28, Section 8.1.5 on page 30, Section 8.2 on page 32, Section 8.3 on page 34, Section 8.5.3 on page 36, Section 8.8 on page 40, Section 8.9 on page 41, Section 8.10 on page 42, Section 8.14 on page 43, Chapter 10 on page 47, Section 11.2 on page 51, Section 11.3 on page 54, and Section 11.4 on page 57. **Added** Section 3.5.4 on page 19, Section 8.1.3 on page 29, and Section 11.1 on page 50.
November 2012	1.0	Changed from PPS to PS. Updated the feature list on the front page. **Updated** Table 11 on page 25, Table 12 on page 26, Table 14 on page 28, Table 15 on page 28, Table 16 on page 29, Table 17 on page 29, Table 18 on page 30, Table 19 on page 31, Table 21 on page 32, Table 22 on page 32, Table 23 on page 33,Table 27 on page 36, Table 28 on page 37, Table 29 on page 37, Table 31 on page 38, Table 32 on page 38, Table 35 on page 39, Table 38 on page 40, Table 39 on page 40, Table 55 on page 47, Figure 9 on page 48, and Table 57 on page 50.

Table of contents

1 Introduction

The nRF51822 is an ultra-low power 2.4 GHz wireless System on Chip (SoC) integrating the nRF51 series 2.4 GHz transceiver, a 32 bit ARM® Cortex™-M0 CPU, flash memory, and analog and digital peripherals. nRF51822 can support *Bluetooth*® low energy and a range of proprietary 2.4 GHz protocols, such as Gazell from Nordic Semiconductor.

Fully qualified *Bluetooth* low energy stacks for nRF51822 are implemented in the S100 series of SoftDevices. The S100 series of SoftDevices are available for free and can be downloaded and installed on nRF51822 independent of your own application code.

1.1 Required reading

The following documentation is available for download from www.nordicsemi.com:

- *nRF51 Series Reference Manual*
- *nRF51822-PAN (Product Anomaly Notification)*
- *PCN-092 (nRF51822 Product Change Notification)*

1.2 Writing conventions

This product specification follows a set of typographic rules to ensure that the document is consistent and easy to read. The following writing conventions are used:

- Command, event names, and bit state conditions, are written in `Lucida Console`.
- Pin names and pin signal conditions are written in **`Consolas`.**
- File names and User Interface components are written in **bold**.
- Internal cross references are italicized and written in ***semi-bold.***
- Placeholders for parameters are written in italic regular text font. For example, a syntax description of Connect will be written as:
  Connect*(TimeOut, AdvInterval)*.
- Fixed parameters are written in regular text font. For example, a syntax description of Connect will be written as:
  Connect(0x00F0, Interval).

2 Product overview

2.1 Block diagram

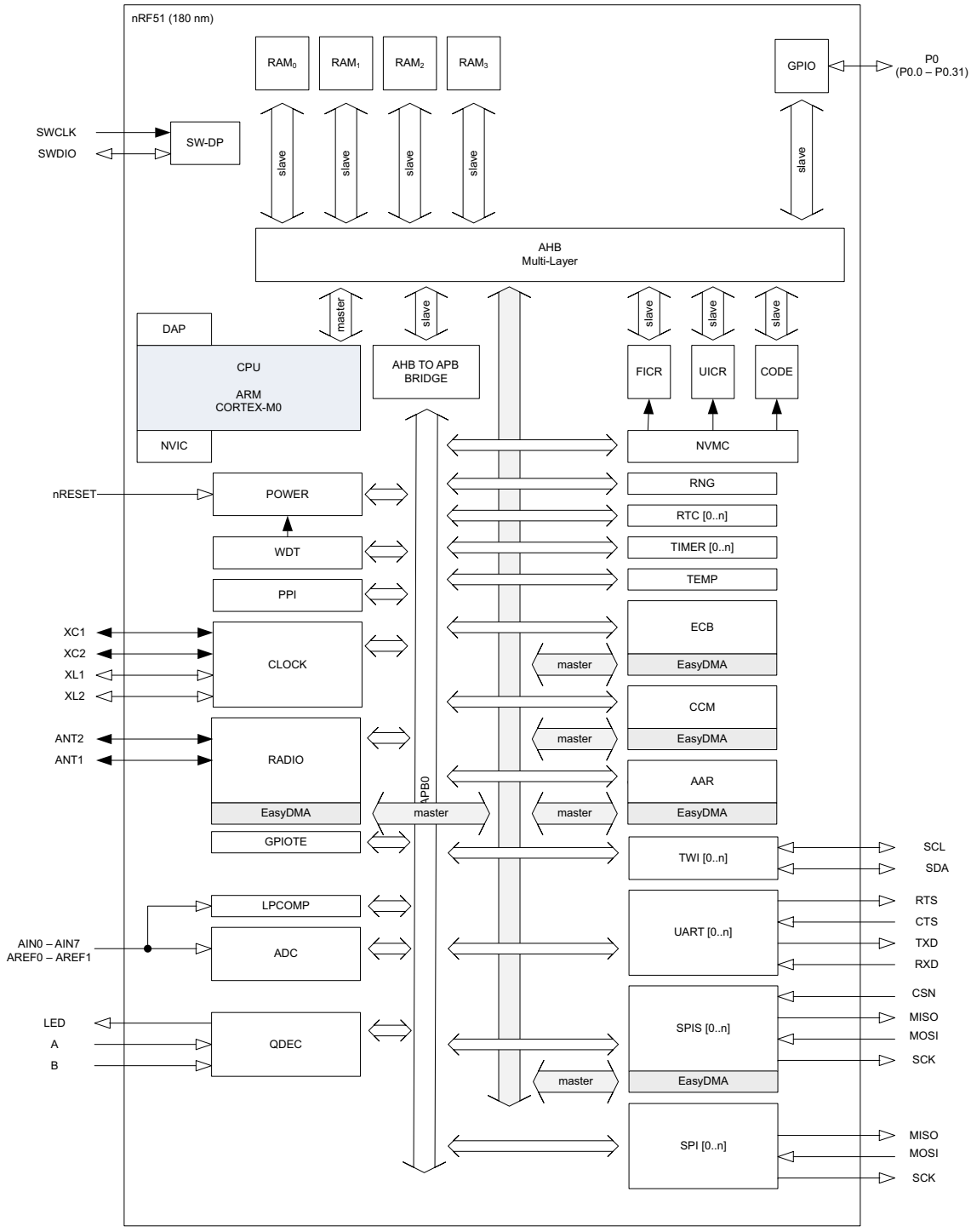

Figure 1 *Block diagram*

2.2 Pin assignments and functions

This section describes the pin assignment and the pin functions.

2.2.1 Pin assignment QFN48

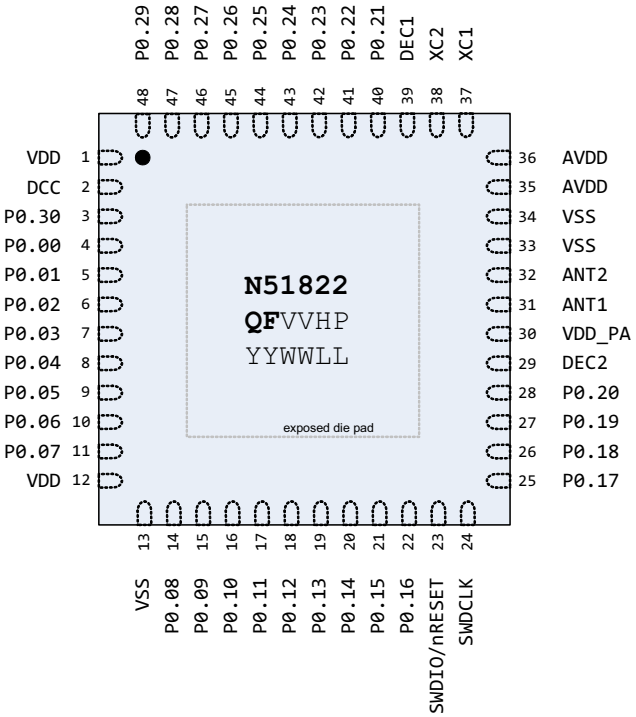

Figure 2 *Pin assignment - QFN48 packet*

Note: VV = Variant code, HP = Build code, YYWWLL = Tracking code.
For more information, see ***Section 10.6 "Code ranges and values"*** on page 73.

2.2.1.1 Pin functions QFN48

Pin	Pin name	Pin function	Description
1	VDD	Power	Power supply.
2	DCC	Power	DC/DC output voltage to external LC filter.
3	P0.30	Digital I/O	General purpose I/O pin.
4	P0.00 AREF0	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP reference input 0.
5	P0.01 AIN2	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP input 2.
6	P0.02 AIN3	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP input 3.
7	P0.03 AIN4	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP input 4.
8	P0.04 AIN5	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP input 5.
9	P0.05 AIN6	Digital I/O Analog input	General purpose I/O pin. ADC/LPCOMP input 6.
10	P0.06 AIN7 AREF1	Digital I/O Analog input Analog input	General purpose I/O pin. ADC/LPCOMP input 7. ADC/LPCOMP reference input 1.
11	P0.07	Digital I/O	General purpose I/O pin.
12	VDD	Power	Power supply.
13	VSS	Power	Ground (0 V)[1].
14 to 22	P0.08 to P0.16	Digital I/O	General purpose I/O pin.
23	SWDIO/nRESET	Digital I/O	System reset (active low). Also hardware debug and flash programming I/O.
24	SWDCLK	Digital input	Hardware debug and flash programming I/O.
25 to 28	P0.17 to P0.20	Digital I/O	General purpose I/O pin.
29	DEC2	Power	Power supply decoupling.
30	VDD_PA	Power output	Power supply output (+1.6 V) for on-chip RF power amp.
31	ANT1	RF	Differential antenna connection (TX and RX).
32	ANT2	RF	Differential antenna connection (TX and RX).
33, 34	VSS	Power	Ground (0 V).
35, 36	AVDD	Power	Analog power supply (Radio).
37	XC1	Analog input	Connection for 16/32 MHz crystal or external 16 MHz clock reference.
38	XC2	Analog output	Connection for 16/32 MHz crystal.
39	DEC1	Power	Power supply decoupling.

Pin	Pin name	Pin function	Description
40 to 44	P0.21 to P0.25	Digital I/O	General purpose I/O pin.
45	P0.26 AIN0 XL2	Digital I/O Analog input Analog output	General purpose I/O pin. ADC/LPCOMP input 0. Connection for 32.768 kHz crystal.
46	P0.27 AIN1 XL1	Digital I/O Analog input Analog input	General purpose I/O pin. ADC/LPCOMP input 1. Connection for 32.768 kHz crystal or external 32.768 kHz clock reference.
47, 48	P0.28 and P0.29	Digital I/O	General purpose I/O pin.

1. The exposed center pad of the QFN48 package must be connected to ground for proper device operation.

Table 1 *Pin functions QFN48 packet*

2.2.2 CDAB WLCSP ball assignment and functions

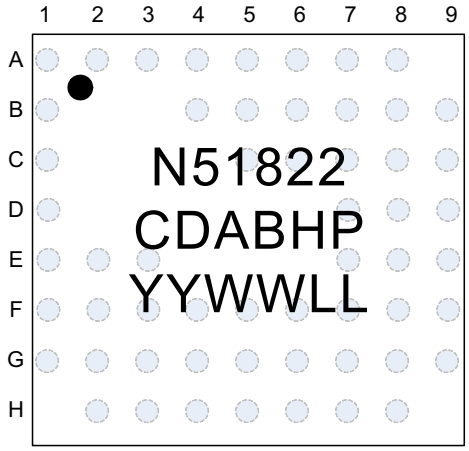

Figure 3 *Ball assignment CDAB packet (top side view)*

2.2.2.1 Ball functions CDAB

Ball	Name	Function	Description
A1	AVDD	Power	Analog power supply (Radio).
A2	XC1	Analog input	Crystal connection for 16/32 MHz crystal oscillator or external 16/32 MHz crystal reference.
A3	XC2	Analog output	Crystal connection for 16/32 MHz crystal.
A4	DEC1	Power	Power supply decoupling.
A5	P0.21	Digital I/O	General purpose I/O.
A6	P0.24	Digital I/O	General purpose I/O.
A7	P0.26 AIN0 XL2	Digital I/O Analog input Analog output	General purpose I/O. ADC input 0. Crystal connection for 32.768 kHz crystal oscillator.
A8	P0.27 AIN1 XL1	Digital I/O Analog input Analog input	General purpose I/O. ADC input 1. Crystal connection for 32.768 kHz crystal oscillator or external 32.768 kHz crystal reference.
B1	VSS	Power	Ground (0 V).
B4	VSS	Power	Ground (0 V).
B5	P0.22	Digital I/O	General purpose I/O.
B6	P0.23	Digital I/O	General purpose I/O.
B7	P0.28	Digital I/O	General purpose I/O.
B8	VDD	Power	Power supply.
B9	DCC	Power	DC/DC output voltage to external LC filter.
C1	ANT2	RF	Differential antenna connection (TX and RX).
C5	P0.25	Digital I/O	General purpose I/O.
C6	N.C.	No Connection	Must be soldered to PCB.
C7	P0.29	Digital I/O	General purpose I/O.
C8	P0.30	Digital I/O	General purpose I/O.
C9	P0.00 AREF0	Digital I/O Analog input	General purpose I/O. ADC Reference voltage.
D1	ANT1	RF	Differential antenna connection (TX and RX).
D7	VSS	Power	Ground (0 V).
D8	P0.31	Digital I/O	General purpose I/O.
D9	P0.02 AIN3	Digital I/O Analog input	General purpose I/O. ADC input 3.
E1	VDD_PA	Power output	Power supply output (+1.6 V) for on-chip RF power amp.
E2	N.C.	No Connection	Must be soldered to PCB.
E3	N.C.	No Connection	Must be soldered to PCB.
E7	P0.01 AIN2	Digital I/O Analog input	General purpose I/O. ADC input 2.
E8	P0.04 AIN5	Digital I/O Analog input	General purpose I/O. ADC input 5.

Ball	Name	Function	Description
E9	P0.03 AIN4	Digital I/O Analog input	General purpose I/O. ADC input 4.
F1	DEC2	Power	Power supply decoupling.
F2	P0.19	Digital I/O	General purpose I/O.
F3	P0.18	Digital I/O	General purpose I/O.
F4	VSS	Power	Ground (0 V).
F5	N.C.	No Connection	Must be soldered to PCB.
F6	VSS	Power	Ground (0 V).
F7	N.C.	No Connection	Must be soldered to PCB.
F8	P0.06 AIN7 AREF1	Digital I/O Analog input Analog input	General purpose I/O. ADC input 7. ADC Reference voltage.
F9	VSS	Power	Ground (0 V).
G1	P0.20	Digital I/O	General purpose I/O.
G2	SWDCLK	Digital input	Hardware debug and flash programming I/O.
G3	P0.17	Digital I/O	General purpose I/O.
G4	P0.14	Digital I/O	General purpose I/O.
G5	P0.13	Digital I/O	General purpose I/O.
G6	P0.10	Digital I/O	General purpose I/O.
G7	P0.07	Digital I/O	General purpose I/O.
G8	VDD	Power	Power supply.
G9	P0.05 AIN6	Digital I/O Analog input	General purpose I/O. ADC input 6.
H2	nRESET SWDIO	Digital I/O	System reset (active low). Hardware debug and flash programming I/O.
H3	P0.16	Digital I/O	General purpose I/O.
H4	P0.15	Digital I/O	General purpose I/O.
H5	P0.12	Digital I/O	General purpose I/O.
H6	P0.11	Digital I/O	General purpose I/O.
H7	P0.09	Digital I/O	General purpose I/O.
H8	P0.08	Digital I/O	General purpose I/O.

Table 2 *Ball functions CDAB packet*

2.2.3 CEAA and CFAC WLCSP ball assignment and functions

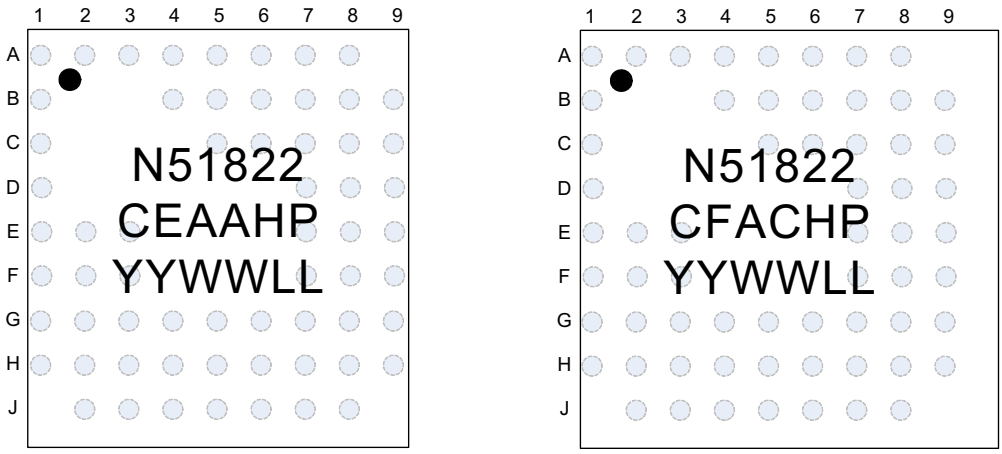

Figure 4 *Ball assignment CEAA and CFAC packet (top side view)*

Note: HP = Buildcode, YYWWLL = Tracking code
Solder balls not visible on the top side. Dot denotes A1 corner.

2.2.3.1 Ball functions CEAA and CFAC

Ball	Name	Function	Description
A1	AVDD	Power	Analog power supply (Radio).
A2	XC1	Analog input	Crystal connection for 16/32 MHz crystal oscillator or external 16/32 MHz crystal reference.
A3	XC2	Analog output	Crystal connection for 16/32 MHz crystal.
A4	DEC1	Power	Power supply decoupling.
A5	P0.21	Digital I/O	General purpose I/O.
A6	P0.24	Digital I/O	General purpose I/O.
A7	P0.26 AIN0 XL2	Digital I/O Analog input Analog output	General purpose I/O. ADC input 0. Crystal connection for 32.768 kHz crystal oscillator.
A8	P0.27 AIN1 XL1	Digital I/O Analog input Analog input	General purpose I/O. ADC input 1. Crystal connection for 32.768 kHz crystal oscillator or external 32.768 kHz crystal reference.
B1	VSS	Power	Ground (0 V).
B4	VSS	Power	Ground (0 V).
B5	P0.22	Digital I/O	General purpose I/O.
B6	P0.23	Digital I/O	General purpose I/O.
B7	P0.28	Digital I/O	General purpose I/O.
B8	VDD	Power	Power supply.
B9	DCC	Power	DC/DC output voltage to external LC filter.
C1	ANT2	RF	Differential antenna connection (TX and RX).
C5	P0.25	Digital I/O	General purpose I/O.
C6	N.C.	No Connection	Must be soldered to PCB.
C7	P0.29	Digital I/O	General purpose I/O.
C8	VSS	Power	Ground (0 V).
C9	P0.00 AREF0	Digital I/O Analog input	General purpose I/O. ADC Reference voltage.
D1	ANT1	RF	Differential antenna connection (TX and RX).
D7	VSS	Power	Ground (0 V).
D8	P0.30	Digital I/O	General purpose I/O.
D9	P0.02 AIN3	Digital I/O Analog input	General purpose I/O. ADC input 3.
E1	VDD_PA	Power output	Power supply output (+1.6 V) for on-chip RF power amp.
E2	N.C.	No Connection	Must be soldered to PCB.
E3	N.C.	No Connection	Must be soldered to PCB.
E7	N.C.	No Connection	Must be soldered to PCB.
E8	P0.31	Digital I/O	General purpose I/O.
E9	P0.01 AIN2	Digital I/O Analog input	General purpose I/O. ADC input 2.

Ball	Name	Function	Description
F1	DEC2	Power	Power supply decoupling.
F2	P0.19	Digital I/O	General purpose I/O.
F3	N.C.	No Connection	Must be soldered to PCB.
F7	N.C.	No Connection	Must be soldered to PCB.
F8	P0.04 AIN5	Digital I/O Analog input	General purpose I/O. ADC input 5.
F9	P0.03 AIN4	Digital I/O Analog input	General purpose I/O. ADC input 4.
G1	P0.20	Digital I/O	General purpose I/O.
G2	P0.17	Digital I/O	General purpose I/O.
G3	N.C.	No Connection	Must be soldered to PCB.
G4	N.C.	No Connection	Must be soldered to PCB.
G5	N.C.	No Connection	Must be soldered to PCB.
G6	VSS	Power	Ground (0 V).
G7	N.C.	No Connection	Must be soldered to PCB.
G8	P0.06 AIN7 AREF1	Digital I/O Analog input Analog input	General purpose I/O. ADC input 7. ADC Reference voltage.
G9	VSS	Power	Ground (0 V).
H1	P0.18	Digital I/O	General purpose I/O.
H2	SWDCLK	Digital input	Hardware debug and flash programming I/O.
H3	VSS	Power	Ground (0 V).
H4	P0.14	Digital I/O	General purpose I/O.
H5	P0.13	Digital I/O	General purpose I/O.
H6	P0.10	Digital I/O	General purpose I/O.
H7	P0.07	Digital I/O	General purpose I/O.
H8	VDD	Power	Power supply.
H9	P0.05 AIN6	Digital I/O Analog input	General purpose I/O. ADC input 6.
J2	SWDIO/ nRESET	Digital I/O	System reset (active low). Also Hardware debug and flash programming I/O.
J3	P0.16	Digital I/O	General purpose I/O.
J4	P0.15	Digital I/O	General purpose I/O.
J5	P0.12	Digital I/O	General purpose I/O.
J6	P0.11	Digital I/O	General purpose I/O.
J7	P0.09	Digital I/O	General purpose I/O.
J8	P0.08	Digital I/O	General purpose I/O.

Table 3 *Ball functions for CEAA and CFAC*

3 System blocks

The chip contains system-level features common to all nRF51 series devices including clock control, power and reset, interrupt system, Programmable Peripheral Interconnect (PPI), watchdog, and GPIO.

System blocks which have a register interface and/or interrupt vector assigned are instantiated in the device address space. The instances of system blocks, their associated ID (for those with interrupt vectors), and base addresses are found in ***Table 18*** on page 36. Detailed functional descriptions, configuration options, and register interfaces can be found in the *nRF51 Series Reference Manual*.

3.1 CPU

The ARM® Cortex™-M0 CPU has a 16 bit instruction set with 32 bit extensions (Thumb-2® technology) that delivers high-density code with a small-memory-footprint. By using a single-cycle 32 bit multiplier, a 3-stage pipeline, and a Nested Vector Interrupt Controller (NVIC), the ARM Cortex-M0 CPU makes program execution simple and highly efficient.

The ARM Cortex Microcontroller Software Interface Standard (CMSIS) hardware abstraction layer for the ARM Cortex-M processor series is implemented and available for M0 CPU. Code is forward compatible with ARM Cortex M3 based devices.

3.2 Memory

All memory and registers are found in the same address space as shown in the Device Memory Map, see ***Figure 5***. Devices in the nRF51 series use flash based memory in the code, FICR, and UICR regions.
The RAM region is SRAM.

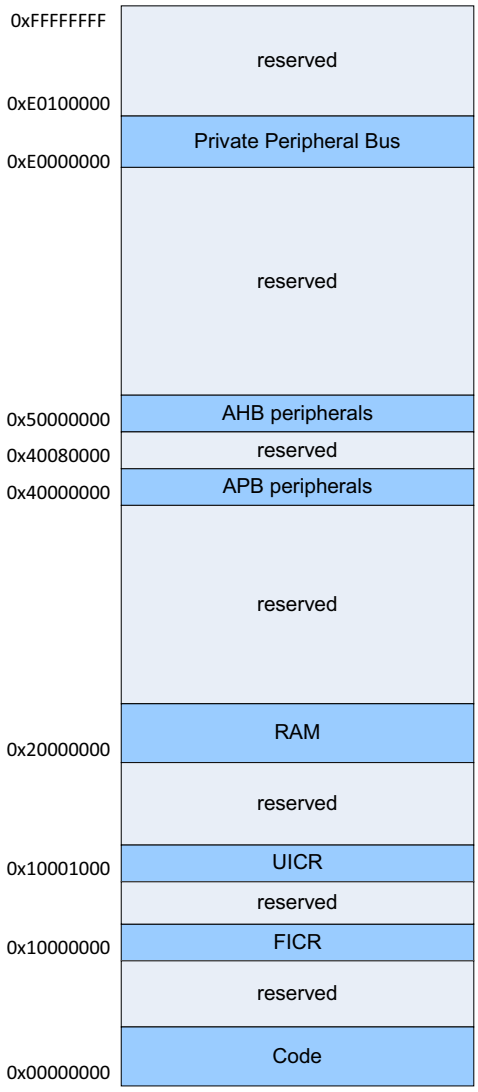

Figure 5 *Memory Map*

The embedded flash memory for program and static data can be programmed using In Application Programming (IAP) routines from RAM through the SWD interface, or in-system from a program executing from code area. The Non-Volatile Memory Controller (NVMC) is used for program/erase operations. Regions of flash memory can be protected from read, write, and erase by the Memory Protection Unit (MPU). A User Information Configuration Register (UICR) contains the lock byte for enabling readback protection to secure the IP, while individual block protection is controlled using registers which can only be cleared on chip reset.

3.2.1 Code organization

Chip variant	Code size	Page size	No of pages
nRF51822-QFAA nRF51822-CEAA	256 kB	1024 byte	256
nRF51822-QFAB nRF51822-CDAB	128 kB	1024 byte	128
nRF51822-QFAC nRF51822-CFAC	256 kB	1024 byte	256

Table 4 *Code organization*

3.2.2 RAM organization

RAM is divided into blocks for separate power management which is controlled by the POWER System Block. Each block is divided into two 4 kByte RAM sections with separate RAM AHB slaves.
Please see the *nRF51 Series Reference Manual* for more information.

Chip variant	RAM size	Block	Size
nRF51822-QFAA nRF51822-CEAA	16 kB	Block0 Block1	8 kB 8 kB
nRF51822-QFAB nRF51822-CDAB	16 kB	Block0 Block1	8 kB 8 kB
nRF51822-QFAC nRF51822-CFAC	32 kB	Block0 Block1 Block2 Block3	8 kB 8 kB 8 kB 8 kB

Table 5 *RAM organization*

How to organize the use of the RAM

For the best performance we recommend the following use of the RAM AHB slaves (Note that the Crypto consists of CCM, ECB, and AAR modules):

- If the Radio and Crypto buffers together are larger in size than one RAM section, the buffers should be separated so the memory used by the Radio is in one RAM section while the memory used by the Crypto is in another RAM section.
- The sections used by CODE should not be combined with sections used by the Radio, Crypto, or SPI.
- The Stack and Heap should be placed at the top section and should not be combined with sections used by the Radio, Crypto, or SPI.

Table 6 and *Table 7* shows how memory allocated to different functions can be distributed between RAM sections for parallel access. There is a table for chip variants with 16 kB or 32 kB RAM.

RAM Blocks/Sections		Radio buffers	Crypto buffers	SPIS buffers	CPU Stack/Heap	CODE	Global variables
Block0	RAM0	x	x				x
	RAM1					x	x
Block1	RAM2			x			x
	RAM3				x	x	x

Table 6 16 kB RAM variants

RAM Blocks/Sections		Radio buffers	Crypto buffers	SPIS buffers	CPU Stack/Heap	CODE	Global variables
Block0	RAM0	x	(x)				x
	RAM1	(x)	x				x
Block1	RAM2			x			x
	RAM3					x	x
Block2	RAM4					x	x
	RAM5					x	x
Block3	RAM6					x	x
	RAM7				x	x	x

Table 7 32 kB RAM variants

3.3 Memory Protection Unit (MPU)

The memory protection unit can be configured to protect all flash memory on the device from read-back, or to protect blocks of flash from over-write or erase.

Chip variant	Flash block size	Number of protectable Flash blocks
nRF51822-QFAA nRF51822-CEAA	4 kB	64
nRF51822-QFAB nRF51822-CDAB	4 kB	32
nRF51822-QFAC nRF51822-CFAC	4 kB	64

Table 8 MPU flash blocks

3.4 Power management (POWER)

3.4.1 Power supply

nRF51 supports three different power supply alternatives:

- Internal LDO setup
- DC/DC converter setup
- Low voltage mode setup

See ***Table 20*** on page 38 for the voltage range on the different alternatives. See ***Chapter 11 "Reference circuitry"*** on page 76 for details on the schematic used for the different power supply alternatives.

3.4.1.1 Internal LDO setup

In internal LDO mode the DC/DC converter is bypassed (disabled) and the system power is generated directly from the supply voltage VDD. This mode could be used as the only option or in combination with the DC/DC converter setup. See DC/DC converter section for more details.

3.4.1.2 DC/DC converter setup

The nRF51 DC/DC buck converter transforms battery voltage to lower internal voltage with minimal power loss. The converted voltage is then available for the linear regulator input. The DC/DC converter can be disabled when the supply voltage drops to the lower limit of the voltage range so the LDO can be used for low supply voltages. When enabled, the DC/DC converter operation is automatically suspended between radio events when only the low current regulator is needed internally.

This feature is particularly useful for applications using battery technologies with nominal cell voltages higher than the minimum supply voltage with DC/DC enabled. The reduction in supply voltage level from a high voltage to a low voltage reduces the peak power drain from the battery. Used with a 3 V coin-cell battery, the peak current drawn from the battery is reduced by approximately 25%.

3.4.1.3 Low voltage mode setup

Devices can be used in low voltage mode where a steady 1.8 V supply is available externally.

3.4.2 Power management

The power management system is highly flexible with functional blocks such as the CPU, Radio Transceiver, and peripherals having separate power state control in addition to the global System ON and OFF modes. In System OFF mode, RAM can be retained and the device state can be changed to System ON through Reset, GPIO DETECT signal, or LPCOMP ANADETECT signal. When in System ON mode, all functional blocks will independently be in IDLE or RUN mode depending on needed functionality.

Power management features:

- Supervisor HW to manage
  - Power on reset
  - Brownout reset
  - Power fail comparator
- System ON/OFF modes
- Pin wake-up from System OFF
  - Reset
  - GPIO DETECT signal
  - LPCOMP ANADETECT signal
- Functional block RUN/IDLE modes
- RAM retention in System OFF mode (8 kB blocks)
  - 16 kB version will have 2 blocks
  - 32 kB version will have 4 blocks

3.4.2.1 System OFF mode

In system OFF mode the chip is in the deepest power saving mode. The system's core functionality is powered down and all ongoing tasks are terminated. The only functionality that can be set up to be responsive is the Pin wake-up mechanism.

One or more blocks of RAM can be retained while in System OFF mode.

3.4.2.2 System ON mode

In system ON mode the system is fully operational and the CPU and selected peripherals can be brought into a state where they are functional and more or less responsive depending on the sub-power mode selected.

There are two sub-power modes:

- Low power
- Constant latency

Low Power

In Low Power mode the automatic power management system is optimized to save power. This is done by keeping as much as possible of the system powered down. The cost of this is that you will have varying CPU wakeup latency and PPI task response.

The CPU wakeup latency will be affected by the startup time of the 1V7 regulator. The PPI task response will vary depending on the resources required by the peripheral where the task originated.

The resources that could be involved are:

- 1V7 with the startup time $\mathbf{t_{1V7}}$
- 1V2 with the startup time $\mathbf{t_{1V2}}$
- One of the following clock sources
  - RC16 with the startup time $\mathbf{t_{START,RC16}}$
  - XO16M/XO32M with the startup time the clock management system $\mathbf{t_{XO}}$[1]

Constant Latency

In Constant Latency mode the system is optimized towards keeping the CPU latency and the PPI task response constant and at a minimum. This is secured by forcing a set of base resources on while in sleep mode. The cost is that the system will have higher power consumption.

The following resources are kept active while in sleep mode:

- 1V7 regulator with the standby current of I_{1V7}
- 1V2 regulator. Here the current consumption is specified in combination with the clock source
- One of the following clock sources:
  - RC16 with the standby current of $I_{1V2RC16}$
  - XO16M with the standby current of $I_{1V2XO16}$
  - XO32M with the standby current of $I_{1V2XO32}$

1. For the clock source XO16M and XO32M we assume that the crystal is already running (standby). This will give an increase of the power consumption in sleep mode given by $\mathbf{I_{STBY,X16M}}$ / $\mathbf{I_{STBY,X32M}}$.

3.5 Programmable Peripheral Interconnect (PPI)

The Programmable Peripheral Interconnect (PPI) enables peripherals to interact autonomously with each other using tasks and events independent of the CPU. The PPI allows precise synchronization between peripherals when real-time application constraints exist and eliminates the need for CPU activity to implement behavior which can be predefined using PPI.

Instance	Channel	Number of channels	Number of groups
PPI	0 - 15	16	4

Table 9 *PPI properties*

The PPI system has in addition to the fully programmable peripheral interconnections, a set of channels where the event (EEP) and task (TEP) endpoints are set in hardware. These fixed channels can be individually enabled, disabled, or added to PPI channel groups in the same way as ordinary PPI channels. See the *nRF51 Series Reference Manual* for more information.

Instance	Channel	Number of channels	Number of groups
PPI	20 - 31	12	4

Table 10 *Pre-programmed PPI channels*

3.6 Clock management (CLOCK)

The advanced clock management system can source the system clocks from a range of internal or external high and low frequency oscillators and distribute them to modules based upon a module's individual requirements. This prevents large clock trees from being active and drawing power when system modules needing this clock reference are not active.

If an application enables a module that needs a clock reference without the corresponding oscillator running, the clock management system will automatically enable the RC oscillator option and provide the clock. When the module goes back to idle, the clock management will automatically set the oscillator to idle. To avoid delays involved in starting a given oscillator, or if a specific oscillator is required, the application can override the automatic oscillator management so it keeps oscillators active when no system modules require the clock reference.

Clocks are only available in System ON mode and can be generated by the sources listed in ***Table 11***.

Clock	Source	Frequency options
High Frequency Clock (HFCLK)[1]	External Crystal (XOSC)	16/32 MHz[2]
	External clock reference[3]	16 MHz
	Internal RC Oscillator (RCOSC)	16 MHz
Low Frequency Clock (LFCLK)	External Crystal (XOSC)	32.768 kHz
	External clock reference[3]	32.768 kHz
	Synthesized from HFCLK	32.768 kHz
	Internal RC Oscillator (RCOSC)	32.768 kHz

1. External Crystal must be used for Radio operation.
2. The HFCLK will be 16 MHz for both the 16 and 32 MHz crystal option.
3. See the *nRF51 Series Reference Manual* for more details on external clock reference.

Table 11 *Clock properties*

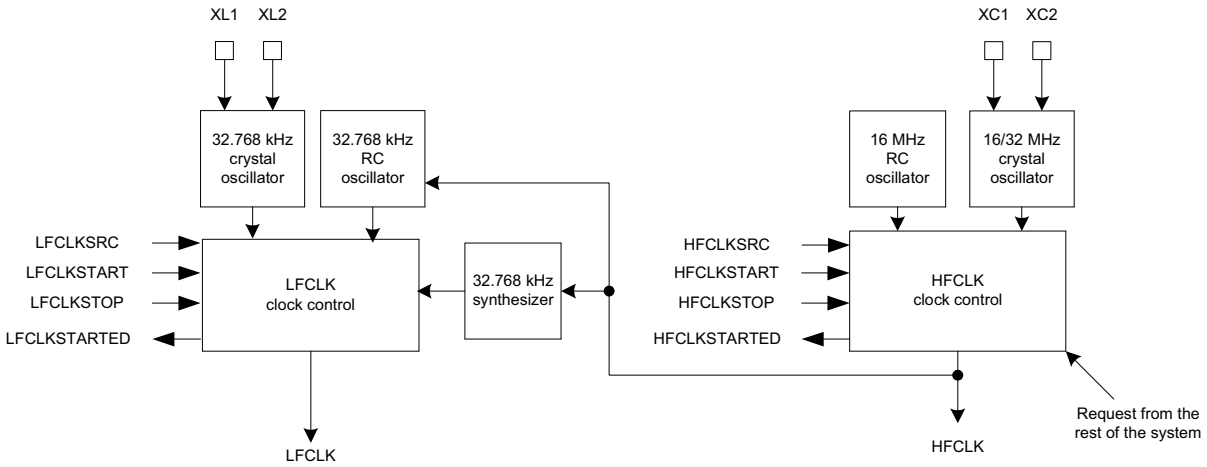

Figure 6 *Clock management*

3.6.1 16/32 MHz crystal oscillator

The crystal oscillator can be controlled either by a 16 MHz or a 32 MHz external crystal. However, the system clock is always 16 MHz, see the *nRF51 Series Reference Manual* for more details. The crystal oscillator is designed for use with an AT-cut quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. ***Figure 7*** shows how the crystal is connected to the 16/32 MHz crystal oscillator.

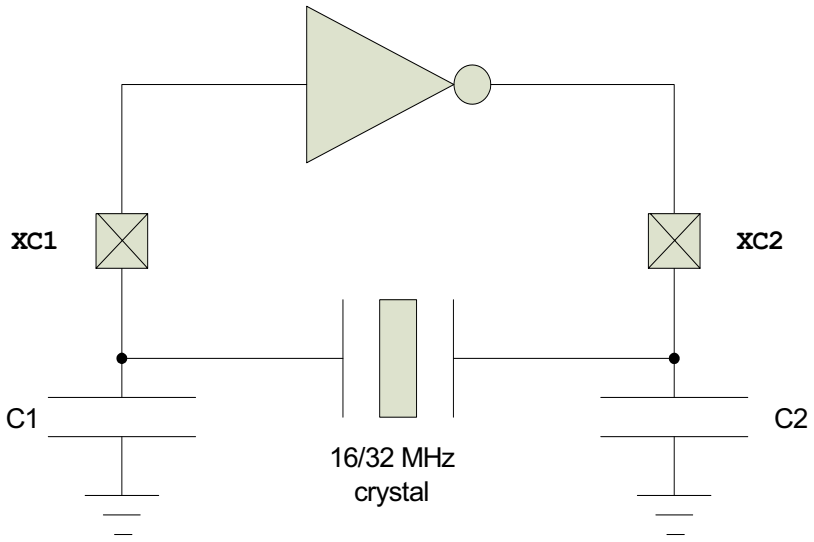

Figure 7 *Circuit diagram of the 16/32 MHz crystal oscillator*

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C\_pcb1 + C\_pin$$

$$C2' = C2 + C\_pcb2 + C\_pin$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_pcb1 and C_pcb2 are stray capacitances on the PCB. C_pin is the pin input capacitance on the XC1 and XC2 pins, see ***Table 22*** on page 40 (16 MHz) and ***Table 23*** on page 41 (32 MHz). The load capacitors C1 and C2 should have the same value. See ***Chapter 11 "Reference circuitry"*** on page 76 for the capacitance value used for C_pcb1 and C_pcb2 in reference circuitry.

For reliable operation, the crystal load capacitance, shunt capacitance, equivalent series resistance ($R_{S,X16M}$/$R_{S,X32M}$), and drive level must comply with the specifications in ***Table 22*** on page 40 (16 MHz) and ***Table 23*** on page 41 (32 MHz). It is recommended to use a crystal with lower than maximum $R_{S,X16M}$/$R_{S,X32M}$ if the load capacitance and/or shunt capacitance is high. This will give faster startup and lower current consumption. A low load capacitance will reduce both startup time and current consumption.

3.6.2 32.768 kHz crystal oscillator

The 32.768 kHz crystal oscillator is designed for use with a quartz crystal in parallel resonant mode. To achieve correct oscillation frequency, the load capacitance must match the specification in the crystal data sheet. ***Figure 8*** shows how the crystal is connected to the 32.768 kHz crystal oscillator.

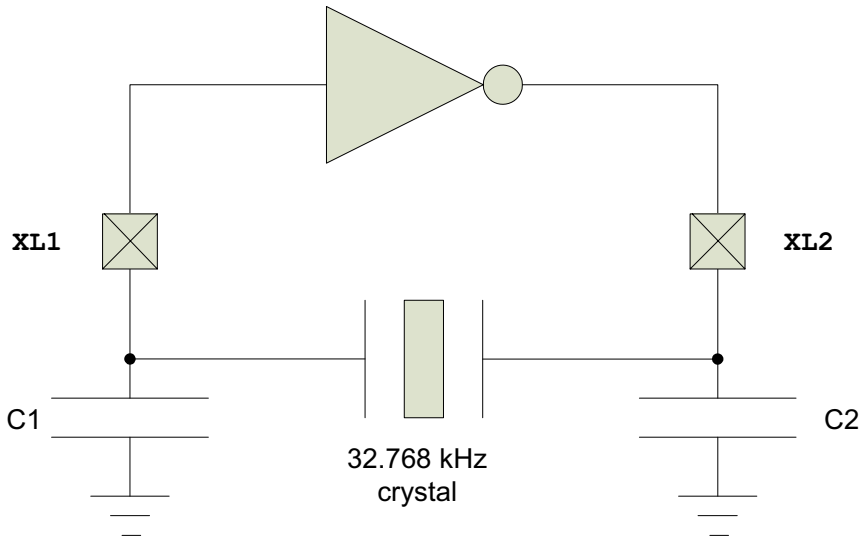

Figure 8 *Circuit diagram of the 32.768 kHz crystal oscillator*

The load capacitance (CL) is the total capacitance seen by the crystal across its terminals and is given by:

$$CL = \frac{(C1' \cdot C2')}{(C1' + C2')}$$

$$C1' = C1 + C\_pcb1 + C\_pin$$

$$C2' = C2 + C\_pcb2 + C\_pin$$

C1 and C2 are ceramic SMD capacitors connected between each crystal terminal and ground. C_pcb1 and C_pcb2 are stray capacitances on the PCB. C_pin is the pin input capacitance on the XC1 and XC2 pins, see ***Section 8.1.5 "32.768 kHz crystal oscillator (32k XOSC)"*** on page 42. The load capacitors C1 and C2 should have the same value. See ***Chapter 11 "Reference circuitry"*** on page 76 for the capacitance value used for C_pcb1 and C_pcb2 in reference circuitry.

3.6.3 32.768 kHz RC oscillator

The 32.768 kHz RC low frequency oscillator may be used as an alternative to the 32.768 kHz crystal oscillator. It has a frequency accuracy of less than ± 250 ppm in a stable temperature environment or when calibration is periodically performed in changing temperature environments. The 32.768 kHz RC oscillator does not require external components.

3.6.4 Synthesized 32.768 kHz clock

The low frequency clock can be synthesized from the high frequency clock. This saves the cost of a crystal but increases average power consumption as the high frequency clock source will have to be active.

3.7 GPIO

The general purpose I/O is organized as one port with up to 32 I/Os (dependent on package) enabling access and control of up to 32 pins through one port. Each GPIO can be accessed individually with the following user configurable features:

- Input/output direction
- Output drive strength
- Internal pull-up and pull-down resistors
- Wake-up from high or low level triggers on all pins
- Trigger interrupt on all pins
- All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels
- All pins can be individually configured to carry serial interface or quadrature demodulator signals

3.8 Debugger support

The two pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints and single stepping are part of this support.

4 Peripheral blocks

Peripheral blocks which have a register interface and/or interrupt vector assigned are instantiated, one or more times, in the device address space. The instances, associated ID (for those with interrupt vectors), and base address of features are found in ***Table 18*** on page 36**.** Detailed functional descriptions, configuration options, and register interfaces can be found in the *nRF51 Series Reference Manual*.

4.1 2.4 GHz radio (RADIO)

The nRF51 series 2.4 GHz RF transceiver is designed and optimized to operate in the worldwide ISM frequency band at 2.400 to 2.4835 GHz. Radio modulation modes and configurable packet structure enable interoperability with *Bluetooth*® low energy (BLE), ANT™, Enhanced ShockBurst™, and other 2.4 GHz protocol implementations.

The transceiver receives and transmits data directly to and from system memory for flexible and efficient packet data management. The nRF51 series transceiver has the following features:

- General modulation features
  - GFSK modulation
  - Data whitening
  - On-air data rates
    - 250 kbps
    - 1 Mbps
    - 2 Mbps
- Transmitter with programmable output power of +4 dBm to -20 dBm, in 4 dB steps
- Transmitter whisper mode -30 dBm
- RSSI function (1 dB resolution)
- Receiver with integrated channel filters achieving maximum sensitivity
  - -96 dBm at 250 kbps
  - -93 dBm at 1 Mbps BLE
  - -90 dBm at 1 Mbps
  - -85 dBm at 2 Mbps
- RF Synthesizer
  - 1 MHz frequency programming resolution
  - 1 MHz non-overlapping channel spacing at 1 Mbps and 250 kbps
  - 2 MHz non-overlapping channel spacing at 2 Mbps
  - Works with low-cost ± 60 ppm 16 MHz crystal oscillators
- Baseband controller
  - EasyDMA RX and TX packet transfer directly to and from RAM
  - Dynamic payload length
  - On-the-fly packet assembly/disassembly and AES CCM payload encryption
  - 8 bit, 16 bit, and 24 bit CRC check (programmable polynomial and initial value)

Note: EasyDMA is an integrated DMA implementation requiring no configuration to take advantage of flexible data management and avoids copying operations to and from RAM.

4.2 Timer/counters (TIMER)

The timer/counter runs on the high-frequency clock source (HFCLK) and includes a 4 bit ($1/2^X$) prescaler that can divide the HFCLK.

The TIMER will start requesting the 1 MHz mode of the HFCLK for values of the prescaler that gives f_{TIMER} less or equal to 1 MHz. If the timer module is the only one requesting the HFCLK, the system will automatically switch to using the 1 MHz mode resulting in a decrease in the current consumption. See the parameters $I_{1v2XO16,1M}$, $I_{1v2XO32,1M}$, $I_{1v2RC16,1M}$ in ***Table 32*** on page 47 and $I_{TIMER0/1/2,1M}$ in ***Table 52*** on page 61.

The task/event and interrupt features make it possible to use the PPI system for timing and counting tasks between any system peripheral including any GPIO of the device. The PPI system also enables the TIMER task/event features to generate periodic output and PWM signals to any GPIO. The number of input/outputs used at the same time is limited by the number of GPIOTE channels.

Instance	Bit-width	Capture/Compare registers
TIMER0	8/16/24/32	4
TIMER1	8/16	4
TIMER2	8/16	4

Table 12 *Timer/counter properties*

4.3 Real Time Counter (RTC)

The Real Time Counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). The RTC features a 24 bit COUNTER, 12 bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

Instance	Capture/Compare registers
RTC0	3
RTC1	4

Table 13 *RTC properties*

4.4 AES Electronic Codebook Mode Encryption (ECB)

The ECB encryption block supports 128 bit AES block encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption. ECB encryption uses EasyDMA to access system RAM for in-place operations on cleartext and ciphertext during encryption.

4.5 AES CCM Mode Encryption (CCM)

Cipher Block Chaining - Message Authentication Code (CCM) Mode is an authenticated encryption algorithm designed to provide both authentication and confidentiality during data transfer. CCM combines counter mode encryption and CBC-MAC authentication.

Note: The CCM terminology "Message Authentication Code (MAC)" is called the "Message Integrity Check (MIC)" in *Bluetooth* terminology and this document and the *nRF51 Series Reference Manual* are consistent with *Bluetooth* terminology.

The CCM block generates an encrypted keystream, applies it to the input data using the XOR operation, and generates the 4 byte MIC field in one operation. The CCM and radio can be configured to work synchronously, as described in the *nRF51 Series Reference Manual*. The CCM will encrypt in time for transmission and decrypt after receiving bytes into memory from the Radio. All operations can complete within the packet RX or TX time.

CCM on this device is implemented according to *Bluetooth* requirements and the algorithm as defined in IETF RFC3610, and depends on the AES-128 block cipher. A description of the CCM algorithm can also be found in the NIST Special Publication 800-38C. The *Bluetooth* Core Specification v4.0 describes the configuration of counter mode blocks and encryption blocks to implement compliant encryption for BLE.

The CCM block uses EasyDMA to load key, counter mode blocks (including the nonce required), and to read/write plain text and cipher text.

4.6 Accelerated Address Resolver (AAR)

Accelerated Address Resolver is a cryptographic support function to implement the "Resolvable Private Address Resolution Procedure" described in the *Bluetooth Core Specification* v4.1. "Resolvable Private Address Generation" should be achieved using ECB and is not supported by AAR. The procedure allows two devices that share a secret key to generate and resolve a hash based on their device address.

The AAR block enables real-time address resolution on incoming packets when configured according to the description in the *nRF51 Series Reference Manual*. This allows real-time packet filtering (whitelisting) using a list of known shared secrets (Identity Resolving Keys (IRK) in *Bluetooth*).

The following table outlines the properties of the AAR.

Instance	Number of IRKs supported for simultaneous resolution
AAR	8

Table 14 *AAR properties*

4.7 Random Number Generator (RNG)

The Random Number Generator (RNG) generates true non-deterministic random numbers derived from thermal noise that are suitable for cryptographic purposes. The RNG does not require a seed value.

4.8 Watchdog Timer (WDT)

A countdown watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up. The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU.

4.9 Temperature sensor (TEMP)

The temperature sensor measures die temperature over the temperature range of the device with 0.25° C resolution.

4.10 Serial Peripheral Interface (SPI/SPIS)

The SPI interfaces enable full duplex synchronous communication between devices. They support a three-wire (SCK, MISO, MOSI) bi-directional bus with fast data transfers. The SPI Master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus. Control of chip select signals is left to the application through use of GPIO signals. SPI Master has double buffered I/O data. The SPI Slave includes EasyDMA for data transfer directly to and from RAM allowing Slave data transfers to occur while the CPU is IDLE.

The GPIOs used for each SPI interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of printed circuit board space and signal routing.

The SPI peripheral supports SPI mode 0, 1, 2, and 3.

Instance	Master/Slave
SPI0	Master
SPI1	Master
SPIS1	Slave

Table 15 *SPI properties*

4.11 Two-wire interface (TWI)

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching, supporting data rates of 100 kbps and 400 kbps.

The GPIOs used for each two-wire interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

Instance	Master/Slave
TWI0	Master
TWI1	Master

Table 16 *Two-wire properties*

4.12 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in hardware up to 1 Mbps baud. Parity checking is supported.

The GPIOs used for each UART interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pinout and efficient use of board space and signal routing.

4.13 Quadrature Decoder (QDEC)

The quadrature decoder provides buffered decoding of quadrature-encoded sensor signals. It is suitable for mechanical and optical sensors with an optional LED output signal and input debounce filters. The sample period and accumulation are configurable to match application requirements.

4.14 Analog to Digital Converter (ADC)

The 10 bit incremental Analog to Digital Converter (ADC) enables sampling of up to 8 external signals through a front-end multiplexer. The ADC has configurable input and reference prescaling, and sample resolution (8, 9, and 10 bit).

Note: The ADC module uses the same analog inputs as the LPCOMP module (AIN0 - AIN7 and AREF0 - AREF1). Only one of the modules can be enabled at the same time.

4.15 GPIO Task Event blocks (GPIOTE)

A GPIOTE block enables GPIOs on Port 0 to generate events on pin state change which can be used to carry out tasks through the PPI system. A GPIO can also be driven to change state on system events using the PPI system. Low power detection of pin state changes on Port 0 is possible when in System ON or System OFF.

Instance	Number of GPIOTE channels
GPIOTE	4

Table 17 *GPIOTE properties*

4.16 Low Power Comparator (LPCOMP)

In System ON, the block can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

Note: The LPCOMP module uses the same analog inputs as the ADC module (AIN0 - AIN7 and AREF0 - AREF1). Only one of the modules can be enabled at the same time.

5 Instance table

The peripheral instantiation of the chip is shown in the table below.

ID	Base address	Peripheral	Instance	Description
0	0x40000000	POWER	POWER	Power Control.
0	0x40000000	CLOCK	CLOCK	Clock Control.
0	0x40000000	MPU	MPU	Memory Protection Unit.
1	0x40001000	RADIO	RADIO	2.4 GHz Radio.
2	0x40002000	UART	UART0	Universal Asynchronous Receiver/Transmitter.
3	0x40003000	SPI	SPI0	SPI Master.
3	0x40003000	TWI	TWI0	I2C compatible Two-Wire Interface 0.
4	0x40004000	SPIS	SPIS1	SPI Slave.
4	0x40004000	SPI	SPI1	SPI Master.
4	0x40004000	TWI	TWI1	I2C compatible Two-Wire Interface 1.
5				Unused.
6	0x40006000	GPIOTE	GPIOTE	GPIO Task and Events.
7	0x40007000	ADC	ADC	Analog to Digital Converter.
8	0x40008000	TIMER	TIMER0	Timer/Counter 0.
9	0x40009000	TIMER	TIMER1	Timer/Counter 1.
10	0x4000A000	TIMER	TIMER2	Timer/Counter 2.
11	0x4000B000	RTC	RTC0	Real Time Counter 0.
12	0x4000C000	TEMP	TEMP	Temperature Sensor.
13	0x4000D000	RNG	RNG	Random Number Generator.
14	0x4000E000	ECB	ECB	Crypto AES ECB.
15	0x4000F000	CCM	CCM	AES Crypto CCM.
15	0x4000F000	AAR	AAR	Accelerated Address Resolver.
16	0x40010000	WDT	WDT	Watchdog Timer.
17	0x40011000	RTC	RTC1	Real Time Counter 1.
18	0x40012000	QDEC	QDEC	Quadrature Decoder.
19	0x40013000	LPCOMP	LPCOMP	Low Power Comparator.
20 - 25				Reserved as software interrupt.
26 - 29				Unused.
30	0x4001E000	NVMC	NVMC	Non-Volatile Memory Controller.
31	0x4001F000	PPI	PPI	Programmable Peripheral Interconnect.
NA	0x50000000	GPIO	GPIO	General Purpose Input and Output.
NA	0x10000000	FICR	FICR	Factory Information Configuration Registers.
NA	0x10001000	UICR	UICR	User Information Configuration Registers.

Table 18 *Peripheral instance reference*

6 Absolute maximum ratings

Maximum ratings are the extreme limits the chip can be exposed to without causing permanent damage. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the chip. ***Table 19*** specifies the absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
Supply voltages				
VDD		-0.3	+3.9	V
DEC2			2	V
VSS			0	V
I/O pin voltage				
VIO		-0.3	VDD + 0.3	V
Environmental QFN48 package				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		2	
ESD HBM	Human Body Model		4	kV
ESD CDM	Charged Device Model		750	V
Environmental WLCSP package				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		1	
ESD HBM	Human Body Model		4	kV
ESD CDM	Charged Device Model		500	V
Flash memory				
Endurance		20 000[1]		write/erase cycles
Retention		10 years at 40 °C		
Number of times an address can be written between erase cycles			2	times

1. Flash endurance is 20,000 erase cycles. The smallest element of flash that can be written is a 32 bit word.

Table 19 *Absolute maximum ratings*

7 Operating conditions

The operating conditions are the physical parameters that the chip can operate within as defined in ***Table 20***.

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units
VDD	Supply voltage, internal LDO setup		1.8	3.0	3.6	V
VDD	Supply voltage, DC/DC converter setup		2.1	3.0	3.6	V
VDD	Supply voltage, low voltage mode setup	1	1.75	1.8	1.95	V
t_{R_VDD}	Supply rise time (0 V to VDD)	2			100	ms
T_A	Operating temperature		-25	25	75	°C

1. DEC2 shall be connected to VDD in this mode.
2. The on-chip power-on reset circuitry may not function properly for rise times outside the specified interval.

Table 20 *Operating conditions*

Nominal operating conditions (NOC) - conditions under which the chip is operated and tested are the typical (Typ.) values in ***Table 20***.

Extreme operating conditions (EOC) - conditions under which the chip is operated and tested are the minimum (Min.) and maximum (Max.) values in ***Table 20***.

7.1 WLCSP light sensitivity

The WLCSP package variant is sensitive to visible and near infrared light which means a final product design must shield the chip properly. The marking side is covered with a light absorbing film, while the side edges of the chip and the ball side must be protected by coating or other means.

8 Electrical specifications

This chapter contains electrical specifications for device interfaces and peripherals including radio parameters and current consumption.

The test levels referenced are defined in ***Table 21***.

Test level	Description
1	Simulated, calculated, by design (specification limit) or prototype samples tested at NOC.
2	Parameters have been verified at Test level 1 and in addition: Prototype samples tested at EOC.
3	Parameters have been verified at Test level 2 and in addition: Production samples tested at EOC in accordance with JEDEC47.
4	Parameters have been verified at Test level 3 and in addition: Production devices are limit tested at NOC.

Table 21 *Test level definitions*

8.1 Clock sources

8.1.1 16/32 MHz crystal startup

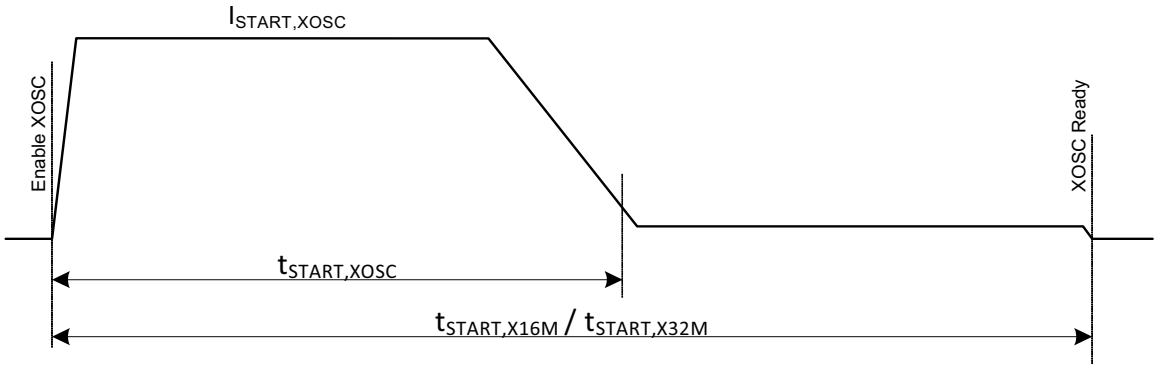

Figure 9 *Current drawn at oscillator startup*

Figure 9 shows the current drawn by the crystal oscillator (XOSC) at startup. The $t_{START,XOSC}$ period is the time needed for the oscillator to start clocking. The length of $t_{START,XOSC}$ is dependent on the crystal specifications.

The period following $t_{START,XOSC}$ to the end of $t_{START,X16M}$ /$t_{START,X32M}$ is fixed. This is the debounce period where the clock stabilizes before it is made available to rest of the system.

8.1.2 16 MHz crystal oscillator (16M XOSC)

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$f_{NOM,X16M}$	Crystal frequency.			16		MHz	N/A
$f_{TOL,X16M}$	Frequency tolerance.[1]				±50[2]	ppm	N/A
$f_{TOL,X16M,BLE}$	Frequency tolerance, *Bluetooth* low energy applications.[1]				±40[2]	ppm	N/A
$R_{S,X16M}$	Equivalent series resistance.	C0 ≤ 7 pF, $C_{L,MAX}$ ≤ 16 pF C0 ≤ 5 pF, $C_{L,MAX}$ ≤ 12 pF C0 ≤ 3 pF, $C_{L,MAX}$ ≤ 12 pF		50 75 100	100 150 200	Ω Ω Ω	N/A N/A N/A
$P_{D,X16M}$	Drive level.				100	µW	N/A
C_{pin}	Input capacitance on XC1 and XC2 pads.			4		pF	1
I_{X16M}	Run current for 16 MHz crystal oscillator.	SMD 2520 CL = 8 pF		470[3]		µA	1
$I_{X16M,1M}$	Run current for the 16 MHz crystal oscillator when used only for a Timer at 1 MHz or less.	SMD 2520 CL = 8pF		250[3]		µA	1
$I_{STBY,X16M}$	Standby current for 16 MHz crystal oscillator.[4]	SMD 2520 CL = 8 pF		25		µA	1
$I_{START,XOSC}$	Startup current for 16 MHz crystal oscillator.			1.1		mA	3
$t_{START,XOSC}$	Startup time for 16 MHz crystal oscillator.	SMD 2520 CL = 8 pF		400	500[5]	µs	2
$t_{START,X16M}$	Total startup time ($t_{START,XOSC}$ + debounce period).[6]	SMD 2520 CL = 8 pF		800		µs	1

1. The Frequency tolerance relates to the amount of time the radio can be in transmit mode. See ***Table 38*** on page 51.
2. Includes initial tolerance of the crystal, drift over temperature, aging, and frequency pulling due to incorrect load capacitance.
3. This number includes the current used by the automated power and clock management system.
4. Standby current is the current drawn by the oscillator when there are no resources requesting the 16M, meaning there is no clock management active (see ***Table 33*** on page 48). This value will depend on type of crystal.
5. Crystals with other specification than SMD 2520 may have much longer startup times.
6. This is the time from when the crystal oscillator is powered up until its output becomes available to the system. It includes both the crystal startup time and the debounce period.

Table 22 *16 MHz crystal oscillator*

8.1.3 32 MHz crystal oscillator (32M XOSC)

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$f_{NOM,X32M}$	Crystal frequency.			32		MHz	N/A
$f_{TOL,X32M}$	Frequency tolerance.[1]				±50[2]	ppm	N/A
$f_{TOL,X32M,BLE}$	Frequency tolerance, *Bluetooth* low energy applications.[1]				±40[2]	ppm	N/A
$R_{S,X32M}$	Equivalent series resistance.	C0 ≤ 7 pF, $C_{L,MAX}$ ≤ 12 pF C0 ≤ 5 pF, $C_{L,MAX}$ ≤ 12 pF C0 ≤ 3 pF, $C_{L,MAX}$ ≤ 9 pF		30 40 50	60 80 100	Ω Ω Ω	N/A N/A N/A
$P_{D,X32M}$	Drive level.				100	µW	N/A
C_{pin}	Input capacitance on XC1 and XC2 pads.			4		pF	1
I_{X32M}	Run current for 32 MHz crystal oscillator.	SMD 2520 CL = 8 pF		500[3]		µA	1
$I_{X32M,1M}$	Run current for the 32 MHz crystal oscillator when used only for a Timer at 1 MHz or less.	SMD 2520 CL = 8 pF		300[3]		µA	1
$I_{STBY,X32M}$	Standby current for 32 MHz crystal oscillator.[4]	SMD 2520 CL = 8 pF		30		µA	1
$I_{START,XOSC}$	Startup current for 32 MHz crystal oscillator.			1.1		mA	3
$t_{START,XOSC}$	Startup time for 32 MHz crystal oscillator.	SMD 2520 CL = 8 pF		300	400[5]	µs	1
$t_{START,X32M}$	Total startup time ($t_{START,XOSC}$ + debounce period).[6]	SMD 2520 CL = 8 pF		750		µs	1

1. The Frequency tolerance relates to the amount of time the radio can be in transmit mode. See ***Table 38*** on page 51.
2. Includes initial tolerance of the crystal, drift over temperature, aging and frequency pulling due to incorrect load capacitance.
3. This number includes the current used by the automated power and clock management system.
4. Standby current is the current drawn by the oscillator when there are no resources requesting the 32M, meaning there is no clock management active (see ***Table 33*** on page 48). This value will depend on type of crystal.
5. Crystals with other specification than SMD 2520 may have much longer startup times.
6. This is the time from when the crystal oscillator is powered up until its output becomes available to the system. It includes both the crystal startup time and the debounce period.

Table 23 *32 MHz crystal oscillator*

8.1.4 16 MHz RC oscillator (16M RCOSC)

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$f_{NOM,RC16M}$	Nominal frequency.		16		MHz	N/A
$f_{TOL,RC16M}$	Frequency tolerance.		±1	±5	%	3
I_{RC16M}	Run current for 16 MHz RC oscillator.		750[1]		µA	1
$I_{RC16M,1M}$	Run current for 16 MHz RCOSC when used only for a Timer at 1 MHz or less.		540[1]		µA	1
$t_{START,RC16M}$	Startup time for 16 MHz RC oscillator.		4.2	5.2	µs	1
$I_{RC16M, START}$	Startup current for 16 MHz RC oscillator.		400		µA	1

1. This number includes the current used by the automated power and clock management system.

Table 24 *16 MHz RC oscillator*

8.1.5 32.768 kHz crystal oscillator (32k XOSC)

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$f_{NOM,X32k}$	Crystal frequency.		32.768		kHz	N/A
$f_{TOL,X32k,BLE}$	Frequency tolerance, *Bluetooth* low energy applications.			±250	ppm	N/A
$C_{L,X32k}$	Load capacitance.			12.5	pF	N/A
$C_{0,X32k}$	Shunt capacitance.			2	pF	N/A
$R_{S,X32k}$	Equivalent series resistance.		50	80	kΩ	N/A
$P_{D,X32k}$	Drive level.			1	µW	N/A
C_{pin}	Input capacitance on XL1 and XL2 pads.		4		pF	1
I_{X32k}	Run current for 32.768 kHz crystal oscillator.		0.4	1	µA	1
$I_{START,X32k}$	Startup current for 32.768 kHz crystal oscillator.		1.3	1.8	µA	1
$t_{START,X32k}$	Startup time for 32.768 kHz crystal oscillator.		0.3	1	s	2

Table 25 *32.768 kHz crystal oscillator*

8.1.6 32.768 kHz RC oscillator (32k RCOSC)

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$f_{NOM,RC32k}$	Nominal frequency.			32.768		kHz	N/A
$f_{TOL,RC32k}$	Frequency tolerance.			±2		%	3
$f_{TOL,CAL,RC32k}$	Frequency tolerance.	Calibration interval 4 s			±250	ppm	1
I_{RC32k}	Run current.		0.5	0.8	1.1	µA	1
$t_{START,RC32k}$	Startup time.			390	487	µs	1

Table 26 *32.768 kHz RC oscillator*

8.1.7 32.768 kHz Synthesized oscillator (32k SYNT)

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$f_{NOM,SYNT32k}$	Nominal frequency.			32.768		kHz	1
$f_{TOL,SYNT}$	Frequency tolerance.			$f_{TOL,XO16M}$ ±8 $f_{TOL,XO32M}$ ±8		ppm	1
$I_{SYNT32k}$	Run and startup current for 32.768 kHz Synthesized clock including the 16M XOSC.			15		µA	1
$t_{START,SYNT32k}$	Startup time for 32.768 kHz Synthesized clock.			406		µs	1

Table 27 *32.768 kHz Synthesized oscillator*

8.2 Power management

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
V_{POF}	Nominal power level warning thresholds (falling supply voltage).	Accuracy as defined by V_{TOL}		2.1 2.3 2.5 2.7		V	2
V_{TOL}	Threshold voltage tolerance.				±5	%	3
V_{HYST}	Threshold voltage hysteresis.	V_{POF} = 2.1 V V_{POF} = 2.3 V V_{POF} = 2.5 V V_{POF} = 2.7 V		46 62 79 100		mV	3

Table 28 *Power Fail Comparator*

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$t_{HOLDRESETNORMAL}$	Hold time for reset pin when doing a pin reset.[1]	0.2			µs	1
$t_{HOLDRESETDEBUG}$	Hold time for reset pin when doing a pin reset during debug.[1,2]	100			µs	1

1. SWDCLK pin must be kept low during reset.
2. Bit 0 in the RESET register in the power management module must be set to 1 to enable reset during debug.

Table 29 *Pin Reset*

Power on reset time (t_{POR}) is the time from when the supply starts rising to when the device comes out of reset and the CPU starts. The time increases with, and is inclusive of, supply rise time from 0 V to VDD. ***Table 30*** gives t_{POR} for a number of supply rise times, simulated with a linear ramp from 0 V to VDD, over the supply voltage range 1.8 V to 3.6 V.

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$t_{POR, 10\ \mu s}$	Power on reset time, 10 µs rise time (0 V to VDD).		0.7	2.4	19	ms	1
$t_{POR, 1\ ms}$	Power on reset time, 10 µs rise time (0 V to VDD).		1.7	3.4	20	ms	1
$t_{POR, 10\ ms}$	Power on reset time, 10 µs rise time (0 V to VDD).		11	12	28	ms	1
$t_{POR, 100\ ms}$	Power on reset time, 10 µs rise time (0 V to VDD).		68	101	115	ms	1

Table 30 *Power on reset time*

The data in ***Figure 10*** and ***Table 31*** show measured $t_{\_POR}$ data. Measurements were taken using the reference circuit shown in ***Section 11.3.1 "QFAA QFN48 schematic with internal LDO setup"*** on page 79 with the given supply voltage and temperature conditions.

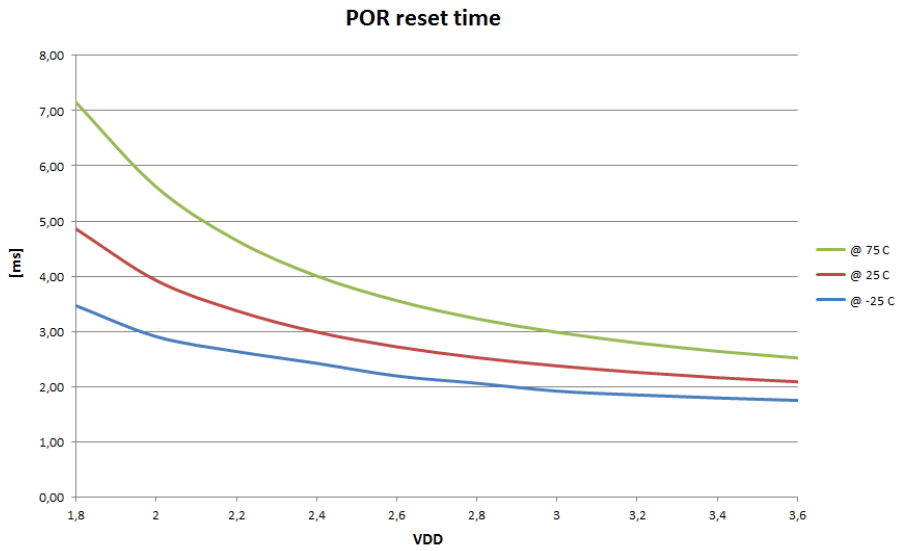

Figure 10 *Power on reset time (Test level 2)*

VDD	Rise Time from 10% to 90% of VDD
1.8	570 µs
3.0	605 µs
3.6	635 µs

Table 31 *Supply rise time at sample voltages for the measured data shown in* ***Figure 10****.*

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
I_{OFF}	Current in SYSTEM OFF, no RAM retention.			0.6[1]		µA	2
$I_{OFF, RET, 8k}$	Additional current in SYSTEM OFF per retained RAM block (8 kB)			0.6[1]		µA	2
I_{OFF2ON}	OFF to CPU execute transition current.			400		µA	1
t_{OFF2ON}	OFF to CPU execute.			9.6	10.6	µs	1
$I_{ON,16k}$	SYSTEM-ON base current with 16 kB RAM enabled.			2.6[1]		µA	2
$I_{ON,32k}$	SYSTEM-ON base current with 32 kB RAM enabled.			3.8[1]		µA	2
t_{1V2}	Startup time for 1V2 regulator.			2.3		µs	1
$I_{1V2XO16}$	Current drawn by 1V2 regulator and 16 MHz XOSC when both are on at the same time.	See ***Table 33*** on page 48.		810[2]		µA	1
$I_{1V2XO32}$	Current drawn by 1V2 regulator and 32 MHz XOSC when both are on at the same time.	See ***Table 33*** on page 48.		840[2]		µA	1
$I_{1V2RC16}$	Current drawn by 1V2 regulator and 16 MHz RCOSC when both are on at the same time.	See ***Table 33*** on page 48.		880[2]		µA	1
$I_{1V2XO16,1M}$	For HFCLK in 1 MHz mode[3]. Current drawn by 1V2 regulator and 16 MHz XOSC when both are on at the same time.	See ***Table 33*** on page 48.		520[2]		µA	1
$I_{1V2XO32,1M}$	For HFCLK in 1 MHz mode[3]. Current drawn by 1V2 regulator and 32 MHz XOSC when both are on at the same time.	See ***Table 33*** on page 48.		560[2]		µA	1
$I_{1V2RC16,1M}$	For HFCLK in 1 MHz mode[3]. Current drawn by 1V2 regulator and 16 MHz RCOSC when both are on at the same time.	See ***Table 33*** on page 48.		630[2]		µA	1
t_{XO}	Startup time for the clock management system when the XTAL is in standby.			2.3	5.3	µs	1

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
t_{1V7}	Startup time for 1V7 regulator			2	3.6	µs	1
I_{1V7}	Current drawn by 1V7 regulator			105		µA	2
F_{DCDC}	DC/DC converter current conversion factor.		0.65[4]		1.2[4]		1

1. Add 1 µA to the current value if the device is used in Low voltage mode.
2. This number includes the current used by the automated power and clock management system.
3. For details on 1 MHz mode, see ***Section 4.2 "Timer/counters (TIMER)"*** on page 32.
4. F_{DCDC} will vary depending on VDD and internal radio current consumption (I_{DD}). Please refer to the *nRF51 Series Reference Manual*, v3.0 or later, for a method to calculate $I_{DD,DCDC}$. See ***Figure 11*** on page 50 for a DC/DC conversion factor chart.

Table 32 *Power management*

8.3 Block resource requirements

Block	ID	Resource requirements				Comment
		1V2	HFCLK[1]	LFCLK	1V7	
Radio	1	x	x			Requires HFCLK XOSC.
UART	2	x	x			When receiver or transmitter are STARTed.
SPIS	4	x	x			Requested when CSN asserts.
SPI	3, 4	x	x			
TWI	3, 4	x	x			
GPIOTE	6	x	x			Only in input mode.
ADC	7	x	x			Requires HFCLK XOSC.
TIMER	8, 9, 10		x			Requires 1V2 when a TIMER EVENT is triggered.
RTC	11, 17			x		HFCLK will be requested if the LFCLK is synthesized from HFCLK.
TEMP	12	x	x			Requires HFCLK XOSC.
RNG	13	x	x			
ECB	14	x	x			
WDT	16			x		HFCLK will be requested if the LFCLK is synthesized from HFCLK.
QDEC	18	x	x			
LPCOMP	19					No resources required.
CPU	--	x	x		x	

1. HFCLK could be one of the following; RC16M, XO16M, or XO32M.

Table 33 *Clock and power requirements for different blocks*

8.4 CPU

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$I_{CPU, FLASH}$	Run current at 16 MHz (XOSC). Executing code from flash memory.		4.1[1]		mA	2
$I_{CPU, RAM}$	Run current at 16 MHz (XOSC). Executing code from RAM.		2.4[2]		mA	1
$I_{START, CPU}$	CPU startup current.		600		µA	1
$t_{START, CPU}$	IDLE to CPU execute.	0[3]			µs	1

1. Includes CPU, flash, 1V2, 1V7, RC16M.
2. Includes CPU, RAM, 1V2, RC16M.
3. t_{1V2} if 1V2 regulator is not running already.

Table 34 *CPU specifications*

8.5 Radio transceiver

8.5.1 General radio characteristics

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
f_{OP}	Operating frequencies.	1 MHz channel spacing.	2400		2483	MHz	N/A
PLL_{res}	PLL programming resolution.			1		MHz	N/A
Δf250	Frequency deviation at 250 kbps.			±170		kHz	2
Δf_{1M}	Frequency deviation at 1 Mbps.			±170		kHz	2
Δf_{2M}	Frequency deviation at 2 Mbps.			±320		kHz	2
Δf_{BLE}	Frequency deviation at BLE.		±225	±250	±275	kHz	4
bps_{FSK}	On-air data rate.		250		2000	kbps	N/A

Table 35 *General radio characteristics*

8.5.2 Radio current consumption with DC/DC disabled

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$I_{TX,+4dBm}$	TX only run current at P_{OUT} = +4 dBm.	1		16		mA	4
$I_{TX,0dBm}$	TX only run current at P_{OUT} = 0 dBm.	1		10.5		mA	4
$I_{TX,-4dBm}$	TX only run current at P_{OUT} = -4 dBm.	1		8		mA	2
$I_{TX,-8dBm}$	TX only run current at P_{OUT} = -8 dBm.	1		7		mA	2
$I_{TX,-12dBm}$	TX only run current at P_{OUT} = -12 dBm.	1		6.5		mA	2
$I_{TX,-16dBm}$	TX only run current at P_{OUT} = -16 dBm.	1		6		mA	2
$I_{TX,-20dBm}$	TX only run current at P_{OUT} = -20 dBm.	1		5.5		mA	2
$I_{TX,-30dBm}$	TX only run current at P_{OUT} = -30 dBm.	1		5.5		mA	2
$I_{START,TX}$	TX startup current.	2		7		mA	1
$I_{RX,250}$	RX only run current at 250 kbps.			12.6		mA	1
$I_{RX,1M}$	RX only run current at 1 Mbps.			13		mA	4
$I_{RX,2M}$	RX only run current at 2 Mbps.			13.4		mA	1
$I_{START,RX}$	RX startup current.	3		8.7		mA	1

1. Valid for data rates 250 kbps, 1 Mbps, and 2 Mbps.
2. Average current consumption (at 0 dBm TX output power) for TX startup (130 µs), and when changing mode from RX to TX (130 µs).
3. Average current consumption for RX startup (130 µs), and when changing mode from TX to RX (130 µs).

Table 36 *Radio current consumption with DC/DC disabled (NOC, VDD = 3 V)*

8.5.3 Radio current consumption with DC/DC enabled

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$I_{TX,+4dBm}$	TX only run current at P_{OUT} = +4 dBm.	1		11.8		mA	2
$I_{TX,0dBm}$	TX only run current at P_{OUT} = 0 dBm.	1		8.0		mA	2
$I_{TX,-4dBm}$	TX only run current at P_{OUT} = -4 dBm.	1		6.3		mA	2
$I_{TX,-8dBm}$	TX only run current at P_{OUT} = -8 dBm.	1		5.6		mA	2
$I_{TX,-12dBm}$	TX only run current at P_{OUT} = -12 dBm.	1		5.3		mA	2
$I_{TX,-16dBm}$	TX only run current at P_{OUT} = -16 dBm.	1		5.0		mA	2
$I_{TX,-20dBm}$	TX only run current at P_{OUT} = -20 dBm.	1		4.7		mA	2
$I_{TX,-30dBm}$	TX only run current at P_{OUT} = -30 dBm.	1		4.7		mA	2
$I_{RX,1M}$	RX only run current at 1 Mbps.			9.7		mA	2

1. Valid for data rates 250 kbps, 1 Mbps, and 2 Mbps.

Table 37 *Radio current consumption with DC/DC enabled (NOC, VDD = 3 V)*

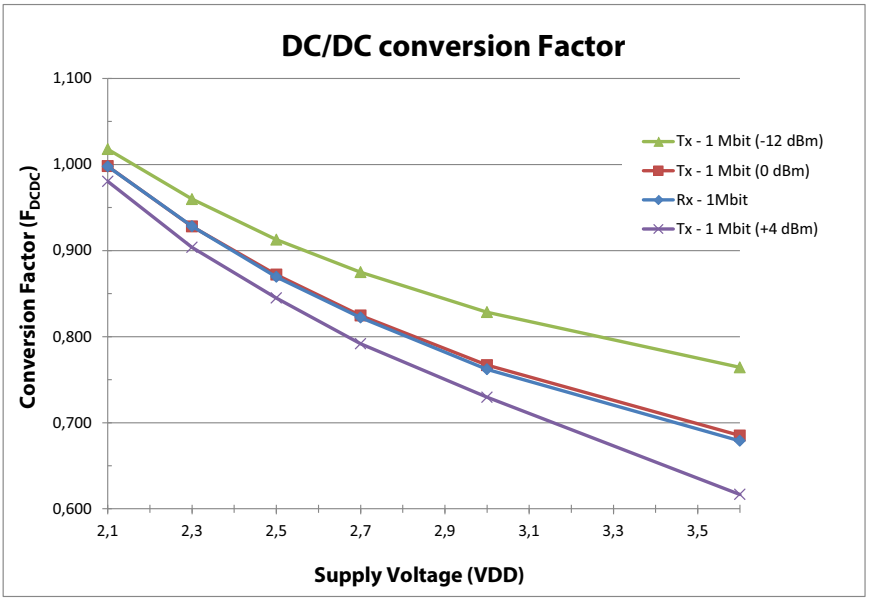

Figure 11 *DC/DC conversion factor as function of VDD*

See Power chapter in the *nRF51 Series Reference Manual* on how to use the DC/DC conversion factor to calculate the actual power consumption.

8.5.4 Transmitter specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
P_{RF}	Maximum output power.		4		dBm	4
P_{RFC}	RF power control range.	20	24		dB	2
PRFCR	RF power accuracy.			±4	dB	1
P_{WHISP}	RF power whisper mode.		-30		dBm	2
P_{BW2}	20 dB bandwidth for modulated carrier (2 Mbps).		1800	2000	kHz	2
P_{BW1}	20 dB bandwidth for modulated carrier (1 Mbps).		950	1100	kHz	2
P_{BW250}	20 dB bandwidth for modulated carrier (250 kbps).		700	800	kHz	2
$P_{RF1.2}$	1^{st} Adjacent Channel Transmit Power. ±2 MHz (2 Mbps).			-20	dBc	2
$P_{RF2.2}$	2^{nd} Adjacent Channel Transmit Power. ±4 MHz (2 Mbps).			-45	dBc	2
$P_{RF1.1}$	1^{st} Adjacent Channel Transmit Power. ±1 MHz (1 Mbps).			-20	dBc	2
$P_{RF2.1}$	2^{nd} Adjacent Channel Transmit Power. ±2 MHz (1 Mbps).			-40	dBc	2
$P_{RF1.250}$	1^{st} Adjacent Channel Transmit Power. ±1 MHz (250 kbps).			-25	dBc	2
$P_{RF2.250}$	2^{nd} Adjacent Channel Transmit Power. ±2 MHz (250 kbps).			-40	dBc	2
$t_{TX,30}$	Maximum consecutive transmission time, f_{TOL} < ±30 ppm.			16	ms	1
$t_{TX,60}$	Maximum consecutive transmission time, f_{TOL} < ±60 ppm.			4	ms	1

Table 38 *Transmitter specifications*

8.5.5 Receiver specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
Receiver operation						
PRX_{MAX}	Maximum received signal strength at < 0.1% PER.		0		dBm	1
$PRX_{SENS,2M}$	Sensitivity (0.1% BER) at 2 Mbps.		-85		dBm	2
$PRX_{SENS,1M}$	Sensitivity (0.1% BER) at 1 Mbps.		-90		dBm	2
$PRX_{SENS,250k}$	Sensitivity (0.1% BER) at 250 kbps.		-96		dBm	2
P_{SENS} IT 1 Mbps BLE	Receiver sensitivity: Ideal transmitter.		-93		dBm	2
P_{SENS} DT 1 Mbps BLE	Receiver sensitivity: Dirty transmitter.[1]		-91		dBm	2
RX selectivity - modulated interfering signal[2]						
	2 Mbps					
C/I_{CO}	C/I co-channel.		12		dB	2
C/I_{1ST}	1^{st} ACS, C/I 2 MHz.		-4		dB	2
C/I_{2ND}	2^{nd} ACS, C/I 4 MHz.		-24		dB	2
C/I_{3RD}	3^{rd} ACS, C/I 6 MHz.		-28		dB	2
C/I_{6th}	6^{th} ACS, C/I 12 MHz.		-44		dB	2
C/I_{Nth}	N^{th} ACS, C/I f_i > 25 MHz.		-50		dB	2
	1 Mbps					
C/I_{CO}	C/I co-channel (1 Mbps).		12		dB	2
C/I_{1ST}	1^{st} ACS, C/I 1 MHz.		4		dB	2
C/I_{2ND}	2^{nd} ACS, C/I 2 MHz.		-24		dB	2
C/I_{3RD}	3^{rd} ACS, C/I 3 MHz.		-30		dB	2
C/I_{6th}	6^{th} ACS, C/I 6 MHz.		-40		dB	2
C/I_{12th}	12^{th} ACS, C/I 12 MHz.		-50		dB	2
C/I_{Nth}	N^{th} ACS, C/I f_i > 25 MHz.		-53		dB	2

Symbol	Description	Min.	Typ.	Max.	Units	Test level
	250 kbps					
C/I_{CO}	C/I co-channel.		4		dB	2
C/I_{1ST}	1^{st} ACS, C/I 1 MHz.		-10		dB	2
C/I_{2ND}	2^{nd} ACS, C/I 2 MHz.		-34		dB	2
C/I_{3RD}	3^{rd} ACS, C/I 3 MHz.		-39		dB	2
C/I_{6th}	6^{th} ACS, C/I f_i > 6 MHz.		-50		dB	2
C/I_{12th}	12^{th} ACS, C/I 12 MHz.		-55		dB	2
C/I_{Nth}	N^{th} ACS, C/I f_i > 25 MHz.		-60		dB	2
	***Bluetooth* Low Energy RX selectivity**					
C/I_{CO}	C/I co-channel.		10		dB	2
C/I_{1ST}	1^{st} ACS, C/I 1 MHz.		1		dB	2
C/I_{2ND}	2^{nd} ACS, C/I 2 MHz.		-25		dB	2
C/I_{3+N}	ACS, C/I (3+n) MHz offset [n = 0, 1, 2, . . .].		-51		dB	2
C/I_{Image}	Image blocking level.		-30		dB	2
$C/I_{Image\pm1MHz}$	Adjacent channel to image blocking level (±1 MHz).		-31		dB	2
RX intermodulation[3]						
P_IMD_{2Mbps}	IMD performance, 2 Mbps, 3rd, 4th, and 5th offset channel.		-41		dBm	2
P_IMD_{1Mbps}	IMD performance, 1 Mbps, 3rd, 4th, and 5th offset channel.		-40		dBm	2
$P\_IMD_{250kbps}$	IMD performance, 250 kbps, 3rd, 4th, and 5th offset channel.		-36		dBm	2
P_IMD_{BLE}	IMD performance, 1 Mbps BLE, 3rd, 4th, and 5th offset channel.		-39		dBm	2

1. As defined in the *Bluetooth Core Specification* v4.0 Volume 6: Core System Package (Low Energy Controller Volume).
2. Wanted signal level at P_{IN} = -67 dBm. One interferer is used, having equal modulation as the wanted signal. The input power of the interferer where the sensitivity equals BER = 0.1% is presented.
3. Wanted signal level at P_{IN} = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is not modulated, the other interferer is modulated equal with the wanted signal. The input power of interferers where the sensitivity equals BER = 0.1% is presented.

Table 39 *Receiver specifications*

8.5.6 Radio timing parameters

Symbol	Description	250 k	1 M	2 M	BLE	Jitter	Units
t_{TXEN}	Time between TXEN task and READY event.	132	132	132	140	0	µs
$t_{TXDISABLE}$	Time between DISABLE task and DISABLED event when the radio was in TX.	10	4	3	4	1	µs
t_{RXEN}	Time between the RXEN task and READY event.	130	130	130	138	0	µs
$t_{RXDISABLE}$	Time between DISABLE task and DISABLED event when the radio was in RX.	0	0	0	0	1	µs
$t_{TXCHAIN}$	TX chain delay.	5	1	0.5	1	0	µs
$t_{RXCHAIN}$	RX chain delay.	12.5	3	2	3	0	µs

Table 40 *Radio timing*

8.5.7 Antenna matching network requirements

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$Z_{QFN48,ANT1,2}$	Optimum differential impedance at 2.4 GHz seen into the matching network from pin ANT1 and ANT2 on the QFN48 packet.		15 + j85		Ω	1
$Z_{WLCSP,ANT1,2}$	Optimum differential impedance at 2.4 GHz seen into the matching network from pin ANT1 and ANT2 on the WLCSP packet.		12.6 + j106		Ω	1

Table 41 *Optimum differential load impedance*

8.6 Received Signal Strength Indicator (RSSI) specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$RSSI_{ACC}$	RSSI accuracy.	Valid range -50 dBm to -80 dBm.			±6	dB	2
$RSSI_{RESOLUTION}$	RSSI resolution.			1		dB	1
$RSSI_{PERIOD}$	Sample period.		8.8			µs	1
$RSSI_{CURRENT}$	Current consumption in addition to I_{RX}.			250		µA	1

Table 42 *RSSI specifications*

8.7 Universal Asynchronous Receiver/Transmitter (UART) specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
I_{UART1M}	Run current at max baud rate.			230		µA	1
$I_{UART115k}$	Run current at 115200 bps.			220		µA	1
$I_{UART1k2}$	Run current at 1200 bps.			210		µA	1
f_{UART}	Baud rate for UART.		1.2		1000	kbps	N/A
t_{CTSH}	CTS high time.		1			µs	1

Table 43 *UART specifications*

8.8 Serial Peripheral Interface Slave (SPIS) specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$I_{SPIS125K}$	Run current for SPI slave at 125 kbps.[1]		180		µA	1
I_{SPIS2M}	Run current for SPI slave at 2 Mbps.[1]		183		µA	1
f_{SPIS}	Bit rates for SPIS.	0.125		2	Mbps	N/A

1. CSN asserted.

Table 44 SPIS specifications

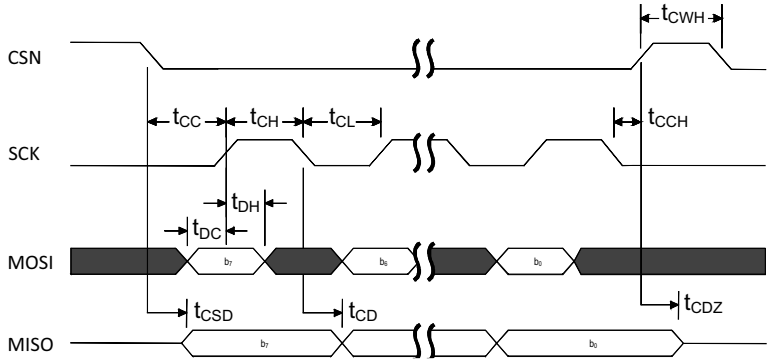

***Figure 12** SPIS timing diagram, one byte transmission, SPI Mode 0*

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
t_{DC}	Data to SCK setup.		10			ns	1
t_{DH}	SCK to Data hold.		10			ns	1
t_{CSD}	CSN to Data valid.	Low power mode.[1] Constant latency mode.[1]			7100 2100	ns	1
t_{CD}	SCK to Data Valid.	C_{LOAD} = 10 pF			97[2]	ns	1
t_{CL}	SCK Low time.		40			ns	1
t_{CH}	SCK High time.		40			ns	1
t_{CC}	CSN to SCK Setup.	Low power mode.[1] Constant latency mode.[1]	7000 2000			ns	1
t_{CCH}	Last SCK edge to CSN Hold.		2000			ns	1
t_{CWH}	CSN Inactive time.		300			ns	1
t_{CDZ}	CSN to Output High Z.				40	ns	1
f_{SCK}	SCK frequency.		0.125		2	MHz	1
t_R,t_F	SCK Rise and Fall time.				100	ns	1

1. For more information on how to control the sub power modes, see the *nRF51 Series Reference Manual*.
2. Increases/decreases with 1.2 ns/pF load.

Table 45 SPIS timing parameters

8.9 Serial Peripheral Interface (SPI) Master specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$I_{SPI125K}$	Run current for SPI master at 125 kbps.		180		µA	1
I_{SPI4M}	Run current for SPI master at 4 Mbps.		200		µA	1
f_{SPI}	Bit rates for SPI.	0.125		4	Mbps	N/A

Table 46 *SPI specifications*

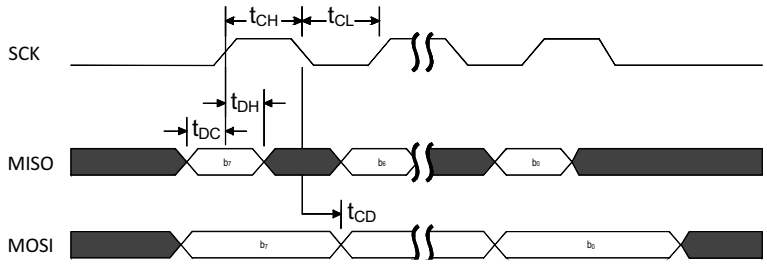

Figure 13 *SPI timing diagram, one byte transmission, SPI mode 0*

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
t_{DC}	Data to SCK setup.		10			ns	1
t_{DH}	SCK to Data hold.		10			ns	1
t_{CD}	SCK to Data valid.	C_{LOAD} = 10 pF			97[1]	ns	1
t_{CL}	SCK Low time.		40			ns	1
t_{CH}	SCK High time.		40			ns	1
f_{SCK}	SCK Frequency.		0.125		4	MHz	1
t_R,t_F	SCK Rise and Fall time.				100	ns	1

1. Increases/decreases with 1.2 ns/pF load.

Table 47 *SPI timing parameters*

8.10 I2C compatible Two Wire Interface (TWI) specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
I_{2W100K}	Run current for TWI at 100 kbps.			380		µA	1
I_{2W400K}	Run current for TWI at 400 kbps.			400		µA	1
f_{2W}	Bit rates for TWI.		100		400	kbps	N/A
$t_{TWI,START}$	Time from STARTRX/STARTTX task is given until start condition.	Low power mode.[1] Constant latency mode.[1]		3 1	4.4	µs	1

1. For more information on how to control the sub power modes, see the *nRF51 Series Reference Manual*.

Table 48 *TWI specifications*

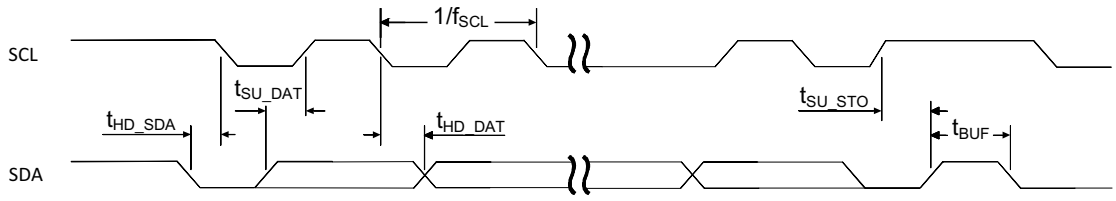

Figure 14 *SCL/SDA timing*

Symbol	Description	Standard Min.	Standard Max.	Fast Min.	Fast Max.	Units	Test level
f_{SCL}	SCL clock frequency.		100		400	kHz	1
t_{HD_STA}	Hold time for START and repeated START condition.	5200		1300		ns	1
t_{SU_DAT}	Data setup time before positive edge on SCL.	300		300		ns	1
t_{HD_DAT}	Data hold time after negative edge on SCL.	300		300		ns	1
t_{SU_STO}	Setup time from SCL goes high to STOP condition.	5200		1300		ns	1
t_{BUF}	Bus free time between STOP and START conditions.	4700		1300		ns	1

Table 49 *TWI timing parameters*

8.11 GPIO Tasks and Events (GPIOTE) specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
$I_{GPIOTE,IN}$	Run current with 1 or more GPIOTE active channels in Input mode.		22		µA	1
$I_{GPIOTE,OUT}$	Run current with 1 or more GPIOTE active channels in Output mode.		0.1		µA	1
$I_{GPIOTE,IDLE}$	Run current when all channels in Idle mode. PORT event can be generated with a delay of up to t_{1V2}.		0.1		µA	1

Table 50 *GPIOTE specifications*

Note: Setting up one or more GPIO DETECT signals to generate PORT EVENT, which can be used either as a wakeup source or to give an interrupt, will not lead to an increase of the current consumption.

8.12 Analog to Digital Converter (ADC) specifications

Note: HFCLK XOSC is required to get the stated ADC accuracy.

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
DNL_{10b}	Differential non-linearity (10 bit mode).			< 1		LSB	2
INL_{10b}	Integral non-linearity (10 bit mode).			2		LSB	2
V_{OS}	Offset error.		-2		+2	%	2
e_G	Gain error.	1	-2		+2	%	2
V_{REF_VBG}	Internal Band Gap reference voltage (VBG).			1.20 V		V	2
$V_{REF\_VBG\_ERR}$	Internal Band Gap reference voltage error.		-1.5		+1.5	%	2
$TC_{REF\_VBG\_DRIFT}$	Internal Band Gap reference voltage drift.		-200		+200	ppm/°C	2
V_{REF_EXT}	External reference voltage (AREF0/1).		0.83	1.2	1.3	V	1
$V_{REF\_VDD\_LIM}$	Limited supply voltage range for ADC using VDD with prescaler as the reference. CONFIG.REFSEL = SupplyOneHalfPrescaling CONFIG.REFSEL = SupplyOneThirdPrescaling		1.7 2.5		2.6 3.6	V V	1 1
t_{ADC10b}	Time required to convert a single sample in 10 bit mode.			68		µs	1
t_{ADC9b}	Time required to convert a single sample in 9 bit mode.			36		µs	1
t_{ADC8b}	Time required to convert a single sample in 8 bit mode.			20		µs	1
I_{ADC}	Current drawn by ADC during conversion.			260		µA	1
ADC_ERR_1V8	Absolute error when used for battery measurement at 1.8 V, 2.2 V, 2.6 V, 3.0 V, and 3.4 V.	2		3		LSB	2
ADC_ERR_2V2				2		LSB	2
ADC_ERR_2V6				1		LSB	2
ADC_ERR_3V0				1		LSB	2
ADC_ERR_3V4				1		LSB	2

1. Source impedance less than 5 kΩ.
2. Internal reference, input from VDD/3, 10 bit mode.

Table 51 *Analog to Digital Converter (ADC) specifications*

8.13 Timer (TIMER) specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$I_{TIMER0/1/2}$	Timer current when running from HFCLK in 16 MHz mode.			30		µA	1
$I_{TIMER0/1/2,1M}$	Timer current when running from HFCLK in 1 MHz mode.			4		µA	1
$t_{TIMER,START}$	Time from START task is given until timer starts counting.			0.25		µs	1

***Table 52** Timer specifications*

8.14 Real Time Counter (RTC)

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I_{RTC}	Timer (LFCLK source).		0.1		µA	1

***Table 53** RTC*

8.15 Temperature sensor (TEMP)

Note: HFCLK XOSC is required to get the stated accuracy.

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I_{TEMP}	Run current for Temperature sensor.		185		µA	1
t_{TEMP}	Time required for temperature measurement.		35		µs	1
T_{RANGE}	Temperature sensor range.	-25		75	°C	N/A
T_{ACC}	Temperature sensor accuracy.[1]	-4		+4	°C	N/A
T_{RES}	Temperature sensor resolution.		0.25		°C	1

1. Stated temperature accuracy is valid in the range 0 to 60°C.
Temperature accuracy outside the 0 to 60°C range is ± 8°C.

***Table 54** Temperature sensor*

8.16 Random Number Generator (RNG) specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
I_{RNG}	Run current at 16 MHz.			60		µA	1
$t_{RNG,RAW}$	Run time per byte in RAW mode.	Uniform distribution of 0 and 1 is not guaranteed.		167		µs	1
$t_{RNG,UNI}$	Run time per byte in Uniform mode.	Uniform distribution of 0 and 1 is guaranteed. Time to generate a byte cannot be guaranteed.		677		µs	1

Table 55 *Random Number Generator (RNG) specifications*

8.17 AES Electronic Codebook Mode Encryption (ECB) specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I_{ECB}	Run current for ECB.		550		µA	1
$t_{STARTECB, ENDECB}$	Time for a 16 byte AES block encrypt.		8.5	17	µs	1

Table 56 *ECB specifications*

8.18 AES CCM Mode Encryption (CCM) specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I_{CCM}	Run current for CCM.		550		µA	1

Table 57 *CCM specifications*

8.19 Accelerated Address Resolver (AAR) specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I_{AAR}	Run current for AAR.		550		µA	1
$t_{START,RESOLVED}$	Time for address resolution of 8 IRKs.		68		µs	1

Table 58 *AAR specifications*

8.20 Watchdog Timer (WDT) specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I_{WDT}	Run current for watchdog timer.		0.1		µA	1
t_{WDT}	Time out interval, watchdog timer.	30 µs		36 hrs		1

Table 59 *Watchdog Timer specifications*

8.21 Quadrature Decoder (QDEC) specifications

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
I_{QDEC}				12		µA	1
t_{SAMPLE}	Time between sampling signals from quadrature decoder.		128		16384	µs	N/A
t_{LED}	Time from LED is turned on to signals are sampled.	Only valid for optical sensors.	0		511	µs	N/A

Table 60 *Quadrature Decoder specifications*

8.22 Non-Volatile Memory Controller (NVMC) specifications

Flash write is done by executing a program that writes one word (32 bit) consecutively after the other to the flash memory.

The program doing the flash writes could be set up to run from flash or from RAM. The timing of one flash write operation depends on whether the next instructions following the flash write will be fetched from flash or from RAM. Any fetch from flash done before the write operation is finished will give $t_{WRITE,FLASH}$ timing.

The flash memory is organized in 256 byte rows starting at CODE and UICR start address. Crossing from one row to another will affect the flash write timing when running from RAM.

The time it takes to program the flash memory will depend on different parameters:

- Whether the program doing the flash write is running from RAM or running from flash.
- When running from RAM we will have different timing for:
  - First write operation.
  - Repeated write operations within the same row.
  - Repeated write operation that are crossing from one row to another.

Symbol	Description	Note	Min.	Typ.	Max.	Units	Test level
$t_{ERASEALL}$	Erase flash memory.	1, 2			22.3	ms	1
$t_{PAGEERASEALL}$	Erase page in flash memory.	1, 2			22.3	ms	1
$t_{WRITE,FLASH}$	Program running from flash. Write one word to flash memory.	1, 3			46.3	µs	1
$t_{WRITE,RAM,1st}$	Program running from RAM. Write the first word to flash memory.	1			39.3	µs	1
$t_{WRITE,RAM,2nd}$	Program running from RAM. Repeated writes operations following the first, within the same row.	1			22.3	µs	1
$t_{WRITE,RAM,3rd}$	Program running from RAM. Repeated write operation, new word is located on a different row compare to the previous write.	1			46.3	µs	1

1. Max timing is assuming using RC16M, worst case tolerance.
2. The CPU will be halted for the duration of NVMC operations if the CPU tries to fetch data/code from the flash memory.
3. The CPU will be halted for the duration of NVMC operations.

Table 61 *NVMC specifications*

8.23 General Purpose I/O (GPIO) specifications

Symbol	Parameter (condition)	Note	Min.	Typ.	Max.	Units
V_{IH}	Input high voltage.		0.7 VDD		VDD	V
V_{IL}	Input low voltage.		VSS		0.3 VDD	V
V_{OH}	Output high voltage (std. drive, 0.5 mA).		VDD-0.3		VDD	V
V_{OH}	Output high voltage (high-drive, 5 mA).	1	VDD-0.3		VDD	V
V_{OL}	Output low voltage (std. drive, 0.5 mA).		VSS		0.3	V
V_{OL}	Output low voltage (high-drive, 5 mA).		VSS		0.3	V
R_{PU}	Pull-up resistance.		11	13	16	kΩ
R_{PD}	Pull-down resistance.		11	13	16	kΩ

1. Maximum number of pins with 5 mA high drive is 3.

Table 62 *General Purpose I/O (GPIO) specifications*

8.24 Low Power Comparator (LPCOMP) specifications

Symbol	Description	Min.	Typ.	Max.	Units	Test level
I_{LPC}	Run current for LPCOMP.		0.5		µA	1
$t_{LPCANADETOFF}$	Time from VIN crossing to ANADETECT signal generated when in System OFF.			15[1]	µs	1
$t_{LPCANADETON}$	Time from VIN crossing to ANADETECT signal generated when in System ON.			15[1]	µs	1
$t_{LPCOMPSTARTUP}$	Startup time for the Low Power Comparator.			40	µs	1

1. For 50 mV overdrive

Table 63 *Low power comparator specifications*

9 Mechanical specifications

This chapter covers the mechanical specifications for all chip variants of the nRF51822. The following table lists the cross references to the package sections describing each package variant.

Package	Cross references
QFN48	***Section 9.1 "QFN48 package"*** on page 66
CDAB	***Section 9.2 "CDAB WLCSP package"*** on page 67
CEAA	***Section 9.3 "CEAA WLCSP package"*** on page 68
CFAC	***Section 9.4 "CFAC WLCSP package"*** on page 69

Table 64 *Cross references to package variants*

9.1 QFN48 package

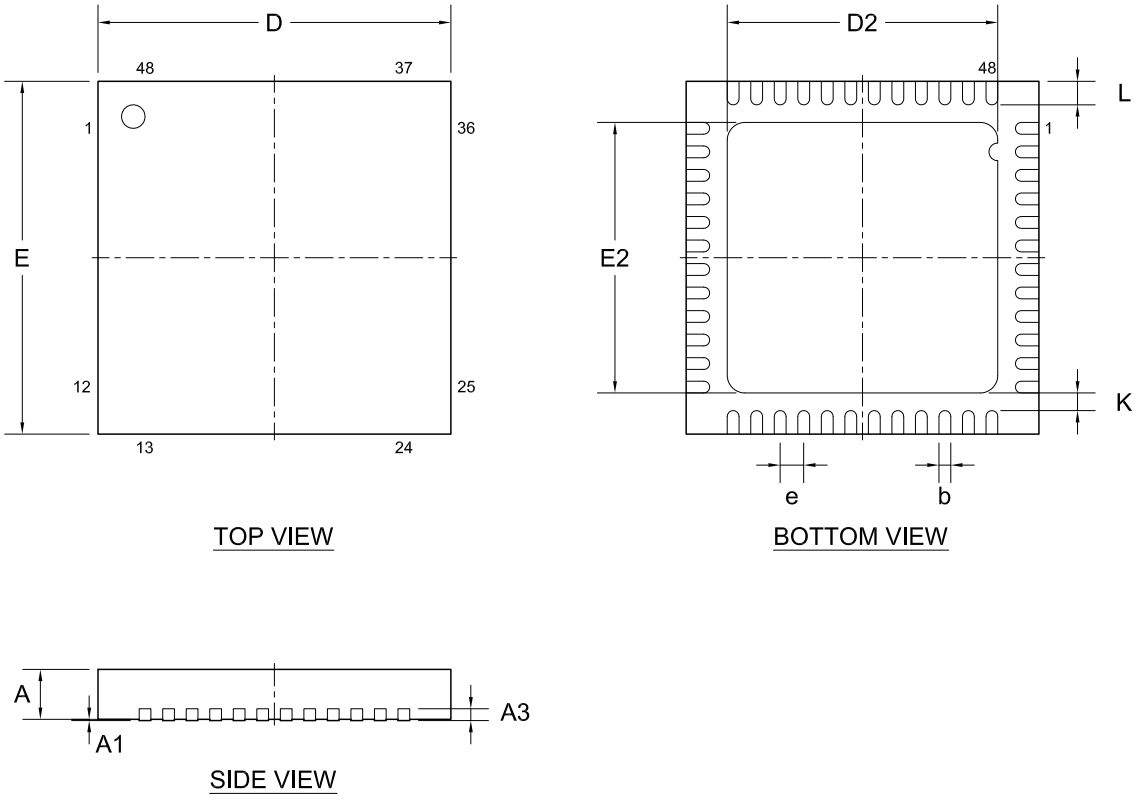

Figure 15 *QFN48 6 x 6 mm package*

Package	A	A1	A3	b	D, E	D2, E2	e	K	L	
QFN48 (6 x 6)	0.80	0.00	0.2	0.15	6.0	4.50	0.4	0.20	0.35	**Min.**
	0.85	0.02		0.20		4.60			0.40	**Nom.**
	0.90	0.05		0.25		4.70			0.45	**Max.**

Table 65 *QFN48 dimensions in millimeters*

9.2 CDAB WLCSP package

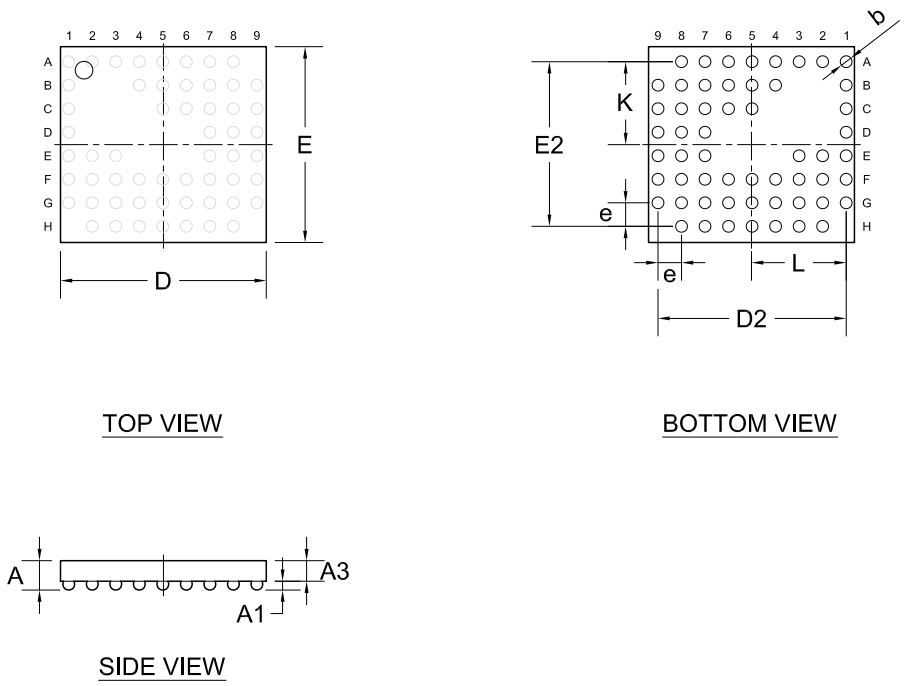

Figure 16 *CDAB WLCSP package*

Package	A	A1	A3	b	D	E	D2	E2	e	K	L	
		0.12	0.33	0.16	3.45	3.28						**Min.**
CDAB WLCSP	0.50	0.15	0.35	0.20	3.50	3.33	3.2	2.8	0.4	1.41	1.61	**Nom.**
	0.55	0.18	0.37	0.24	3.55	3.38						**Max.**

Table 66 *CDAB WLCSP package dimensions in millimeters*

9.3 CEAA WLCSP package

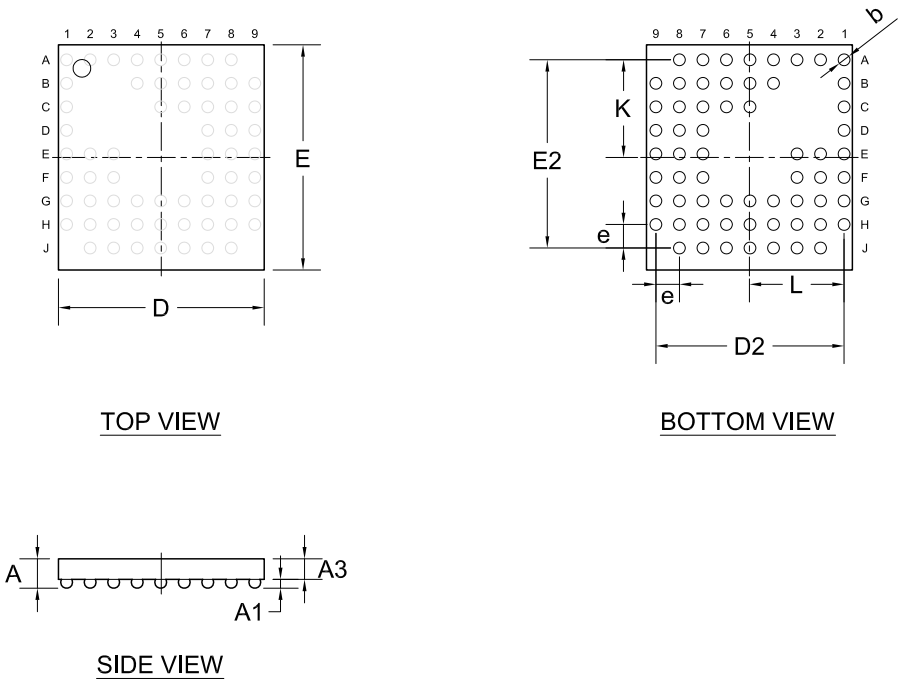

Figure 17 *CEAA WLCSP package*

Package	A	A1	A3	b	D	E	D2	E2	e	K	L	
		0.12	0.33	0.16	3.45	3.78						**Min.**
CEAA WLCSP	0.50	0.15	0.35	0.20	3.50	3.83	3.2	3.2	0.4	1.66	1.61	**Nom.**
	0.55	0.18	0.37	0.24	3.55	3.88						**Max.**

Table 67 *CEAA WLCSP package dimensions in millimeters*

9.4 CFAC WLCSP package

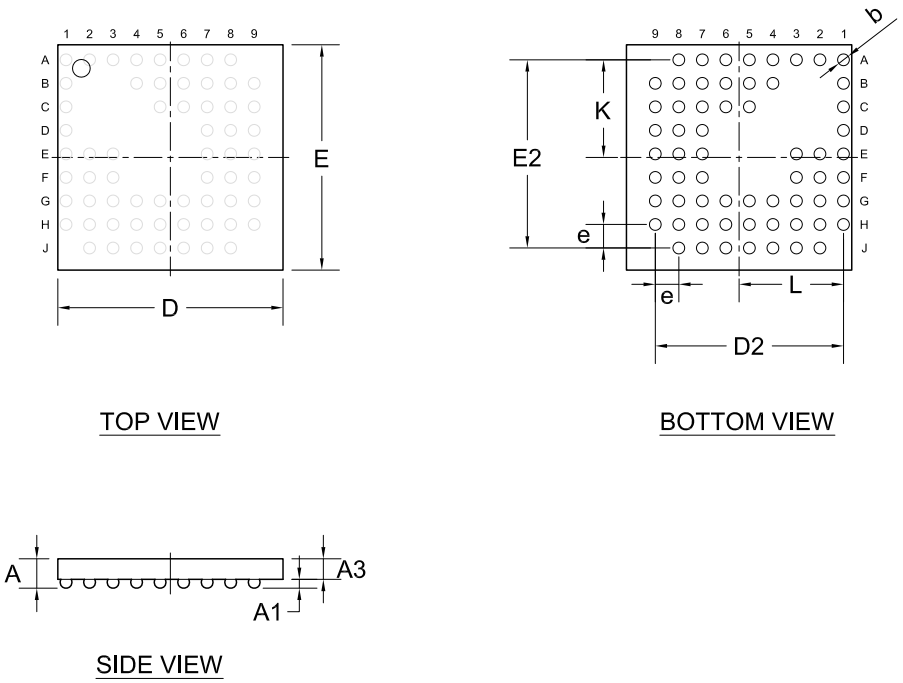

Figure 18 *CFAC WLCSP package*

Package	A	A1	A3	b	D	E	D2	E2	e	K	L	
		0.12	0.33	0.16	3.78	3.78						**Min.**
CFAC WLCSP	0.50	0.15	0.35	0.20	3.83	3.83	3.2	3.2	0.4	1.66	1.78	**Nom.**
	0.55	0.18	0.37	0.24	3.88	3.88						**Max.**

Table 68 *CFAC WLCSP package dimensions in millimeters*

10 Ordering information

10.1 Chip marking

N	5	1	8	2	2
<P	P>	<V	V>	<H>	<P>
<Y	Y>	<W	W>	<L	L>

Table 69 *Package marking*

10.2 Inner box label

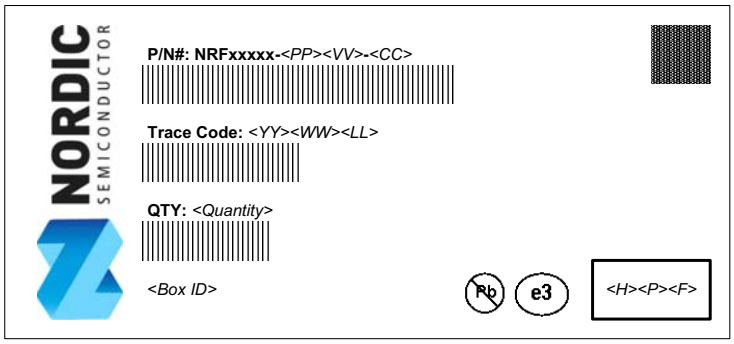

Figure 19 *Inner box label*

10.3 Outer box label

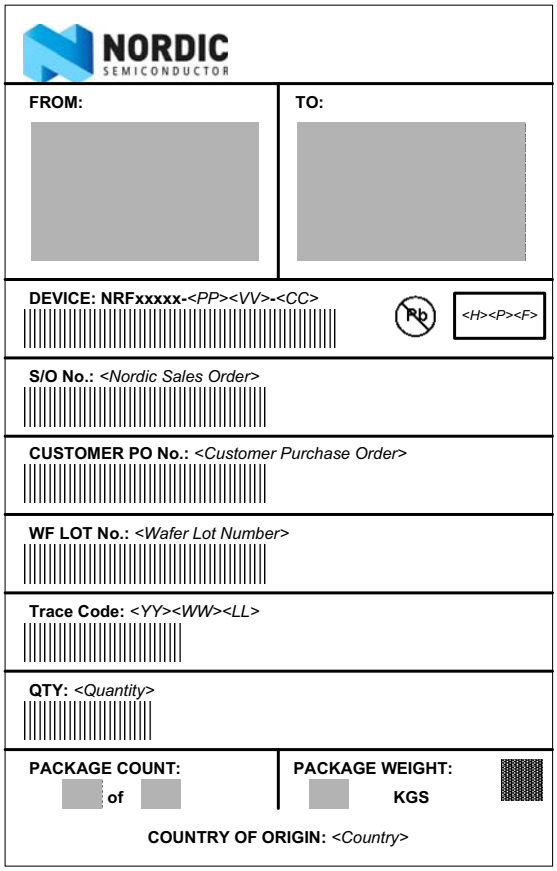

Figure 20 *Outer box label*

10.4 Order code

n	R	F	5	1	8	2	2	-	<P	P>	<V	V>	-	<C	C>

Table 70 *Order code*

10.5 Abbreviations

Abbreviation	Definition and Implemented Codes
N51/nRF51	nRF51 series product
822	Part code
<PP>	Package code
<VV>	Variant code
<H><P><F>	Build code H - Hardware version code P - Production configuration code (production site, etc.) F - Firmware version (Only visible on shipping container label)
<YY><WW><LL>	Tracking code YY - Year code WW - Assembly week number LL - Wafer lot code
<CC>	Container code

Table 71 *Abbreviations*

10.6 Code ranges and values

<PP>	Packet	Size (mm)	Pin/Ball Count	Pitch (mm)
QF	QFN	6 x 6	48	0.4
CD	WLCSP	3.50 x 3.33	56	0.4
CE	WLCSP	3.50 x 3.83	62	0.4
CF	WLCSP	3.83 x 3.83	62	0.4

Table 72 *Package codes*

<VV>	Flash (kB)	RAM (kB)	DC/DC Bond-out
AA	256	16	YES
AB	128	16	YES
AC	256	32	YES

Table 73 *Variant codes*

<H>	Description
[A. .Z]	Hardware version/revision identifier (incremental)

Table 74 *Hardware version codes*

<P>	Description
[0. .9]	Production device identifier (incremental)
[A. .Z]	Engineering device identifier (incremental)

Table 75 *Production version codes*

<F>	Description
[A. .N, P. .Z]	Version of programmed firmware
[0]	Delivered without preprogrammed firmware

Table 76 *Firmware version codes*

<YY>	Description
[12. .99]	Production year: 2012 to 2099

Table 77 *Year codes*

<WW>	Description
[1. .52]	Week of production

Table 78 *Week codes*

<LL>	Description
[AA. .ZZ]	Wafer production lot identifier

Table 79 *Lot codes*

<CC>	Description
R7	7″ Reel
R	13″ Reel
T	Tray

Table 80 *Container codes*

10.7 Product options

10.7.1 nRF ICs

Order code	MOQ[1]
nRF51822-QFAA-R7 nRF51822-QFAB-R7 nRF51822-QFAC-R7	1000
nRF51822-QFAA-R nRF51822-QFAB-R nRF51822-QFAC-R	3000
nRF51822-CEAA-R7 nRF51822-CDAB-R7 nRF51822-CFAC-R7	1500
nRF51822-CEAA-R nRF51822-CDAB-R nRF51822-CFAC-R	7000
nRF51822-QFAA-T nRF51822-QFAB-T nRF51822-QFAC-T	490

1. Minimum Order Quantity.

Table 81 *Order code*

10.7.2 Development tools

Order code	Description
nRF51-DK[1]	nRF51 *Bluetooth* Smart/ANT/2.4 GHz RF Development Kit
nRF51-Dongle[1]	nRF51 USB dongle for emulator, sniffer, firmware development

1. Uses the nRF51422-QFAC version of the chip (capable of running both *Bluetooth* low energy and ANT).

Table 82 *Development tools*

11 Reference circuitry

For the following reference layouts, C_pcb1 and C_pcb2, between X1 and XC1/XC2, is estimated to 0.5 pF each.

The exposed center pad of the QFN48 package must be connected to supply ground for proper device operation.

11.1 PCB guidelines

A well designed PCB is necessary to achieve good RF performance. A poor layout can lead to loss in performance or functionality. A qualified RF layout for the IC and its surrounding components, including matching networks, can be downloaded from www.nordicsemi.com.

To ensure optimal performance it is essential that you follow the schematics- and layout references closely. Especially in the case of the antenna matching circuitry (components between device pins ANT1,ANT2, VDD_PA and the antenna), any changes to the layout can change the behavior, resulting in degradation of RF performance or a need to change component values. All the reference circuits are designed for use with a 50 ohm single end antenna.

A PCB with a minimum of two layers, including a ground plane, is recommended for optimal performance. On PCBs with more than two layers, put a keep-out area on the inner layers directly below the antenna matching circuitry (components between device pins **ANT1**, **ANT2**, **VDD_PA**, and the antenna) to reduce the stray capacitances that influence RF performance.

A matching network is needed between the differential RF pins **ANT1** and **ANT2** and the antenna, to match the antenna impedance (normally 50 ohm) to the optimum RF load impedance for the chip. For optimum performance, the impedance for the matching network should be set as described in ***Section 8.5.7 "Antenna matching network requirements"*** on page 54 along with the recommended QFN48 package reference circuitry from ***Section 11.3 "QFAA QFN48 package"*** on page 79 and WLCSP package reference circuitry from ***Section 11.7 "CEAA WLCSP package"*** on page 103.

The DC supply voltage should be decoupled as close as possible to the VDD pins with high performance RF capacitors. See the schematics for recommended decoupling capacitor values. The supply voltage for the chip should be filtered and routed separately from the supply voltages of any digital circuitry.

Long power supply lines on the PCB should be avoided. All device grounds, VDD connections, and VDD bypass capacitors must be connected as close as possible to the IC. For a PCB with a topside RF ground plane, the VSS pins should be connected directly to the ground plane. For a PCB with a bottom ground plane, the best technique is to have via holes as close as possible to the VSS pads. A minimum of one via hole should be used for each VSS pin.

Full-swing digital data or control signals should not be routed close to the crystal or the power supply lines. Capacitive loading of full-swing digital output lines should be minimized in order to avoid radio interference.

11.1.1 PCB layout example

The PCB layout shown in ***Figure 21*** is a reference layout for the QFN package with internal LDO setup. For all available reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

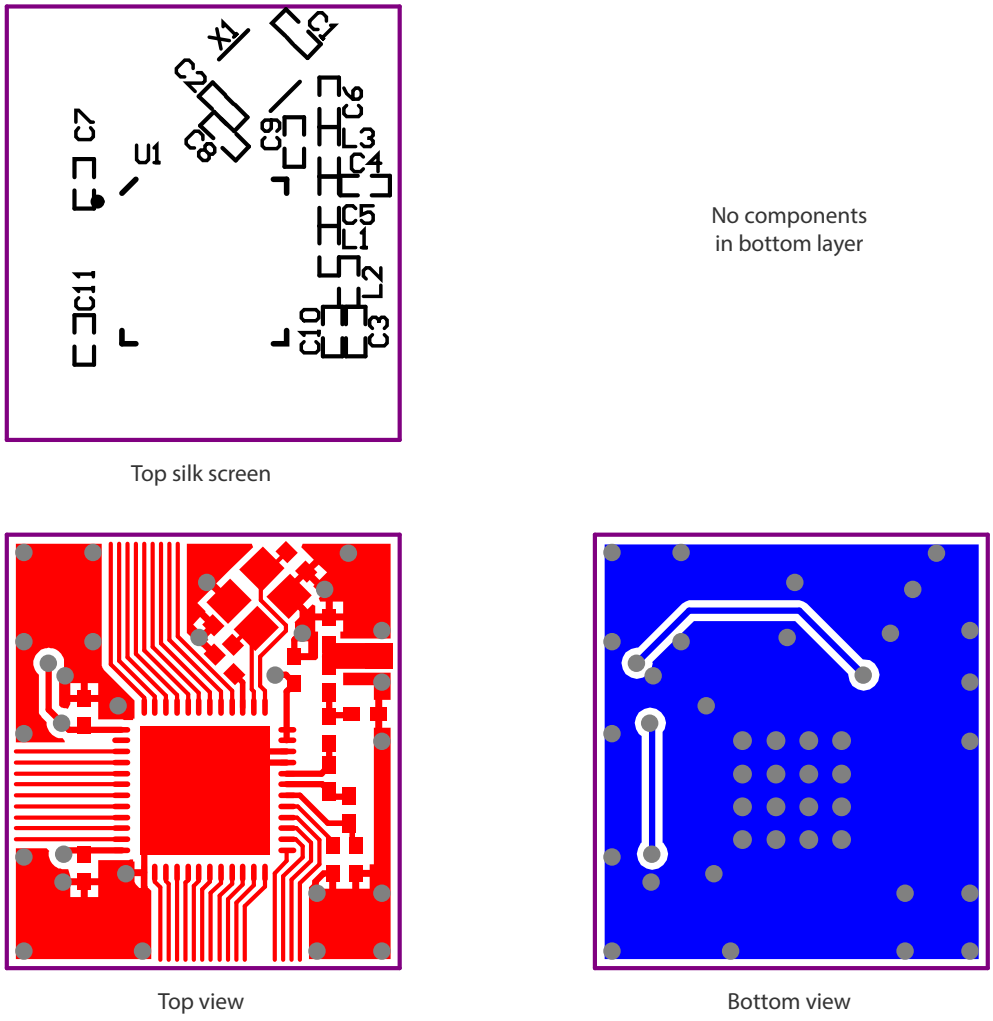

Figure 21 *PCB layout example for QFN48 package with internal LDO setup*

11.2 Reference design schematics

The following sections covers the reference design schematics for all chip variants of the nRF51822. ***Table 83*** lists the cross references to the package sections describing each package variant.

For package	See section:
QFAA	***Section 11.3 "QFAA QFN48 package"*** on page 79
QFAB	***Section 11.4 "QFAB QFN48 package"*** on page 85
QFAC	***Section 11.5 "QFAC QFN48 package"*** on page 91
CDAB	***Section 11.6 "CDAB WLCSP package"*** on page 97
CEAA	***Section 11.7 "CEAA WLCSP package"*** on page 103
CFAC	***Section 11.8 "CFAC WLCSP package"*** on page 109

Table 83 *Cross references to the reference design variants*

11.3 QFAA QFN48 package

Documentation for the QFAA QFN48 package reference circuit, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from www.nordicsemi.com.

11.3.1 QFAA QFN48 schematic with internal LDO setup

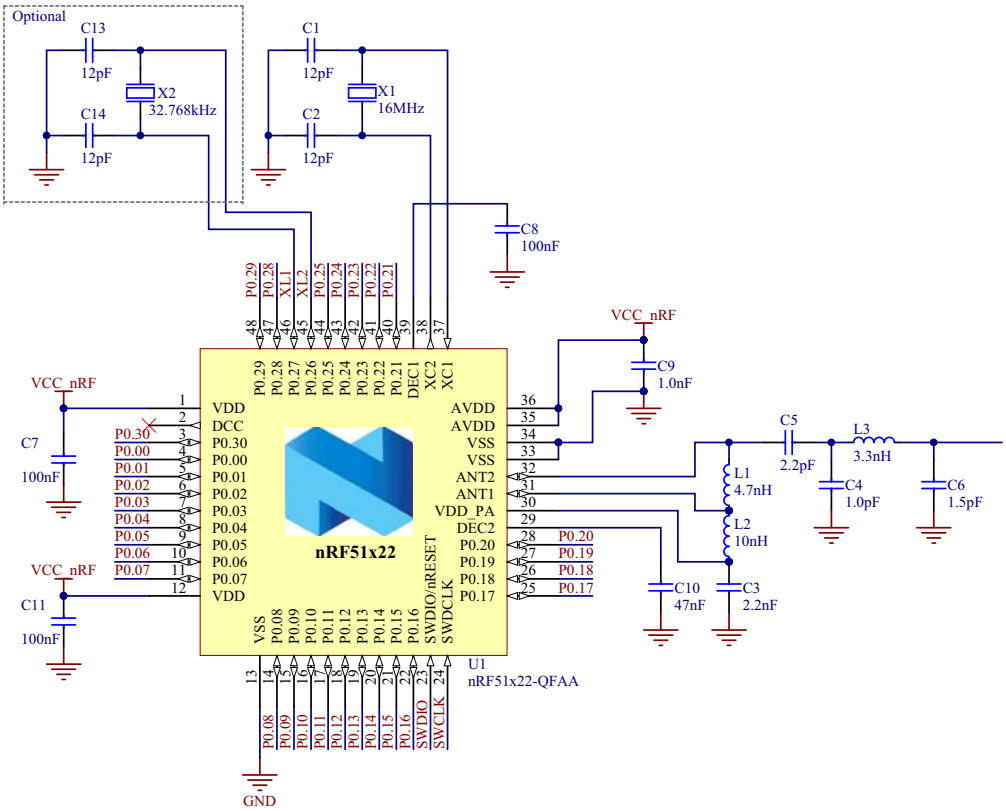

Figure 22 *QFAA QFN48 with internal LDO setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.3.1.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	10 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
U1	nRF51822-QFAA	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 84 *QFAA QFN48 with internal LDO setup*

11.3.2 QFAA QFN48 schematic with low voltage mode setup

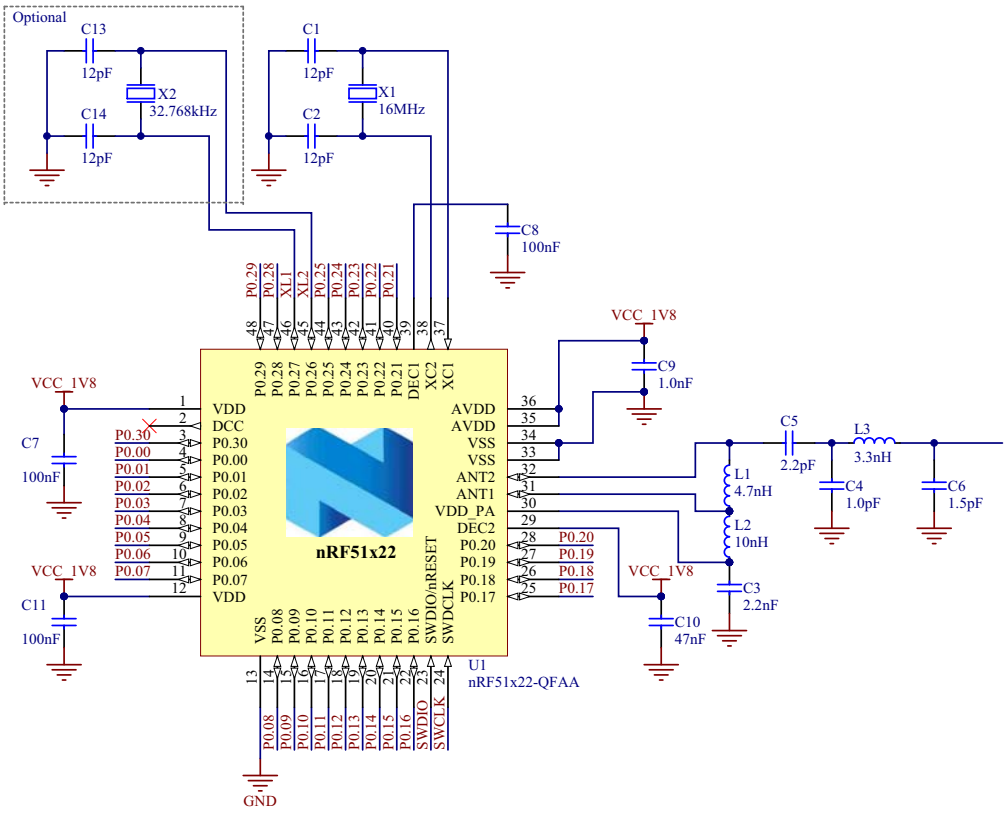

Figure 23 *QFAA QFN48 with low voltage mode setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.3.2.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	10 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
U1	nRF51822-QFAA	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 85 *QFAA QFN48 with low voltage mode setup*

11.3.3 QFAA QFN48 schematic with DC/DC converter setup

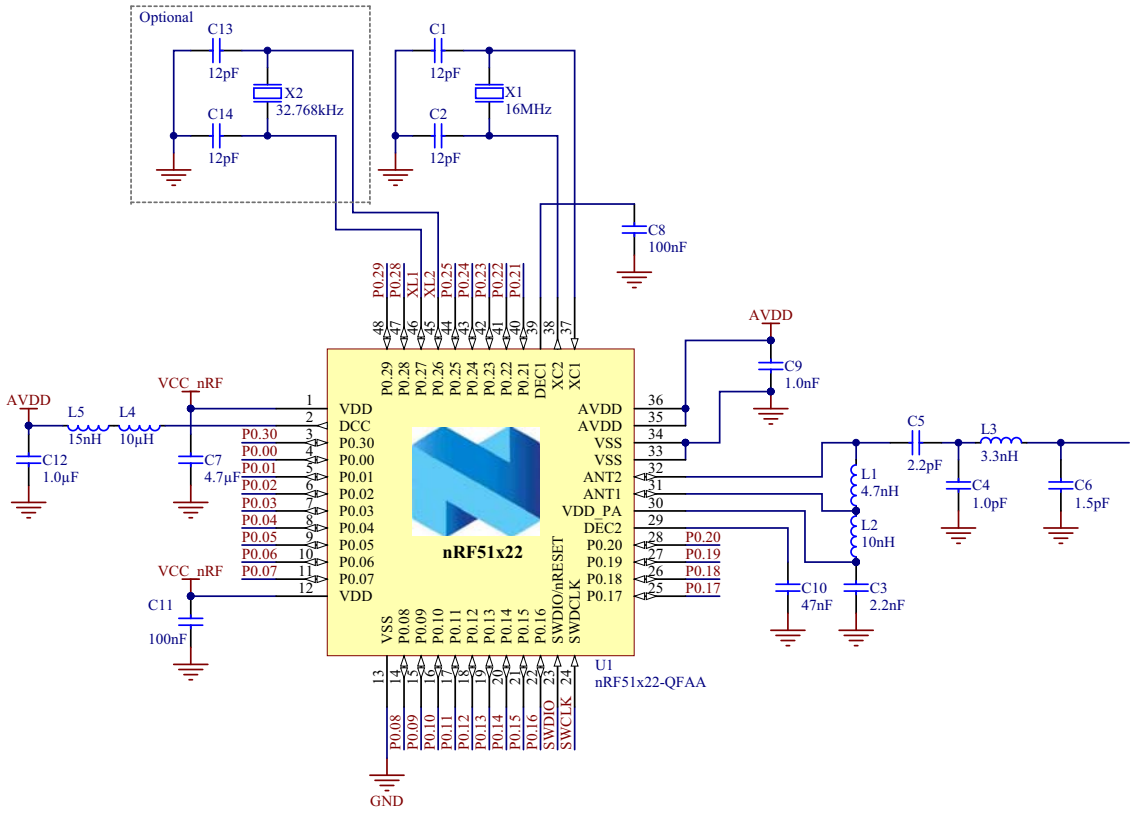

Figure 24 *QFAA QFN48 with DC/DC converter setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.3.3.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7	4.7 µF	Capacitor, X5R, ±10%	0603
C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
C12	1.0 µF	Capacitor, X7R, ±10%	0603
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	10 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
L4	10 µH	Chip inductor, $I_{DC,min}$ = 50 mA, ±20%	0603
L5	15 nH	High frequency chip inductor ±10%	0402
U1	nRF51822-QFAA	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 86 *QFAA QFN48 with DC/DC converter setup*

11.4 QFAB QFN48 package

Documentation for the QFAB QFN48 package reference circuit, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from www.nordicsemi.com.

11.4.1 QFAB QFN48 schematic with internal LDO setup

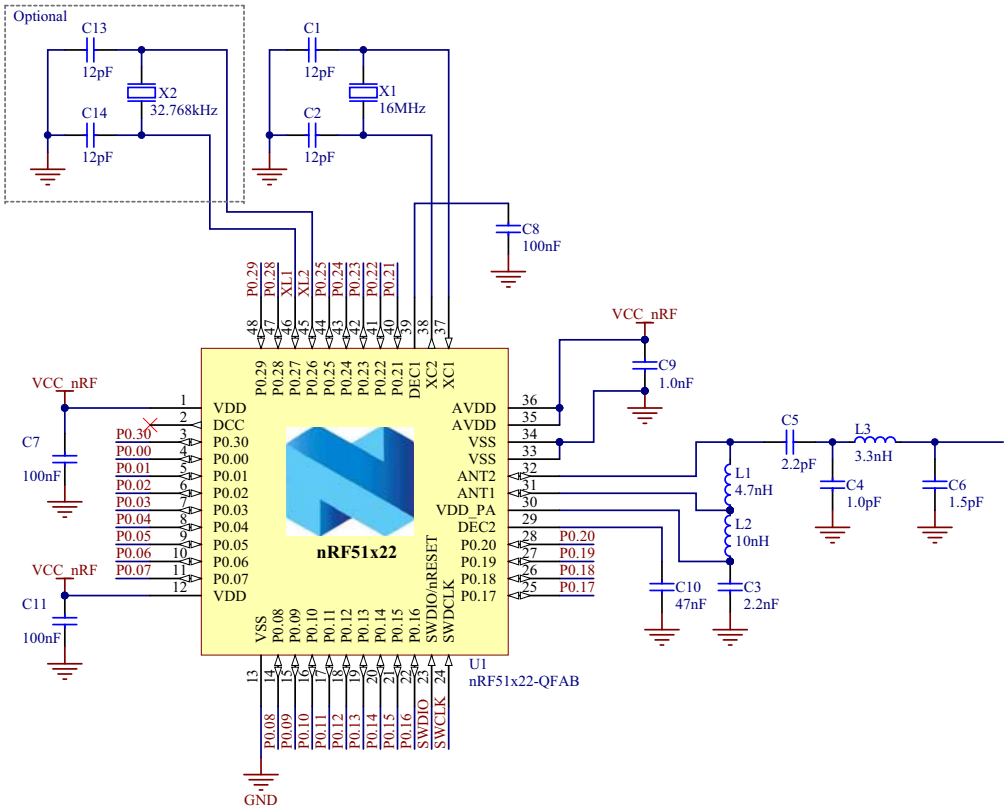

Figure 25 *QFAB QFN48 with internal LDO setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.4.1.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	10 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
U1	nRF51822-QFAB	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 87 *QFAB QFN48 with internal LDO setup*

11.4.2 QFAB QFN48 schematic with low voltage mode setup

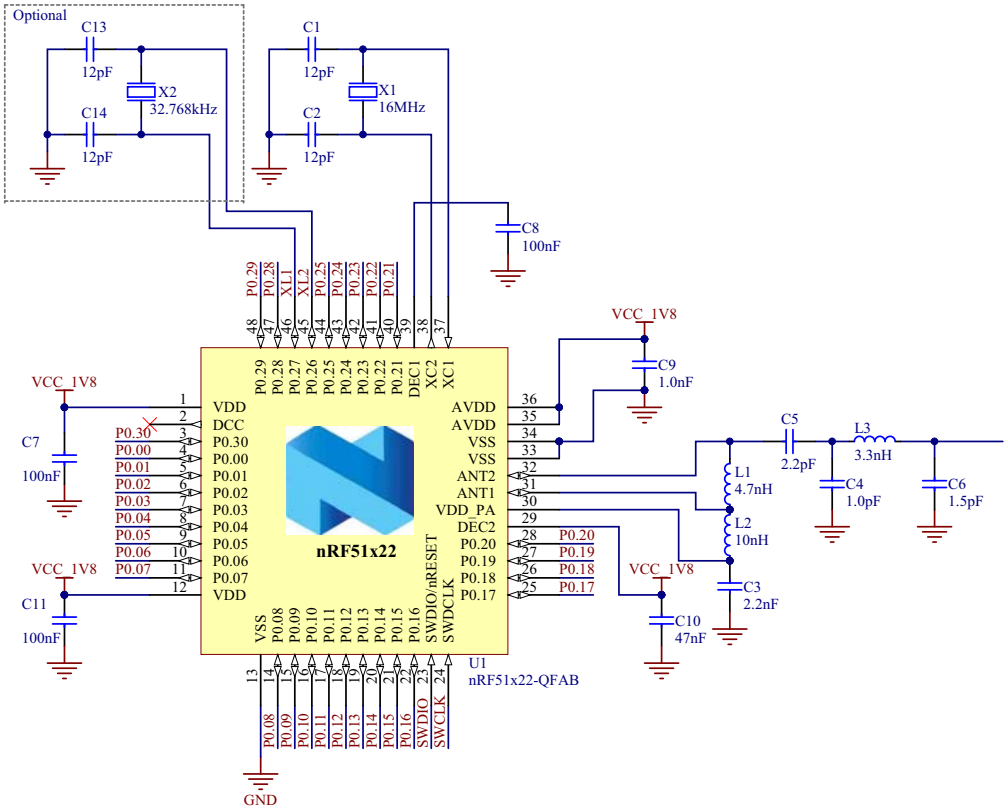

Figure 26 *QFAB QFN48 with low voltage mode setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.4.2.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	10 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
U1	nRF51822-QFAB	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 88 *QFAB QFN48 with low voltage mode setup*

11.4.3 QFAB QFN48 schematic with DC/DC converter setup

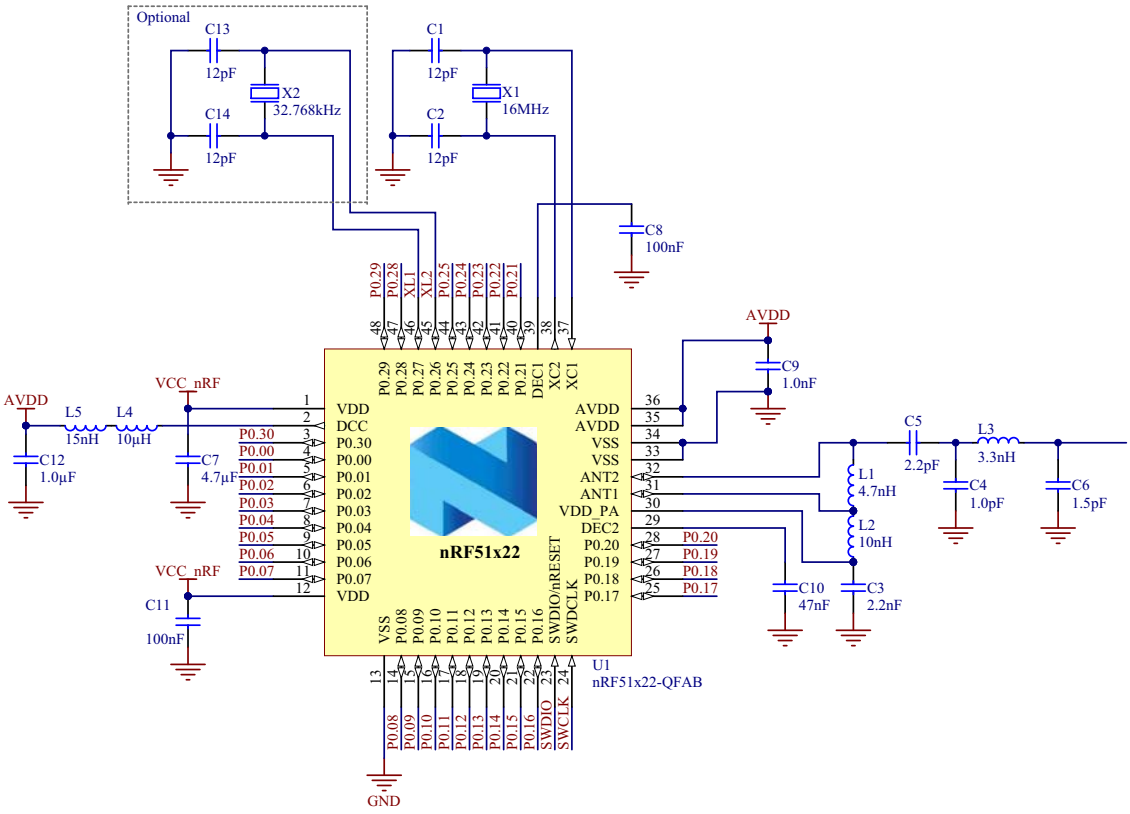

Figure 27 *QFAB QFN48 with DC/DC converter setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.4.3.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	2.2 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7	4.7 µF	Capacitor, X5R, ±10%	0603
C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
C12	1.0 µF	Capacitor, X7R, ±10%	0603
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	10 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
L4	10 µH	Chip inductor, $I_{DC,min}$ = 50 mA, ±20%	0603
L5	15 nH	High frequency chip inductor ±10%	0402
U1	nRF51822-QFAB	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 89 *QFAB QFN48 with DC/DC converter setup*

11.5 QFAC QFN48 package

Documentation for the QFAC QFN48 package reference circuit, including Altium Designer files, PCB layout files, and PCB production files can be downloaded from www.nordicsemi.com.

11.5.1 QFAC QFN48 schematic with internal LDO setup

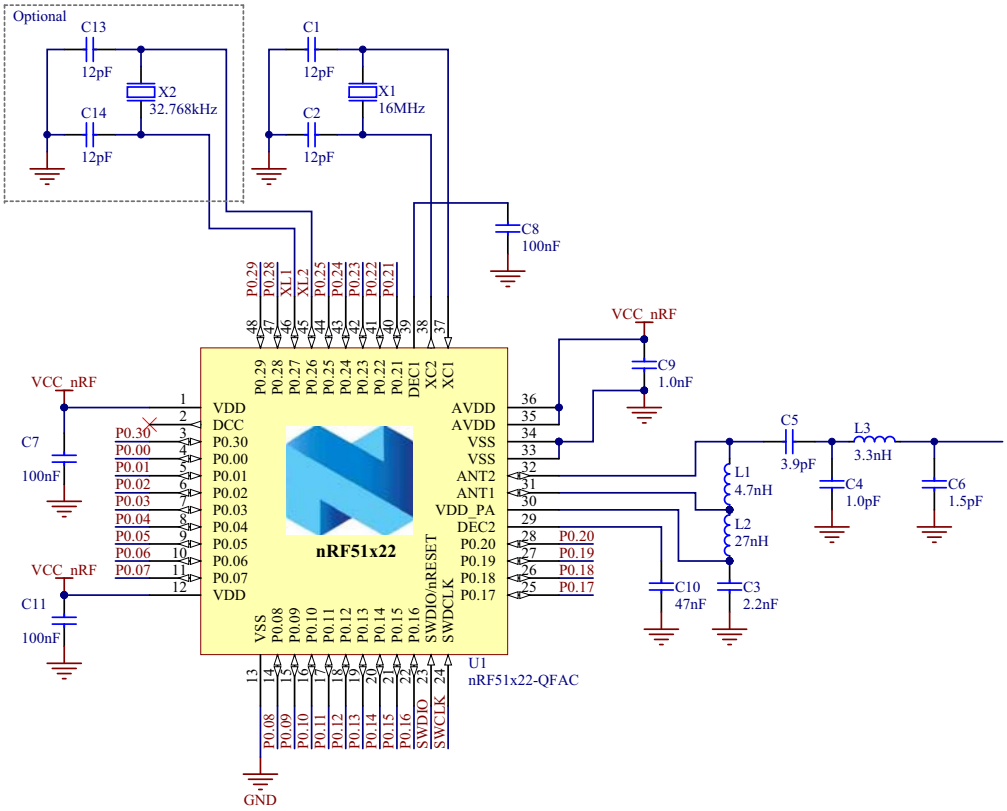

Figure 28 *QFAC QFN48 with internal LDO setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.5.1.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	3.9 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	27 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
U1	nRF51822-QFAC	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 90 *QFAC QFN48 with internal LDO setup*

11.5.2 QFAC QFN48 schematic with low voltage mode setup

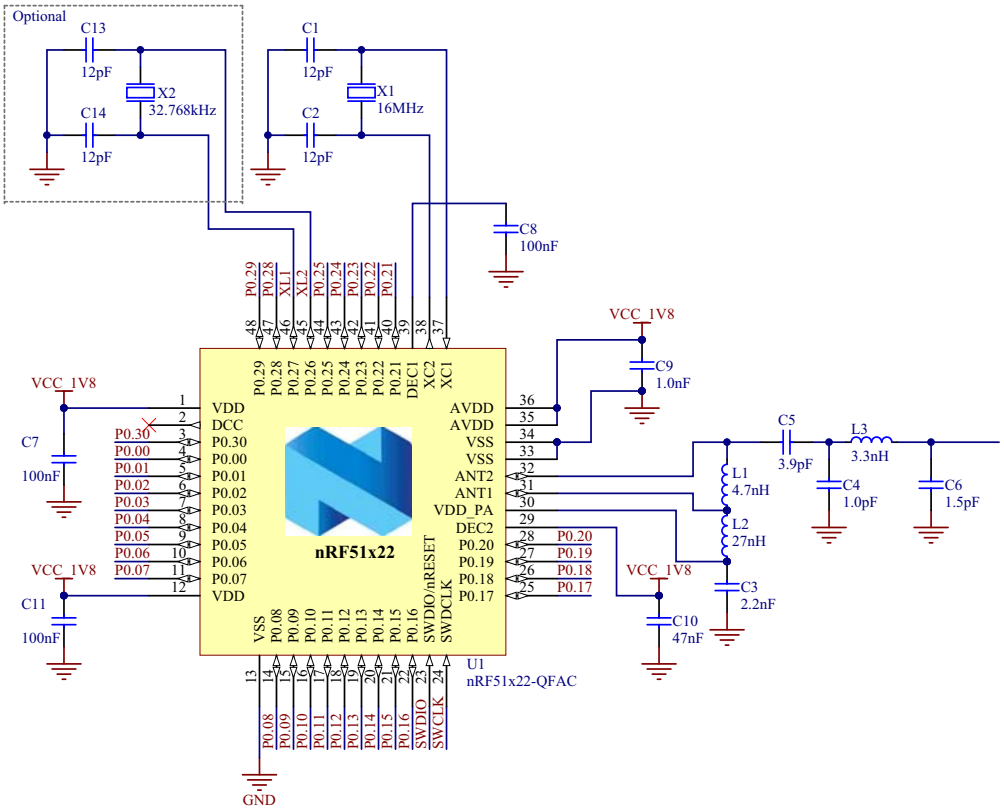

Figure 29 *QFAC QFN48 with low voltage mode setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.5.2.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	3.9 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	27 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
U1	nRF51822-QFAC	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 91 *QFAC QFN48 with low voltage mode setup*

11.5.3 QFAC QFN48 schematic with DC/DC converter setup

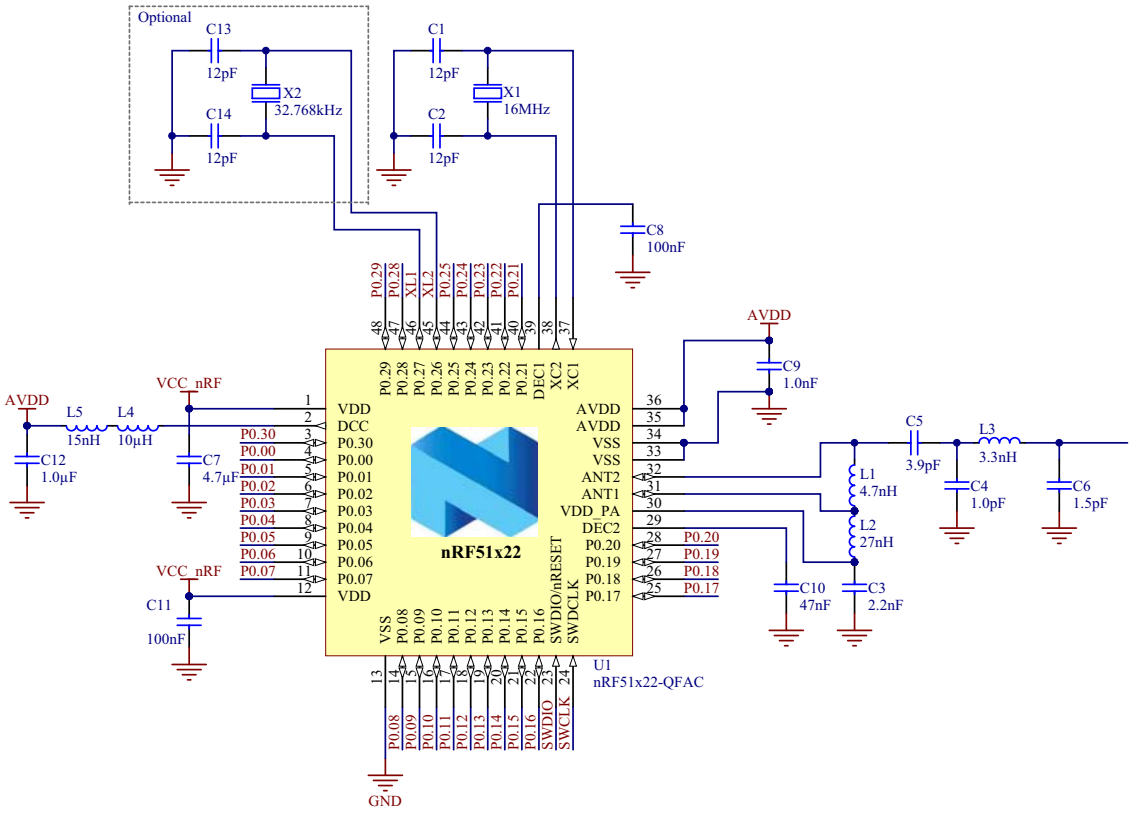

Figure 30 *QFAC QFN48 with DC/DC converter setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.5.3.1 Bill of Materials

Designator	Value	Description	Footprint
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C4	1.0 pF	Capacitor, NP0, ±0.1 pF	0402
C5	3.9 pF	Capacitor, NP0, ±0.1 pF	0402
C6	1.5 pF	Capacitor, NP0, ±0.1 pF	0402
C7	4.7 µF	Capacitor, X5R, ±10%	0603
C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
C12	1.0 µF	Capacitor, X7R, ±10%	0603
L1	4.7 nH	High frequency chip inductor ±5%	0402
L2	27 nH	High frequency chip inductor ±5%	0402
L3	3.3 nH	High frequency chip inductor ±5%	0402
L4	10 µH	Chip inductor, $I_{DC,min}$ = 50 mA, ±20%	0603
L5	15 nH	High frequency chip inductor ±10%	0402
U1	nRF51822-QFAC	RF SoC	QFN40P600X600X90-48N
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 92 *QFAC QFN48 with DC/DC converter setup*

11.6 CDAB WLCSP package

Documentation for the CDAB WLCSP package reference circuit, including Altium Designer files, PCB layout files, and PCB production files, can be downloaded from www.nordicsemi.com.

11.6.1 CDAB WLCSP schematic with internal LDO setup

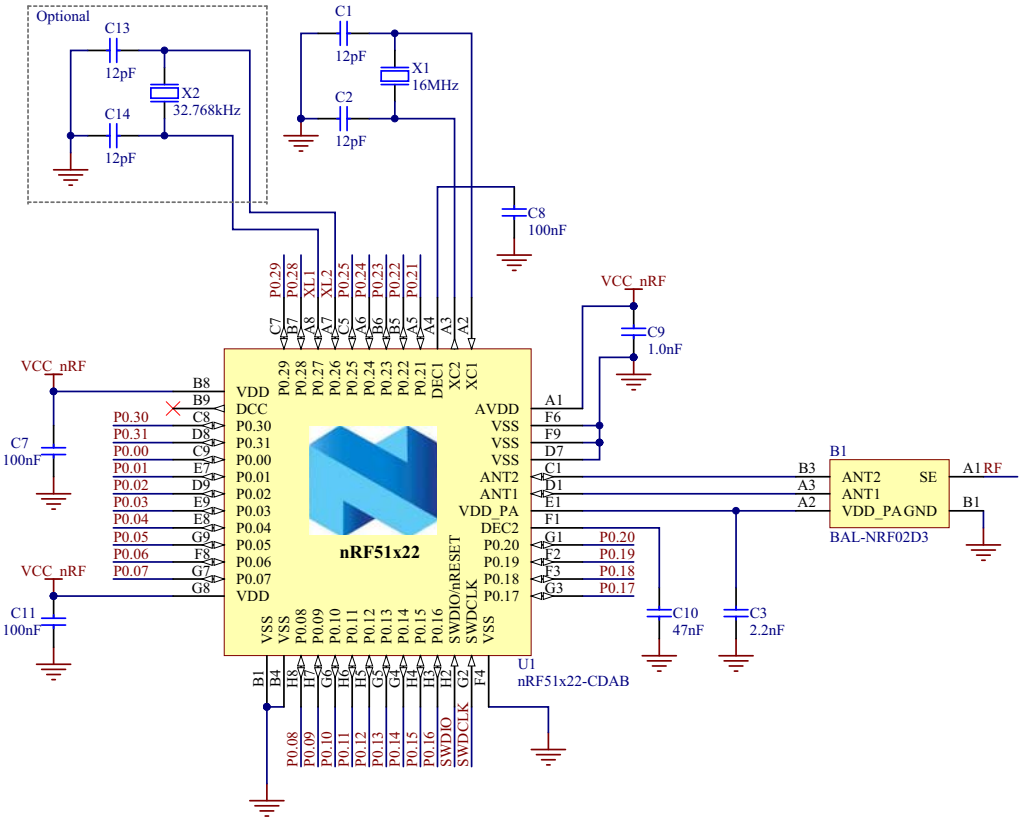

Figure 31 *CDAB WLCSP with internal LDO setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.6.1.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelecronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-ST-WLCSP
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
U1	nRF51822-CDAB	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 93 *CDAB WLCSP with internal LDO setup*

11.6.2 CDAB WLCSP schematic with low voltage mode setup

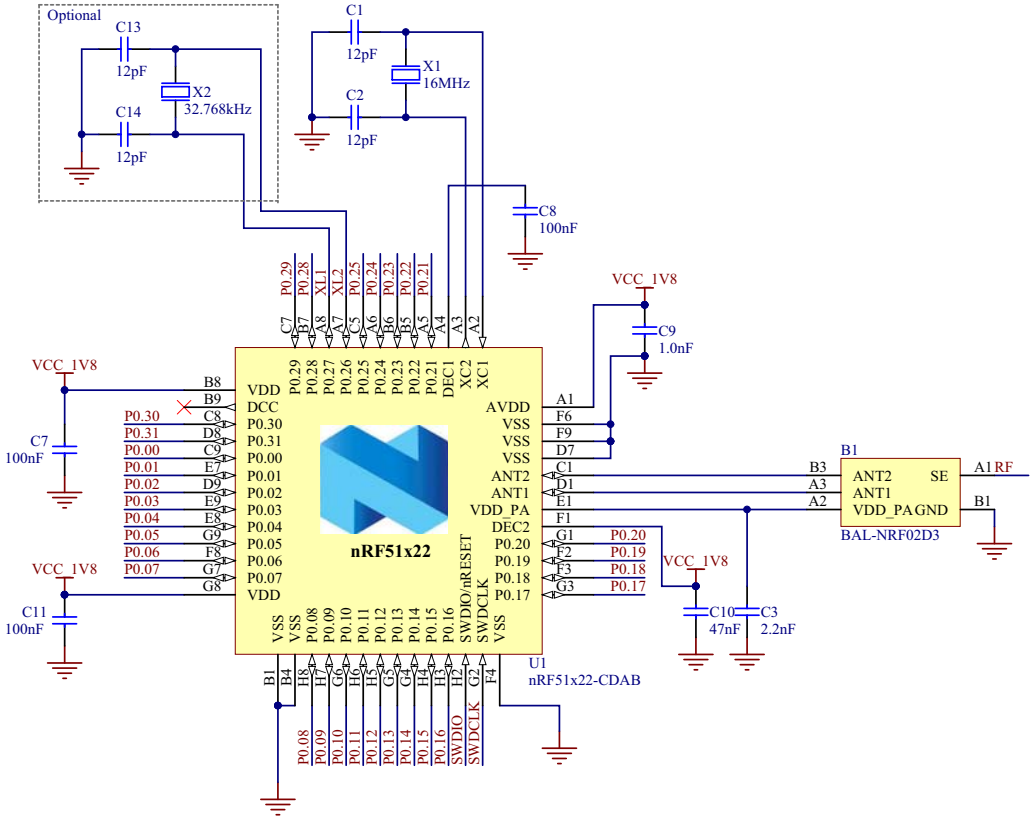

Figure 32 *CDAB WLCSP with low voltage mode setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.6.2.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-ST-WLCSP
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
U1	nRF51822-CDAB	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 94 *CDAB WLCSP with low voltage mode setup*

11.6.3 CDAB WLCSP schematic with DC/DC converter setup

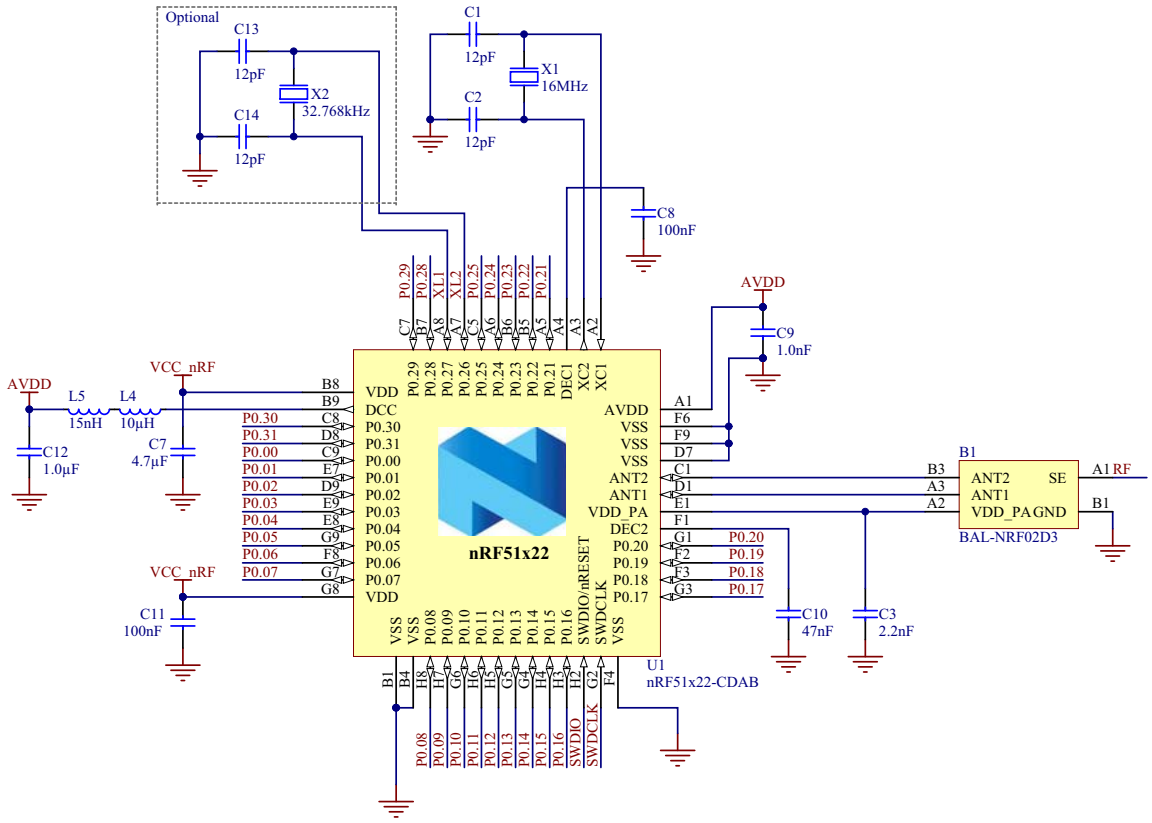

Figure 33 *CDAB WLCSP with DC/DC converter setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.6.3.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-ST-WLCSP
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C7	4.7 µF	Capacitor, X5R, ±10%	0603
C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
C12	1.0 µF	Capacitor, X7R, ±10%	0603
L4	10 µH	Chip inductor, $I_{DC,min}$ = 50 mA, ±20%	0603
L5	15 nH	High frequency chip inductor ±10%	0402
U1	nRF51822-CDAB	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 95 *CDAB WLCSP with DC/DC converter setup*

11.7 CEAA WLCSP package

Documentation for the CEAA WLCSP package reference circuit, including Altium Designer files, PCB layout files, and PCB production files, can be downloaded from www.nordicsemi.com.

11.7.1 CEAA WLCSP schematic with internal LDO setup

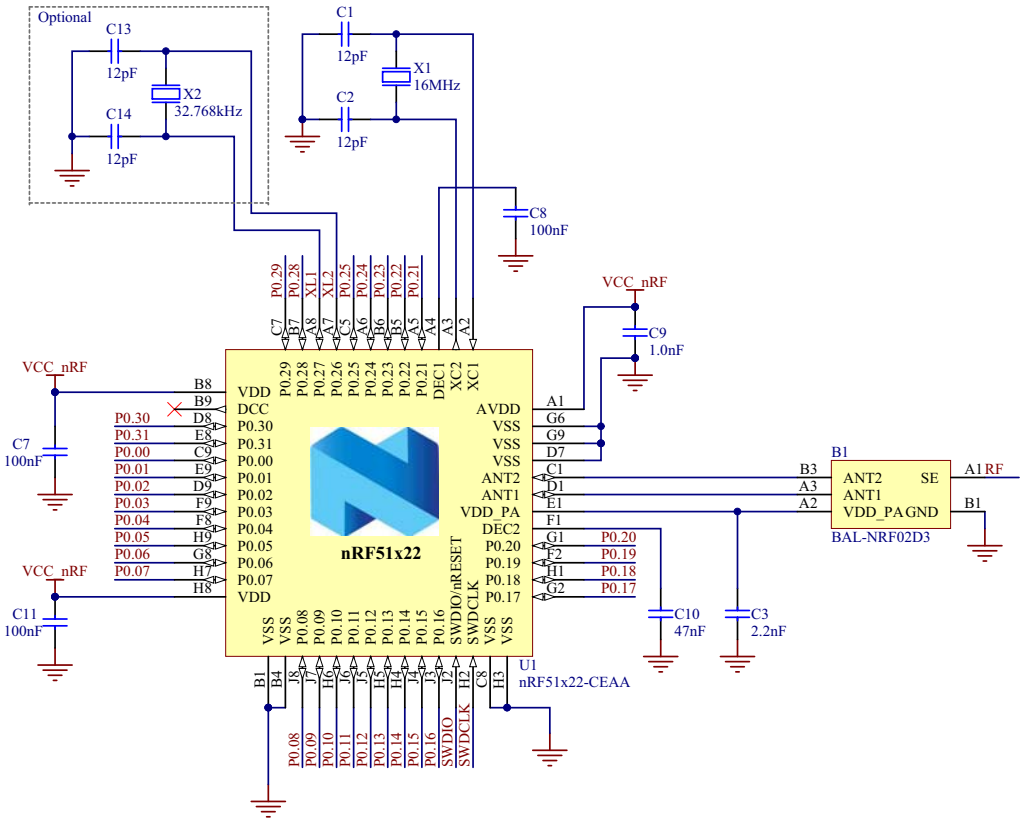

Figure 34 *CEAA WLCSP with internal LDO setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.7.1.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelecronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-ST-WLCSP
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
U1	nRF51822-CEAA	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 96 *CEAA WLCSP with internal LDO setup*

11.7.2 CEAA WLCSP schematic with low voltage mode setup

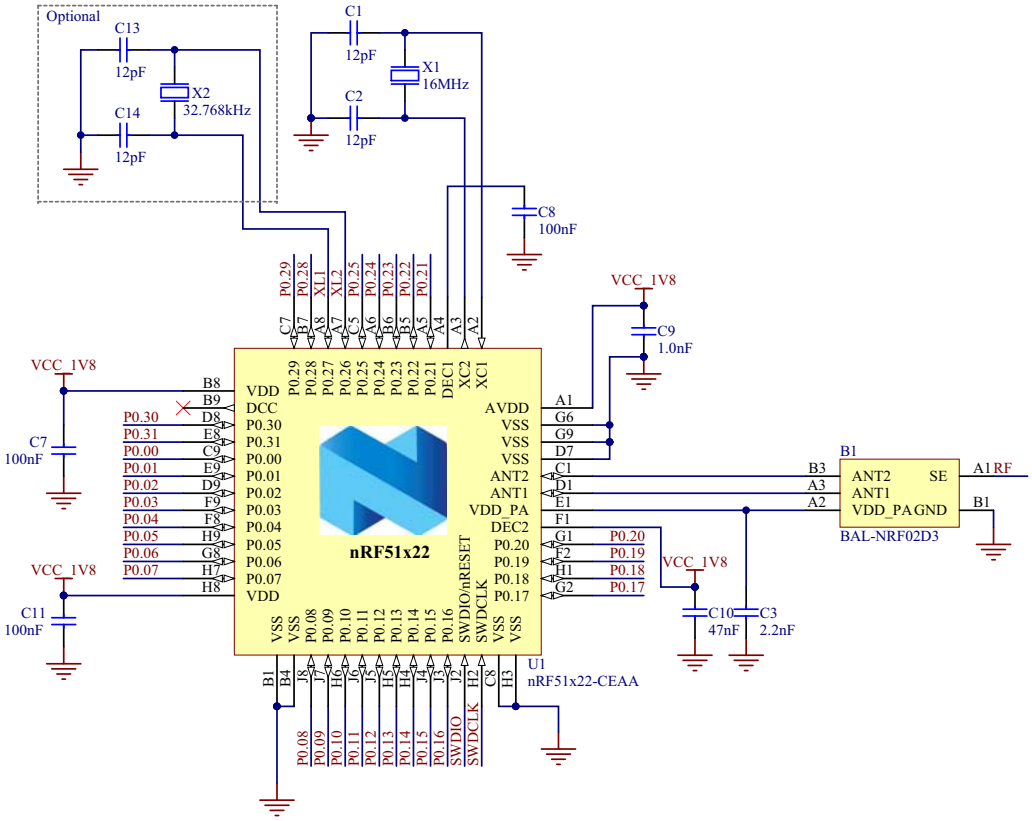

Figure 35 *CEAA WLCSP with low voltage mode setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.7.2.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-ST-WLCSP
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
U1	nRF51822-CEAA	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 97 *CEAA WLCSP with low voltage mode setup*

11.7.3 CEAA WLCSP schematic with DC/DC converter setup

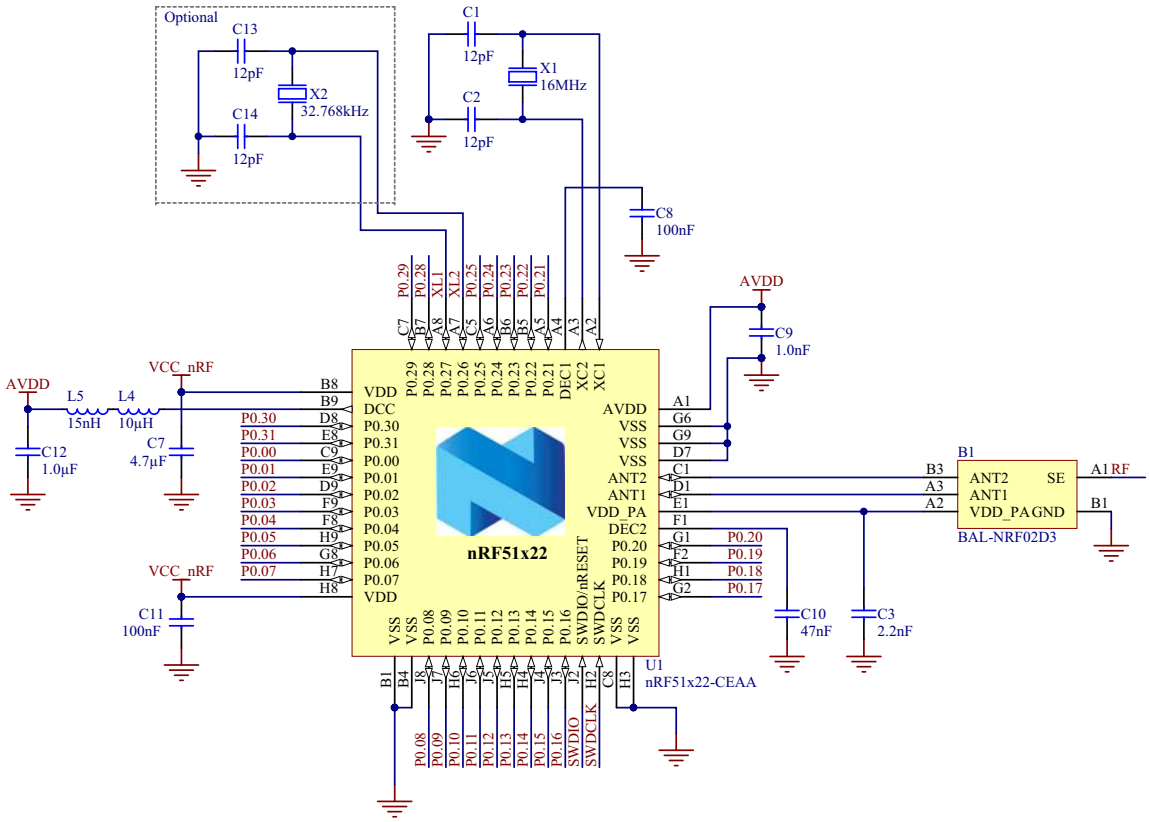

Figure 36 *CEAA WLCSP with DC/DC converter setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.7.3.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-ST-WLCSP
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C7	4.7 µF	Capacitor, X5R, ±10%	0603
C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
C12	1.0 µF	Capacitor, X7R, ±10%	0603
L4	10 µH	Chip inductor, $I_{DC,min}$ = 50 mA, ±20%	0603
L5	15 nH	High frequency chip inductor ±10%	0402
U1	nRF51822-CEAA	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 98 *CEAA WLCSP with DC/DC converter setup*

11.8 CFAC WLCSP package

Documentation for the CFAC WLCSP package reference circuit, including Altium Designer files, PCB layout files, and PCB production files, can be downloaded from www.nordicsemi.com.

11.8.1 CFAC WLCSP schematic with internal LDO setup

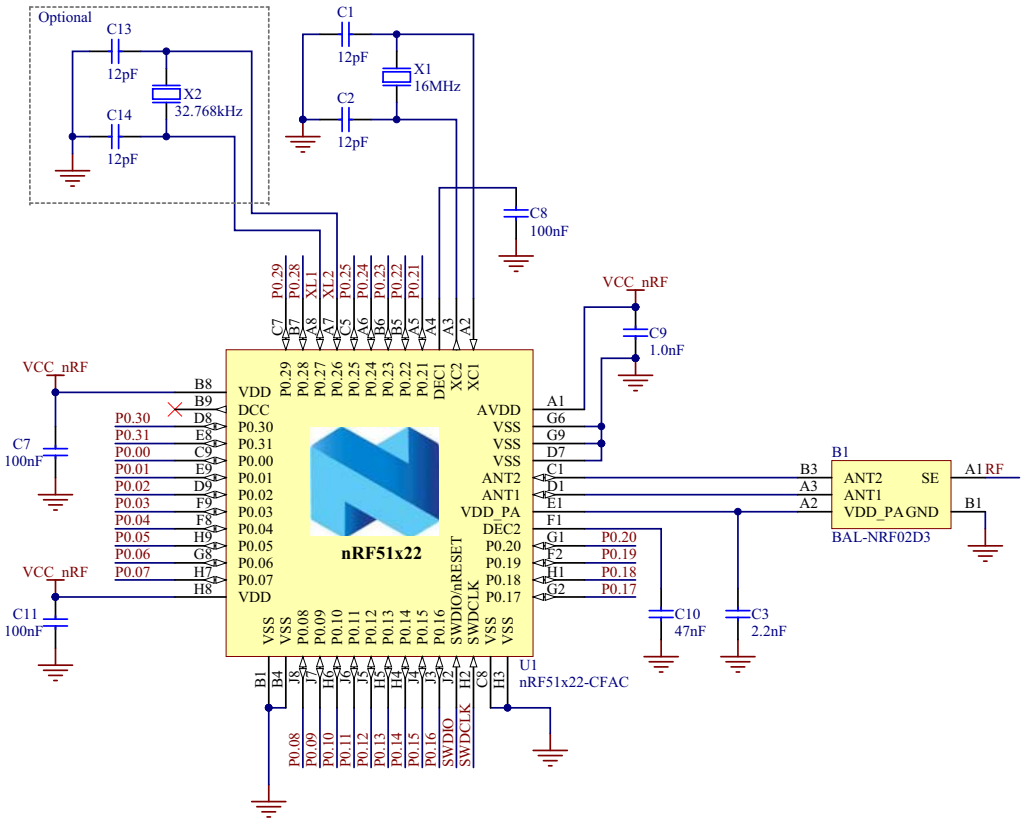

Figure 37 *CFAC WLCSP with internal LDO setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.8.1.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelecronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-ST-WLCSP
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
U1	nRF51822-CFAC	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 99 *CFAC WLCSP with internal LDO setup*

11.8.2 CFAC WLCSP schematic with low voltage mode setup

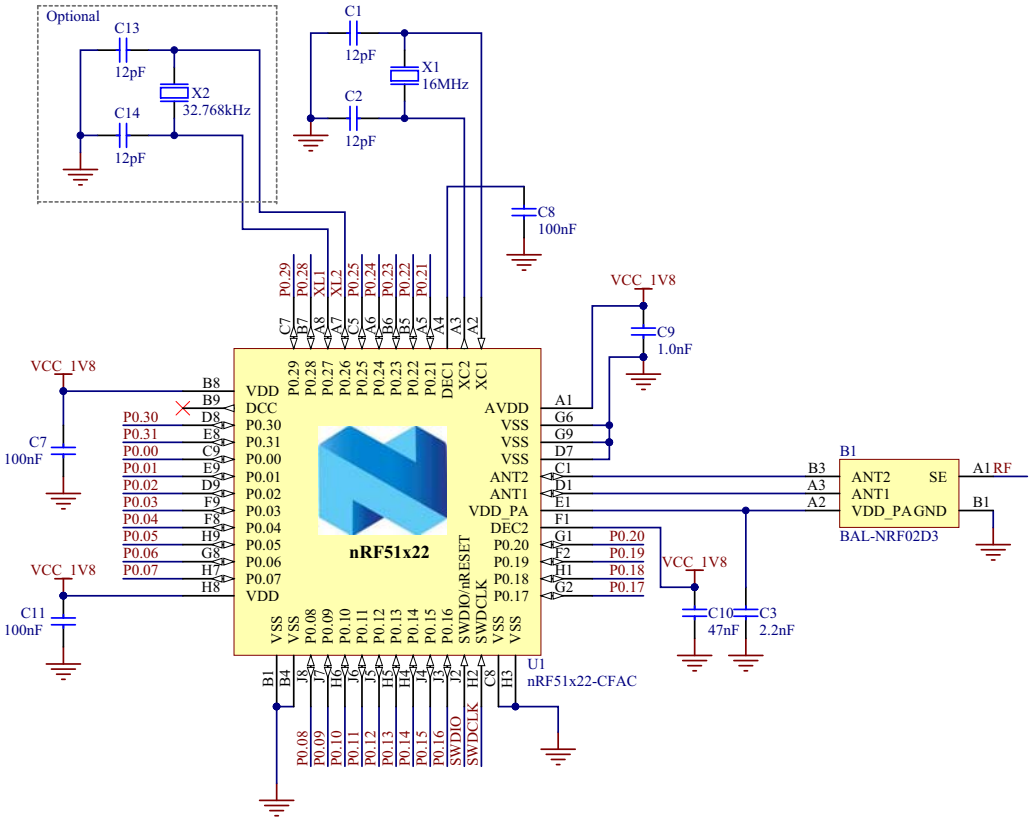

Figure 38 *CFAC WLCSP with low voltage mode setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.8.2.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-ST-WLCSP
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C7, C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
U1	nRF51822-CEAA	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 100 *CFAC WLCSP with low voltage mode setup*

11.8.3 CFAC WLCSP schematic with DC/DC converter setup

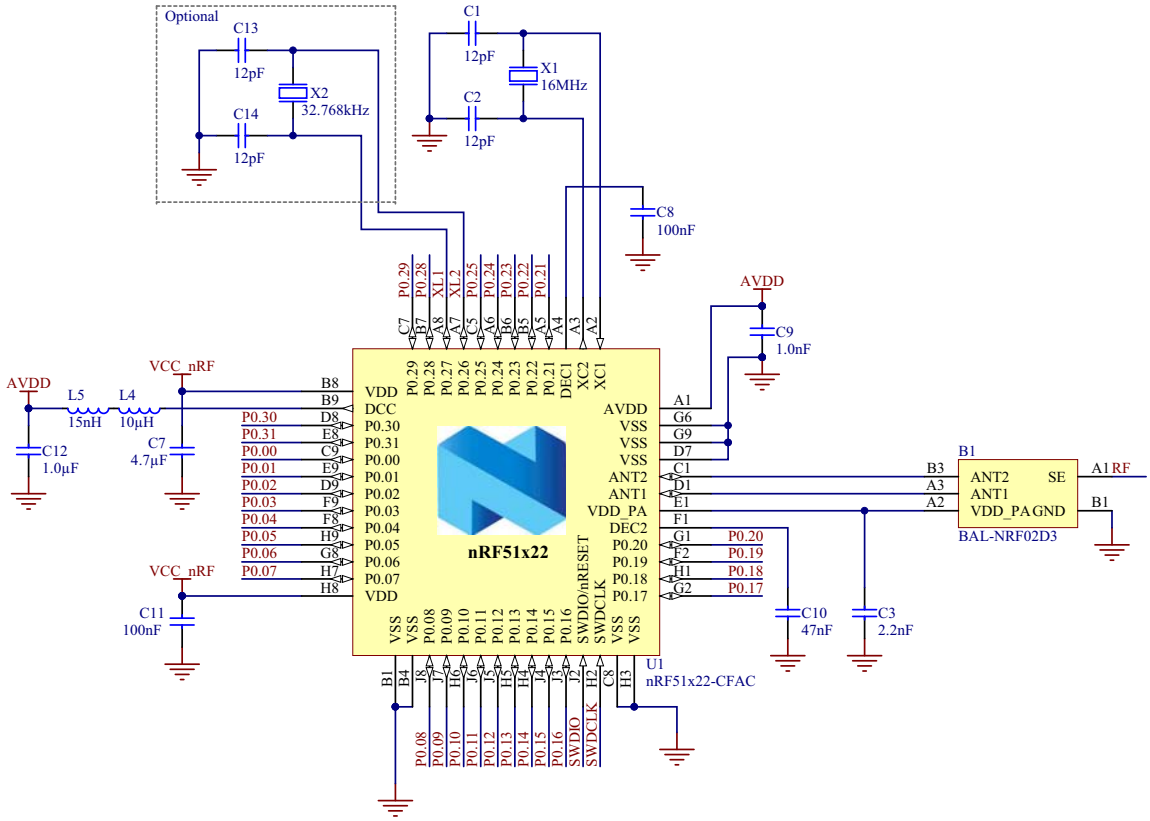

Figure 39 *CFAC WLCSP with DC/DC converter setup*

Note: For PCB reference layouts, see the Reference Layout section on the Downloads tab for the different chip variants on www.nordicsemi.com.

11.8.3.1 Bill of Materials

Designator	Value	Description	Footprint
B1	BAL-NRF02D3	ST Microelectronics, 50 Ω balun transformer for 2.45 GHz ISM	BAL-ST-WLCSP
C1, C2, C13, C14	12 pF	Capacitor, NP0, ±2%	0402
C3	2.2 nF	Capacitor, X7R, ±10%	0402
C7	4.7 µF	Capacitor, X5R, ±10%	0603
C8, C11	100 nF	Capacitor, X7R, ±10%	0402
C9	1.0 nF	Capacitor, X7R, ±10%	0402
C10	47 nF	Capacitor, X7R, ±10%	0402
C12	1.0 µF	Capacitor, X7R, ±10%	0603
L4	10 µH	Chip inductor, $I_{DC,min}$ = 50 mA, ±20%	0603
L5	15 nH	High frequency chip inductor ±10%	0402
U1	nRF51822-CFAC	RF SoC	BGA62C40P9X9_383X350X55
X1	16 MHz	Crystal SMD 2520, 16 MHz, 8 pF, ±40 ppm	2.5 x 2.0 mm
X2	32.768 kHz	Crystal SMD FC-135, 32.768 kHz, 9 pF, ±20 ppm	FC-135

Table 101 *CFAC WLCSP with DC/DC converter setup*

12 Glossary

Term	Description
EOC	Extreme Operating Conditions
GFSK	Gaussian Frequency-Shift Keying
GPIO	General Purpose Input Output
ISM	Industrial Scientific Medical
MOQ	Minimum Order Quantity
NOC	Nominal Operating Conditions
NVMC	Non-Volatile Memory Controller
QDEC	Quadrature Decoder
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RSSI	Radio Signal Strength Indicator
SPI	Serial Peripheral Interface
TWI	Two-Wire Interface
UART	Universal Asynchronous Receiver Transmitter
WLCSP	Wafer Level Chip Scale Packet

Table 102 *Glossary*