ATS2825_MODULE_V1.2

Sheets List

Revision History

V1.0 Original Version 2015-04-16

V1.1 2015-09-09
Add the crystal external matching capacitor CZ25, CZ26.

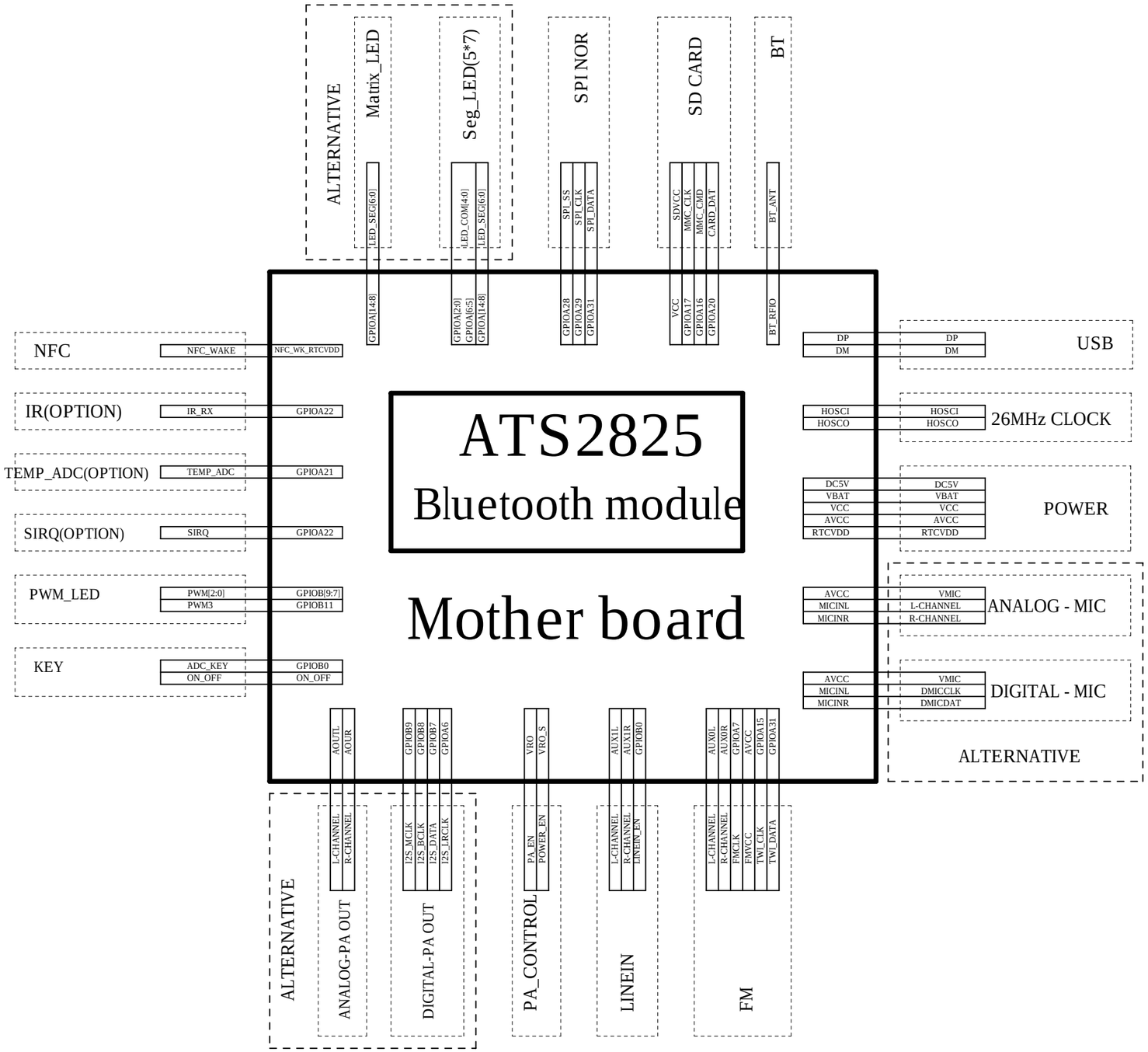
V1.2 2016-02-24
Modify the PCB layer to the 4 layer
Modify the components parameters:
CZ21 is 0.1pF;
CZ20 and LZ2 are 0R;
CZ22 isTVS(LESD8L3.3CT5G)

Design Guide

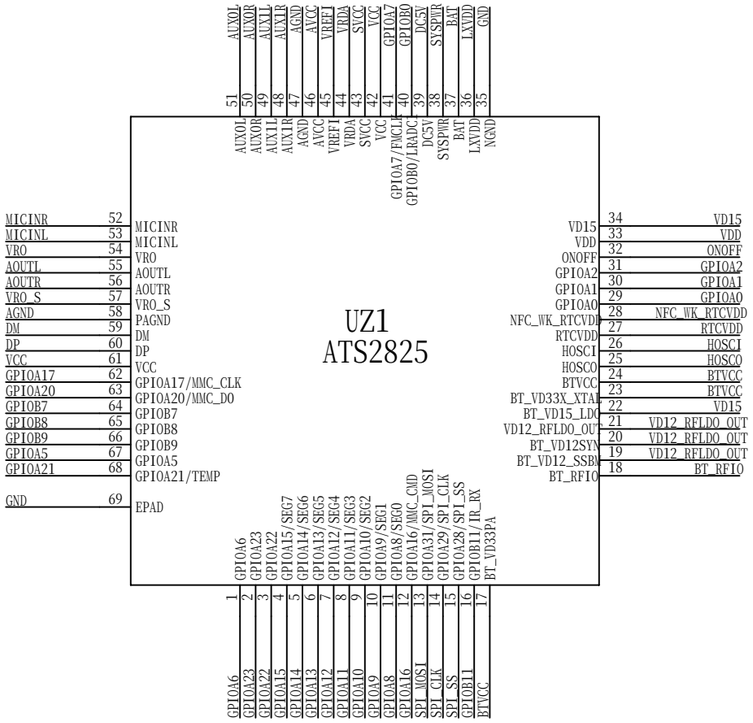
Diagram of the GPIO's state

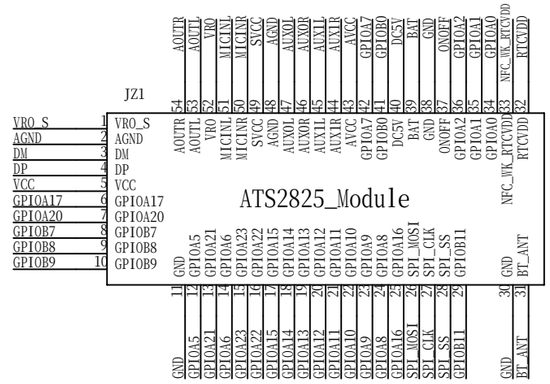
GPIOX(NAME)	Driving Capability(mA)	Initial State	Application Module	Remark

Block Diagram



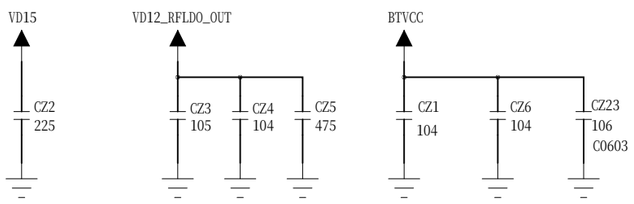
File name: ATS2825_MODULE_V1.2_20160224.sch	
Sheet name: BLOCK	
Drawing No:	Version: V1.2
Drawn By:	Date: 2016-02-24
Checked By:	Date:
Approved By:	Date:
Size: A3	Sheet: 2 of 3



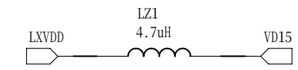


4Layer：L x W x H = 24.9 x 14 x 0.8 (mm)

GPIO_A16=LOW Level,enter BT ONLY TEST MODE

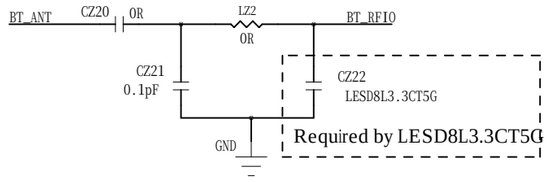


CZ1 close to PIN23

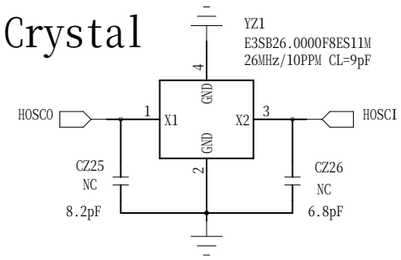


LZ1's Decal large than 0806

VLS201612CX-4R7M,DRC < 0.3 OHM



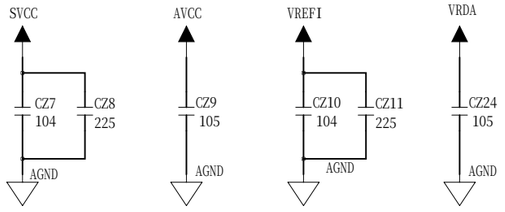
Crystal

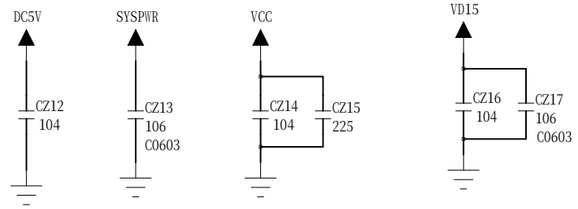


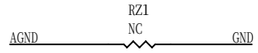
Option:

CZ25,CZ26, the capacitance value needs to be adjusted according to crystal parameters.

Capacitor material / accuracy: NPO/1%.







Option：0R 5%

File name: ATS2825_MODULE_V1.2_20160224.sch	
Sheet name: CORE	
Drawing No:	Version: V1.2
Drawn By:	Date: 2016-02-24
Checked By:	Date:
Approved By:	Date:
Size: A3	Sheet: 3 of 3