ATS2825 Datasheet

Version: 1.0

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Contents

Revision History

Date	Revision	Description
2015-03-23	1.0	First Release

1 Introduction

Features

- 104MHz MIPS32 Processor and 180MHz Gogir DSP
- Internal ROM and serial flash memory interface supporting randomizer
- Internal RAM for data and program
- Built-in high performance stereo 24 bit input DAC & ADC
- Supports Digital microphones, single-ended Analog microphones and fully differential microphone
- Built-in stereo PA for headphone and differential audio output for speaker PA
- Bluetooth V4.1 compatible with Bluetooth V4.1 (BLE), V3.0, V2.1 systems
- Bluetooth fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve Bluetooth transmission quality
- Support SD/MMC/eMMC card interface and SPI NorFlash interface
- Audio Interfaces: I2S, SPDIF TX
- Serial Interfaces: USB2.0, UART, TWI, SPI
- Infrared Remote controller supported
- TFT and Segment LCD panels
- Digital matrix LED panels
- Integrated PMU supports multiple low energy states
- Integrated Linear battery charger up to 600mA charging current
- Package QFN-68 (8mm*8mm, Pitch 0.4mm)

Applications

- Portable stereo speakers and speakerphones
- Bluetooth car audio unit
- Stereo headsets and headphones
- Other Bluetooth audio applications

Actions® ATS2825™ QFN68

Bluetooth Audio Solution

Low Power Solution for
Portable & Wireless Audio Applications
Local MMC/SD Card Audio Playback

MIPS + DSP Dual-core Single-chip Bluetooth V4.1

Revision V1.0

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1.1 Overview

Actions' ATS2825 is a highly integrated single-chip Bluetooth Audio solution. Positioning at Bluetooth portable stereo speakers, headsets and speakerphones and local MMC/SD Card Audio Playback market, ATS2825 satisfies the market requirements with high performance, low cost and low power consumption.

ATS2825 adopts MIPS + DSP dual core architecture. Large capacity RAM is embedded to meet different Bluetooth applications, and support Bluetooth background working while playing high quality music with traditional plug-in card and USB flash disk. ATS2825 supports all Bluetooth formats audio decode and loading sound effects simultaneously, support Bluetooth handfree calls with dual MIC AEC and noise reduction.

ATS2825 integrates Bluetooth controller fully compliant with 4.1/4.0/3.1/2.1 Bluetooth specification, and supports dual mode (BR/EDR + Low Energy Controllers). The links in BR/EDR and LE can be active simultaneously.

ATS2825 takes special methods at power optimization, especially for various applications scenarios, including sniff, Bluetooth idle, Bluetooth playing and call modes. Embedded PMU supports power optimization and provide long battery life. The competitive advantages of ATS2825 are high music and call qualities with low power and BOM, which lays the foundation for our goal at high-end market. Above all, ATS2825 provides a true "ALL-IN-ONE" solution, making it the ideal choice for highly integrated and optimized Bluetooth audio products.

1.2 Application Diagram

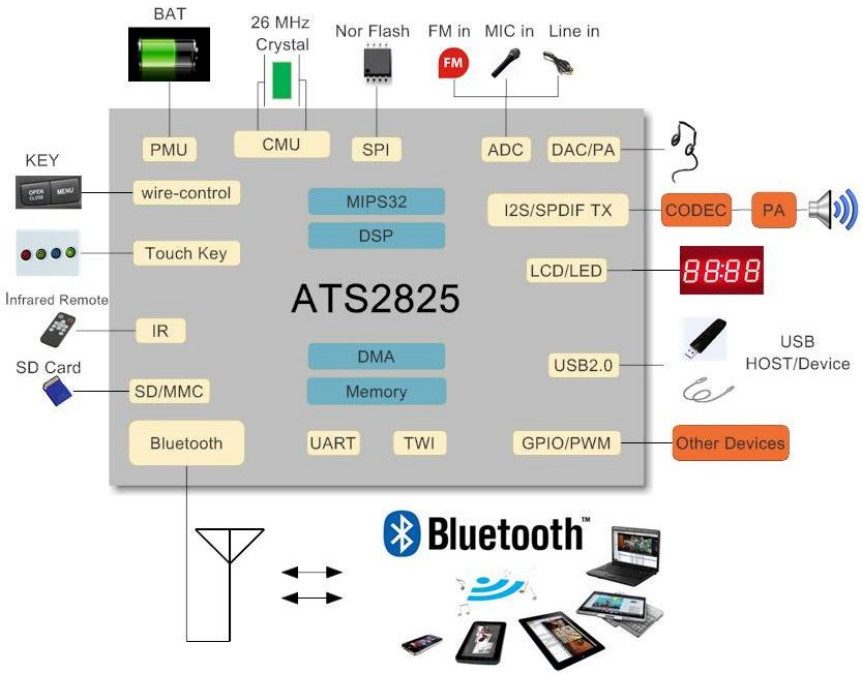


Figure 1-1 ATS2825 Application Diagram

1.3 Detail Features

System

- 104MHz MIPS32 processor Core
- 180MHz Gogir DSP core
- Internal RAM for data and program storage
- Support 26MHz OSC with on-chip PLL
- Operating voltage: I/O 3.1V, Core 1.2V
- Fully configurable PEQ, up to 14 segments
- Actions' super voice technology for voice connections
- Support for echo cancellation and noise reduction
- Support for wind noise reduction
- Support for packet loss concealment
- Support for multiple sound effect, such as TEQ, MDRC, bass enhancement, virtual surround effects
- Support for voice prompt

Bluetooth

- Support Bluetooth V4.1 and V4.1 BLE
- Compatible with Bluetooth V2.1 and V3.0
- Compatible with AVRCP Profile V1.6
- Compatible with A2DP Profile V1.3
- Compatible with HFP Profile V1.7
- Compatible with HSP Profile V1.2
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/Esco link
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff / Sniff Sub-rating / Hold / Park)
- Bluetooth 4.1 Dual Mode support: Simultaneous LE and BR / EDR
- Supports multiple Low Energy states
- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Integrated Class1, Class2, and Class 3 PA
- Bluetooth 3.0 compliant
- Supports Power / Enhanced Power Control
- Integrated 32K oscillator for power management

Package

- QFN-68 (8mm*8mm, Pitch 0.4mm)

Audio

- Built-in stereo 24 bit input sigma-delta DAC, SNR > 98dB, THD <- 87dB
- DAC supports sample rate 8k/12k/11.025k/ 16k/22.05k/24k/32k/44.1/48kHz
- Built-in stereo 20mW PA for headphone. PA output supports traditional mode and direct drive mode (for earphone)
- Support differential audio output for speaker PA
- Built-in stereo 24 bit input sigma-delta ADCs, SNR>90dB, THD<-82dB.
- ADC supports sample rate 8k/12k/11.025k/ 16k/22.05k/24k/32k/44.1k/48kHz
- Supports stereo single-ended input analog or mono fully differential input microphone
- Supports Digital microphones and Analog microphones

Power Management

- Supports Li-Ion battery and 5V power supply
- Dynamic power management
- Integrated Linear battery charger
- Integrated DC-DC buck converters, switchable to LDO mode
- Linear regulators output VCC, AVCC, BTVCC
- Standby Leakage Current <50uA (Whole System)
- Low Power Consumption (No LCD/ SPEAKER/ LAMP): Typical Sniff Current: 800uA @ Vbat = 3.8V; ACL: < 18mA @ Vbat = 3.8V; SCO: < 20mA@Vbat=3.8V

Physical Interfaces

- Support SD/MMC/eMMC card interface and SPI NorFlash interface
- USB 2.0 device and host controllers
- A variety of serial controllers supporting I2S, SPDIF TX, SPI, UART, TWI
- Support Remote Control with the internal IRC for decoding
- Support independent capacitive touch keys
- Support LCM with 8bit CPU Interface, 4COM/5COM/6COM Segment LCD, 7pin LED
- 4 LED drivers with PWM flasher independent of MCU

1.4 Pin Assignment and Descriptions

1.4.1 Pin Assignment

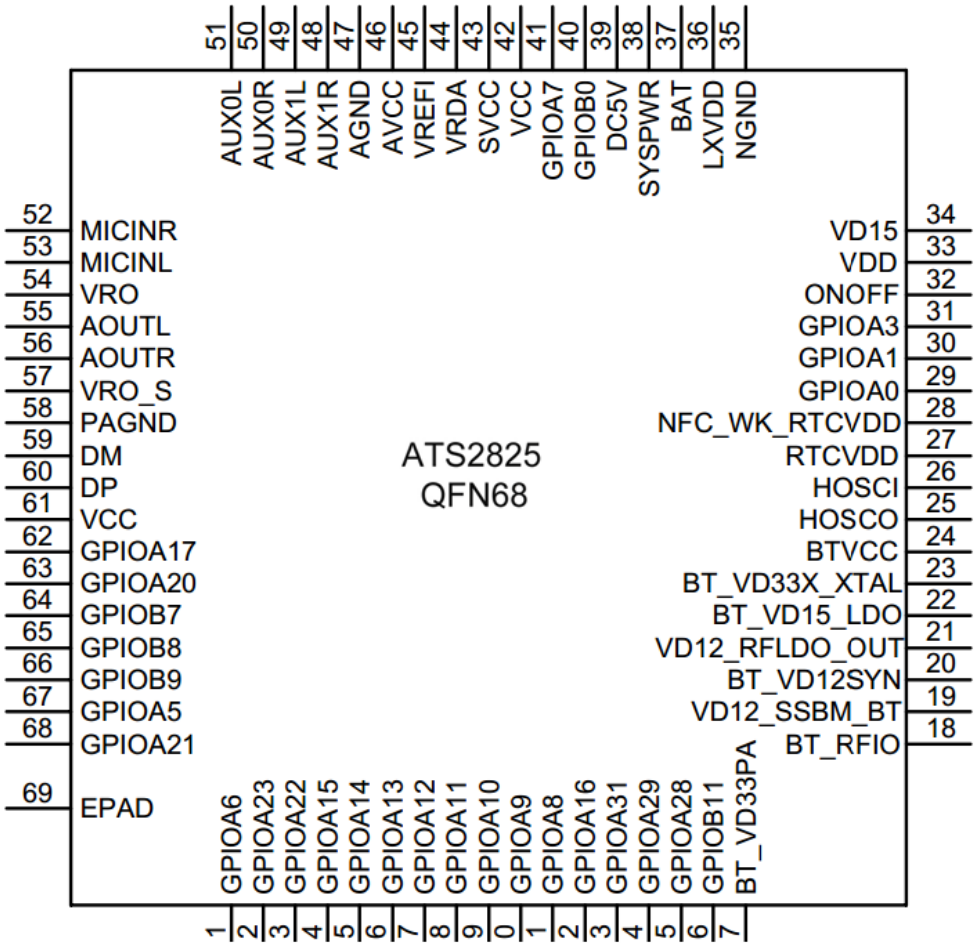


Figure 1-2 ATS2825 (QFN68) Pin Assignment

1.4.2 Pin Description

Table 1-1 ATS2825 Pin Description

Pin No.	Pin Name	Default Function	Function Multiplex	IO Type	PAD Drive Level	GPIO Initial State	Description
1	GPIOA6	LED_COM6	GPIOA6/LED_COM6/EM_CEB3/LCD_SEG0/I2S_LRCLK/TK6	DIO	LED_COM:24 mA;2/4/6/8/18/20/22/24 mA	Z	Bit6 of General purpose I/O portA
2	GPIOA23	SD_DAT3	GPIOA23/SD_DAT3/EM_D11/LCD_D11/LCD_SEG13/SPDIFTX/PWM2/SPDIFTX/UART_TX1/SD_DAT0/LRADC3/TK7/MEJ_TDO	DIO	2/4/6/8/10/12/14/16mA	Z	Bit23 of General purpose I/O portA
3	GPIOA22	SD_DAT2	GPIOA22/SD_DAT2/EM_D10/LCD_D10/LCD_SEG12/SIRQ0/IR_RX/PWM1/LRADC2/SHIELD	DIO	2/4/6/8/10/12/14/16mA	Z	Bit22 of General purpose I/O portA
4	GPIOA15	LED_SEG7	GPIOA15/LED_SEG7/EM_D7/LCD_D7/LCD_SEG9/TK7	DIO	2/4/6/8/10/12/14/16mA	Z	Bit15 of General purpose I/O portA
5	GPIOA14	LED_SEG6	GPIOA14/LED_SEG6/EM_D6/LCD_D6/LCD_SEG8/TK6	DIO	2/4/6/8/10/12/14/16mA	Z	Bit14 of General purpose I/O portA
6	GPIOA13	LED_SEG5	GPIOA13/LED_SEG5/EM_D5/LCD_D5/LCD_SEG7/TK5	DIO	2/4/6/8/10/12/14/16mA	Z	Bit13 of General purpose I/O portA
7	GPIOA12	LED_SEG4	GPIOA12/LED_SEG4/EM_D4/LCD_D4/LCD_SEG6/TK4/DEJ_TDO/MEJ_TDO	DIO	2/4/6/8/10/12/14/16mA	Z	Bit12 of General purpose I/O portA
8	GPIOA11	LED_SEG3	GPIOA11/LED_SEG3/EM_D3/LCD_D3/LCD_SEG5/UART_RTS1/SPI1_MOSI/TK3/DEJ_TDI/MEJ_TDI	DIO	2/4/6/8/10/12/14/16mA	Z	Bit11 of General purpose I/O portA
9	GPIOA10	LED_SEG2	GPIOA10/LED_SEG2/EM_D2/LCD_D2/LCD_SEG4/UART_CTS1/SPI1_MISO/TK2/DEJ_TCK/MEJ_TCK	DIO	2/4/6/8/10/12/14/16mA	Z	Bit10 of General purpose I/O portA
10	GPIOA9	LED_SEG1	GPIOA9/LED_SEG1/EM_D1/LCD_D1/LCD_SEG3/SPI1_SCLK/TK1/DEJ_TMS/MEJ_TMS	DIO	2/4/6/8/10/12/14/16mA	Z	Bit9 of General purpose I/O portA
11	GPIOA8	LED_SEG0	GPIOA8/LED_SEG0/EM_D0/LCD_D0/LCD_SEG2/SPI1_SS/PWM3/TK0/DEJ_RTCK/MEJ_TRST	DIO	2/4/6/8/10/12/14/16mA	Z	Bit8 of General purpose I/O portA
12	GPIOA16	SD_CMD	GPIOA16/SD_CMD/UART	DIO	2/4/6/8/10/1	Z	Bit22 of

			_RX1/LCD_SEG14/SPI1_SS/MEJ_TMS		2/14/16mA		General purpose I/O portA
13	GPIOA31	SPI_MOSI	GPIOA31/SPI_MOSI/SPI_MISO/LCD_SEG20	DIO	2/4/6/8/10/12/14/16mA	Z	Bit31 of General purpose I/O portA
14	GPIOA29	SPI_SCLK	GPIOA29/SPI_SCLK/SPI_SS/SD_CLK1/TWI_SDA/SIRQ1LCD_SEG19	DIO	2/4/6/8/10/12/14/16mA	Z	Bit29 of General purpose I/O portA
15	GPIOA28	SPI_SS	GPIOA28/SPI_SS/SPI_MOSI/LCD_SEG18	DIO	2/4/6/8/10/12/14/16mA	Z	Bit28 of General purpose I/O portA
16	GPIOB11	SPIBT_IO2	GPIO_B11/SPIBT_IO2/TWI_SCL/PWM3/SIRQ0/IR_RX/SD_CLK0	DIO	2/4/6/8/10/12/14/16mA	Z	Bit11 of General purpose I/O portB
17	BT_VD33PA						3.3V Voltage
18	BT_RFIO						Bluetooth antenna IO
19	VD12_SSBM_BT						1.2V Voltage
20	BT_VD12SYN						1.2V Voltage
21	VD12_RFLDO_OUT						1.2V Voltage
22	BT_VD15_LDO						1.5V Voltage
23	BT_VD33X_XTAL			PWR			3.3V Voltage
24	BTVCC			PWR			
25	HOSCO			AO			32kHz clock output
26	HOSCI			AI			32kHz clock input
27	RTCVDD			PWR			RTC power
28	NFC_WK_RTCVDD			DI			NFC wakeup
29	GPIOA0	LED_COM0	GPIOA0/LED_COM0/EM_WRB/LCD_WRB/LCD_COM0/TWI_SCL/PWM1/UART_RTS1/I2S_MCLK	DIO	LED_COM:24mA;2/4/6/8/18/20/22/24mA	Z	Bit0 of General purpose I/O portA
30	GPIOA1	LED_COM1	GPIOA1/LED_COM1/EM_RS/LCD_RS/LCD_COM1/TWI_SDA/SIRQ1/PWM3/UART_CTS1/I2S_BCLK/MEJ_TMS/DEJ_TMS	DIO	LED_COM:24mA;2/4/6/8/18/20/22/24mA	Z	Bit1 of General purpose I/O portA

31	GPIOA2	LED_COM2	GPIOA2/LED_COM2/EM_RDB/LCD_RDB/LCD_COM2/PWM2/UART_RX1/I2S_LRCLK/LRADC4/BT_ACT/MEJ_TCK/DEJ_TCK	DIO	LED_COM:24mA;2/4/6/8/18/20/22/24mA	Z	Bit2 of General purpose I/O portA
32	ONOFF			PWR			ON/OFF reset signal
33	VDD			PWR			Core Logic PWR
34	VD15			PWR			1.5V DCDC feedback
35	NGND			GND			GND
36	LXVDD			PWR			DCDC Output
37	BAT			PWR			Battery Voltage input.
38	SYSPWR			PWR			System PWR
39	DC5V			PWR			5.0V Voltage
40	GPIOB0	GPIOB0	GPIOB0/LRADC1/REMOTE	DIO/AI	2/4/6/8/10/12/14/16mA	Z	Bit0 of General purpose I/O portB
41	GPIOA7	LED_COM7	GPIOA7/LED_COM7/EM_CEB4/LCD_SEG1/SIRQ1/PWM0/FMCLKOUT/MEJ_TRST/DEJ_RTCK	DIO	LED_COM:24mA;2/4/6/8/18/20/22/24mA	Z	Bit7 of General purpose I/O portA
42	VCC			PWR			Digital IO PWR
43	SVCC			PWR			PWR for standby
44	VRDA			PWR			
45	VREFI			PWR			Reference voltage input
46	AVCC			PWR			Analog IO PWR
47	AGND			GND			Analog GND
48	AUX1R		AUX1R/SIO5	AI/DIO	SIO:5mA		Linein/FM right channel input1
49	AUX1L		AUX1L/SIO4	AI/DIO	SIO:5mA		Linein/FM left channel input1
50	AUX0R		AUX0R/SIO3	SIO3	SIO:5mA		Linein/FM right channel input0

51	AUX0L		AUX0L/SIO2	AI/DIO	SIO:5mA		Linein/FM left channel input0
52	MICINR	MICINR	MICINR/MICINRN/DMICDAT/SIO1	AI/AI/DI/DIO	SIO:5mA		MIC right channel input
53	MICINL	MICINL	MICINL/MICINLP/DMICCLK/SIO0	AI/AI/DO/DIO	SIO:5mA		MIC left channel input
54	VRO	VRO	VRO/I2S_LRCLK/SIO7/AOUTLN	AO/DIO/DIO	2/4/6/8/10/12/14/16mA		Direct drive circuit reference voltage
55	AOUTL	AOUTL	AOUTL/AOUTLP/I2S_BCLK/SIO6	AO/DIO/DIO	2/4/6/8/10/12/14/16mA		Left channel output
56	AOUTR	AOUTR	AOUTR/AOUTRP/I2S_MCLK/SIO8	AO/DIO/DIO	2/4/6/8/10/12/14/16mA		Right channel output
57	VRO_S	VRO_S	VRO_S/I2S_DOUT/SIO9/AOUTRN	A0/DO/DIO	2/4/6/8/10/12/14/16mA		Direct drive circuit reference voltage
58	PAGND			GND			GND for PA
59	DM			DIO			USB Data minus
60	DP			DIO			USB Data plus
61	VCC			PWR			Digital IO PWR
62	GPIOA17	SD_CLK0	GPIOA17/SD_CLK0/UART_TX1/LCD_SEG15/SPI1_SCLK/MEJ_TCK	DIO	2/4/6/8/10/12/14/16mA	L	Bit17 of General purpose I/O portA
63	GPIOA20	SD_DAT0	GPIOA20/SD_DAT0/EM_D8/LCD_D8/LCD_SEG10/PWM2/SPI1_MISO/MEJ_TDI	DIO	2/4/6/8/10/12/14/16mA	Z	Bit20 of General purpose I/O portA
64	GPIOB7	LCD_SEG28	GPIOB7/DEJ_TMS/LCD_SEG28/PWM0/I2S_DOUT/I2S_DIN/TK1	DIO	2/4/6/8/10/12/14/16mA	H	Bit7 of General purpose I/O portB
65	GPIOB8	LCD_SEG29	GPIOB8/DEJ_TCK/LCD_SEG29/PWM1/I2S_BCLK/TK2	DIO	2/4/6/8/10/12/14/16mA	H	Bit8 of General purpose I/O portB
66	GPIOB9	LCD_SEG30	GPIOB9/DEJ_TDI/LCD_SEG30/PWM2/I2S_MCLK/TK3	DIO	2/4/6/8/10/12/14/16mA	H	Bit9 of General purpose I/O portB

67	GPIOA5	LED_COM5	GPIOA5/LED_COM5/EM_CEB2/LCD_COM5/PWM3/TK5	DIO	LED_COM:24 mA;2/4/6/8/18/20/22/24 mA	Z	Bit5 of General purpose I/O portA
68	GPIOA21	SD_DAT1	GPIOA21/SD_DAT1/EM_D9/LCD_D9/LCD_SEG11/UART_RX1/PWM0/SPI1_MOSI/TEMPADC/TK0/MEJ_TRST	DIO	2/4/6/8/10/12/14/16mA	Z	Bit21 of General purpose I/O portA

Note: H: high level; L:low level; Z: high resistance

2 Bluetooth

- Support Bluetooth V4.1
- Compatible with Bluetooth V2.1 and V3.0 systems
- Supports Bluetooth 4.1 Low Energy (BLE)
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/Esco link
- Supports Secure Simple Pairing
- Supports Low Power Mode (Sniff / Sniff Sub-rating / Hold / Park)
- Bluetooth 4.1 Dual Mode support: Simultaneous LE and BR / EDR
- Supports multiple Low Energy states
- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Integrated Class1, Class2, and Class 3 PA
- Bluetooth 3.0 compliant
- Supports Power / Enhanced Power Control
- Integrated 32K oscillator for power management

Performance

- Bluetooth transmitting power: -20dBm~10dBm
- Bluetooth receiving sensitivity: -93dBm

3 Processor Core

- 104MHz MIPS32 processor Core
- 32-bit Address and Data Paths
- MIPS32-Compatible Instruction Set
- MIPS32 Enhanced Architecture (Release 2) Features
- MIPS16e™ Code Compression
- Enhanced JTAG (EJTAG) Controller

4 DSP Core

Audio Configuration Features set

- High code compactness
- All instructions can be conditional
  - Conditional execution
  - Reduces cycle count and code size on control and overhead code
- Computational units:
  - One 32-bit x 32-bit Multiply-and-Accumulate (MAC) using 72-bit product
  - One 32-bit x 16-bit MAC using 72-bit product
  - One 32-bit x 32-bit MAC unit with automatic scaling
  - One 32-bit x 16-bit MAC unit with automatic scaling
  - One 36-bit arithmetic unit
  - One 36-bit logical unit
  - One 36-bit bit-manipulation unit, including a full barrel shifter and an exponent unit
  - Four 36-bit accumulators
  - Fully programmable product post-shifter for product scaling
- 32-bit Scalar (SC) unit for integer operations
- Unaligned memory access for load and store operations

5 Memory Controller

- Full synchronous design with operation clock rate up to 104MHz.
- It is accessible for all the RAM blocks through DMA0/1/2/3/4/5
- It is accessible for all the RAM blocks through DSP's data bus and program bus.
- It is accessible for all the RAM and ROM block through MIPS' data bus and program bus.
- The hardware code replace mechanism can fix up to 4 instructions at the same time.
- The page miss control mechanism can support 22 different pages at the same time.

6 DMA Controller

6.1 Features

- DMA transmission is independent with the CPU and DSP.
- Support for memory-to-memory, memory-to-peripheral, peripheral-to-memory, CARD-to-USB, and USB-to-CARD transmission.
- 6-channel DMA
  - 5-channel ordinary DMA, including DMA0, DMA1, DMA2, DMA3, and DMA4, supports for transmission in burst 8 mode.
  - 1-channel special DMA (DMA5), supports for transmission in single mode.
  - Only one of the six DMA channels can transfer data at the same time.
- DMA0/DMA1/DMA2/DMA3/DMA4 transmission can be triggered on the occurrence of selected events as following:
  - SPI TX DRQ
  - SPI RX DRQ
  - UART TX DRQ
  - UART RX DRQ
  - USB DRQ
  - ADC DRQ
  - SD/MMC DRQ
  - DAC DRQ
  - LCD DRQ
  - I2S TX DRQ
  - I2S RX DRQ
  - SPDIF TX DRQ
- DMA5 transmission can only be triggered by UART RX DRQ.
- Each channel can send two interrupts to the CPU on completion of certain operational events as following:
  - DMA5HFIP
  - DMA4HFIP
  - DMA3HFIP
  - DMA2HFIP
  - DMA1HFIP
  - DMA0HFIP
  - DMA5TCIP
  - DMA4TCIP
  - DMA3TCIP
  - DMA2TCIP
  - DMA1TCIP

- DMA0TCIP

- Transmission width includes 8-bit, 16-bit, 24-bit, 32-bit, and 64-bit, which is determined by DMA transmission type as following:
  - 8-bit: SPI, UART, ADC, DAC, I2S, and SPDIF
  - 16-bit: ADC, DAC, LCD, I2S, and SPDIF
  - 24-bit: ADC, DAC, I2S and SPDIF
  - 32-bit: memory, SPI, USB, and SD/MMC
  - 64-bit: memory

6.2 Memory and Peripheral Access Description

6.2.1 Access Peripheral FIFO

The peripherals that can be accessed by DMA are shown as following:

Table 6-1 Accessible Peripherals FIFO for DMA

FIFO Type	FIFO Width
SPI TX FIFO	32
SPI RX FIFO	32
UART TX FIFO	8
UART RX FIFO	8
USB FIFO	32
SD/MMC FIFO	32
LCD FIFO	16
I2S TX/DAC/SPDIF TX FIFO0	24
I2S TX/DAC/SPDIF TX FIFO1	24
I2S RX/ADC FIFO	24

6.2.2 DMA channel priority

The DMA can access the memory block, once the DMA obtains a highest priority and the DMA channel occupies the DMA bus according to the following internal priority table of DMA channels. The possible combinations of priority of each DMA channel are listed below:

Table 6-2 Priority of Each DMA Channel

Priority / Channel Combinations	Priority0 (highest)	Priority1	Priorit2	Priority3	Priority4	Priority5 (lowest)
0	DMA5	DMA0	DMA1	DMA2	DMA3	DMA4
1	DMA0	DMA5	DMA1	DMA2	DMA3	DMA4
2	DMA0	DMA1	DMA5	DMA2	DMA3	DMA4
3	DMA0	DMA1	DMA2	DMA5	DMA3	DMA4
4	DMA0	DMA1	DMA2	DMA3	DMA5	DMA4
5	DMA0	DMA1	DMA2	DMA4	DMA4	DMA5

6.3 DMA Register List

Table 6-3 DMA Control Group Base Address

Name	Physical Base Address	KSEG1 Base Address
DMAController	0xC00C0000	0xC00C0000

Table 6-4 DMA Controller Register List

Offset	Register Name	Description

0x00000000	DMAPriority	DMA priority register
0x00000004	DMAIP	DMA interrupt pending register
0x00000008	DMAIE	DMA interrupt enable register
0x00000010	DMA0CTL	DMA0 control register
0x00000014	DMA0SADDR0	DMA0 source address register 0
0x00000018	DMA0SADDR1	DMA0 source address register 1
0x0000001C	DMA0DADDR0	DMA0 destination address register 0
0x00000020	DMA0DADDR1	DMA0 destination address register 1
0x00000024	DMA0FrameLen	DMA0 frame length register
0x00000028	DMA1CTL	DMA1 control register
0x0000002C	DMA1SADDR0	DMA1 source address register 0
0x00000030	DMA1SADDR1	DMA1 source address register 1
0x00000034	DMA1DADDR0	DMA1 destination address register 0
0x00000038	DMA1DADDR1	DMA1 destination address register 1
0x0000003C	DMA1FrameLen	DMA1 frame length register
0x00000040	DMA2CTL	DMA2 control register
0x00000044	DMA2SADDR0	DMA2 source address register 0
0x00000048	DMA2SADDR1	DMA2 source address register 1
0x0000004C	DMA2DADDR0	DMA2 destination address register 0
0x00000050	DMA2DADDR1	DMA2 destination address register 1
0x00000054	DMA2FrameLen	DMA2 frame length register
0x00000058	DMA3CTL	DMA3 control register
0x0000005C	DMA3SADDR0	DMA3 source address register 0
0x00000060	DMA3SADDR1	DMA3 source address register 1
0x00000064	DMA3DADDR0	DMA3 destination address register 0
0x00000068	DMA3DADDR1	DMA3 destination address register 1
0x0000006C	DMA3FrameLen	DMA3 frame length register
0x00000070	DMA4CTL	DMA4 control register
0x00000074	DMA4SADDR0	DMA4 source address register 0
0x00000078	DMA4SADDR1	DMA4 source address register 1
0x0000007C	DMA4DADDR0	DMA4 destination address register 0
0x00000080	DMA4DADDR1	DMA4 destination address register 1
0x00000084	DMA4FrameLen	DMA4 frame length register
0x00000088	DMA5CTL	DMA5 control register
0x0000008C	DMA5DADDR	DMA5 destination address register
0x00000090	DMA5FrameLen	DMA5 frame length register
0x00000094	DMA5CONT	DMA5 counter register

6.4 DMA Register Description

6.4.1 DMAPriority

DMAPriority (DMA Priority Register, offset = 0x00000000)

Bits	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2:0	PRIORITYTAB	DMA Priority table : 5'd0:DMA5>DMA0>DMA1>DMA2>DMA3>DMA4 5'd1:DMA0>DMA5>DMA1>DMA2>DMA3>DMA4 5'd2:DMA0>DMA1>DMA5>DMA2>DMA3>DMA4 5'd3:DMA0>DMA1>DMA2>DMA5>DMA3>DMA4 5'd4:DMA0>DMA1>DMA2>DMA3>DMA5>DMA4	RW	0x0

		5'd5:DMA0>DMA1>DMA2>DMA3>DMA4>DMA5 Others:DMA5>DMA0>DMA1>DMA2>DMA3>DMA4		

6.4.2 DMAIP

DMAIP (DMA Interrupt Pending Register, offset = 0x00000004)

Bits	Name	Description	Access	Reset
31:14	-	Reserved	-	-
13	DMA5HFIP	DMA5 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
12	DMA4HFIP	DMA4 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
11	DMA3HFIP	DMA3 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
10	DMA2HFIP	DMA2 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
9	DMA1HFIP	DMA1 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
8	DMA0HFIP	DMA0 Half Transmission IRQ Pending This bit can be written '1' to clear. (1)	RW	0x0
7:6	-	Reserved	-	-
5	DMA5TCIP	DMA5 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
4	DMA4TCIP	DMA4 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
3	DMA3TCIP	DMA3 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
2	DMA2TCIP	DMA2 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
1	DMA1TCIP	DMA1 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0
0	DMA0TCIP	DMA0 Transmission Complete IRQ Pending This bit can be written '1' to clear.	RW	0x0

6.4.3 DMAIE

DMAIE (DMA Interrupt Enable Register, offset = 0x00000008)

Bits	Name	Description	Access	Reset
31:14	-	Reserved	-	-
13	DMA5HFIE	DMA5 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
12	DMA4HFIE	DMA4 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
11	DMA3HFIE	DMA3 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
10	DMA2HFIE	DMA2 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
9	DMA1HFIE	DMA1 Half Transmission Complete IRQ enable:	RW	0x0

		0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.		
8	DMA0HFIE	DMA0 Half Transmission Complete IRQ enable: 0: Disable Half Transmission Complete interrupt; 1: Enable Half Transmission Complete interrupt.	RW	0x0
6:7	-	Reserved	-	-
5	DMA5TCIE	DMA5 Transmission Complete IRQ Enable: 0: disable DMA5 Transmission Complete interrupt 1: enable DMA5 Transmission Complete interrupt	RW	0x0
4	DMA4TCIE	DMA4 Transmission Complete IRQ Enable: 0: disable DMA4 Transmission Complete interrupt 1: enable DMA4 Transmission Complete interrupt	RW	0x0
3	DMA3TCIE	DMA3 Transmission Complete IRQ Enable: 0: disable DMA3 Transmission Complete interrupt 1: enable DMA3 Transmission Complete interrupt	RW	0x0
2	DMA2TCIE	DMA2 Transmission Complete IRQ Enable: 0: disable DMA2 Transmission Complete interrupt 1: enable DMA2 Transmission Complete interrupt	RW	0x0
1	DMA1TCIE	DMA1 Transmission Complete IRQ Enable: 0: disable DMA1 Transmission Complete interrupt 1: enable DMA1 Transmission Complete interrupt	RW	0x0
0	DMA0TCIE	DMA0 Transmission Complete IRQ Enable: 0: disable DMA0 Transmission Complete interrupt 1: enable DMA0 Transmission Complete interrupt	RW	0x0

6.4.4 DMA0CTL

DMA0CTL (DMA0 control Register, offset = 0x00000010)

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	AUDIOTYPE	The method of audio data stored of DMA-ADC, DMA-DAC, DMA-I2S transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15:14	DATAWIDTH	The data width to write to DAC/I2S TX or read from ADC/I2S TX FIFO: 00: 8bit 01: 16bit 10: 24bit 11: reserved The data width to write to SPI TX FIFO or read from SPI RX FIFO: 00: 8bit 01: reserved 10: reserved 11: 32bit	RW	0x0
13:12	-	Reserved	-	-
11:8	DSTTYPE	Destination type: 4'b0000: memory 4'b0010: SPI**0** TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: USB FIFO 4'b0110: SD/MMC FIFO	RW	0x0

		4'b0111: LCD FIFO 4'b1001: UART1 TX FIFO 4'b1011: I2S TX/DAC/SPDIF TX FIFO0 4'b1100: I2S TX/DAC/SPDIF TX FIFO1 4'b1111: SPI1 TX FIFO Others: Reserved		
7:4	SRCTYPE	Source type: 4'b0000: memory 4'b0010: SPI**0** RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: USB FIFO 4'b0110: SD/MMC FIFO 4'b1001: UART1 RX FIFO 4'b1011:I2S RX/ADC FIFO 4'b1100: reserved 4'b1111: SPI1 RX FIFO Others: Reserved	RW	0x0
3:2	-	Reserved	-	-
1	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA0START	DMA0 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA0 controller if the DMA0 transmission is complete or DMA0 transmission error occurs. This bit can be written '0' to abort DMA0 transmission.	RW	0x0

6.4.5 DMA0SADDR0

DMA0SADDR0 (DMA0 Source Address Register 0, offset = 0x00000014)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA0SADDR0	The source address 0 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.6 DMA0SADDR1

DMA0SADDR1 (DMA0 Source Address Register 1, offset = 0x00000018)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA0SADDR1	The source address 1 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.7 DMA0DADDR0

DMA0DADDR0 (DMA0 Destination Address Register 0, offset = 0x0000001C)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA0DADDR0	The destination address 0 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.8 DMA0DADDR1

DMA0DADDR1 (DMA0 Destination Address Register 1, offset = 0x00000020)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA0DADDR1	The destination address 1 of DMA0 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.9 DMA0FrameLen

DMA0FrameLen (DMA0 Frame Length Register 1, offset = 0x00000024)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA0FrameLen	The frame length of DMA0 transmission. If DSTTYPE is I2S TX (DAC/SPDIF TX) FIFO or LCD FIFO, the value of DMA0FrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is I2S RX (ADC) FIFO, the value of DMA0FrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA0FrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

6.4.10 DMA1CTL

DMA1CTL (DMA1 control Register, offset = 0x00000028)

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	AUDIOTYPE	The method of audio data stored of DMA-ADC/ DMA-DAC/ DMA-I2S transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15:14	DATAWIDTH	The data width to write DAC/I2S TX FIFO or read from ADC/I2S TX FIFO: 00: 8bit 01: 16bit 10: 24 bit 11: reserved The data width to write SPI TX FIFO or read from SPI RX FIFO: 00: 8bit 01: reserved 10: reserved 11: 32bit	RW	0x0
13:12	-	Reserved	-	-

11:8	DSTTYPE	Destination type: 4'b0000: memory 4'b0010: SPI**0** TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: USB FIFO 4'b0110: SD/MMC FIFO 4'b0111: LCD FIFO 4'b1001: UART1 TX FIFO 4'b1011: I2S TX/DAC/SPDIF TX FIFO0 4'b1100: I2S TX/DAC/SPDIF TX FIFO1 4'b1111: SPI1 TX FIFO Others: Reserved	RW	0x0
7:4	SRCTYPE	Source type: 4'b0000: memory 4'b0010: SPI**0** RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: USB FIFO 4'b0110: SD/MMC FIFO 4'b1001: UART1 RX FIFO 4'b1011:I2S RX/ADC FIFO 4'b1111: SPI1 RX FIFO Others: Reserved	RW	0x0
3:2	-	Reserved	-	-
1	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA1START	DMA1 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA1 controller if the DMA1 transmission is complete or DMA1 transmission error occurs. This bit can be written '0' to abort DMA1 transmission.	RW	0x0

6.4.11 DMA1SADDR0

DMA1SADDR0 (DMA1 Source Address Register 0, offset = 0x0000002C)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA1SADDR0	The source address 0 of DMA1 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.12 DMA1SADDR1

DMA1SADDR1 (DMA1 Source Address Register 1, offset = 0x00000030)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA1SADDR1	The source address 1 of DMA1 transmission. The bit[0] is no effect if data width is 16-bit.	RW	0x0

		The bit[1:0] is no effect if data width is 24-bit or 32-bit.		

6.4.13 DMA1DADDR0

DMA1DADDR0 (DMA1 Destination Address Register 0, offset = 0x00000034)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA1DADDR0	The destination address 0 of DMA1 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.14 DMA1DADDR1

DMA1DADDR1 (DMA1 Destination Address Register 1, offset = 0x00000038)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA1DADDR1	The destination address 1 of DMA1 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.15 DMA1FrameLen

DMA1FrameLen (DMA1 Frame Length Register 1, offset = 0x0000003c)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA1FrameLen	The frame length of DMA1 transmission. If DSTTYPE is I2S TX (DAC/SPDIF TX) FIFO or LCD FIFO, the value of DMA1FrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is I2S RX (ADC) FIFO or, the value of DMA1FrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DM1FrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

6.4.16 DMA2CTL

DMA2CTL (DMA2 control Register, offset = 0x00000040)

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	AUDIOTYPE	The method of audio data stored of DMA-ADC/ DMA-DAC/DMA-I2S transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15:14	DATAWIDTH	The data width to write DAC/I2S TX FIFO or read from ADC/I2S TX FIFO: 00: 8bit 01: 16bit 10: 24bit 11: reserved The data width to write SPI TX FIFO or read from SPI RX	RW	0x0

		FIFO: 00: 8bit 01: reserved 10: reserved 11: 32bit		
13:12	-	Reserved	-	-
11:8	DSTTYPE	Destination type: 4'b0000: memory 4'b0010: SPI0 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: USB FIFO 4'b0110: SD/MMC FIFO 4'b0111: LCD FIFO 4'b1001: UART1 TX FIFO 4'b1011: I2S TX/DAC/SPDIF TX FIFO0 4'b1100: I2S TX/DAC/SPDIF TX FIFO1 4'b1111: SPI1 TX FIFO Others: Reserved	RW	0x0
7:4	SRCTYPE	Source type: 4'b0000: memory 4'b0010: SPI0 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: USB FIFO 4'b0110: SD/MMC FIFO 4'b1001: UART1 RX FIFO 4'b1011:I2S RX/ADC FIFO 4'b1111: SPI1 RX FIFO Others: Reserved	RW	0x0
3:2	-	Reserved	-	-
1	RELOAD	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA2START	DMA2 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA2 controller if the DMA2 transmission is complete or DMA2 transmission error occurs. This bit can be written '0' to abort DMA2 transmission.	RW	0x0

6.4.17 DMA2SADDR0

DMA2SADDR0 (DMA2 Source Address Register 0, offset = 0x00000044)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA2SADDR0	The source address 0 of DMA2 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.18 DMA2SADDR1

DMA2SADDR1 (DMA2 Source Address Register 1, offset = 0x00000048)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA2SADDR1	The source address 1 of DMA2 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.19 DMA2DADDR0

DMA2DADDR0 (DMA2 Destination Address Register 0, offset = 0x0000004C)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA2DADDR0	The destination address 0 of DMA2 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.20 DMA2DADDR1

DMA2DADDR1 (DMA2 Destination Address Register 1, offset = 0x00000050)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA2DADDR1	The destination address 1 of DMA2 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.21 DMA2FrameLen

DMA2FrameLen (DMA2 Frame Length Register 1, offset = 0x00000054)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA2FrameLen	The frame length of DMA2 transmission. If DSTTYPE is I2S TX (DAC/SPDIF TX) FIFO or LCD FIFO, the value of DMA2FrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is I2S RX (ADC) FIFO or, the value of DMA2FrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA2FrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

6.4.22 DMA3CTL

DMA3CTL (DMA3 control Register, offset = 0x00000058)

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	AUDIOTYPE	The method of audio data stored of DMA-ADC/ DMA-DAC/DMA-I2S transmission: 0: interleaved stored in the memory	RW	0x0

		1: separated stored in the memory		
15:14	DATAWIDTH	The data width to write DAC/I2S TX FIFO or read from ADC/I2S TX FIFO: 00: 8bit 01: 16bit 10: 24bit 11: reserved The data width to write SPI TX FIFO or read from SPI RX FIFO: 00: 8bit 01: reserved 10: reserved 11: 32bit	RW	0x0
13:12	-	Reserved	-	-
11:8	DSTTYPE	Destination type: 4'b0000: memory 4'b0010: SPI**0** TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: USB FIFO 4'b0110: SD/MMC FIFO 4'b0111: LCD FIFO 4'b1001: UART1 TX FIFO 4'b1011: I2S TX/DAC/SPDIF TX FIFO0 4'b1100: I2S TX/DAC/SPDIF TX FIFO1 4'b1111: SPI1 TX FIFO Others: Reserved	RW	0x0
7:4	SRCTYPE	Source type: 4'b0000: memory 4'b0010: SPI**0** RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: USB FIFO 4'b0110: SD/MMC FIFO 4'b1001: UART1 RX FIFO 4'b1011:I2S RX/ADC FIFO 4'b1111: SPI1 RX FIFO Others: Reserved	RW	0x0
3:2	-	Reserved	-	-
1	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA3START	DMA3 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA3 controller if the DMA3 transmission is complete or DMA3 transmission error occurs. This bit can be written '0' to abort DMA3 transmission.	RW	0x0

6.4.23 DMA3SADDR0

DMA3SADDR0 (DMA3 Source Address Register 0, offset = 0x0000005c)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA3SADDR0	The source address 0 of DMA3 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.24 DMA3SADDR1

DMA3SADDR1 (DMA3 Source Address Register 1, offset = 0x00000060)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA3SADDR1	The source address 1 of DMA3 transmission. The DMA3SADDR1[0] is no effect if data size is 16 bit, 24 bit or 32 bit. The DMA3SADDR1[1] is no effect if data size is 24 bit or 32 bit.	RW	0x0

6.4.25 DMA3DADDR0

DMA3DADDR0 (DMA3 Destination Address Register 0, offset = 0x00000064)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA3DADDR0	The destination address 0 of DMA3 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.26 DMA3DADDR1

DMA3DADDR1 (DMA3 Destination Address Register 1, offset = 0x00000068)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA3DADDR1	The destination address 1 of DMA3 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.27 DMA3FrameLen

DMA3FrameLen (DMA3 Frame Length Register 1, offset = 0x0000006c)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA3FrameLen	The frame length of DMA3 transmission. If DSTTYPE is I2S TX (DAC) FIFO or LCD FIFO, the value of DMA3FrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is I2S RX (ADC) FIFO or, the value of DMA3FrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA3FrameLen is equal to the number of bytes transferred by DMA.	RW	0x0

6.4.28 DMA4CTL

DMA4CTL (DMA4 control Register, offset = 0x00000070)

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	AUDIOTYPE	The method of audio data stored of DMA-ADC/ DMA-DAC/DMA-I2S transmission: 0: interleaved stored in the memory 1: separated stored in the memory	RW	0x0
15:14	DATAWIDTH	The data width to write DAC/I2S TX or read from ADC/I2S TX FIFO: 00: 8bit 01: 16bit 10: 24bit 11: reserved The data width to write SPI TX FIFO or read from SPI RX FIFO: 00: 8bit 01: reserved 10: reserved 11: 32bit	RW	0x0
13:12	-	Reserved	-	-
11:8	DSTTYPE	Destination type: 4'b0000: memory 4'b0010: SPI0 TX FIFO 4'b0011: UART0 TX FIFO 4'b0100: USB FIFO 4'b0110: SD/MMC FIFO 4'b0111: LCD FIFO 4'b1001: UART1 TX FIFO 4'b1011: I2S TX/DAC/SPDIF TX FIFO0 4'b1100: I2S TX/DAC/SPDIF TX FIFO1 4'b1111: SPI1 TX FIFO Others: Reserved	RW	0x0
7:4	SRCTYPE	Source type: 4'b0000: memory 4'b0010: SPI0 RX FIFO 4'b0011: UART0 RX FIFO 4'b0100: USB FIFO 4'b0110: SD/MMC FIFO 4'b1001: UART1 RX FIFO 4'b1011:I2S RX/ADC FIFO 4'b1111: SPI1 RX FIFO Others: Reserved	RW	0x0
3:2	-	Reserved	-	-
1	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA4START	DMA4 start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data	RW	0x0

		width to the DMA controller. This bit will be automatically cleared by the DMA4 controller if the DMA4 transmission is complete or DMA4 transmission error occurs. This bit can be written '0' to abort DMA4 transmission.		

6.4.29 DMA4SADDR0

DMA4SADDR0 (DMA4 Source Address Register 0, offset = 0x00000074)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA4SADDR0	The source address 0 of DMA4 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.30 DMA4SADDR1

DMA4SADDR1 (DMA4 Source Address Register 1, offset = 0x00000078)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA4SADDR1	The source address 1 of DMA4 transmission. The DMA4SADDR1[0] is no effect if data size is 16 bit, 24 bit or 32 bit. The DMA4SADDR1[1] is no effect if data size is 24 bit or 32 bit.	RW	0x0

6.4.31 DMA4DADDR0

DMA4DADDR0 (DMA4 Destination Address Register 0, offset = 0x0000007C)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA4DADDR0	The destination address 0 of DMA4 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.32 DMA4DADDR1

DMA4DADDR1 (DMA4 Destination Address Register 1, offset = 0x00000080)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA4DADDR1	The destination address 1 of DMA4 transmission. The bit[0] is no effect if data width is 16-bit. The bit[1:0] is no effect if data width is 24-bit or 32-bit.	RW	0x0

6.4.33 DMA4FrameLen

DMA4FrameLen (DMA4 Frame Length Register 1, offset = 0x00000084)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA4FrameLen	The frame length of DMA4 transmission. If DSTTYPE is I2S TX (DAC/SPDIF TX) FIFO or LCD FIFO, the	RW	0x0

		value of DMA4FrameLen is equal to the times that DMA writes FIFO. If SRCTYPE is I2S RX (ADC) FIFO or, the value of DMA4FrameLen is equal to the times that DMA reads FIFO. If other DSTTYPE or SRCTYPE, the value of DMA4FrameLen is equal to the number of bytes transferred by DMA.		

6.4.34 DMA5CTL

DMA5CTL (DMA5 control Register, offset = 0x00000088)

Bits	Name	Description	Access	Reset
31:5	-	Reserved	-	-
4	SRCTYPE	Source type: 1'b0: UART0 RX FIFO 1'b1: UART1 RX FIFO	RW	0x0
3:2	-	Reserved	-	-
1	reload	Reload the DMA controller registers and start DMA transmission after current DMA transmission is complete: 0: disable reload mode 1: enable reload mode	RW	0x0
0	DMA5START	Special DMA start bit: A low-to-high conversion of this bit will lead to load source address, destination address, destination step size, source step size, transfer type, burst length, DRQ type, and data width to the DMA controller. This bit will be automatically cleared by the DMA controller if the DMA transmission is complete or DMA transmission error occurs. This bit can be written '0' to abort DMA transmission.	RW	0x0

6.4.35 DMA5DADDR

DMA5DADDR (DMA5 Destination Address Register, offset = 0x0000008C)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA5DADDR	The destination address of Special DMA transmission.	RW	0x0

6.4.36 DMA5FrameLen

DMA5FrameLen (DMA5 Frame Length Register 1, offset = 0x00000090)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA5FrameLen	The value of DMA5FrameLen is equal to the number of bytes transferred by Special DMA.	RW	0x0

6.4.37 DMA5CONT

DMA5CONT (DMA5 counter register, offset = 0x00000094)

Bits	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17:0	DMA5CONT	The counter is equal to the number of bytes written to	R	0x0

		memory by special DMA currently. The counter is cleared automatically by hardware when special DMA transmission is complete.		

7 PMU

7.1 Features

The ATS2825 integrates a comprehensive power supply system, including the following features:

- Supports Li-Ion battery / 5V power supply and Integrate Linear battery charger
- Integrated DC-DC buck converters output 1.5V, which can be switch to LDO mode.
- Linear regulators output VCC, BTVCC, AVCC

7.2 Module Description

7.2.1 DC-DC Converter

The DC-DC converter integrated in ATS2825 efficiently scales battery voltage to the required supply voltage. It can work in Pulse Frequency Modulation (PFM) or Pulse Width Modulation (PWM) automatically for different load current.

7.2.2 Linear Regulators

The ATS2825 integrates multiple linear regulators; they generate VCC, VDD, AVCC, BTVCC and VD15.

7.2.2.1 Regulators Accurate and Maximum Output Current

The output voltages are precisely within ±2%, providing large currents with a significantly small dropout voltage within ±5%. Table below shows data of maximum output current.

Table 7-1 Regulators Maximum Output Current

Block Name	Output Voltage	Load Capacity
VCC	2.7~3.4V	300 mA
VDD	0.8~1.5V	100 mA
VD15	1.0~1.7V	170 mA
BTVCC	2.8~3.5V	100 mA
AVCC	VCC-0.15V	50 mA@98%

7.2.2.2 Regulators Power Down

If the system is to operate from an external power supply, then the internal linear regulators are powered down automatically.

7.2.3 Li-Ion Cell Charger

Some products in the ATS2825 family integrate charging for Li-Ion battery from a 5-V source connected to the DC5V pin. The battery charger is essentially a linear regulator that has current and voltage limits. Charge current is software-programmable within REG[CHG_CURRENT]. You can enable charger by setting REG[CHG_EN]=1.

One can programmatically monitor the battery voltage using the BATADC. The charger has its own voltage limiting that operates independently of the BATADC. But monitoring the battery voltage and VBUS voltage during the charge might be helpful for reporting the charge progress.

The battery charger is capable of generating a large amount of heat within the ATS2825, especially at currents above 400 mA. The dissipated power can be estimated as: (5V – battery voltage) * current. At max current (500 mA) and a 3-V battery, the charger can dissipate 1 W.
The TEMPADC can be used to monitor battery temperatures.
The SENSADC is used to monitor the charger and diode's temperature.

7.2.4 Reference Voltage

7.2.5 A/D Converters

There are 4 low resolutions 7 bit A/Ds for system monitor, the input voltage range of which is 0.7V to 2.2V at TEMPADC pin, 1.4V to 4.4V at VBAT pin, 2.1V to 6.6V at DC5V pin and 0.7V to 2.2V at temp sensor circuit, 0V to SVCC at LRADC1 / LRADC2 / LRADC3 pin.

1LSB= 3.1/(2^7) = 24.22mV

When the input voltage is V, the related ADC data n = V/(3.1/2^7).
Then the data n is 0x00 related from 0V to 0.02422V, the data n is 0x01 related from 0.02422Vto 0.4844V.

7.3 Register List

Table 7-2 PMU block base address

Name	Physical Base Address	KSEG1 Base Address
PMU	0xC0020000	0xC0020000

Table 7-3 PMU Block Configuration Registers List

Offset	Register Name	Description	Voltage Domain
0x00	VOUT_CTL	VCC/VDD/AVCC voltage set Register	VDD
0x04	MULTI_USED	multi-used set Register	VDD
0x08	VD15_DCDC_CTL	VDD DCDC Modulation/frequency/MAX current set Register	RTCVDD
0x0C	CHG_CTL	Charge enable and current set Register	VDD
0x10	CHG_DET	Charge status detect Register	VDD
0x14	PMUADC_CTL	PMU ADC frequency and enable Register	RTCVDD
0x18	BATADC_DATA	BATADC data Register	VDD
0x1C	TEMPADC_DATA	TEMPADC data Register	VDD
0x20	DC5VADC_DATA	DC5V ADC data Register	VDD
0x24	SENSADC_DATA	Sensor ADC DATA Register	VDD
0x28	LRADC1_DATA	LRADC1 data Register	VDD
0x2C	LRADC2_DATA	LRADC2 data Register	VDD
0x30	LRADC3_DATA	LRADC3 data Register	VDD
0x38	BDG_CTL	Bandgap enable and voltage set Register	RTCVDD
0x3C	LDO_CTL	LDO SET Register	RTCVDD
0x40	SYSTEM_SET	System set Register	RTCVDD
0x44	POWER_CTL	POWER on/off control Register	RTCVDD
0x48	TIMER_CTL	S3/S3BT MODE auto Play/standby time set	RTCVDD
0x4C	WKEN_CTL	Wake up source select Register	RTCVDD
0x50	WAKE_PD	Wake up source pending	RTCVDD
0x54	ONOFF_KEY	On/off KEY control Register	RTCVDD
0x5C	NFC_CTL	NFC field detect control	RTCVDD
0x64	SPD_CTL	Standby mode power pull down	RTCVDD

7.4 Register Description

7.4.1 VOUT_CTL

Voltage set register (VDD) Default: 0x60048

Offset: 0x00

Bit (s)	Name	Description	Access	Reset
31:20	-	Reserved	-	-
19	TK_IBIAS	Touch key offset current enable: 0: disable 1: enable	RW	0
18	AVDD_PD	AVDD no capacitor LDO pull down 0: no pull down 1: 1mA pull down	RW	1
17:16	AVDD_VOL	00 1.0V 01 1.1V 10 1.2V 11 1.3V	RW	0x2
15	-	Reserved	-	-
13:12	AVCC_DROP	AVCC LDO margin tuning, voltage drop from VCC 00 0.15V 01 0.20V 10 0.25V 11 0.30V	RW	00
11:10	-	Reserved	-	-
9	VCCOC_SET	VCC LDO Current limit: 0: 400mA 1: 500mA	RW	0
8	VDDOC_SET	VDD LDO Current limit: 0: 200mA 1: 300mA	RW	0
7	-	Reserved	-	-
6:4	VCC_SET	VCC voltage level select 000: 2.7V 001: 2.8V 010: 2.9V 011: 3.0V 100: 3.1V 101: 3.2V 110: 3.3V 111: 3.4V	RW	0x4
3:0	VDD_SET	VDD (Regulator) voltage coarse control 0000: 0.80V 0001: 0.85V 0010: 0.90V 0011: 0.95V 0100: 1.00V 0101: 1.05V 0110: 1.10V 0111: 1.15V	RW	0x8

		1000: 1.20V 1001: 1.25V 1010: 1.30V 1011: 1.35V 1100: 1.40V 1101: 1.45V 1111: 1.50V		

7.4.2 MULTI_USED

Multi use register (VDD) Default: 0x80

Offset: 0x04

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8	UVDD_EN	USBVDD LDO enable: 0: disable 1: enable	RW	0
7:5	UVDD_V	USBVDD LDO output voltage control: 000 1.00 001 1.05 010 1.10 011 1.15 100 1.20 101 1.25 110 1.30 111 reserved	RW	0x4
4:2	-	Reserved	-	-
1	SEG_DISP_VCC_EN	Section code screen power enable control bit 0: disable 1: enable	RW	0
0	SEG_LED_EN	Nixie tube constant current enable bit 0: disable 1: enable	RW	0

7.4.3 VD15_DCDC_CTL

VD15 DCDC set register (RTCVDD) Default: 0x942625

Offset: 0x08

Bit (s)	Name	Description	Access	Reset
29:17	-	Reserved	-	-
16:15	ANTI_ADUIO	Provide pull down current selection 00: disable 01: 4mA 10: 8mA 11: 12mA	RW	0
14:13	-	Reserved	-	-
12:11	VD15_MODE_S1	Under S1 state, VD15 using DCDC or LDO mode switch bit: 00: fixed to LDO 01: fixed to DCDC 10: switch automatically through UVLO signal 11: switch automatically through DC5VOV signal	RW	0
9:8	-	Reserved	-	-

3:1	DCDC_FS	DC-DC frequency control 000: 889KHz (8 / 9) 001: 1MHz 010: 1.4MHz 011: 2MHz 100: 2.6MHz 101: 3MHz 110: 4MHz 111: 4MHZ Adjustable DC-DC frequency for difference load current.	RW	0x2
0	-	Reserved	-	-

7.4.4 CHG_CTL

Charging control register (VDD) Default: 0x18013A

Offset = 0x0C

Bit (s)	Name	Description	Access	Reset
31:21	-	Reserved	-	-
19	DC5VOV_EN	DC5V overvoltage detection enable bit 0:disable/ reset 1:enable	RW	1
16	-	Reserved	-	-
15	CHGEN	Enable Charge Circuit 0:disable 1:enable	RW	0
14	ENTKLE	Trickle charging enable: 0: disable trickle charge. 1: enable trickle charge.	RW	0
13:11	CHG_CURRENT	Charger constant charging Current Configure 000:25mA 001:50mA 010:100mA 011:200mA 100:300mA 101:400mA 110:500mA 111:600mA	RW	0
10	ENBATDT	Battery detection enable bit: 0:disable 1:enable	RW	0
9:7	ENFASTCHG	Constant charging voltage setting: 000: 4.2V 001: 4.23V 010: 4.26V 011: 4.29V 100: 4.32V 101: 4.35V 110: 4.38V 111: 4.41V	RW	0x2
6:5	STOPV	End-of-charging voltage	RW	1

		00: 4.16V 01 :4.18V 10: 4.32V 11: 4.34V		
4	ENSAMP	DC5V constant loop enable bit: 0:disable 1:enable	RW	1
3:2	STDY_SET	Set DC5V steady voltage 00 3.81 01 4.0 10 4.25 11 4.4	RW	0x2
1	ENCHGATDT	Auto detection of end-of-charging enable bit 0:disable 1:enable	RW	1
0	DTSEL	End-of-charging detection time selection: 0: once per 12min 1: once per 20s	RW	0

7.4.5 CHG_DET

Charging detect register (VDD)

Offset = 0x10

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	UVLO	DC5V insertion detection conditions: 0: no DC5V is inserted 1: DC5V >= BAT+0.1V or BAT+0.02V	R	x
6:5	CHGPHASE	Charging state flag bit 00: reserved 01: trickle charging phase 10: CC charging phase 11: CV charging phase	R	x
4	CHG_STA0	Whether Ichg>5%Ichg_reg flag 0: Ichg<5%Ichg_reg 1: Ichg>5%Ichg_reg	R	x
3	CHG_STA1	Whether Ichg>20%Ichg_reg flag 0: Ichg<20%Ichg_reg 1: Ichg>20%Ichg_reg	R	x
2	CHGEND	End-of-charging flag 0: in charging 1: end-of-charging	R	x
1	BATEXT	BAT exsistants flag 0: no battery 1: battery is on	R	x
0	DTOVER	Battery detection over flag 0: under detection 1: detection is over	R	x

7.4.6 PMUADC_CTL

PMUADC Control Register Default: 0xD7

Offset = 0x14

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	BATADC_FS	BAT/DC5V/TEMP/SENSOR ADCs Frequency Source Select: 0: 125HZ 1: 250HZ	RW	1
6	LRADC_FS	LRADC1234 Frequency Source Select: 0: 125HZ 1: 250HZ	RW	1
5	LRADC234_EN	7bit LRADC2/3/4 A/D enable. 0: Disable 1: Enable	RW	0
4	LRADC1_EN	7bit LRADC1 A/D enable. 0: Disable 1: Enable	RW	1
3	SENSORADC_EN	TEMP sensor A/D enable 0: Disable, TEMP sensor circuit and output disable 1: Enable, TEMP sensor circuit and output enable	RW	0
2	DC5VADC_EN	DC5V A/D enable 0: Disable 1: Enable	RW	1
1	TEMPADC_EN	TEMP A/D enable 0: Disable 1: Enable	RW	1
0	BATADC_EN	Battery A/D enable 0: Disable 1: Enable	RW	1

7.4.7 BATADC_DATA

BATADC DATA Register (VDD)

Offset = 0x18

Bit (s)	Name	Description	Access	Reset
15:7	-	Reserved	-	-
6:0	BATADC	7bit Voltage ADC, used to detect Battery voltage. Input voltage range is: Li-ion: 1.4-4.4V	R	x

7.4.8 TEMPADC_DATA

TEMPADC DATA Register (VDD)

Offset = 0x1C

Bit (s)	Name	Description	Access	Reset
15:7	-	Reserved	-	-
6:0	TEMPADC	7bit Voltage ADC, used to detect TEMPADC voltage. Input voltage range is: 0.7-2.2V	R	x

7.4.9 DC5VADC_DATA

DC5V ADC DATA Register (VDD)

Offset = 0x20

Bit (s)	Name	Description	Access	Reset

15:7	-	Reserved	-	-
6:0	DC5VADC	7bit Voltage ADC, used to detect DC5V voltage. Input voltage range is: 2.1-6.6V	R	x

7.4.10 SENSADC_DATA

Sensor ADC DATA Register (VDD)

Offset = 0x24

Bit (s)	Name	Description	Access	Reset
15:7	-	Reserved	-	-
6:0	SENSADC	7bit Voltage ADC, used to detect TEMPSENSOR voltage.	R	x

7.4.11 LRADC1_DATA

LRADC1 DATA Register (VDD)

Offset = 0x28

Bit (s)	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6:0	LRADC1	7bit LRADC1 data output LRADC1 input voltage range is from 0 to AVCC.	R	x

7.4.12 LRADC2_DATA

LRADC2 DATA Register (VDD)

Offset = 0x2C

Bit (s)	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6:0	LRADC2	7bit LRADC2 data output LRADC2 input voltage range is from 0 to AVCC.	R	x

7.4.13 LRADC3_DATA

LRADC3 DATA Register (VDD)

Offset = 0x30

Bit (s)	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6:0	LRADC3	7bit LRADC3 data output. LRADC3 input voltage range is from 0 to AVCC.	R	x

7.4.14 BDG_CTL

Bandgap Control Register (RTCVDD) Default: 0x2D

Offset = 0x38

Bit (s)	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6	BDG_FILTER	BANDGAP filter Control REG 0: BANDGAP has no filter resistor 1: BANDGAP has filter resistor Notes: Make sure this bit is set to 1 before using	RW	0

		DAC/ADC, OR IT WILL CAUSE BIG NOISE!		
5	BDG_PDR	BANDGAP pull down resistor control 0: NO pull down resistor 1: have pull down resistor	RW	1

7.4.15 LDO_CTL

LDO set register (RTCVDD) Default: 0x002AA888

Offset: 0x3C

Bit (s)	Name	Description	Access	Reset
31:19	-	Reserved	-	-
18	VD15OC_SET	VD15 LDO Current limit: 0: 270mA 1: 370mA	RW	0
17:14	VD15_SET	VD15 DC-DC / Regulator voltage coarse control 0000: 1.00V 0001: 1.05V 0010: 1.10V 0011: 1.15V 0100: 1.20V 0101: 1.25V 0110: 1.30V 0111: 1.35V 1000: 1.40V 1001: 1.45V 1010: 1.50V 1011: 1.55V 1100: 1.60V 1101: 1.65V 1111: 1.70V	RW	0xA
13	BTVDD_PD	BTVDD no capacitor LDO pull down 0: no pull down 1: 1mA pull down	RW	1
12	BTVDD_EN	BTVDD enable bit 0: disable 1: enable	RW	0
11:8	BTVDD_VOL	BTVDD voltage coarse control 0000: 0.80V 0001: 0.85V 0010: 0.90V 0011: 0.95V 0100: 1.00V 0101: 1.05V 0110: 1.10V 0111: 1.15V 1000: 1.20V 1001: 1.25V 1010: 1.30V 1011: 1.35V 1100: 1.40V 1101: 1.45V 1111: 1.50V	RW	0x8
4	BTVCCOC_SET	BTVCC LDO Current limit:	RW	0

		0: 200mA 1: 300mA		
3:1	BTVCC_VOL	BTVCC voltage level select 000: 2.8V 001: 2.9V 010: 3.0V 011: 3.1V 100: 3.2V 101: 3.3V 110: 3.4V 111: 3.5V	RW	0x4
0	BTVCC_EN	BTVCC power enable: 0: disable 1: enable	RW	0

7.4.16 SYSTEM_SET

System set Register (RTCVDD) Default: 0x3BF

Offset = 0x40

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	LB_EN	LB (Low battery) enter standby enable: 0: disable 1: enable	RW	1
6:5	LB_VOL	LB (Low battery) voltage setting 00: 2.7V 01: 3.0V 1x: 3.3V	RW	1
4	OC_EN	VCC/VDD/BTVCC/VD15 LDO overcurrent protection enable bit 0: disable 1: enable	RW	1
3	LVPRO_EN	VCC/VDD/BTVCC/VD15 undervoltage protection enable 0: disable 1: enable	RW	1

7.4.17 POWER_CTL

Power source as VCC/VDD/BTVCC/SVCC on/off Control Register (RTCVDD) Default: 0x1

Offset = 0x44

Bit (s)	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2	EN_S3	EN_S3 enable bit 0:disable 1:enable	RW	0
1	EN_S3BT	EN_S3BT enable bit 0:disable 1:enable	RW	0
0	EN_S1	EN_S1 enable bit 0:disable 1:enable	RW	1

7.4.18 TIMER_CTL

System timer set Register (RTCVDD) Default: 0x200000

Offset = 0x48

Bit (s)	Name	Description	Access	Reset
31:22	-	Reserved	-	-
21	S3_TIMER_EN	S3timer_EN bit 0:Disable 1:Enable	RW	1
20	S3TIMER	S3timer 0: 300ms 1: 1s	RW	0
19:16	-	Reserved	-	-
15	S3BT_ON_EN	S3BT ON timer Enable bit 0:Disable 1:Enable	RW	0
14:8	S3BT_ON_TIMER	S3BT power on by alarm timer 7 bits corresponds to 0~127 mins	RW	0
7:0	-	Reserved	-	-

7.4.19 WKEN_CTL

WAKE up source enable Register (RTCVDD) Default: 0x6FB

Offset = 0x4C

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10	BATWK_EN	Battery insert wakeup enable bit 0: disable 1: enable	RW	1
9	REMOTE_WKEN	Drive-by-wire wakeup enable bit 0: disable 1: enable	RW	1
8	HDSW_BLOCK	Toggle switch shields long/short press on play key to wakeup enable release bit 0: Toggle switch turn to OFF will shield long/shot press on the play key to wake up 1: Toggle switch do not shield long/short press on the play key to wake up	RW	0
7	HDSWOFF_EN	Under S3BT state, toggle switch ON/OFF enable 0:disable 1:enable	RW	1
5	BT_WK_EN	Bluetooth wakeup enable 0:Disable 1:Enable	RW	1
4	NFC_WK_EN	NFC wakeup enable 0:Disable 1: enable	RW	1
3	RESET_WKEN	RESET wakeup enable 0:disable 1:enable	RW	1
2	SHORT_WKEN	On off short press wakeup enable 0:disable	RW	0

		1:enable		
1	LONG_WKEN	On off long press wakeup enable 0:disable 1:enable	RW	1
0	HDSW_WKEN	HDSW toggle switch wakeup enable 0:disable 1:enable	RW	1

Note: needs to update code before writing this register.

7.4.20 WAKE_PD

WAKE up source enable Register (RTCVDD) Default: 0x0

Offset = 0x50

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8	BATIN_PD	Battery insert wakeup pending bit 0: no battery insert wakeup 1: battery insert wakeup happened	RW	0
7	REMOTE_PD	Drive-by-wire wakeup pending bit 0: no Drive-by-wire wakeup 1: Drive-by-wire happened	RW	0
6	LONG_PLAY	Long press on play key pending bit 0: no long press on play key 1: long press on play key happened	RW	0
5	S3BT_TON_PD	S3BT_ON timer wakeup indication pending bit 0: no S3BT_ON_TIMER wakeup 1: S3BT_ON_TIMER wakeup	RW	0
4	HDSWOFF_PD	Toggle switch OFF pending bit 0: no toggle switch operation 1: toggle switch OFF operation	RW	0
3	HDSWON_PD	Toggle switch ON pending bit 0: no toggle switch operation 1: toggle switch ON operation	RW	0
2	ONOFF_PD	ONOFF wakeup pending bit 0: no ONOFF wakeup happened 1: ONOFF wakeup happened	RW	0
1	NFC_PD	NFC Pending 0: Interrupt source is not active. 1: Interrupt source is active. Write 1 to this bit to clear this pending bit. This bit must be cleared by software before trigger a new interrupt pending.	RW	0
0	BT_PD	Bluetooth Pending 0: Interrupt source is not active. 1: Interrupt source is active. Write 1 to this bit to clear this pending bit. This bit must be cleared by software before trigger a new interrupt pending.	RW	0

7.4.21 ONOFF_KEY

ONOFF key control & detect register (RTCVDD) Default: 0x80D8

Offset = 0x54

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10	RESTART_SET	RESET key function setting 0: reset VDD region registers 1: restart	RW	0
9:7	ONOFF_PRESS_TIME	ONOFF key press time setting: 000: 50ms < t < 0.125s, recognized as short press; t >=0.125s, recognized as long press; 001: 50ms < t < 0.25s, recognized as short press; t >=0.25s, recognized as long press; 010: 50ms < t < 0.5s, recognized as short press; t >=0.5s, recognized as long press; 011: 50ms < t < 1s, recognized as short press; t >=1s, recognized as long press; 100: 50ms < t < 1.5s, recognized as short press; t >=2s, recognized as long press; 101: 50ms < t < 2s, recognized as short press; t >=2s, recognized as long press; 110: 50ms < t < 3s, recognized as short press; t >=3s, recognized as long press; 111: 50ms < t < 4s, recognized as short press; t >=4s, recognized as long press;	RW	1
6	ONOFF_RST_EN	ONOFF long press reset function enable 0:disable 1:enable	RW	1
5:4	ONOFF_RST_T_SEL	ONOFF long press send Reset time selection 00:6s 01:8s 10:10s 11:12s	RW	1
2	HDSWOFF_2_3	ONOFF level 0: not on this level 1: on 2⁄3 level (digital realization)	R	0
1	HDSWON_1_3	ONOFF level 0: not this level 1: at 1⁄3 level (digital realization)	R	0
0	ONOFF_PRESS_0	ONOFF key whether pressed down 0:ONOFF not pressed 1:ONOFF is pressed (digital realization)	R	0

7.4.22 NFC_CTL

NFC field detect control Register (RTCVDD) Default: 0x1C

Offset = 0x5C

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8	BT_WAKE_DET	BT_WAKE_HOST signal level flag: 0: signal is low 1: signal is high	R	0
7	NFC_DET	NFC_FD level flag	R	X

6	NFCPU_CTL	Pull up resistor selection: 0: disable 1: 50K	RW	0
5:1	-	Reserved	-	-
0	NFCTM_SET	Trigger mode set: 0: when higher than 2/3RTCVDD, trigger interrupt sending and wakeup 1: when lower than 2/3RTCVDD, trigger interrupt sending and wakeup	RW	0

7.4.23 SPD_CTL

Standby power pull down control (RTCVDD) Default: 0x13D

Offset: 0x64

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8:7	DC5V_SYS_VOL	Adjusting DC5V generated SYSPOWER voltage 00: 3.3V 01: 4.2V 10: 4.3V 11: 4.4V	RW	0x2

8 System Control

8.1 RMU

8.1.1 Features

The RMU Controller of ATS2825 has following features:

- The RMU (Reset Management Unit) can reset all the peripherals.
- The MCU can enter power-saving mode by setting the registers of RMU .

8.1.2 Register List (Digital part)

Table 8-1 RMU digital part base address

Name	Physical Base Address	KSEG1 Base Address
RMU_DIGITAL	0xC0000000	0xC0000000

Table 8-2 RMU digital part register list

Offset	Register Name	Description
0x00000000	MRCR	Module Reset Control Register

8.1.3 Register Description

8.1.3.1 MRCR

MRCR (Module Reset Control Register, offset = 0x00000000)

Bit (s)	Name	Description	Access	Reset
31:18	-	Reserved	-	-
17	UART1RESET	UART1 Controller & IR Reset 0: reset 1: normal	RW	0
16	USBRESET2	This bit should be reset before USB Reset bit is reset. 0: reset 1: normal	RW	0
15	-	Reserved	-	-
14	SEGLCDRESET	SEGLCD & SEGLED Controller Reset 0: reset 1: normal	RW	0
13	TOUCHKEYRESET	Touch Key Controller Reset 0: reset 1: normal	RW	0
12	PWM_LIGHT_RESET	PWM back light Reset 0: reset 1: normal	RW	0
11	AUDIOIORESET	DAC & ADC & IIS & SPDIF Reset 0: reset 1: normal	RW	0
10	SPI1RESET	SPI Controller 1 Reset	RW	0

		0: reset 1: normal		
9	USBRESET	USB Reset 0: reset 1: normal	RW	0
8	-	Reserved	-	-
7	LCDRESET	LCD controller Reset 0: reset 1: normal	RW	0
6	SPI0RESET	SPI Controller 0 Reset 0: reset 1: normal	RW	0
5	TWIRESET	TWI Controller Reset 0: reset 1: normal	RW	0
4	UART0RESET	UART0 & H5 Controller Reset 0: reset 1: normal	RW	0
3	SDRESET	SD/MMC Card Controller Reset 0: reset 1: normal	RW	0
2	DSP_PART	All but OCEM DSP reset 0: reset DSP except OCEM 1: normal *Note: Debug use only, do not set to 0.*	RW	1
1	DSP_ALL	All DSP reset 0: reset all DSP 1: depends on DSP_PART	RW	0
0	DMA012345RESET	DMA012345 Reset 0: reset 1: normal The reset bit of DMA012345 controller is active while it is driven by MCU clock.	RW	0

*Note: * The reset signal of SPI BOOT controller and interrupt controller is connected to the wire of CPU reset. It can be reset while the power on reset, watch dog reset or the reset pin of CPU is set low.*
** RTC, LRADC, timer0/1 have no reset control in this register.*

8.2 CMU Analog

8.2.1 Features

- Support only one oscillator inputs: 26MHz
- Supply 3 PLLs and special clocks of all modules. The 3 PLLs is PLL_24M, CORE PLL, Audio PLL
- CORE PLL can select from two clock source: CK_24M and HOSC

8.2.2 Register List

Table 8-3 CMU Analog Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
CMU_ANALOG_REGISTER	0xC0000100	0xC0000100

Table 8-4 CMU Analog Controller Registers

Offset	Register Name	Description
0x00	HOSC_CTL	HOSC control register
0x08	_24MPLL_CTL	24M PLL Control Register
0x0C	CORE_PLL_CTL	CORE_PLL Control Register

8.2.3 Register Description

8.2.3.1 HOSC_CTL

HOSC control register.
Offset = 0x00 (RTCVDD domain)

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:13	HOSCI_BC_SEL	HOSCI PAD base capacitor select: 000: 0p 001: 3p 010: 6p 011: 9p 100: 6p 101: 9p 110: 12p 111: 15p	RW	101
12:8	HOSCI_TC_SEL	HOSCI PAD trim cap select, range from 0pF to 3.1pF Trim cap = 0.1pF * HOSCI_TC_SEL	RW	0x00
7:5	HOSCO_BC_SEL	HOSCO PAD base capacitor select: 000: 0p 001: 3p 010: 6p 011: 9p 100: 6p 101: 9p 110: 12p 111: 15p	RW	101
4:0	HOSCO_TC_SEL	HOSCO PAD trim cap select, range from 0pF to 3.1pF Trim cap = 0.1pF * HOSCO_TC_SEL	RW	0x00

8.2.3.2 _24MPLL_CTL

24MPLL Control Register
Offset = 0x08 (VDD domain)

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3	HOSC_EN	HOSC enable: 0: disable 1: enable	RW	1
2:1	-	Reserved	-	-

0	24MPLL_EN	24MPLL Enable: 0: disable 1: enable	RW	0

8.2.3.3 CORE_PLL_CTL

CORE_PLL Control Register
Offset = 0x0C (VDD domain)

Bit (s)	Name	Description	Access	Reset
31:9	-	Reserved	-	-
8	CORE_PLL_SCLK_SEL	CORE PLL source clock select: 0: HOSC_26M 1: CK_24M	RW	0
7	CORE_PLL_EN	CORE PLL Enable: 0: Disable 1: Enable	RW	0
6:0	SCORE	CORE PLL Frequency Select: When core PLL source clock select HOSC_26M, Formula: 6.5M* SCORE Range:39 ~ 409.5M Value must be bigger than 6 0-5: reserved 6: 6*6.5M=39M …… 63: 63*6.5M=409.5M Others reserved. When core PLL source clock select CK_24M, Formula: 6M* SCORE Range:36 ~ 378M Value must be bigger than 6 0-5: reserved 6: 6*6M=36M …… 63: 63*6M=378M Others reserved.	RW	0x06

;

8.3 RTC

This part have individual modules: Calendar, 2Hz, Watch Dog (WD) and Timer0/1.

8.3.1 Features

- Built-in a 32k oscillator
- Calendar with a alarm IRQ which can wake up the PMU
- 2Hz IRQ
- Two Timers with IRQ
- A watch dog which can be configured as IRQ or Reset

8.3.2 Register List

Table 8-5 RTC block base address

Name	Physical Base Address	KSEG1 Base Address
RTC	0xC0120000	0xC0120000

Table 8-6 RTC Controller Registers

Offset	Register Name	Description
0x00	RTC_CTL	RTC Control Register
0x04	RTC_REGUPDATA	RTC Register update Register
0x08	RTC_DHMSALM	RTC Day Hour Minute and Second Alarm Register
0x0C	RTC_DHMS	RTC Day Hour Minute and Second Register
0x10	RTC_YMD	RTC Year Month Date Register
0x14	RTC_ACCESS	RTC freely access Register
0x18	Hz2_CTL	2Hz Control Register
0x1c	WD_CTL	Watch Dog Control register
0x20	T0_CTL	Timer0 Control register
0x24	T0_VAL	Timer0 Value
0x28	T1_CTL	Timer1 Control register
0x2C	T1_VAL	Timer1 Value
0X30	RTC_BAK0	Backup Register
0X34	RTC_BAK1	Backup Register
0X38	RTC_BAK2	Backup Register
0X3C	RTC_BAK3	Backup Register

Note:
The following Register marked by RTCVDD, means "The register's power is supplied by RTCVDD. And the register is reset by RTCVDD_OK."
And that marked by VDD, means "The register's power is supplied by VDD. And the register is reset by VDD_RST."

8.3.3 Register Description

8.3.3.1 RTC_CTL

Calendar Control Register
Offset=0x0000 (RTCVDD) (Default value 0x80)

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	LEAP	RTC Leap Year bit 1: leap year 0: not leap year	R	1
6:5	-	Reserved	-	-
4	CAL_EN	Calendar Enable 1: Enable 0: Disable	RW	0
3:2	-	Reserved	-	-
1	ALIE	Alarm IRQ Enable 1: Enable 0: Disable	RW	0
0	ALIP	Alarm IRQ Pending bit, writing 1 to this bit will clear it	RW	0

NOTE:
The CAL_EN bit must be disabled when The RTC_DHMS / RTC_YMD register being written. And RTC_DHMS / RTC_YMD register must be written before CAL_EN is enabled when set the time or error will occur.

8.3.3.2 RTC_REGUPDATA

Offset=0x0004 (RTCVDD)

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	UPDATA	The RTCVDD register update control Register. When writing the RTC registers (except RTCREGUPDATE register or bit “ALIP”), the RTC registers’ values are not update immediately. The value is written to backup registers (in VDD) first. Just when writing RTCREGUPDATE register “A596H”, the RTCVDD registers’ values are update with the backup registers’ value. RTCREGUPDATE register is automatically reset as “5A69H” after the RTCVDD register is update. NOTE: Do not write RTCVDD registers when this register value is “A5C3E283H” NOTE: When writing the bit “ALM_IP”, it will take effect immediately. Do not need writing this register.	RW	0x5A69H

8.3.3.3 RTC_DHMSALM

Offset=0x0008 (RTCVDD)

Bits	Name	Description	Access	Reset
31:21	-	Reserved	-	-
20:16	HOUEAL	Alarm hour setting 0x00 – 0x17	RW	0
15:14	-	Reserved	-	-
13:8	MINAL	Alarm minute setting 0x00 – 0x3B	RW	0
7:6	-	Reserved	-	-
5:0	SECAL	Alarm second setting 0x00 – 0x3B	RW	0

8.3.3.4 RTC_DHMS

Offset=0x000C (RTCVDD)

Bits	Name	Description	Access	Reset
31:21	-	Reserved	-	-
20:16	HOUR	Time hour setting 0x00 – 0x17	RW	0
15:14	-	Reserved	-	-
13:8	MIN	Time minute setting 0x00 – 0x3B	RW	0
7:6	-	Reserved	-	-
5:0	SEC	Time second setting 0x00 – 0x3B	RW	0

8.3.3.5 RTC_YMD

Offset=0x0010 (RTCVDD)

Bits	Name	Description	Access	Reset
31:23	-	Reserved	-	-
22:16	YEAR	Time year setting 0x00 – 0x63	RW	00
15:12	-	Reserved	-	-
11:8	MON	Time month setting 0x01 – 0x0C	RW	01
7:5	-	Reserved	-	-
4:0	DATE	Time day setting 0x01 – 0x1F	RW	01

8.3.3.6 RTC_ACCESS

Offset=0x0014 (RTCVDD)

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	ACCESS	These bits can be accessed by CPU freely.	RW	0

8.3.3.7 HZ2_CTL

Offset=0x0018 (VDD)

Bits	Name	Description	Access	Reset
31:2	-	Reserved	-	-
1	2HIE	2Hz IRQ Enable 1: Enable 0: Disable	RW	0
0	2HIP	2Hz IPQ pending bit, writing 1 to this bit will clear it	RW	0

8.3.3.8 WD_CTL

Offset=0x001C (VDD)

Bits	Name	Description	Access	Reset
37	-	Reserved	-	-
6	IRQP	Watch dog IRQ pending bit, writing 1 to this bit will clear it	RW	0
5	SIGS	Watchdog Signal (IRQ or Reset-) Select.0: Reset, 1: IRQ-. 0: Send Reset signal when watchdog overflow. 1: Send IRQ signal when watchdog overflow.	RW	0
4	WDEN	Watch Dog timer enable, when WD timer is enabled and the WD timer overflows, an internal reset (WDRST-) is generated to force the system into reset status and then reboot. 1: Enable 0: Disable	RW	0
3:1	CLKSEL	Watch Dog timer Clock Select, WDCKS Clock Selected Watch Dog Length The watch dog's overflow value is 180. 000 1kHz 176 ms 001 512Hz 352 ms 010 256Hz 703ms 011 128Hz 1.4 s 100 64Hz 2.8s 101 32Hz 5.6 s 110 16Hz 11.2s	RW	0

		111 Reserved		
0	CLR	Clear bit, write 1 to clear WD timer, cleared automatically	RW	0

8.3.3.9 T0_CTL

Offset=0x0020 (VDD)

Bits	Name	Description	Access	Reset
31:6	-	Reserved	-	-
5	EN	Timer 0 Enable 0:Disable,1:Enable	RW	0
4:3	-	Reserved	-	-
2	RELO	Timer 0 Reload. 0:Not reload,1:Reload	RW	0
1	ZIEN	T0 Zero IRQ Enable When this bit is enabled, Timer0_Zero_IRQ sent out the IRQ signal until the pending bit was cleared.	RW	0
0	ZIPD	Timer0 IRQ Pending, Writing 1 to clear this bit.	RW	0

Note: The timer only can count down

8.3.3.10 T0_VAL

Offset=0x0024 (VDD)

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:0	T0	Read or write current Timer0 value	RW	-

8.3.3.11 T1_CTL

Offset=0x0028 (VDD)

Bits	Name	Description	Access	Reset
31:6	-	Reserved	-	-
5	En	Timer0 Enable 0:Disable,1:Enable	RW	0
4:3	-	Reserved	-	-
2	RELO	Timer1 Reload 0:Not reload,1:Reload	RW	0
1	ZIEN	Timer1 Zero IRQ Enable When this bit is enabled, Timer1_Zero_IRQ sent out the IRQ signal until the pending bit was cleared.	RW	0
0	ZIPD	Timer1 IRQ Pending, Writing 1 to clear this bit.	RW	0

Note: The timer only can count down.

8.3.3.12 T1_VAL

Offset=0x002C (VDD)

Bits	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:0	T1	Read or write current Timer1 value	RW	0

8.4 Exceptions and Interrupts Controller (INTC)

8.4.1 Features

The ATS2825 use MIPS processor. The ATS2825 also adds additional controller to manage up to 32 interrupt sources.

Table below shows all interrupt sources.

Table 8-7 Interrupt sources

Interrupt Number	Sources	Type
0	BT	High Level
1	NFC	High Level
2	2Hz/WatchDog	High Level
3	TIMER1	High Level
4	TIMER0	High Level
5	RTC	High Level
6	UART0	High Level
7	SIRQ0	High Level
8	Touch Key	High Level
9	SPI0	High Level
10	USB	High Level
11	TWI	High Level
12	UART1	High Level
13	SIRQ1	High Level
14	DAC OR IIS TX	High Level
15	ADC OR IIS RX	High Level
16	Reserved	-
17	SD/MMC	High Level
18	DMA0	High Level
19	DMA1	High Level
20	DMA2	High Level
21	DMA3	High Level
22	DMA4	High Level
23	DMA5	High Level
24	Reserved	-
25	Reserved	-
26	SPI1	High Level
27	OUT_USER0	High Level
28	OUT_USER1	High Level
29	OUT_USER2	High Level
30	OUT_USER3	High Level
31	OUT_USER4	High Level

8.4.2 Register List

The ATS2825 implements a controller to handle 32 interrupt request, the registers are listed below:

Table 8-8 Interrupt Controller base address

Name	Physical Base Address	KSEG1 Base Address

InterruptController	0xC00B0000	0xC00B0000

Table 8-9 Interrupt Controller Registers

Offset	Register Name	Description
0x00000000	INTC_PD	Interrupt Pending register
0x00000004	INTC_MSK	Interrupt Mask register
0x00000014	INTC_EXTCTL	External interrupt control register
0x00000018	INTC_EXTIP	External interrupt status register
0x0000001C	REQ_INT_OUT	Request interrupt output register
0x00000020	REQ_IN	Request input register
0x00000024	REQ_IN_PD	Request input pending register
0x00000028	REQ_OUT	Request output register

8.4.3 Register Description

8.4.3.1 INTC_PD

INTC_PD (Interrupt Pending Register, offset = 0x00000000)

Bit (s)	Name	Description	Access	Reset
31	OUT_USER4_IP	OUT_USER4 interrupt pending bit	R	0
30	OUT_USER3_IP	OUT_USER3 interrupt pending bit	R	0
29	OUT_USER2_IP	OUT_USER2 interrupt pending bit	R	0
28	OUT_USER1_IP	OUT_USER1 interrupt pending bit	R	0
27	OUT_USER0_IP	OUT_USER0 interrupt pending bit	R	0
26	SPI1_IP	SPI1 interrupt pending bit	R	0
25:24	-	Reserved	-	-
23	DMA5_IP	DMA5 controller interrupt pending bit	R	0
22	DMA4_IP	DMA4 controller interrupt pending bit	R	0
21	DMA3_IP	DMA3 controller interrupt pending bit	R	0
20	DMA2_IP	DMA2 controller interrupt pending bit	R	0
19	DMA1_IP	DMA1 controller interrupt pending bit	R	0
18	DMA0_IP	DMA0 controller interrupt pending bit	R	0
17	SD_IP	SD/MMC interrupt pending bit	R	0
16	-	Reserved	-	-
15	ADC_IIS_RX_IP	ADC or IIS-RX interrupt pending bit	R	0
14	DAC_IIS_TX_IP	DAC or IIS-TX interrupt pending bit	R	0
13	SIRQ1_IP	SIRQ1 interrupt pending bit	R	0
12	UART1_IP	UART1 interrupt pending bit	R	0
11	TWI_IP	TWI interrupt pending bit	R	0
10	USB_IP	USB interrupt pending bit	R	0
9	SPI0_IP	SPI0 interrupt pending bit	R	0
8	TouchKey_IP	Touch Key interrupt pending bit	R	0
7	SIRQ0_IP	SIRQ0 interrupt pending bit	R	0
6	UART0_IP	UART0 interrupt pending bit	R	0
5	RTC_IP	RTC interrupt pending bit	R	0
4	TIMER0_IP	TIMER0 interrupt pending bit	R	0
3	TIMER1_IP	TIMER1 interrupt pending bit	R	0
2	2Hz_IP	2Hz/WatchDog interrupt pending bit	R	0
1	NFC_IP	NFC pending	R	0

0	BT_IP	BT pending	R	0

Note:

(1) Interrupt Pending bits cannot be cleared by writing 1. These bits are automatically cleared only by clear all the corresponding interrupt pending bits of the device register, otherwise unchanged.

(2) 0: no interrupt request; 1: interrupt request detected

8.4.3.2 INTC_MSK

INTC_MSK (Interrupt Mask Register, offset = 0x00000004)

Bit (s)	Name	Description	Access	Reset
31	OUT_USER4_IM	OUT_USER4 interrupt enable bit	RW	0
30	OUT_USER3_IM	OUT_USER3 interrupt mask bit	RW	0
29	OUT_USER2_IM	OUT_USER2 interrupt mask bit	RW	0
28	OUT_USER1_IM	OUT_USER1 interrupt mask bit	RW	0
27	OUT_USER0_IM	OUT_USER0 interrupt mask bit	RW	0
26	SPI1_IM	SPI1 interrupt mask bit	RW	0
25:24	-	Reserved	-	-
23	DMA5_IM	DMA5 controller interrupt mask bit	RW	0
22	DMA4_IM	DMA4 controller interrupt mask bit	RW	0
21	DMA3_IM	DMA3 controller interrupt mask bit	RW	0
20	DMA2_IM	DMA2 controller interrupt mask bit	RW	0
19	DMA1_IM	DMA1 controller interrupt mask bit	RW	0
18	DMA0_IM	DMA0 controller interrupt mask bit	RW	0
17	SD_IM	SD/MMC interrupt mask bit	RW	0
16	-	Reserved	-	-
15	ADC_IIS_RX_IM	ADC or IIS-RX interrupt mask bit	RW	0
14	DAC_IIS_TX_IM	DAC or IIS-TX interrupt mask bit	RW	0
13	SIRQ1_IM	SIRQ1 interrupt mask bit	RW	0
12	UART1_IM	UART1 interrupt mask bit	RW	0
11	TWI_IM	TWI interrupt mask bit	RW	0
10	USB_IM	USB interrupt mask bit	RW	0
9	SPI0_IM	SPI0 interrupt mask bit	RW	0
8	TOUCHKEY_IM	Touch Key interrupt mask bit	RW	0
7	SIRQ0_IM	SIRQ0 interrupt mask bit	RW	0
6	UART0_IM	UART0 interrupt mask bit	RW	0
5	RTC_IM	RTC interrupt mask bit	RW	0
4	TIMER0_IM	TIMER0 interrupt mask bit	RW	0
3	TIMER1_IM	TIMER1 interrupt mask bit	RW	0
2	2HZ_IM	2Hz/WatchDog interrupt mask bit	RW	0
1	NFC_IM	NFC interrupt mask bit	RW	0
0	BT_IM	BT interrupt mask bit	RW	0

Note: 0: Interrupt is masked. 1: Interrupt is unmasked.

8.4.3.3 INTC_EXTCTL

INTC_EXTCTL (External Interrupt Control register, offset = 0x00000014)

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3	EXTYPE1	External Interrupt 1 Type 0: Rising edge-triggered; 1: Falling edge-triggered.	RW	0

2	-	Reserved	-	-
1	EXTYPE0	External Interrupt 0 Type 0: Rising edge-triggered; 1: Falling edge-triggered.	RW	0
2	-	Reserved	-	-

8.4.3.4 INTC_EXTIP

INTC_IP (External Interrupt Pending register, offset = 0x00000018)

Bit (s)	Name	Description	Access	Reset
31:2	-	Reserved	-	-
1	E1PD	External Interrupt 1 Pending 0: External interrupt source 1 is not active. 1: External interrupt source 1 is active. Write 1 to will clear this bit. This bit must be cleared by software before trigger a new interrupt pending.	RW	0
0	E0PD	External Interrupt 0 Pending 0: External interrupt source 0 is not active. 1: External interrupt source 0 is active. Write 1 to will clear this bit. This bit must be cleared by software before trigger a new interrupt pending.	RW	0

8.4.3.5 REQ_INT_OUT

REQ_INT_OUT (Request interrupt output register, offset = 0x0000001C)

Bit (s)	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	DSP_INT3	Send interrupt request to DSP.	RW	0

8.4.3.6 REQ_IN

REQ_IN (Request input register, offset = 0x00000020)

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	-	-
4	OUT_USER4	It is a CPU interrupt controller sampled value of OUT_USER4 signal.	R	0
3	OUT_USER3	It is a CPU interrupt controller sampled value of OUT_USER3 signal.	R	0
2	OUT_USER2	It is a CPU interrupt controller sampled value of OUT_USER2 signal.	R	0
1	OUT_USER1	It is a CPU interrupt controller sampled value of OUT_USER1 signal.	R	0
0	OUT_USER0	It is a CPU interrupt controller sampled value of OUT_USER0 signal.	R	0

8.4.3.7 REQ_IN_PD

REQ_IN_PD (Request input pending register, offset = 0x00000024)

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	-	-
4	OUT_USER4_PD	0: interrupt pending is not detected.	RW	0

		1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER4 signal. Writing '1' can clear this bit.		
3	OUT_USER3_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER3 signal. Writing '1' can clear this bit.	RW	0
2	OUT_USER2_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER2 signal. Writing '1' can clear this bit.	RW	0
1	OUT_USER1_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER1 signal. Writing '1' can clear this bit.	RW	0
0	OUT_USER0_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER0 signal. Writing '1' can clear this bit.	RW	0

8.4.3.8 REQ_OUT

REQ_OUT (Request output register, offset = 0x00000028)

Bit (s)	Name	Description	Access	Reset
31:2	-	Reserved	-	-
1	IN_USER1	Send information to DSP.	RW	0
0	IN_USER0	Send information DSP.	RW	0

9 Storage

SD/MMC Card Controller Features

- Fully compliant with MMC Specification 4.3
- Fully compliant with SD card Specification 2.0
- Integrated Clock Delay Chain Technique to Regulate Card Interface Timing: Latching Delay Chain for input Signal, Output Delay Chain for output signal.
- Integrated Watchdog timeout Counter to report Exception happening.
- Integrated Pull up resistance (value 51Komh) for Data and CMD Line.
- Integrated CRC calculate and check circuit.
- Send continuous clock to support SDIO card.
- Support 3.1V CLK PAD voltage.
- Support 3.1V CMD PAD voltage.
- Support 3.1V DAT PAD voltage.
- Band Width: 25MByte/S
- Maximal SD interface Clock: 50MHz

10 Transfer and Communication

10.1 USB

10.1.1 Features

- Complies with the USB2.0 Specification Revision 1.0a.
- UTMI+ level2 Transceiver Macrocell Interface.
- Supports point-to-point communication with one full-speed or high-speed device in Host mode (no HUB support).
- Supports full-speed or high-speed in peripheral mode.
- Supports 3 IN endpoint and 3 OUT endpoint except endpoint0.
- Supports bulk Isochronous and Interrupt transfer.
- Partially configurable endpoint endpoint type and single, double triple or quad buffering.
- Integrated synchronous RAM as endpoint FIFOs.
- Supports suspend, resume and power managements function.
- Support remote wakeup.

10.1.2 Register List

Table 10-1 USB Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
USB_CONTROLLER_REGISTERS	0xC0080000	0xC0080000

Table 10-2 USB Controller Registers

Offset	Register Name	Description
0x419	LINESTATUS	Line status register
0x41A	DPDMCTRL	DPDM control register

10.1.3 Register Description

10.1.3.1 LINESTATUS

Line status register
Offset = 0x419

Bit (s)	Name	Description	Access	Reset
7:5	-	Reserved	-	-
4:3	USB_LS	USB linestate[1:0] Linestate0:DP Linestase1:DM	R	00
2:0	-	Reserved	-	-

10.1.3.2 DPDMCTRL

DP DM control register
Offset = 0x41A

Bit (s)	Name	Description	Access	Reset
7	-	Reserved	-	-

6	PLUGIN	This bit Indicated the USB connection status when Linedeten is enabled. 1: connect 0: disconnect	R	x
5	-	Reserved	-	-
4	LINEDETEN	Line status detect enable 1: enable 0: disable	RW	1
3	DMPUEN	500Kohm DM pull up resistor enable. 1: enable 0: disable	RW	1
2	DPPUEN	500Kohm DP pull up resistor enable. 1: enable 0: disable	RW	1
1	DMPDDIS	DM pull down disable. 1: disable 0: enable	RW	1
0	DPPDDIS	DP pull down disable. 1: disable 0: enable	RW	1

10.2 TWI

10.2.1 Features

- Both master and slave functions supported
- Support standard mode (100kbps) and fast-speed mode (400kpbs),
- Multi-master, Hi-speed mode and 10bit address mode not supported
- Internal Pull-Up Resistor (10kOhm) optional

10.2.2 Function Description

Two wire interfaces (TWI) bus is used to communicate across circuit-board distances. At the low end of the spectrum of communication options for "inside the box" communication is TWI.
TWI provides support for communication with various slow, on-board peripheral devices that are accessed intermittently, while being extremely modest in its hardware resource needs. It is a simple, low-bandwidth, short-distance protocol. Most available TWI devices operate at speeds up to 400Kbit/s, with some venturing up into the low megahertz range. TWI is easy to use to link multiple devices together since it has a built-in addressing scheme.

Note:

1. *The TWI module is Slave mode when in IDLE status.*
2. *Generate the IRQ while the bus status changes.*
   - *A byte transfer complete, include transmit and receive data or address*
   - *A stop bit detected*

   If the address received don't match the content of TWI_ADDR, indicate the address is not matched, don't generate the IRQ and reset to IDLE when detect the start bit followed the slave address in slave mode.
3. *Release the bus by software after receiving data or address.*

10.2.3 Operation Manual

Master mode:

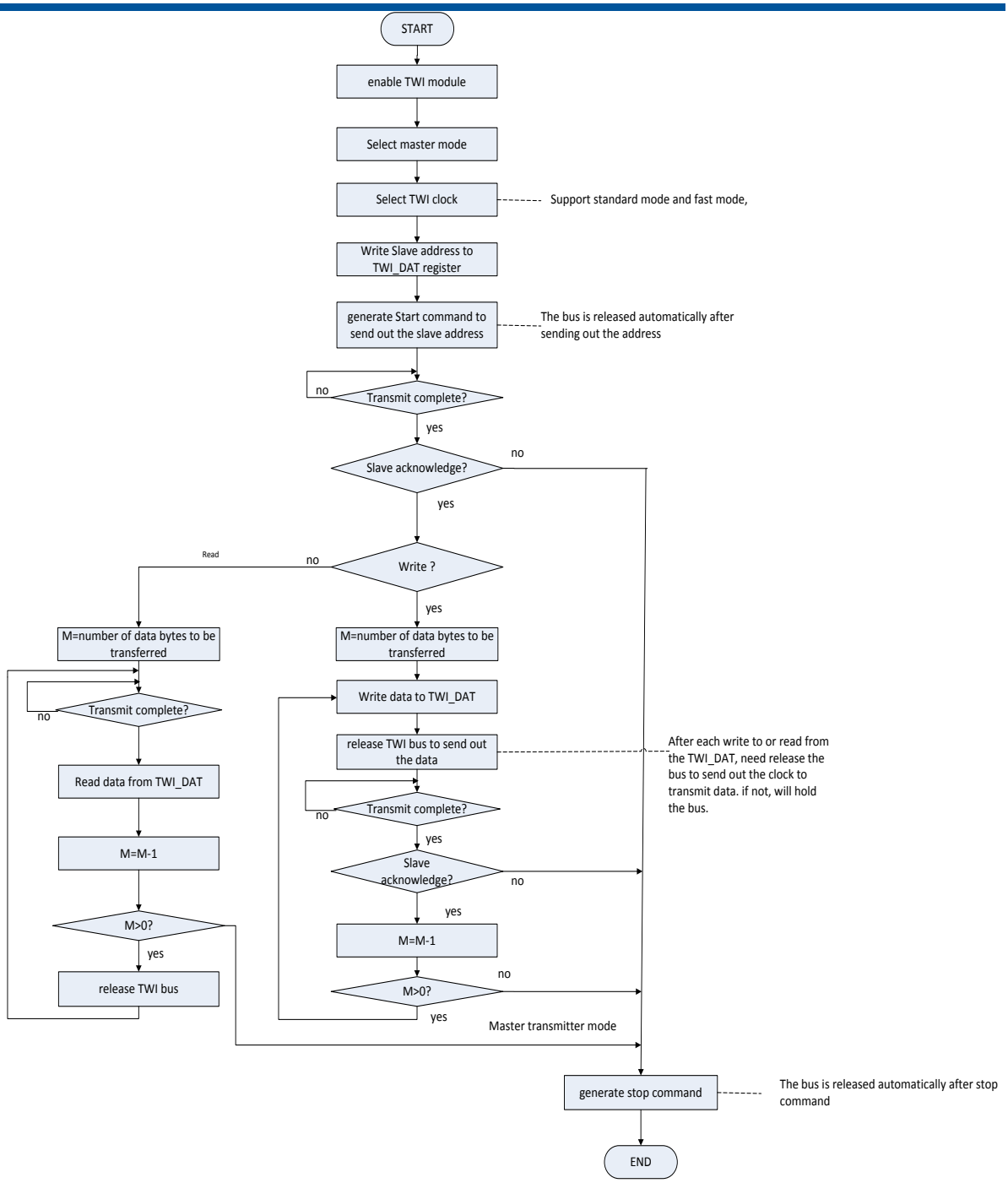


Figure 10-1 TWI Master Mode Operation Flow

Slave mode:

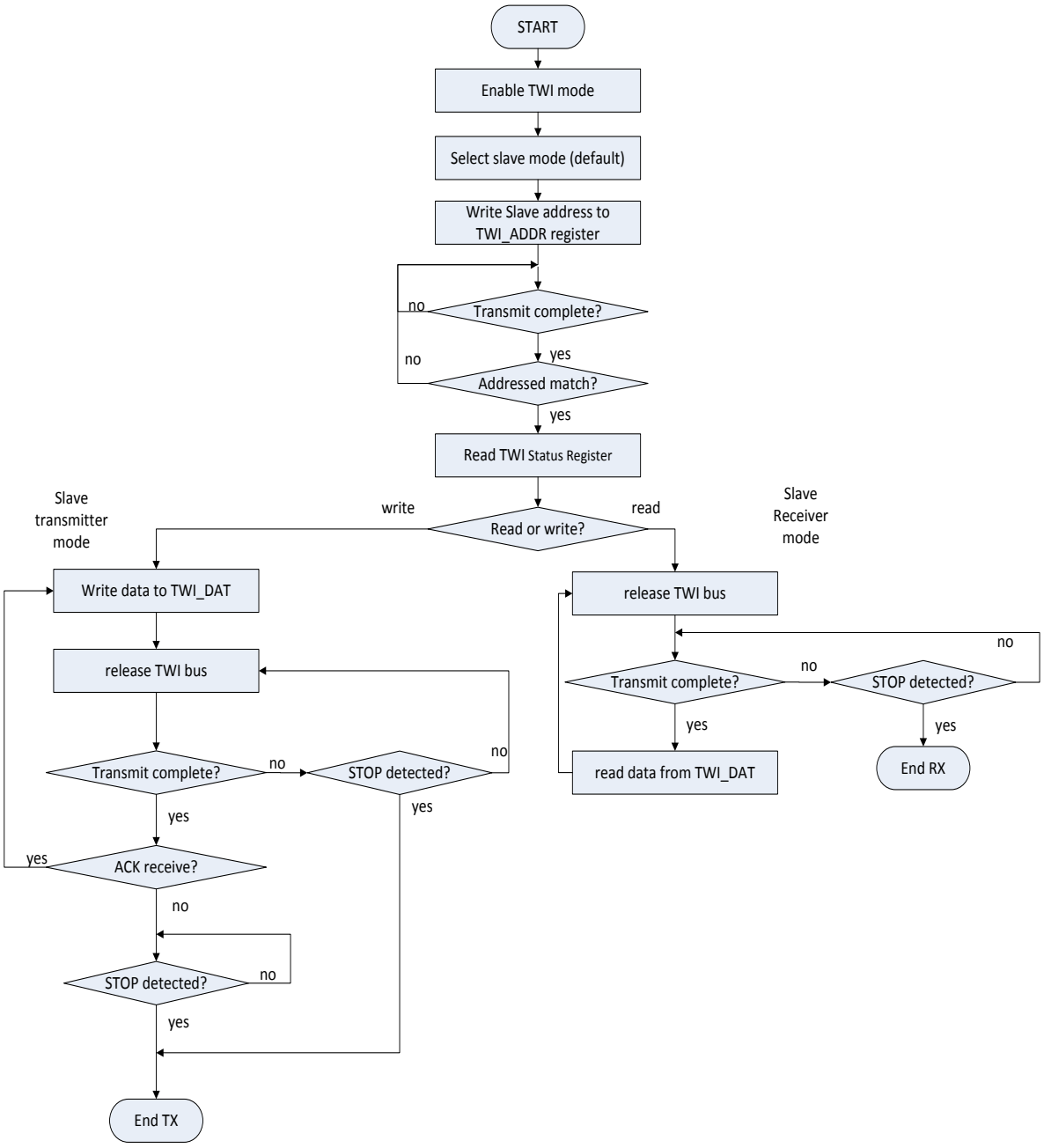


Figure 10-2 TWI Slave mode operation flow

10.2.4 Register List

Table 10-3 TWI Register Block Base Address

Name	Physical Base Address	KSEG1 Base Address
TWI	0xC0130000	0xC0130000

Table 10-4 TWI Registers Offset Address

Offset	Register Name	Description
0x0000	TWI_CTL	TWI Control Register
0x0004	TWI_STAT	TWI Status Register
0x0008	TWI_ADDR	TWI Address Register

0x000c	TWI_DAT	TWI Data Register

10.2.5 Register Description

10.2.5.1 TWI_CTL

TWI Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	EN	Enable. When enable, reset the status machine to IDLE 0: Disable 1: Enable	RW	0
6	MS	Mode Select. 0: Slave mode 1: Master mode	RW	0
5	CLKSEL	TWI clock select, only used for master mode 0: standard speed (100kbps) 1: fast speed (400kbps)	RW	0
4	IRQE	IRQ Enable. When the TWI status changes, generate IRQ.TWI can detect four status: complete a byte transfer, stop. 0: Disable 1: Enable	RW	0
3:2	GBCC	Generating Bus Control Condition (only for master mode). 00: No effect 01: Generating START condition 10: Generating STOP condition 11: Generating Repeated START condition Write the slave address to the TWI_DAT register, select start or restart, and then the start or restart command follow by the slave address will occur on the bus. These commands should be used with release bus.	RW	0
1	RB	Release Bus. Write 1 to this bit will release the bus. MCU should write 1 to this bit after transmitting or receiving the last bit of a whole transfer.	RW	0
0	GACK	Generating Acknowledge signal. In receive mode: 0: Generating the ACK signal to the transmitter at 9th clock of SCL 1: generate the NACK signal at 9th clock of SCL	RW	0

10.2.5.2 TWI_STAT

TWI Status Register
Offset=0x0004

Bits	Name	Description	Access	Reset
31: 9	-	Reserved	-	-
8	TCB	Transfer Complete Bit 0: not finish transfer 1: A byte transfer finish, include transfer the ACK or NACK bit	RW	0

		Write “1” to clear this bit		
7	STPD	Stop Detect bit The bit is clear when the TWI module is disable or when the START condition is detected. Writing 1 to the bit will clear it. 0: Stop bit is not detected 1: Stop bit is detected	RW	0
6	STAD	Start Detect bit, include restart. The bit is clear when the TWI module is disable or when the STOP condition is detected. Writing 1 to the bit will clear it. 0: Start bit is not detected 1: Start bit is detected	RW	0
5	RWST	Read/Write Status bit for both slave mode and master mode. When in slave mode, this bit reflects the master device read from or write to the slave device if the last address is matched. This bit is valid before the next start bit, stop bit or NAK bit occurred. 1: Read 0: Write	R	0
4	LBST	Last Byte Status bit. 0: Indicate the last byte received or transmitted is address 1: Indicate the last byte received or transmitted is data	R	0
3	IRQP	IRQ Pending bit. Writing 1 to this bit will clear it. 1: IRQ 0: No IRQ	RW	0
2	BBB	Bus Busy Bit 0: Not busy 1: Busy This bit will set to 1 while the start command detected, and set to 0 after the stop command	R	0
1	BEB	Bus Error Bit 0: No error occur 1: Bus error occur Write “1” to clear this bit Generate error bit when following conditions occur: Detect stop bit right after detecting start/restart bit. Detect stop start bit when sending or receiving data.	RW	0
0	RACK	In transmit mode: 0: Has not received the ACK signal 1: Has received the ACK signal. This bit will be cleared when the 9th clock of the next SCL arrived automatically.	R	0

10.2.5.3 TWI_ADDR

TWI Address Register
Offset=0x0008

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:1	SDAD	Slave Device Address. In master mode, these bits are TWI slave device address. In slave mode, these bits are used to compare with the address that the master device sends out.	RW	0

0	-	Reserved	-	-

10.2.5.4 TWI_DAT

TWI Data Register
Offset=0x000C

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	TXRXDAT	TWIDAT contains the byte to be transmitted on the TWI-bus or a byte that has been received from the TWI-bus.	RW	0

10.3 IRC

10.3.1 Features

- Support multiple protocols, compatible 36 kHz, 38 kHz, 40 kHz carrier.

10.3.2 Operation Manual

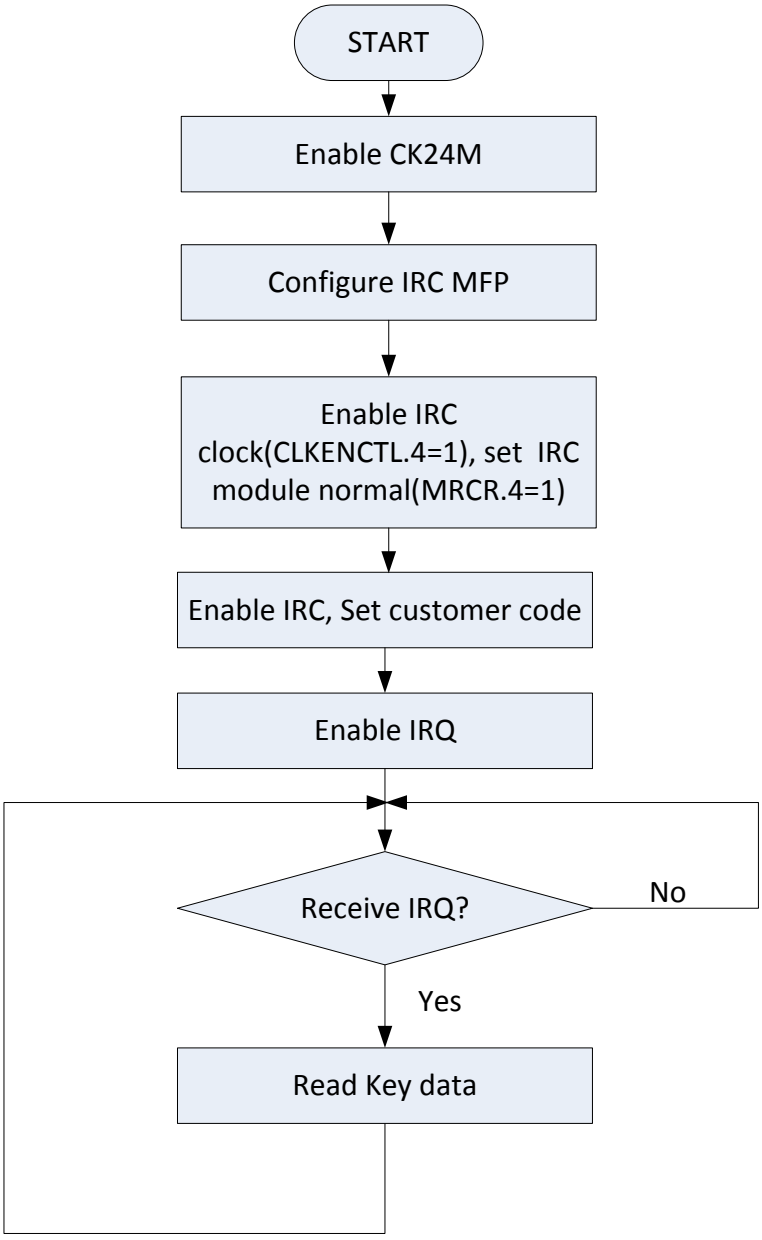


Figure 10-3 IRC receive flow

Note:

1. *When transmit, High level indicate transfer carrier.*
2. *When receive, carrier indicate Low level.*
3. *If the customer code received doesn't match, don't generate IRQ, then reset the status and set the pending bit.*
4. *If the customer code correct, but the command data error, don't generate IRQ. Then reset the status and set the pending bit.*
5. *When receive the repeat code, generate IRQ and set repeat code detected bit to 1.*

10.3.3 Register List

Table 10-5 IRC Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address

IRC	0xC00F0000	0xC00F0000

Table 10-6 IRC Registers Offset Address

Offset	Register Name	Description
0x0050	IRC_CTL	Infrared remote control (IRC) interface control register
0x0054	IRC_STA	IRC status register
0x0058	IRC_CC	IRC customer code register
0x005C	IRC_KDC	IRC key data code register

10.3.4 Register Description

10.3.4.1 IRC_CTL

infrared remote control register
Offset=0x0050

Bits	Name	Description	Access	Reset
31:17	-	Reserved	-	-
16	DBB_EN	Debounce Bypass enable 0: bypass disable 1:bypass enable	RW	0
15:4	DBC	Debounce counter, 1 counter=1/200KHz Default counter=40=200us	RW	0x028
3	IRE	IRC enable 0: disable 1:enable	RW	0
2	IIE	IRC IRQ enable 0:disable 1:enable	RW	0
1:0	ICMS	IRC coding mode select 00:9012 code 01:8bits NEC code 10:RC5 code 11: RC6 code	RW	0

10.3.4.2 IRC_STA

Infrared remote status register
Offset=0x0054

Bits	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6	UCMP	User code don't match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct code the next time 0:user code match 1:user code don't match	RW	0
5	KDCM	Key data code don't match pending bit. Write 1 to this bit will clear it, or auto clear if receive the correct code the next time 0:key data code match 1:key data code don't match	RW	0
4	RCD	Repeated code detected, Write 1 to this bit will clear it, otherwise don't change 0: no repeat code	RW	0

		1: detect repeat code		
3	-	Reserved	-	-
2	IIP	IRC IRQ pending bit. write 1 to this bit will clear it 0:no IRQ pending 1: IRQ pending	RW	0
1	-	Reserved	-	-
0	IREP	IRC receive error pending. 0: receive ok 1: receive error occurs if not match the protocol. Writing 1 to this bit will clear this bit, or auto clear if receive the correct user code and key data code the next time.	RW	0

10.3.4.3 IRC_CC

Infrared remote control customer code register.
Offset=0x0058

Bits	Name	Description	Access	Reset
31:16	CCRCV	customer code received In **RC5 mode**, Bit 4:0 is the customer code In **9012 mode**, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit **NEC mode**, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	R	0
15:0	ICCC	Infrared remote control customer code In **RC5 mode**, Bit 4:0 is the customer code In **9012 mode**, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit **NEC mode**, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	RW	0

10.3.4.4 IRC_KDC

Infrared remote control KEY data code register.
Offset=0x005C

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	IKDC	IRC key data code In RC5 mode, Bit 5:0 is the Key data In 9012 and 8 bit NEC mode, Bit 7:0 is the Key data, Bit 15:8 is the Key anti-data	R	0

10.4 UART

10.4.1 Features

UART1 has the following features:

- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- Support IRQ and DMA mode to transmit data
- Support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system
- UART RX Support DMA single mode
- Baud Rate up to 6Mbps

10.4.2 Register List

Table 10-7 UART1 Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
UART1	0xC00F0000	0xC00F0000

Table 10-8 UART1 Registers Offset Address

Offset	Register Name	Description
0x0000	UART1_CTL	UART1 Control Register
0x0004	UART1_RXDAT	UART1 Receive FIFO Data Register
0x0008	UART1_TXDAT	UART1 Transmit FIFO Data Register
0x000c	UART1_STA	UART1 Status Register
0x0010	UART1_BR	UART1 BAUDRATE divider Register

10.4.3 Register Description

10.4.3.1 UART1_CTL

UART1 Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31:22	-	Reserved	-	-
21	TXAHB_DMA_SEL1	UART1 TX FIFO Clock Select 0: AHB Clock 1:DMA Clock	RW	0
20	LBEN1	Loop Back Enable. Set this bit to enable a loop back mode that data coming on the input will be presented on the output. 0: Disable 1: Enable	RW	0
19	TXIE1	UART1 TX IRQ Enable. 0: Disable 1: Enable	RW	0
18	RXIE1	UART1 RX IRQ Enable. 0: Disable 1: Enable	RW	0
17	TXDE1	UART1 TX DRQ Enable. 0: Disable 1: Enable	RW	0
16	RXDE1	UART1 RX DRQ Enable. 0: Disable 1: Enable	RW	0
15	EN1	UART1 Enable.	RW	0

		When this bit is clear, the UART clock source is inhibited. This can be used to place the module in a low power standby state. 0:disable 1: enable		
14	RXAHB_DMA_SEL1	UART1 RX FIFO Clock Select 0: AHB Clock 1:DMA Clock	RW	0
13	RTSE1	RTS Enable. When this bit is set, request to send data. Note: This bit has no effect if Autoflow enable bit is set. 0:no request 1: request to send data	RW	0
12	AFE1	Autoflow mode Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals. 0: Autoflow mode disable (normal mode) 1: Autoflow mode enable	RW	0
11:10	RDIC1	UART1 RX DRQ/IRQ Control 00: set when RX FIFO received at least one byte data in IRQ/DRQ mode. 01: set when RX FIFO received 4 bytes data in IRQ mode 10: set when RX FIFO received 8 bytes data in IRQ/DRQ mode 11: set when RX FIFO received 12 bytes data in IRQ/DRQ mode In DMA burst mode (normal DMA), DO not set 00, 01 because at least 8 bytes necessary. In DMA single mode (special DMA), DO set 00 for 1 Bytes transfer for each DRQ.	RW	0
9:8	TDIC1	UART1 TX DRQ/IRQ Control 00: set when TX FIFO is at least 1 byte empty in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00, 01 because at least 8 bytes necessary.	RW	0
7	-	Reserved	-	-
6:4	PRS1	Parity Select. Bit 6: PEN, Parity enable Bit 5: STKP, Stick parity Bit 4: EPS, Even parity PEN STKP EPS Selected Parity 0 x x None 1 0 0 Odd 1 0 1 logic 1 1 1 0 Even 1 1 1 logic 0	RW	0
3	-	Reserved	-	-

2	STPS1	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated. 0: 1 stop bit 1: 2 stop bit	RW	0
1:0	DWLS1	Data Width Length Select. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	RW	0

10.4.3.2 UART1_RXDAT

UART1 Receive FIFO Data Register

Offset=0x0004

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	RXDAT1	Received Data.	R	x

10.4.3.3 UART1_TXDAT

UART1 Transmit FIFO Data Register

Offset=0x0008

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7:0	TXDAT1	Transmitted Data.	W	0

10.4.3.4 UART1_STA

UART1 Status Register

Offset=0x000C

Bits	Name	Description	Access	Reset
31:22	-	Reserved	-	-
21	UTBB1	UART1 TX busy bit 0:not busy, TX FIFO is empty and all data be shift out 1:busy	R	0
20:16	TXFL1	TX FIFO Level. The field indicates the current TX FIFO empty level.	R	0x10
15:11	RXFL1	RX FIFO Level. The field indicates the current RX FIFO level of valid data.	R	0
10	TFES1	TX FIFO empty Status 0: no empty 1: empty	R	1
9	RFFS1	RX FIFO full Status 0: no full 1: full	R	0
8	RTSS1	RTS Status. The bit reflects the status of the external RTS- pin.	R	0
7	CTSS1	CTS Status. The bit reflects the status of the external CTS- pin.	R	x
6	TFFU1	TX FIFO Full.	R	0

		1: Full 0: No Full		
5	RFEM1	RX FIFO Empty. 1: Empty 0: No Empty	R	1
4	RXST1	Receive Status. 0: receive OK 1: receive error. Writing 1 to the bit will clear the bit. When stop bit detect error, or parity error, or clock error	RW	0
3	TFER1	TX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the TX FIFO.	RW	0
2	RXER1	RX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the RX FIFO.	RW	0
1	TIP1	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit.	RW	1
0	RIP1	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	RW	0

10.4.3.5 UART1_BR

UART1 BAUDRATE divider register
Offset=0x0010

Bits	Name	Description	Access	Reset
31:16	TXBRDIV1	UART1 TX BAUDRATE divider Baud Rate = Clock_source/Baud Rate divider Clock_source=HOSC or CK24M, selected by CMU_UART1CLK[0]	RW	0x0028
15:0	RXBRDIV1	UART1 BAUDRATE divider Baud Rate = Clock_source/Baud Rate divider Clock_source=HOSC or CK24M, selected by CMU_UART1CLK[0]	RW	0x0028

10.5 SPI

The SPI module is designed according to Motorola serial peripheral interface protocols. It can be configured as either a master or slave device. It can generate a large range of SPI clock so as to communicate with different devices supporting SPI protocols. Especially, this module support three operation mode: write & read, write only, read only mode.
SPI write & read mode use the MOSI pin to serially write instructions, addresses or data to the device. It also uses the MISO pin to read data or status from the device synchronous. This mode is designed to meet normal SPI application.

10.5.1 Features

- ATS2825 integrated 2 SPI Interfaces: SPI1 and SPI0
- SPI0 is for serial flash memory and support randomizer
- Support dual I/O write and read mode
- Support IRQ and DMA mode to transmit data
- SPI clock up to 60MHz

10.5.2 Register List

Table 10-9 SPI1 Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
SPI1	0xC0150000	0xC0150000

Table 10-10 SPI1 Registers Offset Address

Offset	Register Name	Description
0x0000	SPI1_CTL	SPI Control Register
0x0004	SPI1_DRQ	SPI DRQ/IRQ Control Register
0x0008	SPI1_STA	SPI Status Register
0x000C	SPI1_CLKDIV	SPI Clock Divide Register
0x0010	SPI1_TXDAT	SPI Transmit FIFO Data Register
0x0014	SPI1_RXDAT	SPI Receive FIFO Data Register
0x0018	SPI1_BCL	SPI Byte Counter Low Register
0x001C	SPI1_BCH	SPI Byte Counter High Register

10.5.3 Register Description

10.5.3.1 SPI1_CTL

SPI1 Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:8	RLRS1	Config RX FIFO level for restart reading:1~15 When RX FIFO level is less than this number, restart to sending clock out, used only for read only mode.	RW	0x0C
7	SPI1_EN	**SPI1 Enable** 0: Disable 1: Enable	RW	0
6	SPI1_MS	**SPI1 master/slave select** 0: master 1: slave	RW	0
5	SPI1_LM	**LSB/MSB First Select** 0: transmit and receive MSB first 1: transmit and receive LSB first	RW	0
4	SPI1_SS	**SPI1 SS pin control output,** this bit is valid only in master mode 0: output low 1: output high	RW	1
3:2	SPI1_MODE	**SPI1 mode select** CPOL CPHA	RW	0x3

		00: mode 0 01: mode 1 10: mode 2 11: mode 3		
1:0	SPI1_WR	**SPI1 write/read select** 00: write and read 01: write and read 10: write only 11: read only	RW	0

10.5.3.2 SPI1_DRQ

SPI1 DRQ/IRQControl Register
Offset=0x0004

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	SPI1_TDRQ_EN	**SPI1 TX DRQ Enable,** trigger DRQ when SPI1 TX FIFO at least 8 level empty; When DMA remain counter < 8, trigger DRQ until all data transfer completely; 0: disable 1: enable	RW	0
6	SPI1_RDRQ_EN	**SPI1 RX DRQ Enable,** trigger DRQ when SPI1 RX FIFO at least 8 level full.; When DMA remain counter < 8, trigger DRQ until all data received completely; 0: disable 1: enable	RW	0
5	TXAHB_DMA_SEL	**SPI1 TX FIFO Bus Select** **0: AHB Bus** **1:DMA Bus**	RW	0
4	RXAHB_DMA_SEL	**SPI1 RX FIFO Bus Select** **0: AHB Bus** **1:DMA Bus**	RW	0
3	SPI1_TIRQ_EN	**SPI1 TX IRQ Enable,** trigger SPI1 TX IRQ when SPI1 TX FIFO is empty. 0: disable 1: enable	RW	0
2	SPI1_RIRQ_EN	**SPI1 RX IRQ Enable,** trigger SPI1 RX IRQ when SPI1 RX FIFO is not empty. 0: disable 1: enable	RW	0
1	SPI1_TIRQ_PD	**SPI1 TX IRQ Pending**, Write 1 to this bit will clear it. 0: No TX IRQ Pending 1: TX IRQ Pending.	RW	1
0	SPI1_RIRQ_PD	**SPI1 RX IRQ Pending**, Write 1 to this bit will clear it. 0: No RX IRQ Pending 1: RX IRQ Pending.	RW	0

10.5.3.3 SPI1_STA

SPI1 Status Register
Offset=0x0008

Bits	Name	Description	Access	Reset

31:8	-	Reserved	-	-
7	TXEM	**SPI1 TX FIFO Empty** 0: not empty 1: empty	R	1
6	TXFU	**SPI1 TX FIFO Full** 0: not full 1: full	R	0
5	RXEM	**SPI1 RX FIFO Empty** 0: not empty 1: empty	R	1
4	RXFU	**SPI1 RX FIFO Full** 0: not full 1: full	R	0
3	SPI1_BUSY	**SPI1 master mode busy status bit.** The bit is automatically clear when all data have been send out or received and SPISCK has finished; and automatically setup in transmitting/receiving status ; this bit is valid only in SPI1 master mode; 0: SPI1 idle status 1: SPI1 busy status	R	0
2	TXER	**SPI1 TX FIFO error Pending**. Writing 1 to this bit will clear it and reset the TX FIFO, otherwise unchanged. This bit set when SPI1 TX FIFO is wrote overflow;	RW	0
1	RXER	**SPI1 RX FIFO error Pending**. Writing 1 to this bit will clear it and reset the TX FIFO, otherwise unchanged. This bit set when SPI1 RX FIFO is wrote or read overflow;	RW	0
0	-	Reserved	-	-

10.5.3.4 SPI1_CLKDIV

SPI1 Clock Divider Register

Offset=0x000C

Bits	Name	Description	Access	Reset
31:7	-	Reserved	-	-
6	DAWS	Data/Address Width. Select 0: 8 bit data and address, low 8 bit 1: 32 bit data and address	RW	0
5	TXCEB	TX Convert Endian bit, only used in 32bit mode: 0: not convert Endian 0x76543210 ->0x76543210 1: convert Endian 0x76543210 ->0x10325476 When in 8 bit mode, this bit have no effect	RW	0
4	RXCEB	RX Convert Endian bit, only used in 32bit mode: 0: not convert Endian 0x76543210 ->0x76543210 1: convert Endian 0x76543210 ->0x10325476 When in 8 bit mode, this bit have no effect	RW	0
3:0	SPI1_CLKDIV	**SPI1 Clock Divide Factor [3:0]** 0000 /1 0001 /2	RW	0

		0010 /4 … 1111 /30 SPI1 clock = SPI1 source clock/ (SPI1_CLKDIV[3:0]*2)		

10.5.3.5 SPI1_TXDAT

SPI1 Transmit FIFO Data Register
Offset=0x0010

Bits	Name	Description	Access	Reset
31:0	SPI1_TXDAT	**SPI1 Data[7:0]**	W	0

10.5.3.6 SPI1_RXDAT

SPI1 Receive FIFO Data Register
Offset=0x0014

Bits	Name	Description	Access	Reset
31:0	SPI1_RXDAT	**SPI1 Data[7:0]**	R	0

10.5.3.7 SPI1_BCL

SPI1 Bytes Count Register, this register is used for setting SPI1 bytes counter bits in the SPI1 read mode only.
Offset=0x0018

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	SPI1_BCL	Bytes Counter Low bits [15: 0]	RW	0

10.5.3.8 SPI1_BCH

SPI1 Bytes Count Register, this register is used for setting SPI1 I/O mode and delay chain.
Offset=0x001C

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
7	SPI1_IO	**SPI1 data I/O mode select** (valid when SPI1 select write or read only mode) 0: 1x I/O mode select 1: 2x I/O mode select	RW	0
6	SPI1_DELAY_EN	**SPI1 delay chain enable** 0: Disable 1: Enable	RW	0
5:4	SPI1_DELAY	**SPI1 read clock delay time** (valid when SPI1 select write/read and read mode) 00: delay 2 ns 01: delay 4 ns 10: delay 8 ns 11: delay 12 ns	RW	0
3	SPI1_RS	**Read Start Control**, write 1 to start read clock, valid when SPI1 select read only mode. (When transfer is finished, this bit will be auto cleared)	RW	0

2:0	-	Reserved	-	-

11 Audio Interface

11.1 I2S

11.1.1 Features

- Support I2S Transmitter (TX) and I2S Receiver (RX) with master mode and slave mode synchronously
- I2S Support Sample Rate of 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/96kHz

11.1.2 Register List

Table 11-1 DAC_I2S Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
DAC_Control_Register	0xC0050000	0xC0050000

Table 11-2 DAC_I2S Controller Registers

Offset	Register Name	Description
0x00	DAC_DIGCTL	DAC Digital Control Register

11.1.3 Register Description

11.1.3.1 DAC_DIGCTL

DAC Digital Control Register
Offset = 0x00

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
11	I2SLPEN	I2S Loopback Enable: 0x0: Disable 0x1: Enable Note, when enable, I2Stx sends clock and data to I2Srx.	RW	0x0
10	I2SM	I2S Mode: 0x0: Master 0x1: Slave	RW	0x0
9	I2STXEN	I2STX Enable: 0x0: Disable 0x1: Enable	RW	0x0
8	I2SRXEN	I2SRX Enable: 0x0: Disable 0x1: Enable	RW	0x0
7:0	-	Reserved	-	-

11.2 SPDIF TX

11.2.1 Features

- SPDIF supports transmitter mode only.
- SPDIFTX supports sample rate of 192k/96k/48k/44.1k/32k.

11.2.2 Register List

Table 11-3 SPDIFTX Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
SPDIFTX_Control_Register	0xC0052000	0xC0052000

Table 11-4 SPDIFTX Controller Registers

Offset	Register Name	Description
0x00	SPDTX_CTL	SPDIFTX Control Register
0x04	SPDTX_CSL	SPDIFTX Channel State Low Register
0x08	SPDTX_CSH	SPDIFTX Channel State High Register

11.2.3 Register Description

11.2.3.1 SPDTX_CTL

SPDIFTX Control Register
Offset = 0x00

Bit (s)	Name	Description	Access	Reset
31:1	-	Reserved	-	-
0	SPDEN	SPDIFTX Enable. 0: Disable (will reset TX state machine) 1: Enable	RW	0

11.2.3.2 SPDTX_CSL

SPDIFTX Channel State Low Register
Offset = 0x04

Bit (s)	Name	Description	Access	Reset
31:0	SPDCSL	SPDIFTX Channel State Low. (Channel state bit31 to bit0.)	W	x

11.2.3.3 SPDTX_CSH

SPDIFTX Channel State High Register
Offset = 0x08

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:0	SPDCSH	SPDIFTX Channel State High. (Channel state bit47 to bit32.)	W	x

12 User Interface (UI)

12.1 LCD Controller (LCDC)

12.1.1 Features

- RGB565 source data format
- Source data Transfer to FIFO by DMA
- Support 8-bit active (TFT) LCD panels with digital CPU input interface
- Support read and write operation

12.1.2 Function Description

12.1.2.1 RGB888 to RGB565 conversion

This module can convert 24bits RBG format to 16bits RGB before translating to LCD Panel.

12.1.2.2 Source DATA transfer channel

Source data is transferred to frame FIFO through DMA.

12.1.2.3 Source DATA

This LCDC can transfer YCbCr444 or RGB565 format data by setting bit SDT of register LCD_CTL.

12.1.2.4 External Memory Interface

The External Memory Interface Supports 8-bit or 16-bit CPU LCD. It is used to sent command to CPU LCD and read data back from CUP LCD to LCDC.
CPU can write or read through EXTMEM_DATA to access the extended bus according to IFSEL of EXTMEM_CTL.
When it is set to 8bit interface, CPU writes or reads the lowest 8 bits of EXTMEM_DATA, the bus accesses the lower 8bit data bus. When it is set to 16bit interface, CPU writes or reads the lowest 16 bits of EXTMEM_DATA, the bus accesses the 16 bit data bus.

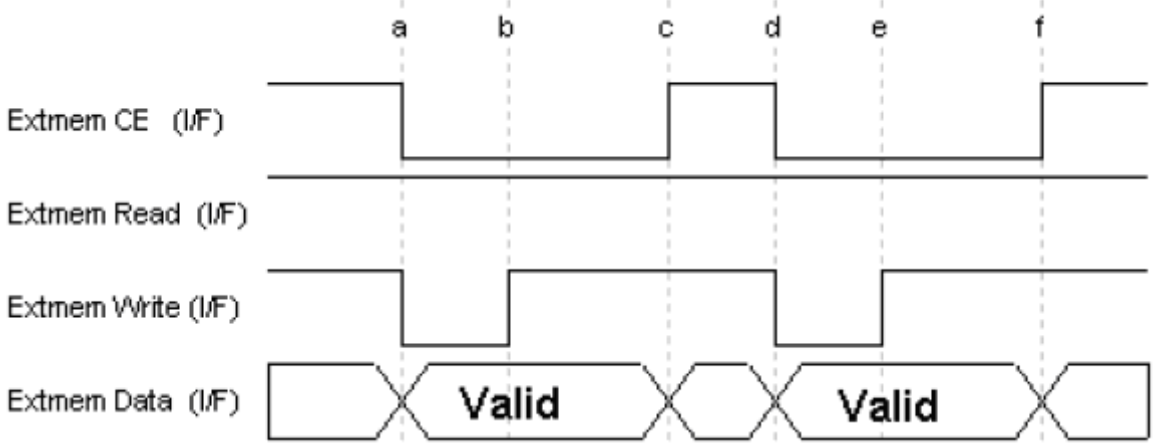


Figure 12-1 LCD Controller Write Timing

Write Timing:

a to b is the low state of writing cycle, the cycles depends on CLKLDU

b to c is the high state of writing cycle, the cycles depends on CLKHDU

a to c is a writing cycle,

When CPU writes EXTMEM_DATA register, the EXTMEM CEB is driven to low level, the host will drive the EXTMEM Data bus until the EXTMEM Write cycle is over. When the EXTMEM CEB is low level, the LCM will be chip selected.

The EXTMEM Write signal will be driven to low level until the low state counter is CLKLDU, then the write signal will be driven to high level until the high state counter is CLKHDU. The device will latch the data at the rise edge of EXTMEM Write.

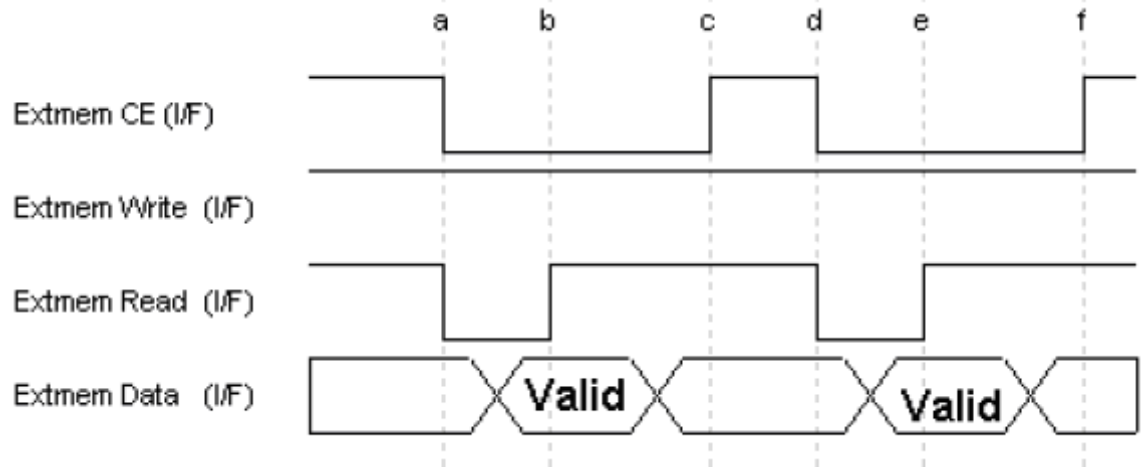


Figure 12-2 LCD Controller Read Timing

Read Timing:

a to b is the low state of reading cycle, the cycles depends on CLKLDU

b to c is the high state of reading cycle, the cycles depends on CLKHDU

a to c is a read cycle

When CPU reads EXTMEM_DATA register, the EXTMEM CEB is driven to low level until the EXTMEM Read cycle is over. When the EXTMEM CEB is low level, the LCM will be chip selected. The EXTMEM Read signal will be driven to low level until the low state counter is CLKLDU, then the read signal will be driven to high level until the high state counter is CLKHDU. When EXTMEM Read is low level, the LCM will drive the EXTMEM Data bus.

12.1.2.5 CPU IF timing

Table 12-1 Control signal define

RS	R/W	Function
0	0	Sets Index Register
0	1	Read Status
1	0	Writes Instruction
1	1	Reads Instruction

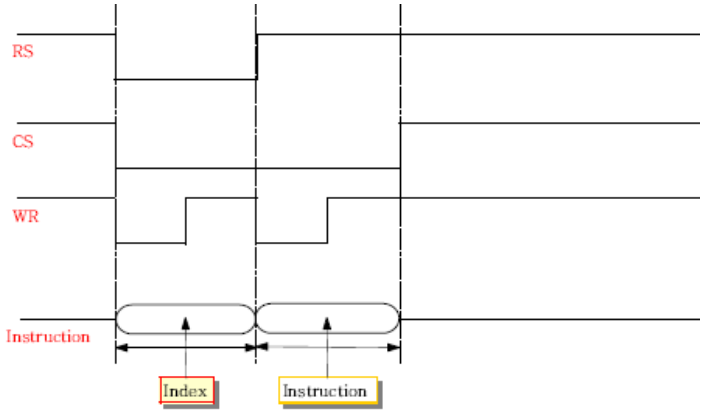


Figure 12-3 CPU LCD Timing

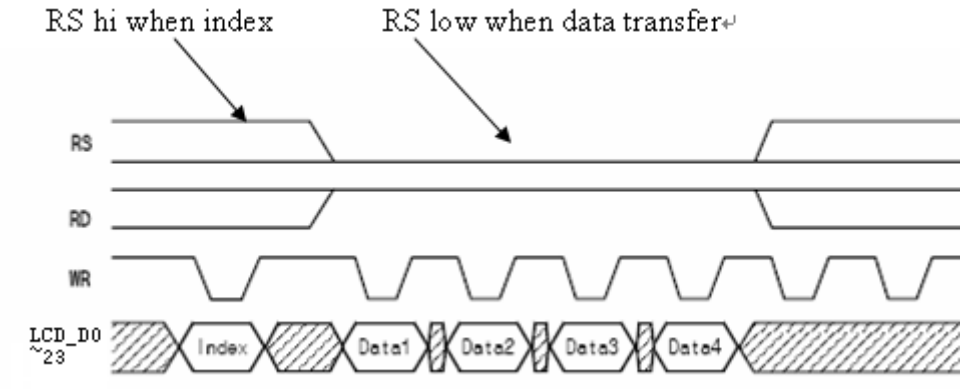


Figure 12-4 LCD Controller 8080 mode bus

12.1.3 Register List

Table 12-2 LCD Controller Registers base address

Name	Physical Base Address	KSEG1 Base Address
LCDC	0xC00D0000	0xC00D0000

Table 12-3 RTC Controller Registers

Offset	Register Name	Description
0x0000	LCD_CTL	LCD Control Register
0x0004	LCD_CLKCTL	LCD and EXTMEM Clock adjust Register
0x0008	EXTMEM_CTL	Extended Memory Interface Control Register
0x000c	EXTMEM_CLKCTL	Extended Memory Interface DATA Register
0x0010	EXTMEM_DATA	Extended Memory Interface DATA Register

12.1.4 Register Description

12.1.4.1 LCD_CTL

LCD controller control register
Offset=0x0000

Bits	Name	Description	Access	Reset
31	LCDFI	LCD Data translate Finish 0: busy 1: finish Write 1 to clear the bit.	RW	0
30:11	-	Reserved	-	-
10	FIFOET	FIFO Empty Status 0: Not Empty 1: Empty	R	0
9:8	-	Reserved	-	-
7	EMDE	FIFO Empty DRQ Enable. 0: Disable 1: Enable This bit should be enabled when DMA is used to transmit the LCD data.	RW	0
6:5	-	Reserved	-	-
4	FORMATS	RGB Format Select: 0: 8bit (RGB 565 2transfer) 1:16bit (RGB 565 1transfer)	RW	0
3	SEQ	RGB Sequence. 0: RGB 1: BGR	RW	0
2:1	-	Reserved	-	-
0	EN	LCD controller Enable. 0: Disable 1: Enable ***Note:*** *before setting this bit all other setting of LCDC should be set. This bit would be cleared by hardware after AHB Clock is synchronized with LCD Clock.*	RW	0

12.1.4.2 LCD_CLKCTL

LCD and EXTMEM Clock adjust Register
Offset=0x0004

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:8	CLKHDU	Clock High Level Duration (from LCD_CLK). from 1 to 16 (CLKHDU +1)	RW	0xF
7:4	-	Reserved	-	-
3:0	CLKLDU	Clock Low Level Duration (from LCD_CLK) from 1 to 16 (CLKLDU +1)	RW	0xF

12.1.4.3 EXTMEM_CTL

Extended Memory Interface Control Register

Offset=0x0008

Bits	Name	Description	Access	Reset
31:29	CESEL	Choose the Chip Select of extended memory Interface 001:CE0 010:CE1 011:CE2 100:CE3 101:CE4 Others: Reserved *Note: Write or read from LCDM, must select CE4*	RW	101
28:9	-	Reserved	-	-
8	IFSEL	Choose the 8bits/16bits bus interface 0: 8 bits interface 1: 16 bits interface	RW	0
7:1	-	Reserved	-	-
0	RS	RS select 0:RS output low voltage level 1:RS output high voltage level RS is low or high voltage in the case of writing INDEX/DATA/REG in different LCM	RW	0

12.1.4.4 EXTMEM_CLKCTL

EM clock control register
Offset=0x000c

Bits	Name	Description	Access	Reset
31:12	-	Reserved	-	-
11:8	EXCLKH	Clock High Level Duration (from AHB_CLK). from 1 to 16 (EXCLKH +1)	RW	0xF
7:4	-	Reserved	-	-
3:0	EXCLKL	Clock Low Level Duration (from AHB_CLK) from 1 to 16 (EXCLKL +1)	RW	0xF

NOTE: *EXTMEM use clock from AHB_CLK, when use EXTMEM to sent command to LCDM or read data from LCDM, this register should be set to obtain perfect operation clock.*

12.1.4.5 EXTMEM_DATA

Extended Memory Interface DATA Register
Offset=0x0010

Bits	Name	Description	Access	Reset
31:16	-	Reserved	-	-
15:8	EXT_DATAH	The higher 8bit data bus of extended interface	RW	0x0
7:0	EXT_DATAL	The lower 8bit data bus of extended interface	RW	0x0

12.2 SEG_LCD&LED controller

12.2.1 Features

- Support 3com / 4com / 5com / 6com SEG_LCD Driving Timing
- Support 4com or 8com DIG_LED Driving Timing
- Support 7 / 8 pin matrix_LED driving timing
- Support LED segment analog constant current configuration
- Support HOSC / LOSC for SEG_LCD & DIG_LED clock source

12.2.2 Register List

Table 12-4 SEG_SREEN Registers base address

Name	Physical Base Address	KSEG1 Base Address
SEG_SREEN	0xC00E_0000	0xC00E0000

Table 12-5 SEG_SREEN Registers

Offset	Register Name	Description
0x0000	SEG_SREEN_CTL	Seg LCD control register
0x0004	SEG_SREEN_DATA0	Seg LCD data register0
0x0008	SEG_SREEN_DATA1	Seg LCD data register1
0x000C	SEG_SREEN_DATA2	Seg LCD data register2
0x0010	SEG_SREEN_DATA3	Seg LCD data register3
0x0014	SEG_SREEN_DATA4	Seg LCD data register4
0x0018	SEG_SREEN_DATA5	Seg LCD data register5

12.2.3 Register Description

12.2.3.1 SEG_SREEN_CTL

Offset=0x0000
Seg-screen control register

Bits	Name	Description	Access	Reset
31:8	-	Reserved	-	-
9:8	LED_COM_DZ	Dead zone: The com of LED will got a “dead zone”, this register define the width of the dead zone: 00b: no dead zone between LED COM Beats 01b: 1/32 of the LED COM beat will be dead zone 10b: 2/32 of the LED COM beat will be dead zone 11b: 3/32 of the LED COM beat will be dead zone	RW	0x0
7	SEGOFF	Segment Off 0:Segment is always off 1:Segment value is according to LCD_DATA P.S. Only active in COM/SEG or Digit-LED Mode	RW	0x0
6	-	Reserved	-	-

5	LCD_OUT_EN	LCD&LED pad output Enable select: 0: the pads of seg_LCD and LED will output “high_Z”. 1: the pads of seg_LCD and LED output signal as its timing.	RW	0x0
4	REFRSH	Refresh LCD/LED Data 0:Hold LCD_DATA Refresh LCD/LED panel according to the LCD_DATA buffer value 1:Update LCD_DATA Refresh the LCD_DATA buffer value from LCD_DATA register P.S. Only active in COM/SEG or Digit-LED Mode; When updating the value of LCD_DATA register, write “1” to this bit, the hardware will clear this bit when the LCD_DATA has been updated.	RW	0x0
3:0	MODE_SEL	Mode Select 0b0000: 3Com,1/3 Bias SEG/COM LCD Frame-Invert 0b0001: 3Com,1/3 Bias SEG/COM LCD Row-Invert 0b0010: 4Com,1/3 Bias SEG/COM LCD Frame-Invert 0b0011: 4Com,1/3 Bias SEG/COM LCD Row-Invert 0b0100: 5Com,1/3 Bias SEG/COM LCD Frame-Invert 0b0101: 5Com,1/3 Bias SEG/COM LCD Row-Invert 0b0110: 6Com,1/3 Bias SEG/COM LCD Frame-Invert 0b0111: 6Com,1/3 Bias SEG/COM LCD Row-Invert 0b1000: 4Com Digit-LED Common-Cathode Mode 0b1001: 4Com Digit-LED Common- Anode Mode 0b1010: 8Com Digit-LED Common-Cathode Mode 0b1011: 8Com Digit-LED Common- Anode Mode 0b1100: 7Matrix_LED mode 0b1101: 8Matrix_LED mode	RW	0x0

12.2.3.2 SEG_SREEN_DATA0

Offset=0x0004
Seg-screen data register0

Bits	Name	Description	Access	Reset
31:24	COM0_BYTE3	SEG/COM Mode: COM0_SEG[31:24]. Digit-LED Mode: COM3_seg[7:0] Matrix_LED Byte3 When set to “1”, the cross of COM and SEG is ON; Else is OFF.	RW	0x0

23:16	COM0_BYTE2	SEG/COM Mode: COM0_SEG[23:16]. Digit-LED Mode: COM2_seg[7:0] Matrix_LED Byte2.	RW	0x0
15:8	COM0_BYTE1	SEG/COM Mode: COM0_SEG[15:8]. Digit-LED Mode: COM1_seg[7:0] Matrix_LED Byte1.	RW	0x0
7:0	COM0_BYTE0	SEG/COM Mode: COM 0_SEG[7:0]. Digit-LED Mode: COM0_seg[7:0] Matrix_LED Byte0.	RW	0x0

12.2.3.3 SEG_SREEN_DATA1

Offset=0x0008
Seg-screen data register1

Bits	Name	Description	Access	Reset
31:24	COM1_BYTE3	SEG/COM Mode: COM1_SEG[31:24]. Digit-LED Mode: COM7_seg[7:0] Matrix_LED Byte7.	RW	0x0
23:16	COM1_BYTE2	SEG/COM Mode: COM1_SEG[23:16]. Digit-LED Mode: COM6_seg[7:0] Matrix_LED Byte6	RW	0x0

15:8	COM1_BYTE1	SEG/COM Mode: COM1_SEG[15:8]. Digit-LED Mode: COM5_seg[7:0] Matrix_LED Byte5	RW	0x0
7:0	COM1_BYTE0	SEG/COM Mode: COM1_SEG[7:0]. Digit-LED Mode: COM4_seg[7:0] Matrix_LED Byte4	RW	0x0

12.2.3.4 SEG_SREEN_DATA2

Offset=0x000C
Seg-screen data register2

Bits	Name	Description	Access	Reset
31:0	COM2_WORD	SEG/COM Mode: COM2_SEG[31:0]. if the xTH bit of this register is “1”, Com2_seg-x will on.	RW	0x0

12.2.3.5 SEG_SREEN_DATA3

Offset=0x0010
Seg-screen data register3

Bits	Name	Description	Access	Reset
31:0	COM3_WORD	SEG/COM Mode: COM3_SEG[31:0]. if the xTH bit of this register is “1”, Com3_seg-x will on.	RW	0x0

12.2.3.6 SEG_SREEN_DATA4

Offset=0x0014
Seg_screen data register4

Bits	Name	Description	Access	Reset
31:0	COM4_WORD	SEG/COM Mode: COM4_SEG[31:0]. if the xTH bit of this register is “1”, Com4_seg-x will on.	RW	0x0

12.2.3.7 SEG_SREEN_DATA5

Offset=0x0018
Seg_screen data register5

Bits	Name	Description	Access	Reset

31:0	COM5_WORD	SEG/COM Mode: COM5_SEG[31:0]. if the xTH bit of this register is “1”, Com5_seg-x will on.	RW	0x0

13 GPIO and I/O Multiplexer

13.1 Features

GPIO (General Purpose Input /Output) MFP:
GPIO can output 0 or 1 and detect the signal level of the external circuit. Each GPIO has its own enable control bit and data registers. But the PADs are limited, so MFP module is designed for multiplexing these PADs.

- Some PAD has internal pull down or pull up resistors
- Driving strength can be adjusted, Level (n) corresponds to (2n) mA
- Automatically switching PAD function
- Support 4 channels PWM output, frequency ranges from 0.015625Hz~80K, adjustable. Under normal mode, PWM can output 256 kinds of duty cycles; Under breath mode, PWM support breathing lights.

SIO (Special Input /Output) MFP:
There are 10 Special I/O ports to bring more flexible application possibility.
Settings in actual practice please consult our engineers. The multiplexing relationship can be found in *Chapter 13 Pin Description.*

13.2 Operation Manual

13.2.1 GPIO Output

13.2.2 GPIO Output

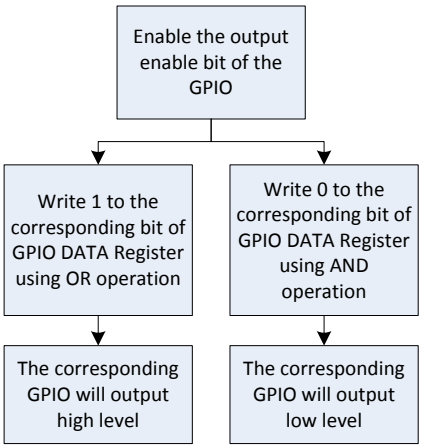


Figure 13-4 GPIO Output Configuration

13.2.3 GPIO Input

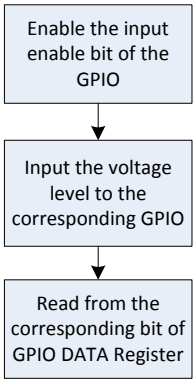


Figure 13-5 GPIO Input Configuration

13.2.4 SIO Output

Refer to the procedure as follows to configure an analog pin MICINL as a digital function such as SIO0.

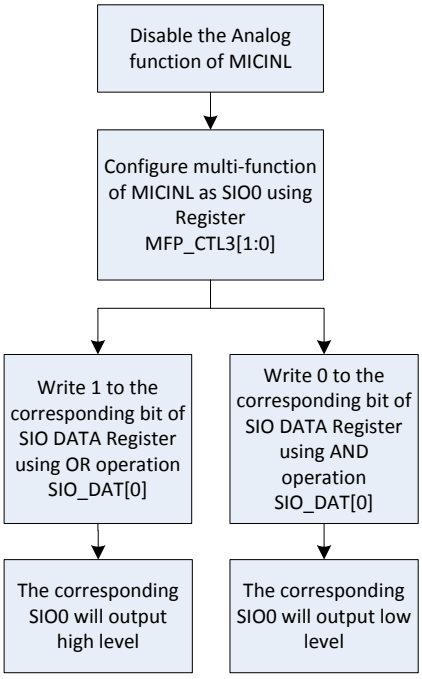


Figure 13-6 SDIO Output Configuration

13.2.5 GPIO Output/Input Loop Test

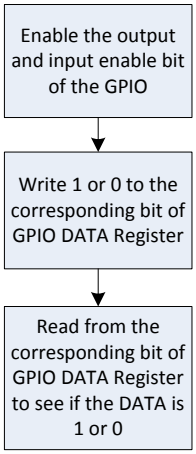


Figure 13-7 GPIO In/Out Loop Test

13.2.6 PWM Configure

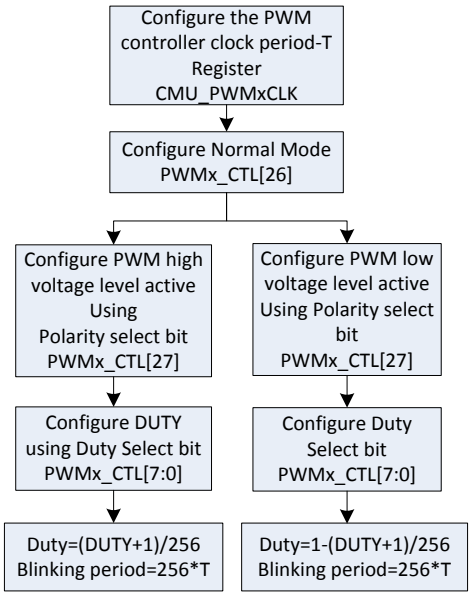


Figure 13-8 PWM Configuration

For example, if Duty =50% and the Blinking period is two seconds, T=2/256, the Frequency of the PWM controller clock is 1/T=128Hz, So CMU_PWMxCLK can be configured as 0xF9, PWMx_CTL can be configured as 0x0800007F.

13.3 Register List

Table 13-1 GPIO_MFP Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
GPIO_MFP	0xC0090000	0xC0090000

Table 13-2 GPIO&MFP Controller Registers

Offset	Register Name	Description
GPIO Register		
0x0000	GPIOAOUTEN	GPIOA Output Enable

0x0004	GPIOAINEN	GPIOA Input Enable
0x0008	GPIOADAT	GPIOA Data
0x000C	GPIOAPUEN	GPIOA 50K PU Enable
0x0010	GPIOAPDEN	GPIOA 50K PD Enable
0x0014	GPIOBOUTEN	GPIOB Output Enable
0x0018	GPIOBINEN	GPIOB Input Enable
0x001C	GPIOBDAT	GPIOB Data
0x0020	GPIOBPUEN	GPIOB 50K PU Enable
0x0024	GPIOBPDEN	GPIOB 50K PD Enable
0x0028	SIO_OUTEN	SIO Output Enable
0x002C	SIO_INEN	SIO Input Enable
0x0030	SIO_DAT	SIO Data
0x0034	SIO_PUEN	SIO 50K PU Enable
0x0038	SIO_PDEN	SIO 50K PD Enable
0x003C	GPIOB0_CTL	GPIOB0 Control
PWM Register		
0x0048	PWM0_CTL	PWM0 Output Control
0x004C	PWM1_CTL	PWM1 Output Control
0x0050	PWM2_CTL	PWM2 Output Control
0x0044	PWM3_CTL	PWM3 Output Control
MFP Register		
0x0054	MFP_CTL0	Multiplexing Control 0
0x0058	MFP_CTL1	Multiplexing Control 1
0x005C	MFP_CTL2	Multiplexing Control 2
0x0060	MFP_CTL3	Multiplexing Control 3
Analog/Digital Select Register		
0x0064	AD_SELECT	Analog/Digital Select
0x00A4	AD_SELECT1	Analog/Digital Select 1
PAD Drive Register		
0x0068	PADPUPD	PAD PU PD Resistance Enable
0x006C	PAD_SMIT	PAD Schmitt Control Register
0x0070	PADDRV0	PAD Drive Capacity Select 0
0x0074	PADDRV1	PAD Drive Capacity Select 1
0x0078	PADDRV2	PAD Drive Capacity Select 2
0x007C	PADDRV3	PAD Drive Capacity Select 3
0x0040	PADDRV4	PAD Drive Capacity Select 4
LED Register		
0x008C	LED_SEG_RC_EN	LED SEG Restrict Current Enable
0x0090	LED_SEG_BIAS_EN	LED SEG Bias Current Enable

13.4 GPIO Register Description

13.4.1 GPIOAOUTEN

GPIOA Output Enable Register
Offset=0x00

Bit (s)	Name	Description	Access	Reset
31:0	GPIOAOUTEN	GPIOA[31:0] Output Enable. 0: Disable 1: Enable	RW	0x0

13.4.2 GPIOAINEN

GPIOA Input Enable Register
Offset=0x04

Bit (s)	Name	Description	Access	Reset
31:0	GPIOAINEN	GPIOA[31:0] Input Enable. 0: Disable 1: Enable	RW	0x0

13.4.3 GPIOADAT

GPIOA Data Register
Offset=0x08

Bit (s)	Name	Description	Access	Reset
31:0	GPIOADAT	GPIOA[31:0] Input/Output Data.	RW	0x0

13.4.4 GPIOAPUEN

GPIOA 50K PU Enable Register
Offset=0x0C

Bit (s)	Name	Description	Access	Reset
31:0	GPIOAPUEN	GPIOA[31:0] 100K PU Enable. 0: Disable 1: Enable	RW	0x10000

13.4.5 GPIOAPDEN

GPIOA 50K PD Enable Register
Offset=0x10

Bit (s)	Name	Description	Access	Reset
31:0	GPIOAPDEN	GPIOA[31:0] 100K PD Enable. 0: Disable 1: Enable	RW	0x0

13.4.6 GPIOBOUTEN

GPIOB Output Enable Register
Offset=0x14

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12:1	GPIOBOUTEN	GPIOB[12:1] Output Enable. 0: Disable 1: Enable	RW	0x0
0	-	Reserved	-	-

13.4.7 GPIOBINEN

GPIOB Input Enable Register
Offset=0x18

Bit (s)	Name	Description	Access	Reset

31:13	-	Reserved	-	-
12:1	GPIOBINEN	GPIOB[12:1] Input Enable. 0: Disable 1: Enable	RW	0x0
0	-	Reserved	-	-

13.4.8 GPIOBDAT

GPIOB Data Register
Offset=0x1C

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12:1	GPIOBDAT	GPIOB[12:1] Input/Output Data.	RW	0x0
0	-	Reserved	-	-

13.4.9 GPIOBPUEN

GPIOB 50K PU Enable Register
Offset=0x20

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12:1	GPIOBPUEN	GPIOB[12:1] 100K PU Enable. 0: Disable 1: Enable	RW	0x0
0	-	Reserved	-	-

13.4.10 GPIOBPDEN

GPIOB 50K PD Enable Register
Offset=0x24

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	-	-
12:1	GPIOBPDEN	GPIOB[12:1] 100K PD Enable. 0: Disable 1: Enable	RW	0x0
0	-	Reserved	-	-

13.4.11 SIO_OUTEN

SpecialIO Output Enable Control Register
Offset = 0x28

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	SIO_OUTEN1	SpecialIO[9:0] Output Enable. 0: Disable 1: Enable	RW	0x0

13.4.12 SIO_INEN

SpecialIO Input Enable Control Register

Offset = 0x2C

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	SIO_INEN	SpecialIO[9:0] Input Enable. 0: Disable 1: Enable	RW	0x0

13.4.13 SIO_DAT

SpecialIO DATA Register
Offset = 0x30

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	SIO_DAT	SpecialIO[9:0] Input/Output Data. SIO0~SIO5 is AVCC Domain; SIO6~SIO9 is VCC Domain.	RW	0x0

13.4.14 SIO_PUEN

SpecialIO PULL UP Enable Control Register
Offset = 0x34

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	SIO_PUEN	SpecialIO[9:0] 50K PULL UP Enable. 0: Disable 1: Enable	RW	0x0

13.4.15 SIO_PDEN

SpecialIO PULL DOWN Enable Control Register
Offset = 0x38

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9:0	SIO_PDEN	SpecialIO[9:0] 50K PULL DOWN Enable. 0: Disable 1: Enable	RW	0x0

13.4.16 GPIOB0_CTL

GPIOB0 Control Register (RTCVDD)
Offset = 0x3C

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	-	-
10:9	GPIOB0_MFP	00: GPIOB0 is used as digital function 01: GPIOB0 is used as LRADC1 (Analog Function), 10: Reserved 11: Reserved	RW	0x0
8:7	GPIOB0_DRV	GPIOB0 PAD Drive Control 00: Level 1 01: Level 2	RW	0x1

		10: Level 4 11: Level 8		
6:5	-	Reserved	-	-
4	GPIOB0OUTEN	GPIOB0 Output Enable. 0: Disable 1: Enable	RW	0x0
3	GPIOB0INEN	GPIOB0 Input Enable. 0: Disable 1: Enable	RW	0x0
2	GPIOB0DAT	GPIOB0 Input/Output Data.	RW	0x0
1	GPIOB0PUEN	GPIOB0 100K PU Enable. 0: Disable 1: Enable	RW	0x0
0	GPIOB0PDEN	GPIOB0 100K PD Enable. 0: Disable 1: Enable	RW	0x0

13.5 PWM Register Description

13.5.1 PWM0_CTL

PWM0 Output Control Register
Offset=0x48

Bit (s)	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	MODE_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Time of climb up and fall down: T2= (Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

13.5.2 PWM1_CTL

PWM1 Output Control Register
Offset=0x4C

Bit (s)	Name	Description	Access	Reset
31:28	-	Reserved	-	-

27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	MODE_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Time of climb up and fall down: T2= (Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

13.5.3 PWM2_CTL

PWM2 Output Control Register
Offset=0x50

Bit (s)	Name	Description	Access	Reset
31:28	-	Reserved	-	-
27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	MODE_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Time of climb up and fall down: T2= (Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

13.5.4 PWM3_CTL

PWM3 Output Control Register
Offset=0x44

Bit (s)	Name	Description	Access	Reset
31:28	-	Reserved	-	-

27	POL_SEL	Polarity select: 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	RW	0x0
26	MODE_SEL	Mode Select: 0: Normal_Mode 1: Breath_Mode	RW	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Time of climb up and fall down: T2= (Q+1)*32*32t t is the period of CMU_PWM	RW	0x0
23:16	H	Time of Duty =32/32 : High Level Time = H*32t t is the period of CMU_PWM	RW	0x0
15:8	L	Time of Duty =0/32 : Low Level Time = L*32t t is the period of CMU_PWM	RW	0x0
7:0	DUTY	Duty Select: T Active = (Duty+1)/256 Only Active in Normal Mode	RW	0x0

13.6 MFP Register Description

13.6.1 MFP_CTL0

Multi-Function PAD Control Register 0
Offset=0x54

Bit (s)	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:27	GPIOA23	000: SD_DAT3 001: EM_D11 010: LCD_D11 011: LCD_SEG13 100: SPDIFTX 101: PWM2 110: UART_TX1 111: SD_DAT0	RW	0
26:24	GPIOA22	000: SD_DAT2 001: EM_D10 010: LCD_D10 011: LCD_SEG12 100: UART_TX1 101: SIRQ0 110: IR_RX 111: PWM1	RW	0
23:21	GPIOA21	000: SD_DAT1 001: EM_D9 010: LCD_D9 011: LCD_SEG11 100: UART_RX1 101: PWM0 110: SPI1_MOSI 111: Reserved	RW	0

20:18	GPIOA20	000: SD_DAT0 001: EM_D8 010: LCD_D8 011: LCD_SEG10 100: PWM2 101: SPI1_MISO 110:111: Reserved	RW	0
17:15	-	Reserved	-	-
14:13	GPIOA17	00: SD_CLK0 01: UART_TX1 10: LCD_SEG15 11: SPI1_SCLK	RW	0
12:11	GPIOA16	00: SD_CMD 01: UART_RX1 10: LCD_SEG14 11: SPI1_SS	RW	0
10:9	GPIOA15	00: LED_SEG7 01: EM_D7 10: LCD_D7 11: LCD_SEG9	RW	0
8:7	GPIOA14	00: LED_SEG6 01: EM_D6 10: LCD_D6 11: LCD_SEG8	RW	0
6:5	GPIOA13	00: LED_SEG5 01: EM_D5 10: LCD_D5 11: LCD_SEG7	RW	0
4:3	GPIOA12	00: LED_SEG4 01: EM_D4 10: LCD_D4 11: LCD_SEG6	RW	0
2:0	GPIOA11	000: LED_SEG3 001: EM_D3 010: LCD_D3 011: LCD_SEG5 100: UART_RTS1 101: SPI1_MOSI 110:111: Reserved	RW	0

13.6.2 MFP_CTL1

Multi-Function PAD Control Register 1
Offset=0x58

Bit (s)	Name	Description	Access	Reset
31:29	GPIOA10	000: LED_SEG2 001: EM_D2 010: LCD_D2 011: LCD_SEG4 100: UART_CTS1 101: SPI1_MISO 110:111: Reserved	RW	0
28:26	GPIOA9	000: LED_SEG1	RW	0

		001: EM_D1 010: LCD_D1 011: LCD_SEG3 100: SPI1_SCLK 101:111: Reserved		
25:23	GPIOA8	000: LED_SEG0 001: EM_D0 010: LCD_D0 011: LCD_SEG2 100: SPI1_SS 101: PWM3 110:111: Reserved	RW	0
22:20	GPIOA7	000: LED_COM7 001: EM_CEB4 010: LCD_SEG1 011: SIRQ1 100: PWM0 101: FMCLKOUT 110:111: Reserved	RW	0
19:18	GPIOA6	00: LED_COM6 01: EM_CEB3 10: LCD_SEG0 11: I2S_LRCLK	RW	0
17:16	GPIOA5	00: LED_COM5 01: EM_CEB2 10: LCD_COM5 11: PWM3	RW	0
15:10	-	Reserved	-	-
9:7	GPIOA2	000: LED_COM2 001: EM_RDB 010: LCD_RDB 011: LCD_COM2 100: PWM2 101: UART_RX1 110: I2S_LRCLK 111: Reserved	RW	0
6:3	GPIOA1	0000: LED_COM1 0001: EM _RS 0010: LCD _RS 0011: LCD_COM1 0100: TWI_SDA 0101: SIRQ1 0110: PWM3 0111: UART_CTS1 1000: I2S_BCLK 1001…1111: Reserved	RW	0
2:0	GPIOA0	000: LED_COM0 001: EM_WRB 010: LCD_WRB 011: LCD_COM0 100: TWI_SCL 101: PWM1 110: UART_RTS1 111: I2S_MCLK	RW	0

13.6.3 MFP_CTL2

Multi-Function PAD Control Register2
Offset=0x5C

Bit (s)	Name	Description	Access	Reset
31:20	-	Reserved	-	-
19	GPIO_B12	0: SPI_IO3 1: TWI_SDA	RW	0
18:16	GPIO_B11	000: SPI_IO2 001: TWI_SCL 010: PWM3 011: SIRQ0 100: IR_RX 101: SD_CLK0 110…111: Reserved	RW	0
15	GPIO_B5	0: LCD_SEG26 1: I2S_DIN	RW	0
14:13	GPIO_B4	00: LCD_SEG25 01: I2S_DOUT 10: I2S_DIN 11: SPDIFTX	RW	0
12	GPIO_B3	0: LCD_SEG24 1: I2S_LRCLK	RW	0
11	GPIO_B2	0: LCD_SEG23 1: I2S_BCLK	RW	0
10	GPIO_B1	0: LCD_SEG22 1: I2S_MCLK	RW	0
9	-	Reserved	-	-
8:7	GPIOA31	00: SPI_MOSI 01: SPI_MISO 10: LCD_SEG20 11: Reserved	RW	0
6:5	-	Reserved	-	-
4:2	GPIOA29	000: SPI_SCLK 001: SPI_SS 010: SD_CLK1 011: TWI_SDA 100: SIRQ1 101: LCD_SEG19 110…111: Reserved	RW	0
1:0	GPIOA28	00: SPI_SS 01: SPI_MOSI 10: LCD_SEG18 11: Reserved	RW	0

13.6.4 MFP_CTL3

Mult-Function PAD Control Register 3
Offset = 0x60

Bit (s)	Name	Description	Access	Reset
31	-	Reserved	-	-
30	GPIOA14	0: according to MFP_CTL0[8:7]	RW	0

		1: TWI_SDA0		
29	GPIOA13	0: according to MFP_CTL0[6:5] 1: TWI_SCL0	RW	0
28	GPIOA12	0: according to MFP_CTL0[4:3] 1: TWI_INT	RW	0
27	-	Reserved	-	-
26	GPIOA2	0: according to MFP_CTL1[9:7] 1: BT_ACT	RW	0
25	GPIOA1	0: according to MFP_CTL1[6:3] 1: BT_STE	RW	0
24	GPIOA0	0: according to MFP_CTL1[2:0] 1: BT_CK	RW	0
23:22	GPIOB9	00: LCD_SEG30 01: PWM2 10: I2S_MCLK 11: Reserved	RW	0
21:20	GPIOB8	00: LCD_SEG29 01: PWM1 10: I2S_BCLK 11: Reserved	RW	0
19:18	VROS	0x0: VROS 0x1: I2S_DOUT 0x2: SpecialIO9 0x3: Reserved	RW	0
17:16	AOUTR	0x0: AOUTR / AOUTRP 0x1: I2S_MCLK 0x2: SpecialIO8 0x3: Reserved	RW	0
15:14	VRO	0x0: VRO 0x1: I2S_LRCLK 0x2: SpecialIO7 0x3: Reserved	RW	0
13:12	AOUTL	0x0: AOUTL / AOUTLP 0x1: I2S_BCLK 0x2: SpecialIO6 0x3: Reserved	RW	0
11:10	-	Reserved	-	-
9:8	GPIOB7	00: LCD_SEG28 01: PWM0 10: I2S_DOUT 11: I2S_DIN	RW	0
7	AUX1R	0x0: AUX1R 0x1: SpecialIO5	RW	0
6	AUX1L	0x0: AUX1L 0x1: SpecialIO4	RW	0
5	AUX0R	0x0: AUX0R 0x1: SpecialIO3	RW	0
4	AUX0L	0x0: AUX0L 0x1: SpecialIO2	RW	0
3:2	MICINR	0x0: MICINR/ MICINLN 0x1: DMICDAT 0x2: SpecialIO1 0x3: Reserved	RW	0

1:0	MICINL	0x0: MICINL/ MICINLP 0x1: DMICCLK 0x2: SpecialIO0 0x3: Reserved	RW	0

13.7 Analog/Digital Select Register

13.7.1 AD_SELECT

Analog/Digital Select Register
Offset=0x64

Bit (s)	Name	Description	Access	Reset
31:30	GPIOA15	00: GPIOA15 is used as digital function, 01: GPIOA15 is used as TK7 (Analog Function) 10: Reserved 11: Reserved	RW	0
29:28	GPIOA14	00: GPIOA14 is used as digital function, 01: GPIOA14 is used as TK6 (Analog Function) 10: Reserved 11: Reserved	RW	0
27:26	GPIOA13	00: GPIOA13 is used as digital function, 01: GPIOA13 is used as TK5 (Analog Function) 10: Reserved 11: Reserved	RW	0
25:24	GPIOA12	00: GPIOA12 is used as digital function, 01: GPIOA12 is used as TK4 (Analog Function) 10: Reserved 11: Reserved	RW	0
23:22	GPIOA11	00: GPIOA11 is used as digital function, 01: GPIOA11 is used as TK3 (Analog Function) 10: Reserved 11: Reserved	RW	0
21:20	GPIOA10	00: GPIOA10 is used as digital function, 01: GPIOA10 is used as TK2 (Analog Function) 10: Reserved 11: Reserved	RW	0
19:18	GPIOA9	00: GPIOA9 is used as digital function, 01: GPIOA9 is used as TK1 (Analog Function) 10: Reserved 11: Reserved	RW	0
17:16	GPIOA8	00: GPIOA8 is used as digital function, 01: GPIOA8 is used as TK0 (Analog Function) 10: Reserved 11: Reserved	RW	0
15:14	GPIOA23	00: GPIOA23 is used as digital function, 01: GPIOA23 is used as LRADC3 (Analog Function), 10: GPIOA23 is used as TK7 (Analog Function), 11: Reserved	RW	0
13:12	GPIOA6	00: GPIOA6 is used as digital function, 01: GPIOA6 is used as TK6 (Analog Function) 10: Reserved 11: Reserved	RW	0

11:10	GPIOA5	00: GPIOA5 is used as digital function, 01: GPIOA5 is used as TK5 (Analog Function) 10: Reserved 11: Reserved	RW	0
9:8	-	Reserved	-	-
7:6	GPIOB9	00: GPIOB9 is used as digital function, 01: GPIOB9 is used as TK3 (Analog Function) 10: Reserved 11: Reserved	RW	0
5:4	GPIOB8	00: GPIOB8 is used as digital function, 01: GPIOB8 is used as TK2 (Analog Function) 10: Reserved 11:Reserved	RW	0
3:2	GPIOB7	00: GPIOB7 is used as digital function, 01: GPIOB7 is used as TK1 (Analog Function) 10: Reserved 11: Reserved	RW	0
1:0	GPIOA21	00: GPIOA21 is used as digital function, 01: GPIOA21 is used as TEMPADC (Analog Function) 10: GPIOA21 is used as TK0 (Analog Function) 11: Reserved	RW	0

13.7.2 AD_SELECT1

Analog/Digital Select Register 1
Offset=0xA4

Bit (s)	Name	Description	Access	Reset
31:3	-	Reserved	-	-
2:1	GPIOA22	00: GPIOA22 is used as digital function, 01: GPIOA22 is used as LRADC2 (Analog Function), 10: GPIOA22 is used as SHEILD (Analog Function), 11: Reserved	RW	0
0	GPIOA2	0: GPIOA2 is used as digital function, 1: GPIOA2 is used as LRADC4 (Analog Function)	RW	0

13.8 PAD Drive Register Description

13.8.1 PADPUPD

PAD PU PD Resistance Control Register
Offset=0x68

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	-	-
9	SD_DATA4_7	MMC/SD Data4~7 50k PU Select 0:Disable 1:Enable	RW	0
8	-	Reserved	-	-
7	SD_CMD	MMC/SD CMD 50k PU Enable 0:Disable 1:Enable	RW	0
6	SD_DATA0_3	MMC/SD Data0~3 50k PU Select	RW	0

		0:Disable 1:Enable		
5	SIRQ1PD	SIRQ1 100k PD Enable 0:Disable 1:Enable	RW	0
4	SIRQ1PU	SIRQ1 100k PU Enable 0:Disable 1:Enable	RW	0
3	SIRQ0PD	SIRQ0 100k PD Enable 0:Disable 1:Enable	RW	0
2	SIRQ0PU	SIRQ0 100k PU Enable 0:Disable 1:Enable	RW	0
1	TWI	TWI 10k PU Enable 0:Disable 1:Enable	RW	0
0	UART_RX1	UART_RX1 10k PU Enable 0:Disable 1:Enable	RW	0

13.8.2 PAD_SMIT

PAD Schmitt Control Register
Offset=0x6C

Bit (s)	Name	Description	Access	Reset
31:23	-	Reserved	-	-
22	SPIBT_SS	SPIBT_SS & SPI_SS SMIT Enable 0:Disable 1:Enable	RW	1
21	-	Reserved	-	-
20	GPIOA29	SPI_SS TWI_SCL & SIRQ1 SMIT Enable 0:Disable 1:Enable	RW	1
19	GPIOA28	SPI_SS SMIT Enable 0:Disable 1:Enable	RW	1
18	GPIOA22	SIRQ0 &IR_RX SMIT Enable 0:Disable 1:Enable	RW	1
17:16	-	Reserved	-	-
15	GPIOA11	DEJ_TDI SMIT Enable 0:Disable 1:Enable	RW	1
14	GPIOA10	DEJ_TCK SMIT Enable 0:Disable 1:Enable	RW	1
13	GPIOA9	DEJ_TMS SMIT Enable 0:Disable 1:Enable	RW	1
12	GPIOA7	SIRQ1 SMIT Enable 0:Disable 1:Enable	RW	1

11	-	Reserved	-	-
10	GPIOA2	MEJ_TCK SMIT Enable 0:Disable 1:Enable	RW	1
9	GPIOA1	MEJ_TMS & SIRQ1 & TWI_SDA SMIT Enable 0:Disable 1:Enable	RW	1
8	GPIOA0	TWI_SCL SMIT Enable 0:Disable 1:Enable	RW	1
7	-	Reserved	-	-
6	GPIOB11	TWI_SCL SMIT Enable 0:Disable 1:Enable	RW	1
5	GPIOB9	DEJ_TDI SMIT Enable 0:Disable 1:Enable	RW	1
4	GPIOB8	DEJ_TCK SMIT Enable 0:Disable 1:Enable	RW	1
3	GPIOB7	DEJ_TMS SMIT Enable 0:Disable 1:Enable	RW	1
2:0	-	Reserved	-	-

13.8.3 PADDRV0

PAD Drive Control Register 0
Offset=0x70

Bit (s)	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:27	GPIOA9	GPIOA9 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1
26:24	GPIOA8	GPIOA8 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1
23:21	GPIOA7	GPIOA7 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3	RW	1

		011: Level 4 100: Level 9 101: Level 10 110: Level 11 111: Level 12		
20:18	GPIOA6	GPIOA6 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 9 101: Level 10 110: Level 11 111: Level 12	RW	1
17:15	GPIOA5	GPIOA5 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 9 101: Level 10 110: Level 11 111: Level 12	RW	1
14:9	-	Reserved	-	-
8:6	GPIOA2	GPIOA2 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 9 101: Level 10 110: Level 11 111: Level 12	RW	1
5:3	GPIOA1	GPIOA1 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 9 101: Level 10 110: Level 11 111: Level 12	RW	1
2:0	GPIOA0	GPIOA0 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 9 101: Level 10 110: Level 11 111: Level 12	RW	1

13.8.4 PADDRV1

PAD Drive Control Register 1
Offset=0x74

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	-	-
23:21	GPIOA17	GPIOA17 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x3
20:18	GPIOA16	GPIOA16 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1
17:15	GPIOA15	GPIOA15 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1
14:12	GPIOA14	GPIOA14 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1
11:9	GPIOA13	GPIOA13 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1
8:6	GPIOA12	GPIOA12 PAD Drive Control 000: Level 1 001: Level 2	RW	1

		010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8		
5:3	GPIOA11	GPIOA11 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1
2:0	GPIOA10	GPIOA10 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1

13.8.5 PADDRV2

PAD Drive Control Register 2
Offset=0x78

Bit (s)	Name	Description	Access	Reset
31:30	-	Reserved	-	-
29:27	GPIOA29	GPIOA29 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x7
26:24	GPIOA28	GPIOA28 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x7
23:12	-	Reserved	-	-
11:9	GPIOA23	GPIOA23 PAD Drive Control 000: Level 1 001: Level 2	RW	1

		010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8		
8:6	GPIOA22	GPIOA22 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1
5:3	GPIOA21	GPIOA21 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1
2:0	GPIOA20	GPIOA20 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1

13.8.6 PADDRV3

PAD Drive Control Register 3
Offset = 0x7C

Bit (s)	Name	Description	Access	Reset
31:27	-	Reserved	-	-
26:24	GPIOB9	GPIOB9 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1
23:21	GPIOB8	GPIOB8 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3	RW	1

		011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8		
20:18	GPIOB7	GPIOB7 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	1
17:0	-	Reserved	-	-

13.8.7 PADDRV4

PAD Drive Control Register 4
Offset = 0x40

Bit (s)	Name	Description	Access	Reset
31:30	SPIBT_SS	SPIBT_SS PAD Drive Control 00: Level 1 01: Level 2 10: Level 4 11: Level 8	RW	0x3
29:28	SPIBT_CLK	SPIBT_CLK PAD Drive Control 00: Level 1 01: Level 2 10: Level 4 11: Level 8	RW	0x3
27:26	SPIBT_MOSI	SPIBT_MOSI PAD Drive Control 00: Level 1 01: Level 2 10: Level 4 11: Level 8	RW	0x3
25:24	SPIBT_MISO	SPIBT_MISO PAD Drive Control 00: Level 1 01: Level 2 10: Level 4 11: Level 8	RW	0x3
23:21	GPIOA31	GPIOA31 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x7
20:15	-	Reserved	-	-
14:12	GPIOB11	GPIOB11 PAD Drive Control 000: Level 1	RW	0x1

		001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8		
11:9	SIO9	SIO9 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x1
8:6	SIO8	SIO8 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x1
5:3	SIO7	SIO7 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x1
2:0	SIO6	SIO6 PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	RW	0x1

13.9 LED Register Description

13.9.1 LED_SEG_RC_EN

LED SEG Enhancement Enable
Offset=0x8C

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	-	-

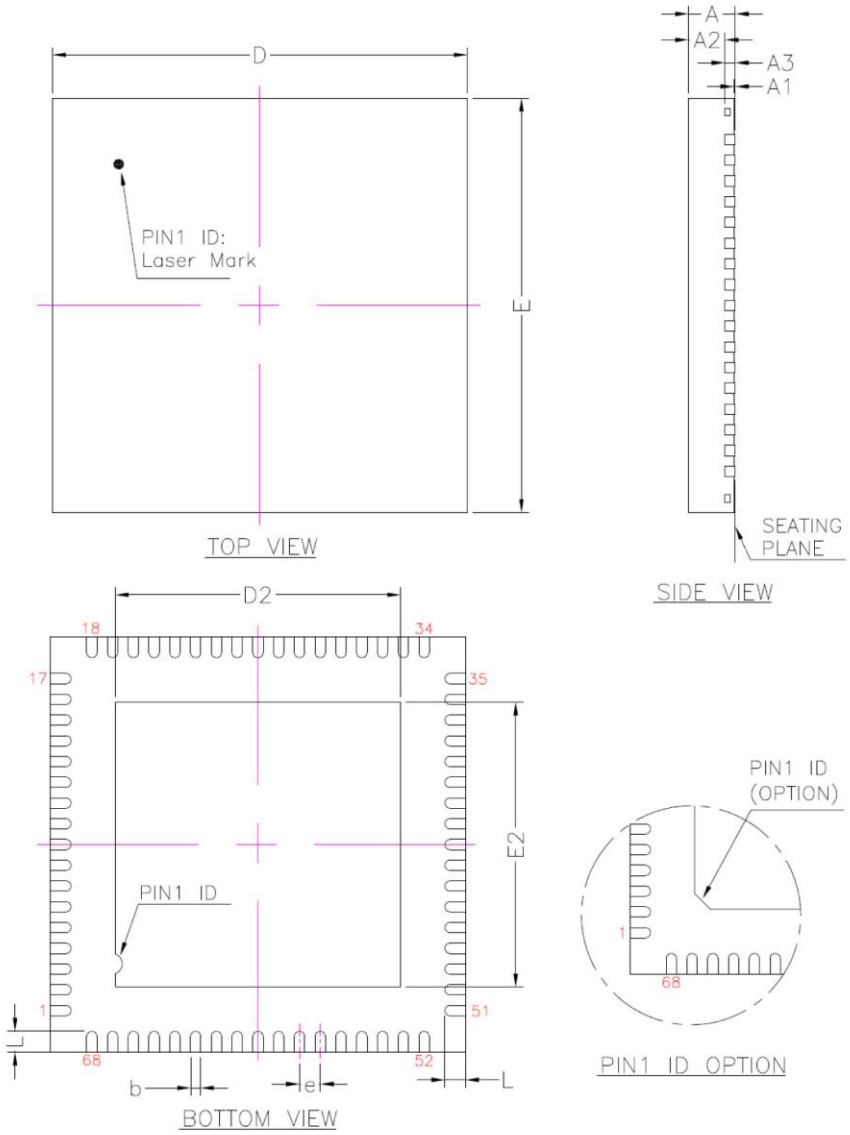
7	LED_SEG7	LED SEG7 Enhancement Enable	RW	0
6	LED_SEG6	LED SEG6 Enhancement Enable	RW	0
5	LED_SEG5	LED SEG5 Enhancement Enable	RW	0
4	LED_SEG4	LED SEG4 Enhancement Enable	RW	0
3	LED_SEG3	LED SEG3 Enhancement Enable	RW	0
2	LED_SEG2	LED SEG2 Enhancement Enable	RW	0
1	LED_SEG1	LED SEG1 Enhancement Enable	RW	0
0	LED_SEG0	LED SEG0 Enhancement Enable	RW	0

13.9.2 LED_SEG_BIAS_EN

LED SEG Bias Enable
Offset=0x90

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	-	-
3	LED_SEG_ALL_EN	LED SEG Enhancement ALL Enable 0:Disable 1:Enable	RW	0
2	LED_CATHODE_ANODE_MODE	LED Cathode/Anode Mode 0: Cathode Mode 1: Anode Mode	RW	0
1:0	LED_SEG_BIAS	LED SEG BIAS: 00:level 1 01: level 2 10: level 311: level 4 *Note: Level 4 is the brightest level.*	RW	1

14 Package and Drawings



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	---	0.65	0.70	---	0.026	0.028
A_3		0.2 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		8.00 BSC			0.315 BSC	
D_2/E_2	5.25	5.50	5.75	0.207	0.217	0.227
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Figure 14-1 ATS2825 Package and Dimension

15 Electrical Characteristics

15.1 Absolute Maximum Ratings

Table 15-1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Temperature	Tamb	TBD	TBD	°C
Storage temperature	Tstg	-55	+150	°C
ESD Stress voltage	Vesd (Human body model)	2000	-	V
Supply Voltage	DC5V	-0.3	9	V
	BAT	-0.3	5	V
	VCC/AVCC/BTVCC	-0.3	3.6	V
	VDD	-0.3	1.32	V
Input Voltage	3.3V IO	-0.3	3.6	V
	1.2V IO	-0.3	1.32	V

Note:
Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.

15.2 Recommended PWR Supply

Table 15-2 Recommended PWR Supply

Supply Voltage	Min	Typ	Max	Unit
BAT (Li)	3.4	3.8	4.3	V
DC5V	4.5	5.0	7.0	V
VCC/AVCC/BTVCC	2.8	3.1	3.4	V
VDD/RTCVDD/AVDD	1.08	1.2	1.32	V

Note:
1) *According to different application, the VDD can be setting different voltage. For optimum CPU performance, the VDD should be higher than 1.2V; for reduced the PWR consumption, the VDD can supply with 1.0V.*
2) *If the system is supply with Li-BAT, the range of DC5V would be 3.3V~4.2V; or the supply source of system is come from DC5V, DC5V would be 4.5V~5.2V.*

15.3 DC Characteristics

Table 15-3 DC Parameters for +3.3V IO Pin with Schmitt Trigger Off

Parameter	Symbol	Min.	Max.	Unit	Condition
Low-level input voltage	VIL	-	0.8	V	VCC = 3.1V Tamb = -10 to 70 °C
High-level input voltage	VIH	2.0	-	V	
Low-level output voltage	VOL	-	0.4	V	
High-level output voltage	VOH	2.4	-	V	

Table 15-4 DC Parameter for +3.3V IO Pin with Schmitt Trigger On

Parameter	Symbol	Min.	Max.	Unit	Condition
Schmitt trigger positive-going threshold	VT+	-	1.9	V	VCC=3.1V Tamb = -10 to

Schmitt trigger negative-going threshold	VT-	1.2	-	V	70 °C

15.4 PWR Consumption

Table 15-5 PWR Consumption Table

VDD = 1.2V @ Tamb unless otherwise specified

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
A2DP	Ct	Peak Current	-	-	18	mA
HFP	Cr	Receive Current	-	-	19	mA
Sniff Mode	Cs	500ms	-	-	800	uA
Deep Sleep	Cd	Vbat = 3.8V	35	-	50	uA

15.5 Bluetooth Characteristics

15.5.1 Transmitter

Table 15-6 Basic Data Rate of Transmitter

VDD = 1.2V @ 25°C

Parameter	Condition	Min.	Typ.	Max.	Unit
Maximum RF Transmit PWR	-	-	8[1]	-	dBm
RF PWR Control Range	-	-	20	-	dB
20dB Bandwidth for Modulated Carrier	-	-	900	-	KHz
Adjacent Channel Transmit	+2 MHz	-	-	-20	dBm
	-2 MHz	-	-	-20	dBm
	+3 MHz	-	-	-40	dBm
	-3 MHz	-	-	-40	dBm
Frequency Deviation	Δf1avg Maximum Modulation	-	169	-	KHz
	Δf2max Maximum Modulation	-	126	-	KHz
	Δf1avg/Δf2avg	-	0.9	-	
Initial Carrier Frequency Tolerance	-	-75	-	75	KHz
Frequency Drift	HD1 Packet	-25	-	25	KHz
	HD3 Packet	-40	-	40	KHz
	HD5 Packet	-40	-	40	KHz
Frequency Drift Rate	-	-20	-	20	KHz/50us
Harmonic Content	-	-	-50	-	dBm

[1] The maximum RF transmit PWR could reach to 8dBm with appropriate settings.

Table 15-7 Enhanced Data Rate of Transmitter

Core Supply Voltage = 1.2V @ 25°C

Parameter	Condition	Min.	Typ.	Max.	Unit
Relative Transmit PWR	-	-	-0.8	-	dB
π/4 DQPSK max carrier frequency stability $\|\omega_0\|$	-	-10	-	10	KHz
π/4 DQPSK max carrier frequency stability $\|\omega_i\|$	-	-75	-	75	KHz
π/4 DQPSK max carrier frequency stability $\|\omega_0+\omega_i\|$	-	-75	-	75	KHz

8DPSK max carrier frequency stability|ω_0|	-	-10	-	10	KHz
8DPSK max carrier frequency stability|ω_i|	-	-75	-	75	KHz
8DPSK max carrier frequency stability|$\omega_0+\omega_i$|	-	-75	-	75	KHz
π/4 DQPSK Modulation Accuracy	RMS DEVIN	-	-	20	%
	99% DEVM	99	-	-	%
	Peak DEVM	-	-	35	%
8DPSK Modulation Accuracy	RMS DEVIN	-	-	13	%
	99% DEVM	99	-	-	%
	Peak DEVM	-	-	25	%
In-band spurious emissions	F > F0 + 3MHz	-	-	-40	dBm
	F < F0 - 3MHz	-	-	-40	dBm
	F = F0 + 3MHz	-	-	-40	dBm
	F = F0 - 3MHz	-	-	-40	dBm
	F = F0 + 2MHz	-	-	-20	dBm
	F = F0 - 2MHz	-	-	-20	dBm
	F = F0 + 1MHz	-	-	-26	dB
	F = F0 - 1MHz	-	-	-26	dB
EDR Differential Phase Encoding	-	99	-	-	%

[1] The maximum RF transmit PWR could reach to 8dBm with appropriate settings.

15.5.2 Receiver

Table 15-8 Basic Data Rate of Receiver

Core Supply Voltage = 1.2V @ 25°C

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity at 0.1% BER	2.404GHz	-	-93	-	dBm
	2.441GHz	-	-93	-	dBm
	2.480GHz	-	-92	-	dBm
Maximum Input PWR at 0.1% BER	-	-20	-	-	dBm
Co-Channel Interface	-	-	-	11	dB
Adjacent Channel Selectivity C/I	F = F_0 + 1MHz	-	-	0	dB
	F = F_0 - 1MHz	-	-	0	dB
	F = F_0 + 2MHz	-	-	-30	dB
	F = F_0 - 2MHz	-	-	-20	dB
	F = F_0 + 3MHz	-	-	-40	dB
	F = F_{image}	-	-	-9	dB
Maximum Level of Intermodulation Interface	-	-39	-	-	dBm
Blocking @ Pin = -67dBm with 0.1% BER	30-2000 MHz	-10	-	-	dBm
	2000-2400 MHz	-27	-	-	dBm
	2500-3000 MHz	-27	-	-	dBm
	3000-12750 MHz	-10	-	-	dBm

Table 15-9 Enhanced Data Rate of Receiver

Core Supply Voltage = 1.2V @ 25°C

Parameter	Condition	Min.	Typ.	Max.	Unit
Sensitivity at 0.01% BER	π/4 DQPSK		-93		dBm
	8DPSK		-85		dBm
Maximum Input PWR at 0.1% BER	π/4 DQPSK	-20			dBm
	8DPSK	-20			dBm
Co-Channel Interference	π/4 DQPSK			13	dB

	8DPSK				21	dB
Adjacent Channel Selectivity C/I	$F = F_0 + 1MHz$	π/4 DQPSK		0		dB
		8DPSK		5		dB
	$F = F_0 - 1MHz$	π/4 DQPSK		0		dB
		8DPSK		5		dB
	$F = F_0 + 2MHz$	π/4 DQPSK		-30		dB
		8DPSK		-25		dB
	$F = F_0 - 2MHz$	π/4 DQPSK		-20		dB
		8DPSK		-13		dB
	$F = F_0 + 3MHz$	π/4 DQPSK		-40		dB
		8DPSK		-33		dB
	$F = F_{image}$	π/4 DQPSK		-7		dB
		8DPSK		0		dB

15.6 Audio ADC

Table 15-10 Audio ADC Parameters

Pre-Amplifier						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Full Scale Input Voltage	THD+N < 1%		-	-	2.8	Vpp
Analogue gain	AUX OP	-	-12	-	6	dB
	MIC OP	Single Ended	-6	-	32	dB
		Full Differential	0	-	38	
Analogue to Digital Converter						
Resolution	-		-	-	16	Bits
Input Sample Rate	-		8	-	48	kHz
SNR	fin = 1kHz@Full Scale Input Voltage B/W = 22Hz~22kHz Fs=48kHz		-	90	-	dB
Dynamic Range	fin = 1kHz@-40dBFS Input Voltage B/W = 22Hz~22kHz Fs=48kHz		-	90	-	dB
THD+N	fin = 1kHz(input=1.6Vpp) B/W = 22Hz~22kHz Fs=48kHz		-	-82	-	dB
Digital gain	-		0	-	12	dB

15.7 Stereo DAC

Table 15-11 Stereo DAC Parameters

Digital to Analogue Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	-		-	-	20	Bits
Output Sample Rate	-		8	-	48	kHz
SNR	fin = 1kHz@0dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω	-	-	98	-	dB
		A-Weighting	-	101	-	dB

Dynamic Range	fin = 1kHz@-48dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω	-	-	98	-	dB
		A-Weighting	-	101	-	dB
THD+N	fin = 1kHz@0dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω	-	-	-87	-	dB
Digital gain	-		<-60	-	24	dB
Stereo crosstalk	fin = 1kHz@0dBFS input	-	-	-78	-	dB
PWR Amplifier						
Analogue gain	-		-60	-	0	dB
Max Amplitude/PWR	fin = 1kHz@0dBFS input Fs=48kHz,Load=16Ω	Single Ended Output	-	-	550	mVrms
			-	-	18.5	mW
	fin = 1kHz@0dBFS input Fs=48kHz,Load=16Ω	Full Differential Output	-	-	60	mW
	fin = 1kHz@0dBFS input Fs=48kHz,Load=10KΩ	Full Differential Output	-	-	1.8	Vrms

Acronyms and Abbreviations

Abbreviations	Descriptions
AEC	acoustic echo cancellers
AXI	AMBA Advanced extensible Interface
ADC	Analog-to-Digital-Converter
ALU	Arithmetic Logic Unit
CC	Constant Current
CP0	Control Coprocessor 0
UDI	CorExtend® User Defined Instructions
DAC	Digital-to-Analog-Converter
DMA	Direct Memory Access
ER	Error Resilience
FMT	Fixed Mapping Translation
FSM	Flash State Machine
GPIO	General Purpose Input Output
GPRs	general-purpose registers
HOSC	High Frequency OSC (24MHz)
INTC	Interrupt Controller
IRQ	Interrupt Request
LED	Light Emitting Diode
LCD	Liquid Crystal Display
LTP	Long Term Predictor (added in MPEG-4)
LOSC	Low Frequency OSC, include internal RC OSC (about 32K) and external LOSC (32.768K)
LFPLL	Low Frequency source PLL
Matrix_led	Matrix LED (7-pin LED)
MIC	Microphone
MMU	Memory Management Unit
MFP	Multiple Function PAD
MDU	Multiply-Divide Unit
NMI	Nonmaskable Interrupt
OSC	Oscillator
PNS	Perceptual Noise Substitution (added in MPEG-4)
PA	PWR Amplifier
Seg-lcd	Segment LCD
SIE	Serial Interface Engine
SBR	Spectral band replication
TKC	Touch Key Controller
TLB	translation lookaside buffer
UTMI	USB Transceiver Macro Interface
WMA	Windows Media Audio

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