MT2503A SOC Processor Data Sheet

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Specifications are subject to change without notice.

Document Revision History

Revision	Date	Author	Description
0.1	2015-10-08	Sharon Chu	Initial draft

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Lists of Tables and Figures

1 System Overview

MT2503A is a monolithic chip integrating leading edge power management unit, analog baseband and radio circuitry based on the low-power CMOS process.

MT2503A is a feature-rich and extremely powerful single-chip solution for high-end GSM/GPRS capability. Based on the 32-bit ARM7EJ-S™ RISC processor, MT2503A's superb processing power, along with high bandwidth architecture and dedicated hardware support, provides a platform for high-performance GPRS Class 12 MODEM application and leading-edge multimedia applications.

MT2503A also features:

- A highly integrated Bluetooth transceiver which is fully compliant with Bluetooth specification v3.0.
- A FM receiver supporting both audio broadcast de-modulation and RDS/RBDS data decoding.

Typical application diagram is shown in **Figure 1**.

Platform

MT2503A is capable of running the ARM7EJ-S™ RISC processor, which provides the best trade-off between system performance and power consumption.

For large amounts of data transfer, high-performance DMA (Direct Memory Access) with hardware flow control is implemented, which greatly enhances the data movement speed while reducing the MCU processing load.

Targeted as a media-rich platform for mobile applications, MT2503A also provides hardware security digital rights management for copyright protection. For further safeguard and to protect the manufacturer's development investment, hardware flash content protection is provided to prevent unauthorized porting of the software load.

Memory

MT2503A supports serial flash interface with various operating frequencies.

Multimedia

The MT2503A multimedia subsystem provides serial interface for CMOS sensors. The camera resolution is up to VGA size. The software-based codec can be used to process various video types. To take advantage of the high MCU performance, GIF and PNG decoders are implemented by the software.

In addition, MT2503A is implemented with a high-performance audio synthesis technology, as well as a high-quality audio amplifier to provide superior audio experiences.

Connectivity and storage

MT2503A supports UART, USB 1.1 FS/LS , SDIO and SD storage systems. These interfaces provide MT2503A users with the highest level of flexibility in implementing high-end solutions.

To achieve a complete user interface, MT2503A also brings together all the necessary peripheral blocks for a multimedia GSM/GPRS phone. The peripheral blocks include the keypad scanner with the capability to detect multiple key presses, SIM controller, real-time clock, PWM, serial LCD

controller and general-purpose programmable I/Os.

Audio

Using a highly integrated mixed-signal audio front-end, the MT2503A architecture provides easy audio interfacing with direct connection to the audio transducers. The audio interface integrates A/D converters for voice band, as well as high-resolution stereo D/A converters for both audio and voice band.

MT2503A supports AMR codec to adaptively optimize the quality of speech and audio. Moreover, HE-AAC codec is implemented to deliver CD-quality audio at low bit rates.

In addition, an 1.2W audio amplifier is also embedded to save the BOM cost of adopting external amplifiers.

GSM/GPRS radio

MT2503A integrates a mixed-signal baseband front-end in order to provide a well-organized radio interface with flexibility for efficient customization. The front-end contains gain and offset calibration mechanisms and filters with programmable coefficients for comprehensive compatibility control on RF modules. MT2503A achieves outstanding MODEM performance by utilizing a highly dynamic range ADC in the RF downlink path.

MT2503A embeds a high-performance and completely integrated single-ended SAW-less RF transceiver for multi-band GSM cellular system. In this RF transceiver, a quad-band receiving feature with high sensitivity is supported utilizing one RF receiver and a fully integrated channel filter. With ultra-high dynamic range, the off-chip balun and SAW filters on the receiving path can be removed for BOM cost reduction. In addition, the minimum component count is guaranteed by realizing a highly integrated transmitter, low-spur frequency synthesizer and a Digitally-Controlled Crystal Oscillator (DCXO).

GPS

A high-performance single-chip multi-GNSS solution which includes on-chip CMOS RF, digital baseband, ARM7 CPU and an embedded NOR flash. It is able to achieve the industry's highest level of sensitivity, accuracy and Time-to-First-Fix (TTFF) with the lowest power consumption in a small-footprint lead-free package. Its small footprint and minimal BOM requirement provide significant reductions in the design, manufacturing and testing resource required for portable applications.

With built-in LNA to reach total receiver chain NF to 2.2 dB, you can eliminate antenna requirement and do not need external LNA. It also up to 12 multi-tone active interference cancellers (ISSCC2011 award) offer you more flexibility in system design.

MT2503A acquires and tracks satellites in the shortest time even at indoor signal levels. In addition, MT2503A supports various location and navigation applications, including autonomous GPS, GLONASS, GALILEO, BEIDOU(after ICD released), SBAS ranging (WAAS, EGNOS, GAGAN, and MSAS), QZSS, DGPS (RTCM) and AGPS.

Bluetooth radio

MT2503A offers a highly integrated Bluetooth radio and baseband processor. Only a minimum of external components are required. MT2503A provides superior sensitivity and class 1 output power and thus ensures the quality of the

connection with a wide range of Bluetooth devices.

MT2503A is fully compliant with Bluetooth v3.0 and offers enhanced data rates of up to 3Mbps. It also provides the coexistence protocol with 802.11 system.

MT2503A supports rich Bluetooth profiles, enabling diversified applications that are widely used on the handset with excellent interoperability.

FM radio

The FM radio subsystem provides a completely integrated FM Rx receiver supporting 65 ~ 108MHz FM bands with 50kHz tuning step. In addition to receiving FM audio broadcasting, the digital RDS/RBDS data system is supported as well. The integrated FM transceiver utilizes state-of-the-art digital demodulation/modulation techniques to achieve excellent performance.

In order to achieve high SINAD, good sensitivity and excellent noise suppression, the FM receiver adopts adaptive demodulation scheme to optimize Rx system performance in all ranges of signal quality by reference of a very sophisticated channel quality index (CQI). When the received signal quality is poor, the design not only enhances the ACI rejection capability but also uses a very ingenious skill to soft mute annoying noise so as to provide good perception quality.

The FM radio subsystem supports both long antenna, which is usually an earphone, and auto-calibrated short antenna, which is usually a FPC short antenna or shared antenna with GSM for different application scenarios.

Debugging function

The JTAG interface enables in-circuit debugging of the software program with the ARM7EJ-S™ core. With this standardized debugging interface, MT2503A provides developers with a wide set of options in choosing ARM development kits from different third party vendors.

Power management

A power management is embedded in MT2503A to provide rich features a high-end feature phone supports, including Li-ion battery charger, high performance and low quiescent current LDOs, and drivers for LED and backlight.

MT2503A offers various low-power features to help reduce the system power consumption. MT2503A is also fabricated in an advanced low-power CMOS process, hence providing an overall ultra-low leakage solution.

Package

The MT2503A device is offered in a 8.4mm*6.2mm, 215-ball, 0.4mm pitch, TFBGA package.

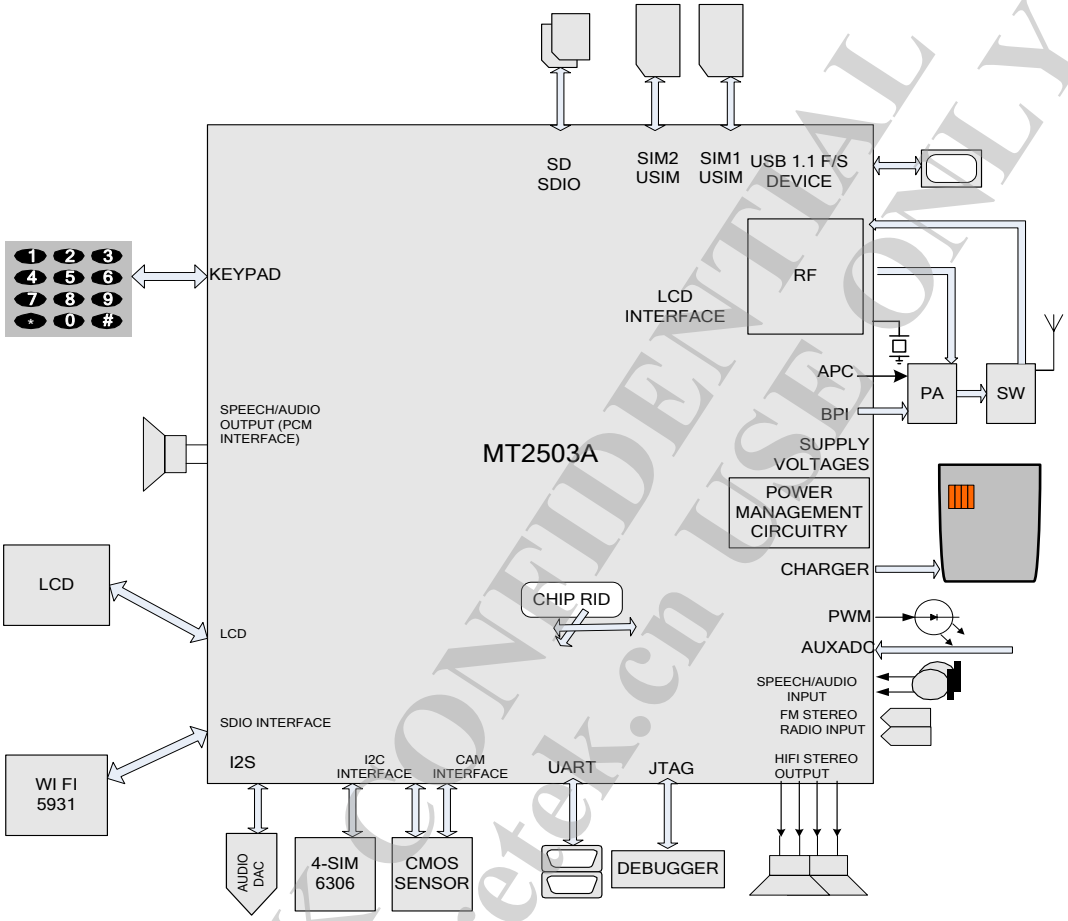


Figure 1. Typical application of MT2503A

1.1 Platform Features

General

- Integrated voice-band, audio-band and base-band analog front-end
- Integrated full-featured power management unit

MCU subsystem

- ARM7EJ-S™ 32-bit RISC processor
- Java hardware acceleration for fast Java-based games and applets
- High-performance multi-layer AHB bus
- Dedicated DMA bus with 16 DMA channels
- On-chip boot ROM for factory flash programming
- Watchdog timer for system crash recovery
- 3 sets of general-purpose timers
- Division coprocessor

User interfaces

- 5-row x 5-column keypad controller with hardware scanner
- Supports multiple key presses for gaming
- Dual SIM/USIM controller with hardware T = 0/T = 1 protocol control
- Real-time clock (RTC) operating with a low-quiescent-current power supply
- General-purpose I/Os (GPIOs) available for auxiliary applications
- 2 sets of Pulse Width Modulation (PWM) output
- 24 external interrupt lines
- 1 external channel auxiliary 10-bit A/D converter

Security

- Supports security key and chip random ID

Connectivity

- 3 UARTs with hardware flow control and supports baud rate up to 921,600 bps
- FS/LS USB 1.1 device controller
- Multimedia card, secure digital Memory Card, host controller with flexible I/O voltage power
- Supports 4-bit SDIO interface for SDIO peripherals as well as WIFI connectivity
- DAI/PCM and I2S interface for audio applications
- I2C master interface for peripheral management including image sensors
- SPI master/slave interface for peripheral management.

Power management

- Li-ion battery charger
- 13 LDOs for the power supply of memory card, camera, Bluetooth, RF, SIM card and other diversified usage
- 1 open-drain output switches to supply/control the LED
- LDO type vibrator
- One NMOS switch to control keypad LED
- Thermal overload protection
- Under-voltage lock-out protection
- Over-voltage protection
- Different levels of power-down modes with sophisticated software control enables excellent power saving performance.

Test and debugging

- Built-in digital and analog loop back modes for both audio and baseband front-end

- DAI port complies with GSM Rec.11.10.
- JTAG port for debugging embedded MCU

1.2 MODEM Features

Radio interface and baseband front-end

- Digital PM data path with baseband front-end
- High dynamic range delta-sigma ADC converts the downlink analog I and Q signals to digital baseband.
- 10-bit D/A converter for Automatic Power Control (APC)
- Programmable radio Rx filter with adaptive gain control
- Dedicated Rx filter for FB acquisition
- 6-pin Baseband Parallel Interface (BPI) with programmable driving strength
- Supports multi-band

Voice and modem CODEC

- Dial tone generation
- Voice memo
- Noise reduction
- Echo suppression
- Advanced sidetone oscillation reduction
- Digital sidetone generator with programmable gain
- Two programmable acoustic compensation filters
- Supports GSM/GPRS modem
- GSM quad vocoders for adaptive multirate (AMR), enhanced full rate (EFR), full rate (FR) and half rate (HR)
- GSM channel coding, equalization and A5/1, A5/2 and A5/3 ciphering
- GPRS GEA1, GEA2 and GEA3 ciphering
- GPRS packet switched data with CS1/CS2/CS3/CS4 coding schemes
- GPRS Class 12
- Supports SAIC (single antenna interference cancellation) technology
- Supports VAMOS(Voice services over Adaptive Multi-user channels on One Slot) technology in R9 spec.

Voice interface and voice front-end

- Microphone input has one low-noise amplifier with programmable gain and Automatic Gain Control (AGC) mechanisms
- Voice power amplifier with programmable gain
- 2nd order Sigma-Delta A/D converter for voice uplink path
- Shares D/A converter with audio playback path
- Supports full-duplex hands-free operation
- Compliant with GSM 03.50

1.3 GSM/GPRS RF Features

Receiver

- Dual single-ended LNAs support Quad bandQuadrature RF mixer
- Fully integrated channel filter
- High dynamic range ADC
- 12dB PGA gain with 6dB gain step

Transmitter

- Transmitter outputs support quad bands.
- Highly precise and low noise RF transmitter for GSM/GPRS applications

Frequency synthesizer

- Programmable fractional-N synthesizer
- Integrated wide range RFVCO
- Integrated loop filter
- Fast settling time suitable for multi-slot GPRS applications

Digitally-Controlled Crystal Oscillator (DCXO)

- Two-pin 26MHz crystal oscillator
- On-chip programmable capacitor array for coarse-tuning
- On-chip programmable capacitor array for fine-tuning
- Low power mode supports 32K crystal removal

1.4 Multimedia Features

LCD controller

- Supports simultaneous connection to seral 2 lane LCD modules
- LCM formats supported: RGB565, RGB666, RGB888
- Supports LCD module with maximum resolution up to 320x240
- Per pixel alpha channel
- True color engine
- Supports hardware display rotation
- Capable of combining display memories with up to 4 blending layers

Camera interface

- YUV422 format image input
- Capable of processing image of size up to VGA (Mediatek serial interface)

JPEG decoder

- Baseline JPEG decoding
- Supports various YUV formats, DC/AC Huffman tables and quantization tables

JPEG encoder

- ISO/IEC 10918-1 JPEG baseline mode
- ISO/IEC 10918-2 compliance
- Supports YUV420 and grayscale formats
- Supports EXIF/JFIF
- Standard DC and AC Huffman tables
- Provides 5 levels of encode quality
- Supports zeros shutter delay

MJPEG

- Decode spec: CIF@30fps
- Encode spec: QVGA@15fps

Image data processing

- Supports 4x digital zoom
- High throughput hardware scaler. Capable of tailoring an image to an arbitrary size.
- Horizontal scaling with bilinear interpolation
- Vertical scaling with bilinear interpolation
- YUV and RGB color space conversion
- RGB/YCbCr format thumbnail output

MPEG-4/H.263 CODEC

- Software-based MPEG4 encoder
- Software-based MPEG4 decoder
- ISO/IEC 14496-2 simple profile:
  - Decode spec: 480x320@25fps
  - Encode spec: QVGA@15fps
- ISO/IEC 14496-2 advanced simple profile:
  - Decode @ level 0/1/2/3
  - ITU-T H.263 profile 0 @ level 40
- Supports visual tools for decoder: I-VOP, P-VOP, B-VOP, AC/DC prediction, 4-MV, unrestricted MV, error resilience, short header, global motion compensation, method 1/2 quantization, quarter-pel motion compensation.
- Error resilience for decoder: Slice resynchronization, data partitioning, reversible VLC
- Supports visual tools for encoder: I-VOP, P-VOP, Half-Pel, DC prediction, unrestricted MV, short header

H.264

- ISO/IEC 14496-10 baseline profile
  - Decode spec: QCIF@30fps

2D accelerator

- Supports 32-bpp ARGB8888, 24-bpp RGB888, 16-bpp RGB565, 24-bpp ARGB6666.

- 4 layers overlay with individual color format, window size, source key, constant alpha and rotation
- Rectangle fill with constant
- BitBlt: Capable with 7 rotation types
- Alpha blending with 7 rotation types, per-pixel alpha and pre-multiplied alpha
- Font drawing: Normal font and anti-aliasing font

Audio CODEC

- Supports AAC codec decoding
- Wavetable synthesis with up to 64 tones
- Advanced wavetable synthesizer capable of generating simulated stereo
- Wavetable including GM full set of 128 instruments and 47 sets of percussions
- PCM playback and record
- Digital audio playback

Audio interface and audio front-end

- Supports I2S interface
- High-resolution D/A converters for stereo audio playback
- Voice band A/D converter support
- Stereo to mono conversion

1.5 Bluetooth Features

Radio features

- Fully compliant with Bluetooth specification 3.0
- Low out-of-band spurious emissions support simultaneous operation with GPS and GSM/GPRS worldwide radio systems
- Low-IF architecture with high degree of linearity and high order channel filter
- Integrated T/R switch and Balun
- Fully integrated PA provides 7.5dBm output power
- -95dBm sensitivity with excellent interference rejection performance
- Hardware AGC dynamically adjusts receiver performance in changing environments

Baseband features

- Up to 4 simultaneous active ACL links
- Up to 1 simultaneous SCO or eSCO link with CVSD coding
- Supports eSCO
- Scatternet support: Up to 4 piconets simultaneously with background inquiry/page scan
- Supports sniff mode
- AFH and PTA collaborative support for WLAN/BT coexistence
- Idle mode and sleep mode enables ultra-low power consumption.
- Supports PCM interface and built-in programmable transcoders for linear voice with re-transmission
- Built-in hardware modem engine for access code correlation, header error correction, forward error correction, CRC, whitening and encryption
- Channel quality driven data rate adaptation
- Channel assessment for AFH

Platform features

- Embedded processor for Bluetooth protocol stack with built-in memory system
- Fully verified ROM based system with code patch for feature enhancement

1.6 FM Features

- 65-108MHz worldwide FM bands with 50KHz tuning step
- Supports RDS/RBDS radio data system
- Digital stereo demodulator
- Adaptive FM demodulator for both high- and low-quality scenarios
- Low sensitivity level with superior interference rejection
- Programmable de-emphasis (bypass/50 S/75 S)
- Stereophonic multiplex signal (MPX) signal detection and demodulation
- Superior stereo noise reduction and soft mute volume control
- Audio dynamic range control
- Mono/stereo blending
- Audio sensitivity3dBμVemf (SINAD=26dB)
- Audio SINAD≥60dB
- Supports Anti-jamming algorithm
- Supports short antenna

1.7 GPS feature

Specifications

- GPS/GLONASS/GALILEO/BEIDOU(after ICD released) receiver
- Supports multi-GNSS incl. QZSS, SBAS ranging
- Supports WAAS/EGNOS/MSAS/GAGAN
- 12 multi-tone active interference cancellers (ISSCC2011 award)
- RTCM ready
- Indoor and outdoor multi-path detection and compensation
- Supports FCC E911 compliance and A-GPS
- Max. fixed update rate up to 10 Hz

Advanced software features

- AlwaysLocateTM advanced location awareness technology
- EPOTM/HotStillTM orbit prediction
- EASYTM self-generated orbit prediction
- Supports logger function
- Supports time service application which can be achieved by PPS VS. NMEA feature.

Reference oscillator

- TCXO
  Frequency: 16.368 MHz, 12.6 ~ 40.0 MHz
  Frequency variation: ±2.5 ppm
- Crystal
  Frequency: 26 MHz, 12.6 ~ 40.0 MHz
  Frequency accuracy: ±10 ppm

RF configuration

- SoC, integrated in single chip with CMOS process

ARM7EJ-S CPU

- Up to 158 MHz processor clock
- Dynamic clock rate control

Pulse-per-second (PPS) GPS time reference

- Adjustable duty cycle
- Typical accuracy: ±10 ns

Power scheme

- A 1.8 volts SMPS build-in SOC
- Direct lithium battery connection (2.8 ~ 4.3 volts)
- Self build 1.1 volts RTC LDO, 1.1 volts core LDO, and 2.8 volts TCXO LDO

Build-in reset controller

- Does not need external reset control IC

Internal real-time clock (RTC)

- 32.768 KHz ± 20 ppm crystal
- 1.1 volts RTC clock output
- Supports external pin to wake up

Backup mode

- A Force_On pin to ease backup mode application circuit

Serial interface

- 3 UARTs
- SPI, I2C
- GPIO interface (up to 16 pins)

NMEA

- NMEA 0183 standard V4.1 and backward compliance
- Supports 219 different data

Superior sensitivities

- Acq.: -148 dBm (cold) / -163 dBm (hot)
- Tracking: -165 dBm

Ultra-low power consumption (GPS+GLONASS)

- Acquisition: 37 mW
- Tracking: 27 mW
- AlwaysLocateTM: 3.0 mW

Slim hardware design

- 9 passive external components
- Single RF Front-End for Multi-GNSS frequency bands

1.8 General Descriptions

Figure 2 is the block diagram of MT2503A. Based on a multi-processor architecture, MT2503A integrates an ARM7EJ-S™ core, the main processor running high-level GSM protocol software as well as multimedia applications, single digital signal processor core, which manages the low-level MODEM and advanced audio functions, an embedded processor running Bluetooth baseband and link control protocol and the Bluetooth radio control.

MT2503A consists of the following subsystems:

- Microcontroller Unit (MCU) subsystem: Includes an ARM7EJ-S™ RISC processor and its accompanying memory management and interrupt handling logics
- Digital Signal Processor (DSP) subsystem: Includes a DSP and its accompanying memory, memory controller and interrupt controller
- MCU/DSP interface: Junction at which the MCU and the DSP exchange hardware and software information
- Microcontroller peripherals: Include all user interface modules and RF control interface modules
- Microcontroller coprocessors: Run computing-intensive processes in place of the microcontroller
- DSP peripherals: Hardware accelerators for GSM/GPRS channel codec
- Multimedia subsystem: Integrates several advanced accelerators to support multimedia applications
- Voice front-end: Data path for converting analog speech to and from digital speech
- Audio front-end: Data path for converting stereo audio from an audio source
- Baseband front-end: Data path for converting a digital signal to and from an analog signal from the RF modules
- Timing generator: Generates the control signals related to the TDMA frame timing
- Power, reset and clock subsystem: Manage the power, reset and clock distribution inside MT2503A.
- Bluetooth subsystem: Includes an embedded processor with embedded ROM/RAM system, baseband processor, and a high-performance radio block
- Power management unit: Self-contained power supply source which also controls the charging and system startup circuitry.

Details of the individual subsystems and blocks are described in the following chapters.

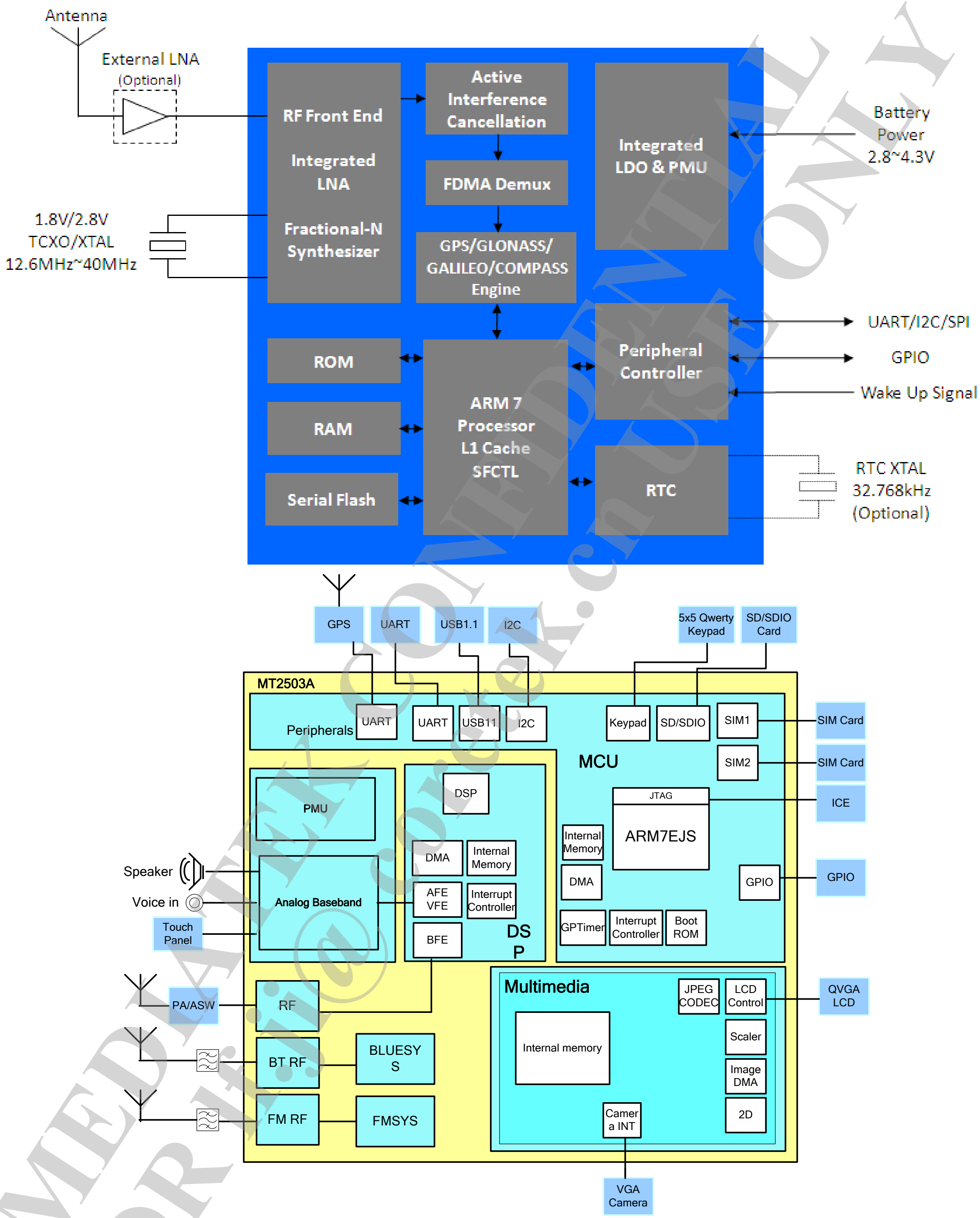


Figure 2. MT2503A block diagram

2 Product Descriptions

2.1 Pin Description

2.1.1 Ball Diagram

For MT2503A, an TFBGA 8.4mm*6.2mm, 215-ball, 0.4mm pitch package is offered. Pin-outs and the top view are illustrated in **Figure 3** for this package.

215	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	RXLB	AVSS_2GHF	SRCLKENAI		AVSS_2GHF	BT_LNA		VIO28		BPI_BUS2		SCL28	CMRST		CMMCLK	CMCSD0	GPS_XIN	GPS_XOUT	GPS_AVDD43_RTC	GPS_AVDD43_DCV	A
B	RXHB	TX_LB	AVSS_2GHF	XTAL1	XTAL2	AVSS_2GHF	AVDD15_BTRF	BPI_BUS1		BPI_BUS0	VDDK	SDA28	GPIO_3	GPIO_2	CMCSD1	CMCSK		GPS_DVSS11_CORE	GPS_DCV_FB	GPS_AVSS11_CLDO	B
C		TX_HB	EINT		FREF			KCOL1	KROW1	KROW2			GPIO_0		CMPDN	GPS_DVDD11_CORE1	GPS_FORCE_ON		GPS_DCV	GPS_AVSS43_DCV	C
D	VRF	AVSS_2GHF	GPIO_10	GPIO_11	BKT_CLK_SEL		KROW0	KROW3	KCOL3		KCOL4	SPSWP	SPSIN	GPIO_1	SPSCS0	GPS_32K_OUT	GPS_AVDD11_RTC		GPS_AVDD11_CLDO		D
E	VBAT_VA	AVSS44_ALDO	VCAMA	TESTMODE	KCOL0	KCOL2	UTXD1	URXD1	KROW4	SPSHOLD	SPSCK	SPSOUT					GPS_DVDD28_SF	GPS_TX1	GPS_AVDD28_TLDO	GPS_AVDD28_CLDO	E
F		FM_ANT_P		PWRKEY	GND	GND							GPS_DVSS11_CORE	GPS_DVSS11_CORE	GPS_DVSS28_SF		GPS_JCK		GPS_AVDD_TCXO_SW		F
G	VREF	AVSS_FM	CHRLDO	BATON	GND	GND	GND	GND	GND	GND			GPS_DVSS11_CORE	GPS_DVSS11_CORE	GPS_DVSS11_CORE	GPS_DVSS11_CORE	GPS_TX2	GPS_RX1	GPS_AVDD43_VBAT	GPS_AVSS43_MISC	G
H	BATSNS	ISENSE	VCDT	KPLED	GND	GND	GND	GND	GND	GND	GND		GPS_DVSS11_CORE	GPS_DVSS11_CORE	GPS_DVSS11_CORE	GPS_DVSS11_CORE	GPS_DVSS28_IO	GPS_DVDD28_IO1	GPS_VREF		H
J		DRV		AUXIN4	GND	GND	GND	GND	GND	GND	GND	VSF	GPS_DVSS11_CORE	GPS_DVSS11_CORE		GPS_SCK1	GPS_DVDD11_CORE2		GPS_AVDD18_CM	GPS_OSC	J
K		ISINK	AVSS44_PMU	AVSS44_PMU	GND		LSCK	MCCM0	MCDA1	MCCK						GPS_RX0	GPS_RX2		GPS_T1P	GPS_T1N	K
L	AVSS44_BOOST	AVSS44_BOOST	AU_HPL	ACCDET	LSCE_B	TESTMODE_D	RESETB	LPTE		MCDA0	MCDA3	VMC	VSIM2	GPS_JRST_			GPS_JDI	GPS_DVDD28_IO2	GPS_HRST_B		L
M	AVDD_SPK	AU_HPR	AVSS28_ABB	AU_VIN0_P	AU_VIN0_N		LSA0	LSDA		MCDA2			SIM2_SCLK	SIM2_SRST		GPS_TX0	GPS_JRCK	GPS_SCS1_	GPS_XTEST	GPS_AVSS_RF	M
N	SPK_OUTN	AVSS_SPK	AU_HSP	AU_HSN	AU_VIN1_N	AU_MICBIAS0	APC	AVSS44_DLDO	VIBR	VUSB	VIO18	VIO18	SIM2_SIO	SIM1_SIO	SIM1_SRST	GPS_JDO	GPS_EINT0	GPS_EINT1	GPS_AVSS_RF	GPS_RFIN	N
P	SPK_OUTP	AVSS_SPK	VA		AU_VIN1_P		VRTC	VCORE		VBAT_DIGITAL		USB11_DP	USB11_DM		VSIM1	SIM1_SCLK	GPS_JMS		GPS_AVDD18_RXFE	GPS_AVSS_RF	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 3. Ball diagram and top view

2.1.2 Pin Coordination

Table 1. Pin coordinates

Pin#	Net name	Pin#	Net name	Pin#	Net name
A1	RXLB	**E12**	SFSOUT	**K9**	MCDA1
A2	AVSS_2GHF	**E17**	GPS_DVDD28_SF	**K10**	MCCK
A3	SRCLKENAI	**E18**	GPS_TX1	**K16**	GPS_RX0
A5	AVSS_2GHF	**E19**	GPS_AVDD28_TLDO	**K17**	GPS_RX2
A6	BT_LNA	**E20**	GPS_AVDD28_CLDO	**K19**	GPS_T1P

Pin#	Net name	Pin#	Net name	Pin#	Net name
A8	VIO28	F2	FM_ANT_P	K20	GPS_T1N
A10	BPI_BUS2	F4	PWRKEY	L1	AVSS44_BOOST
A12	SCL28	F5	GND	L2	AVSS44_BOOST
A13	CMRST	F6	GND	L3	AU_HPL
A15	CMMCLK	F13	GPS_DVSS11_CORE	L4	ACCDET
A16	CMCSD0	F14	GPS_DVSS11_CORE	L5	LSCE_B
A17	GPS_XIN	F15	GPS_DVSS28_SF	L6	TESTMODE_D
A18	GPS_XOUT	F17	GPS_JCK	L7	RESETB
A19	GPS_AVDD43_RTC	F19	GPS_AVDD_TCXO_SW	L8	LPTE
A20	GPS_AVDD43_DCV	G1	VREF	L10	MCDA0
B1	RXHB	G2	AVSS_FM	L11	MCDA3
B2	TX_LB	G3	CHRLDO	L12	VMC
B3	AVSS_2GHF	G4	BATON	L13	VSIM2
B4	XTAL1	G5	GND	L14	GPS_JRST_
B5	XTAL2	G6	GND	L17	GPS_JDI
B6	AVSS_2GHF	G7	GND	L18	GPS_DVDD28_IO2
B7	AVDD15_BTRF	G8	GND	L19	GPS_HRST_B
B8	BPI_BUS1	G9	GND	M1	AVDD_SPK
B10	BPI_BUS0	G10	GND	M2	AU_HPR
B11	VDDK	G13	GPS_DVSS11_CORE	M3	AVSS28_ABB
B12	SDA28	G14	GPS_DVSS11_CORE	M4	AU_VIN0_P
B13	GPIO_3	G15	GPS_DVSS11_CORE	M5	AU_VIN0_N
B14	GPIO_2	G16	GPS_DVSS11_CORE	M7	LSA0
B15	CMCSD1	G17	GPS_TX2	M8	LSDA
B16	CMCSK	G18	GPS_RX1	M11	MCDA2
B18	GPS_DVSS11_CORE	G19	GPS_AVDD43_VBAT	M13	SIM2_SCLK
B19	GPS_DCV_FB	G20	GPS_AVSS43_MISC	M14	SIM2_SRST
B20	GPS_AVSS11_CLDO	H1	BATSNS	M16	GPS_TX0
C2	TX_HB	H2	ISENSE	M17	GPS_JRCK
C3	EINT	H3	VCDT	M18	GPS_SCS1_
C5	FREF	H4	KPLED	M19	GPS_XTEST
C8	KCOL1	H5	GND	M20	GPS_AVSS_RF
C9	KROW1	H6	GND	N1	SPK_OUTN
C10	KROW2	H7	GND	N2	AVSS_SPK
C13	GPIO_0	H8	GND	N3	AU_HSP
C15	CMPDN	H9	GND	N4	AU_HSN
C16	GPS_DVDD11_CORE1	H10	GND	N5	AU_VIN1_N
C17	GPS_FORCE_ON	H11	GND	N6	AU_MICBIAS0

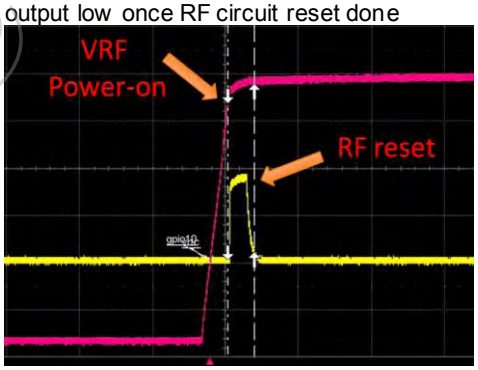
Pin#	Net name	Pin#	Net name	Pin#	Net name
C19	GPS_DCV	H13	GPS_DVSS11_CORE	N7	APC
C20	GPS_AVSS43_DCV	H14	GPS_DVSS11_CORE	N8	AVSS44_DLDO
D1	VRF	H15	GPS_DVSS11_CORE	N9	VIBR
D2	AVSS_2GHF	H16	GPS_DVSS11_CORE	N10	VUSB
D3	GPIO_10	H17	GPS_DVSS28_IO	N11	VIO18
D4	GPIO_11	H18	GPS_DVDD28_IO1	N12	VIO18
D5	EXT_CLK_SEL	H19	GPS_VREF	N13	SIM2_SIO
D7	KROW0	J2	DRV	N14	SIM1_SIO
D8	KROW3	J4	AUXIN4	N15	SIM1_SRST
D9	KCOL3	J5	GND	N16	GPS_JDO
D11	KCOL4	J6	GND	N17	GPS_EINT0
D12	SFSWP	J7	GND	N18	GPS_EINT1
D13	SFSIN	J8	GND	N19	GPS_AVSS_RF
D14	GPIO_1	J9	GND	N20	GPS_RFIN
D15	SFSCS0	J10	GND	P1	SPK_OUTP
D16	GPS_32K_OUT	J11	GND	P2	AVSS_SPK
D17	GPS_AVDD11_RTC	J12	VSF	P3	VA
D19	GPS_AVDD11_CLDO	J13	GPS_DVSS11_CORE	P5	AU_VIN1_P
E1	VBAT_VA	J14	GPS_DVSS11_CORE	P7	VRTC
E2	AVSS44_ALDO	J16	GPS_SCK1	P8	VCORE
E3	VCAMA	J17	GPS_DVDD11_CORE2	P10	VBAT_DIGITAL
E4	TESTMODE	J19	GPS_AVDD18_CM	P12	USB11_DP
E5	KCOL0	J20	GPS_OSC	P13	USB11_DM
E6	KCOL2	K2	ISINK	P15	VSIM1
E7	UTXD1	K3	AVSS44_PMU	P16	SIM1_SCLK
E8	URXD1	K4	AVSS44_PMU	P17	GPS_JMS
E9	KROW4	K5	GND	P19	GPS_AVDD18_RXFE
E10	SFSHOLD	K7	LSCK	P20	GPS_AVSS_RF
E11	SFSCK	K8	MCCM0		

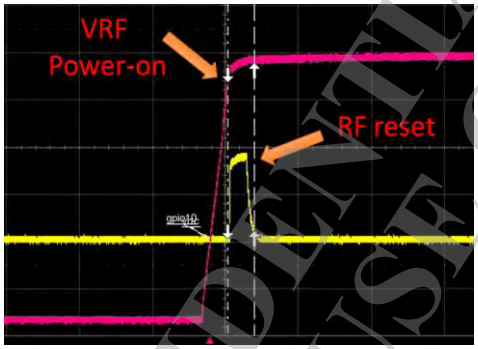
2.1.3 Detailed Pin Description

Table 2. Acronym for pin types

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 3. PIN function description and power domain

Pin name	Type	Description	Power domain
System			
RESETB	DIO	System reset	DVDD18_EMI
SRCLKENAI	DIO	26MHz clock request by external devices	VRF
EINT	DIO	External Interrupt	VRF
TESTMODE_D	DIO	Digital Test Mode	DVDD18_EMI
GPIO_0	DIO	General purpose input /output 0	DVDD28
GPIO_1	DIO	General purpose input /output 1	DVDD28
GPIO_2	DIO	General purpose input /output 2	DVDD28
GPIO_3	DIO	General purpose input /output 3	DVDD28
GPIO_10	DIO	General purpose input /output 10, with analog output function, please be notified that this GPIO may temporarily output high signal after VRF power-on then output low once RF circuit reset done 	VRF

Pin name	Type	Description	Power domain
GPIO_11	DIO	General purpose input /output 11, with analog output function, please be notified that this GPIO temporarily output high signal after VRF power-on then output low once RF circuit reset done 	VRF
RF control circuitro			
BPI_BUS0	DIO	RF hard-wire control bus bit 0	DVDD28
BPI_BUS1	DIO	RF hard-wire control bus bit 1	DVDD28
BPI_BUS2	DIO	RF hard-wire control bus bit 2	DVDD28
UART interface			
URXD1	DIO	UART1 receive data	DVDD28
UTXD1	DIO	UART1 transmit data	DVDD28
Keypad interface			
KCOL0	DIO	Keypad column 0	DVDD28
KCOL1	DIO	Keypad column 1	DVDD28
KCOL2	DIO	Keypad column 2	DVDD28
KCOL3	DIO	Keypad column 3	DVDD28
KCOL4	DIO	Keypad column 4	DVDD28
KROW0	DIO	Keypad row 0	DVDD28
KROW1	DIO	Keypad row 1	DVDD28
KROW2	DIO	Keypad row 2	DVDD28
KROW3	DIO	Keypad row 3	DVDD28
KROW4	DIO	Keypad row 4	DVDD28
Serial Flash interface			
SFSWP	DIO	Serial Flash Interface	DVDD28_SF
SFSIN	DIO	Serial Flash Interface	DVDD28_SF
SFSCS0	DIO	Serial Flash Interface	DVDD28_SF
SFSHOLD	DIO	Serial Flash Interface	DVDD28_SF
SFSCK	DIO	Serial Flash Interface	DVDD28_SF
SFSOUT	DIO	Serial Flash Interface	DVDD28_SF
Camera interface			
CMRST	DIO	CMOS sensor reset signal output	DVDD28
CMPDN	DIO	CMOS sensor power down control	DVDD28
CMCSD0	DIO	CMOS sensor data input 0	DVDD28

Pin name	Type	Description	Power domain
CMCSD1	DIO	CMOS sensor data input 1	DVDD28
CMMCLK	DIO	CMOS sensor pixel clock input	DVDD28
CMCSK	DIO	CMOS sensor pixel clock output	DVDD28
MS/SD card interface			
MCDA0	DIO	SD serial data IO 0/memory stick serial data IO	DVDD33_MSDC
MCDA1	DIO	SD serial data IO 1/memory stick serial data IO	DVDD33_MSDC
MCDA2	DIO	SD serial data IO 2/memory stick serial data IO	DVDD33_MSDC
MCDA3	DIO	SD serial data IO 3/memory stick serial data IO	DVDD33_MSDC
MCCK	DIO	SD serial clock/memory stick serial clock	DVDD33_MSDC
MCCM0	DIO	SD command output/memory stick bus state output	DVDD33_MSDC
SIM card interface			
SIM1_SIO	DIO	SIM1 data input/outputs	VSIM1
SIM1_SRST	DIO	SIM1 card reset output	VSIM1
SIM1_SCLK	DIO	SIM1 card clock output	VSIM1
SIM2_SIO	DIO	SIM2 data input/outputs	VSIM2
SIM2_SRST	DIO	SIM2 card reset output	VSIM2
SIM2_SCLK	DIO	SIM2 card clock output	VSIM2
I2C interface			
SCL28	DIO	I2C clock 2.8v power domain	DVDD28
SDA28	DIO	I2C data 2.8v power domain	DVDD28
LCD interface			
LSCE_B	DIO	Serial display interface chip select output	DVDD18_EMI
LSCK	DIO	Serial display interface clock	DVDD18_EMI
LSDA	DIO	Serial display interface data	DVDD18_EMI
LSA0	DIO	Serial display interface address	DVDD18_EMI
LPTE	DIO	Serial display tearing signal	DVDD18_EMI
FM			
FM_ANT_P	AI	FM input from antenna	VCAMA
Bluetooth			
BT_LNA	AIO	Bluetooth RF single-ended input	DVDD28
2G RF			
RXHB	AI	RF input for highband Rx (DCS/PCS)	VRF
RXLB	AI	RF input for low band Rx (GSM900/GSM850)	VRF
TX_HB	AO	RF output for highband Tx (DCS/PCS)	VRF
TX_LB	AO	RF output pin for low band Tx (GSM900/GSM850)	VRF
FREF	AO	DCXO reference clock output	VRF
XTAL1	AIO	Input 1 for DCXO crystal	VRF

Pin name	Type	Description	Power domain
XTAL2	AIO	Input 2 for DCXO crystal	VRF
EXT_CLK_SEL	AIO	DCXO mode selection	VRF
USB			
USB11_DM	AIO	D- data input/output	-
USB11_DP	AIO	D+ data input/output	-
GPS			
GPS_RFIN	RF signal	LNA RF Input pin	
GPS_XIN	Analog input	RTC 32KHz XTAL input	
GPS_XOUT	Analog output	RTC 32KHz XTAL output	
GPS_AVDD43_RTC	Analog power	RTC LDO input	
GPS_AVDD43_DCV	SMPS	SMPS input pin.	
GPS_DVSS11_CORE	Digital ground	Digital 1.1V core ground	
GPS_DCV_FB	SMPS	SMPS feedback pin	
GPS_AVSS11_CLDO	Analog ground	GND pin for core LDO	
GPS_DVDD11_CORE1	Digital power	Digital 1.1V core power input	
GPS_FORCE_ON	1.2V LVTTL input PPU,PPD, SMT	Logic high to force power on this chip. Default: pull-up	
GPS_DCV	SMPS	SMPS output pin	
GPS_AVSS43_DCV	SMPS	SMPS GND pin	
GPS_32K_OUT	1.2V LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	RTC domain GPIO pin, can be programmed to 32KHz clock output or DR wake-up signal input Default: pull-down Default: 16mA driving	
GPS_AVDD11_RTC	Analog power	RTC LDO output	
GPS_AVDD11_CLDO	Analog power	Core LDO output pin	
GPS_DVDD28_SF	Digital power	Digital 2.8V serial flash power input	

Pin name	Type	Description	Power domain
GPS_TX1	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial output for UART 1 Default: pull-up Default: 8mA driving	
GPS_AVDD28_TLDO	Analog power	TCXO LDO output pin	
GPS_AVDD28_CLDO	Analog power	Core LDO input pin. Always powered by external source or SMPS	
GPS_DVSS28_SF	Digital ground	Digital 2.8V serial flash ground	
GPS_JCK	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial input for UART 1 Default: pull-up Default: 8mA driving	
GPS_AVDD_TCXO_SW	Analog power	TCXO power switch output pin	
GPS_TX2	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial output for UART 2 Default: pull-up Default: 8mA driving Strap pin tcxo_sw_sel 1'b0: AVDD_TCXO_SW output 1.8V 1'b1: AVDD_TCXO_SW output 2.8V	
GPS_RX1	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial input for UART 1 Default: pull-up Default: 8mA driving	

Pin name	Type	Description	Power domain
GPS_AVDD43_VBAT	Analog power	TCXO LDO input pin. Always be powered by external source. UVLO will detect this PIN to check power status.	
GPS_AVSS43_MISC	Analog ground	GND pin for buck controller, TCXO LDO and start-up block	
GPS_DVSS28_IO	Digital ground	Digital 1.8/2.8V IO ground	
GPS_DVDD28_IO1	Digital power	Digital 1.8/2.8V IO power input	
GPS_VREF	Analog	Bandgap output pin. Must add 1uF decoupling cap on EVB.	
GPS_SCK1	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	SPI clock output Default: pull-up Default: 8mA driving Strap pin clk_sel[0] **Clk_sel[1:0] Mode** 2'b00: XTAL mode 2'b01: External clock mode 2'b10: TCXO mode 2'b11: 16.368MHz TCXO mode	
GPS_DVDD11_CORE2	Digital power	Digital 1.1V core power input	
GPS_AVDD18_CM	RF power	1.8V supply for XTAL OSC, bandgap, thermal sensor and level shifter	
GPS_OSC	Analog signal	Input for crystal oscillator or TCXO	
GPS_RX0	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial input for UART 0 Default: pull-up Default: 8mA driving	
GPS_RX2	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial input for UART 2 Default: pull-up Default: 8mA driving	

Pin name	Type	Description	Power domain
GPS_T1P	Analog signal	RF testing signal	
GPS_T1N	Analog signal	RF testing signal	
GPS_JRST_	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	SPI slave selection 1 Default: pull-up Default: 8mA driving Strap pin clk_sel[1]	
GPS_JDI	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	JTAG interface data input. Default: pull-down Default: 8mA driving	
GPS_DVDD28_IO2	Digital power	Digital 1.8/2.8V IO power input	
GPS_HRST_B	2.8V LVTTL input SMT	System reset. Active low Default: pull-up	
GPS_TX0	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial output for UART 0 Default: pull-up Default: 8mA driving	

Pin name	Type	Description	Power domain
GPS_JRCK	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	SPI clock output Default: pull-up Default: 8mA driving Strap pin clk_sel[0] **Clk_sel[1:0] Mode** 2'b00: XTAL mode 2'b01: External clock mode 2'b10: TCXO mode 2'b11: 16.368MHz TCXO mode	
GPS_SCS1_	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	SPI slave selection 1 Default: pull-up Default: 8mA driving Strap pin clk_sel[1]	
GPS_XTEST	2.8V LVTTL input SMT	Test mode. *Must keep low in normal mode.* Default: pull-down	
GPS_AVSS_RF	RF ground	RF ground pins	
GPS_JDO	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial output for UART 2 Default: pull-up Default: 8mA driving Strap pin tcxo_sw_sel 1'b0: AVDD_TCXO_SW output 1.8V 1'b1: AVDD_TCXO_SW output 2.8V	
GPS_EINT0	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	External interrupt 0 Default: pull-down Default: 8mA driving	

Pin name	Type	Description	Power domain
GPS_EINT1	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	External interrupt 1 Default: pull-down Default: 8mA driving	
GPS_AVSS_RF	RF ground	RF ground pins	
GPS_JMS	SMPS	SMPS GND pin	
GPS_AVDD18_RXFE	2.8V, LVTTL I/O PPU, PPD, SMT 4mA, 8mA, 12mA, 16mA PDR	Serial output for UART 1 Default: pull-up Default: 8mA driving	
Analog baseband			
AU_HPR	AIO	Audio head phone output (R channel)	AVDD28_ABB
AU_HPL	AIO	Audio head phone output (L channel)	AVDD28_ABB
AU_HSP	AIO	Voice handset output (positive)	AVDD28_ABB
AU_HSN	AIO	Voice handset output (negative)	AVDD28_ABB
AU_VIN0_P	AIO	Microphone 0 input (positive)	AVDD28_ABB
AU_VIN0_N	AIO	Microphone 0 input (negative)	AVDD28_ABB
AU_VIN1_P	AIO	Microphone 1 input (positive)	AVDD28_ABB
AU_VIN1_N	AIO	Microphone 1 input (negative)	AVDD28_ABB
AUX_IN4	AIO	Auxiliary ADC input	AVDD28_ABB
SPK_OUTP	AIO	Speaker positive output	VBAT_SPK
SPK_OUTN	AIO	Speaker negative output	VBAT_SPK
APC	AIO	Automatic power control DAC output	AVDD28_ABB
AU_MICBIAS0	AIO	Microphone bias source 0	AVDD28_ABB
ACCDET	AIO	Accessory detection	AVDD28_ABB
Power management unit			
VA	AIO	LDO output for ABB - VA	VBAT_ANALOG
VCAMA	AIO	LDO output for sensor – VCAMA	VBAT_VA
VIBR	AIO	LDO output for vibrator - VIBR	VBAT_DIGITAL
VIO18	AIO	LDO output for 1.8V power - VIO18	VBAT_DIGITAL
VIO28	AIO	LDO output for 2.8V power - VIO28	VBAT_DIGITAL

Pin name	Type	Description	Power domain
VMC	AIO	LDO output for memory card - VMC	VBAT_DIGITAL
VSF	AIO	LDO output - VSF	VBAT_DIGITAL
VRF	AIO	LDO output for GSMRF - VRF	VBAT_VA
VRTC	AIO	LDO output for RTC - VRTC	VBAT_DIGITAL
VSIM1	AIO	LDO output for 1st SIM - VSIM	VBAT_DIGITAL
VSIM2	AIO	LDO output for 2nd SIM - VSIM2	VBAT_DIGITAL
VUSB	AIO	LDO output for USB - VUSB	VBAT_DIGITAL
VCORE	AIO	LDO output for core circuit - Vcore	VBAT_DIGITAL
VREF	AIO	Band gap reference	BATSNS
VCDT	AIO	Charger-In level sense pin	BATSNS
DRV	AIO	IDAC current output open-drain pin	BATSNS
BATON	AIO	Battery Pack, NTC connected pin	BATSNS
ISENSE	AIO	Top node of current sensing 0.2ohm Rsense resistor	BATSNS
CHRLDO	AIO	2.8V shunt-regulator output	BATSNS
BATDET	AIO	Battery detection pin	BATSNS
ISINK0	AIO	Backlight driver channel 0	VBAT_VA
KPLED	AIO	Keypad led driver	VBAT_VA
TESTMODE	AIO	Test mode	BATSNS
PWRKEY	AIO	PWR key	BATSNS
AVDD25_V2P5	AIO	Reference voltage for ABT	-
Analog power			
AVDD15_BTRF	P	BTRF power input	-
VBAT_DIGITAL	P	Digital LDOs used battery voltage input	-
VBAT_VA	P	Analog LDOs used battery voltage input	-
AVDD_SPK	P	Input for loud speaker driver	-
BATSNS	P	Battery node of battery pack	-
AVDD15_BTRF	P	BTRF power input	-
Analog ground			
AVSS28_ABB	G	ABB 2.8V ground	-
AVSS_BT	G	BT ground	-
AVSS_2G	G	2G RF ground	-
AVSS_FM	G	FM ground	-
AVSS44_PMU	G	PMU ground	-
AVSS44_ALDO	G	ALDO ground	-
AVSS44_DLDO	G	DLDO ground	-
AVSS_SPK	G	SPK ground	-
AGND	G	GND for VREF	-
AVSS44_BOOST	G	Audio boost GND	-
Digital power			
VDDK	P	Core power	-
Digital ground			

Pin name	Type	Description	Power domain
GND	G	Ground	-

Table 4. Acronym for state of pins

Abbreviation	Description
I	Input
LO	Low output
HO	High output
LO	Low output
PU	Pull-up
PD	Pull-down
-	No PU/PD
0~N	Aux. function number
X	Delicate function pin

Table 5. State of pins

Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
System						
RESETB	HO	1	-	DIOH3/DIOL3	No need	IO Type 3
SRCLKENAI	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
EINT	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_0	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_1	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_2	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_3	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_4	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
GPIO_5	LO	0	PD	DIOH2/DIOL2	No need	IO Type 2
GPIO_6	LO	0	PD	DIOH2/DIOL2	No need	IO Type 2
GPIO_7	LO	0	PD	DIOH2/DIOL2	No need	IO Type 2
GPIO_8	I	0	PD	DIOH2/DIOL2	No need	IO Type 2

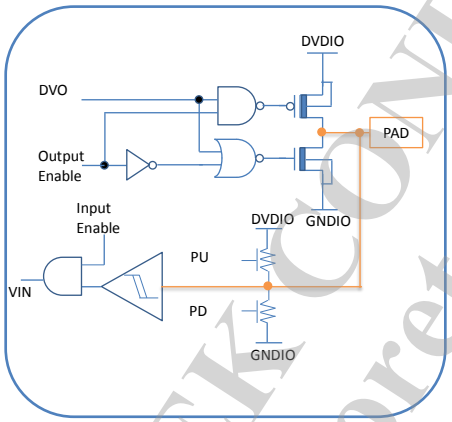
[1] The column "State" of "Reset" shows the pin state during reset. (Input, High Output, Low Output, etc)

[2] The column "Aux" for "Reset" means the default aux function number, shown in the table "Pin Multiplexing, Capability and Settings".

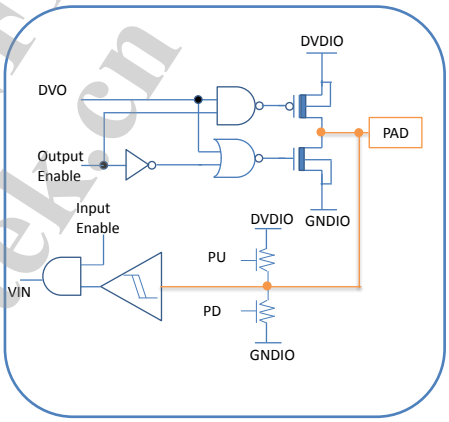
[3] The column "PU/PD" for "Reset" means if there is internal pull-up or pull-down when the pin is input in the reset state.

Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
GPIO_9	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
GPIO_10	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
GPIO_11	I	0	PD	DIOH1/DIOL1	No need	IO Type 1
RF control circuitry						
BPI_BUS0	LO	1	PD	DIOH2/DIOL2	No need	IO Type 2
BPI_BUS1	I	1	PD	DIOH2/DIOL2	No need	IO Type 2
BPI_BUS2	I	1	PD	DIOH2/DIOL2	No need	IO Type 2
UART interface						
URXD1	I	1	PU	DIOH3/DIOL3	No need	IO Type 3
UTXD1	HO	1	PU	DIOH2/DIOL2	No need	IO Type 2
Keypad Interface						
KCOL0	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KCOL1	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KCOL2	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KCOL3	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KCOL4	I	0	PU	DIOH4/DIOL4	No need	IO Type 4
KROW0	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
KROW1	I	0	PD	DIOH5/DIOL5	No need	IO Type 5
KROW2	I	0	PD	DIOH6/DIOL6	No need	IO Type 6
KROW3	I	0	PD	DIOH6/DIOL6	No need	IO Type 6
KROW4	I	0	PD	DIOH6/DIOL6	No need	IO Type 6
Camera interface						
CMRST	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
CMPDN	HO	0	-	DIOH3/DIOL3	No need	IO Type 3
CMCSD0	I	0	PU	DIOH3/DIOL3	No need	IO Type 3
CMCSD1	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
CMMCLK	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
CMCSK	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
MS/SD card interface						
MCDA0	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCDA1	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCDA2	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCDA3	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
MCCK	I	0	PU	DIOH3/DIOL3	No need	IO Type 3
MCCM0	I	0	PU	DIOH3/DIOL3	No need	IO Type 3
SIM card interface						
SIM1_SIO	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
SIM1_SRST	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
SIM1_SCLK	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
SIM2_SIO	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
SIM2_SRST	I	1	PD	DIOH6/DIOL6	No need	IO Type 6
SIM2_SCLK	I	1	PD	DIOH6/DIOL6	No need	IO Type 6

Name	Reset			Output drivability	Termination when not used	IO type
	State[1]	Aux[2]	PU/PD[3]			
I2C interface						
SCL28	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
SDA28	I	0	PD	DIOH2/DIOL2	No need	IO Type 2
LCD interface						
TESTMODE_D	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
LSCE_B	HO	1	-	DIOH3/DIOL3	No need	IO Type 3
LSCK	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
LSDA	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
LSA0	I	0	PD	DIOH3/DIOL3	No need	IO Type 3
LPTE	I	0	PD	DIOH3/DIOL3	No need	IO Type 3



IO type1



IO type2

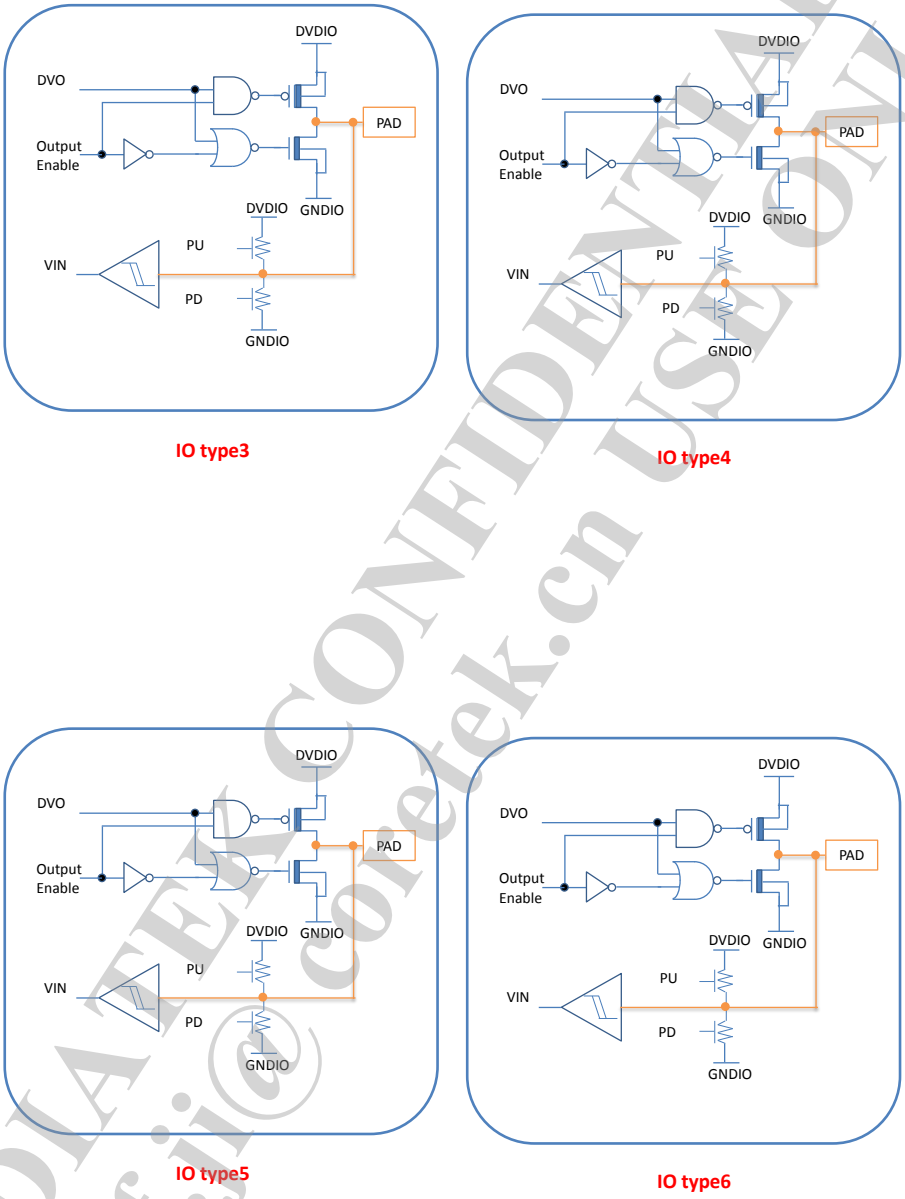


Figure 4. IO types in state of pins

2.1.4 Pin Multiplexing, Capability and Settings

Table 6. Acronym for pull-up and pull-down types

Abbreviation	Description
PU	Pull-up, not controllable
PD	Pull-down, not controllable
CU	Pull-up, controllable
CD	Pull-down, controllable
X	Cannot pull-up or pull-down

Table 7. Capability of PU/PD, driving and Schmitt trigger

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
GPIO_0	0	GPIO0	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT0	I	CU, CD	4, 8, 12, 16mA	0
	2	XP	AIO	-	4, 8, 12, 16mA	0
	3	U3RXD	I	CU, CD	4, 8, 12, 16mA	0
	4	CMCSD2	I	CU, CD	4, 8, 12, 16mA	0
	5	CMCSK	I	CU, CD	4, 8, 12, 16mA	0
	6	EDIDO	O	CU, CD	4, 8, 12, 16mA	0
	7	JTDI	I	PU	4, 8, 12, 16mA	0
	8	BTJTDI	I	CU, CD	4, 8, 12, 16mA	0
	9	FMJTDI	I	CU, CD	4, 8, 12, 16mA	0
GPIO_1	0	GPIO1	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT1	I	CU, CD	4, 8, 12, 16mA	0
	2	XM	AIO	-	4, 8, 12, 16mA	0
	3	U3TXD	O	CU, CD	4, 8, 12, 16mA	0
	4	U1CTS	I	CU, CD	4, 8, 12, 16mA	0
	5	CMMCLK	O	CU, CD	4, 8, 12, 16mA	0
	6	EDIDI	I	CU, CD	4, 8, 12, 16mA	0
	7	JTMS	I	PU	4, 8, 12, 16mA	0
	8	BTJTMS	I	CU, CD	4, 8, 12, 16mA	0
	9	FMJTMS	I	CU, CD	4, 8, 12, 16mA	0
GPIO_2	0	GPIO2	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT2	O	CU, CD	4, 8, 12, 16mA	0
	2	YP	AIO	-	4, 8, 12, 16mA	0
	3	GPSFSYNC	O	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	4	PWM0	O	CU, CD	4, 8, 12, 16mA	0
	5	CMCSD0	I	CU, CD	4, 8, 12, 16mA	0
	6	EDIWS	O	CU, CD	4, 8, 12, 16mA	0
	7	JTRST_B	I	PD	4, 8, 12, 16mA	0
	8	BTJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	9	FMJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
GPIO_3	0	GPIO3	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCINS	I	CU, CD	4, 8, 12, 16mA	0
	2	YM	AIO	-	4, 8, 12, 16mA	0
	4	PWM1	O	CU, CD	4, 8, 12, 16mA	0
	5	CMCSD1	I	CU, CD	4, 8, 12, 16mA	0
	6	EDICK	O	CU, CD	4, 8, 12, 16mA	0
	7	JTDO	O	CU, CD	4, 8, 12, 16mA	0
	8	BTJTDO	O	CU, CD	4, 8, 12, 16mA	0
	9	FMJTDO	O	CU, CD	4, 8, 12, 16mA	0
GPIO_4	0	GPIO4	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT3	I	CU, CD	4, 8, 12, 16mA	0
	4	U1RTS	O	CU, CD	4, 8, 12, 16mA	0
GPIO_5	0	GPIO5	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT4	I	CU, CD	4, 8, 12, 16mA	0
	3	BPI_BUS3	O	CU, CD	4, 8, 12, 16mA	0
GPIO_6	0	GPIO6	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT5	I	CU, CD	4, 8, 12, 16mA	0
	2	MCINS	I	CU, CD	4, 8, 12, 16mA	0
	3	BPI_BUS4	O	CU, CD	4, 8, 12, 16mA	0
GPIO_7	0	GPIO7	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT6	I	CU, CD	4, 8, 12, 16mA	0
	3	BPI_BUS5	O	CU, CD	4, 8, 12, 16mA	0
GPIO_8	0	GPIO8	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT7	I	CU, CD	4, 8, 12, 16mA	0
	2	SCL	IO	CU, CD	4, 8, 12, 16mA	0
GPIO_9	0	GPIO9	IO	CU, CD	4, 8, 12, 16mA	0
	1	EINT8	I	CU, CD	4, 8, 12, 16mA	0
	2	SDA	IO	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
URXD1	0	GPIO10	IO	CU, CD	4, 8, 12, 16mA	0
	1	U1RXD	I	PU	4, 8, 12, 16mA	0
	2	CMRST	O	CU, CD	4, 8, 12, 16mA	0
	3	EINT9	I	CU, CD	4, 8, 12, 16mA	0
	4	MCINS	I	CU, CD	4, 8, 12, 16mA	0
UTXD1	0	GPIO11	IO	CU, CD	4, 8, 12, 16mA	0
	1	U1TXD	O	CU, CD	4, 8, 12, 16mA	0
	2	CMPDN	O	CU, CD	4, 8, 12, 16mA	0
	3	EINT10	I	CU, CD	4, 8, 12, 16mA	0
KCOL4	0	GPIO12	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL4	IO	-	4, 8, 12, 16mA	0
	2	U2RXD	I	CU, CD	4, 8, 12, 16mA	0
	3	EDIDI	I	CU, CD	4, 8, 12, 16mA	0
	4	FMJTDI	I	CU, CD	4, 8, 12, 16mA	0
	5	JTDI	I	PU	4, 8, 12, 16mA	0
	6	BTJTDI	I	CU, CD	4, 8, 12, 16mA	0
KCOL3	0	GPIO13	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL3	IO	-	4, 8, 12, 16mA	0
	2	EINT11	I	CU, CD	4, 8, 12, 16mA	0
	3	PWM0	O	CU, CD	4, 8, 12, 16mA	0
	4	FMJTMS	I	CU, CD	4, 8, 12, 16mA	0
	5	JTMS	I	PU	4, 8, 12, 16mA	0
	6	BTJTMS	I	CU, CD	4, 8, 12, 16mA	0
KCOL2	0	GPIO14	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL2	IO	-	4, 8, 12, 16mA	0
	2	EINT12	I	CU, CD	4, 8, 12, 16mA	0
	3	U1RTS	I	CU, CD	4, 8, 12, 16mA	0
KCOL1	0	GPIO15	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL1	IO	-	4, 8, 12, 16mA	0
	2	GPSFSYNC	O	CU, CD	4, 8, 12, 16mA	0
	3	U1CTS	I	CU, CD	4, 8, 12, 16mA	0
	4	FMJTCK	I	CU, CD	4, 8, 12, 16mA	0
	5	JTCK	I	PU	4, 8, 12, 16mA	0
	6	BTJTCK	I	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
KCOL0	0	GPIO16	IO	CU, CD	4, 8, 12, 16mA	0
	1	KCOL0	IO	-	4, 8, 12, 16mA	0
KROW4	0	GPIO17	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW4	IO	-	4, 8, 12, 16mA	0
	2	U2TXD	O	CU, CD	4, 8, 12, 16mA	0
	3	EDICK	O	CU, CD	4, 8, 12, 16mA	0
KROW3	0	GPIO18	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW3	IO	-	4, 8, 12, 16mA	0
	2	EINT13	I	CU, CD	4, 8, 12, 16mA	0
	3	CLKO0	O	CU, CD	4, 8, 12, 16mA	0
	4	FMJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	5	JTRST_B	I	PD	4, 8, 12, 16mA	0
	6	BTJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
KROW2	0	GPIO19	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW2	IO	-	4, 8, 12, 16mA	0
	2	PWM1	O	CU, CD	4, 8, 12, 16mA	0
	3	EDIWS	O	CU, CD	4, 8, 12, 16mA	0
	4	FMJTDO	O	CU, CD	4, 8, 12, 16mA	0
	5	JTDO	O	CU, CD	4, 8, 12, 16mA	0
	6	BTJTDO	O	CU, CD	4, 8, 12, 16mA	0
KROW1	0	GPIO20	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW1	IO	-	4, 8, 12, 16mA	0
	2	EINT14	I	CU, CD	4, 8, 12, 16mA	0
	3	EDIDO	O	CU, CD	4, 8, 12, 16mA	0
	4	BTPRI	IO	CU, CD	4, 8, 12, 16mA	0
	5	JTRCK	O	CU, CD	4, 8, 12, 16mA	0
	6	BTDBGACKN	O	CU, CD	4, 8, 12, 16mA	0
KROW0	0	GPIO21	IO	CU, CD	4, 8, 12, 16mA	0
	1	KROW0	IO	-	4, 8, 12, 16mA	0
	5	MCINS	I	CU, CD	4, 8, 12, 16mA	0
	6	BTDBGIN	I	CU, CD	4, 8, 12, 16mA	0
BPI_BUS2	0	GPIO22	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPI_BUS2	O	CU, CD	4, 8, 12, 16mA	0
BPI_BUS1	0	GPIO23	IO	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	1	BPI_BUS1	O	CU, CD	4, 8, 12, 16mA	0
BPI_BUS0	0	GPIO24	IO	CU, CD	4, 8, 12, 16mA	0
	1	BPI_BUS0	IO	CU, CD	4, 8, 12, 16mA	0
CMRST	0	GPIO25	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMRST	O	CU, CD	4, 8, 12, 16mA	0
	2	TESTMODE_D	O	CU, CD	4, 8, 12, 16mA	0
	3	CLKO1	O	CU, CD	4, 8, 12, 16mA	0
	4	EINT15	I	CU, CD	4, 8, 12, 16mA	0
	5	FMJTDI	I	CU, CD	4, 8, 12, 16mA	0
	6	JTDI	I	PU	4, 8, 12, 16mA	0
CMPDN	0	GPIO26	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMPDN	O	CU, CD	4, 8, 12, 16mA	0
	2	LSCK1	O	CU, CD	4, 8, 12, 16mA	0
	3	DAICLK	O	CU, CD	4, 8, 12, 16mA	0
	4	SPICS	IO	CU, CD	4, 8, 12, 16mA	0
	5	FMJTMS	I	CU, CD	4, 8, 12, 16mA	0
	6	JTMS	I	PU	4, 8, 12, 16mA	0
CMCSD0	0	GPIO27	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMCSD0	I	CU, CD	4, 8, 12, 16mA	0
	2	LSCE_B1	O	CU, CD	4, 8, 12, 16mA	0
	3	DAIPCMIN	I	CU, CD	4, 8, 12, 16mA	0
	4	SPISCK	IO	CU, CD	4, 8, 12, 16mA	0
	5	FMJTCK	I	CU, CD	4, 8, 12, 16mA	0
	6	JTCK	I	PU	4, 8, 12, 16mA	0
	8	MC2CM0	O	-	4, 8, 12, 16mA	0
CMCSD1	0	GPIO28	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMCSD1	I	CU, CD	4, 8, 12, 16mA	0
	2	LSDA1	IO	CU, CD	4, 8, 12, 16mA	0
	3	DAIPCMOUT	O	CU, CD	4, 8, 12, 16mA	0
	4	SPIMOSI	IO	CU, CD	4, 8, 12, 16mA	0
	5	FMJTRSTB	I	CU, CD	4, 8, 12, 16mA	0
	6	JTRST_B	I	PD	4, 8, 12, 16mA	0
	8	MC2CK	O	-	4, 8, 12, 16mA	0
CMMCLK	0	GPIO29	IO	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	1	CMMCLK	O	CU, CD	4, 8, 12, 16mA	0
	2	LSA0DA1	O	CU, CD	4, 8, 12, 16mA	0
	3	DAISYNC	O	CU, CD	4, 8, 12, 16mA	0
	4	SPIMISO	IO	CU, CD	4, 8, 12, 16mA	0
	5	FMJTDO	O	CU, CD	4, 8, 12, 16mA	0
	6	JTDO	O	CU, CD	4, 8, 12, 16mA	0
	8	MC2DA0	IO	-	4, 8, 12, 16mA	0
CMCSK	0	GPIO30	IO	CU, CD	4, 8, 12, 16mA	0
	1	CMCSK	I	CU, CD	4, 8, 12, 16mA	0
	2	LPTE	I	CU, CD	4, 8, 12, 16mA	0
	3	CMCSD2	I	CU, CD	4, 8, 12, 16mA	0
	4	EINT16	I	CU, CD	4, 8, 12, 16mA	0
	6	JTRCK	O	CU, CD	4, 8, 12, 16mA	0
MCCK	0	GPIO31	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCCK	O	-	4, 8, 12, 16mA	0
	4	U2RXD	I	CU, CD	4, 8, 12, 16mA	0
MCCM0	0	GPIO32	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCCM0	IO	-	4, 8, 12, 16mA	0
	4	U2TXD	O	CU, CD	4, 8, 12, 16mA	0
MCDA0	0	GPIO33	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA0	IO	-	4, 8, 12, 16mA	0
	4	DAISYNC	O	CU, CD	4, 8, 12, 16mA	0
MCDA1	0	GPIO34	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA1	IO	-	4, 8, 12, 16mA	0
	2	EINT17	I	CU, CD	4, 8, 12, 16mA	0
	4	DAIPCMIN	I	CU, CD	4, 8, 12, 16mA	0
MCDA2	0	GPIO35	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA2	IO	-	4, 8, 12, 16mA	0
	2	EINT18	I	CU, CD	4, 8, 12, 16mA	0
	4	DAICLK	O	CU, CD	4, 8, 12, 16mA	0
MCDA3	0	GPIO36	IO	CU, CD	4, 8, 12, 16mA	0
	1	MCDA3	IO	-	4, 8, 12, 16mA	0
	2	EINT19	I	CU, CD	4, 8, 12, 16mA	0
	3	CLKO2	O	CU, CD	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	4	DAIPCMOUT	O	CU, CD	4, 8, 12, 16mA	0
SIM1_SIO	0	GPIO37	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM1_SIO	IO	-	2, 4, 6, 8mA	0
SIM1_SRST	0	GPIO38	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM1_SRST	IO	-	2, 4, 6, 8mA	0
SIM1_SCLK	0	GPIO39	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM1_SCLK	IO	-	2, 4, 6, 8mA	0
SIM2_SIO	0	GPIO40	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM2_SIO	IO	-	2, 4, 6, 8mA	0
	3	U2RTS	O	CU, CD	2, 4, 6, 8mA	0
SIM2_SRST	0	GPIO41	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM2_SRST	IO	-	2, 4, 6, 8mA	0
	2	CLKO3	O	CU, CD	2, 4, 6, 8mA	0
	3	U2CTS	I	CU, CD	2, 4, 6, 8mA	0
SIM2_SCLK	0	GPIO42	IO	CU, CD	2, 4, 6, 8mA	0
	1	SIM2_SCLK	IO	-	2, 4, 6, 8mA	0
	2	LSCE1_B1	O	CU, CD	2, 4, 6, 8mA	0
SCL	0	GPIO43	IO	CU, CD	4, 8, 12, 16mA	0
	1	SCL	IO	CU, CD	4, 8, 12, 16mA	0
SDA	0	GPIO44	IO	CU, CD	4, 8, 12, 16mA	0
	1	SDA	IO	CU, CD	4, 8, 12, 16mA	0
TESTMODE_D	0	GPIO45	IO	CU, CD	4, 8, 12, 16mA	0
	1	TESTMODE_D	O	CU, CD	4, 8, 12, 16mA	0
	3	CMRST	O	CU, CD	4, 8, 12, 16mA	0
LSCE_B0	0	GPIO46	IO	CU, CD	4, 8, 12, 16mA	0
	1	LSCE_B0	O	CU, CD	4, 8, 12, 16mA	0
	2	EINT20	I	CU, CD	4, 8, 12, 16mA	0
	3	CMCSD0	I	CU, CD	4, 8, 12, 16mA	0
	4	CLKO4	O	CU, CD	4, 8, 12, 16mA	0
LSCK0	0	GPIO47	IO	CU, CD	4, 8, 12, 16mA	0
	1	LSCK0	O	CU, CD	4, 8, 12, 16mA	0
	3	CMPDN	O	CU, CD	4, 8, 12, 16mA	0
LSDA0	0	GPIO48	IO	CU, CD	4, 8, 12, 16mA	0
	1	LSDA0	IO	-	4, 8, 12, 16mA	0

Name	Aux. function	Aux. name	Aux. type	PU/PD/ CU/CD	Driving	SMT
	2	EINT21	I	CU, CD	4, 8, 12, 16mA	0
	3	CMCSD1	I	CU, CD	4, 8, 12, 16mA	0
	4	WIFITOBT	I	CU, CD	4, 8, 12, 16mA	0
LSA0	0	GPIO49	IO	CU, CD	4, 8, 12, 16mA	0
	1	LSA0DA0	O	-	4, 8, 12, 16mA	0
	2	LSCE1_B0	O	CU, CD	4, 8, 12, 16mA	0
	3	CMMCLK	O	CU, CD	4, 8, 12, 16mA	0
LPTE	0	GPIO50	IO	CU, CD	4, 8, 12, 16mA	0
	1	LPTE	I	CU, CD	4, 8, 12, 16mA	0
	2	EINT22	I	CU, CD	4, 8, 12, 16mA	0
	3	CMCSK	I	CU, CD	4, 8, 12, 16mA	0
	4	CMCSD2	I	CU, CD	4, 8, 12, 16mA	0
	6	MCINS	I	CU, CD	4, 8, 12, 16mA	0
	9	CLKO5	O	CU, CD	4, 8, 12, 16mA	0
RESETB	0	GPIO51	IO	CU, CD	4, 8, 12, 16mA	0
	1	RESETB	IO	CU, CD	4, 8, 12, 16mA	0
EINT	0	AGPI52	I	CU, CD	8mA	0
	2	EINT23	I	CU, CD	8mA	0
SRCLKENAI	0	AGPI53	I	CU, CD	8mA	0
	1	SRCLKENAI	I	CU, CD	8mA	0
	2	EINT24	I	-	8mA	0
GPIO_10	0	AGPIO54	IO	CU, CD	8mA	0
GPIO_11	0	AGPIO55	IO	CU, CD	8mA	0

2.2 Electrical Characteristics

2.2.1 Absolute Maximum Ratings

Table 8. Absolute maximum ratings for power supply

Symbol or pin name	Description	Min.	Max.	Unit
VBAT_DIGITAL	Digital used battery voltage input	-0.3	+4.4	V
VBAT_VA	Analog used battery voltage input	-0.3	+4.4	V
AVDD_SPK	VBAT input for loud speaker driver	-0.3	+5.5	V
VDDK	1.3v core power	-0.3	+1.43	V

Table 9. Absolute maximum ratings for voltage input

Symbol or pin name	Description	Min.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	3.08	V
VIN2	Digital input voltage for IO Type 2	-0.3	3.08	V
VIN3	Digital input voltage for IO Type 3	-0.3	3.63	V
VIN4	Digital input voltage for IO Type 4	-0.3	3.08	V
VIN5	Digital input voltage for IO Type 5	-0.3	3.08	V
VIN6	Digital input voltage for IO Type 6	-0.3	3.08	V
VIN7	Digital input voltage for IO Type 7	-0.3	3.63	V

Table 10. Absolute maximum ratings for storage temperature

Symbol or pin name	Description	Min.	Max.	Unit
Tstg	Storage temperature	-55	125	°C

2.2.2 Recommended Operating Conditions

Table 11. Recommended operating conditions for power supply

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VBAT_DIGITAL	Digital used battery voltage input	3.4	3.8	4.2	V
VBAT_VA	Analog used battery voltage input	3.4	3.8	4.2	V
AVDD_SPK	VBAT input for loud speaker driver	3.4	3.8	4.2	V
VDDK	1.2v core power	1.17	1.3	1.43	V

Table 12. Recommended operating conditions for voltage input

Symbol or pin name	Description	Min.	Typ.	Max.	Unit
VIN1	Digital input voltage for IO Type 1	-0.3	-	DVDIO+0.3	V
VIN2	Digital input voltage for IO Type 2	-0.3	-	DVDIO+0.3	V
VIN3	Digital input voltage for IO Type 3	-0.3	-	DVDIO+0.3	V
VIN4	Digital input voltage for IO Type 4	-0.3	-	DVDIO+0.3	V
VIN5	Digital input voltage for IO Type 5	-0.3	-	DVDIO+0.3	V
VIN6	Digital input voltage for IO Type 6	-0.3	-	DVDIO+0.3	V
VIN7	Digital input voltage for IO Type 7	-0.3	-	DVDIO+0.3	V

Table 13. Recommended operating conditions for operating temperature

Symbol or pin name	Description	Min.	Typ	Max.	Unit
Tc	Operating temperature	-20	-	85	°C

2.2.3 Electrical Characteristics under Recommended Operating Conditions

Table 14. Electrical characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIH1	Digital high input current for IO Type 1	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN1<3.1	6.1	-	82.5	
DIIL1	Digital low input current for IO Type 1	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN1 < 0.7	-12.5	-	22.5	
DIOH1	Digital high output current for IO Type 1	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
DIOL1	Digital low output current for IO Type 1	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
DRPU1	Digital I/O pull-up resistance for IO Type 1	DVDIO = 2.8V	40	85	190	kΩ
DRPD1	Digital I/O pull-down resistance for IO Type 1	DVDIO = 2.8V	40	85	190	kΩ
DVOH1	Digital output high voltage for IO Type 1	DVDIO = 2.8V	2.38			V
DVOL1	Digital output low voltage for IO Type 1	DVDIO = 2.8V			0.42	V
DIIH2	Digital high input current for IO Type 2	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN1 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN1<3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-5	-	5	µA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PU enabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN1 < 2.1	-0.8	-	35	
DIIL2	Digital low input current for IO Type 2	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN2 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN1 < 0.45	-9.3	-	11.4	
DIOH2	Digital high output current for IO Type 2	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL2	Digital low output current for IO Type 2	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU2	Digital I/O pull-up resistance for IO Type 2	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD2	Digital I/O pull-down resistance for IO Type 2	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH2	Digital output high voltage for IO Type 2	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL2	Digital output low voltage for IO Type 2	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH3	Digital high input current for IO Type 3	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	-22.5	-	12.5	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PD enabled, DVDIO = 2.8V, 2.1 < VIN3 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN3 < 2.1	-0.8	-	35	
DIIL3	Digital low input current for IO Type 3	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN3 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN3 < 0.45	-9.3	-	11.4	
DIOH3	Digital high output current for IO Type 3	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL3	Digital low output current for IO Type 3	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU3	Digital I/O pull-up resistance for IO Type 3	DVDIO = 2.8V	10	47	100	kΩ
		DVDIO = 1.8V	10	47	100	kΩ
DRPD3	Digital I/O pull-down resistance for IO Type 3	DVDIO = 1.8V	10	47	100	kΩ
		DVDIO = 2.8V	10	47	100	kΩ
DVOH3	Digital output high voltage for IO Type 3	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL3	Digital output low voltage for IO Type 3	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIH4	Digital high input current for IO Type 4	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN4 < 3.1	6.1	-	82.5	
DIIL4	Digital low input current for IO Type 4	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN4 < 0.7	-12.5	-	22.5	
DIOH4	Digital high output current for IO Type 4	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
DIOL4	Digital low output current for IO Type 4	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
DRPU4	Digital I/O pull-up resistance for IO Type 4 (GPIO mode)	DVDIO = 2.8V	15	36	55	kΩ
DRPD4	Digital I/O pull-down resistance for IO Type 4 (GPIO mode)	DVDIO = 2.8V	15	36	55	kΩ
DRPU4 1200K	Digital I/O pull-up resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1200	-	-	kΩ
DRPD4 1200K	Digital I/O pull-down resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1200	-	-	kΩ
DVOH4	Digital output high voltage for IO Type 4	DVDIO = 2.8V	2.38			V
DVOL4	Digital output low voltage for IO Type 4	DVDIO = 2.8V			0.42	V
DIIH5	Digital high input current for IO Type 5	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN5 < 3.1	6.1	-	82.5	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
DIIL5	Digital low input current for IO Type 5	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN5 < 0.7	-12.5	-	22.5	
DIOH5	Digital high output current for IO Type 5	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
DIOL5	Digital low output current for IO Type 5	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
DRPU5	Digital I/O pull-up resistance for IO Type 5 (GPIO mode)	DVDIO = 2.8V	15	36	55	kΩ
DRPD5	Digital I/O pull-down resistance for IO Type 5 (GPIO mode)	DVDIO = 2.8V	15	36	55	kΩ
DRPU5 1K	Digital I/O pull-up resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1	-	-	kΩ
DRPD5 1K	Digital I/O pull-down resistance for IO Type 4 (Key PAD mode)	DVDIO = 2.8V	1	-	-	kΩ
DVOH5	Digital output high voltage for IO Type 5	DVDIO = 2.8V	2.38			V
DVOL5	Digital output low voltage for IO Type 5	DVDIO = 2.8V			0.42	V
DIIH6	Digital high input current for IO Type 6	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN6 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN6 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1 < VIN6 < 3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-11.4	-	9.3	
		PD enabled, DVDIO = 1.8V, 1.35 < VIN6 < 2.1	-0.8	-	35	
DIIL6	Digital low input current for IO Type 6	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-5	-	5	µA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PU enabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN6 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN6 < 0.45	-9.3	-	11.4	
DIOH6	Digital high output current for IO Type 6	DVOH > 2.38V, DVDIO = 2.8V	-8	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-6	-	-	mA
DIOL6	Digital low output current for IO Type 6	DVOL < 0.42V, DVDIO = 2.8V	-	-	8	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	6	mA
DRPU6	Digital I/O pull-up resistance for IO Type 6	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD6	Digital I/O pull-down resistance for IO Type 6	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH6	Digital output high voltage for IO Type 6	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL6	Digital output low voltage for IO Type 6	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V
DIIH7	Digital high input current for IO Type 7	PU/PD disabled, DVDIO = 2.8V, 2.1 < VIN7 < 3.1	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, 2.1 < VIN7 < 3.1	-22.5	-	12.5	
		PD enabled, DVDIO = 2.8V, 2.1<VIN7<3.1	6.1	-	82.5	
		PU/PD disabled, DVDIO = 1.8V, 1.35 < VIN7 < 2.1	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, 1.35 < VIN7 < 2.1	-11.4	-	9.3	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		PD enabled, DVDIO = 1.8V, 1.35 < VIN7 < 2.1	-0.8	-	35	
DIIL7	Digital low input current for IO Type 7	PU/PD disabled, DVDIO = 2.8V, -0.3 < VIN7 < 0.7	-5	-	5	µA
		PU enabled, DVDIO = 2.8V, -0.3 < VIN7 < 0.7	-82.5	-	-6.1	
		PD enabled, DVDIO = 2.8V, -0.3 < VIN7 < 0.7	-12.5	-	22.5	
		PU/PD disabled, DVDIO = 1.8V, -0.3 < VIN7 < 0.45	-5	-	5	µA
		PU enabled, DVDIO = 1.8V, -0.3 < VIN7 < 0.45	-35	-	0.8	
		PD enabled, DVDIO = 1.8V, -0.3 < VIN7 < 0.45	-5	-	5	
DIOH7	Digital high output current for IO Type 7	DVOH > 2.38V, DVDIO = 2.8V	-16	-	-	mA
		DVOH > 1.53V, DVDIO = 1.8V	-12	-	-	mA
DIOL7	Digital low output current for IO Type 7	DVOL < 0.42V, DVDIO = 2.8V	-	-	16	mA
		DVOL < 0.27V, DVDIO = 1.8V	-	-	12	mA
DRPU7	Digital I/O pull-up resistance for IO Type 7	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DRPD7	Digital I/O pull-down resistance for IO Type 7	DVDIO = 2.8V	40	85	190	kΩ
		DVDIO = 1.8V	70	150	320	kΩ
DVOH7	Digital output high voltage for IO Type 7	DVDIO = 2.8V	2.38			V
		DVDIO = 1.8V	1.53			V
DVOL7	Digital output low voltage for IO Type 7	DVDIO = 2.8V			0.42	V
		DVDIO = 1.8V			0.27	V

2.3 System Configuration

2.3.1 Strapping Resistors

Table 15. Strapping table

Pin name	Description	Trapping condition

Pin name	Description	Trapping condition
LSA0	Pull-up with 10K resister(Default internal pull-down with 47K resister)	Power-on reset
BPI_BUS1	Pull-up with 10K resister (Default internal pull-down with 75K resister)	Power-on reset
BPI_BUS2	Pull-up with 10K resister (Default internal pull-down with 75K resister)	Power-on reset

2.3.2 Mode Selection

Table 16. Mode selection of chip

Pin name	Description
EXT_CLK_SEL	GND: Uses DCXO as 26M clock source VRF: Uses external clock as 26M clock source
LSA0	GND: Uses 1.8V serial flash device DVDD18_EMI: Uses 3.3V serial flash device
KCOL0	GND: Boots ROM to enter USB download mode DVDD28: Normal boot-up mode
{BPI_BUS1,BPI_BUS2}	{GND, GND}: No JTAG {GND, DVDD28}: JTAG at keypad pins {DVDD28, GND}: JTAG at GPIO pins {DVDD28, DVDD28}: JTAG at camera pins

2.4 Power-on Sequence and Protection Logic

MT2503A provides 32K crystal removal feature. The XOSC32_ENB state tells if MT2503A provides this feature or not. VRF will be turned on at the same time with VRTC when XOSC32_ENB = 1. The power-on/off sequence controlled by “Control” and “Reset Generator” is shown as the figure below.

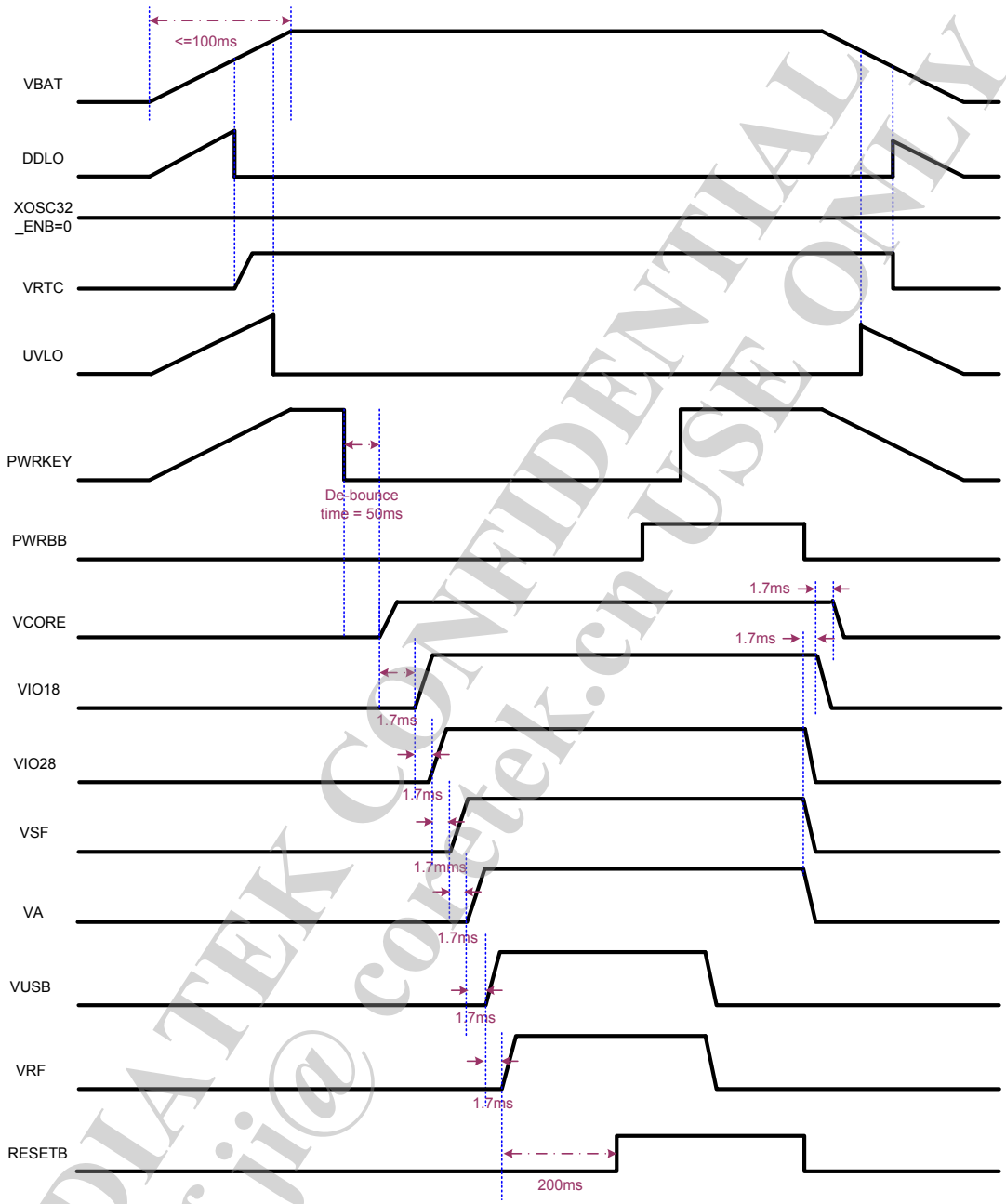


Figure 5. Power-on/off control sequence by pressing PWRKEY and XOSC32_ENB = 0

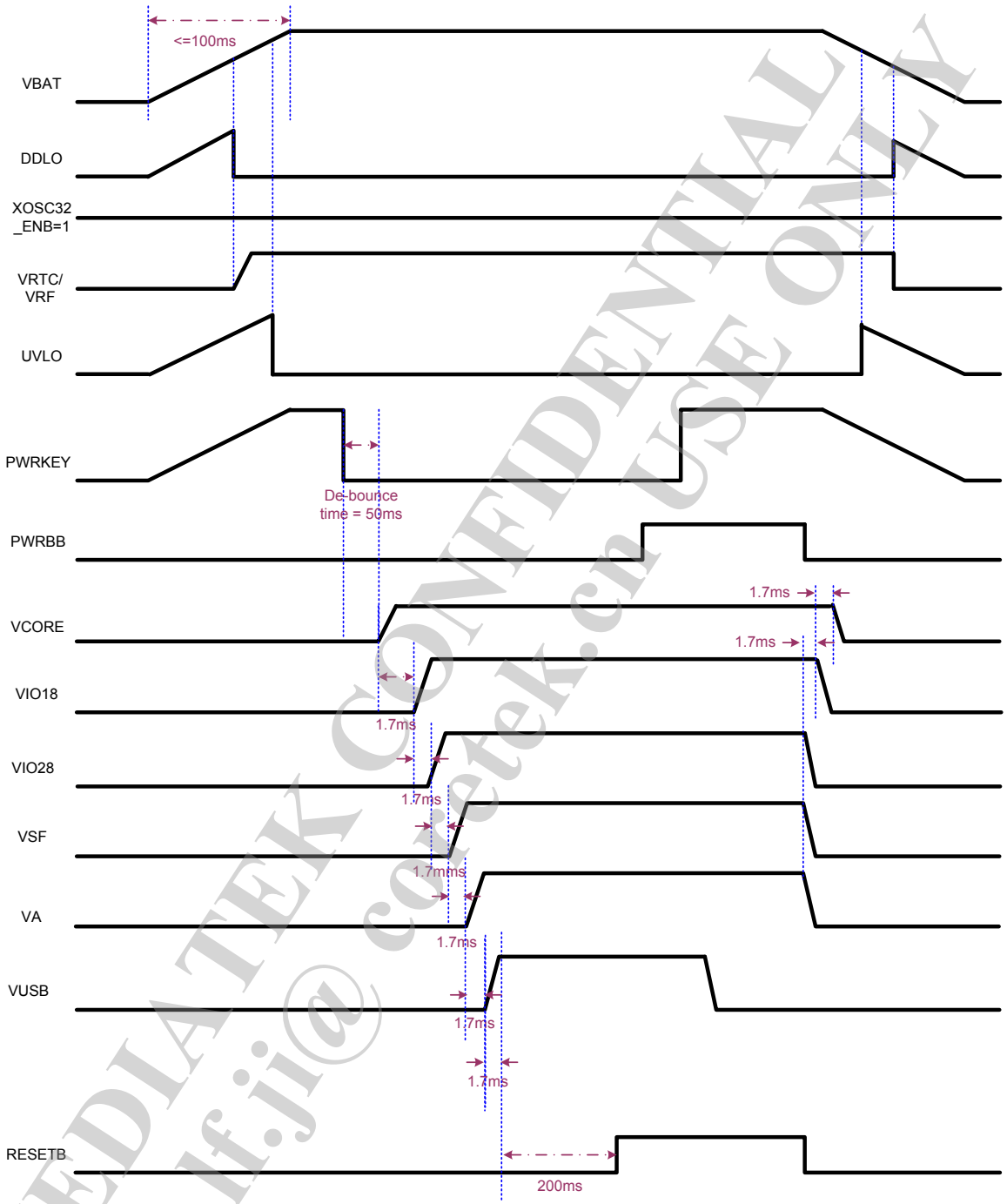


Figure 6. Power-on/off control sequence by pressing PWRKEY and XOSC32_ENB = 1

Note that each of the above figures only shows one power-on/off condition when XOSC32_ENB = 0 or XOSC32_ENB = 1. MT2503A handles the power-on and off of the handset. The following three methods can switch on the handset (when leaving UVLO): XOSC32_ENB = 0

1. Push PWRKEY (Pull the PWRKEY pin to the low level.)

Pulling PWRKEY low is the typical way to turn on the handset. The turn-on sequence is VCORE → VIO18 → VIO28 → VSF → VA → VUSB → VRF.

The supplies for the baseband are ready, and the system reset ends at the moment when the above LDOs are fully turned on to ensure correct timing and function. After that, the baseband will send the PWRBB signal back to the PMU for acknowledgement. To successfully power on the handset, PWRKEY should be kept low until PMU receives PWRBB from the baseband.

2. RTC module generates PWRBB to wake up the system.

   If the RTC module is scheduled to wake up the handset at a certain time, the PWRBB signal will be directly sent to the PMU. In this case, PWRBB will become high at specific moment and allow the PMU to be powered on as the sequence described above. This is called the RTC alarm.

3. Valid charger plug-in (CHRIN voltage is within the valid range.)

   The charger plug-in will also turn on the handset if the charger is valid (no OVP takes place). However, if the battery voltage is too low to power on the handset (UVLO state), the system will not be turned on by any of the three methods. In this case, the charger will charge the battery first and the handset will be powered on automatically as long as the battery voltage is high enough.

Under-voltage lockout (UVLO)

The UVLO state in the PMU prevents startup if the initial voltage of the main battery is below the 3.2V threshold. It ensures that the handset is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures a smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state, and the PMU will be turned off by itself, except for VRTC LDO, to prevent further discharging. Once the PMU enters the UVLO state, it will draw low quiescent current. The RTC LDO will still be working until the DDLO disables it.

Deep discharge lockout (DDLO)

The PMU will enter the deep discharge lockout (DDLO) state when the battery voltage drops below 2.5V. In this state, the VRTC LDO will be shut down. Otherwise, it will draw very low quiescent current to prevent further discharging or damage to the cells.

Reset

The PMU contains a reset control circuit which takes effect at both power-up and power-down. The RESETB pin is held low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter which uses the clock from internal ring-oscillator. At power-off, the RESETB pin will return to low immediately without any delay.

Over-temperature protection

If the die temperature of PMU exceeds 150°C, the PMU will automatically disable all the LDOs except for VRTC. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the LDOs.

2.5 Analog Baseband

To communicate with analog blocks, a common control interface for all analog blocks is implemented. In addition, there are some dedicated interfaces for data transfer. The common control interface translates the APB bus write and read cycle for specific addresses related to analog front-end control. During the writing or reading of any of these control registers, there is a latency associated with the transfer of data to or from the analog front-end. Dedicated data interface of each analog block is implemented in the corresponding digital block. An analog block includes the following analog functions for the complete GSM/GPRS baseband signal processing:

1. RF control: DAC for automatic power control (APC) is included, and its output is provided to external RF power amplifier respectively.
2. Auxiliary ADC: Provides an ADC for the battery and other auxiliary analog functions monitoring
3. Audio mixed-signal block: Provides complete analog voice signal processing including microphone amplification, A/D conversion, D/A conversion, earphone driver, etc. Dedicated stereo D/A conversion and amplification for audio signals are also included.
4. Clock generation: Includes a clock squarer for shaping the system clock, and PLL providing clock signals to DSP, MCU and USB unit

2.5.1 APC-DAC

2.5.1.1 Block Description

APC-DAC is a 10-bit DAC with output buffer aiming at automatic power control. See the tables below for its analog pin assignment and functional specifications. It is an event-driven scheme for power saving purpose.

2.5.1.2 Functional Specifications

Table 17. APC-DAC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
FS	Sampling rate			1.0833	MSPS

Symbol	Parameter	Min.	Typ.	Max.	Unit
SINAD	Signal to noise and distortion ratio (10-kHz sine with 1.0V swing & 100-kHz BW)	47			dB
	99% settling time (full swing on maximal capacitance)			5	µS
	Output swing	0		AVDD	V
	Output capacitance		200	2200	pF
	Output resistance	0.47	10		KΩ
DNL	Differential nonlinearity for code 20 to 970		± 1		LSB
INL	Integral nonlinearity for code 20 to 970		± 1		LSB
DVDD	Digital power supply	1.1	1.2	1.3	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-20		80	°C
	Current consumption Power-up Power-down		 400 1		 µA µA

2.5.2 Auxiliary ADC

2.5.2.1 Block Description

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the seven auxiliary input pins. Real-world messages to be monitored, e.g. temperature, should be transferred to the voltage domain.

2. 10-bit A/D converter: Converts the multiplexed input signal to 10-bit digital data.

Channel	Application	Input range [V]
0	BATSNS	3.2 ~ 4.2
1	ISENSE	3.2 ~ 4.2
2	VCDT	Decided by application circuit
3	BATON	0 ~ AVDD28
4	AUXIN4	0 ~ AVDD28
others	Internal use	N/A

2.5.2.2 Functional Specifications

The functional specifications of the auxiliary ADC are listed in the following table.

Table 18. Functional specifications of auxiliary ADC

Symbol	Parameter	Min.	Typ.	Max.	Unit

Symbol	Parameter	Min.	Typ.	Max.	Unit
N	Resolution		10		Bit
FC	Clock rate		1.08		MHz
FS	Sampling rate @ N-Bit		1.08/(N+1)		MSPS
	Input swing	0		AVDD	V
CIN	Input capacitance Unselected channel Selected channel			 50 4	 fF pF
RIN	Input resistance Unselected channel Selected channel	 400 1			 MΩ MΩ
	Clock latency		N+1		1/FC
DNL	Differential nonlinearity		± 1		LSB
INL	Integral nonlinearity		± 1		LSB
OE	Offset error		± 10		mV
FSE	Full swing error		± 10		mV
SINAD	Signal to noise and distortion ratio (10-kHz full swing input & 1.0833-MHz clock rate)		50		dB
DVDD	Digital power supply	1.1	1.2	1.3	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-20		80	°C
	Current consumption Power-up Power-down		 280 1		 μA μA

2.5.3 Audio Mixed-Signal Blocks

2.5.3.1 Block Description

Audio mixed-signal blocks (AMB) integrate complete voice uplink/downlink and audio playback functions. As shown in the figure below, it includes three parts. The first consists of stereo audio DACs and audio amplifiers for audio playback. The second part is the voice downlink path, including voice-band DACs (left channel audio DAC) and voice amplifier, which produces voice signals to earphones or other auxiliary output devices. Moreover, a ClassK amplifier is embedded to support continuous >1W output power with an on-chip boost. The last part is the voice uplink path, which is the interface between the microphone (or other auxiliary input device) input and MT2503A DSP. A set of bias voltage is provided for the external electric microphone.

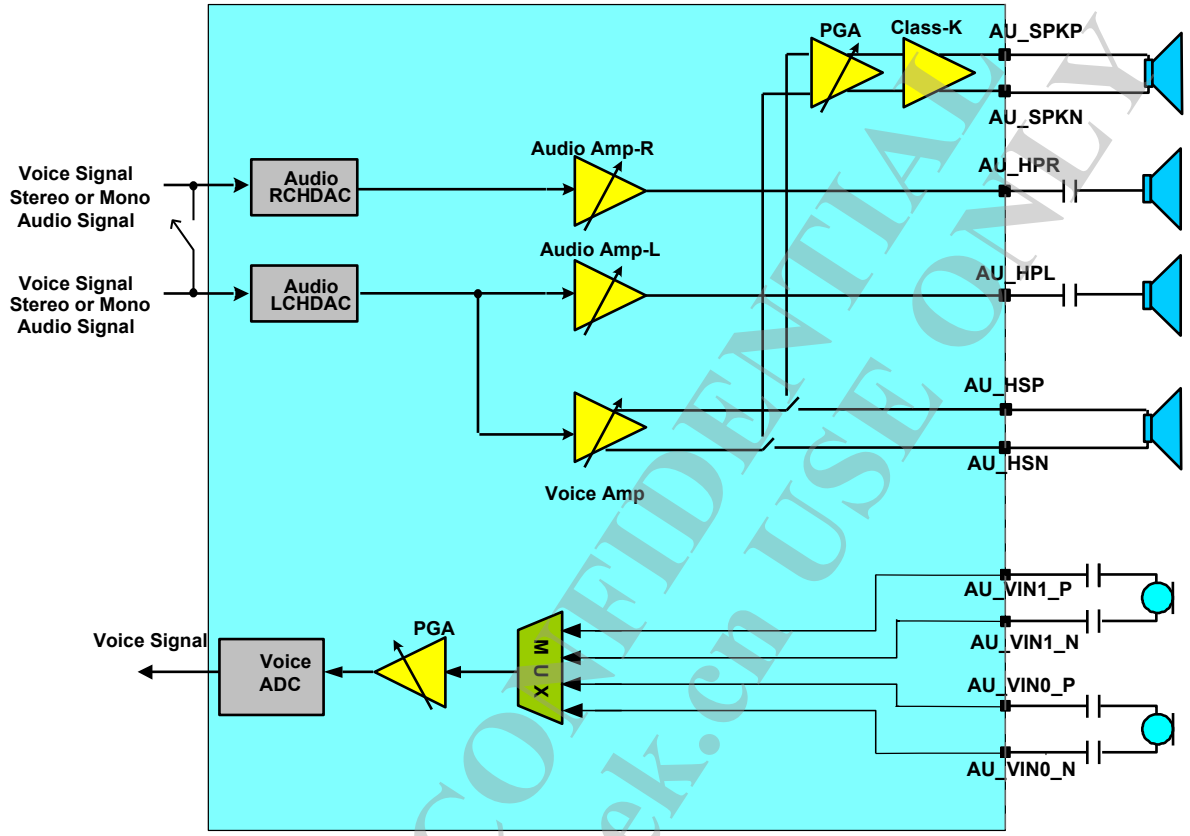


Figure 7. Block diagram of audio mixed-signal blocks

2.5.3.2 Functional Specifications

See the table below for the functional specifications of voice-band uplink/downlink blocks.

Table 19. Functional specifications of analog voice blocks

Symbol	Parameter	Min.	Typ.	Max.	Unit
FS	Sampling rate		6,500		kHz
DVDD	Digital power supply	1.1	1.2	1.3	V
AVDD	Analog power supply	2.6	2.8	3.0	V
T	Operating temperature	-20		80	°C
VMIC	Microphone biasing voltage		1.9	2.2	V
IMIC	Current draw from microphone bias pins			2	mA
Uplink path[4]					
IDC	Current consumption for one channel		1.5		mA
SINAD	Signal to noise and distortion ratio Input level: -40 dbm0	29			dB

[4] For uplink-path, not all gain settings of VUPG meet the specifications listed in the table, especially for several the lowest gains. The minimum gain that meets the specifications is to be determined.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Input level: 0 dbm0		69		dB
RIN	Input impedance (differential)	13	20	27	KΩ
ICN	Idle channel noise			-67	dBm0
Downlink path					
IDC	Current consumption		4		mA
SINAD	Signal to noise and distortion ratio Input level: -40 dBm0 Input level: 0 dBm0	29	 69		 dB dB
RLOAD	Output resistor load (differential)	16	32		Ω
CLOAD	Output capacitor load			250	pF
ICN	Idle channel noise of transmit path			-64	dBPa
XT	Crosstalk level on transmit path			-66	dBm0

See the table below for the functional specifications of audio blocks.

Table 20. Functional specifications of analog audio blocks

Symbol	Parameter	Min.	Typ.	Max.	Unit
FCK	Clock frequency		6.5		MHz
Fs	Sampling rate	32	44.1	48	kHz
AVDD	Power supply	2.6	2.8	3.0	V
T	Operating temperature	-20		80	°C
IDC	Current consumption		4		mA
PSNR	Peak signal to noise ratio		88		dB
DR	Dynamic range		88		dB
VOUT	Output swing for 0dBFS input level @ -1dB headphone gain		0.707		Vrms
$VOUT_{MAX}$	Maximum output swing		2.0		Vpp
THD	Total harmonic distortion 10mW at 64Ω load			 -70	 dB
RLOAD	Output resistor load (single-ended)	64			Ω
CLOAD	Output capacitor load			250	pF
XT	L-R channel cross talk	70			dB

2.6 Power Management Unit Blocks

The power management unit (PMU) manages the power supply of the entire chip, such as baseband, processor, memory, SIM cards, camera, vibrator, etc. The digital part of PMU is integrated into the analog part (see the figure below). PMU includes the following analog functions for signal processing:

- LDO: Regulates battery voltage to lower voltage level
- BOOST: Boosts battery voltage to target voltage for Class-AB audio amplifier
- Keypad LED driver (KPLED) and current sink (ISINK) switches: Sink current for keypad LED and LCM module

- Start-up (STRUP): Generates power-on/off control sequence of start-up circuits
- Pulse charger (PCHR): Controls battery charging

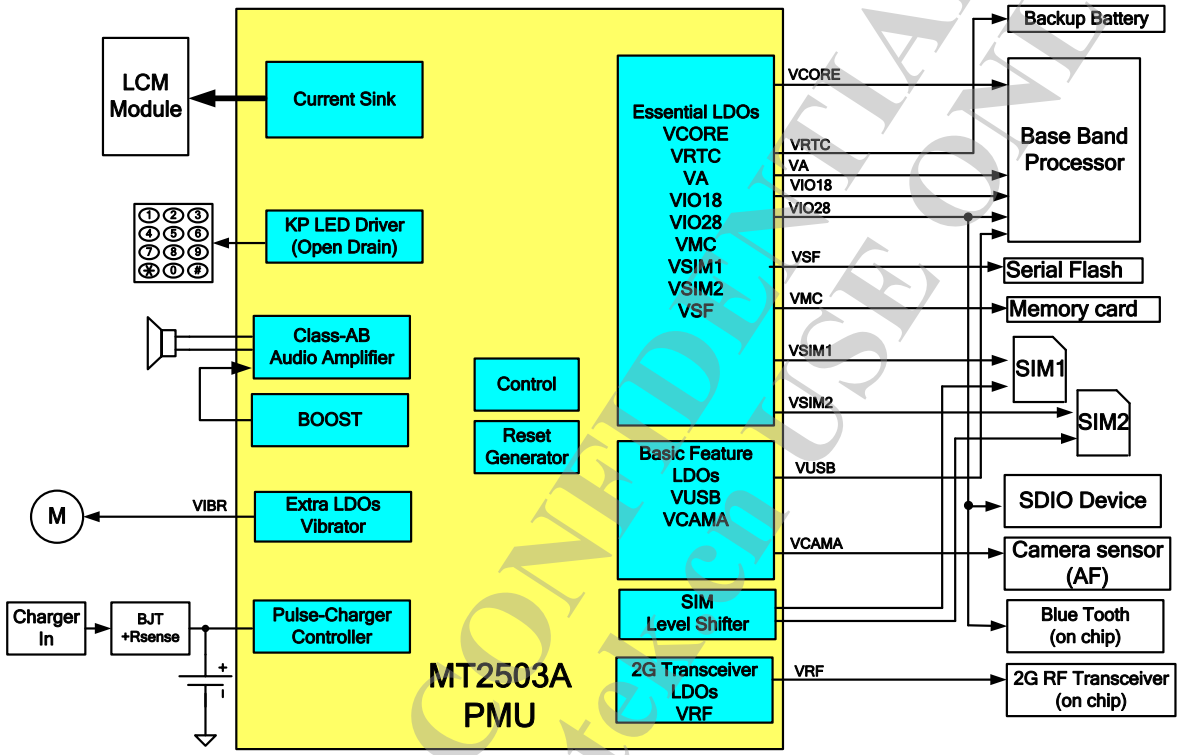


Figure 8. PMU system block diagram

2.6.1 LDO

PMU integrates 13 general low dropout regulators (LDO) optimized for their given functions by balancing the quiescent current, dropout voltage, line/load regulation, ripple rejection and output noise.

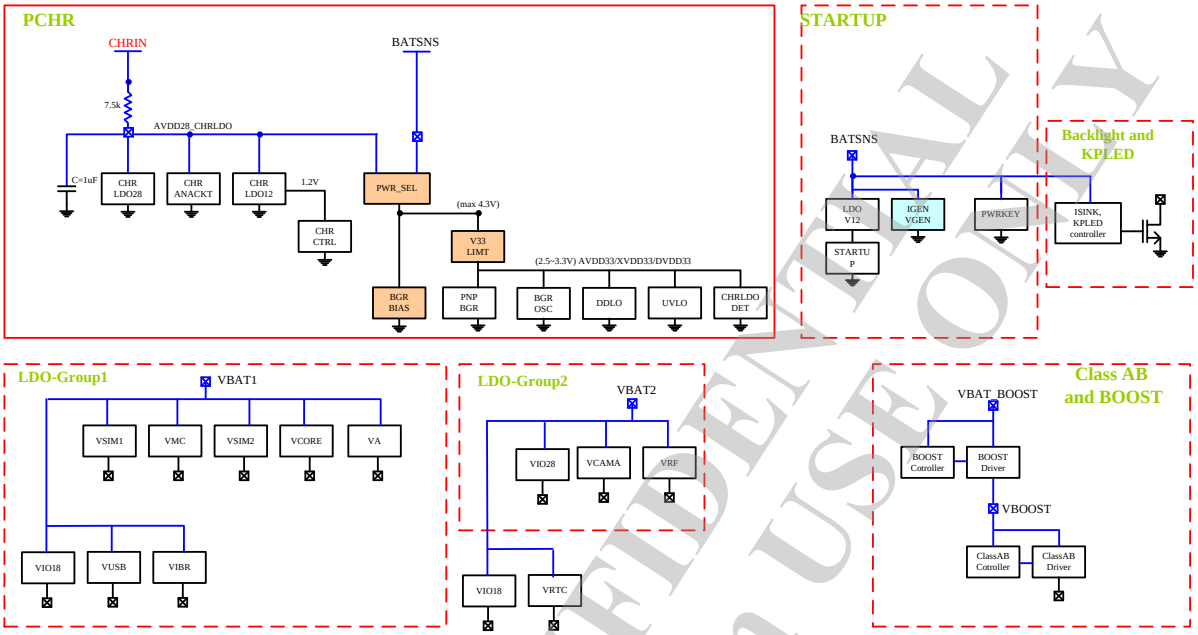


Figure 9. Power domain

2.6.1.1 LDO

A low-dropout regulator (LDO) is capable of maintaining its specified output voltage over a wide range of load current and input voltage, down to a very small difference between input and output voltages.

There are several features in the design of LDO, including discharge control, soft start and current limit. Before LDO is enabled, the output pin of LDO should be discharged first to avoid voltage accumulation on the capacitance. The soft-start limits inrush current and controls output-voltage rising time during the power-up. The current limit is the current protection to limit the LDO's output current and power dissipation.

There are three types of LDOs in PMU of MT2503A PMU. The analog LDO is optimized for low-frequency ripple rejection in order to reject the ripples coming from the burst of RF power amplifier. The digital IO LDO is a linear regulator optimized for very low quiescent current. The single-step RTC LDO is a linear regulator that can charge up a capacitor-type backup coin cell, which also supplies the RTC module even at the absence of the main battery. The single-step LDO features reverse current protection and is optimized for ultra-low quiescent current while sustaining the RTC function as long as possible.

2.6.1.1.1 Block Description

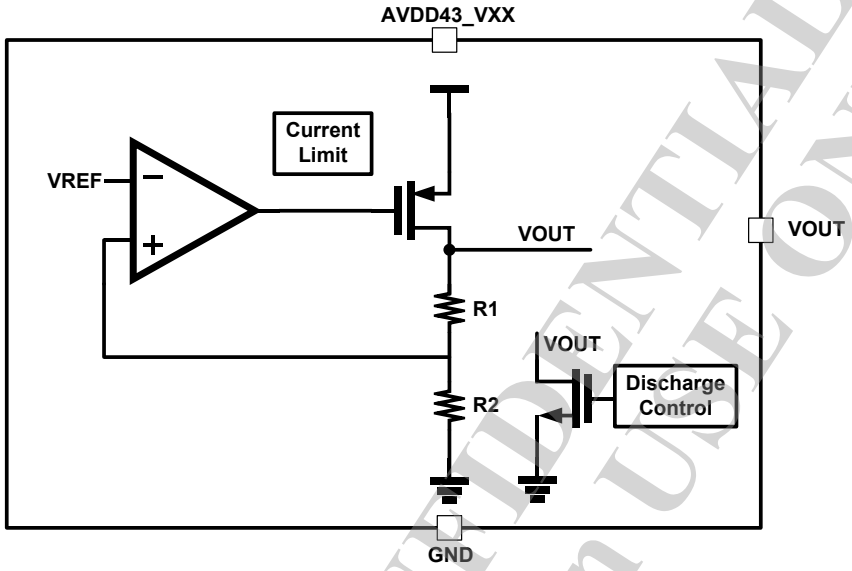


Figure 10. LDO block diagram

2.6.1.1.2 LDO Types

Table 21. LDO types and brief specifications

Type	LDO name	Vout (Volt)	Imax(mA)	Description
ALDO	VRF	2.8	150	RF chip and 26MHz reference clock
ALDO	VA	2.8	150	Analog baseband
ALDO	VCAMA	2.8	70	Camera sensor
DLDO	VIO28	2.8	100	Digital IO and Blue tooth
DLDO	VSIM1	1.8/3.0	30	SIM card
DLDO	VSIM2	1.8/3.0	30	SIM card
DLDO	VUSB	3.3	50	USB
DLDO	VIO18	1.8	100	Digital IO
DLDO	VCORE	0.75~1.35	150	Digital baseband
DLDO	VIBR	1.8/2.8/3.0	100	Vibrator
DLDO	VMC	1.8/2.8/3.0/3.3	100	Memory card
DLDO	VSF	1.86/2.8/3.0/3.3	50	Serial flash
RTCLDO	VRTC	2.8/3.3	2	Real-time clock

2.6.1.1.3 Functional Specifications

Table 22. Analog LDO specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Load capacitor			1		µF
	Current limit		1.2*Imax		5*Imax	mA
	Vout	Includes load regulation, line regulation, and temperature coefficient	Max. (-5%, -0.1V)		Max. (+5%, +0.1V)	V
	Transient response	Slew: 15mA/us	Max. (-5%, -0.1V)		Max. (+5%, +0.1V)	V
	Temperature coefficient				100	ppm/C
	PSRR	Iout < 0.5*Imax 10 < f < 3 kHz	65			dB
		Iout < 0.5*Imax 3K < f< 30 kHz	45			dB
	Output noise	With A-weighted filter			90	uVrms
	Quiescent current	Iout = 0		55		µA
	Turn-on overshoot	Iout = 0			Max. (+10%, +0.1V)	V
	Turn-on settling time	Iout = 0			240	µsec

Table 23. Digital LDO specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Load capacitor			1[5]		µF
	Current limit		1.2*Imax		5*Imax	mA
	Vout	Includes load regulation, line regulation, and temperature coefficient	Max. (-5%, -0.1V)		Max. (+5%, +0.1V)	V
	Transient response	Slew: 15mA/us	Max. (-5%, -0.1V)		Max. (+5%, +0.1V)	V
	Temperature coefficient				100	ppm/C
	Quiescent current	Iout = 0		30		µA

[5] VCORE loading capacitor typical value is 2.2uF. Other LDOs are 1uF.

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Turn-on overshoot	Iout = 0			Max. (+10%, +0.1V)	V
	Turn-on settling time	Iout = 0			240	µs

Table 24. RTC LDO specification

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Load capacitor			1		µF
	Vout	Includes load regulation, line regulation, and temperature coefficient	2	2.8	3	V
	Temperature coefficient				100	ppm/C
	Quiescent current	Iout = 0		15		µA

2.6.2 BOOST

2.6.2.1 Functional Specifications

Table 25. RTC LDO specification.

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Cin Cout			2.2uF 4.7uF		µF
	L	Rdcr,max<80mOhm		0.68		uH
	Vout			5.3		V
	Ripple	Vin=3.4V/3.8V/4.2V, Cin=2.2uF & Cout=4.7uF, L= 0.68uH (Rdcr,max<80mOhm) 650mA , switching Freq 2MHz			100	mV
	Switching frequency			2		MHz
	Quiescent current	Iout = 0		4	6	mA

2.6.3 ISINK and KPLED Switches

One built-in open-drain output switch drives the keypad LED (KPLED) in the handset. The switch is controlled by the baseband with enabling registers. The switch of keypad LED can sink as much as

60mA current, and the output is high impedance when disabled. The value of the sink current decides the brightness of the LED.

The current controlled open drain drivers are also implemented to drive the LCM backlight module, and provides currentfrom 4mA to 96mA.

2.6.3.1 Block Description

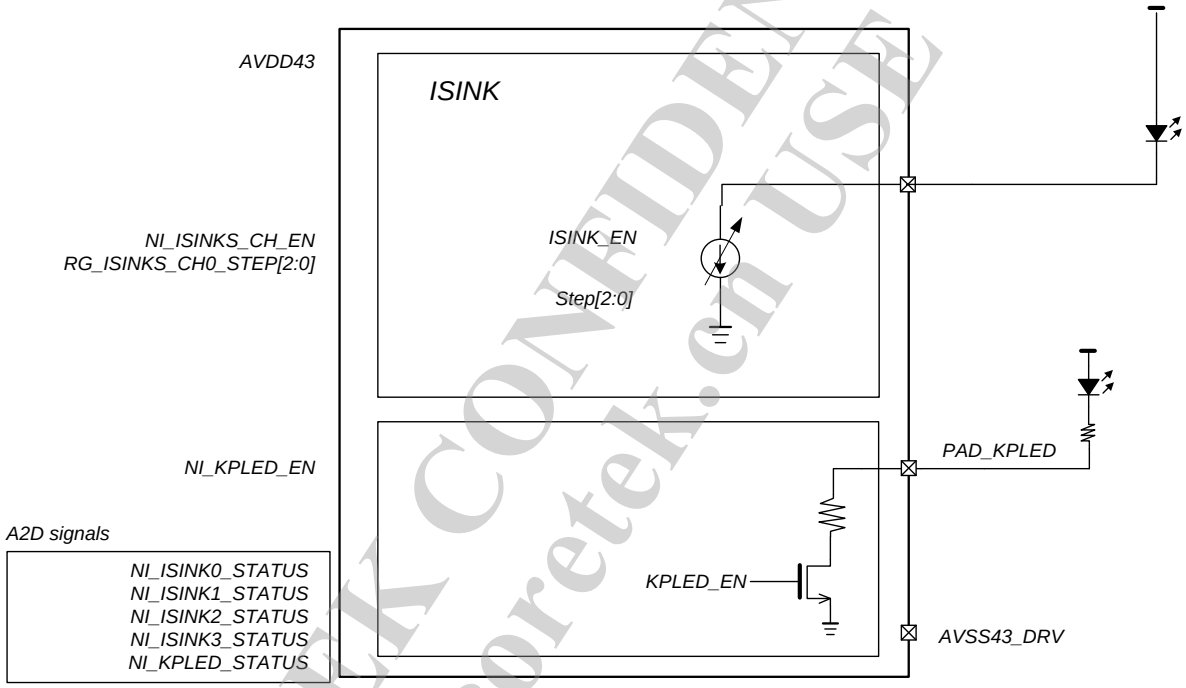


Figure 11. ISINKs and KPLED switches bock diagram.

2.6.3.2 Functional Specifications

Table 26. ISINKs and KPLED Switches Specification.

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Sink current of keypad LED driver	Von > 0.5V, 100% dimming duty	60			mA
	1 ch Sink current of ISINK without current double option	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 000		4		mA
	1 ch Sink current of ISINK without current double option	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 001		8		mA
	1 ch Sink current of	Von > 0.15V, 100%		12		mA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	ISINK without current double option	dimming duty, ISINKS_CHx_STEP = 010				
	1 ch Sink current of ISINK without current double option	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 011		16		mA
	1 ch Sink current of ISINK without current double option	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 100		20		mA
	1 ch Sink current of ISINK without current double option	Von > 0.15V, 100% dimming duty, ISINKS_CHx_STEP = 101		24		mA
	Current mismatch	Von > 0.15V, 100% dimming duty	-5		5	%

2.6.4 STRUP

PMU handles the power-on and off of the handset. If the battery voltage is neither in the UVLO state (VBAT ≥ 3.4V) nor in the thermal condition, there are three methods to power on the handset system: pulling PWRKEY low (the user pushes PWRKEY), pulling PWRBB high (baseband BB_WakeUp) or valid charger plug-in.

According to different battery voltage (VBAT) and phone states, control signals and regulators will have different responses.

2.6.5 PCHR

The charger controller senses the charger input voltage from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a pre-determined range, the charging process will be activated. This detector can resist higher input voltage than other parts of the PMU.

2.6.5.1 Block Description

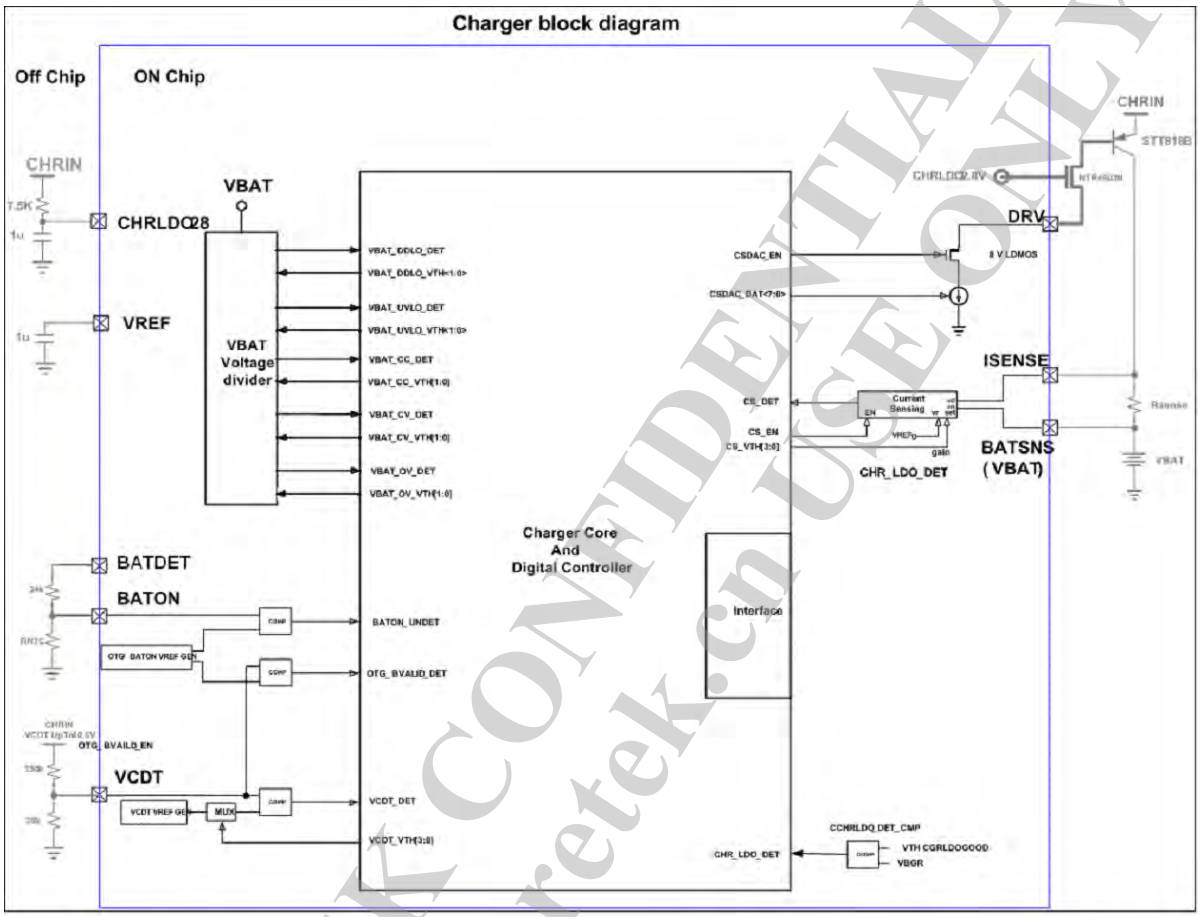


Figure 12. PCHR block diagram.

2.6.5.1.1 Charger Detection

Whenever an invalid charging source is detected (> 7.0 V), the charger detector stops the charging process immediately to avoid burning out the chip or even the phone. In addition, if the charger-in level is not high enough (< 4.3V), the charger will also be disabled to avoid improper charging behavior.

2.6.5.1.2 Charging Control

When the charger is active, the charger controller manages the charging phase according to the battery status. During the charging period, the battery voltage is constantly monitored. The battery charger supports pre-charge mode (VBAT < 3.2V, PMU power-off state), CC mode (constant current mode or fast charging mode at the range 3.2V < VBAT < 4.2V) and CV mode (constant voltage mode) to optimize the charging procedure for Li-ion battery. The charging states diagram is shown in the figure below.

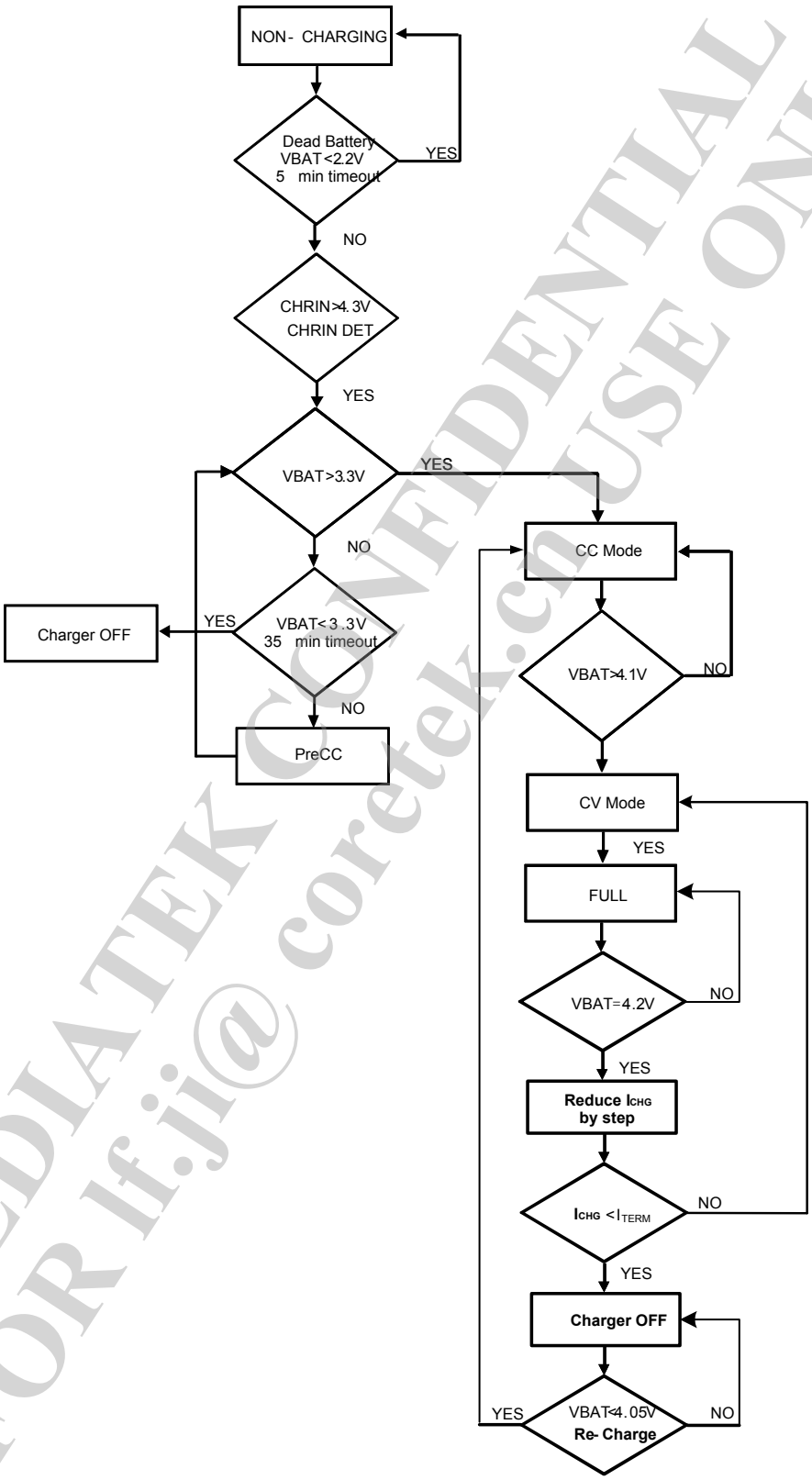


Figure 13. Charging states diagram

Pre-charge mode

When the battery voltage is in the UVLO state, the charger operates in the pre-charge mode. There are two steps in this mode. When the battery voltage is deeply discharged below 2.2V, PRECC1 trickle charging current will be applied to the battery.

The PRECC1 trickle charging current is about 550ms pulse 70mA current when VBAT is under 2.2V.

When the battery voltage exceeds 2.2V, called the PRECC2 stage, the closed-loop pre-charge is enabled. The voltage drop across the external RSENSE is kept around 40mV (AC charger) or 14mV (USB host). The closed-loop pre-charge current can be calculated:

$$I_{PRECC2,ACadapter} = \frac{V_{SENSE}}{Rsense} = \frac{40mV}{Rsense}$$

$$I_{PRECC2,USBHOST} = \frac{V_{SENSE}}{Rsense} = \frac{14mV}{Rsense}$$

Constant current mode

As the battery is charged up and over 3.4V, it can switch to the CC mode. (CHR_EN should be high) In the CC mode, several charging currents can be set by programming registers or the external RSENSE resistor. The charging current can be determined by CS_VTH/RSENSE, where CS_VTH is programmed by registers. For example, if RSENSE is selected as 0.2ohm, the CC mode charging current can be set from 70 to 800mA. It can accommodate the battery charger to various charger inputs with different current capabilities.

Constant voltage mode and over-voltage protection (OV)

While the battery voltage reaches about 4.2V, a constant voltage is used for charging. This is called the full-voltage charging mode or constant-voltage charging mode in correspondence to a linear charger. While the battery voltage actually reaches 4.2V, the charging current is gradually decreased step-by-step, the end-of-charging process starts. It may prolong the charging and detecting period for acquiring optimized full charging volume. The charging process is completed once the current reaches zero automatically and this mechanism is optimized for different battery

BC1.1 Dead-Battery Support of China Standard

MT2503A supports dead-battery condition from China standard (called BC1.1). The specification protects dead-battery charging by timer and trickle current. Once the battery voltage is below 2.2V, a period (TUNIT) of trickle current (IUNIT) will be applied to the battery.

If the battery voltage is still below 2.2V after applying trickle current, the charger will be disabled. On the other hand, if the battery voltage is raised to above 2.2V, the charger will enter the PRECC2 stage, and the charging current will be 70mA or 200mA depending on the type of charging port.

Under the condition of battery voltage from 2.2V to 3.3V, the charger will charge the battery with the PRECC2 current.

A dedicated 5mins (T1) timer will be timed out and disable the charger if the battery voltage is always below 2.7V under charging. Another 35mins (T2) timer will also be timed out and disable the charger if the battery voltage is always kept between 2.7V and 3.3V under charging.

The trickle current (IUNIT) and two dedicated timers protect the charging action if the battery is dead.

2.6.5.2 Functional Specifications

Table 27. Charger detection specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Charger detect-on range		4.3		7	V

Table 28. Pre-charge specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	IUNIT with 500ms pulse	VBAT < 2.2V	20	48	100	mA
	Pre-charging current	VBAT < 2.2V (500ms pulse)	20	48	100	mA
		VBAT ≥ 2.2V (USB host)	$7/R_{sense}$	$14/R_{sense}$	$20/R_{sense}$	mA
		VBAT ≥ 2.2V (AC adapter < 7V)	$30/R_{sense}$	$40/R_{sense}$	$50/R_{sense}$	mA
		VBAT ≥ 2.2V (AC adapter > 7V)	$7/R_{sense}$	$14/R_{sense}$	$20/R_{sense}$	mA
	Pre-charging off threshold	CHR_EN = L		3.3		V
	Pre-charging off hysteresis			0.4		V

Table 29. Constant current specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	CC mode charging current (CS_VTH)	CS_VTH [3:0] = 0000		$320/R_{sense}$		mA
		CS_VTH [3:0] = 0001		$300/R_{sense}$		mA
		CS_VTH [3:0] = 0010		$280/R_{sense}$		mA
		CS_VTH [3:0] = 0011		$260/R_{sense}$		mA
		CS_VTH [3:0] = 0100		$240/R_{sense}$		mA
		CS_VTH [3:0] = 0101		$220/R_{sense}$		mA
		CS_VTH [3:0] = 0110		$200/R_{sense}$		mA

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		CS_VTH [3:0] = 0111		180/R_{sense}		mA
		CS_VTH [3:0] = 1000		160/R_{sense}		
		CS_VTH [3:0] = 1001		140/R_{sense}		
		CS_VTH [3:0] = 1010		130/R_{sense}		
		CS_VTH [3:0] = 1011		110/R_{sense}		
		CS_VTH [3:0] = 1100		90/R_{sense}		
		CS_VTH [3:0] = 1101		60/R_{sense}		
		CS_VTH [3:0] = 1110		40/R_{sense}		
		CS_VTH [3:0] = 1111		14/R_{sense}		
	Current sensing resistor	RSENSE		0.2		ohm

Table 30. Constant voltage and over-voltage protection specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Charging complete threshold		4.15	4.2	4.25	V
	Battery over-voltage protection threshold (OV)			4.3		V

Table 31. BC1.1 specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
IUNIT	BC1.1 trickle current	VBAT < 2.2V		50	100	mA
IPRECC2 (USB host)	PRECC2 current	2.2 < VBAT < 3.3V		70	100	mA
IPRECC2 (AC adapter)	PRECC2 current	2.2 < VBAT < 3.3V		200	250	mA
T1	5 minute dedicated timer	2.2 < VBAT < 2.7V		5	6.5	min.
T2	35 minute dedicated timer	2.7 < VBAT < 3.3V		35	38.5	min.
TUNIT	BC1.1 trickle current period			550	770	ms.

2.7 GSM/GPRS RF

2.7.1 General Description

2G RFSYS which is built in MT2503A SOC is a highly integrated RF transceiver for multi-band GSM and GPRS cellular systems.

The features include:

Receiver

- Single-end saw-less Rx
- Quadrature RF mixer
- Fully integrated channel filter
- High dynamic range ADC
- 12dB PGA gain with 6dB gain step

Transmitter

- High accurate transmitter modulator for GSM/GPRS application
- Built-in calibration of SX loop filter and loop gain

Frequency synthesizer

- Programmable fractional-N synthesizer
- Integrated wide range RFVCO
- Integrated loop filter
- Fast settling time suitable for multi-slot GSM/GPRS applications

Digitally-Controlled Crystal Oscillator (DCXO)

- Two-pin 26 MHz crystal oscillator
- On-chip programmable capacitor array for coarse-tuning
- On-chip programmable capacitor array for fine-tuning

– Supports 32K XTAL-less operation

2.7.2 Functional Block Diagram

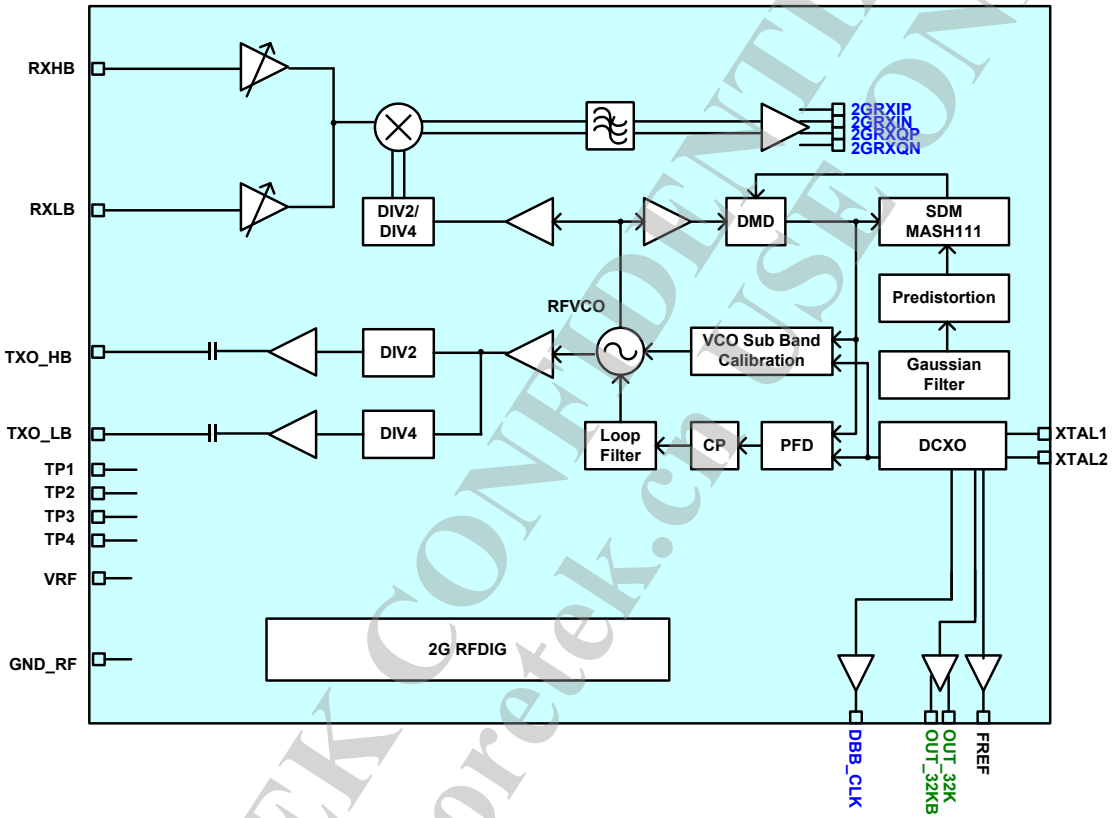


Figure 14. Diagram of MT2503A 2G RFSYS

2.7.3 Electrical Characteristics

Table 32. DC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

RFSYS mode	VRF	AVDD28_2GAFE	RFSYS total	Unit
BCM_Deep sleep (DCXO is off)	17	1	18	uA
BCM_Sleep (DCXO is on)	1.2	0.26	1.5	mA
Low power mode	60	1	61	uA
Full power mode	1.2	0.26	1.5	mA
RX (GSM850/EGSM)	62	5	67	mA
RX (DCS/PCS)	66	5	71	mA
TX (GSM850/EGSM)	41	2	43	mA
TX (DCS/PCS)	36	2	38	mA

Table 33. Rx AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

Item	Symbol	Band	Test condition	Min.	Typ.	Max.	Unit
Input frequency	F_{RX}	GSM850		869		894	MHz
		GSM900		925		960	MHz
		DCS1800		1,805		1,880	MHz
		PCS1900		1,930		1,990	MHz
Voltage gain 1	G_1	GSM850	LNA = High gain PGA = High gain	52[1]	55		dB
		GSM900		52[2]	55		dB
		DCS1800	LNA = High gain PGA = High gain	52[3]	55		dB
		PCS1900		52[4]	55		dB
Voltage gain 2	G_2	GSM850	LNA = Middle gain PGA = High gain		46		dB
		GSM900			46		dB
		DCS1800	LNA = Middle gain PGA = High gain		45		dB
		PCS1900			45		dB
Voltage gain 3	G_3	GSM850	LNA = Low gain PGA = High gain		26		dB
		GSM900			26		dB
		DCS1800	LNA = Low gain PGA = High gain		26		dB
		PCS1900			26		dB
Noise figure at 25°C	NF_{25}	GSM850	G_1		3	5[1]	dB
		GSM900			3	5[2]	dB
		DCS1800			3	5[3]	dB
		PCS1900			3	5[4]	dB
Noise figure at 85°C	NF_{85}	GSM850	G_1		4.5		dB
		GSM900			4.5		dB
		DCS1800			4.5		dB
		PCS1900			4.5		dB
2nd-order input intercept point	IIP2	GSM850	G2	31[1]	43		dBm
		GSM900		31[2]	43		dBm
		DCS1800		31[3]	43		dBm
		PCS1900		31[4]	43		dBm
3rd-order input intercept point	IIP3	GSM850	G2	-14[1]	-3		dBm
		GSM900		-14[2]	-3		dBm
		DCS1800		-14[3]	-3		dBm
		PCS1900		-14[4]	-3		dBm
3rd-order input intercept point @ -20°C	$IIP3_{-20}$	GSM850	G2		-5		dBm
		GSM900			-5		dBm
		DCS1800			-5		dBm
		PCS1900			-5		dBm
Receiver S/N with 3MHz blocker	SN_{3M}	GSM850	G2 Blocker = -23dBm	8[1]	12		dB
		GSM900		8[2]	12		dB
		DCS1800	G2 Blocker = -26dBm	8[3]	12		dB
		PCS1900		8[4]	12		dB

Item	Symbol	Band	Test condition	Min.	Typ.	Max.	Unit
Receiver S/N with OBB	SN_{OOB}	GSM850	G2 Blocker = 2dBm, offset +/-20MHz	6[5]	8		dB
		GSM900		6[5]	8		dB
		DCS1800	G2 Blocker = -10/2dBm, offset +/-80/-100MHz	6[5]	8		dB
		PCS1900		6[5]	8		dB
Image rejection ratio	IRR	ALL	G2	32[1,2,3,4]	40		dB
Receiver channel response attenuation		ALL	@3MHz offset		20		dB
			@6MHz offset		35		dB
Receiver filtering 3-dB bandwidth		ALL	For all gain settings		900		kHz
PGA gain linearity		ALL	INL		0.2	1[5]	dBΩ
			DNL		0.1	0.5[5]	dBΩ
PGA gain step		ALL			6		dBΩ
PGA dynamic range		ALL			12		dBΩ
I/Q common-mode output voltage		ALL	G1	1.1[5]	1.2	1.3[5]	V
Output static dc offset		ALL	G1		100	200	mV

Table 34. Tx GMSK AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

Item	Symbol	Band	Test condition	Min.	Typ.	Max.	Unit
Frequency	F_{TX}	GSM850		824		849	MHz
		GSM900		880		915	MHz
		DCS1800		1,710		1,785	MHz
		PCS1900		1,850		1,910	MHz
RMS phase error	PE_{rms}	GSM850 GSM900			1.5	2.5[1,2]	degree
		DCS1800 PCS1900			1.5	2.5[3,4]	degree
Output modulation spectrum	ORFS	GSM850 GSM900	400kHz offset (RBW = 30kHz bandwidth)		-66	-64[1,2]	dBc
		DCS1800 PCS1900			-66	-64[3,4]	dBc
		GSM850 GSM900	1.8MHz offset (RBW = 30kHz bandwidth)			-75[5]	dBc
		DCS1800 PCS1900				-75[5]	dBc
Tx noise in Rx band		GSM850	20MHz offset		-165	-163[5]	dBc/Hz
			35MHz offset		-166	-164[5]	dBc/Hz
		GSM900	20MHz offset		-165	-163[5]	dBc/Hz
			35MHz offset		-166	-164[5]	dBc/Hz
		DCS1800	20MHz offset		-160	-156[5]	dBc/Hz
		PCS1900	20MHz offset		-160	-156[5]	dBc/Hz

Item	Symbol	Band	Test condition	Min.	Typ.	Max.	Unit
Output power level	P_{out}	GSM850 GSM900	PA driver amplifier R_{load} = 50Ω	1[1,2]	3	6[1,2]	dBm
		DCS1800 PCS1900		1[3,4]	3	6[3,4]	dBm
Output 3rd harmonics		ALL	PA driver amplifier		-10		dBc

Table 35. SX AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Frequency range	F_{range}		3,296		3,980	MHz
Reference frequency	F_{ref}			26		MHz
Frequency step resolution	F_{res}			3		Hz
Phase noise	PN_{10k}	@ 10kHz offset		-83		dBc/Hz
	PN_{400k}	@ 400kHz offset		-114		dBc/Hz
	PN_{3M}	@ 3MHz offset		-136		dBc/Hz
Lock time of Rx burst	T_{lock_rx}	Frequency error < ± 0.1ppm		150	200[5]	us
Lock time of Tx burst	T_{lock_tx}	Frequency error < ± 0.1ppm		200	300[5]	us
Pushing figure		With internal RFVCO LDO		400		kHz/V

Table 36. DCXO AC characteristics (TA = 25oC, VDD = 2.8V unless otherwise stated)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit
Operating frequency	F_{ref}			26		MHz
Crystal C load	C_L			7.5		pF
Crystal tuning sensitivity	T_S		27.5	32.3		ppm/pF
Static range	SR	CDAC from 0 to 255	± 22	± 50		ppm
Dynamic range	DR	CAFC from 0 to 8191	36	50		ppm
AFC tuning step	$F_{res-AFC}$			0.008		ppm/DAC
AFC settling time	T_{AFC}	CAFC from 0 to 8191 CAFC from 8191 to 0 Frequency error < 0.1ppm		100	200[5]	us
Start-up time	T_{DCXO}	Frequency error < 1ppm Amplitude > 90 %			4[5]	ms
Pushing figure				0.2		ppm/V
Fref buffer output level	V_{Fref}	Max. loading = 19pF	0.8[5]			V_{p-p}
Fref buffer output phase noise		10kHz offset Jitter noise		-135		dBc/Hz

[1, 2]: Tested at E-GSM Tx channel 0 and GSM850 Rx channel 190.
[3, 4]: Tested at PCS Tx channel 601 and DCS Rx channel 636.
[5]: Not subject to production test – verified by characterization and design.

2.8 Bluetooth

2.8.1 Block Description

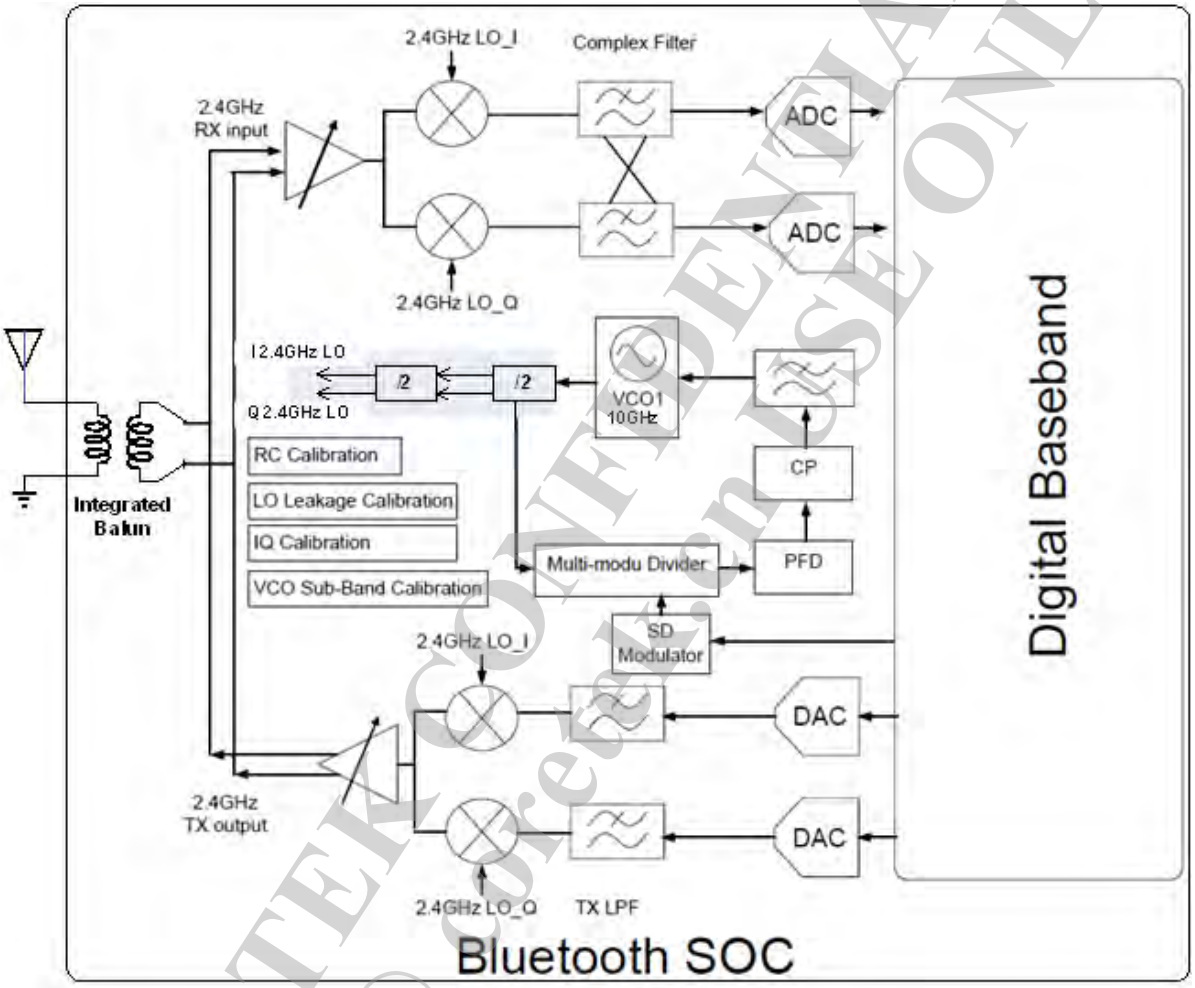


Figure 15. System diagram of Bluetooth RF transceiver

The Bluetooth RF subsystem contains a fully integrated transceiver.

For TX path, the baseband transmit data are digitally modulated in the baseband processor then up-converted to 2.4GHz RF channels through DA converter, filter, IQ up-converter and power amplifier. The power amplifier is capable of transmitting 7.5dBm power for class-1 operation.

For RX path, MT2503A is a low IF receiver architecture. An image-reject mixer down-converts the RF signal to the IF with LO from the synthesizer, which supports different clock frequencies as the reference clock. The mixer output is then converted to digital signal and down-converted to baseband for demodulation. A fast AGC enables effective discovery of device within dynamic range of the receiver.

MT2503A features self calibration schemes to compensate the process and temperature variation to maintain high performance. Those calibrations are performed automatically right after system boot-up.

2.8.2 Functional Specifications

2.8.2.1 Basic Data Rate – Receiver Specifications

Table 37. Basic data rate – receiver specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Receiver sensitivity	BER < 0.1%	-	-95	-	dBm
	Max. detectable input power	BER < 0.1%	-	0	-	dBm
	C/I co-channel selectivity	BER < 0.1%	-	4	-	dB
	C/I 1 MHz adj. channel selectivity	BER < 0.1%	-	-12	-	dB
	C/I 2 MHz adj. channel selectivity	BER < 0.1%	-	-42.5	-	dB
	C/I ≥ 3 MHz adj. channel selectivity	BER < 0.1%	-	-46	-	dB
	C/I image channel selectivity	BER < 0.1%	-	-24	-	dB
	C/I image 1 MHz adj. channel selectivity	BER < 0.1%	-	-45	-	dB
	Out-of-band blocking	30 to 2,000 MHz	-	-4	-	dBm
		2,000 to 2,399 MHz	-	-18	-	dBm
		2,498 to 3,000 MHz	-	-18	-	dBm
		3,000 MHz to 12.75 GHz	-	1	-	dBm
	Intermodulation		-	-22	-	dBm

2.8.2.2 Basic Data Rate – Transmitter Specification

Table 38. Basic data rate – transmitter specification

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Maximum transmit power		-	7.5	-	dBm
	Gain step		-	4	-	dB
	Δf1avg (00001111)		140	158	175	kHz
	Δf2max (10101010)		115	130	-	kHz
	Δf1avg/Δf2avg		0.8	0.9	-	kHz
	Initial carrier frequency drift		-75	5	75	kHz
	Frequency drift	DH1	-25	9	25	kHz
		DH3	-40	10	40	kHz

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		DH5	-40	10	40	kHz
	Max. drift rate		-	100	400	Hz/µs
	BW_{20dB} of Tx output spectrum		-	920	1,000	kHz
	In-band spurious emission	±2 MHz offset	-	-38	-	dBm
		±3 MHz offset	-	-43	-	dBm
		> ±3 MHz offset	-	-43	-	dBm
	Out-of-band spurious emission	30 MHz to 1 GHz	-	-36	-	dBm
		1 to 12.75 GHz	-	-30	-	dBm
		1.8 to 1.9 GHz	-	-47	-	dBm
		5.15 to 5.3 GHz	-	-47	-	dBm

2.8.2.3 Enhanced Data Rate – Receiver Specifications

Table 39. Enhanced data rate – receiver specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Receiver sensitivity	π/4 DQPSK, BER < 0.01%	-	-95	-	dBm
		8PSK, BER < 0.01%	-	-88	-	dBm
	Max. detectable input power	π/4 DQPSK, BER < 0.01%	-	-4.5	-	dBm
		8PSK, BER < 0.01%	-	-4.5	-	dBm
	C/I co-channel selectivity	π/4 DQPSK, BER < 0.01%	-	8	-	dB
		8PSK, BER < 0.01%	-	14.5	-	dB
	C/I 1MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-13	-	dB
		8PSK, BER < 0.01%	-	-7	-	dB
	C/I 2MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-42	-	dB
		8PSK, BER < 0.01%	-	--41.5	-	dB
	C/I ≥ 3MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-48	-	dB
		8PSK, BER < 0.01%	-	-44.5	-	dB
	C/I image channel selectivity	π/4 DQPSK, BER < 0.01%	-	-30	-	dB
		8PSK, BER < 0.01%	-	-23	-	dB
	C/I image 1 MHz adj. channel selectivity	π/4 DQPSK, BER < 0.01%	-	-47.5	-	dB
		8PSK, BER < 0.01%	-	-44.5	-	dB

2.8.2.4 Enhanced Data Rate – Transmitter Specifications

Table 40. Enhanced data rate – transmitter specifications

Symbol	Description	Condition	Min.	Typ.	Max.	Unit

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Frequency range		2,402	-	2,480	MHz
	Max. transmit power	π/4 DQPSK	-	4.5	-	dBm
		8PSK	-	4.5	-	dBm
	Relative transmit power	π/4 DQPSK	-	-1.7	-	dB
		8PSK	-	-1.7	-	dB
	Freq. stability ω_0	π/4 DQPSK	-	1.5	-	kHz
		8PSK	-	1.5	-	kHz
	Freq. stability ω_1	π/4 DQPSK	-	3	-	kHz
		8PSK	-	3	-	kHz
	$\lvert \omega_0+\omega_1 \rvert$	π/4 DQPSK	-	2.8	-	kHz
		8PSK	-	2.8	-	kHz
	RMS DEVM	π/4 DQPSK	-	7	-	%
		8PSK	-	6	-	%
	99% DEVM	π/4 DQPSK	-	11	-	%
		8PSK	-	11	-	%
	Peak DEVM	π/4 DQPSK	-	18	-	%
		8PSK	-	18	-	%
	In-band spurious emission	π/4 DQPSK, ±1 MHz offset	-	-28	-	dBm
		8PSK, ±1 MHz offset	-	-28	-	dBm
		π/4 DQPSK, ±2 MHz offset	-	-25	-	dBm
		8PSK, ±2 MHz offset	-	-25	-	dBm
		π/4 DQPSK, ±3 MHz offset	-	-40.5	-	dBm
		8PSK, ±3 MHz offset	-	-40.5	-	dBm

Note: To meet the specifications, use a front-end band-pass filter.

2.9 FM RF

2.9.1 Block Description

The connection between internal modules, as well as external interfaces, are as shown in Figure 16. The FM receiver section incorporates the complete receiving path with wide tuning range. The FM baseband signal processor incorporates the digital demodulator and audio processing function which provides superior audio quality.

FM contains completely integrated FM audio receiver functions (RDS/RBDS may also be supported depending on the model number). The integrated receiver enables superior sensitivity, ACI performance and FM audio performances with minimum external BOM.

The FM subsystem supports either high performance stereo analog line out or digital audio output (I2S).

For models supporting RDS/RBDS, large dedicated internal data buffers are allocated to reduce the frequency of the interrupt to the host, so that the receiving host can enter low power states efficiently.

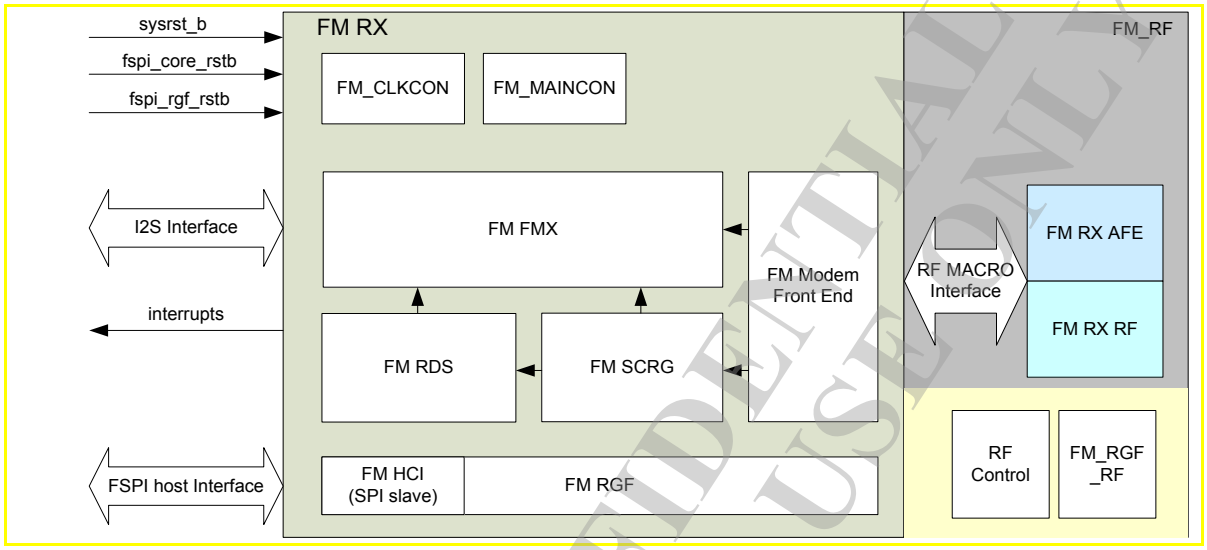


Figure 16. Block diagram of hardware top-level architecture

2.9.2 Functional Specifications

Table 41. FM receiver DC characteristics (TA=25°C, VDD=2.8V unless otherwise stated)

Operating mode	Current consumption	Unit
Idle	5	µA
FM receiver	12	mA

Unless otherwise stated, all receiver characteristics are applicable to both long and short antenna ports when operated under the recommended operating conditions. Typical specifications are for channel 98.7MHz, default register settings and under recommended operating conditions. The minimum and maximum specifications are for extreme operating voltage and temperature conditions, unless otherwise stated.

Table 42. FM receiver AC characteristics

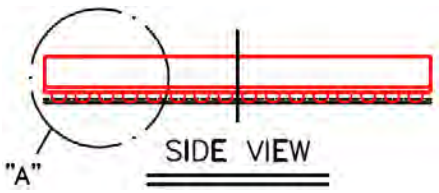
Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	Input frequency range		65		108	MHz
	Sensitivity (long antenna)[1,3]	SINAD = 26dB, unmatched		3		dBµVemf
		SINAD = 26dB, matched		2		dBµVemf
	RDS sensitivity (long antenna)	Δf=2kHz, BLER < 5%, unmatched		18		dBµVemf
	Sensitivity (short antenna)[1,3]	SINAD = 26dB, unmatched		3		dBµVemf
	RDS sensitivity (short antenna)	Δf = 2kHz, BLER < 5%, unmatched		18		dBµVemf

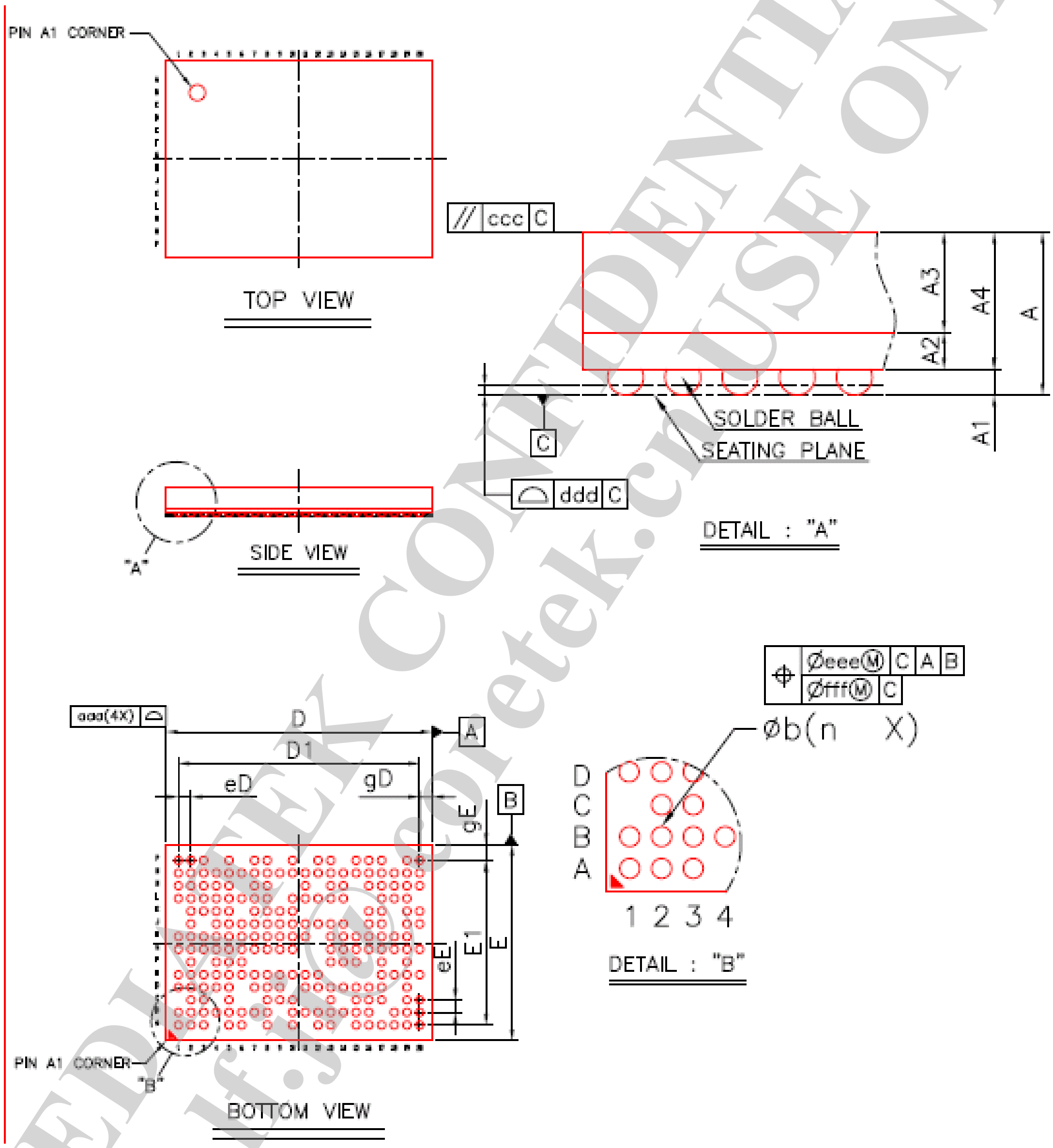
Symbol	Description	Condition	Min.	Typ.	Max.	Unit
	LNA input resistance[4]	Antenna port		2.4k		Ohm
	LNA input capacitance[4]	Antenna port		8		pF
	AM suppression[1,4]	M = 0.3		58		dB
	Adjacent channel selectivity[1,4]	±200kHz		53		dB
	Alternate channel selectivity[1,4]	±400kHz		65		dB
	Spurious response rejection[4]	In-band		55		dB
	Maximum input level			117		dBμVemf
	Audio mono (S+N+D)/(N+D)[1,3,4]			60		dB
	Audio stereo (S+N+D)/(N+D)[2,3,4]			52		dB
	Audio stereo separation[4]	Δf = 75kHz		45		dB
	Audio output load resistance	Single-ended at AFR/AFL outputs		10k		Ohm
	Audio output load capacitance	Single-ended at AFR/AFL outputs		12.5		pF
	Audio output voltage[1,4]	At AFR/AFL outputs		80		mVrms
	Audio output THD[1,4]			0.05	0.1	%
	Audio output frequency range	3dB corner frequency	30		15k	Hz

[1] Δf = 22.5kHz, fm = 1kHz, 50μs de-emphasis, mono, L = R
[2] Δf = 22.5kHz, fm = 1kHz, 50us de-emphasis, stereo
[3] A-weighting, BW = 300 Hz to 15 kHz
[4] Vin = 60dBμVemf
[5] Reference clock accuracy assumes ideal FM source. If the input FM source has less frequency error, it is recommended to use a reference clock of accuracy within ±100ppm so as not to affect the channel scan quality.

2.10 Package Information

2.10.1 Package Outlines





Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package Type			VFBGA		
Body Size	X	D	8.30	8.40	8.50
	Y	E	6.10	6.20	6.30
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.65 Ref.	
Substrate Thickness		A2		0.13 Ref.	
Substrate+Mold Thickness		A4	0.73	0.78	0.83
Total Thickness		A	—	—	1.00
Ball Diameter				0.25	
Ball Stand Off		A1	0.110	0.150	0.190
Ball Width		b	0.220	0.270	0.320
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		215	
Edge Ball Center to Center	X	D1		7.60	
	Y	E1		5.20	
Edge Ball Center to Package Edge	X	gD		0.40	
	Y	gE		0.50	

Figure 17. Outlines and dimension of TFBGA 8.4mm*6.2mm, 215-ball, 0.4mm pitch package

2.10.2 Thermal Operating Specifications

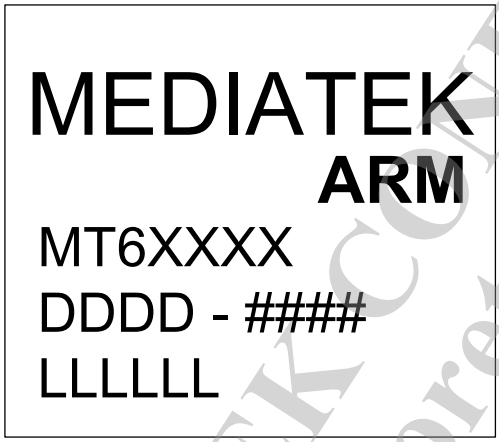
Symbol	Description	Value	Unit	Notes
	Thermal resistance from device junction to package case	48	C/W	
	Maximum package temperature	65	Deg C	
	Maximum power dissipation	1.28	W	

2.10.3 Lead-free Packaging

MT2503A is provided in a lead-free package and meets RoHS requirements

2.11 Ordering Information

2.11.1 Top Marking Definition



MTXXXXXX Product No.
DDDD: Date Code
####: Subcontractor Code
LLLLLL: Die Lot No.

Figure 18. Mass production top marking of MT2503A

Part number	Package	Description
MT2503AA/B	TFBGA	8.4mm*6.2mm, 215-ball, 0.4mm pitch package, non-security version

3 Micro-Controller Unit Peripherals

3.1 Pulse-Width Modulation Outputs (2 Channel)

3.1.1 General Description

2 generic pulse-width modulators are implemented to generate pulse sequences with programmable frequency and duty cycles for LCD backlight. As long as the internal counter value is bigger than or equal to the threshold value, the duration of the PWM output signal is LOW. The waveform is shown in Figure 19.

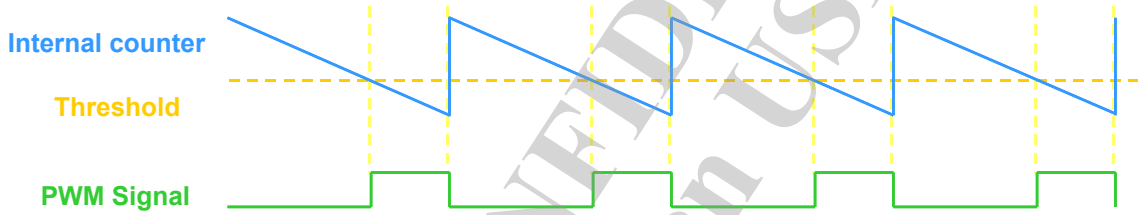


Figure 19. PWM waveform

The frequency and volume of the PWM output signal are determined by PWM1_COUNT, PWM1_THRES and PWM1_CON. The POWERDOWN (pdn1_pwm) signal is applied to power-down the PWM_1ch module. When PWM_1ch is deactivated (pwm1_pdn=1), the output is in the LOW state.

The output PWM frequency is determined by:

$$\frac{CLK}{CLOCK\_DIV \times (PWM\_COUNT + 1)} \quad \text{CLK} = 13000000 \text{ when CLKSEL} = 0, CLK = 32000 when CLKSEL = 1$$

CLOCK_DIV = 1, when CLK[1:0] = 00b
CLOCK_DIV = 2, when CLK[1:0] = 01b
CLOCK_DIV = 4, when CLK[1:0] = 10b
CLOCK_DIV = 8, when CLK[1:0] = 11b

The output PWM duty cycle is determined by: $\frac{PWM\_THRES}{PWM\_COUNT + 1}$

Note: PWM_THRES should be less than the PWM_COUNT. If this condition is not satisfied, the output pulse of the PWM will always be HIGH.

Figure 20 shows the PWM waveform with the indicated register values.

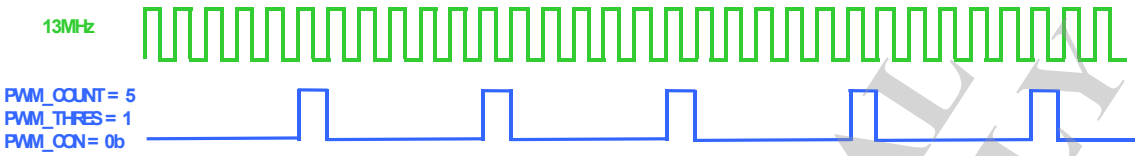


Figure 20. PWM waveform with register values

3.1.2 Register Definition

Module name: Pulse Width Modulation base address: (+A00E0000h)

Address	Name	Width	Register function
A00E0000	PWM1_CTRL_ADDR	16	PWM1 control register
A00E0004	PWM1_COUNT_ADDR	16	PWM1 max counter value register
A00E0008	PWM1_THRESH_ADDR	16	PWM1 threshold value register

A00E0000 PWM1_CTRL_ADDR PWM1 Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PWM1_CLK_SEL	PWM1_CLK_DIV	
Type														RW	RW	
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	PWM1_CLK_SEL	CLK_SEL	**Selects source clock frequency of PWM1** 0: CLK = 13MHz 1: CLK = 32kHz
1:0	PWM1_CLK_DIV	CLK_DIV	**Selects clock prescaler scale of PWM1** 2'b00: f = fclk 2'b01: f = fclk/2 2'b10: f = fclk/4 2'b11: f = fclk/8

A00E0004 PWM1_COUNT_ADDR PWM1 Max. Counter Value Register 1FFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM1_COUNT												
Type				RW												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
12:0	PWM1_COUNT	PWM1_COUNT	**PWM1 maximum counter value** This value is the initial value of the internal counter. Regardless of the operation mode, if PWM1_COUNT is written while the internal counter is counting backwards, the new initial value will not take effect until the internal counter counts down to 0, i.e. a complete period.

A00E0008 PWM1_THRESH_ADDR PWM1 Threshold Value Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM1_THRES												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	PWM1_THRES	PWM1_THRES	**PWM1 threshold value** When the internal counter value is bigger than or equal to PWM1_THRES, the PWM1 output signal will be "0". When the internal counter is less than PWM1_THRES, the PWM1 output signal will be "1".

Module name: Pulse Width Modulation base address: (+A0280000h)

Address	Name	Width	Register function
A0280000	PMW4_CTRL_ADDR	16	PMW4 control register
A0280004	PMW4_COUNT_ADDR	16	PMW4 max counter value register
A0280008	PMW4_THRESH_ADDR	16	PMW4 threshold value register

A0280000 PMW4_CTRL_ADDR PMW4 Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PMW4_CLK_SEL	PMW4_CLK_DIV	
Type														RW	RW	
Reset														0	0	0

Bit(s)	Mnemonic	Name	Description
2	PMW4_CLK_SEL	CLK_SEL	**Selects source clock frequency of PMW4** 0: CLK = 13MHz 1: CLK = 32kHz
1:0	PMW4_CLK_DIV	CLK_DIV	**Selects clock prescaler scale of PMW4** 2'b00: f = fclk 2'b01: f = fclk/2 2'b10: f = fclk/4 2'b11: f = fclk/8

A0280004 PMW4_COUNT_ADDR PMW4 Max. Counter Value Register 1FFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PMW4_COUNT												
Type				RW												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Mnemonic	Name	Description
12:0	**PMW4_COUNT**	PMW4_COUNT	**PMW4 maximum counter value** This value is the initial value of the internal counter. Regardless of the operation mode, if PMW4_COUNT is written while the internal counter is counting backwards, the new initial value will not take effect until the internal counter counts down to 0, i.e. a complete period.

A0280008 PMW4_THRESH_ADDR PMW4 Threshold Value Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PMW4_THRES												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
12:0	**PMW4_THRES**	PMW4_THRES	**PMW4 threshold value** When the internal counter value is bigger than or equal to PMW4_THRES, the PMW4 output signal will be "0". When the internal counter is less than PMW4_THRES, the PMW4 output signal will be "1".

Module name: PWM_2CH base address: (+A0740000h)

Address	Name	Width	Register Function
A074000C	PWM2_CTRL	16	**PWM2 control register** Selects CLK SRC and prescaler scale.
A0740014	PWM2_THRES	16	**PWM2 threshold value register** Controls the duty of waveform
A0740018	PWM3_CTRL	16	**PWM3 control register** Select CLK SRC and prescaler scale.
A074001C	PWM3_COUNT	16	**PWM3 max counter value register** Configures internal counter's max. value
A0740020	PWM3_THRES	16	**PWM3 threshold value register**

A074000C PWM2_CTRL PWM2 Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														PWM2_CLK_SEL		
Type														RW		
Reset														1		

Bit(s)	Name	Description
2	PWM2_CLK_SEL	**Selects PWM2 CLK** 0: CLK = 13M CLK 1: CLK = 32k CLK

A0740014 PWM2_THRES PWM2 Threshold Value Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name															PWM2_THRES	
Type															RW	
Reset															0	0

Bit(s)	Name	Description
1:0	PWM2_THRES	**PWM2 threshold value** 0: Duty = 0% 1: Duty = 50% 2: Duty = 100%

A0740018 PWM3_CTRL PWM3 Control Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													PWM3_ALWAYS_HIGH	PWM3_CLK_SEL	PWM3_CLK_DIV	
Type													RW	RW	RW	
Reset													0	0	0	0

Bit(s)	Name	Description
3	PWM3_ALWAYS_HIGH	**When pwm3_thresh is set to be bigger than pwm3_width, which means the PWM output is always high, the driver should set this register to 1.** It is specially used by ISINK. 0: Duty! = 100% 1: Duty = 100%
2	PWM3_CLK_SEL	**Selects PWM3 CLK** 0: CLK = 13M CLK 1: CLK = 32k CLK
1:0	PWM3_CLK_DIV	**PWM3 CLK division** 2'b0: f = fclk 2'b1: f = fclk/2 2'b2: f = fclk/4 2'b3: f = fclk/8

A074001C PWM3_COUNT PWM3 Max Counter Value Register 1FFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM3_COUNT												
Type				RW												
Reset				1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
12:0	PWM3_COUNT	**PWM3 maximum counter value** This value is the initial value of the internal counter. Regardless of the operation mode, if PWM3_COUNT is written while the internal counter is counting backwards, the new initial value will not take effect until the internal

Bit(s)	Name	Description
		counter counts down to 0, i.e. a complete period.

A0740020 PWM3_THRES PWM3 Threshold Value Register 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				PWM3_THRES												
Type				RW												
Reset				0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
12:0	PWM3_THRES	**PWM3 threshold value** When the internal counter value is bigger than or equal to PWM3_THRES, the PWM3 output signal will be 0. When the internal counter is less than PWM3_THRES, the PWM3 output signal will be 1.

3.2 SIM Interface

MT2503A contains two dedicated smart card interfaces to allow the MCU to access two SIM cards. Each interface can operate via 5 terminals. See Figure 21, SIMVCC, SIMSEL, SIMRST, SIMCLK and SIMDATA are for one SIM interface, and SIM2VCC, SIM2SEL, SIM2RST, SIM2CLK and SIM2DATA are for the other SIM interface.

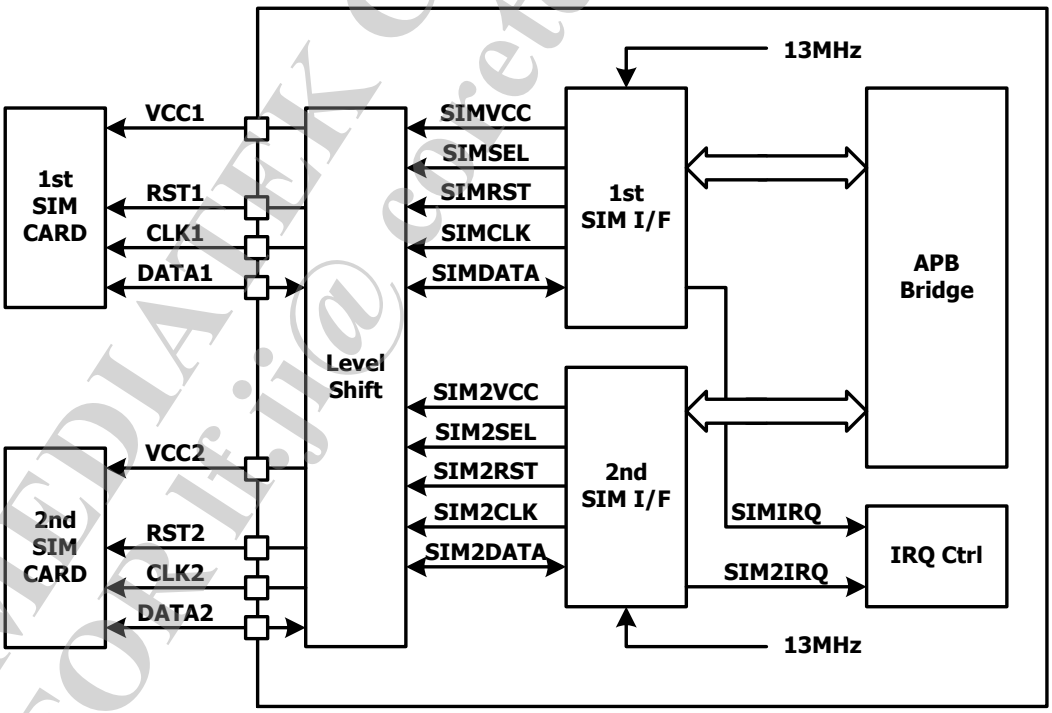


Figure 21.** Block diagram of **SIM interface

The functions of the two SIM interfaces are identical; therefore, only the first SIM interface will be described in this document. SIMVCC is used to control the external voltage supply to the SIM card, and SIMSEL determines the regulated smart card supply voltage. SIMRST is used as the SIM card reset signal. Besides, SIMDATA and SIMCLK are used for data exchange.

The SIM interface is a half duplex asynchronous communication port, and its data format is composed of ten consecutive bits: a start bit in state “low”, eight information bits and a tenth bit used for parity checking. The data format can be divided into two modes as follows:

- Direct convention mode (ODD = SDIR = SINV = 0)

  SB D0 D1 D2 D3 D4 D5 D6 D7 PB
  SB: Start bit (in state “low”)
  Dx: Data byte (LSB is the first and logic level ONE is in state “high”)
  PB: Even parity check bit

- Inverse convention mode (ODD = SDIR = SINV = 1)

  SB N7 N6 N5 N4 N3 N2 N1 N0 PB
  SB: Start bit (in state “low”)
  ***Nx*:** Data byte (MSB is the first and logic level ONE is in state “low”)
  PB: Odd parity check bit

If the receiver obtains a wrong parity bit, it will respond by pulling the SIMDATA “low” to inform the transmitter, and the transmitter will retransmit the character.

If the receiver is an SIM card, the error response will start 0.5 bit after the PB and may last for 1 ~ 2-bit period. If the receiver is an SIM interface, the error response will start 0.5 bit after the PB and last for 1.5-bit period.

If the SIM interface is a transmitter, it will take total 14 bits guard period wherever the error response appears. If the receiver shows the error response, the SIM interface will retransmit the previous character again, or it will transmit the next character.

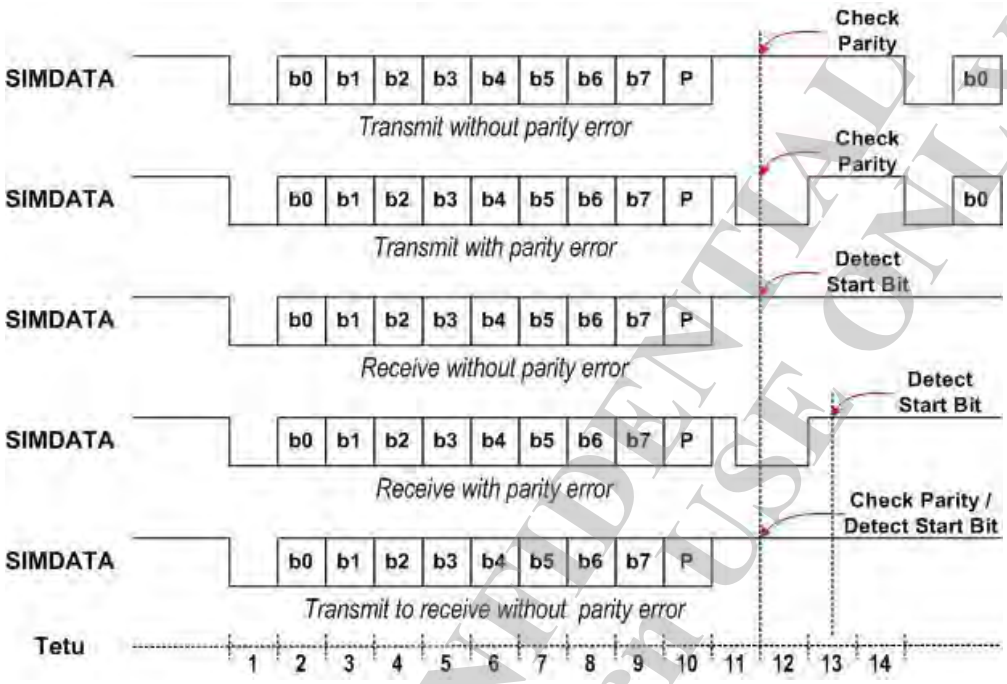


Figure 22. Timing diagram of SIM interface

3.2.1 Register Definition

When the MCU controls two SIM card interfaces, all registers will be duplicated to two copies but with different base address. n = "0" is for the 1st SIM card interface; n=1 is for the 2nd SIM card interface. For example, address SIMIF0+0000h is mapped to the SIMIF0_SIM_CTRL register while address SIMIF1+0000h is mapped to the SIMIF1_SIM_CTRL register.

3.2.1.1 Register Overview

MCU register address (hex)	Acronym	Description
1st SIM card interface		
SIMIF0+0000h	SIMIF0_SIM_CTRL	Control register
SIMIF0+0004h	SIMIF0_SIM_CONF	Configuration register
SIMIF0+0008h	SIMIF0_SIM_BRR	Baudrate register
SIMIF0+0010h	SIMIF0_SIM_IRQEN	Interrupt enabling register
SIMIF0+0014h	SIMIF0_SIM_STS	Status register
SIMIF0+0018h	SIMIF0_SIM_CLR_STA	SIM clear status
SIMIF0+0020h	SIMIF0_SIM_RETRY	Retry limit register
SIMIF0+0024h	SIMIF0_SIM_TIDE	FIFO tide mark register
SIMIF0+0030h	SIMIF0_SIM_DATA	TX/RX data register

MCU register address (hex)	Acronym	Description
SIMIF0+0034h	SIMIF0_SIM_COUNT	FIFO count register
SIMIF0+0040h	SIMIF0_SIM_ATIME	Activation time register
SIMIF0+0044h	SIMIF0_SIM_DTIME	Deactivation time register
SIMIF0+0048h	SIMIF0_SIM_TOUT	Character to character waiting time register
SIMIF0+004Ch	SIMIF0_SIM_GTIME	Block to block guard time register
SIMIF0+0050h	SIMIF0_SIM_ETIME	Block to error signal time register
SIMIF0+0054h	SIMIF0_SIM_EXT_TIME	Extend data I/O state switch time register
SIMIF0+0058h	SIMIF0_SIM_CGTIME	Character to character guard time register
SIMIF0+0060h	SIMIF0_SIM_INS	Command header register : INS
SIMIF0+0064h	SIMIF0_SIM_IMP3	Command header register : P3
SIMIF0+0068h	SIMIF0_SIM_SW1	Procedure byte register : SW1
SIMIF0+006Ch	SIMIF0_SIM_SW2	Procedure byte register : SW2
SIMIF0+0070h	SIMIF0_SIM_ATRSTA	ATR state register
SIMIF0+0074h	SIMIF0_SIM_STATUS	Protocol state register
SIMIF0+0080h	SIMIF0_SIM_DMADATA	TX/RX data register for DMA
SIMIF0+0090h	SIMIF0_SIM_DBG	Debug register
SIMIF0+0094h	SIMIF0_SIM_DBGDATA	FIFO data debug register
SIMIF0+00A0h	SIMIF0_SIM_SCLK	SCLK PAD control register
SIMIF0+00A4h	SIMIF0_SIM_SRST	SRST PAD control register
SIMIF0+00A8h	SIMIF0_SIM_SIO	SIO PAD control register
SIMIF0+00ACh	SIMIF0_SIM_MON	PAD monitor register
SIMIF0+00B0h	SIMIF0_SIM_SEL	Testing output select
2nd SIM card interface		
SIMIF1+0000h	SIMIF1_SIM_CTRL	Control register
SIMIF1+0004h	SIMIF1_SIM_CONF	Configuration register
SIMIF1+0008h	SIMIF1_SIM_BRR	Baudrate register
SIMIF1+0010h	SIMIF1_SIM_IRQEN	Interrupt enabling register
SIMIF1+0014h	SIMIF1_SIM_STS	Status register
SIMIF1+0018h	SIMIF1_SIM_CLR_STA	Sim clear status
SIMIF1+0020h	SIMIF1_SIM_RETRY	Retry limit register
SIMIF1+0024h	SIMIF1_SIM_TIDE	FIFO tide mark register
SIMIF1+0030h	SIMIF1_SIM_DATA	TX/RX data register
SIMIF1+0034h	SIMIF1_SIM_COUNT	FIFO count register
SIMIF1+0040h	SIMIF1_SIM_ATIME	Activation time register
SIMIF1+0044h	SIMIF1_SIM_DTIME	Deactivation time register
SIMIF1+0048h	SIMIF1_SIM_TOUT	Character to character waiting time register
SIMIF1+004Ch	SIMIF1_SIM_GTIME	Block to block guard time register
SIMIF1+0050h	SIMIF1_SIM_ETIME	Block to error signal time register
SIMIF1+0054h	SIMIF1_SIM_EXT_TIME	Extend data I/O state switch time register
SIMIF1+0058h	SIMIF1_SIM_CGTIME	Character to character guard time register
SIMIF1+0060h	SIMIF1_SIM_INS	Command header register : INS

MCU register address (hex)	Acronym	Description
SIMIF1+0064h	SIMIF1_SIM_IMP3	Command header register : P3
SIMIF1+0068h	SIMIF1_SIM_SW1	Procedure byte register : SW1
SIMIF1+006Ch	SIMIF1_SIM_SW2	Procedure byte register : SW2
SIMIF1+0070h	SIMIF1_SIM_ATRSTA	ATR state register
SIMIF1+0074h	SIMIF1_SIM_STATUS	Protocol state register
SIMIF1+0080h	SIMIF1_SIM_DMADATA	TX/RX data register for DMA
SIMIF1+0090h	SIMIF1_SIM_DBGD	Debug register
SIMIF1+0094h	SIMIF1_SIM_DBGDATA	FIFO data debug register
SIMIF1+00A0h	SIMIF1_SIM_SCLK	SCLK PAD control register
SIMIF1+00A4h	SIMIF1_SIM_SRST	SRST PAD control register
SIMIF1+00A8h	SIMIF1_SIM_SIO	SIO PAD control register
SIMIF1+00ACh	SIMIF1_SIM_MON	PAD monitor register
SIMIF1+00B0h	SIMIF1_SIM_SEL	Testing output select

3.2.1.2 Register Description

SIMn+0000h SIM Module Control Register **SIMIFN_SIM_CTRL**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										VCCCTRL	VCCLV	RSTCTRL	RSTLV	WRST	CSTOP	SIMON
Type										R/W	R/W	R/W	R/W	W	R/W	R/W
Reset										0	0	0	0	0	0	0

SIMON Conrols SIM card power-up/power-down
0 1-to-0 change will start the card deactivation sequence.
1 0-to-1 change will start the card activation sequence.

CSTOP Enables clock stop mode. Together with CPOL in the SIM_CONF register, it determines the polarity of SIMCLK in this mode.
0 Enable SIMCLK output
1 Disable SIMCLK outpu

WRST Controls SIM card warm reset

RSTLV Controls SIMRST parking level in SIMRST direct control mode

RSTCTRL Enables SIMRST direct control mode

VCCLV Controls SIMVCC parking level in SIMVCC direct control mode

VCCCTRL Enables SIMVCC direct control mode

SIMn+0004h SIM Module Configuration Register **SIMIFN_SIM_CONF**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			T1TX2RXEN	TXRDIS	RXRDIS	HFEN	T0EN	T1EN	TOUT	SIMSEL	ODD	SDIR	SINV	CPOL	TXACK	RXACK
Type			R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

RXACK Handshaking control of SIM card reception error
- **0** Disable character receipt handshaking
- **1** Enable character receipt handshaking

TXACK Handshaking control of SIM card transmission error
- **0** Disable character transmission handshaking
- **1** Enable character transmission handshaking

CPOL SIMCLK polarity control in clock stop mode
- **0** Make SIMCLK stop in “low” level
- **1** Make SIMCLK stop in “high” level

SINV Data inversion mode
- **0** Does not invert the transmitted and received data; data logic ONE is in “high” state
- **1** Invert the transmitted and received data; data logic ONE is in “low” state

SDIR Direction of data transfer
- **0** LSB is transmitted and received first.
- **1** MSB is transmitted and received first.

ODD Selecting odd or even parity
- **0** Even parity
- **1** Odd parity

SIMSEL Selects SIM card supply voltage (also configure SIMSEL in PMU register)
- **0** SIMSEL pin is set to “low” level, 1.8V
- **1** SIMSEL pin is set to “high” level, 3V

TOUT Controls SIM work waiting time counter
- **0** Disable time-out counter
- **1** Enable time-out counter

T1EN Controls T = 1 protocol controller
- **0** Disable T = 1 protocol controller
- **1** Enable T = 1 protocol controller

T0EN Controls T = 0 protocol controller
- **0** Disable T = 0 protocol controller
- **1** Enable T = 0 protocol controller

HFEN Controls hardware flow
- **0** Disable hardware flow control
- **1** Enable hardware flow control

RXRDIS Disables RX DMA request
- **0** Enable RX DMA request (default)
  RXRDIS must be set to 0 for protocol T = 1
- **1** Disable RX DMA request
  During TX transmission and not protocol T = 1, the recommended setting of RXRDIS is 1

TXRDIS Disables TX DMA request disable
- **0** Enable TX DMA request (default)
  TXRDIS must be set to 0 for protocol T = 1
- **1** Disable TX DMA request

During RX transmission and not protocol T = 1, the recommended setting of TXRDIS is 1.

T1TX2RXEN Enables DMA type auto switch for protocol T = 1 (this function is not supported in MT6260)

0 Disable DMA type auto switch function

If the current block is TX transmission and the next block is also TX transmission, disabling this bit is recommended

1 Enable DMA type auto switch function

If the current block is TX transmission and the next block is RX transmission, enabling this bit is recommended to improve transmission quality

SIMn +0008h SIM Baudrate Register **SIMIFN_SIM_BRR**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						ETU[8:0]									SIMCLK[1:0]	
Type						R/W									R/W	
Reset						372d									01	

SIMCLK Sets up SIMCLK frequency

00 Reserved

01 13/4 MHz

10 13/8 MHz

11 13/12 MHz

ETU Determines duration of elementary time unit in SIMCLK unit

The minimum valid setting of ETU is 8

SIMn +0010h SIM Interrupt Enable Register **SIMIFN_SIM_IRQEN**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					UDRUN	EDCERR	T1END	RXERR	T0END	SIMOFF	ATRERR	TXERR	TOUT	OVRUN	RXTIDE	TXTIDE
Type					R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset					0	0	0	0	0	0	0	0	0	0	0	0

For all the bits

0 Disable interrupt

1 Enable interrupt

SIMn +0014h SIM Module Status Register **SIMIFN_SIM_STS**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					UDRUN	EDCERR	T1END	RXERR	T0END	SIMOFF	ATRERR	TXERR	TOUT	OVRUN	RXTIDE	TXTIDE
Type					R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R/C	R	R
Reset				-	-	-	-	-	-	-	-	-	-	-	-	-

TXTIDE The interrupt occurs when the number of transmitted data in the FIFO is less than the transmitted tide.
RXTIDE The interrupt occurs when the number of received data in the FIFO is less than the received tide.
OVRUN Receiving FIFO overflow interrupt occurrs.
TOUT Between characters time-out interrupt occurs.
TXERR Character transmission error interrupt occurs.
ATRERR ATR start time-out interrupt occurrs.
SIMOFF Card deactivation completed interrupt occurs.
T0END Data transfer handled by T = 0 controller completed interrupt occurs.
RXERR Character reception error interrupt occurrs.
T1END Data transfer handled by T = 1 controller completed interrupt occurs.
EDCERR T = 1 controller CRC error occurs.
UDRUN FIFO underflow interrupt occurs (still reading FIFO when FIFO is empty).

SIMn +0018h SIM Clear Status Register **SIMIFN_SIM_CLR_STA**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																CLR_STA
Type																RO
Reset																0

CLA_STA 1: Clear SIMIF. Do not write to SIMIF; 0: SIMIF clear finished or not in clear status, you can write data to SIMIF.

SIMn +0020h SIM Retry Limit Register **SIMIFN_SIM_RETRY**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TXRETRY[2:0]									RXRETRY[2:0]		
Type					R/W									R/W		
Reset					3h									3h		

RXRETRY Specifies maximum number of receive retries allowed when parity error occurrs.
TXRETRY Specifies maximum number of transmit retries allowed when parity error occurrs.

SIMn +0024h SIM FIFO Tide Mark Register **SIMIFN_SIM_TIDE**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TXTIDE[3:0]								RXTIDE[3:0]			
Type					R/W								R/W			
Reset					0h								0h			

RXTIDE Trigger point of RXTIDE interrupt
TXTIDE Trigger point of TXTIDE interrupt

SIMn +0030h Data Register Used As Tx/Rx Data Register SIMIFN_SIM_DATA

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									DATA[7:0]							
Type									R/W							
Reset									-							

DATA Eight data digits, corresponding to the character being read or written

SIMn +0034h SIM FIFO Count Register SIMIFN_SIM_COUNT

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												COUNT[4:0]				
Type												R/W				
Reset												0h				

COUNT Number of characters in the SIM FIFO when read and flushes when written.

SIMn +0040h SIM Activation Time Register SIMIFN_SIM_ATIME

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							ATIME[9:0]									
Type							R/W									
Reset							2BEh									

ATIME Defines the duration, in 64 SIM clock cycles, of the time taken for each of the three stages of the card activation process, from SIMON transiting to “high” to turning on VCC, from turning on VCC to pull data “high” and then from pulling data “high” to turning on CLK.

SIMn +0044h SIM Deactivation Time Register SIMIFN_SIM_DTIME

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											DTIME[5:0]					
Type											R/W					
Reset											Fh					

DTIME Defines the duration, in 64 13 MHz clock cycles, of the time taken for each of the three stages of the card deactivation sequence, from pulling RST “low” to turning off CLK, from turning off CLK to pulling data “low”, from pulling data “low” to turning off VCC.

SIMn +0048h Character to Character Waiting Time Register SIMIFN_SIM_TOUT

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											WTIME[21:0]					

Type											R/W					
Reset											260h					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WTIME[21:0]															
Type	R/W															
Reset	260h															

WTIME Maximum interval between the leading edge of two consecutive characters in 16 ETU units

SIMn +004Ch Block to Block Guard Time Register **SIMIFN_SIM_GTIME**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													GTIME[3:0]			
Type													R/W			
Reset													10d			

GTIME Minimum interval between the leading edge of two consecutive characters sent in opposite directions in ETU unit

SIMn +0050h Block to Error Signal Time Register **SIMN_SIM_ETIME**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											ETIME[5:0]					
Type											R/W					
Reset											15d					

ETIME Defines the interval, in 1/16 ETU unit, between the end of the transmitted parity bit and the time to check the parity error signal sent from SIM card.

SIMn +0054h Active High Period Control Register **SIMIFN_SIM_EXT_TIME**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													EXT_TIME[3:0]			
Type													R/W			
Reset													1d			

EXT_TIME Defines the interval, in 1/16 ETU unit, between the end of the transmitted parity bit and the time to switch SIO to input mode. This value should be smaller than ETIME.

SIMn +0058h Character to Character Guard Time Register **SIMIFN_SIM_CGTIME**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									CGTIME[7:0]							
Type									R/W							
Reset									2h							

CGTIME Defines the minimum interval between the leading edges of two consecutive characters in ETU unit.
In the same transmission direction, the minimum interval is (12 + CGTIME) ETU. In opposite transmission direction, the minimum interval is (12 + CGTIME + GTIME) ETU.

SIMn +0060h SIM Command Header Register: INS **SIMIFN_SIM_INS**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								INSD	SIMINS[7:0]							
Type								R/W	R/W							
Reset								0h	0h							

SIMINS This field should be identical to the INS instruction code. When writing to this register, the T = 0 controller will be activated and data transfer initiated.

INSD Instruction direction

0 T = 0 controller receives data from the SIM card.

1 T = 0 controller sends data to the SIM card.

SIMn +0064h SIM Command Header Register: P3 **SIMIFN_SIM_IMP3 (ICC_LEN)**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								SIMP3[8]	SIMP3[7:0]							
Type								R	R/W							
Reset								0h	0h							

SIMP3 This field should be identical to the P3 instruction code. It should be written prior to the SIM_INS register. When the data transfer is being conducted, this field will show the number of the remaining data to be sent or to be received.

SIMn +0068h SIM Procedure Byte Register: SW1 **SIMIFN_SIM_SW1 (ICC_LEN)**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SIMSW1[7:0]							
Type									R							
Reset									0h							

SIMSW1 This field holds the last received procedure byte for debugging. When the T0END interrupt occurrs, it will keep the SW1 procedure byte.

SIMn +006Ch SIM Procedure Byte Register: SW2 **SIMIFN_SIM_SW2 (ICC_EDC)**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									SIMSW2[7:0]							

Type									R
Reset									0h

SIMSW2 This field holds the SW2 procedure byte

SIMn +0070h SIM ATR State Register **SIMIFN_SIM_ATRSTA**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								**AL**	**IR**							**OFF**
Type								R	R							R
Reset								0h	0h							1h

The SIM card is initially turned off. After configuring SIMON of SIMn_SIM_CTRL and ATR procedure, SIMn_SIM_ATRSTA will set IR or AL to 1 to indicate the card's feature.

OFF Indicates On/Off of the SIM card
IR SIM card is IR (internal reset) card
AL SIM card is AL (active low reset) card

SIMn +0074h SIM Protocol State Register **SIMIFN_SIM_STATUS**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**ALL**	**ONE**				**IDLE**
Type											R	R				R
Reset											0h	0h				1h

T0 or T1 protocol of the SIM card is initially turned off. When T0 or T1 protocol is turned on, SIMn_SIM_T0STA will transit between ONE or ALL according to the procedure byte of the SIM card.

IDLE SIM card's T0 or T1 protocol is active or idle.
ONE SIM card will send the next byte
ALL SIM card will send all the remaining bytes.

SIMn +0080h Data Register Used As Tx/Rx Data Register **SIMIFN_SIM_DMADATA**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									**DATA[7:0]**							
Type									R/W							
Reset									-							

DATA Eight data digits, corresponding to the character being read or written

SIMn +0090h SIM Module Debug Register **SIMIFN_SIM_DBG**

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name					DBG7	DBG6	DBG5	DBG4				DBG3[4:0]				
Type					R	R	R	R				R				
Reset					0h	0h	0h	0h				0h				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				DBG2[4:0]								DBG1[4:0]				
Type				R								R				
Reset				0h								0h				

DBG1 Debugging register 1
DBG2 Debugging register 2
DBG3 Debugging register 3
DBG4 Debugging register 4
DBG5 Debugging register 5
DBG6 Debugging register 6
DBG7 Debugging register 7

SIMn +0094h SIM FIFO Data Debug Register **SIMIFN_SIM_DBGDATA**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					DBGRPTR[3:0]				DBGDATA[7:0]							
Type					R				R							
Reset					0h				-							

DBGDATA FIFO data debugging register
There is no impact on data transmission when this register is read.
DBGRPTR FIFO read pointer related to DBGDATA
Automatically increases by 1 after this register is read.

SIMn +00A0h SIM SCLK PAD Control Register **SIMIFN_SIM_SCLK**

bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															DEBUG	ACD_FUNC
Type															R/W	R/W
Reset															0h	0h
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IES_CTRL	IES_LV			TDSEL[1:0]		RDSEL[1:0]		R1	R0	PUPD	SMT	E4	E2	SR[1:0]	
Type	R/W	R/W			R/W		R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0h	0h			0h		0h		0h	0h	0h	1h	0h	1h	3h	

SR Output slew rate control
High asserted. SR = 1, slower slew. SR = 0, no slew rate control.
For SIM card mode, SR[1:0] = [1 1] is the recommended setting to eliminate overshooting/undershooting. For non-SIM card mode, SR[1:0] = [0 0] is set for best speed.
E2 TX driving strength control
For SIM card mode, E2 = [1] is the recommended setting for SCLK/SRST/SIO. (SIO/SRST can use [0])

E4 TX driving strength control
For SIM card mode, E4 = [0] is the recommended setting for SCLK/SRST/SIO.

SMT RX input buffer schmit trigger hysteresis control enable
High asserted. SMT = 1, schmit trigger enable.
For SIM card mode, SMT = [1] is the recommended setting.

PUPD Weak pull-up/pull-down control
- **0** Pull-up
- **1** Pull-down

R0 Weak pull-up/pull-down resistance select
Check the table in register "R1".

R1 Weak pull-up/pull-down resistance select
Check the following table.

E	PUPD	R1	R0	R Value
0	0	0	0	High – Z
0	0	0	1	PU – 20k
0	0	1	0	PU – 5k
0	0	1	1	PU – 4k
0	1	0	0	High – Z
0	1	0	1	PD – 75k
0	1	1	0	PD – 75k
0	1	1	1	PD – 37.5k
1	x	x	x	High - Z

RDSEL Selects RX duty
RDSEL[0]: Input buffer duty high when asserted. (high pulse width adjustment)
RDSEL[1]: Input buffer duty low when asserted. (low pulse width adjustment)
For SIM card mode, RDSEL = [0 0] is the recommended setting.

TDSEL Selects TX duty
TDSEL[0]: Output level shifter duty high when asserted. (high pulse width adjustment)
TDSEL[1]: Output level shifter duty low when asserted. (low pulse width adjustment)
For SIM card mode, TDSEL = [0 0] is the recommended setting.

IES_LV Controls IES (RX input buffer enable) parking level in IES direct control mode
High asserted. Datapath: From IO to O. IES = 0, O = 0.
In quiescent mode, IES = 0 is suggested for power saving.

IES_CTRL Enables IES direct control mode

ACD_FUNC ACD function mode for analog designer

DEBUG Output PAD related signals for monitoring
- **0** Disable
- **1** Enable

SIMn +00A4h SIM SRST PAD Control Register **SIMIFN_SIM_SRST**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IES_CTRL	IES_LV			TDSEL[1:0]		RDSEL[1:0]		R1	R0	PUPD	SMT	E4	E2	SR[1:0]	
Type	R/W	R/W			R/W		R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0h	0h			0h		0h		0h	0h	0h	1h	0h	1h	3h	

SR Output slew rate control
High asserted. SR = 1, slower slew. SR = 0, no slew rate control.
For SIM card mode, SR[1:0] = [1 1] is the recommended setting to eliminate overshooting/undershooting. For non-SIM card mode, SR[1:0] = [0 0] is set for best speed.

E2 TX driving strength control
For SIM card mode, E2 = [1] is the recommended setting for SCLK/SRST/SIO. (SIO/SRST can use [0])

E4 TX driving strength control
For SIM card mode, E4 = [0] is the recommended setting for SCLK/SRST/SIO.

SMT RX input buffer schmit trigger hysteresis control enable
High asserted. SMT = 1, schmit trigger enable.
For SIM card mode, SMT = [1] is the recommended setting.

PUPD Weak pull-up/pull-down control
0 Pull-up
1 Pull-down

R0 Weak pull-up/pull-down resistance select
Check the table in register “R1”.

R1 Weak pull-up/pull-down resistance select
Check the following table.

E	PUPD	R1	R0	R Value
0	0	0	0	High – Z
0	0	0	1	PU – 20k
0	0	1	0	PU – 5k
0	0	1	1	PU – 4k
0	1	0	0	High – Z
0	1	0	1	PD – 75k
0	1	1	0	PD – 75k
0	1	1	1	PD – 37.5k
1	x	x	x	High - Z

RDSEL Selects RX duty
RDSEL[0]: Input buffer duty high when asserted. (high pulse width adjustment)
RDSEL[1]: Input buffer duty low when asserted. (low pulse width adjustment)
For SIM card mode, RDSEL = [0 0] is the recommended setting.

TDSEL Selects TX duty
TDSEL[0]: Output level shifter duty high when asserted. (high pulse width adjustment)
TDSEL[1]: Output level shifter duty low when asserted. (low pulse width adjustment)

For SIM card mode, TDSEL = [0 0] is the recommended setting.

IES_LV Controls IES (RX input buffer enable) parking level in IES direct control mode
High asserted. Datapath: From IO to O. IES = 0, O = 0.
In quiescent mode, IES = 0 is suggested for power saving.

IES_CTRL Enables IES direct control mode

SIMn +00A8h SIM SIO PAD Control Register **SIMIFN_SIM_SIO**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IES_CTRL	IES_LV			TDSEL[1:0]		RDSEL[1:0]		R1	R0	PUPD	SMT	E4	E2	SR[1:0]	
Type	R/W	R/W			R/W		R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0h	0h			0h		0h		1h	0h	0h	1h	0h	1h	3h	

SR Output slew rate control
High asserted. SR = 1, slower slew. SR = 0, no slew rate control.
For SIM card mode, SR[1:0] = [1 1] is the recommended setting to eliminate overshooting/undershooting. For non-SIM card mode, SR[1:0] = [0 0] is set for best speed.

E2 TX driving strength control
For SIM card mode, E2 = [1] is the recommended setting for SCLK/SRST/SIO. (SIO/SRST can use [0])

E4 TX driving strength control
For SIM card mode, E4 = [0] is the recommended setting for SCLK/SRST/SIO.

SMT RX input buffer schmit trigger hysteresis control enable
High asserted. SMT = 1, schmit trigger enable.
For SIM card mode, SMT = [1] is the recommended setting.

PUPD Weak pull-up/pull-down control
0 Pull-up
1 Pull-down

R0 Weak pull-up/pull-down resistance select
Check the table in register "R1".

R1 Weak pull-up/pull-down resistance select
Check the following table.
For SIO, [R1 R0] = [1 0] is the recommended setting for 5k weak pull-up. In 4 SIM application and SIO is connected to external SIM switch, please disable pull-up resistance. ([R1 R0] = [0 0])

E	PUPD	R1	R0	R Value
0	0	0	0	High – Z
0	0	0	1	PU – 20k
0	0	1	0	PU – 5k
0	0	1	1	PU – 4k
0	1	0	0	High – Z
0	1	0	1	PD – 75k
0	1	1	0	PD – 75k

E	PUPD	R1	R0	R Value
0	1	1	1	PD – 37.5k
1	x	x	x	High - Z

RDSEL Selects RX duty
RDSEL[0]: Input buffer duty high when asserted. (high pulse width adjustment)
RDSEL[1]: Input buffer duty low when asserted. (low pulse width adjustment)
For SIM card mode, RDSEL = [0 0] is the recommended setting.

TDSEL Selects TX duty
TDSEL[0]: Output level shifter duty high when asserted. (high pulse width adjustment)
TDSEL[1]: Output level shifter duty low when asserted. (low pulse width adjustment)
For SIM card mode, TDSEL = [0 0] is the recommended setting.

IES_LV Controlling IES (RX input buffer enable) parking level in IES direct control mode
High asserted. Datapath: From IO to O. IES = 0, O = 0.
In quiescent mode, IES = 0 is suggested for power saving.

IES_CTRL Enables IES direct control mode

SIMn +00ACh SIM Monitor Register **SIMIFN_SIM_MON**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		MON12	MON11	MON10		MON9	MON8	MON7		MON6	MON5	MON4		MON3	MON2	MON1
Type		R	R	R		R	R	R		R	R	R		R	R	R
Reset		0h	0h	0h		0h	0h	0h		0h	0h	0h		0h	0h	0h

MON1 Monitor signal 1
MON2 Monitor signal 2
MON3 Monitor signal 3
MON4 Monitor signal 4
MON5 Monitor signal 5
MON6 Monitor signal 6
MON7 Monitor signal 7
MON8 Monitor signal 8
MON9 Monitor signal 9
MON10 Monitor signal 10
MON11 Monitor signal 11
MON12 Monitor signal 12

SIMn+00B0h SIM Test Select **SIMIFN_SIM_SEL**

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														SIMSEL		
Type														R/W		
Reset														3'b001		

SIMSEL **Selects** monitor SIMRST, SIMCLK, SIMIO input signal
001 SIMRST input is monitored.
010 SIMCLK input is monitored.
100 SIMSIO input is monitored.
Others No meaning

3.2.2 SIM Card Insertion and Removal

The detection of physical connection to the SIM card and card removal can be done by the external interrupt controller or by GPIO.

3.2.3 Card activation and Deactivation

The card activation and deactivation sequence are both controlled by H/W. The MCU initiates the activation sequence by writing “1” to bit 0 of the SIM_CTRL register, and then the interface performs the following activation sequence:

- Assert SIMRST ”low”
- Set SIMVCC at “high” level and SIMDATA in the reception mode
- Enable SIMCLK clock
- De-assert SIMRST “high” (required if it belongs to active low reset SIM card)

The final step in a typical card session is contacting deactivation in case the card will be electrically damaged. The deactivation sequence is initiated by writing “0” to bit 0 of the SIM_CTRL register, and the interface will perform the following deactivation sequence:

- Assert SIMRST ”low”
- Set SCIMCLK at “low” level
- Set SIMDATA at “low” level
- Set SIMVCC at “low” level

3.2.4 Answering to Reset Sequence

After the card is activated, a reset operation will result in an answer from the card consisting of the initial character TS, followed by maximum 32 characters. The initial character TS provides a bit synchronization sequence and defines the conventions to interpret data bytes in all subsequent characters.

On reception of the first character, TS, the MCU should read this character, establish the respective required convention and re-program the related registers. These processes should be completed prior to the completion of reception of the next character. Next, the remainder of the ATR sequence will be received, read via the SIM_DATA in the selected convention and interpreted by the S/W.

The timing requirement and procedures for ATR sequence are handled by H/W and shall meet the requirement of ISO 7816-3, as shown in Figure 23.

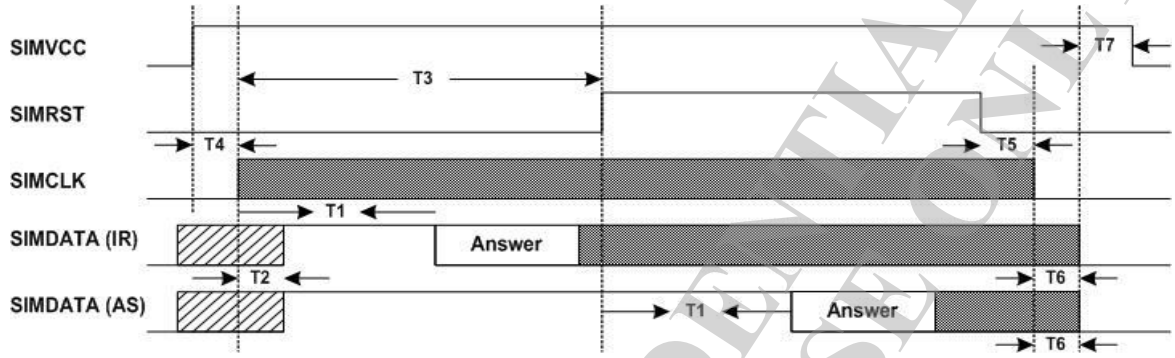


Figure 23. Answering to reset sequence

Table 43.** Time-out condition for **answering to reset sequence

Time	Value	Comment
T1	> 400 SIMCLK	SIMCLK start to ATR appears
T2	< 200 SIMCLK	SIMCLK start to SIMDATA in reception mode
T3	> 40,000 SIMCLK	SIMCLK start to SIMRST "high"
T4	-	SIMVCC "high" to SIMCLK start
T5	-	SIMRST "low" to SIMCLK stop
T6	-	SIMCLK stop to SIMDATA "low"
T7	-	SIMDATA "low" to SIMVCC "low"

3.2.5 SIM Data Transfer

There are two transfer modes provided, in software controlled byte by byte fashion or in a block fashion using T=0 controller and DMA controller. In both modes, the time-out counter can be enabled to monitor the elapsed time between two consecutive bytes.

3.2.5.1 Byte Transfer Mode

This mode is used during ATR and PPS procedure. In this mode, the SIM interface only ensures error free character transmission and reception.

Receiving characters

Upon detection of the start-bit sent by SIM card, the interface transforms into reception mode and the following bits are shifted into an internal register. If no parity error is detected or the character-received handshaking is disabled, the received-character will be written into the SIM FIFO and the SIM_COUNT register increased by one. Otherwise, the SIMDATA line will be held "low" at 0.5 etu after detecting the parity error for 1.5 etus, and the character will be re-received. If a character fails to be

received correctly for the RXRETRY times, the receive-handshaking will be aborted, the last-received character written into the SIM FIFO, the SIM_COUNT increased by one and the RXERR interrupt generated.

When the number of characters held in the received FIFO exceeds the level defined in the SIM_TIDE register, a RXTIDE interrupt will be generated. The number of characters held in the SIM FIFO can be determined by reading the SIM_COUNT register, and writing to this register will flush the SIM FIFO.

Sending characters

Characters that are to be sent to the card are first written into the SIM FIFO and then automatically transmitted to the card at timed intervals. If character-transmitted handshaking is enabled, the SIMDATA line will be sampled at 1 etu after the parity bit. If the card indicates that it does not receive the character correctly, the character will be re-transmitted for maximum of TXRETRY times before a TXERR interrupt is generated and the transmission is aborted. Otherwise, the succeeding byte in the SIM FIFO will be transmitted.

If a character fails to be transmitted and a TXERR interrupt is generated, the interface will need to be reset by flushing the SIM FIFO before any subsequent transmission or reception operation.

When the number of characters held in the SIM FIFO falls below the level defined in the SIM_TIDE register, a TXTIDE interrupt will be generated. The number of characters held in the SIM FIFO can be determined by reading the SIM_COUNT register, and writing to this register will flush the SIM FIFO.

3.2.5.2 Block Transfer Mode

Basically the SIM interface is designed to work in conjunction with the T=0 protocol controller and the DMA controller during non-ATR and non-PPS phase, though it is still possible for software to service the data transfer manually as in the byte transfer mode if necessary. Thus the T=0 protocol should be controlled by software.

The T=0 controller can be accessed via four registers representing the instruction header bytes INS and P3, and the procedure bytes SW1 and SW2. The registers are:

- SIM_INS, SIM_P3
- SIM_SW1, SIM_SW2

During the character transfer, SIM_P3 holds the number of characters to be sent or to be received, and SIM_SW1 holds the last received procedure byte including NULL, ACK, NACK and SW1 for debugging.

Data receiving instruction

Data receiving instructions receive data from the SIM card. See the following instantiated procedure.

1. Enable the T=0 protocol controller by setting the T0EN bit to 1 in the SIM_CONF register.
2. Program the SIM_TIDE register to 0x0000 (TXTIDE = 0, RXTIDE = 0).
3. Program the SIM_IRQEN to 0x019C (enable RXERR, TXERR, T0END, TOUT and OVRUN interrupts).
4. Write CLA, INS, P1, P2 and P3 into SIM FIFO.
5. Program the DMA controller:
   - DMA*n*_MSBSRC and DMA*n*_LSBSRC: Address of the SIM_DATA register
   - DMA*n*_MSBDST and DMA*n*_LSBDST: Memory address reserved to store the received characters
   - DMA*n*_COUNT: Identical to P3 or 256 (if P3 = 0)
   - DMA*n*_CON: 0x0078
6. Write P3 into the SIM_P3 register and then INS into SIM_INS register. (Data transfer is initiated now.)
7. Enable the time-out counter by setting the TOUT bit to 1 in the SIM_CONF register.
8. Start the DMA controller by writing 0x8000 into the DMA*n*_START register.

Upon completion of the data receiving instruction, T0END interrupt will be generated and the time-out counter should be disabled by setting the TOUT bit to 0 in the SIM_CONF register.

If error occurs during the data transfer (RXERR, TXERR, OVRUN or TOUT interrupt is generated), the SIM card should be deactivated first and then activate the prior subsequent operations.

Data sending instruction

Data sending instructions send data to the SIM card. See the following instantiated procedure.

1. Enable the T=0 protocol controller by setting the T0EN bit to 1 in the SIM_CONF register.
2. Program the SIM_TIDE register to 0x0100 (TXTIDE = 1, RXTIDE = 0)
3. Program the SIM_IRQEN to 0x019C (enable RXERR, TXERR, T0END, TOUT and OVRUN interrupts)
4. Write CLA, INS, P1, P2 and P3 into SIM FIFO
5. Program the DMA controller:
   - DMA*n*_MSBSRC and DMA*n*_LSBSRC: Memory address reserved to store the transmitted characters
   - DMA*n*_MSBDST and DMA*n*_LSBDST: Address of the SIM_DATA register
   - DMA*n*_COUNT: Identical to P3
   - DMA*n*_CON: 0x0074
6. Write P3 into the SIM_P3 register and then (0x0100 | INS) into SIM_INS register. (Data transfer is initiated now.)
7. Enable the time-out counter by setting the TOUT bit to 1 in the SIM_CONF register.
8. Start the DMA controller by writing 0x8000 into the DMA*n*_START register.

Upon completion of the data sending instruction, T0END interrupt will be generated and the time-out counter should be disabled by setting the TOUT bit back to 0 in the SIM_CONF register.

If error occurs during the data transfer (RXERR, TXERR, OVRUN or TOUT interrupt is generated), the SIM card should be deactivated first and then activate the prior subsequent operations.

3.3 Keypad Scanner

3.3.1 General Description

The keypad supports two types of keypads: 5*5 double keypad and 5*5 triple keypad.

The 5*5 keypad can be divided into two parts: 1) The keypad interface including 5 columns and 5 rows (see Figure 24 and Figure 25); 2) The key detection block providing key pressed, key released and de-bounce mechanisms.

Each time the key is pressed or released, i.e. something different in the 5*5 matrix, the key detection block senses the change and recognizes if a key has been pressed or released. Whenever the key status changes and is stable, a KEYPAD IRQ will be issued. The MCU can then read the key(s) pressed directly in the KP_MEM1, KP_MEM2, KP_MEM3, KP_MEM4 and KP_MEM5 registers. To ensure the key pressed information is not missed, the status register in keypad is not read-cleared by the APB read command. The status register can only be changed by the key-pressed detection FSM.

This keypad can detect one or two keys pressed simultaneously. Figure 27 shows the one key pressed condition. Figure 28(a) and Figure 28(b) illustrate the two keys pressed cases. Since the key pressed detection depends on the HIGH or LOW level of the external keypad interface, if the keys are pressed at the same time and there exists a key that is on the same column and the same row with other keys, the pressed key cannot be correctly decoded. For example, if there are three key pressed: key1 = (x1, y1), key2 = (x2, y2), and key3 = (x1, y2), then both key3 and key4 = (x2, y1) will be detected, and therefore they cannot be distinguished correctly. Hence, the keypad can detect only one or two keys pressed simultaneously at any combination. More than two keys pressed simultaneously in a specific pattern will retrieve the wrong information.

The 5*5 double keypad (Figure 24) supports a 5*5*2 = 50 keys matrix. The 50 keys are divided into 25 sub groups and each group consists of 2 keys and a off-chip resistor. 5*5 double keypad has another limitation, which is it cannot detect two keys pressed simultaneously when the two keys are in one group, i.e. the 5*5 keypad cannot detect key0 and key1 pressed simultaneously or key15 and key16 pressed simultaneously.

The 5*5 triple keypad (Figure 25) supports a 5*5*3 = 75 keys matrix. The 75 keys are divided into 25 sub groups and each group consists of 3 keys and two off-chip resistors. 5*5 triple keypad has another limitation, which is it cannot detect three keys pressed simultaneously when the three keys are in one group, i.e. 5*5 keypad cannot detect key0, key1 and key2 pressed simultaneously or key15, key16 and key17 pressed simultaneously.

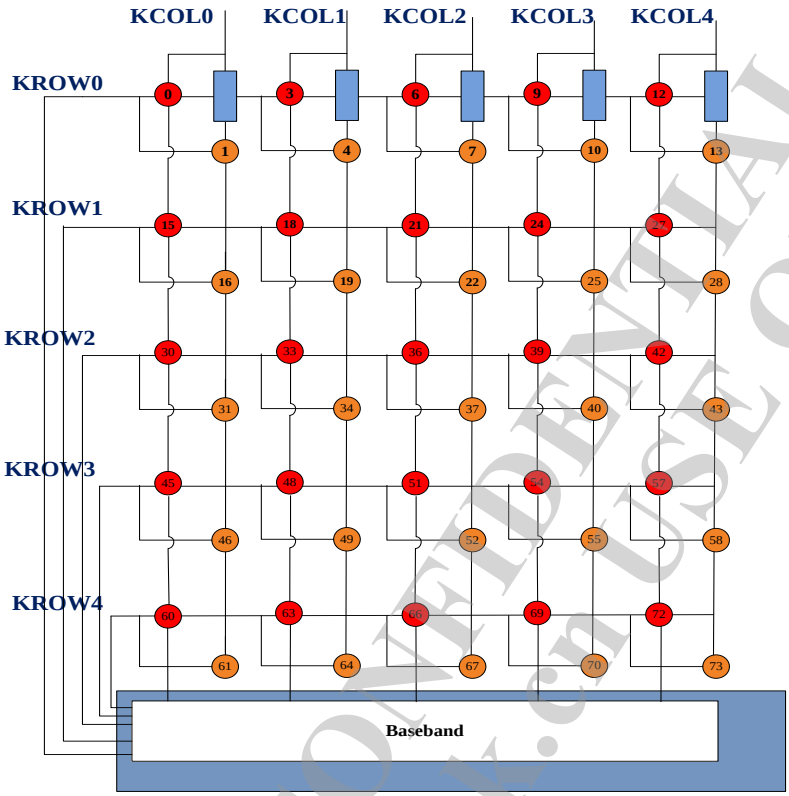


Figure 24. 5x5 double keypad matrix (50 keys)

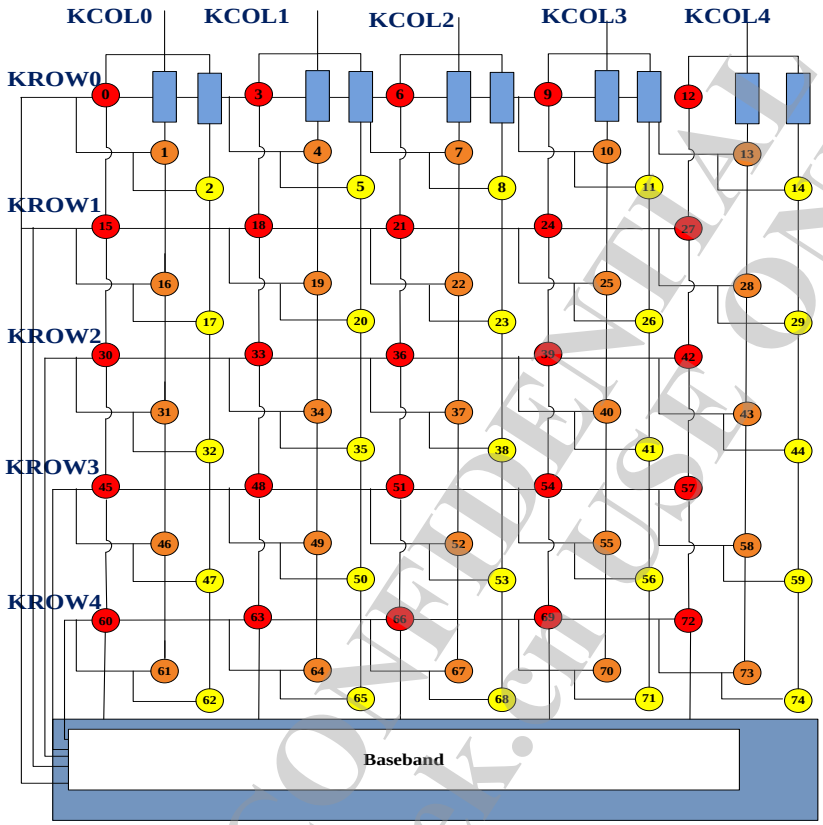


Figure 25. 5x5 triple keypad matrix (75 keys)

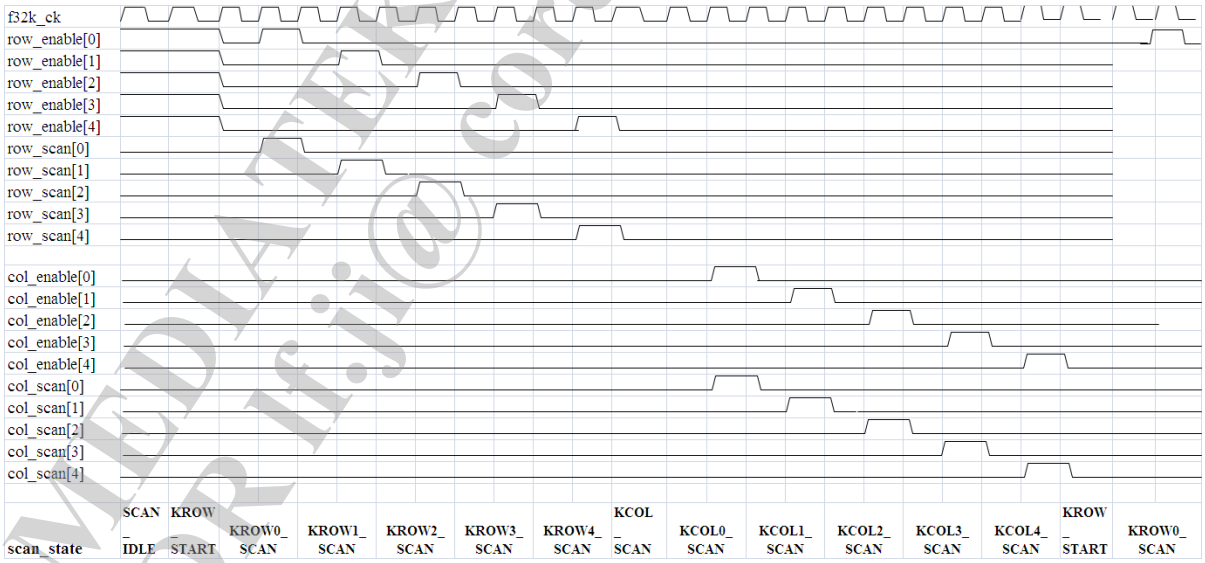


*Figure 26. 5*5 double keypad scan waveform*

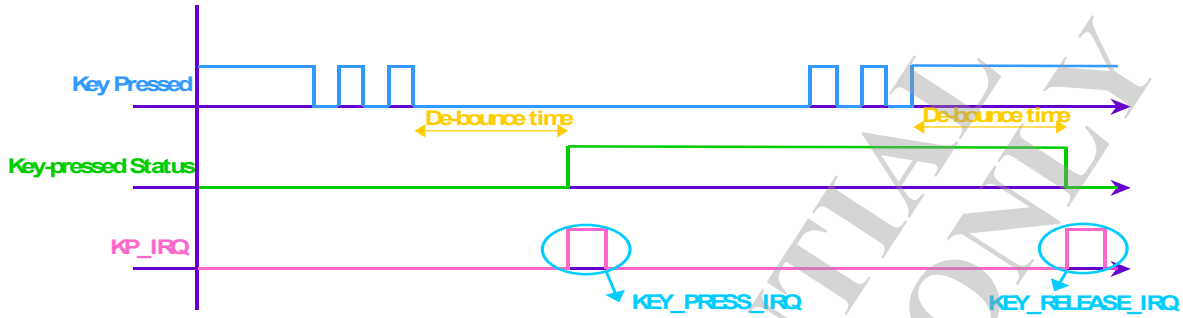


Figure 27. One key pressed with de-bounce mechanism denoted

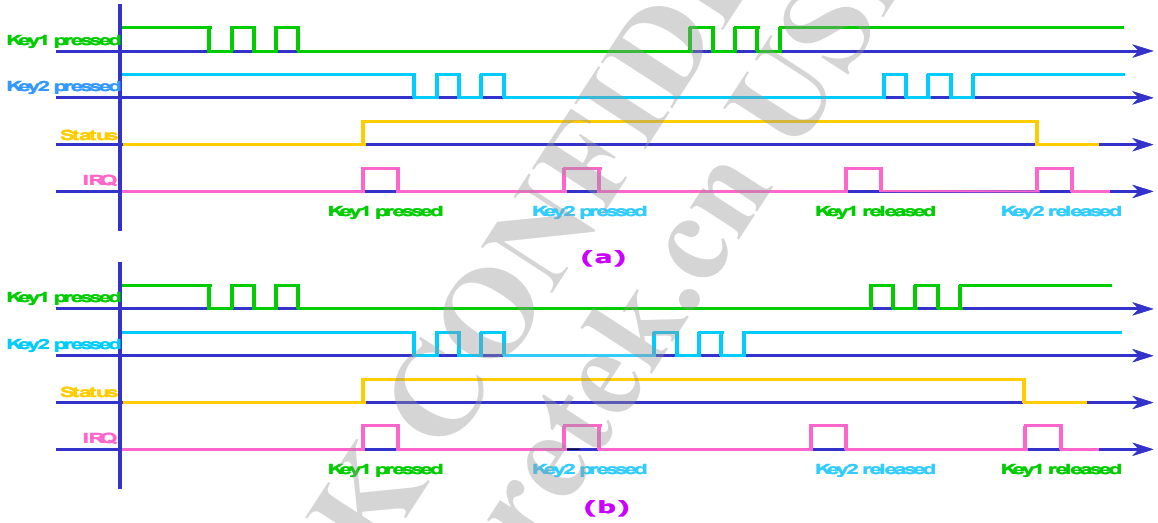


Figure 28. (a) Two keys pressed, case 1; (b) Two keys pressed, case 2

3.3.2 Register Definitions

Module name: KP Base address: (+A00D0000)

Address	Name	Width	Register Function
A00D0000	KP_STA	16	**Keypad Status**
A00D0004	KP_MEM1	16	**Keypad Scanning Output Register** Shows the key-pressed status of key 0 (LSB) ~ key 15. Refer to Table 1 and Table 2.
A00D0008	KP_MEM2	16	**Keypad Scanning Output Register** Shows the key-pressed status of key 16 (LSB) ~ key 31. Refer to Table 1 and Table 2.
A00D000C	KP_MEM3	16	**Keypad Scanning Output Register** Shows the key-pressed status of key 32 (LSB) ~ key 47. Refer to Table 1 and Table 2.
A00D0010	KP_MEM4	16	**Keypad Scanning Output Register** Shows the key-pressed status of key 48 (LSB) ~ key 63. Refer to Table 1 and Table 2.

Address	Name	Width	Register Function
A00D0014	KP_MEM5	16	**Keypad Scanning Output Register** Shows the key-pressed status of key 64 (LSB) ~ key 77. Refer to Table 1 and Table 2.
A00D0018	KP_DEBOUNCE	16	**De-bounce Period Setting** Defines the waiting period before key pressing or release events are considered stable. If the de-bounce setting is too small, the keypad will be too sensitive and detect too many unexpected key presses. The suitable de-bounce time setting must be adjusted according to the user's habit.
A00D001C	KP_SCAN_TIMING	16	**Keypad Scan Timing Adjustment Register** Sets up the keypad scan timing. *Note: ROW_SCAN_DIV > ROW_INTERVAL_DIV and COL_SCAN_DIV > COL_INTERVAL_DIV. ROW_INTERVAL_DIV/COL_INTERVAL_DIV are used to lower the power consumption for it decreases the actual scan number during the de-bounce time.*
A00D0020	KP_SEL	16	**Keypad Selection Register** Selects: 1: Use the double keypad or triple keypad 2: Which cols and rows are used
A00D0024	KP_EN	16	**Keypad Enable Register** Enables/Disables keypad.

A00D0000 KP_STA Keypad Status 0000

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																STA
Type																RO
Reset																0

Bit(s)	Mnemonic	Name	Description
0	**STA**	STA	**Indicates the keypad status** The register is not cleared by the read operation. 0: No key pressed 1: Key pressed

A00D0004 KP_MEM1 Keypad Scanning Output Register FFFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY15	KEY14	KEY13	KEY12	KEY11	KEY10	KEY9	KEY8	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Overview: Shows the key-pressed status of key 0 (LSB) ~ key 15. Refer to Table 1 and Table 2.

Bit(s)	Mnemonic	Name	Description
15	**KEY15**	KEY15	
14	**KEY14**	KEY14	

Bit(s)	Mnemonic	Name	Description
13	**KEY13**	KEY13	
12	**KEY12**	KEY12	
11	**KEY11**	KEY11	
10	**KEY10**	KEY10	
9	**KEY9**	KEY9	
8	**KEY8**	KEY8	
7	**KEY7**	KEY7	
6	**KEY6**	KEY6	
5	**KEY5**	KEY5	
4	**KEY4**	KEY4	
3	**KEY3**	KEY3	
2	**KEY2**	KEY2	
1	**KEY1**	KEY1	
0	**KEY0**	KEY0	

A00D0008 KP_MEM2 Keypad Scanning Output Register FFFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY31	KEY30	KEY29	KEY28	KEY27	KEY26	KEY25	KEY24	KEY23	KEY22	KEY21	KEY20	KEY19	KEY18	KEY17	KEY16
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Overview: Shows the key-pressed status of key 16 (LSB) ~ key 31. Refer to Table 1 and Table 2.

Bit(s)	Mnemonic	Name	Description
15	**KEY31**	KEY31	
14	**KEY30**	KEY30	
13	**KEY29**	KEY29	
12	**KEY28**	KEY28	
11	**KEY27**	KEY27	
10	**KEY26**	KEY26	
9	**KEY25**	KEY25	
8	**KEY24**	KEY24	
7	**KEY23**	KEY23	
6	**KEY22**	KEY22	
5	**KEY21**	KEY21	
4	**KEY20**	KEY20	
3	**KEY19**	KEY19	
2	**KEY18**	KEY18	
1	**KEY17**	KEY17	
0	**KEY16**	KEY16	

A00D000C KP_MEM3 Keypad Scanning Output Register FFFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY47	KEY46	KEY45	KEY44	KEY43	KEY42	KEY41	KEY40	KEY39	KEY38	KEY37	KEY36	KEY35	KEY34	KEY33	KEY32
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Overview: Shows the key-pressed status of key 32 (LSB) ~ key 47. Refer to Table 1 and Table 2.

Bit(s)	Mnemonic	Name	Description
15	**KEY47**	KEY47	
14	**KEY46**	KEY46	
13	**KEY45**	KEY45	
12	**KEY44**	KEY44	
11	**KEY43**	KEY43	
10	**KEY42**	KEY42	
9	**KEY41**	KEY41	
8	**KEY40**	KEY40	
7	**KEY39**	KEY39	
6	**KEY38**	KEY38	
5	**KEY37**	KEY37	
4	**KEY36**	KEY36	
3	**KEY35**	KEY35	
2	**KEY34**	KEY34	
1	**KEY33**	KEY33	
0	**KEY32**	KEY32	

A00D0010 KP_MEM4 Keypad Scanning Output Register FFFF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KEY63	KEY62	KEY61	KEY60	KEY59	KEY58	KEY57	KEY56	KEY55	KEY54	KEY53	KEY52	KEY51	KEY50	KEY49	KEY48
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Overview: Shows the key-pressed status of key 48 (LSB) ~ key 63. Refer to Table 1 and Table 2.

Bit(s)	Mnemonic	Name	Description
15	**KEY63**	KEY63	
14	**KEY62**	KEY62	
13	**KEY61**	KEY61	
12	**KEY60**	KEY60	
11	**KEY59**	KEY59	
10	**KEY58**	KEY58	
9	**KEY57**	KEY57	
8	**KEY56**	KEY56	
7	**KEY55**	KEY55	

Bit(s)	Mnemonic	Name	Description
6	**KEY54**	KEY54	
5	**KEY53**	KEY53	
4	**KEY52**	KEY52	
3	**KEY51**	KEY51	
2	**KEY50**	KEY50	
1	**KEY49**	KEY49	
0	**KEY48**	KEY48	

A00D0014 KP_MEM5 Keypad Scanning Output Register 07FF

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						KEY74	KEY73	KEY72	KEY71	KEY70	KEY69	KEY68	KEY67	KEY66	KEY65	KEY64
Type						RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset						1	1	1	1	1	1	1	1	1	1	1

Overview: Shows the key-pressed status of key 64 (LSB) ~ key 77. Refer to Table 1 and Table 2.

Bit(s)	Mnemonic	Name	Description
10	**KEY74**	KEY74	
9	**KEY73**	KEY73	
8	**KEY72**	KEY72	
7	**KEY71**	KEY71	
6	**KEY70**	KEY70	
5	**KEY69**	KEY69	
4	**KEY68**	KEY68	
3	**KEY67**	KEY67	
2	**KEY66**	KEY66	
1	**KEY65**	KEY65	
0	**KEY64**	KEY64	

The five registers list the status of 75 keys on the keypad. For 5*5 keypad, KP_MEM1~4 registers list the status of 75 keys on the keypad. When the MCU receives KEYPAD IRQ, both two registers must be read. If any key is pressed, the relative bit will be set to 0.

In order to work normally, the corresponding pull-up/down setting must be programmed correctly. If some keys can be used because their COL or ROW is used as GPIO, these corresponding enabling bit should be set.

KEYS Status list of the 75 keys.

A00D0018 KP_DEBOUNCE De-bounce Period Setting 0400

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name			DEBOUNCE													
Type			RW													
Reset			0	0	0	1	0	0	0	0	0	0	0	0	0	0

Overview: Defines the waiting period before key pressing or release events are considered stable. If the de-bounce setting is too small, the keypad will be too sensitive and detect too many unexpected key presses. The suitable de-bounce time setting must be adjusted according to the user's habit.

Bit(s)	Mnemonic	Name	Description
13:0	**DEBOUNCE**	DEBOUNCE	De-bounce time = KP_DEBOUNCE/32ms.

A00D001C KP_SCAN_TIMING Keypad Scan Timing Adjustment Register 0011

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COL_INTERVAL_DIV				ROW_INTERVAL_DIV				COL_SCAN_DIV				ROW_SCAN_DIV			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1

Overview: Sets up the keypad scan timing. Note: ROW_SCAN_DIV > ROW_INTERVAL_DIV and COL_SCAN_DIV > COL_INTERVAL_DIV. ROW_INTERVAL_DIV/COL_INTERVAL_DIV are used to lower the power consumption for it decreases the actual scan number during the de-bounce time.

Bit(s)	Mnemonic	Name	Description
15:12	**COL_INTERVAL_DIV**	COL_INTERVAL_DIV	**Sets up the COL SCAN interval cycle, i.e. cycles between two scans** Default 0 means there is 1 cycle between two high scan pulses.
11:8	**ROW_INTERVAL_DIV**	ROW_INTERVAL_DIV	**Sets up the ROW SCAN interval cycle, i.e. cycles between two scans** Default 0 means there is 1 cycle between two high scan pulses.
7:4	**COL_SCAN_DIV**	COL_SCAN_DIV	**Sets up the COL SCAN cycle which includes COL_INTERVAL_DIV and the high pulse period** Default 1 means there are 2 cycles for each scan, including 1 cycle high pulse and 1 cycle interval.
3:0	**ROW_SCAN_DIV**	ROW_SCAN_DIV	**Sets up the ROW SCAN cycle which includes ROW_INTERVAL_DIV and the high pulse period** Default 1 means there are 2 cycles for each scan, including 1 cycle high pulse and 1 cycle interval.

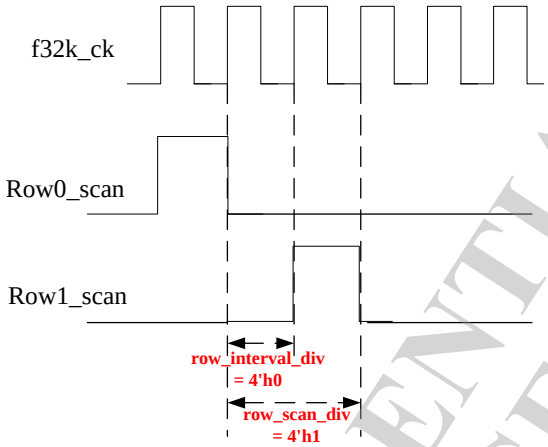


Figure 29. kp timing register

A00D0020 KP_SEL Keypad Selection Register FFC0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	KP1_COL_SEL										SAMPLE_DELAY					KP_SEL
Type	RW										RW					RW
Reset	1	1	1	1	1						0	0	0	0	0	0

Overview: Selects 1: Use the double keypad or triple keypad; 2: Which cols and rows are used.

Bit(s)	Mnemonic	Name	Description
15:11	KP1_COL_SEL	KP1_COL_SEL	**Selects to use which col** 0: Disable corresponding column 1: Enable corresponding column
5:1	SAMPLE_DELAY	SAMPLE_DELAY	**Sets up delay cycles to sample col** 0: No delay n: n*31.25ns delay to sample col
0	KP_SEL	KP_SEL	**Selects to use double keypad or triple keypad** 0: Use triple keypad 1: Use double keypad

A00D0024 KP_EN Keypad Enable Register 0001

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																KP_EN
Type																RW
Reset																1

Overview: Enables/Disables keypad.

Bit(s)	Mnemonic	Name	Description
0	KP_EN	KP_EN	0: Disable keypad (Both double and triple keypads will not work.)

Bit(s)	Mnemonic	Name	Description
			1: Enable keypad (Only either of double or triple keypads can work.)

*Table 44. 5*5 double KEY's order number in COL/ROW matrix*

	COL0	COL1	COL2	COL3	COL4
ROW4	60/61	63/64	66/67	69/70	72/73
ROW3	45/46	48/49	51/52	54/55	57/58
ROW2	30/31	33/34	36/37	39/40	42/43
ROW1	15/16	18/19	21/22	24/25	27/28
ROW0	0/1	3/4	6/7	9/10	12/13

*Table 45. 5*5 triple KEY's order number in COL/ROW matrix*

	COL0	COL1	COL2	COL3	COL4
ROW4	60/61/62	63/64/65	66/67/68	69/70/71	72/73/74
ROW3	45/46/47	48/49/50	51/52/53	54/55/56	57/58/59
ROW2	30/31/32	33/34/35	36/37/38	39/40/41	42/43/44
ROW1	15/16/17	18/19/20	21/22/23	24/25/26	27/28/29
ROW0	0/1/2	3/4/5	6/7/8	9/10/11	12/13/14

3.4 General Purpose Inputs/Outputs

3.4.1 General Description

MT2503A offers 56 general purpose I/O pins. By setting up the control registers, the MCU software can control the direction, the output value, and read the input values on these pins. These GPIOs and GPOs are multiplexed with other functions to reduce the pin count. In addition, all GPO pins are removed. To facilitate application use, the software can configure which clock to send outside the chip. There are 6 clock-out ports embedded in 56 GPIO pins, and each clock-out can be programmed to output appropriate clock source. Besides, when 2 GPIO function for the same peripheral IP, the smaller GPIO serial numbers have higher priority than larger numbers.

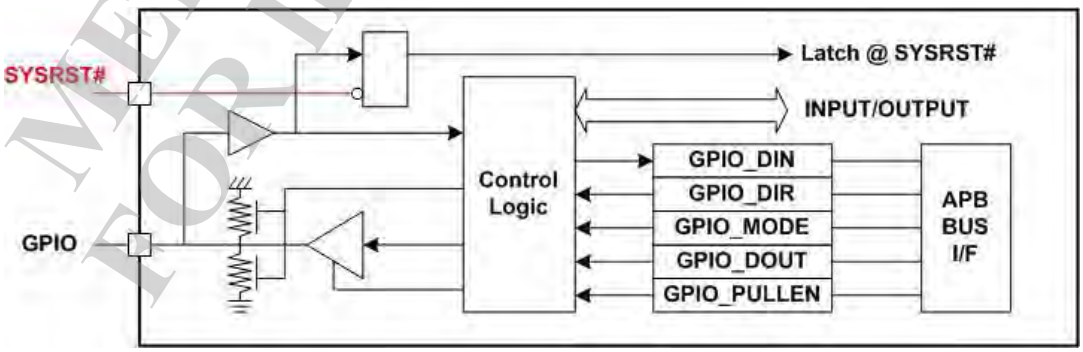


Figure 30. GPIO block diagram

3.4.2 Register Definitions

Module name: gpio_reg Base address: (+A0020000h)

Address	Name	Width	Register Function
A0020000	GPIO_DIR0	32	**GPIO Direction Control** Configures GPIO direction
A0020004	GPIO_DIR0_SET	32	**GPIO Direction Control** For bitwise access of GPIO_DIR0
A0020008	GPIO_DIR0_CLR	32	**GPIO Direction Control** For bitwise access of GPIO_DIR0
A0020010	GPIO_DIR1	32	**GPIO Direction Control** Configures GPIO direction
A0020014	GPIO_DIR1_SET	32	**GPIO Direction Control** For bitwise access of GPIO_DIR1
A0020018	GPIO_DIR1_CLR	32	**GPIO Direction Control** For bitwise access of GPIO_DIR1
A0020100	GPIO_PULLEN0	32	**GPIO Pull-up/down Enable Control** Configures GPIO pull enabling
A0020104	GPIO_PULLEN0_SET	32	**GPIO Pull-up/down Enable Control** For bitwise access of GPIO_PULLEN0
A0020108	GPIO_PULLEN0_CLR	32	**GPIO Pull-up/down Enable Control** For bitwise access of GPIO_PULLEN0
A0020110	GPIO_PULLEN1	32	**GPIO Pull-up/down Enable Control** Configures GPIO pull enabling
A0020114	GPIO_PULLEN1_SET	32	**GPIO Pull-up/down Enable Control** For bitwise access of GPIO_PULLEN1
A0020118	GPIO_PULLEN1_CLR	32	**GPIO Pull-up/down Enable Control** For bitwise access of GPIO_PULLEN1
A0020200	GPIO_DINV0	32	**GPIO Data Inversion Control** Configures GPIO inversion enabling
A0020204	GPIO_DINV0_SET	32	**GPIO Data Inversion Control** For bitwise access of GPIO_DINV0
A0020208	GPIO_DINV0_CLR	32	**GPIO Data Inversion Control** For bitwise access of GPIO_DINV0
A0020210	GPIO_DINV1	32	**GPIO Data Inversion Control** Configures GPIO inversion enabling
A0020214	GPIO_DINV1_SET	32	**GPIO Data Inversion Control** For bitwise access of GPIO_DINV1
A0020218	GPIO_DINV1_CLR	32	**GPIO Data Inversion Control** For bitwise access of GPIO_DINV1
A0020300	GPIO_DOUT0	32	**GPIO Output Data Control** Configures GPIO output value
A0020304	GPIO_DOUT0_SET	32	**GPIO Output Data Control** For bitwise access of GPIO_DIR0
A0020308	GPIO_DOUT0_CLR	32	**GPIO Output Data Control** For bitwise access of GPIO_DIR0
A0020310	GPIO_DOUT1	32	**GPIO Output Data Control** Configures GPIO output value

Address	Name	Width	Register Function
A0020314	GPIO_DOUT1_SET	32	**GPIO Output Data Control** For bitwise access of GPIO_DIR1
A0020318	GPIO_DOUT1_CLR	32	**GPIO Output Data Control** For bitwise access of GPIO_DIR1
A0020400	GPIO_DIN0	32	**GPIO Input Data Value** Reads GPIO input value
A0020410	GPIO_DIN1	32	**GPIO Input Data Value** Reads GPIO input value
A0020500	GPIO_PULLSEL0	32	**GPIO Pullsel Control** Configures GPIO PUPD selection
A0020504	GPIO_PULLSEL0_SET	32	**GPIO Pullsel Control** For bitwise access of GPIO_PULLSEL0
A0020508	GPIO_PULLSEL0_CLR	32	**GPIO Pullsel Control** For bitwise access of GPIO_PULLSEL0
A0020510	GPIO_PULLSEL1	32	**GPIO Pullsel Control** Configures GPIO PUPD selection
A0020514	GPIO_PULLSEL1_SET	32	**GPIO Pullsel Control** For bitwise access of GPIO_PULLSEL1
A0020518	GPIO_PULLSEL1_CLR	32	**GPIO Pullsel Control** For bitwise access of GPIO_PULLSEL1
A0020600	GPIO_SMT0	32	**GPIO SMT Control** Configures GPIO Schmit trigger control
A0020604	GPIO_SMT0_SET	32	**GPIO SMT Control** For bitwise access of GPIO_SMT0
A0020608	GPIO_SMT0_CLR	32	**GPIO SMT Control** For bitwise access of GPIO_SMT0
A0020610	GPIO_SMT1	32	**GPIO SMT Control** Configures GPIO Schmit trigger control
A0020614	GPIO_SMT1_SET	32	**GPIO SMT Control** For bitwise access of GPIO_SMT1
A0020618	GPIO_SMT1_CLR	32	**GPIO SMT Control** For bitwise access of GPIO_SMT1
A0020700	GPIO_SR0	32	**GPIO SR Control** Configures GPIO slew rate control
A0020704	GPIO_SR0_SET	32	**GPIO SR Control** For bitwise access of GPIO_SR0
A0020708	GPIO_SR0_CLR	32	**GPIO SR Control** For bitwise access of GPIO_SR0
A0020710	GPIO_SR1	32	**GPIO SR Control** Configures GPIO slew rate control
A0020714	GPIO_SR1_SET	32	**GPIO SR Control** For bitwise access of GPIO_SR1
A0020718	GPIO_SR1_CLR	32	**GPIO SR Control** For bitwise access of GPIO_SR1
A0020720	GPIO_SIM_SR	32	**GPIO SIM SR Control** Configures GPIO slew rate control for SIM IO
A0020724	GPIO_SIM_SR_SET	32	**GPIO SIM SR Control** For bitwise access of GPIO_SIM_SR
A0020728	GPIO_SIM_SR_CLR	32	**GPIO SIM SR Control** For bitwise access of GPIO_SIM_SR
A0020800	GPIO_DRV0	32	**GPIO DRV Control**

Address	Name	Width	Register Function
			Configures GPIO driving control
A0020804	GPIO_DRV0_SET	32	**GPIO DRV Control** For bitwise access of GPIO_DRV0
A0020808	GPIO_DRV0_CLR	32	**GPIO DRV Control** For bitwise access of GPIO_DRV0
A0020810	GPIO_DRV1	32	**GPIO DRV Control** Configures GPIO driving control
A0020814	GPIO_DRV1_SET	32	**GPIO DRV Control** For bitwise access of GPIO_DRV1
A0020818	GPIO_DRV1_CLR	32	**GPIO DRV Control** For bitwise access of GPIO_DRV1
A0020900	GPIO_IES0	32	**GPIO IES Control** Configures GPIO input enabling control
A0020904	GPIO_IES0_SET	32	**GPIO IES Control** For bitwise access of GPIO_IES0
A0020908	GPIO_IES0_CLR	32	**GPIO IES Control** For bitwise access of GPIO_IES0
A0020910	GPIO_IES1	32	**GPIO IES Control** Configures GPIO input enabling control
A0020914	GPIO_IES1_SET	32	**GPIO IES Control** For bitwise access of GPIO_IES1
A0020918	GPIO_IES1_CLR	32	**GPIO IES Control** For bitwise access of GPIO_IES1
A0020A00	GPIO_PUPD0	32	**GPIO PUPD Control** Configures GPIO PUPD control
A0020A04	GPIO_PUPD0_SET	32	**GPIO PUPD Control** For bitwise access of GPIO_PUPD0
A0020A08	GPIO_PUPD0_CLR	32	**GPIO PUPD Control** For bitwise access of GPIO_PUPD0
A0020A10	GPIO_PUPD1	32	**GPIO PUPD Control** Configures GPIO PUPD control
A0020A14	GPIO_PUPD1_SET	32	**GPIO PUPD Control** For bitwise access of GPIO_PUPD1
A0020A18	GPIO_PUPD1_CLR	32	**GPIO PUPD Control** For bitwise access of GPIO_PUPD1
A0020B00	GPIO_RESEN0_0	32	**GPIO R0 Control** Configures GPIO R0 control
A0020B04	GPIO_RESEN0_0_SET	32	**GPIO R0 Control** For bitwise access of GPIO_RESEN0_0
A0020B08	GPIO_RESEN0_0_CLR	32	**GPIO R0 Control** For bitwise access of GPIO_RESEN0_0
A0020B10	GPIO_RESEN0_1	32	**GPIO R0 Control** Configures GPIO R0 control
A0020B14	GPIO_RESEN0_1_SET	32	**GPIO R0 Control** For bitwise access of GPIO_RESEN0_1
A0020B18	GPIO_RESEN0_1_CLR	32	**GPIO R0 Control** For bitwise access of GPIO_RESEN0_1
A0020B20	GPIO_RESEN1_0	32	**GPIO R1 Control** Configures GPIO R1 control
A0020B24	GPIO_RESEN1_0_SET	32	**GPIO R1 Control** For bitwise access of GPIO_RESEN1_0

Address	Name	Width	Register Function
A0020B28	GPIO_RESEN1_0_CLR	32	**GPIO R1 Control** For bitwise access of GPIO_RESEN1_0
A0020B30	GPIO_RESEN1_1	32	**GPIO R1 Control** Configures GPIO R1 control
A0020B34	GPIO_RESEN1_1_SET	32	**GPIO R1 Control** For bitwise access of GPIO_RESEN1_1
A0020B38	GPIO_RESEN1_1_CLR	32	**GPIO R1 Control** For bitwise access of GPIO_RESEN1_1
A0020C00	GPIO_MODE0	32	**GPIO Mode Control** Configures GPIO aux. mode
A0020C04	GPIO_MODE0_SET	32	**GPIO Mode Control** For bitwise access of GPIO_MODE0
A0020C08	GPIO_MODE0_CLR	32	**GPIO Mode Control** For bitwise access of GPIO_MODE0
A0020C10	GPIO_MODE1	32	**GPIO Mode Control** Configures GPIO aux. mode
A0020C14	GPIO_MODE1_SET	32	**GPIO Mode Control** For bitwise access of GPIO_MODE1
A0020C18	GPIO_MODE1_CLR	32	**GPIO Mode Control** For bitwise access of GPIO_MODE1
A0020C20	GPIO_MODE2	32	**GPIO Mode Control** Configures GPIO aux. mode
A0020C24	GPIO_MODE2_SET	32	**GPIO Mode Control** For bitwise access of GPIO_MODE2
A0020C28	GPIO_MODE2_CLR	32	**GPIO Mode Control** For bitwise access of GPIO_MODE2
A0020C30	GPIO_MODE3	32	**GPIO Mode Control** Configures GPIO aux. mode
A0020C34	GPIO_MODE3_SET	32	**GPIO Mode Control** For bitwise access of GPIO_MODE3
A0020C38	GPIO_MODE3_CLR	32	**GPIO Mode Control** For bitwise access of GPIO_MODE3
A0020C40	GPIO_MODE4	32	**GPIO Mode Control** Configures GPIO aux. mode
A0020C44	GPIO_MODE4_SET	32	**GPIO Mode Control** For bitwise access of GPIO_MODE4
A0020C48	GPIO_MODE4_CLR	32	**GPIO Mode Control** For bitwise access of GPIO_MODE4
A0020C50	GPIO_MODE5	32	**GPIO Mode Control** Configures GPIO aux. mode
A0020C54	GPIO_MODE5_SET	32	**GPIO Mode Control** For bitwise access of GPIO_MODE5
A0020C58	GPIO_MODE5_CLR	32	**GPIO Mode Control** For bitwise access of GPIO_MODE5
A0020C60	GPIO_MODE6	32	**GPIO Mode Control** Configures GPIO aux. mode
A0020C64	GPIO_MODE6_SET	32	**GPIO Mode Control** For bitwise access of GPIO_MODE6
A0020C68	GPIO_MODE6_CLR	32	**GPIO Mode Control** For bitwise access of GPIO_MODE6
A0020D10	GPIO_TDSEL	32	**GPIO TDSEL Control**

Address	Name	Width	Register Function
			GPIO TX duty control register
A0020D14	GPIO_TDSEL_SET	32	**GPIO TDSEL Control** For bitwise access of GPIO_TDSEL
A0020D18	GPIO_TDSEL_CLR	32	**GPIO TDSEL Control** For bitwise access of GPIO_TDSEL
A0020E00	CLK_OUT0	32	**CLK Out Selection Control** CLK OUT0 Setting
A0020E10	CLK_OUT1	32	**CLK Out Selection Control** CLK OUT1 Setting
A0020E20	CLK_OUT2	32	**CLK Out Selection Control** CLK OUT2 Setting
A0020E30	CLK_OUT3	32	**CLK Out Selection Control** CLK OUT3 Setting
A0020E40	CLK_OUT4	32	**CLK Out Selection Control** CLK OUT4 Setting
A0020E50	CLK_OUT5	32	**CLK Out Selection Control** CLK OUT5 Setting

A0020000 GPIO_DIR0 GPIO Direction Control 040008E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	1	0	0	0	1	1	1	0	0	0	0	0

Overview: Configures GPIO direction

Bit(s)	Mnemonic	Name	Description
31	**GPIO31**	GPIO31_DIR	**GPIO31 direction control** 0: GPIO as input 1: GPIO as output
30	**GPIO30**	GPIO30_DIR	**GPIO30 direction control** 0: GPIO as input 1: GPIO as output
29	**GPIO29**	GPIO29_DIR	**GPIO29 direction control** 0: GPIO as input 1: GPIO as output
28	**GPIO28**	GPIO28_DIR	**GPIO28 direction control** 0: GPIO as input 1: GPIO as output
27	**GPIO27**	GPIO27_DIR	**GPIO27 direction control** 0: GPIO as input 1: GPIO as output
26	**GPIO26**	GPIO26_DIR	**GPIO26 direction control** 0: GPIO as input

Bit(s)	Mnemonic	Name	Description
			1: GPIO as output
25	**GPIO25**	GPIO25_DIR	**GPIO25 direction control** 0: GPIO as input 1: GPIO as output
24	**GPIO24**	GPIO24_DIR	**GPIO24 direction control** 0: GPIO as input 1: GPIO as output
23	**GPIO23**	GPIO23_DIR	**GPIO23 direction control** 0: GPIO as input 1: GPIO as output
22	**GPIO22**	GPIO22_DIR	**GPIO22 direction control** 0: GPIO as input 1: GPIO as output
21	**GPIO21**	GPIO21_DIR	**GPIO21 direction control** 0: GPIO as input 1: GPIO as output
20	**GPIO20**	GPIO20_DIR	**GPIO20 direction control** 0: GPIO as input 1: GPIO as output
19	**GPIO19**	GPIO19_DIR	**GPIO19 direction control** 0: GPIO as input 1: GPIO as output
18	**GPIO18**	GPIO18_DIR	**GPIO18 direction control** 0: GPIO as input 1: GPIO as output
17	**GPIO17**	GPIO17_DIR	**GPIO17 direction control** 0: GPIO as input 1: GPIO as output
16	**GPIO16**	GPIO16_DIR	**GPIO16 direction control** 0: GPIO as input 1: GPIO as output
15	**GPIO15**	GPIO15_DIR	**GPIO15 direction control** 0: GPIO as input 1: GPIO as output
14	**GPIO14**	GPIO14_DIR	**GPIO14 direction control** 0: GPIO as input 1: GPIO as output
13	**GPIO13**	GPIO13_DIR	**GPIO13 direction control** 0: GPIO as input 1: GPIO as output
12	**GPIO12**	GPIO12_DIR	**GPIO12 direction control** 0: GPIO as input 1: GPIO as output
11	**GPIO11**	GPIO11_DIR	**GPIO11 direction control** 0: GPIO as input 1: GPIO as output
10	**GPIO10**	GPIO10_DIR	**GPIO10 direction control** 0: GPIO as input 1: GPIO as output
9	**GPIO9**	GPIO9_DIR	**GPIO9 direction control** 0: GPIO as input 1: GPIO as output

Bit(s)	Mnemonic	Name	Description
8	**GPIO8**	GPIO8_DIR	**GPIO8 direction control** 0: GPIO as input 1: GPIO as output
7	**GPIO7**	GPIO7_DIR	**GPIO7 direction control** 0: GPIO as input 1: GPIO as output
6	**GPIO6**	GPIO6_DIR	**GPIO6 direction control** 0: GPIO as input 1: GPIO as output
5	**GPIO5**	GPIO5_DIR	**GPIO5 direction control** 0: GPIO as input 1: GPIO as output
4	**GPIO4**	GPIO4_DIR	**GPIO4 direction control** 0: GPIO as input 1: GPIO as output
3	**GPIO3**	GPIO3_DIR	**GPIO3 direction control** 0: GPIO as input 1: GPIO as output
2	**GPIO2**	GPIO2_DIR	**GPIO2 direction control** 0: GPIO as input 1: GPIO as output
1	**GPIO1**	GPIO1_DIR	**GPIO1 direction control** 0: GPIO as input 1: GPIO as output
0	**GPIO0**	GPIO0_DIR	**GPIO0 direction control** 0: GPIO as input 1: GPIO as output

A0020004 GPIO_DIR0_SET GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DIR0

Bit(s)	Mnemonic	Name	Description
31	**GPIO31**	GPIO31_DIR	**Bitwise SET operation of GPIO31 direction** 0: Keep 1: SET bits
30	**GPIO30**	GPIO30_DIR	**Bitwise SET operation of GPIO30 direction** 0: Keep 1: SET bits

Bit(s)	Mnemonic	Name	Description	
29	**GPIO29**	GPIO29_DIR	**Bitwise SET operation of GPIO29 direction** 0: 1: SET bits	Keep
28	**GPIO28**	GPIO28_DIR	**Bitwise SET operation of GPIO28 direction** 0: 1: SET bits	Keep
27	**GPIO27**	GPIO27_DIR	**Bitwise SET operation of GPIO27 direction** 0: 1: SET bits	Keep
26	**GPIO26**	GPIO26_DIR	**Bitwise SET operation of GPIO26 direction** 0: 1: SET bits	Keep
25	**GPIO25**	GPIO25_DIR	**Bitwise SET operation of GPIO25 direction** 0: 1: SET bits	Keep
24	**GPIO24**	GPIO24_DIR	**Bitwise SET operation of GPIO24 direction** 0: 1: SET bits	Keep
23	**GPIO23**	GPIO23_DIR	**Bitwise SET operation of GPIO23 direction** 0: 1: SET bits	Keep
22	**GPIO22**	GPIO22_DIR	**Bitwise SET operation of GPIO22 direction** 0: 1: SET bits	Keep
21	**GPIO21**	GPIO21_DIR	**Bitwise SET operation of GPIO21 direction** 0: 1: SET bits	Keep
20	**GPIO20**	GPIO20_DIR	**Bitwise SET operation of GPIO20 direction** 0: 1: SET bits	Keep
19	**GPIO19**	GPIO19_DIR	**Bitwise SET operation of GPIO19 direction** 0: 1: SET bits	Keep
18	**GPIO18**	GPIO18_DIR	**Bitwise SET operation of GPIO18 direction** 0: 1: SET bits	Keep
17	**GPIO17**	GPIO17_DIR	**Bitwise SET operation of GPIO17 direction** 0: 1: SET bits	Keep
16	**GPIO16**	GPIO16_DIR	**Bitwise SET operation of GPIO16 direction** 0: 1: SET bits	Keep
15	**GPIO15**	GPIO15_DIR	**Bitwise SET operation of GPIO15 direction** 0: 1: SET bits	Keep
14	**GPIO14**	GPIO14_DIR	**Bitwise SET operation of GPIO14 direction** 0: 1: SET bits	Keep
13	**GPIO13**	GPIO13_DIR	**Bitwise SET operation of GPIO13 direction** 0: 1: SET bits	Keep
12	**GPIO12**	GPIO12_DIR	**Bitwise SET operation of GPIO12 direction**	

Bit(s)	Mnemonic	Name	Description	
			0: 1: SET bits	Keep
11	**GPIO11**	GPIO11_DIR	**Bitwise SET operation of GPIO11 direction** 0: 1: SET bits	Keep
10	**GPIO10**	GPIO10_DIR	**Bitwise SET operation of GPIO10 direction** 0: 1: SET bits	Keep
9	**GPIO9**	GPIO9_DIR	**Bitwise SET operation of GPIO9 direction** 0: 1: SET bits	Keep
8	**GPIO8**	GPIO8_DIR	**Bitwise SET operation of GPIO8 direction** 0: 1: SET bits	Keep
7	**GPIO7**	GPIO7_DIR	**Bitwise SET operation of GPIO7 direction** 0: 1: SET bits	Keep
6	**GPIO6**	GPIO6_DIR	**Bitwise SET operation of GPIO6 direction** 0: 1: SET bits	Keep
5	**GPIO5**	GPIO5_DIR	**Bitwise SET operation of GPIO5 direction** 0: 1: SET bits	Keep
4	**GPIO4**	GPIO4_DIR	**Bitwise SET operation of GPIO4 direction** 0: 1: SET bits	Keep
3	**GPIO3**	GPIO3_DIR	**Bitwise SET operation of GPIO3 direction** 0: 1: SET bits	Keep
2	**GPIO2**	GPIO2_DIR	**Bitwise SET operation of GPIO2 direction** 0: 1: SET bits	Keep
1	**GPIO1**	GPIO1_DIR	**Bitwise SET operation of GPIO1 direction** 0: 1: SET bits	Keep
0	**GPIO0**	GPIO0_DIR	**Bitwise SET operation of GPIO0 direction** 0: 1: SET bits	Keep

A0020008 GPIO_DIR0_CLR GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Mne	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mne	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DIR0

Bit(s)	Mnemonic	Name	Description	
31	**GPIO31**	GPIO31_DIR	**Bitwise CLR operation of GPIO31 direction**	
			0:	Keep
			1: CLR bits	
30	**GPIO30**	GPIO30_DIR	**Bitwise CLR operation of GPIO30 direction**	
			0:	Keep
			1: CLR bits	
29	**GPIO29**	GPIO29_DIR	**Bitwise CLR operation of GPIO29 direction**	
			0:	Keep
			1: CLR bits	
28	**GPIO28**	GPIO28_DIR	**Bitwise CLR operation of GPIO28 direction**	
			0:	Keep
			1: CLR bits	
27	**GPIO27**	GPIO27_DIR	**Bitwise CLR operation of GPIO27 direction**	
			0:	Keep
			1: CLR bits	
26	**GPIO26**	GPIO26_DIR	**Bitwise CLR operation of GPIO26 direction**	
			0:	Keep
			1: CLR bits	
25	**GPIO25**	GPIO25_DIR	**Bitwise CLR operation of GPIO25 direction**	
			0:	Keep
			1: CLR bits	
24	**GPIO24**	GPIO24_DIR	**Bitwise CLR operation of GPIO24 direction**	
			0:	Keep
			1: CLR bits	
23	**GPIO23**	GPIO23_DIR	**Bitwise CLR operation of GPIO23 direction**	
			0:	Keep
			1: CLR bits	
22	**GPIO22**	GPIO22_DIR	**Bitwise CLR operation of GPIO22 direction**	
			0:	Keep
			1: CLR bits	
21	**GPIO21**	GPIO21_DIR	**Bitwise CLR operation of GPIO21 direction**	
			0:	Keep
			1: CLR bits	
20	**GPIO20**	GPIO20_DIR	**Bitwise CLR operation of GPIO20 direction**	
			0:	Keep
			1: CLR bits	
19	**GPIO19**	GPIO19_DIR	**Bitwise CLR operation of GPIO19 direction**	
			0:	Keep
			1: CLR bits	
18	**GPIO18**	GPIO18_DIR	**Bitwise CLR operation of GPIO18 direction**	
			0:	Keep
			1: CLR bits	
17	**GPIO17**	GPIO17_DIR	**Bitwise CLR operation of GPIO17 direction**	
			0:	Keep
			1: CLR bits	
16	**GPIO16**	GPIO16_DIR	**Bitwise CLR operation of GPIO16 direction**	
			0:	Keep
			1: CLR bits	
15	**GPIO15**	GPIO15_DIR	**Bitwise CLR operation of GPIO15 direction**	
			0:	Keep

Bit(s)	Mnemonic	Name	Description	
			1: CLR bits	
14	**GPIO14**	GPIO14_DIR	**Bitwise CLR operation of GPIO14 direction**	
			0: 1: CLR bits	Keep
13	**GPIO13**	GPIO13_DIR	**Bitwise CLR operation of GPIO13 direction**	
			0: 1: CLR bits	Keep
12	**GPIO12**	GPIO12_DIR	**Bitwise CLR operation of GPIO12 direction**	
			0: 1: CLR bits	Keep
11	**GPIO11**	GPIO11_DIR	**Bitwise CLR operation of GPIO11 direction**	
			0: 1: CLR bits	Keep
10	**GPIO10**	GPIO10_DIR	**Bitwise CLR operation of GPIO10 direction**	
			0: 1: CLR bits	Keep
9	**GPIO9**	GPIO9_DIR	**Bitwise CLR operation of GPIO9 direction**	
			0: 1: CLR bits	Keep
8	**GPIO8**	GPIO8_DIR	**Bitwise CLR operation of GPIO8 direction**	
			0: 1: CLR bits	Keep
7	**GPIO7**	GPIO7_DIR	**Bitwise CLR operation of GPIO7 direction**	
			0: 1: CLR bits	Keep
6	**GPIO6**	GPIO6_DIR	**Bitwise CLR operation of GPIO6 direction**	
			0: 1: CLR bits	Keep
5	**GPIO5**	GPIO5_DIR	**Bitwise CLR operation of GPIO5 direction**	
			0: 1: CLR bits	Keep
4	**GPIO4**	GPIO4_DIR	**Bitwise CLR operation of GPIO4 direction**	
			0: 1: CLR bits	Keep
3	**GPIO3**	GPIO3_DIR	**Bitwise CLR operation of GPIO3 direction**	
			0: 1: CLR bits	Keep
2	**GPIO2**	GPIO2_DIR	**Bitwise CLR operation of GPIO2 direction**	
			0: 1: CLR bits	Keep
1	**GPIO1**	GPIO1_DIR	**Bitwise CLR operation of GPIO1 direction**	
			0: 1: CLR bits	Keep
0	**GPIO0**	GPIO0_DIR	**Bitwise CLR operation of GPIO0 direction**	
			0: 1: CLR bits	Keep

A0020010 GPIO_DIR1 GPIO Direction Control 00004000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GPIO5	GPIO5			GPIO5	GPIO5	GPIO4	GPIO4

									5	4			1	0	9	8
Type									RW	RW			RW	RW	RW	RW
Reset									0	0			0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: Configures GPIO direction

Bit(s)	Mnemonic	Name	Description
23	**GPIO55**	GPIO55_DIR	**GPIO55 direction control** 0: GPIO as input 1: GPIO as output
22	**GPIO54**	GPIO54_DIR	**GPIO54 direction control** 0: GPIO as input 1: GPIO as output
19	**GPIO51**	GPIO51_DIR	**GPIO51 direction control** 0: GPIO as input 1: GPIO as output
18	**GPIO50**	GPIO50_DIR	**GPIO50 direction control** 0: GPIO as input 1: GPIO as output
17	**GPIO49**	GPIO49_DIR	**GPIO49 direction control** 0: GPIO as input 1: GPIO as output
16	**GPIO48**	GPIO48_DIR	**GPIO48 direction control** 0: GPIO as input 1: GPIO as output
15	**GPIO47**	GPIO47_DIR	**GPIO47 direction control** 0: GPIO as input 1: GPIO as output
14	**GPIO46**	GPIO46_DIR	**GPIO46 direction control** 0: GPIO as input 1: GPIO as output
13	**GPIO45**	GPIO45_DIR	**GPIO45 direction control** 0: GPIO as input 1: GPIO as output
12	**GPIO44**	GPIO44_DIR	**GPIO44 direction control** 0: GPIO as input 1: GPIO as output
11	**GPIO43**	GPIO43_DIR	**GPIO43 direction control** 0: GPIO as input 1: GPIO as output
10	**GPIO42**	GPIO42_DIR	**GPIO42 direction control** 0: GPIO as input 1: GPIO as output
9	**GPIO41**	GPIO41_DIR	**GPIO41 direction control** 0: GPIO as input 1: GPIO as output
8	**GPIO40**	GPIO40_DIR	**GPIO40 direction control** 0: GPIO as input 1: GPIO as output

Bit(s)	Mnemonic	Name	Description
7	**GPIO39**	GPIO39_DIR	**GPIO39 direction control** 0: GPIO as input 1: GPIO as output
6	**GPIO38**	GPIO38_DIR	**GPIO38 direction control** 0: GPIO as input 1: GPIO as output
5	**GPIO37**	GPIO37_DIR	**GPIO37 direction control** 0: GPIO as input 1: GPIO as output
4	**GPIO36**	GPIO36_DIR	**GPIO36 direction control** 0: GPIO as input 1: GPIO as output
3	**GPIO35**	GPIO35_DIR	**GPIO35 direction control** 0: GPIO as input 1: GPIO as output
2	**GPIO34**	GPIO34_DIR	**GPIO34 direction control** 0: GPIO as input 1: GPIO as output
1	**GPIO33**	GPIO33_DIR	**GPIO33 direction control** 0: GPIO as input 1: GPIO as output
0	**GPIO32**	GPIO32_DIR	**GPIO32 direction control** 0: GPIO as input 1: GPIO as output

A0020014 GPIO_DIR1_SET GPIO Direction Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GPIO55	GPIO54			GPIO51	GPIO50	GPIO49	GPIO48
Type									WO	WO			WO	WO	WO	WO
Reset									0	0			0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DIR1

Bit(s)	Mnemonic	Name	Description
23	**GPIO55**	GPIO55_DIR	**Bitwise SET operation of GPIO55 direction** 0: Keep 1: SET bits
22	**GPIO54**	GPIO54_DIR	**Bitwise SET operation of GPIO54 direction** 0: Keep 1: SET bits
19	**GPIO51**	GPIO51_DIR	**Bitwise SET operation of GPIO51 direction** 0: Keep 1: SET bits

Bit(s)	Mnemonic	Name	Description	
18	**GPIO50**	GPIO50_DIR	**Bitwise SET operation of GPIO50 direction** 0: 1: SET bits	Keep
17	**GPIO49**	GPIO49_DIR	**Bitwise SET operation of GPIO49 direction** 0: 1: SET bits	Keep
16	**GPIO48**	GPIO48_DIR	**Bitwise SET operation of GPIO48 direction** 0: 1: SET bits	Keep
15	**GPIO47**	GPIO47_DIR	**Bitwise SET operation of GPIO47 direction** 0: 1: SET bits	Keep
14	**GPIO46**	GPIO46_DIR	**Bitwise SET operation of GPIO46 direction** 0: 1: SET bits	Keep
13	**GPIO45**	GPIO45_DIR	**Bitwise SET operation of GPIO45 direction** 0: 1: SET bits	Keep
12	**GPIO44**	GPIO44_DIR	**Bitwise SET operation of GPIO44 direction** 0: 1: SET bits	Keep
11	**GPIO43**	GPIO43_DIR	**Bitwise SET operation of GPIO43 direction** 0: 1: SET bits	Keep
10	**GPIO42**	GPIO42_DIR	**Bitwise SET operation of GPIO42 direction** 0: 1: SET bits	Keep
9	**GPIO41**	GPIO41_DIR	**Bitwise SET operation of GPIO41 direction** 0: 1: SET bits	Keep
8	**GPIO40**	GPIO40_DIR	**Bitwise SET operation of GPIO40 direction** 0: 1: SET bits	Keep
7	**GPIO39**	GPIO39_DIR	**Bitwise SET operation of GPIO39 direction** 0: 1: SET bits	Keep
6	**GPIO38**	GPIO38_DIR	**Bitwise SET operation of GPIO38 direction** 0: 1: SET bits	Keep
5	**GPIO37**	GPIO37_DIR	**Bitwise SET operation of GPIO37 direction** 0: 1: SET bits	Keep
4	**GPIO36**	GPIO36_DIR	**Bitwise SET operation of GPIO36 direction** 0: 1: SET bits	Keep
3	**GPIO35**	GPIO35_DIR	**Bitwise SET operation of GPIO35 direction** 0: 1: SET bits	Keep
2	**GPIO34**	GPIO34_DIR	**Bitwise SET operation of GPIO34 direction** 0: 1: SET bits	Keep
1	**GPIO33**	GPIO33_DIR	**Bitwise SET operation of GPIO33 direction**	

Bit(s)	Mnemonic	Name	Description
			0: Keep 1: SET bits
0	**GPIO32**	GPIO32_DIR	**Bitwise SET operation of GPIO32 direction** 0: Keep 1: SET bits

A0020018 **GPIO_DIR1_CLR** **GPIO Direction Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GPIO55	GPIO54			GPIO51	GPIO50	GPIO49	GPIO48
Type									WO	WO			WO	WO	WO	WO
Reset									0	0			0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DIR1

Bit(s)	Mnemonic	Name	Description
23	**GPIO55**	GPIO55_DIR	**Bitwise CLR operation of GPIO55 direction** 0: Keep 1: CLR bits
22	**GPIO54**	GPIO54_DIR	**Bitwise CLR operation of GPIO54 direction** 0: Keep 1: CLR bits
19	**GPIO51**	GPIO51_DIR	**Bitwise CLR operation of GPIO51 direction** 0: Keep 1: CLR bits
18	**GPIO50**	GPIO50_DIR	**Bitwise CLR operation of GPIO50 direction** 0: Keep 1: CLR bits
17	**GPIO49**	GPIO49_DIR	**Bitwise CLR operation of GPIO49 direction** 0: Keep 1: CLR bits
16	**GPIO48**	GPIO48_DIR	**Bitwise CLR operation of GPIO48 direction** 0: Keep 1: CLR bits
15	**GPIO47**	GPIO47_DIR	**Bitwise CLR operation of GPIO47 direction** 0: Keep 1: CLR bits
14	**GPIO46**	GPIO46_DIR	**Bitwise CLR operation of GPIO46 direction** 0: Keep 1: CLR bits
13	**GPIO45**	GPIO45_DIR	**Bitwise CLR operation of GPIO45 direction** 0: Keep 1: CLR bits
12	**GPIO44**	GPIO44_DIR	**Bitwise CLR operation of GPIO44 direction** 0: Keep

Bit(s)	Mnemonic	Name	Description	
			1: CLR bits	
11	**GPIO43**	GPIO43_DIR	**Bitwise CLR operation of GPIO43 direction** 0: 1: CLR bits	Keep
10	**GPIO42**	GPIO42_DIR	**Bitwise CLR operation of GPIO42 direction** 0: 1: CLR bits	Keep
9	**GPIO41**	GPIO41_DIR	**Bitwise CLR operation of GPIO41 direction** 0: 1: CLR bits	Keep
8	**GPIO40**	GPIO40_DIR	**Bitwise CLR operation of GPIO40 direction** 0: 1: CLR bits	Keep
7	**GPIO39**	GPIO39_DIR	**Bitwise CLR operation of GPIO39 direction** 0: 1: CLR bits	Keep
6	**GPIO38**	GPIO38_DIR	**Bitwise CLR operation of GPIO38 direction** 0: 1: CLR bits	Keep
5	**GPIO37**	GPIO37_DIR	**Bitwise CLR operation of GPIO37 direction** 0: 1: CLR bits	Keep
4	**GPIO36**	GPIO36_DIR	**Bitwise CLR operation of GPIO36 direction** 0: 1: CLR bits	Keep
3	**GPIO35**	GPIO35_DIR	**Bitwise CLR operation of GPIO35 direction** 0: 1: CLR bits	Keep
2	**GPIO34**	GPIO34_DIR	**Bitwise CLR operation of GPIO34 direction** 0: 1: CLR bits	Keep
1	**GPIO33**	GPIO33_DIR	**Bitwise CLR operation of GPIO33 direction** 0: 1: CLR bits	Keep
0	**GPIO32**	GPIO32_DIR	**Bitwise CLR operation of GPIO32 direction** 0: 1: CLR bits	Keep

A0020100 GPIO_PULLEN0 GPIO Pull-up/down Enable Control 43C00BFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO30					GPIO25	GPIO24	GPIO23	GPIO22						
Type		RW					RW	RW	RW	RW						
Reset		1					1	1	1	1						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GPIO11		GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type					RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					1		1	1	1	1	1	1	1	1	1	1

Overview: Configures GPIO pull enabling

Bit(s)	Mnemonic	Name	Description	
30	**GPIO30**	GPIO30_PULLEN	**GPIO30 PULLEN** 0: 1: Enable	Disable
25	**GPIO25**	GPIO25_PULLEN	**GPIO25 PULLEN** 0: 1: Enable	Disable
24	**GPIO24**	GPIO24_PULLEN	**GPIO24 PULLEN** 0: 1: Enable	Disable
23	**GPIO23**	GPIO23_PULLEN	**GPIO23 PULLEN** 0: 1: Enable	Disable
22	**GPIO22**	GPIO22_PULLEN	**GPIO22 PULLEN** 0: 1: Enable	Disable
11	**GPIO11**	GPIO11_PULLEN	**GPIO11 PULLEN** 0: 1: Enable	Disable
9	**GPIO9**	GPIO9_PULLEN	**GPIO9 PULLEN** 0: 1: Enable	Disable
8	**GPIO8**	GPIO8_PULLEN	**GPIO8 PULLEN** 0: 1: Enable	Disable
7	**GPIO7**	GPIO7_PULLEN	**GPIO7 PULLEN** 0: 1: Enable	Disable
6	**GPIO6**	GPIO6_PULLEN	**GPIO6 PULLEN** 0: 1: Enable	Disable
5	**GPIO5**	GPIO5_PULLEN	**GPIO5 PULLEN** 0: 1: Enable	Disable
4	**GPIO4**	GPIO4_PULLEN	**GPIO4 PULLEN** 0: 1: Enable	Disable
3	**GPIO3**	GPIO3_PULLEN	**GPIO3 PULLEN** 0: 1: Enable	Disable
2	**GPIO2**	GPIO2_PULLEN	**GPIO2 PULLEN** 0: 1: Enable	Disable
1	**GPIO1**	GPIO1_PULLEN	**GPIO1 PULLEN** 0: 1: Enable	Disable
0	**GPIO0**	GPIO0_PULLEN	**GPIO0 PULLEN** 0: 1: Enable	Disable

A0020104 GPIO_PULLEN0_SET GPIO Pull-up/down Enable Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO30					GPIO25	GPIO24	GPIO23	GPIO22						
Type		WO					WO	WO	WO	WO						
Reset		0					0	0	0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GPIO11		GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type					WO		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset					0		0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_PULLEN0

Bit(s)	Mnemonic	Name	Description
30	**GPIO30**	GPIO30_PULLEN	**Bitwise SET operation of GPIO30 PULLEN_SET** 0: Keep 1: SET bits
25	**GPIO25**	GPIO25_PULLEN	**Bitwise SET operation of GPIO25 PULLEN_SET** 0: Keep 1: SET bits
24	**GPIO24**	GPIO24_PULLEN	**Bitwise SET operation of GPIO24 PULLEN_SET** 0: Keep 1: SET bits
23	**GPIO23**	GPIO23_PULLEN	**Bitwise SET operation of GPIO23 PULLEN_SET** 0: Keep 1: SET bits
22	**GPIO22**	GPIO22_PULLEN	**Bitwise SET operation of GPIO22 PULLEN_SET** 0: Keep 1: SET bits
11	**GPIO11**	GPIO11_PULLEN	**Bitwise SET operation of GPIO11 PULLEN_SET** 0: Keep 1: SET bits
9	**GPIO9**	GPIO9_PULLEN	**Bitwise SET operation of GPIO9 PULLEN_SET** 0: Keep 1: SET bits
8	**GPIO8**	GPIO8_PULLEN	**Bitwise SET operation of GPIO8 PULLEN_SET** 0: Keep 1: SET bits
7	**GPIO7**	GPIO7_PULLEN	**Bitwise SET operation of GPIO7 PULLEN_SET** 0: Keep 1: SET bits
6	**GPIO6**	GPIO6_PULLEN	**Bitwise SET operation of GPIO6 PULLEN_SET** 0: Keep 1: SET bits
5	**GPIO5**	GPIO5_PULLEN	**Bitwise SET operation of GPIO5 PULLEN_SET** 0: Keep 1: SET bits
4	**GPIO4**	GPIO4_PULLEN	**Bitwise SET operation of GPIO4 PULLEN_SET** 0: Keep 1: SET bits
3	**GPIO3**	GPIO3_PULLEN	**Bitwise SET operation of GPIO3 PULLEN_SET**

Bit(s)	Mnemonic	Name	Description
			0: Keep 1: SET bits
2	**GPIO2**	GPIO2_PULLEN	**Bitwise SET operation of GPIO2 PULLEN_SET** 0: Keep 1: SET bits
1	**GPIO1**	GPIO1_PULLEN	**Bitwise SET operation of GPIO1 PULLEN_SET** 0: Keep 1: SET bits
0	**GPIO0**	GPIO0_PULLEN	**Bitwise SET operation of GPIO0 PULLEN_SET** 0: Keep 1: SET bits

A0020108 GPIO_PULLEN0_CLR GPIO Pull-up/down Enable Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO30					GPIO25	GPIO24	GPIO23	GPIO22						
Type		WO					WO	WO	WO	WO						
Reset		0					0	0	0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GPIO11		GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type					WO		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset					0		0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_PULLEN0

Bit(s)	Mnemonic	Name	Description
30	**GPIO30**	GPIO30_PULLEN	**Bitwise CLR operation of GPIO30 PULLEN_CLR** 0: Keep 1: CLR bits
25	**GPIO25**	GPIO25_PULLEN	**Bitwise CLR operation of GPIO25 PULLEN_CLR** 0: Keep 1: CLR bits
24	**GPIO24**	GPIO24_PULLEN	**Bitwise CLR operation of GPIO24 PULLEN_CLR** 0: Keep 1: CLR bits
23	**GPIO23**	GPIO23_PULLEN	**Bitwise CLR operation of GPIO23 PULLEN_CLR** 0: Keep 1: CLR bits
22	**GPIO22**	GPIO22_PULLEN	**Bitwise CLR operation of GPIO22 PULLEN_CLR** 0: Keep 1: CLR bits
11	**GPIO11**	GPIO11_PULLEN	**Bitwise CLR operation of GPIO11 PULLEN_CLR** 0: Keep 1: CLR bits
9	**GPIO9**	GPIO9_PULLEN	**Bitwise CLR operation of GPIO9 PULLEN_CLR** 0: Keep 1: CLR bits
8	**GPIO8**	GPIO8_PULLEN	**Bitwise CLR operation of GPIO8 PULLEN_CLR** 0: Keep

Bit(s)	Mnemonic	Name	Description	
			1: CLR bits	
7	**GPIO7**	GPIO7_PULLEN	**Bitwise CLR operation of GPIO7 PULLEN_CLR** 0: Keep 1: CLR bits	
6	**GPIO6**	GPIO6_PULLEN	**Bitwise CLR operation of GPIO6 PULLEN_CLR** 0: Keep 1: CLR bits	
5	**GPIO5**	GPIO5_PULLEN	**Bitwise CLR operation of GPIO5 PULLEN_CLR** 0: Keep 1: CLR bits	
4	**GPIO4**	GPIO4_PULLEN	**Bitwise CLR operation of GPIO4 PULLEN_CLR** 0: Keep 1: CLR bits	
3	**GPIO3**	GPIO3_PULLEN	**Bitwise CLR operation of GPIO3 PULLEN_CLR** 0: Keep 1: CLR bits	
2	**GPIO2**	GPIO2_PULLEN	**Bitwise CLR operation of GPIO2 PULLEN_CLR** 0: Keep 1: CLR bits	
1	**GPIO1**	GPIO1_PULLEN	**Bitwise CLR operation of GPIO1 PULLEN_CLR** 0: Keep 1: CLR bits	
0	**GPIO0**	GPIO0_PULLEN	**Bitwise CLR operation of GPIO0 PULLEN_CLR** 0: Keep 1: CLR bits	

A0020110 **GPIO_PULLEN1 GPIO Pull-up/down Enable Control** **00F01800**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**GPIO55**	**GPIO54**	**GPIO53**	**GPIO52**				
Type									RW	RW	RW	RW				
Reset									1	1	1	1				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**GPIO44**	**GPIO43**											
Type				RW	RW											
Reset				1	1											

Overview: Configures GPIO pull enabling

Bit(s)	Mnemonic	Name	Description
23	**GPIO55**	GPIO55_PULLEN	**GPIO55 PULLEN** 0: Disable 1: Enable
22	**GPIO54**	GPIO54_PULLEN	**GPIO54 PULLEN** 0: Disable 1: Enable
21	**GPIO53**	GPIO53_PULLEN	**GPIO53 PULLEN** 0: Disable 1: Enable

Bit(s)	Mnemonic	Name	Description
20	**GPIO52**	GPIO52_PULLEN	**GPIO52 PULLEN** 0: Disable 1: Enable
12	**GPIO44**	GPIO44_PULLEN	**GPIO44 PULLEN** 0: Disable 1: Enable
11	**GPIO43**	GPIO43_PULLEN	**GPIO43 PULLEN** 0: Disable 1: Enable

A0020114 **GPIO_PULLEN1_SET** **GPIO Pull-up/down Enable Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GPIO55	GPIO54	GPIO53	GPIO52				
Type									WO	WO	WO	WO				
Reset									0	0	0	0				
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name				GPIO44	GPIO43											
Type				WO	WO											
Reset				0	0											

Overview: For bitwise access of GPIO_PULLEN1

Bit(s)	Mnemonic	Name	Description
23	**GPIO55**	GPIO55_PULLEN	**Bitwise SET operation of GPIO51 PULLEN_SET** 0: Keep 1: SET bits
22	**GPIO54**	GPIO54_PULLEN	**Bitwise SET operation of GPIO44 PULLEN_SET** 0: Keep 1: SET bits
21	**GPIO53**	GPIO53_PULLEN	**Bitwise SET operation of GPIO43 PULLEN_SET** 0: Keep 1: SET bits
20	**GPIO52**	GPIO52_PULLEN	**Bitwise SET operation of GPIO30 PULLEN_SET** 0: Keep 1: SET bits
12	**GPIO44**	GPIO44_PULLEN	**Bitwise SET operation of GPIO44 PULLEN_SET** 0: Keep 1: SET bits
11	**GPIO43**	GPIO43_PULLEN	**Bitwise SET operation of GPIO43 PULLEN_SET** 0: Keep 1: SET bits

A0020118 **GPIO_PULLEN1_CLR** **GPIO Pull-up/down Enable Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name									GPIO55	GPIO54	GPIO53	GPIO52				
Type									WO	WO	WO	WO				
Reset									0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				GPIO44	GPIO43											
Type				WO	WO											
Reset				0	0											

Overview: For bitwise access of GPIO_PULLEN1

Bit(s)	Mnemonic	Name	Description
23	**GPIO55**	GPIO55_PULLEN	**Bitwise CLR operation of GPIO51 PULLEN_CLR** 0: Keep 1: CLR bits
22	**GPIO54**	GPIO54_PULLEN	**Bitwise CLR operation of GPIO44 PULLEN_CLR** 0: Keep 1: CLR bits
21	**GPIO53**	GPIO53_PULLEN	**Bitwise CLR operation of GPIO43 PULLEN_CLR** 0: Keep 1: CLR bits
20	**GPIO52**	GPIO52_PULLEN	**Bitwise CLR operation of GPIO30 PULLEN_CLR** 0: Keep 1: CLR bits
12	**GPIO44**	GPIO44_PULLEN	**Bitwise CLR operation of GPIO44 PULLEN_CLR** 0: Keep 1: CLR bits
11	**GPIO43**	GPIO43_PULLEN	**Bitwise CLR operation of GPIO43 PULLEN_CLR** 0: Keep 1: CLR bits

A0020200 GPIO_DINV0 GPIO Data Inversion Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INV31	INV30	INV29	INV28	INV27	INV26	INV25	INV24	INV23	INV22	INV21	INV20	INV19	INV18	INV17	INV16
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INV15	INV14	INV13	INV12	INV11	INV10	INV9	INV8	INV7	INV6	INV5	INV4	INV3	INV2	INV1	INV0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: Configures GPIO inversion enabling

Bit(s)	Mnemonic	Name	Description
31	**INV31**	GPIO31_DINV	**GPIO31 inversion control** 0: Keep input value 1: Invert input value
30	**INV30**	GPIO30_DINV	**GPIO30 inversion control** 0: Keep input value 1: Invert input value
29	**INV29**	GPIO29_DINV	**GPIO29 inversion control**

Bit(s)	Mnemonic	Name	Description
			0: Keep input value 1: Invert input value
28	**INV28**	GPIO28_DINV	**GPIO28 inversion control** 0: Keep input value 1: Invert input value
27	**INV27**	GPIO27_DINV	**GPIO27 inversion control** 0: Keep input value 1: Invert input value
26	**INV26**	GPIO26_DINV	**GPIO26 inversion control** 0: Keep input value 1: Invert input value
25	**INV25**	GPIO25_DINV	**GPIO25 inversion control** 0: Keep input value 1: Invert input value
24	**INV24**	GPIO24_DINV	**GPIO24 inversion control** 0: Keep input value 1: Invert input value
23	**INV23**	GPIO23_DINV	**GPIO23 inversion control** 0: Keep input value 1: Invert input value
22	**INV22**	GPIO22_DINV	**GPIO22 inversion control** 0: Keep input value 1: Invert input value
21	**INV21**	GPIO21_DINV	**GPIO21 inversion control** 0: Keep input value 1: Invert input value
20	**INV20**	GPIO20_DINV	**GPIO20 inversion control** 0: Keep input value 1: Invert input value
19	**INV19**	GPIO19_DINV	**GPIO19 inversion control** 0: Keep input value 1: Invert input value
18	**INV18**	GPIO18_DINV	**GPIO18 inversion control** 0: Keep input value 1: Invert input value
17	**INV17**	GPIO17_DINV	**GPIO17 inversion control** 0: Keep input value 1: Invert input value
16	**INV16**	GPIO16_DINV	**GPIO16 inversion control** 0: Keep input value 1: Invert input value
15	**INV15**	GPIO15_DINV	**GPIO15 inversion control** 0: Keep input value 1: Invert input value
14	**INV14**	GPIO14_DINV	**GPIO14 inversion control** 0: Keep input value 1: Invert input value
13	**INV13**	GPIO13_DINV	**GPIO13 inversion control** 0: Keep input value 1: Invert input value
12	**INV12**	GPIO12_DINV	**GPIO12 inversion control** 0: Keep input value

Bit(s)	Mnemonic	Name	Description
			1: Invert input value
11	**INV11**	GPIO11_DINV	**GPIO11 inversion control** 0: Keep input value 1: Invert input value
10	**INV10**	GPIO10_DINV	**GPIO10 inversion control** 0: Keep input value 1: Invert input value
9	**INV9**	GPIO9_DINV	**GPIO9 inversion control** 0: Keep input value 1: Invert input value
8	**INV8**	GPIO8_DINV	**GPIO8 inversion control** 0: Keep input value 1: Invert input value
7	**INV7**	GPIO7_DINV	**GPIO7 inversion control** 0: Keep input value 1: Invert input value
6	**INV6**	GPIO6_DINV	**GPIO6 inversion control** 0: Keep input value 1: Invert input value
5	**INV5**	GPIO5_DINV	**GPIO5 inversion control** 0: Keep input value 1: Invert input value
4	**INV4**	GPIO4_DINV	**GPIO4 inversion control** 0: Keep input value 1: Invert input value
3	**INV3**	GPIO3_DINV	**GPIO3 inversion control** 0: Keep input value 1: Invert input value
2	**INV2**	GPIO2_DINV	**GPIO2 inversion control** 0: Keep input value 1: Invert input value
1	**INV1**	GPIO1_DINV	**GPIO1 inversion control** 0: Keep input value 1: Invert input value
0	**INV0**	GPIO0_DINV	**GPIO0 inversion control** 0: Keep input value 1: Invert input value

A0020204 GPIO_DINV0_SET GPIO Data Inversion Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INV31	INV30	INV29	INV28	INV27	INV26	INV25	INV24	INV23	INV22	INV21	INV20	INV19	INV18	INV17	INV16
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INV15	INV14	INV13	INV12	INV11	INV10	INV9	INV8	INV7	INV6	INV5	INV4	INV3	INV2	INV1	INV0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DINV0

Bit(s)	Mnemonic	Name	Description
31	**INV31**	GPIO31_DINV	**Bitwise SET operation of GPIO31 inversion control** 0: Keep 1: SET bits
30	**INV30**	GPIO30_DINV	**Bitwise SET operation of GPIO30 inversion control** 0: Keep 1: SET bits
29	**INV29**	GPIO29_DINV	**Bitwise SET operation of GPIO29 inversion control** 0: Keep 1: SET bits
28	**INV28**	GPIO28_DINV	**Bitwise SET operation of GPIO28 inversion control** 0: Keep 1: SET bits
27	**INV27**	GPIO27_DINV	**Bitwise SET operation of GPIO27 inversion control** 0: Keep 1: SET bits
26	**INV26**	GPIO26_DINV	**Bitwise SET operation of GPIO26 inversion control** 0: Keep 1: SET bits
25	**INV25**	GPIO25_DINV	**Bitwise SET operation of GPIO25 inversion control** 0: Keep 1: SET bits
24	**INV24**	GPIO24_DINV	**Bitwise SET operation of GPIO24 inversion control** 0: Keep 1: SET bits
23	**INV23**	GPIO23_DINV	**Bitwise SET operation of GPIO23 inversion control** 0: Keep 1: SET bits
22	**INV22**	GPIO22_DINV	**Bitwise SET operation of GPIO22 inversion control** 0: Keep 1: SET bits
21	**INV21**	GPIO21_DINV	**Bitwise SET operation of GPIO21 inversion control** 0: Keep 1: SET bits
20	**INV20**	GPIO20_DINV	**Bitwise SET operation of GPIO20 inversion control** 0: Keep 1: SET bits
19	**INV19**	GPIO19_DINV	**Bitwise SET operation of GPIO19 inversion control** 0: Keep 1: SET bits
18	**INV18**	GPIO18_DINV	**Bitwise SET operation of GPIO18 inversion control** 0: Keep 1: SET bits
17	**INV17**	GPIO17_DINV	**Bitwise SET operation of GPIO17 inversion control** 0: Keep 1: SET bits
16	**INV16**	GPIO16_DINV	**Bitwise SET operation of GPIO16 inversion control** 0: Keep 1: SET bits
15	**INV15**	GPIO15_DINV	**Bitwise SET operation of GPIO15 inversion control** 0: Keep 1: SET bits
14	**INV14**	GPIO14_DINV	**Bitwise SET operation of GPIO14 inversion control**

Bit(s)	Mnemonic	Name	Description	
			0: 1: SET bits	Keep
13	**INV13**	GPIO13_DINV	**Bitwise SET operation of GPIO13 inversion control** 0: 1: SET bits	Keep
12	**INV12**	GPIO12_DINV	**Bitwise SET operation of GPIO12 inversion control** 0: 1: SET bits	Keep
11	**INV11**	GPIO11_DINV	**Bitwise SET operation of GPIO11 inversion control** 0: 1: SET bits	Keep
10	**INV10**	GPIO10_DINV	**Bitwise SET operation of GPIO10 inversion control** 0: 1: SET bits	Keep
9	**INV9**	GPIO9_DINV	**Bitwise SET operation of GPIO9 inversion control** 0: 1: SET bits	Keep
8	**INV8**	GPIO8_DINV	**Bitwise SET operation of GPIO8 inversion control** 0: 1: SET bits	Keep
7	**INV7**	GPIO7_DINV	**Bitwise SET operation of GPIO7 inversion control** 0: 1: SET bits	Keep
6	**INV6**	GPIO6_DINV	**Bitwise SET operation of GPIO6 inversion control** 0: 1: SET bits	Keep
5	**INV5**	GPIO5_DINV	**Bitwise SET operation of GPIO5 inversion control** 0: 1: SET bits	Keep
4	**INV4**	GPIO4_DINV	**Bitwise SET operation of GPIO4 inversion control** 0: 1: SET bits	Keep
3	**INV3**	GPIO3_DINV	**Bitwise SET operation of GPIO3 inversion control** 0: 1: SET bits	Keep
2	**INV2**	GPIO2_DINV	**Bitwise SET operation of GPIO2 inversion control** 0: 1: SET bits	Keep
1	**INV1**	GPIO1_DINV	**Bitwise SET operation of GPIO1 inversion control** 0: 1: SET bits	Keep
0	**INV0**	GPIO0_DINV	**Bitwise SET operation of GPIO0 inversion control** 0: 1: SET bits	Keep

A0020208 GPIO_DINV0_CLR GPIO Data Inversion Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INV31	INV30	INV29	INV28	INV27	INV26	INV25	INV24	INV23	INV22	INV21	INV20	INV19	INV18	INV17	INV16
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INV15	INV14	INV13	INV12	INV11	INV10	INV9	INV8	INV7	INV6	INV5	INV4	INV3	INV2	INV1	INV0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DINV0

Bit(s)	Mnemonic	Name	Description
31	**INV31**	GPIO31_DINV	**Bitwise CLR operation of GPIO31 inversion control** 0: Keep 1: CLR bits
30	**INV30**	GPIO30_DINV	**Bitwise CLR operation of GPIO30 inversion control** 0: Keep 1: CLR bits
29	**INV29**	GPIO29_DINV	**Bitwise CLR operation of GPIO29 inversion control** 0: Keep 1: CLR bits
28	**INV28**	GPIO28_DINV	**Bitwise CLR operation of GPIO28 inversion control** 0: Keep 1: CLR bits
27	**INV27**	GPIO27_DINV	**Bitwise CLR operation of GPIO27 inversion control** 0: Keep 1: CLR bits
26	**INV26**	GPIO26_DINV	**Bitwise CLR operation of GPIO26 inversion control** 0: Keep 1: CLR bits
25	**INV25**	GPIO25_DINV	**Bitwise CLR operation of GPIO25 inversion control** 0: Keep 1: CLR bits
24	**INV24**	GPIO24_DINV	**Bitwise CLR operation of GPIO24 inversion control** 0: Keep 1: CLR bits
23	**INV23**	GPIO23_DINV	**Bitwise CLR operation of GPIO23 inversion control** 0: Keep 1: CLR bits
22	**INV22**	GPIO22_DINV	**Bitwise CLR operation of GPIO22 inversion control** 0: Keep 1: CLR bits
21	**INV21**	GPIO21_DINV	**Bitwise CLR operation of GPIO21 inversion control** 0: Keep 1: CLR bits
20	**INV20**	GPIO20_DINV	**Bitwise CLR operation of GPIO20 inversion control** 0: Keep 1: CLR bits
19	**INV19**	GPIO19_DINV	**Bitwise CLR operation of GPIO19 inversion control** 0: Keep 1: CLR bits
18	**INV18**	GPIO18_DINV	**Bitwise CLR operation of GPIO18 inversion control** 0: Keep 1: CLR bits
17	**INV17**	GPIO17_DINV	**Bitwise CLR operation of GPIO17 inversion control** 0: Keep

Bit(s)	Mnemonic	Name	Description	
			1: CLR bits	
16	**INV16**	GPIO16_DINV	**Bitwise CLR operation of GPIO16 inversion control** 0: 1: CLR bits	Keep
15	**INV15**	GPIO15_DINV	**Bitwise CLR operation of GPIO15 inversion control** 0: 1: CLR bits	Keep
14	**INV14**	GPIO14_DINV	**Bitwise CLR operation of GPIO14 inversion control** 0: 1: CLR bits	Keep
13	**INV13**	GPIO13_DINV	**Bitwise CLR operation of GPIO13 inversion control** 0: 1: CLR bits	Keep
12	**INV12**	GPIO12_DINV	**Bitwise CLR operation of GPIO12 inversion control** 0: 1: CLR bits	Keep
11	**INV11**	GPIO11_DINV	**Bitwise CLR operation of GPIO11 inversion control** 0: 1: CLR bits	Keep
10	**INV10**	GPIO10_DINV	**Bitwise CLR operation of GPIO10 inversion control** 0: 1: CLR bits	Keep
9	**INV9**	GPIO9_DINV	**Bitwise CLR operation of GPIO9 inversion control** 0: 1: CLR bits	Keep
8	**INV8**	GPIO8_DINV	**Bitwise CLR operation of GPIO8 inversion control** 0: 1: CLR bits	Keep
7	**INV7**	GPIO7_DINV	**Bitwise CLR operation of GPIO7 inversion control** 0: 1: CLR bits	Keep
6	**INV6**	GPIO6_DINV	**Bitwise CLR operation of GPIO6 inversion control** 0: 1: CLR bits	Keep
5	**INV5**	GPIO5_DINV	**Bitwise CLR operation of GPIO5 inversion control** 0: 1: CLR bits	Keep
4	**INV4**	GPIO4_DINV	**Bitwise CLR operation of GPIO4 inversion control** 0: 1: CLR bits	Keep
3	**INV3**	GPIO3_DINV	**Bitwise CLR operation of GPIO3 inversion control** 0: 1: CLR bits	Keep
2	**INV2**	GPIO2_DINV	**Bitwise CLR operation of GPIO2 inversion control** 0: 1: CLR bits	Keep
1	**INV1**	GPIO1_DINV	**Bitwise CLR operation of GPIO1 inversion control** 0: 1: CLR bits	Keep
0	**INV0**	GPIO0_DINV	**Bitwise CLR operation of GPIO0 inversion control** 0: 1: CLR bits	Keep

A0020210 GPIO_DINV1 GPIO Data Inversion Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									INV55	INV54	INV53	INV52	INV51	INV50	INV49	INV48
Type									RW	RW	RW	RW	RW	RW	RW	RW
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INV47	INV46	INV45	INV44	INV43	INV42	INV41	INV40	INV39	INV38	INV37	INV36	INV35	INV34	INV33	INV32
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: Configures GPIO inversion enabling

Bit(s)	Mnemonic	Name	Description
23	**INV55**	GPIO55_DINV	**GPIO55 inversion control** 0: Keep input value 1: Invert input value
22	**INV54**	GPIO54_DINV	**GPIO54 inversion control** 0: Keep input value 1: Invert input value
21	**INV53**	GPIO53_DINV	**GPIO53 inversion control** 0: Keep input value 1: Invert input value
20	**INV52**	GPIO52_DINV	**GPIO52 inversion control** 0: Keep input value 1: Invert input value
19	**INV51**	GPIO51_DINV	**GPIO51 inversion control** 0: Keep input value 1: Invert input value
18	**INV50**	GPIO50_DINV	**GPIO50 inversion control** 0: Keep input value 1: Invert input value
17	**INV49**	GPIO49_DINV	**GPIO49 inversion control** 0: Keep input value 1: Invert input value
16	**INV48**	GPIO48_DINV	**GPIO48 inversion control** 0: Keep input value 1: Invert input value
15	**INV47**	GPIO47_DINV	**GPIO47 inversion control** 0: Keep input value 1: Invert input value
14	**INV46**	GPIO46_DINV	**GPIO46 inversion control** 0: Keep input value 1: Invert input value
13	**INV45**	GPIO45_DINV	**GPIO45 inversion control** 0: Keep input value 1: Invert input value
12	**INV44**	GPIO44_DINV	**GPIO44 inversion control** 0: Keep input value 1: Invert input value
11	**INV43**	GPIO43_DINV	**GPIO43 inversion control**

Bit(s)	Mnemonic	Name	Description
			0: Keep input value 1: Invert input value
10	**INV42**	GPIO42_DINV	**GPIO42 inversion control** 0: Keep input value 1: Invert input value
9	**INV41**	GPIO41_DINV	**GPIO41 inversion control** 0: Keep input value 1: Invert input value
8	**INV40**	GPIO40_DINV	**GPIO40 inversion control** 0: Keep input value 1: Invert input value
7	**INV39**	GPIO39_DINV	**GPIO39 inversion control** 0: Keep input value 1: Invert input value
6	**INV38**	GPIO38_DINV	**GPIO38 inversion control** 0: Keep input value 1: Invert input value
5	**INV37**	GPIO37_DINV	**GPIO37 inversion control** 0: Keep input value 1: Invert input value
4	**INV36**	GPIO36_DINV	**GPIO36 inversion control** 0: Keep input value 1: Invert input value
3	**INV35**	GPIO35_DINV	**GPIO35 inversion control** 0: Keep input value 1: Invert input value
2	**INV34**	GPIO34_DINV	**GPIO34 inversion control** 0: Keep input value 1: Invert input value
1	**INV33**	GPIO33_DINV	**GPIO33 inversion control** 0: Keep input value 1: Invert input value
0	**INV32**	GPIO32_DINV	**GPIO32 inversion control** 0: Keep input value 1: Invert input value

A0020214 **GPIO_DINV1_SET** **GPIO Data Inversion Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**INV55**	**INV54**	**INV53**	**INV52**	**INV51**	**INV50**	**INV49**	**INV48**
Type									WO	WO	WO	WO	WO	WO	WO	WO
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**INV47**	**INV46**	**INV45**	**INV44**	**INV43**	**INV42**	**INV41**	**INV40**	**INV39**	**INV38**	**INV37**	**INV36**	**INV35**	**INV34**	**INV33**	**INV32**
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DINV1

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description	
23	**INV55**	GPIO55_DINV	**Bitwise SET operation of GPIO55 inversion control** 0: 1: SET bits	Keep
22	**INV54**	GPIO54_DINV	**Bitwise SET operation of GPIO54 inversion control** 0: 1: SET bits	Keep
21	**INV53**	GPIO53_DINV	**Bitwise SET operation of GPIO53 inversion control** 0: 1: SET bits	Keep
20	**INV52**	GPIO52_DINV	**Bitwise SET operation of GPIO52 inversion control** 0: 1: SET bits	Keep
19	**INV51**	GPIO51_DINV	**Bitwise SET operation of GPIO51 inversion control** 0: 1: SET bits	Keep
18	**INV50**	GPIO50_DINV	**Bitwise SET operation of GPIO50 inversion control** 0: 1: SET bits	Keep
17	**INV49**	GPIO49_DINV	**Bitwise SET operation of GPIO49 inversion control** 0: 1: SET bits	Keep
16	**INV48**	GPIO48_DINV	**Bitwise SET operation of GPIO48 inversion control** 0: 1: SET bits	Keep
15	**INV47**	GPIO47_DINV	**Bitwise SET operation of GPIO47 inversion control** 0: 1: SET bits	Keep
14	**INV46**	GPIO46_DINV	**Bitwise SET operation of GPIO46 inversion control** 0: 1: SET bits	Keep
13	**INV45**	GPIO45_DINV	**Bitwise SET operation of GPIO45 inversion control** 0: 1: SET bits	Keep
12	**INV44**	GPIO44_DINV	**Bitwise SET operation of GPIO44 inversion control** 0: 1: SET bits	Keep
11	**INV43**	GPIO43_DINV	**Bitwise SET operation of GPIO43 inversion control** 0: 1: SET bits	Keep
10	**INV42**	GPIO42_DINV	**Bitwise SET operation of GPIO42 inversion control** 0: 1: SET bits	Keep
9	**INV41**	GPIO41_DINV	**Bitwise SET operation of GPIO41 inversion control** 0: 1: SET bits	Keep
8	**INV40**	GPIO40_DINV	**Bitwise SET operation of GPIO40 inversion control** 0: 1: SET bits	Keep
7	**INV39**	GPIO39_DINV	**Bitwise SET operation of GPIO39 inversion control** 0: 1: SET bits	Keep
6	**INV38**	GPIO38_DINV	**Bitwise SET operation of GPIO38 inversion control**	

Bit(s)	Mnemonic	Name	Description	
			0: 1: SET bits	Keep
5	**INV37**	GPIO37_DINV	**Bitwise SET operation of GPIO37 inversion control** 0: 1: SET bits	Keep
4	**INV36**	GPIO36_DINV	**Bitwise SET operation of GPIO36 inversion control** 0: 1: SET bits	Keep
3	**INV35**	GPIO35_DINV	**Bitwise SET operation of GPIO35 inversion control** 0: 1: SET bits	Keep
2	**INV34**	GPIO34_DINV	**Bitwise SET operation of GPIO34 inversion control** 0: 1: SET bits	Keep
1	**INV33**	GPIO33_DINV	**Bitwise SET operation of GPIO33 inversion control** 0: 1: SET bits	Keep
0	**INV32**	GPIO32_DINV	**Bitwise SET operation of GPIO32 inversion control** 0: 1: SET bits	Keep

A0020218 GPIO_DINV1_CLR GPIO Data Inversion Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									INV55	INV54	INV53	INV52	INV51	INV50	INV49	INV48
Type									WO	WO	WO	WO	WO	WO	WO	WO
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INV47	INV46	INV45	INV44	INV43	INV42	INV41	INV40	INV39	INV38	INV37	INV36	INV35	INV34	INV33	INV32
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DINV1

Bit(s)	Mnemonic	Name	Description	
23	**INV55**	GPIO55_DINV	**Bitwise CLR operation of GPIO55 inversion control** 0: 1: CLR bits	Keep
22	**INV54**	GPIO54_DINV	**Bitwise CLR operation of GPIO54 inversion control** 0: 1: CLR bits	Keep
21	**INV53**	GPIO53_DINV	**Bitwise CLR operation of GPIO53 inversion control** 0: 1: CLR bits	Keep
20	**INV52**	GPIO52_DINV	**Bitwise CLR operation of GPIO52 inversion control** 0: 1: CLR bits	Keep
19	**INV51**	GPIO51_DINV	**Bitwise CLR operation of GPIO51 inversion control** 0: 1: CLR bits	Keep

Bit(s)	Mnemonic	Name	Description	
18	**INV50**	GPIO50_DINV	**Bitwise CLR operation of GPIO50 inversion control** 0: 1: CLR bits	Keep
17	**INV49**	GPIO49_DINV	**Bitwise CLR operation of GPIO49 inversion control** 0: 1: CLR bits	Keep
16	**INV48**	GPIO48_DINV	**Bitwise CLR operation of GPIO48 inversion control** 0: 1: CLR bits	Keep
15	**INV47**	GPIO47_DINV	**Bitwise CLR operation of GPIO47 inversion control** 0: 1: CLR bits	Keep
14	**INV46**	GPIO46_DINV	**Bitwise CLR operation of GPIO46 inversion control** 0: 1: CLR bits	Keep
13	**INV45**	GPIO45_DINV	**Bitwise CLR operation of GPIO45 inversion control** 0: 1: CLR bits	Keep
12	**INV44**	GPIO44_DINV	**Bitwise CLR operation of GPIO44 inversion control** 0: 1: CLR bits	Keep
11	**INV43**	GPIO43_DINV	**Bitwise CLR operation of GPIO43 inversion control** 0: 1: CLR bits	Keep
10	**INV42**	GPIO42_DINV	**Bitwise CLR operation of GPIO42 inversion control** 0: 1: CLR bits	Keep
9	**INV41**	GPIO41_DINV	**Bitwise CLR operation of GPIO41 inversion control** 0: 1: CLR bits	Keep
8	**INV40**	GPIO40_DINV	**Bitwise CLR operation of GPIO40 inversion control** 0: 1: CLR bits	Keep
7	**INV39**	GPIO39_DINV	**Bitwise CLR operation of GPIO39 inversion control** 0: 1: CLR bits	Keep
6	**INV38**	GPIO38_DINV	**Bitwise CLR operation of GPIO38 inversion control** 0: 1: CLR bits	Keep
5	**INV37**	GPIO37_DINV	**Bitwise CLR operation of GPIO37 inversion control** 0: 1: CLR bits	Keep
4	**INV36**	GPIO36_DINV	**Bitwise CLR operation of GPIO36 inversion control** 0: 1: CLR bits	Keep
3	**INV35**	GPIO35_DINV	**Bitwise CLR operation of GPIO35 inversion control** 0: 1: CLR bits	Keep
2	**INV34**	GPIO34_DINV	**Bitwise CLR operation of GPIO34 inversion control** 0: 1: CLR bits	Keep
1	**INV33**	GPIO33_DINV	**Bitwise CLR operation of GPIO33 inversion control**	

Bit(s)	Mnemonic	Name	Description	
			0: 1: CLR bits	Keep
0	**INV32**	GPIO32_DINV	**Bitwise CLR operation of GPIO32 inversion control** 0: 1: CLR bits	Keep

A0020300 GPIO_DOUT0 GPIO Output Data Control 04000800

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

Overview: Configures GPIO output value

Bit(s)	Mnemonic	Name	Description		
31	**GPIO31**	GPIO31_OUT	**GPIO31 data output value** 0: GPIO	output	LO
			1: GPIO output HI		
30	**GPIO30**	GPIO30_OUT	**GPIO30 data output value** 0: GPIO	output	LO
			1: GPIO output HI		
29	**GPIO29**	GPIO29_OUT	**GPIO29 data output value** 0: GPIO	output	LO
			1: GPIO output HI		
28	**GPIO28**	GPIO28_OUT	**GPIO28 data output value** 0: GPIO	output	LO
			1: GPIO output HI		
27	**GPIO27**	GPIO27_OUT	**GPIO27 data output value** 0: GPIO	output	LO
			1: GPIO output HI		
26	**GPIO26**	GPIO26_OUT	**GPIO26 data output value** 0: GPIO	output	LO
			1: GPIO output HI		
25	**GPIO25**	GPIO25_OUT	**GPIO25 data output value** 0: GPIO	output	LO
			1: GPIO output HI		
24	**GPIO24**	GPIO24_OUT	**GPIO24 data output value** 0: GPIO	output	LO
			1: GPIO output HI		
23	**GPIO23**	GPIO23_OUT	**GPIO23 data output value** 0: GPIO	output	LO
			1: GPIO output HI		
22	**GPIO22**	GPIO22_OUT	**GPIO22 data output value** 0: GPIO	output	LO
			1: GPIO output HI		

Bit(s)	Mnemonic	Name	Description			
21	**GPIO21**	GPIO21_OUT	**GPIO21 data output value** 0: GPIO 1: GPIO output HI		output	LO
20	**GPIO20**	GPIO20_OUT	**GPIO20 data output value** 0: GPIO 1: GPIO output HI		output	LO
19	**GPIO19**	GPIO19_OUT	**GPIO19 data output value** 0: GPIO 1: GPIO output HI		output	LO
18	**GPIO18**	GPIO18_OUT	**GPIO18 data output value** 0: GPIO 1: GPIO output HI		output	LO
17	**GPIO17**	GPIO17_OUT	**GPIO17 data output value** 0: GPIO 1: GPIO output HI		output	LO
16	**GPIO16**	GPIO16_OUT	**GPIO16 data output value** 0: GPIO 1: GPIO output HI		output	LO
15	**GPIO15**	GPIO15_OUT	**GPIO15 data output value** 0: GPIO 1: GPIO output HI		output	LO
14	**GPIO14**	GPIO14_OUT	**GPIO14 data output value** 0: GPIO 1: GPIO output HI		output	LO
13	**GPIO13**	GPIO13_OUT	**GPIO13 data output value** 0: GPIO 1: GPIO output HI		output	LO
12	**GPIO12**	GPIO12_OUT	**GPIO12 data output value** 0: GPIO 1: GPIO output HI		output	LO
11	**GPIO11**	GPIO11_OUT	**GPIO11 data output value** 0: GPIO 1: GPIO output HI		output	LO
10	**GPIO10**	GPIO10_OUT	**GPIO10 data output value** 0: GPIO 1: GPIO output HI		output	LO
9	**GPIO9**	GPIO9_OUT	**GPIO9 data output value** 0: GPIO 1: GPIO output HI		output	LO
8	**GPIO8**	GPIO8_OUT	**GPIO8 data output value** 0: GPIO 1: GPIO output HI		output	LO
7	**GPIO7**	GPIO7_OUT	**GPIO7 data output value** 0: GPIO 1: GPIO output HI		output	LO
6	**GPIO6**	GPIO6_OUT	**GPIO6 data output value** 0: GPIO 1: GPIO output HI		output	LO
5	**GPIO5**	GPIO5_OUT	**GPIO5 data output value** 0: GPIO 1: GPIO output HI		output	LO
4	**GPIO4**	GPIO4_OUT	**GPIO4 data output value**			

Bit(s)	Mnemonic	Name	Description			
			0: GPIO output LO 1: GPIO output HI	GPIO	output	LO
3	**GPIO3**	GPIO3_OUT	**GPIO3 data output value** 0: GPIO output LO 1: GPIO output HI	GPIO	output	LO
2	**GPIO2**	GPIO2_OUT	**GPIO2 data output value** 0: GPIO output LO 1: GPIO output HI	GPIO	output	LO
1	**GPIO1**	GPIO1_OUT	**GPIO1 data output value** 0: GPIO output LO 1: GPIO output HI	GPIO	output	LO
0	**GPIO0**	GPIO0_OUT	**GPIO0 data output value** 0: GPIO output LO 1: GPIO output HI	GPIO	output	LO

A0020304 GPIO_DOUT0_SET GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DIR0

Bit(s)	Mnemonic	Name	Description	
31	**GPIO31**	GPIO31_OUT	**Bitwise SET operation of GPIO31 data output value** 0: Keep 1: SET bits	Keep
30	**GPIO30**	GPIO30_OUT	**Bitwise SET operation of GPIO30 data output value** 0: Keep 1: SET bits	Keep
29	**GPIO29**	GPIO29_OUT	**Bitwise SET operation of GPIO29 data output value** 0: Keep 1: SET bits	Keep
28	**GPIO28**	GPIO28_OUT	**Bitwise SET operation of GPIO28 data output value** 0: Keep 1: SET bits	Keep
27	**GPIO27**	GPIO27_OUT	**Bitwise SET operation of GPIO27 data output value** 0: Keep 1: SET bits	Keep
26	**GPIO26**	GPIO26_OUT	**Bitwise SET operation of GPIO26 data output value** 0: Keep 1: SET bits	Keep
25	**GPIO25**	GPIO25_OUT	**Bitwise SET operation of GPIO25 data output value** 0:	Keep

Bit(s)	Mnemonic	Name	Description	
			1: SET bits	
24	**GPIO24**	GPIO24_OUT	**Bitwise SET operation of GPIO24 data output value**	
			0: 1: SET bits	Keep
23	**GPIO23**	GPIO23_OUT	**Bitwise SET operation of GPIO23 data output value**	
			0: 1: SET bits	Keep
22	**GPIO22**	GPIO22_OUT	**Bitwise SET operation of GPIO22 data output value**	
			0: 1: SET bits	Keep
21	**GPIO21**	GPIO21_OUT	**Bitwise SET operation of GPIO21 data output value**	
			0: 1: SET bits	Keep
20	**GPIO20**	GPIO20_OUT	**Bitwise SET operation of GPIO20 data output value**	
			0: 1: SET bits	Keep
19	**GPIO19**	GPIO19_OUT	**Bitwise SET operation of GPIO19 data output value**	
			0: 1: SET bits	Keep
18	**GPIO18**	GPIO18_OUT	**Bitwise SET operation of GPIO18 data output value**	
			0: 1: SET bits	Keep
17	**GPIO17**	GPIO17_OUT	**Bitwise SET operation of GPIO17 data output value**	
			0: 1: SET bits	Keep
16	**GPIO16**	GPIO16_OUT	**Bitwise SET operation of GPIO16 data output value**	
			0: 1: SET bits	Keep
15	**GPIO15**	GPIO15_OUT	**Bitwise SET operation of GPIO15 data output value**	
			0: 1: SET bits	Keep
14	**GPIO14**	GPIO14_OUT	**Bitwise SET operation of GPIO14 data output value**	
			0: 1: SET bits	Keep
13	**GPIO13**	GPIO13_OUT	**Bitwise SET operation of GPIO13 data output value**	
			0: 1: SET bits	Keep
12	**GPIO12**	GPIO12_OUT	**Bitwise SET operation of GPIO12 data output value**	
			0: 1: SET bits	Keep
11	**GPIO11**	GPIO11_OUT	**Bitwise SET operation of GPIO11 data output value**	
			0: 1: SET bits	Keep
10	**GPIO10**	GPIO10_OUT	**Bitwise SET operation of GPIO10 data output value**	
			0: 1: SET bits	Keep
9	**GPIO9**	GPIO9_OUT	**Bitwise SET operation of GPIO9 data output value**	
			0: 1: SET bits	Keep
8	**GPIO8**	GPIO8_OUT	**Bitwise SET operation of GPIO8 data output value**	
			0: 1: SET bits	Keep

Bit(s)	Mnemonic	Name	Description
7	**GPIO7**	GPIO7_OUT	**Bitwise SET operation of GPIO7 data output value** 0: Keep 1: SET bits
6	**GPIO6**	GPIO6_OUT	**Bitwise SET operation of GPIO6 data output value** 0: Keep 1: SET bits
5	**GPIO5**	GPIO5_OUT	**Bitwise SET operation of GPIO5 data output value** 0: Keep 1: SET bits
4	**GPIO4**	GPIO4_OUT	**Bitwise SET operation of GPIO4 data output value** 0: Keep 1: SET bits
3	**GPIO3**	GPIO3_OUT	**Bitwise SET operation of GPIO3 data output value** 0: Keep 1: SET bits
2	**GPIO2**	GPIO2_OUT	**Bitwise SET operation of GPIO2 data output value** 0: Keep 1: SET bits
1	**GPIO1**	GPIO1_OUT	**Bitwise SET operation of GPIO1 data output value** 0: Keep 1: SET bits
0	**GPIO0**	GPIO0_OUT	**Bitwise SET operation of GPIO0 data output value** 0: Keep 1: SET bits

A0020308 GPIO_DOUT0_CLR GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DIR0

Bit(s)	Mnemonic	Name	Description
31	**GPIO31**	GPIO31_OUT	**Bitwise CLR operation of GPIO31 data output value** 0: Keep 1: CLR bits
30	**GPIO30**	GPIO30_OUT	**Bitwise CLR operation of GPIO30 data output value** 0: Keep 1: CLR bits
29	**GPIO29**	GPIO29_OUT	**Bitwise CLR operation of GPIO29 data output value** 0: Keep 1: CLR bits

Bit(s)	Mnemonic	Name	Description	
28	**GPIO28**	GPIO28_OUT	**Bitwise CLR operation of GPIO28 data output value** 0: 1: CLR bits	Keep
27	**GPIO27**	GPIO27_OUT	**Bitwise CLR operation of GPIO27 data output value** 0: 1: CLR bits	Keep
26	**GPIO26**	GPIO26_OUT	**Bitwise CLR operation of GPIO26 data output value** 0: 1: CLR bits	Keep
25	**GPIO25**	GPIO25_OUT	**Bitwise CLR operation of GPIO25 data output value** 0: 1: CLR bits	Keep
24	**GPIO24**	GPIO24_OUT	**Bitwise CLR operation of GPIO24 data output value** 0: 1: CLR bits	Keep
23	**GPIO23**	GPIO23_OUT	**Bitwise CLR operation of GPIO23 data output value** 0: 1: CLR bits	Keep
22	**GPIO22**	GPIO22_OUT	**Bitwise CLR operation of GPIO22 data output value** 0: 1: CLR bits	Keep
21	**GPIO21**	GPIO21_OUT	**Bitwise CLR operation of GPIO21 data output value** 0: 1: CLR bits	Keep
20	**GPIO20**	GPIO20_OUT	**Bitwise CLR operation of GPIO20 data output value** 0: 1: CLR bits	Keep
19	**GPIO19**	GPIO19_OUT	**Bitwise CLR operation of GPIO19 data output value** 0: 1: CLR bits	Keep
18	**GPIO18**	GPIO18_OUT	**Bitwise CLR operation of GPIO18 data output value** 0: 1: CLR bits	Keep
17	**GPIO17**	GPIO17_OUT	**Bitwise CLR operation of GPIO17 data output value** 0: 1: CLR bits	Keep
16	**GPIO16**	GPIO16_OUT	**Bitwise CLR operation of GPIO16 data output value** 0: 1: CLR bits	Keep
15	**GPIO15**	GPIO15_OUT	**Bitwise CLR operation of GPIO15 data output value** 0: 1: CLR bits	Keep
14	**GPIO14**	GPIO14_OUT	**Bitwise CLR operation of GPIO14 data output value** 0: 1: CLR bits	Keep
13	**GPIO13**	GPIO13_OUT	**Bitwise CLR operation of GPIO13 data output value** 0: 1: CLR bits	Keep
12	**GPIO12**	GPIO12_OUT	**Bitwise CLR operation of GPIO12 data output value** 0: 1: CLR bits	Keep
11	**GPIO11**	GPIO11_OUT	**Bitwise CLR operation of GPIO11 data output value**	

Bit(s)	Mnemonic	Name	Description	
			0: 1: CLR bits	Keep
10	**GPIO10**	GPIO10_OUT	**Bitwise CLR operation of GPIO10 data output value** 0: 1: CLR bits	Keep
9	**GPIO9**	GPIO9_OUT	**Bitwise CLR operation of GPIO9 data output value** 0: 1: CLR bits	Keep
8	**GPIO8**	GPIO8_OUT	**Bitwise CLR operation of GPIO8 data output value** 0: 1: CLR bits	Keep
7	**GPIO7**	GPIO7_OUT	**Bitwise CLR operation of GPIO7 data output value** 0: 1: CLR bits	Keep
6	**GPIO6**	GPIO6_OUT	**Bitwise CLR operation of GPIO6 data output value** 0: 1: CLR bits	Keep
5	**GPIO5**	GPIO5_OUT	**Bitwise CLR operation of GPIO5 data output value** 0: 1: CLR bits	Keep
4	**GPIO4**	GPIO4_OUT	**Bitwise CLR operation of GPIO4 data output value** 0: 1: CLR bits	Keep
3	**GPIO3**	GPIO3_OUT	**Bitwise CLR operation of GPIO3 data output value** 0: 1: CLR bits	Keep
2	**GPIO2**	GPIO2_OUT	**Bitwise CLR operation of GPIO2 data output value** 0: 1: CLR bits	Keep
1	**GPIO1**	GPIO1_OUT	**Bitwise CLR operation of GPIO1 data output value** 0: 1: CLR bits	Keep
0	**GPIO0**	GPIO0_OUT	**Bitwise CLR operation of GPIO0 data output value** 0: 1: CLR bits	Keep

A0020310 GPIO_DOUT1 GPIO Output Data Control 00004000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GPIO55	GPIO54			GPIO51	GPIO50	GPIO49	GPIO48
Type									RW	RW			RW	RW	RW	RW
Reset									0	0			0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: Configures GPIO output value

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description		
23	**GPIO55**	GPIO55_OUT	**GPIO55 data output value** 0: GPIO output LO 1: GPIO output HI	output	
22	**GPIO54**	GPIO54_OUT	**GPIO54 data output value** 0: GPIO output LO 1: GPIO output HI	output	
19	**GPIO51**	GPIO51_OUT	**GPIO51 data output value** 0: GPIO output LO 1: GPIO output HI	output	
18	**GPIO50**	GPIO50_OUT	**GPIO50 data output value** 0: GPIO output LO 1: GPIO output HI	output	
17	**GPIO49**	GPIO49_OUT	**GPIO49 data output value** 0: GPIO output LO 1: GPIO output HI	output	
16	**GPIO48**	GPIO48_OUT	**GPIO48 data output value** 0: GPIO output LO 1: GPIO output HI	output	
15	**GPIO47**	GPIO47_OUT	**GPIO47 data output value** 0: GPIO output LO 1: GPIO output HI	output	
14	**GPIO46**	GPIO46_OUT	**GPIO46 data output value** 0: GPIO output LO 1: GPIO output HI	output	
13	**GPIO45**	GPIO45_OUT	**GPIO45 data output value** 0: GPIO output LO 1: GPIO output HI	output	
12	**GPIO44**	GPIO44_OUT	**GPIO44 data output value** 0: GPIO output LO 1: GPIO output HI	output	
11	**GPIO43**	GPIO43_OUT	**GPIO43 data output value** 0: GPIO output LO 1: GPIO output HI	output	
10	**GPIO42**	GPIO42_OUT	**GPIO42 data output value** 0: GPIO output LO 1: GPIO output HI	output	
9	**GPIO41**	GPIO41_OUT	**GPIO41 data output value** 0: GPIO output LO 1: GPIO output HI	output	
8	**GPIO40**	GPIO40_OUT	**GPIO40 data output value** 0: GPIO output LO 1: GPIO output HI	output	
7	**GPIO39**	GPIO39_OUT	**GPIO39 data output value** 0: GPIO output LO 1: GPIO output HI	output	
6	**GPIO38**	GPIO38_OUT	**GPIO38 data output value** 0: GPIO output LO 1: GPIO output HI	output	
5	**GPIO37**	GPIO37_OUT	**GPIO37 data output value** 0: GPIO output LO 1: GPIO output HI	output	
4	**GPIO36**	GPIO36_OUT	**GPIO36 data output value**		

Bit(s)	Mnemonic	Name	Description
			0: GPIO output LO 1: GPIO output HI
3	**GPIO35**	GPIO35_OUT	**GPIO35 data output value** 0: GPIO output LO 1: GPIO output HI
2	**GPIO34**	GPIO34_OUT	**GPIO34 data output value** 0: GPIO output LO 1: GPIO output HI
1	**GPIO33**	GPIO33_OUT	**GPIO33 data output value** 0: GPIO output LO 1: GPIO output HI
0	**GPIO32**	GPIO32_OUT	**GPIO32 data output value** 0: GPIO output LO 1: GPIO output HI

A0020314 GPIO_DOUT1_SET GPIO Output Data Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**GPIO55**	**GPIO54**			**GPIO51**	**GPIO50**	**GPIO49**	**GPIO48**
Type									WO	WO			WO	WO	WO	WO
Reset									0	0			0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GPIO47**	**GPIO46**	**GPIO45**	**GPIO44**	**GPIO43**	**GPIO42**	**GPIO41**	**GPIO40**	**GPIO39**	**GPIO38**	**GPIO37**	**GPIO36**	**GPIO35**	**GPIO34**	**GPIO33**	**GPIO32**
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DIR1

Bit(s)	Mnemonic	Name	Description
23	**GPIO55**	GPIO55_OUT	**Bitwise SET operation of GPIO55 data output value** 0: Keep 1: SET bits
22	**GPIO54**	GPIO54_OUT	**Bitwise SET operation of GPIO54 data output value** 0: Keep 1: SET bits
19	**GPIO51**	GPIO51_OUT	**Bitwise SET operation of GPIO51 data output value** 0: Keep 1: SET bits
18	**GPIO50**	GPIO50_OUT	**Bitwise SET operation of GPIO50 data output value** 0: Keep 1: SET bits
17	**GPIO49**	GPIO49_OUT	**Bitwise SET operation of GPIO49 data output value** 0: Keep 1: SET bits
16	**GPIO48**	GPIO48_OUT	**Bitwise SET operation of GPIO48 data output value** 0: Keep 1: SET bits
15	**GPIO47**	GPIO47_OUT	**Bitwise SET operation of GPIO47 data output value** 0: Keep

Bit(s)	Mnemonic	Name	Description	
			1: SET bits	
14	**GPIO46**	GPIO46_OUT	**Bitwise SET operation of GPIO46 data output value** 0: 1: SET bits	Keep
13	**GPIO45**	GPIO45_OUT	**Bitwise SET operation of GPIO45 data output value** 0: 1: SET bits	Keep
12	**GPIO44**	GPIO44_OUT	**Bitwise SET operation of GPIO44 data output value** 0: 1: SET bits	Keep
11	**GPIO43**	GPIO43_OUT	**Bitwise SET operation of GPIO43 data output value** 0: 1: SET bits	Keep
10	**GPIO42**	GPIO42_OUT	**Bitwise SET operation of GPIO42 data output value** 0: 1: SET bits	Keep
9	**GPIO41**	GPIO41_OUT	**Bitwise SET operation of GPIO41 data output value** 0: 1: SET bits	Keep
8	**GPIO40**	GPIO40_OUT	**Bitwise SET operation of GPIO40 data output value** 0: 1: SET bits	Keep
7	**GPIO39**	GPIO39_OUT	**Bitwise SET operation of GPIO39 data output value** 0: 1: SET bits	Keep
6	**GPIO38**	GPIO38_OUT	**Bitwise SET operation of GPIO38 data output value** 0: 1: SET bits	Keep
5	**GPIO37**	GPIO37_OUT	**Bitwise SET operation of GPIO37 data output value** 0: 1: SET bits	Keep
4	**GPIO36**	GPIO36_OUT	**Bitwise SET operation of GPIO36 data output value** 0: 1: SET bits	Keep
3	**GPIO35**	GPIO35_OUT	**Bitwise SET operation of GPIO35 data output value** 0: 1: SET bits	Keep
2	**GPIO34**	GPIO34_OUT	**Bitwise SET operation of GPIO34 data output value** 0: 1: SET bits	Keep
1	**GPIO33**	GPIO33_OUT	**Bitwise SET operation of GPIO33 data output value** 0: 1: SET bits	Keep
0	**GPIO32**	GPIO32_OUT	**Bitwise SET operation of GPIO32 data output value** 0: 1: SET bits	Keep

A0020318 **GPIO_DOUT1_CLR** **GPIO Output Data Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name									GPIO55	GPIO54			GPIO51	GPIO50	GPIO49	GPIO48
Type									WO	WO			WO	WO	WO	WO
Reset									0	0			0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DIR1

Bit(s)	Mnemonic	Name	Description
23	**GPIO55**	GPIO55_OUT	**Bitwise CLR operation of GPIO55 data output value** 0: Keep 1: CLR bits
22	**GPIO54**	GPIO54_OUT	**Bitwise CLR operation of GPIO54 data output value** 0: Keep 1: CLR bits
19	**GPIO51**	GPIO51_OUT	**Bitwise CLR operation of GPIO51 data output value** 0: Keep 1: CLR bits
18	**GPIO50**	GPIO50_OUT	**Bitwise CLR operation of GPIO50 data output value** 0: Keep 1: CLR bits
17	**GPIO49**	GPIO49_OUT	**Bitwise CLR operation of GPIO49 data output value** 0: Keep 1: CLR bits
16	**GPIO48**	GPIO48_OUT	**Bitwise CLR operation of GPIO48 data output value** 0: Keep 1: CLR bits
15	**GPIO47**	GPIO47_OUT	**Bitwise CLR operation of GPIO47 data output value** 0: Keep 1: CLR bits
14	**GPIO46**	GPIO46_OUT	**Bitwise CLR operation of GPIO46 data output value** 0: Keep 1: CLR bits
13	**GPIO45**	GPIO45_OUT	**Bitwise CLR operation of GPIO45 data output value** 0: Keep 1: CLR bits
12	**GPIO44**	GPIO44_OUT	**Bitwise CLR operation of GPIO44 data output value** 0: Keep 1: CLR bits
11	**GPIO43**	GPIO43_OUT	**Bitwise CLR operation of GPIO43 data output value** 0: Keep 1: CLR bits
10	**GPIO42**	GPIO42_OUT	**Bitwise CLR operation of GPIO42 data output value** 0: Keep 1: CLR bits
9	**GPIO41**	GPIO41_OUT	**Bitwise CLR operation of GPIO41 data output value** 0: Keep 1: CLR bits
8	**GPIO40**	GPIO40_OUT	**Bitwise CLR operation of GPIO40 data output value** 0: Keep

Bit(s)	Mnemonic	Name	Description
			1: CLR bits
7	**GPIO39**	GPIO39_OUT	**Bitwise CLR operation of GPIO39 data output value** 0: Keep 1: CLR bits
6	**GPIO38**	GPIO38_OUT	**Bitwise CLR operation of GPIO38 data output value** 0: Keep 1: CLR bits
5	**GPIO37**	GPIO37_OUT	**Bitwise CLR operation of GPIO37 data output value** 0: Keep 1: CLR bits
4	**GPIO36**	GPIO36_OUT	**Bitwise CLR operation of GPIO36 data output value** 0: Keep 1: CLR bits
3	**GPIO35**	GPIO35_OUT	**Bitwise CLR operation of GPIO35 data output value** 0: Keep 1: CLR bits
2	**GPIO34**	GPIO34_OUT	**Bitwise CLR operation of GPIO34 data output value** 0: Keep 1: CLR bits
1	**GPIO33**	GPIO33_OUT	**Bitwise CLR operation of GPIO33 data output value** 0: Keep 1: CLR bits
0	**GPIO32**	GPIO32_OUT	**Bitwise CLR operation of GPIO32 data output value** 0: Keep 1: CLR bits

A0020400 **GPIO_DIN0** **GPIO Input Data Value** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: Reads GPIO input value

Bit(s)	Mnemonic	Name	Description
31	**GPIO31**	GPIO31_DIN	GPIO31 data input value
30	**GPIO30**	GPIO30_DIN	GPIO30 data input value
29	**GPIO29**	GPIO29_DIN	GPIO29 data input value
28	**GPIO28**	GPIO28_DIN	GPIO28 data input value
27	**GPIO27**	GPIO27_DIN	GPIO27 data input value
26	**GPIO26**	GPIO26_DIN	GPIO26 data input value
25	**GPIO25**	GPIO25_DIN	GPIO25 data input value
24	**GPIO24**	GPIO24_DIN	GPIO24 data input value

Bit(s)	Mnemonic	Name	Description
23	**GPIO23**	GPIO23_DIN	GPIO23 data input value
22	**GPIO22**	GPIO22_DIN	GPIO22 data input value
21	**GPIO21**	GPIO21_DIN	GPIO21 data input value
20	**GPIO20**	GPIO20_DIN	GPIO20 data input value
19	**GPIO19**	GPIO19_DIN	GPIO19 data input value
18	**GPIO18**	GPIO18_DIN	GPIO18 data input value
17	**GPIO17**	GPIO17_DIN	GPIO17 data input value
16	**GPIO16**	GPIO16_DIN	GPIO16 data input value
15	**GPIO15**	GPIO15_DIN	GPIO15 data input value
14	**GPIO14**	GPIO14_DIN	GPIO14 data input value
13	**GPIO13**	GPIO13_DIN	GPIO13 data input value
12	**GPIO12**	GPIO12_DIN	GPIO12 data input value
11	**GPIO11**	GPIO11_DIN	GPIO11 data input value
10	**GPIO10**	GPIO10_DIN	GPIO10 data input value
9	**GPIO9**	GPIO9_DIN	GPIO9 data input value
8	**GPIO8**	GPIO8_DIN	GPIO8 data input value
7	**GPIO7**	GPIO7_DIN	GPIO7 data input value
6	**GPIO6**	GPIO6_DIN	GPIO6 data input value
5	**GPIO5**	GPIO5_DIN	GPIO5 data input value
4	**GPIO4**	GPIO4_DIN	GPIO4 data input value
3	**GPIO3**	GPIO3_DIN	GPIO3 data input value
2	**GPIO2**	GPIO2_DIN	GPIO2 data input value
1	**GPIO1**	GPIO1_DIN	GPIO1 data input value
0	**GPIO0**	GPIO0_DIN	GPIO0 data input value

A0020410 GPIO_DIN1 GPIO Input Data Value 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GPIO55	GPIO54	GPIO53	GPIO52	GPIO51	GPIO50	GPIO49	GPIO48
Type									RO	RO	RO	RO	RO	RO	RO	RO
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: Reads GPIO input value

Bit(s)	Mnemonic	Name	Description
23	**GPIO55**	GPIO55_DIN	GPIO55 data input value
22	**GPIO54**	GPIO54_DIN	GPIO54 data input value
21	**GPIO53**	GPIO53_DIN	GPIO53 data input value
20	**GPIO52**	GPIO52_DIN	GPIO52 data input value
19	**GPIO51**	GPIO51_DIN	GPIO51 data input value
18	**GPIO50**	GPIO50_DIN	GPIO50 data input value

Bit(s)	Mnemonic	Name	Description
17	**GPIO49**	GPIO49_DIN	GPIO49 data input value
16	**GPIO48**	GPIO48_DIN	GPIO48 data input value
15	**GPIO47**	GPIO47_DIN	GPIO47 data input value
14	**GPIO46**	GPIO46_DIN	GPIO46 data input value
13	**GPIO45**	GPIO45_DIN	GPIO45 data input value
12	**GPIO44**	GPIO44_DIN	GPIO44 data input value
11	**GPIO43**	GPIO43_DIN	GPIO43 data input value
10	**GPIO42**	GPIO42_DIN	GPIO42 data input value
9	**GPIO41**	GPIO41_DIN	GPIO41 data input value
8	**GPIO40**	GPIO40_DIN	GPIO40 data input value
7	**GPIO39**	GPIO39_DIN	GPIO39 data input value
6	**GPIO38**	GPIO38_DIN	GPIO38 data input value
5	**GPIO37**	GPIO37_DIN	GPIO37 data input value
4	**GPIO36**	GPIO36_DIN	GPIO36 data input value
3	**GPIO35**	GPIO35_DIN	GPIO35 data input value
2	**GPIO34**	GPIO34_DIN	GPIO34 data input value
1	**GPIO33**	GPIO33_DIN	GPIO33 data input value
0	**GPIO32**	GPIO32_DIN	GPIO32 data input value

A0020500 **GPIO_PULLSEL0** **GPIO Pullsel Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO30					GPIO25	GPIO24	GPIO23	GPIO22						
Type		RW					RW	RW	RW	RW						
Reset		0					0	0	0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GPIO11		GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type					RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					0		0	0	0	0	0	0	0	0	0	0

Overview: Configures GPIO PUPD selection

Bit(s)	Mnemonic	Name	Description
30	**GPIO30**	GPIO30_PULLSEL	**GPIO30 PULLSEL** 0: Pull down 1: Pull up
25	**GPIO25**	GPIO25_PULLSEL	**GPIO25 PULLSEL** 0: Pull down 1: Pull up
24	**GPIO24**	GPIO24_PULLSEL	**GPIO24 PULLSEL** 0: Pull down 1: Pull up
23	**GPIO23**	GPIO23_PULLSEL	**GPIO23 PULLSEL** 0: Pull down 1: Pull up

Bit(s)	Mnemonic	Name	Description
22	**GPIO22**	GPIO22_PULLSEL	**GPIO22 PULLSEL** 0: Pull down 1: Pull up
11	**GPIO11**	GPIO11_PULLSEL	**GPIO11 PULLSEL** 0: Pull down 1: Pull up
9	**GPIO9**	GPIO9_PULLSEL	**GPIO9 PULLSEL** 0: Pull down 1: Pull up
8	**GPIO8**	GPIO8_PULLSEL	**GPIO8 PULLSEL** 0: Pull down 1: Pull up
7	**GPIO7**	GPIO7_PULLSEL	**GPIO7 PULLSEL** 0: Pull down 1: Pull up
6	**GPIO6**	GPIO6_PULLSEL	**GPIO6 PULLSEL** 0: Pull down 1: Pull up
5	**GPIO5**	GPIO5_PULLSEL	**GPIO5 PULLSEL** 0: Pull down 1: Pull up
4	**GPIO4**	GPIO4_PULLSEL	**GPIO4 PULLSEL** 0: Pull down 1: Pull up
3	**GPIO3**	GPIO3_PULLSEL	**GPIO3 PULLSEL** 0: Pull down 1: Pull up
2	**GPIO2**	GPIO2_PULLSEL	**GPIO2 PULLSEL** 0: Pull down 1: Pull up
1	**GPIO1**	GPIO1_PULLSEL	**GPIO1 PULLSEL** 0: Pull down 1: Pull up
0	**GPIO0**	GPIO0_PULLSEL	**GPIO0 PULLSEL** 0: Pull down 1: Pull up

A0020504 GPIO_PULLSEL0_SET GPIO Pullsel Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO30					GPIO25	GPIO24	GPIO23	GPIO22						
Type		WO					WO	WO	WO	WO						
Reset		0					0	0	0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GPIO11		GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type					WO		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset					0		0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_PULLSEL0

Bit(s)	Mnemonic	Name	Description	
30	**GPIO30**	GPIO30_PULLSEL	**Bitwise SET operation of GPIO30 PULLSEL_SET** 0: 1: SET bits	Keep
25	**GPIO25**	GPIO25_PULLSEL	**Bitwise SET operation of GPIO25 PULLSEL_SET** 0: 1: SET bits	Keep
24	**GPIO24**	GPIO24_PULLSEL	**Bitwise SET operation of GPIO24 PULLSEL_SET** 0: 1: SET bits	Keep
23	**GPIO23**	GPIO23_PULLSEL	**Bitwise SET operation of GPIO23 PULLSEL_SET** 0: 1: SET bits	Keep
22	**GPIO22**	GPIO22_PULLSEL	**Bitwise SET operation of GPIO22 PULLSEL_SET** 0: 1: SET bits	Keep
11	**GPIO11**	GPIO11_PULLSEL	**Bitwise SET operation of GPIO11 PULLSEL_SET** 0: 1: SET bits	Keep
9	**GPIO9**	GPIO9_PULLSEL	**Bitwise SET operation of GPIO9 PULLSEL_SET** 0: 1: SET bits	Keep
8	**GPIO8**	GPIO8_PULLSEL	**Bitwise SET operation of GPIO8 PULLSEL_SET** 0: 1: SET bits	Keep
7	**GPIO7**	GPIO7_PULLSEL	**Bitwise SET operation of GPIO7 PULLSEL_SET** 0: 1: SET bits	Keep
6	**GPIO6**	GPIO6_PULLSEL	**Bitwise SET operation of GPIO6 PULLSEL_SET** 0: 1: SET bits	Keep
5	**GPIO5**	GPIO5_PULLSEL	**Bitwise SET operation of GPIO5 PULLSEL_SET** 0: 1: SET bits	Keep
4	**GPIO4**	GPIO4_PULLSEL	**Bitwise SET operation of GPIO4 PULLSEL_SET** 0: 1: SET bits	Keep
3	**GPIO3**	GPIO3_PULLSEL	**Bitwise SET operation of GPIO3 PULLSEL_SET** 0: 1: SET bits	Keep
2	**GPIO2**	GPIO2_PULLSEL	**Bitwise SET operation of GPIO2 PULLSEL_SET** 0: 1: SET bits	Keep
1	**GPIO1**	GPIO1_PULLSEL	**Bitwise SET operation of GPIO1 PULLSEL_SET** 0: 1: SET bits	Keep
0	**GPIO0**	GPIO0_PULLSEL	**Bitwise SET operation of GPIO0 PULLSEL_SET** 0: 1: SET bits	Keep

A0020508 **GPIO_PULLSEL0_CLR** **GPIO Pullsel Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO30					GPIO25	GPIO24	GPIO23	GPIO22						
Type		WO					WO	WO	WO	WO						
Reset		0					0	0	0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GPIO11		GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type					WO		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset					0		0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_PULLSEL0

Bit(s)	Mnemonic	Name	Description
30	**GPIO30**	GPIO30_PULLSEL	**Bitwise CKR operation of GPIO30 PULLSEL_CLR** 0: Keep 1: CLR bits
25	**GPIO25**	GPIO25_PULLSEL	**Bitwise CKR operation of GPIO25 PULLSEL_CLR** 0: Keep 1: CLR bits
24	**GPIO24**	GPIO24_PULLSEL	**Bitwise CKR operation of GPIO24 PULLSEL_CLR** 0: Keep 1: CLR bits
23	**GPIO23**	GPIO23_PULLSEL	**Bitwise CKR operation of GPIO23 PULLSEL_CLR** 0: Keep 1: CLR bits
22	**GPIO22**	GPIO22_PULLSEL	**Bitwise CKR operation of GPIO22 PULLSEL_CLR** 0: Keep 1: CLR bits
11	**GPIO11**	GPIO11_PULLSEL	**Bitwise CKR operation of GPIO11 PULLSEL_CLR** 0: Keep 1: CLR bits
9	**GPIO9**	GPIO9_PULLSEL	**Bitwise CKR operation of GPIO9 PULLSEL_CLR** 0: Keep 1: CLR bits
8	**GPIO8**	GPIO8_PULLSEL	**Bitwise CKR operation of GPIO8 PULLSEL_CLR** 0: Keep 1: CLR bits
7	**GPIO7**	GPIO7_PULLSEL	**Bitwise CKR operation of GPIO7 PULLSEL_CLR** 0: Keep 1: CLR bits
6	**GPIO6**	GPIO6_PULLSEL	**Bitwise CKR operation of GPIO6 PULLSEL_CLR** 0: Keep 1: CLR bits
5	**GPIO5**	GPIO5_PULLSEL	**Bitwise CKR operation of GPIO5 PULLSEL_CLR** 0: Keep 1: CLR bits
4	**GPIO4**	GPIO4_PULLSEL	**Bitwise CKR operation of GPIO4 PULLSEL_CLR** 0: Keep 1: CLR bits
3	**GPIO3**	GPIO3_PULLSEL	**Bitwise CKR operation of GPIO3 PULLSEL_CLR**

Bit(s)	Mnemonic	Name	Description
			0: Keep 1: CLR bits
2	**GPIO2**	GPIO2_PULLSEL	**Bitwise CKR operation of GPIO2 PULLSEL_CLR** 0: Keep 1: CLR bits
1	**GPIO1**	GPIO1_PULLSEL	**Bitwise CKR operation of GPIO1 PULLSEL_CLR** 0: Keep 1: CLR bits
0	**GPIO0**	GPIO0_PULLSEL	**Bitwise CKR operation of GPIO0 PULLSEL_CLR** 0: Keep 1: CLR bits

A0020510 GPIO_PULLSEL1 GPIO Pullsel Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									**GPIO55**	**GPIO54**	**GPIO53**	**GPIO52**				
Type									RW	RW	RW	RW				
Reset									0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				**GPIO44**	**GPIO43**											
Type				RW	RW											
Reset				0	0											

Overview: Configures GPIO PUPD selection

Bit(s)	Mnemonic	Name	Description
23	**GPIO55**	GPIO55_PULLSEL	**GPIO55 PULLSEL** 0: Pull down 1: Pull up
22	**GPIO54**	GPIO54_PULLSEL	**GPIO54 PULLSEL** 0: Pull down 1: Pull up
21	**GPIO53**	GPIO53_PULLSEL	**GPIO53 PULLSEL** 0: Pull down 1: Pull up
20	**GPIO52**	GPIO52_PULLSEL	**GPIO52 PULLSEL** 0: Pull down 1: Pull up
12	**GPIO44**	GPIO44_PULLSEL	**GPIO44 PULLSEL** 0: Pull down 1: Pull up
11	**GPIO43**	GPIO43_PULLSEL	**GPIO43 PULLSEL** 0: Pull down 1: Pull up

A0020514 GPIO_PULLSEL GPIO Pullsel Control 00000000

1_SET

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GPIO55	GPIO54	GPIO53	GPIO52				
Type									WO	WO	WO	WO				
Reset									0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				GPIO44	GPIO43											
Type				WO	WO											
Reset				0	0											

Overview: For bitwise access of GPIO_PULLSEL1

Bit(s)	Mnemonic	Name	Description	
23	**GPIO55**	GPIO55_PULLSEL	**Bitwise SET operation of GPIO55 PULLSEL_SET** 0: 1: SET bits	Keep
22	**GPIO54**	GPIO54_PULLSEL	**Bitwise SET operation of GPIO54 PULLSEL_SET** 0: 1: SET bits	Keep
21	**GPIO53**	GPIO53_PULLSEL	**Bitwise SET operation of GPIO53 PULLSEL_SET** 0: 1: SET bits	Keep
20	**GPIO52**	GPIO52_PULLSEL	**Bitwise SET operation of GPIO52 PULLSEL_SET** 0: 1: SET bits	Keep
12	**GPIO44**	GPIO44_PULLSEL	**Bitwise SET operation of GPIO44 PULLSEL_SET** 0: 1: SET bits	Keep
11	**GPIO43**	GPIO43_PULLSEL	**Bitwise SET operation of GPIO43 PULLSEL_SET** 0: 1: SET bits	Keep

A0020518 GPIO_PULLSEL1_CLR GPIO Pullsel Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									GPIO55	GPIO54	GPIO53	GPIO52				
Type									WO	WO	WO	WO				
Reset									0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				GPIO44	GPIO43											
Type				WO	WO											
Reset				0	0											

Overview: For bitwise access of GPIO_PULLSEL1

Bit(s)	Mnemonic	Name	Description	
23	**GPIO55**	GPIO55_PULLSEL	**Bitwise CKR operation of GPIO55 PULLSEL_CLR** 0: 1: CLR bits	Keep

Bit(s)	Mnemonic	Name	Description	
22	**GPIO54**	GPIO54_PULLSEL	**Bitwise CKR operation of GPIO54 PULLSEL_CLR** 0: 1: CLR bits	Keep
21	**GPIO53**	GPIO53_PULLSEL	**Bitwise CKR operation of GPIO53 PULLSEL_CLR** 0: 1: CLR bits	Keep
20	**GPIO52**	GPIO52_PULLSEL	**Bitwise CKR operation of GPIO52 PULLSEL_CLR** 0: 1: CLR bits	Keep
12	**GPIO44**	GPIO44_PULLSEL	**Bitwise CKR operation of GPIO44 PULLSEL_CLR** 0: 1: CLR bits	Keep
11	**GPIO43**	GPIO43_PULLSEL	**Bitwise CKR operation of GPIO43 PULLSEL_CLR** 0: 1: CLR bits	Keep

A0020600 GPIO_SMT0 GPIO SMT Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: Configures GPIO Schmit trigger control

Bit(s)	Mnemonic	Name	Description	
31	**GPIO31**	GPIO31_SMT	**SMT for GPIO31** 0: 1: Enable	Disable
30	**GPIO30**	GPIO30_SMT	**SMT for GPIO30** 0: 1: Enable	Disable
29	**GPIO29**	GPIO29_SMT	**SMT for GPIO29** 0: 1: Enable	Disable
28	**GPIO28**	GPIO28_SMT	**SMT for GPIO28** 0: 1: Enable	Disable
27	**GPIO27**	GPIO27_SMT	**SMT for GPIO27** 0: 1: Enable	Disable
26	**GPIO26**	GPIO26_SMT	**SMT for GPIO26** 0: 1: Enable	Disable
25	**GPIO25**	GPIO25_SMT	**SMT for GPIO25** 0:	Disable

Bit(s)	Mnemonic	Name	Description	
			1: Enable	
24	**GPIO24**	GPIO24_SMT	**SMT for GPIO24**	
			0:	Disable
			1: Enable	
23	**GPIO23**	GPIO23_SMT	**SMT for GPIO23**	
			0:	Disable
			1: Enable	
22	**GPIO22**	GPIO22_SMT	**SMT for GPIO22**	
			0:	Disable
			1: Enable	
21	**GPIO21**	GPIO21_SMT	**SMT for GPIO21**	
			0:	Disable
			1: Enable	
20	**GPIO20**	GPIO20_SMT	**SMT for GPIO20**	
			0:	Disable
			1: Enable	
19	**GPIO19**	GPIO19_SMT	**SMT for GPIO19**	
			0:	Disable
			1: Enable	
18	**GPIO18**	GPIO18_SMT	**SMT for GPIO18**	
			0:	Disable
			1: Enable	
17	**GPIO17**	GPIO17_SMT	**SMT for GPIO17**	
			0:	Disable
			1: Enable	
16	**GPIO16**	GPIO16_SMT	**SMT for GPIO16**	
			0:	Disable
			1: Enable	
15	**GPIO15**	GPIO15_SMT	**SMT for GPIO15**	
			0:	Disable
			1: Enable	
14	**GPIO14**	GPIO14_SMT	**SMT for GPIO14**	
			0:	Disable
			1: Enable	
13	**GPIO13**	GPIO13_SMT	**SMT for GPIO13**	
			0:	Disable
			1: Enable	
12	**GPIO12**	GPIO12_SMT	**SMT for GPIO12**	
			0:	Disable
			1: Enable	
11	**GPIO11**	GPIO11_SMT	**SMT for GPIO11**	
			0:	Disable
			1: Enable	
10	**GPIO10**	GPIO10_SMT	**SMT for GPIO10**	
			0:	Disable
			1: Enable	
9	**GPIO9**	GPIO9_SMT	**SMT for GPIO9**	
			0:	Disable
			1: Enable	
8	**GPIO8**	GPIO8_SMT	**SMT for GPIO8**	
			0:	Disable
			1: Enable	

Bit(s)	Mnemonic	Name	Description	
7	**GPIO7**	GPIO7_SMT	**SMT for GPIO7** 0: 1: Enable	Disable
6	**GPIO6**	GPIO6_SMT	**SMT for GPIO6** 0: 1: Enable	Disable
5	**GPIO5**	GPIO5_SMT	**SMT for GPIO5** 0: 1: Enable	Disable
4	**GPIO4**	GPIO4_SMT	**SMT for GPIO4** 0: 1: Enable	Disable
3	**GPIO3**	GPIO3_SMT	**SMT for GPIO3** 0: 1: Enable	Disable
2	**GPIO2**	GPIO2_SMT	**SMT for GPIO2** 0: 1: Enable	Disable
1	**GPIO1**	GPIO1_SMT	**SMT for GPIO1** 0: 1: Enable	Disable
0	**GPIO0**	GPIO0_SMT	**SMT for GPIO0** 0: 1: Enable	Disable

A0020604 GPIO_SMT0_SET GPIO SMT Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_SMT0

Bit(s)	Mnemonic	Name	Description	
31	**GPIO31**	GPIO31_SMT	**Bitwise SET operation of GPIO31 SMT** 0: 1: SET bits	Keep
30	**GPIO30**	GPIO30_SMT	**Bitwise SET operation of GPIO30 SMT** 0: 1: SET bits	Keep
29	**GPIO29**	GPIO29_SMT	**Bitwise SET operation of GPIO29 SMT** 0: 1: SET bits	Keep

Bit(s)	Mnemonic	Name	Description	
28	**GPIO28**	GPIO28_SMT	**Bitwise SET operation of GPIO28 SMT** 0: 1: SET bits	Keep
27	**GPIO27**	GPIO27_SMT	**Bitwise SET operation of GPIO27 SMT** 0: 1: SET bits	Keep
26	**GPIO26**	GPIO26_SMT	**Bitwise SET operation of GPIO26 SMT** 0: 1: SET bits	Keep
25	**GPIO25**	GPIO25_SMT	**Bitwise SET operation of GPIO25 SMT** 0: 1: SET bits	Keep
24	**GPIO24**	GPIO24_SMT	**Bitwise SET operation of GPIO24 SMT** 0: 1: SET bits	Keep
23	**GPIO23**	GPIO23_SMT	**Bitwise SET operation of GPIO23 SMT** 0: 1: SET bits	Keep
22	**GPIO22**	GPIO22_SMT	**Bitwise SET operation of GPIO22 SMT** 0: 1: SET bits	Keep
21	**GPIO21**	GPIO21_SMT	**Bitwise SET operation of GPIO21 SMT** 0: 1: SET bits	Keep
20	**GPIO20**	GPIO20_SMT	**Bitwise SET operation of GPIO20 SMT** 0: 1: SET bits	Keep
19	**GPIO19**	GPIO19_SMT	**Bitwise SET operation of GPIO19 SMT** 0: 1: SET bits	Keep
18	**GPIO18**	GPIO18_SMT	**Bitwise SET operation of GPIO18 SMT** 0: 1: SET bits	Keep
17	**GPIO17**	GPIO17_SMT	**Bitwise SET operation of GPIO17 SMT** 0: 1: SET bits	Keep
16	**GPIO16**	GPIO16_SMT	**Bitwise SET operation of GPIO16 SMT** 0: 1: SET bits	Keep
15	**GPIO15**	GPIO15_SMT	**Bitwise SET operation of GPIO15 SMT** 0: 1: SET bits	Keep
14	**GPIO14**	GPIO14_SMT	**Bitwise SET operation of GPIO14 SMT** 0: 1: SET bits	Keep
13	**GPIO13**	GPIO13_SMT	**Bitwise SET operation of GPIO13 SMT** 0: 1: SET bits	Keep
12	**GPIO12**	GPIO12_SMT	**Bitwise SET operation of GPIO12 SMT** 0: 1: SET bits	Keep
11	**GPIO11**	GPIO11_SMT	**Bitwise SET operation of GPIO11 SMT**	

Bit(s)	Mnemonic	Name	Description	
			0: 1: SET bits	Keep
10	**GPIO10**	GPIO10_SMT	**Bitwise SET operation of GPIO10 SMT** 0: 1: SET bits	Keep
9	**GPIO9**	GPIO9_SMT	**Bitwise SET operation of GPIO9 SMT** 0: 1: SET bits	Keep
8	**GPIO8**	GPIO8_SMT	**Bitwise SET operation of GPIO8 SMT** 0: 1: SET bits	Keep
7	**GPIO7**	GPIO7_SMT	**Bitwise SET operation of GPIO7 SMT** 0: 1: SET bits	Keep
6	**GPIO6**	GPIO6_SMT	**Bitwise SET operation of GPIO6 SMT** 0: 1: SET bits	Keep
5	**GPIO5**	GPIO5_SMT	**Bitwise SET operation of GPIO5 SMT** 0: 1: SET bits	Keep
4	**GPIO4**	GPIO4_SMT	**Bitwise SET operation of GPIO4 SMT** 0: 1: SET bits	Keep
3	**GPIO3**	GPIO3_SMT	**Bitwise SET operation of GPIO3 SMT** 0: 1: SET bits	Keep
2	**GPIO2**	GPIO2_SMT	**Bitwise SET operation of GPIO2 SMT** 0: 1: SET bits	Keep
1	**GPIO1**	GPIO1_SMT	**Bitwise SET operation of GPIO1 SMT** 0: 1: SET bits	Keep
0	**GPIO0**	GPIO0_SMT	**Bitwise SET operation of GPIO0 SMT** 0: 1: SET bits	Keep

A0020608 **GPIO_SMT0_CLR** **GPIO SMT Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_SMT0

Bit(s)	Mnemonic	Name	Description	
31	**GPIO31**	GPIO31_SMT	**Bitwise CLR operation of GPIO31 SMT** 0: 1: CLR bits	Keep
30	**GPIO30**	GPIO30_SMT	**Bitwise CLR operation of GPIO30 SMT** 0: 1: CLR bits	Keep
29	**GPIO29**	GPIO29_SMT	**Bitwise CLR operation of GPIO29 SMT** 0: 1: CLR bits	Keep
28	**GPIO28**	GPIO28_SMT	**Bitwise CLR operation of GPIO28 SMT** 0: 1: CLR bits	Keep
27	**GPIO27**	GPIO27_SMT	**Bitwise CLR operation of GPIO27 SMT** 0: 1: CLR bits	Keep
26	**GPIO26**	GPIO26_SMT	**Bitwise CLR operation of GPIO26 SMT** 0: 1: CLR bits	Keep
25	**GPIO25**	GPIO25_SMT	**Bitwise CLR operation of GPIO25 SMT** 0: 1: CLR bits	Keep
24	**GPIO24**	GPIO24_SMT	**Bitwise CLR operation of GPIO24 SMT** 0: 1: CLR bits	Keep
23	**GPIO23**	GPIO23_SMT	**Bitwise CLR operation of GPIO23 SMT** 0: 1: CLR bits	Keep
22	**GPIO22**	GPIO22_SMT	**Bitwise CLR operation of GPIO22 SMT** 0: 1: CLR bits	Keep
21	**GPIO21**	GPIO21_SMT	**Bitwise CLR operation of GPIO21 SMT** 0: 1: CLR bits	Keep
20	**GPIO20**	GPIO20_SMT	**Bitwise CLR operation of GPIO20 SMT** 0: 1: CLR bits	Keep
19	**GPIO19**	GPIO19_SMT	**Bitwise CLR operation of GPIO19 SMT** 0: 1: CLR bits	Keep
18	**GPIO18**	GPIO18_SMT	**Bitwise CLR operation of GPIO18 SMT** 0: 1: CLR bits	Keep
17	**GPIO17**	GPIO17_SMT	**Bitwise CLR operation of GPIO17 SMT** 0: 1: CLR bits	Keep
16	**GPIO16**	GPIO16_SMT	**Bitwise CLR operation of GPIO16 SMT** 0: 1: CLR bits	Keep
15	**GPIO15**	GPIO15_SMT	**Bitwise CLR operation of GPIO15 SMT** 0: 1: CLR bits	Keep
14	**GPIO14**	GPIO14_SMT	**Bitwise CLR operation of GPIO14 SMT**	

Bit(s)	Mnemonic	Name	Description	
			0: 1: CLR bits	Keep
13	**GPIO13**	GPIO13_SMT	**Bitwise CLR operation of GPIO13 SMT** 0: 1: CLR bits	Keep
12	**GPIO12**	GPIO12_SMT	**Bitwise CLR operation of GPIO12 SMT** 0: 1: CLR bits	Keep
11	**GPIO11**	GPIO11_SMT	**Bitwise CLR operation of GPIO11 SMT** 0: 1: CLR bits	Keep
10	**GPIO10**	GPIO10_SMT	**Bitwise CLR operation of GPIO10 SMT** 0: 1: CLR bits	Keep
9	**GPIO9**	GPIO9_SMT	**Bitwise CLR operation of GPIO9 SMT** 0: 1: CLR bits	Keep
8	**GPIO8**	GPIO8_SMT	**Bitwise CLR operation of GPIO8 SMT** 0: 1: CLR bits	Keep
7	**GPIO7**	GPIO7_SMT	**Bitwise CLR operation of GPIO7 SMT** 0: 1: CLR bits	Keep
6	**GPIO6**	GPIO6_SMT	**Bitwise CLR operation of GPIO6 SMT** 0: 1: CLR bits	Keep
5	**GPIO5**	GPIO5_SMT	**Bitwise CLR operation of GPIO5 SMT** 0: 1: CLR bits	Keep
4	**GPIO4**	GPIO4_SMT	**Bitwise CLR operation of GPIO4 SMT** 0: 1: CLR bits	Keep
3	**GPIO3**	GPIO3_SMT	**Bitwise CLR operation of GPIO3 SMT** 0: 1: CLR bits	Keep
2	**GPIO2**	GPIO2_SMT	**Bitwise CLR operation of GPIO2 SMT** 0: 1: CLR bits	Keep
1	**GPIO1**	GPIO1_SMT	**Bitwise CLR operation of GPIO1 SMT** 0: 1: CLR bits	Keep
0	**GPIO0**	GPIO0_SMT	**Bitwise CLR operation of GPIO0 SMT** 0: 1: CLR bits	Keep

A0020610 GPIO_SMT1 GPIO SMT Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GPIO51	GPIO50	GPIO49	GPIO48
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: Configures GPIO Schmit trigger control

Bit(s)	Mnemonic	Name	Description
19	**GPIO51**	GPIO51_SMT	**SMT for GPIO51** 0: Disable 1: Enable
18	**GPIO50**	GPIO50_SMT	**SMT for GPIO50** 0: Disable 1: Enable
17	**GPIO49**	GPIO49_SMT	**SMT for GPIO49** 0: Disable 1: Enable
16	**GPIO48**	GPIO48_SMT	**SMT for GPIO48** 0: Disable 1: Enable
15	**GPIO47**	GPIO47_SMT	**SMT for GPIO47** 0: Disable 1: Enable
14	**GPIO46**	GPIO46_SMT	**SMT for GPIO46** 0: Disable 1: Enable
13	**GPIO45**	GPIO45_SMT	**SMT for GPIO45** 0: Disable 1: Enable
12	**GPIO44**	GPIO44_SMT	**SMT for GPIO44** 0: Disable 1: Enable
11	**GPIO43**	GPIO43_SMT	**SMT for GPIO43** 0: Disable 1: Enable
10	**GPIO42**	GPIO42_SMT	**SMT for GPIO42** 0: Disable 1: Enable
9	**GPIO41**	GPIO41_SMT	**SMT for GPIO41** 0: Disable 1: Enable
8	**GPIO40**	GPIO40_SMT	**SMT for GPIO40** 0: Disable 1: Enable
7	**GPIO39**	GPIO39_SMT	**SMT for GPIO39** 0: Disable 1: Enable
6	**GPIO38**	GPIO38_SMT	**SMT for GPIO38** 0: Disable 1: Enable
5	**GPIO37**	GPIO37_SMT	**SMT for GPIO37** 0: Disable

Bit(s)	Mnemonic	Name	Description	
			1: Enable	
4	**GPIO36**	GPIO36_SMT	**SMT for GPIO36** 0: Disable 1: Enable	
3	**GPIO35**	GPIO35_SMT	**SMT for GPIO35** 0: Disable 1: Enable	
2	**GPIO34**	GPIO34_SMT	**SMT for GPIO34** 0: Disable 1: Enable	
1	**GPIO33**	GPIO33_SMT	**SMT for GPIO33** 0: Disable 1: Enable	
0	**GPIO32**	GPIO32_SMT	**SMT for GPIO32** 0: Disable 1: Enable	

A0020614 GPIO_SMT1_SET GPIO SMT Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GPIO51	GPIO50	GPIO49	GPIO48
Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_SMT1

Bit(s)	Mnemonic	Name	Description	
19	**GPIO51**	GPIO51_SMT	**Bitwise SET operation of GPIO51 SMT** 0: Keep 1: SET bits	
18	**GPIO50**	GPIO50_SMT	**Bitwise SET operation of GPIO50 SMT** 0: Keep 1: SET bits	
17	**GPIO49**	GPIO49_SMT	**Bitwise SET operation of GPIO49 SMT** 0: Keep 1: SET bits	
16	**GPIO48**	GPIO48_SMT	**Bitwise SET operation of GPIO48 SMT** 0: Keep 1: SET bits	
15	**GPIO47**	GPIO47_SMT	**Bitwise SET operation of GPIO47 SMT** 0: Keep 1: SET bits	
14	**GPIO46**	GPIO46_SMT	**Bitwise SET operation of GPIO46 SMT** 0: Keep 1: SET bits	

Bit(s)	Mnemonic	Name	Description	
13	**GPIO45**	GPIO45_SMT	**Bitwise SET operation of GPIO45 SMT** 0: 1: SET bits	Keep
12	**GPIO44**	GPIO44_SMT	**Bitwise SET operation of GPIO44 SMT** 0: 1: SET bits	Keep
11	**GPIO43**	GPIO43_SMT	**Bitwise SET operation of GPIO43 SMT** 0: 1: SET bits	Keep
10	**GPIO42**	GPIO42_SMT	**Bitwise SET operation of GPIO42 SMT** 0: 1: SET bits	Keep
9	**GPIO41**	GPIO41_SMT	**Bitwise SET operation of GPIO41 SMT** 0: 1: SET bits	Keep
8	**GPIO40**	GPIO40_SMT	**Bitwise SET operation of GPIO40 SMT** 0: 1: SET bits	Keep
7	**GPIO39**	GPIO39_SMT	**Bitwise SET operation of GPIO39 SMT** 0: 1: SET bits	Keep
6	**GPIO38**	GPIO38_SMT	**Bitwise SET operation of GPIO38 SMT** 0: 1: SET bits	Keep
5	**GPIO37**	GPIO37_SMT	**Bitwise SET operation of GPIO37 SMT** 0: 1: SET bits	Keep
4	**GPIO36**	GPIO36_SMT	**Bitwise SET operation of GPIO36 SMT** 0: 1: SET bits	Keep
3	**GPIO35**	GPIO35_SMT	**Bitwise SET operation of GPIO35 SMT** 0: 1: SET bits	Keep
2	**GPIO34**	GPIO34_SMT	**Bitwise SET operation of GPIO34 SMT** 0: 1: SET bits	Keep
1	**GPIO33**	GPIO33_SMT	**Bitwise SET operation of GPIO33 SMT** 0: 1: SET bits	Keep
0	**GPIO32**	GPIO32_SMT	**Bitwise SET operation of GPIO32 SMT** 0: 1: SET bits	Keep

A0020618 GPIO_SMT1_CLR GPIO SMT Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GPIO51	GPIO50	GPIO49	GPIO48
Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_SMT1

Bit(s)	Mnemonic	Name	Description
19	**GPIO51**	GPIO51_SMT	**Bitwise CLR operation of GPIO51 SMT** 0: Keep 1: CLR bits
18	**GPIO50**	GPIO50_SMT	**Bitwise CLR operation of GPIO50 SMT** 0: Keep 1: CLR bits
17	**GPIO49**	GPIO49_SMT	**Bitwise CLR operation of GPIO49 SMT** 0: Keep 1: CLR bits
16	**GPIO48**	GPIO48_SMT	**Bitwise CLR operation of GPIO48 SMT** 0: Keep 1: CLR bits
15	**GPIO47**	GPIO47_SMT	**Bitwise CLR operation of GPIO47 SMT** 0: Keep 1: CLR bits
14	**GPIO46**	GPIO46_SMT	**Bitwise CLR operation of GPIO46 SMT** 0: Keep 1: CLR bits
13	**GPIO45**	GPIO45_SMT	**Bitwise CLR operation of GPIO45 SMT** 0: Keep 1: CLR bits
12	**GPIO44**	GPIO44_SMT	**Bitwise CLR operation of GPIO44 SMT** 0: Keep 1: CLR bits
11	**GPIO43**	GPIO43_SMT	**Bitwise CLR operation of GPIO43 SMT** 0: Keep 1: CLR bits
10	**GPIO42**	GPIO42_SMT	**Bitwise CLR operation of GPIO42 SMT** 0: Keep 1: CLR bits
9	**GPIO41**	GPIO41_SMT	**Bitwise CLR operation of GPIO41 SMT** 0: Keep 1: CLR bits
8	**GPIO40**	GPIO40_SMT	**Bitwise CLR operation of GPIO40 SMT** 0: Keep 1: CLR bits
7	**GPIO39**	GPIO39_SMT	**Bitwise CLR operation of GPIO39 SMT** 0: Keep 1: CLR bits
6	**GPIO38**	GPIO38_SMT	**Bitwise CLR operation of GPIO38 SMT** 0: Keep 1: CLR bits
5	**GPIO37**	GPIO37_SMT	**Bitwise CLR operation of GPIO37 SMT** 0: Keep 1: CLR bits

Bit(s)	Mnemonic	Name	Description	
4	**GPIO36**	GPIO36_SMT	**Bitwise CLR operation of GPIO36 SMT** 0: 1: CLR bits	Keep
3	**GPIO35**	GPIO35_SMT	**Bitwise CLR operation of GPIO35 SMT** 0: 1: CLR bits	Keep
2	**GPIO34**	GPIO34_SMT	**Bitwise CLR operation of GPIO34 SMT** 0: 1: CLR bits	Keep
1	**GPIO33**	GPIO33_SMT	**Bitwise CLR operation of GPIO33 SMT** 0: 1: CLR bits	Keep
0	**GPIO32**	GPIO32_SMT	**Bitwise CLR operation of GPIO32 SMT** 0: 1: CLR bits	Keep

A0020700 GPIO_SR0 GPIO SR Control FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Overview: Configures GPIO slew rate control

Bit(s)	Mnemonic	Name	Description	
31	**GPIO31**	GPIO31_SR	**SR for GPIO31** 0: 1: Enable	Disable
30	**GPIO30**	GPIO30_SR	**SR for GPIO30** 0: 1: Enable	Disable
29	**GPIO29**	GPIO29_SR	**SR for GPIO29** 0: 1: Enable	Disable
28	**GPIO28**	GPIO28_SR	**SR for GPIO28** 0: 1: Enable	Disable
27	**GPIO27**	GPIO27_SR	**SR for GPIO27** 0: 1: Enable	Disable
26	**GPIO26**	GPIO26_SR	**SR for GPIO26** 0: 1: Enable	Disable
25	**GPIO25**	GPIO25_SR	**SR for GPIO25** 0:	Disable

Bit(s)	Mnemonic	Name	Description	
			1: Enable	
24	**GPIO24**	GPIO24_SR	**SR for GPIO24**	
			0:	Disable
			1: Enable	
23	**GPIO23**	GPIO23_SR	**SR for GPIO23**	
			0:	Disable
			1: Enable	
22	**GPIO22**	GPIO22_SR	**SR for GPIO22**	
			0:	Disable
			1: Enable	
21	**GPIO21**	GPIO21_SR	**SR for GPIO21**	
			0:	Disable
			1: Enable	
20	**GPIO20**	GPIO20_SR	**SR for GPIO20**	
			0:	Disable
			1: Enable	
19	**GPIO19**	GPIO19_SR	**SR for GPIO19**	
			0:	Disable
			1: Enable	
18	**GPIO18**	GPIO18_SR	**SR for GPIO18**	
			0:	Disable
			1: Enable	
17	**GPIO17**	GPIO17_SR	**SR for GPIO17**	
			0:	Disable
			1: Enable	
16	**GPIO16**	GPIO16_SR	**SR for GPIO16**	
			0:	Disable
			1: Enable	
15	**GPIO15**	GPIO15_SR	**SR for GPIO15**	
			0:	Disable
			1: Enable	
14	**GPIO14**	GPIO14_SR	**SR for GPIO14**	
			0:	Disable
			1: Enable	
13	**GPIO13**	GPIO13_SR	**SR for GPIO13**	
			0:	Disable
			1: Enable	
12	**GPIO12**	GPIO12_SR	**SR for GPIO12**	
			0:	Disable
			1: Enable	
11	**GPIO11**	GPIO11_SR	**SR for GPIO11**	
			0:	Disable
			1: Enable	
10	**GPIO10**	GPIO10_SR	**SR for GPIO10**	
			0:	Disable
			1: Enable	
9	**GPIO9**	GPIO9_SR	**SR for GPIO9**	
			0:	Disable
			1: Enable	
8	**GPIO8**	GPIO8_SR	**SR for GPIO8**	
			0:	Disable
			1: Enable	

Bit(s)	Mnemonic	Name	Description	
7	**GPIO7**	GPIO7_SR	**SR for GPIO7** 0: 1: Enable	Disable
6	**GPIO6**	GPIO6_SR	**SR for GPIO6** 0: 1: Enable	Disable
5	**GPIO5**	GPIO5_SR	**SR for GPIO5** 0: 1: Enable	Disable
4	**GPIO4**	GPIO4_SR	**SR for GPIO4** 0: 1: Enable	Disable
3	**GPIO3**	GPIO3_SR	**SR for GPIO3** 0: 1: Enable	Disable
2	**GPIO2**	GPIO2_SR	**SR for GPIO2** 0: 1: Enable	Disable
1	**GPIO1**	GPIO1_SR	**SR for GPIO1** 0: 1: Enable	Disable
0	**GPIO0**	GPIO0_SR	**SR for GPIO0** 0: 1: Enable	Disable

A0020704 GPIO_SR0_SET GPIO SR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**GPIO31**	**GPIO30**	**GPIO29**	**GPIO28**	**GPIO27**	**GPIO26**	**GPIO25**	**GPIO24**	**GPIO23**	**GPIO22**	**GPIO21**	**GPIO20**	**GPIO19**	**GPIO18**	**GPIO17**	**GPIO16**
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GPIO15**	**GPIO14**	**GPIO13**	**GPIO12**	**GPIO11**	**GPIO10**	**GPIO9**	**GPIO8**	**GPIO7**	**GPIO6**	**GPIO5**	**GPIO4**	**GPIO3**	**GPIO2**	**GPIO1**	**GPIO0**
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_SR0

Bit(s)	Mnemonic	Name	Description	
31	**GPIO31**	GPIO31_SR	**Bitwise SET operation of GPIO31 SR** 0: 1: SET bits	Keep
30	**GPIO30**	GPIO30_SR	**Bitwise SET operation of GPIO30 SR** 0: 1: SET bits	Keep
29	**GPIO29**	GPIO29_SR	**Bitwise SET operation of GPIO29 SR** 0: 1: SET bits	Keep
28	**GPIO28**	GPIO28_SR	**Bitwise SET operation of GPIO28 SR** 0:	Keep

Bit(s)	Mnemonic	Name	Description	
			1: SET bits	
27	**GPIO27**	GPIO27_SR	**Bitwise SET operation of GPIO27 SR**	
			0: 1: SET bits	Keep
26	**GPIO26**	GPIO26_SR	**Bitwise SET operation of GPIO26 SR**	
			0: 1: SET bits	Keep
25	**GPIO25**	GPIO25_SR	**Bitwise SET operation of GPIO25 SR**	
			0: 1: SET bits	Keep
24	**GPIO24**	GPIO24_SR	**Bitwise SET operation of GPIO24 SR**	
			0: 1: SET bits	Keep
23	**GPIO23**	GPIO23_SR	**Bitwise SET operation of GPIO23 SR**	
			0: 1: SET bits	Keep
22	**GPIO22**	GPIO22_SR	**Bitwise SET operation of GPIO22 SR**	
			0: 1: SET bits	Keep
21	**GPIO21**	GPIO21_SR	**Bitwise SET operation of GPIO21 SR**	
			0: 1: SET bits	Keep
20	**GPIO20**	GPIO20_SR	**Bitwise SET operation of GPIO20 SR**	
			0: 1: SET bits	Keep
19	**GPIO19**	GPIO19_SR	**Bitwise SET operation of GPIO19 SR**	
			0: 1: SET bits	Keep
18	**GPIO18**	GPIO18_SR	**Bitwise SET operation of GPIO18 SR**	
			0: 1: SET bits	Keep
17	**GPIO17**	GPIO17_SR	**Bitwise SET operation of GPIO17 SR**	
			0: 1: SET bits	Keep
16	**GPIO16**	GPIO16_SR	**Bitwise SET operation of GPIO16 SR**	
			0: 1: SET bits	Keep
15	**GPIO15**	GPIO15_SR	**Bitwise SET operation of GPIO15 SR**	
			0: 1: SET bits	Keep
14	**GPIO14**	GPIO14_SR	**Bitwise SET operation of GPIO14 SR**	
			0: 1: SET bits	Keep
13	**GPIO13**	GPIO13_SR	**Bitwise SET operation of GPIO13 SR**	
			0: 1: SET bits	Keep
12	**GPIO12**	GPIO12_SR	**Bitwise SET operation of GPIO12 SR**	
			0: 1: SET bits	Keep
11	**GPIO11**	GPIO11_SR	**Bitwise SET operation of GPIO11 SR**	
			0: 1: SET bits	Keep

Bit(s)	Mnemonic	Name	Description	
10	**GPIO10**	GPIO10_SR	**Bitwise SET operation of GPIO10 SR** 0: 1: SET bits	Keep
9	**GPIO9**	GPIO9_SR	**Bitwise SET operation of GPIO9 SR** 0: 1: SET bits	Keep
8	**GPIO8**	GPIO8_SR	**Bitwise SET operation of GPIO8 SR** 0: 1: SET bits	Keep
7	**GPIO7**	GPIO7_SR	**Bitwise SET operation of GPIO7 SR** 0: 1: SET bits	Keep
6	**GPIO6**	GPIO6_SR	**Bitwise SET operation of GPIO6 SR** 0: 1: SET bits	Keep
5	**GPIO5**	GPIO5_SR	**Bitwise SET operation of GPIO5 SR** 0: 1: SET bits	Keep
4	**GPIO4**	GPIO4_SR	**Bitwise SET operation of GPIO4 SR** 0: 1: SET bits	Keep
3	**GPIO3**	GPIO3_SR	**Bitwise SET operation of GPIO3 SR** 0: 1: SET bits	Keep
2	**GPIO2**	GPIO2_SR	**Bitwise SET operation of GPIO2 SR** 0: 1: SET bits	Keep
1	**GPIO1**	GPIO1_SR	**Bitwise SET operation of GPIO1 SR** 0: 1: SET bits	Keep
0	**GPIO0**	GPIO0_SR	**Bitwise SET operation of GPIO0 SR** 0: 1: SET bits	Keep

A0020708 GPIO_SR0_CLR GPIO SR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31	GPIO30	GPIO29	GPIO28	GPIO27	GPIO26	GPIO25	GPIO24	GPIO23	GPIO22	GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12	GPIO11	GPIO10	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_SR0

Bit(s)	Mnemonic	Name	Description	
31	**GPIO31**	GPIO31_SR	**Bitwise CLR operation of GPIO31 SR** 0:	Keep

Bit(s)	Mnemonic	Name	Description	
			1: CLR bits	
30	**GPIO30**	GPIO30_SR	**Bitwise CLR operation of GPIO30 SR**	
			0: 1: CLR bits	Keep
29	**GPIO29**	GPIO29_SR	**Bitwise CLR operation of GPIO29 SR**	
			0: 1: CLR bits	Keep
28	**GPIO28**	GPIO28_SR	**Bitwise CLR operation of GPIO28 SR**	
			0: 1: CLR bits	Keep
27	**GPIO27**	GPIO27_SR	**Bitwise CLR operation of GPIO27 SR**	
			0: 1: CLR bits	Keep
26	**GPIO26**	GPIO26_SR	**Bitwise CLR operation of GPIO26 SR**	
			0: 1: CLR bits	Keep
25	**GPIO25**	GPIO25_SR	**Bitwise CLR operation of GPIO25 SR**	
			0: 1: CLR bits	Keep
24	**GPIO24**	GPIO24_SR	**Bitwise CLR operation of GPIO24 SR**	
			0: 1: CLR bits	Keep
23	**GPIO23**	GPIO23_SR	**Bitwise CLR operation of GPIO23 SR**	
			0: 1: CLR bits	Keep
22	**GPIO22**	GPIO22_SR	**Bitwise CLR operation of GPIO22 SR**	
			0: 1: CLR bits	Keep
21	**GPIO21**	GPIO21_SR	**Bitwise CLR operation of GPIO21 SR**	
			0: 1: CLR bits	Keep
20	**GPIO20**	GPIO20_SR	**Bitwise CLR operation of GPIO20 SR**	
			0: 1: CLR bits	Keep
19	**GPIO19**	GPIO19_SR	**Bitwise CLR operation of GPIO19 SR**	
			0: 1: CLR bits	Keep
18	**GPIO18**	GPIO18_SR	**Bitwise CLR operation of GPIO18 SR**	
			0: 1: CLR bits	Keep
17	**GPIO17**	GPIO17_SR	**Bitwise CLR operation of GPIO17 SR**	
			0: 1: CLR bits	Keep
16	**GPIO16**	GPIO16_SR	**Bitwise CLR operation of GPIO16 SR**	
			0: 1: CLR bits	Keep
15	**GPIO15**	GPIO15_SR	**Bitwise CLR operation of GPIO15 SR**	
			0: 1: CLR bits	Keep
14	**GPIO14**	GPIO14_SR	**Bitwise CLR operation of GPIO14 SR**	
			0: 1: CLR bits	Keep

Bit(s)	Mnemonic	Name	Description	
13	**GPIO13**	GPIO13_SR	**Bitwise CLR operation of GPIO13 SR** 0: 1: CLR bits	Keep
12	**GPIO12**	GPIO12_SR	**Bitwise CLR operation of GPIO12 SR** 0: 1: CLR bits	Keep
11	**GPIO11**	GPIO11_SR	**Bitwise CLR operation of GPIO11 SR** 0: 1: CLR bits	Keep
10	**GPIO10**	GPIO10_SR	**Bitwise CLR operation of GPIO10 SR** 0: 1: CLR bits	Keep
9	**GPIO9**	GPIO9_SR	**Bitwise CLR operation of GPIO9 SR** 0: 1: CLR bits	Keep
8	**GPIO8**	GPIO8_SR	**Bitwise CLR operation of GPIO8 SR** 0: 1: CLR bits	Keep
7	**GPIO7**	GPIO7_SR	**Bitwise CLR operation of GPIO7 SR** 0: 1: CLR bits	Keep
6	**GPIO6**	GPIO6_SR	**Bitwise CLR operation of GPIO6 SR** 0: 1: CLR bits	Keep
5	**GPIO5**	GPIO5_SR	**Bitwise CLR operation of GPIO5 SR** 0: 1: CLR bits	Keep
4	**GPIO4**	GPIO4_SR	**Bitwise CLR operation of GPIO4 SR** 0: 1: CLR bits	Keep
3	**GPIO3**	GPIO3_SR	**Bitwise CLR operation of GPIO3 SR** 0: 1: CLR bits	Keep
2	**GPIO2**	GPIO2_SR	**Bitwise CLR operation of GPIO2 SR** 0: 1: CLR bits	Keep
1	**GPIO1**	GPIO1_SR	**Bitwise CLR operation of GPIO1 SR** 0: 1: CLR bits	Keep
0	**GPIO0**	GPIO0_SR	**Bitwise CLR operation of GPIO0 SR** 0: 1: CLR bits	Keep

A0020710 GPIO_SR1 GPIO SR Control 000FF81F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GPIO51	GPIO50	GPIO49	GPIO48
Type													RW	RW	RW	RW
Reset													1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43							GPIO36	GPIO35	GPIO34	GPIO33	GPIO32

	7	6	5	4	3							6	5	4	3	2
Type	RW	RW	RW	RW	RW							RW	RW	RW	RW	RW
Reset	1	1	1	1	1							1	1	1	1	1

Overview: Configures GPIO slew rate control

Bit(s)	Mnemonic	Name	Description	
19	**GPIO51**	GPIO51_SR	**SR for GPIO51** 0: 1: Enable	Disable
18	**GPIO50**	GPIO50_SR	**SR for GPIO50** 0: 1: Enable	Disable
17	**GPIO49**	GPIO49_SR	**SR for GPIO49** 0: 1: Enable	Disable
16	**GPIO48**	GPIO48_SR	**SR for GPIO48** 0: 1: Enable	Disable
15	**GPIO47**	GPIO47_SR	**SR for GPIO47** 0: 1: Enable	Disable
14	**GPIO46**	GPIO46_SR	**SR for GPIO46** 0: 1: Enable	Disable
13	**GPIO45**	GPIO45_SR	**SR for GPIO45** 0: 1: Enable	Disable
12	**GPIO44**	GPIO44_SR	**SR for GPIO44** 0: 1: Enable	Disable
11	**GPIO43**	GPIO43_SR	**SR for GPIO43** 0: 1: Enable	Disable
4	**GPIO36**	GPIO36_SR	**SR for GPIO36** 0: 1: Enable	Disable
3	**GPIO35**	GPIO35_SR	**SR for GPIO35** 0: 1: Enable	Disable
2	**GPIO34**	GPIO34_SR	**SR for GPIO34** 0: 1: Enable	Disable
1	**GPIO33**	GPIO33_SR	**SR for GPIO33** 0: 1: Enable	Disable
0	**GPIO32**	GPIO32_SR	**SR for GPIO32** 0: 1: Enable	Disable

A0020714 GPIO_SR1_SET GPIO SR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GPIO51	GPIO50	GPIO49	GPIO48
Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45	GPIO44	GPIO43							GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	WO	WO	WO	WO	WO							WO	WO	WO	WO	WO
Reset	0	0	0	0	0							0	0	0	0	0

Overview: For bitwise access of GPIO_SR1

Bit(s)	Mnemonic	Name	Description	
19	**GPIO51**	GPIO51_SR	**Bitwise SET operation of GPIO51 SR** 0: 1: SET bits	Keep
18	**GPIO50**	GPIO50_SR	**Bitwise SET operation of GPIO50 SR** 0: 1: SET bits	Keep
17	**GPIO49**	GPIO49_SR	**Bitwise SET operation of GPIO49 SR** 0: 1: SET bits	Keep
16	**GPIO48**	GPIO48_SR	**Bitwise SET operation of GPIO48 SR** 0: 1: SET bits	Keep
15	**GPIO47**	GPIO47_SR	**Bitwise SET operation of GPIO47 SR** 0: 1: SET bits	Keep
14	**GPIO46**	GPIO46_SR	**Bitwise SET operation of GPIO46 SR** 0: 1: SET bits	Keep
13	**GPIO45**	GPIO45_SR	**Bitwise SET operation of GPIO45 SR** 0: 1: SET bits	Keep
12	**GPIO44**	GPIO44_SR	**Bitwise SET operation of GPIO44 SR** 0: 1: SET bits	Keep
11	**GPIO43**	GPIO43_SR	**Bitwise SET operation of GPIO43 SR** 0: 1: SET bits	Keep
4	**GPIO36**	GPIO36_SR	**Bitwise SET operation of GPIO36 SR** 0: 1: SET bits	Keep
3	**GPIO35**	GPIO35_SR	**Bitwise SET operation of GPIO35 SR** 0: 1: SET bits	Keep
2	**GPIO34**	GPIO34_SR	**Bitwise SET operation of GPIO34 SR** 0: 1: SET bits	Keep
1	**GPIO33**	GPIO33_SR	**Bitwise SET operation of GPIO33 SR** 0:	Keep

Bit(s)	Mnemonic	Name	Description	
			1: SET bits	
0	**GPIO32**	GPIO32_SR	**Bitwise SET operation of GPIO32 SR** 0: 1: SET bits	Keep

A0020718 GPIO_SR1_CLR GPIO SR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**GPIO51**	**GPIO50**	**GPIO49**	**GPIO48**
Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GPIO47**	**GPIO46**	**GPIO45**	**GPIO44**	**GPIO43**							**GPIO36**	**GPIO35**	**GPIO34**	**GPIO33**	**GPIO32**
Type	WO	WO	WO	WO	WO							WO	WO	WO	WO	WO
Reset	0	0	0	0	0							0	0	0	0	0

Overview: For bitwise access of GPIO_SR1

Bit(s)	Mnemonic	Name	Description	
19	**GPIO51**	GPIO51_SR	**Bitwise CLR operation of GPIO51 SR** 0: 1: CLR bits	Keep
18	**GPIO50**	GPIO50_SR	**Bitwise CLR operation of GPIO50 SR** 0: 1: CLR bits	Keep
17	**GPIO49**	GPIO49_SR	**Bitwise CLR operation of GPIO49 SR** 0: 1: CLR bits	Keep
16	**GPIO48**	GPIO48_SR	**Bitwise CLR operation of GPIO48 SR** 0: 1: CLR bits	Keep
15	**GPIO47**	GPIO47_SR	**Bitwise CLR operation of GPIO47 SR** 0: 1: CLR bits	Keep
14	**GPIO46**	GPIO46_SR	**Bitwise CLR operation of GPIO46 SR** 0: 1: CLR bits	Keep
13	**GPIO45**	GPIO45_SR	**Bitwise CLR operation of GPIO45 SR** 0: 1: CLR bits	Keep
12	**GPIO44**	GPIO44_SR	**Bitwise CLR operation of GPIO44 SR** 0: 1: CLR bits	Keep
11	**GPIO43**	GPIO43_SR	**Bitwise CLR operation of GPIO43 SR** 0: 1: CLR bits	Keep
4	**GPIO36**	GPIO36_SR	**Bitwise CLR operation of GPIO36 SR** 0: 1: CLR bits	Keep

Bit(s)	Mnemonic	Name	Description	
3	**GPIO35**	GPIO35_SR	**Bitwise CLR operation of GPIO35 SR** 0: 1: CLR bits	Keep
2	**GPIO34**	GPIO34_SR	**Bitwise CLR operation of GPIO34 SR** 0: 1: CLR bits	Keep
1	**GPIO33**	GPIO33_SR	**Bitwise CLR operation of GPIO33 SR** 0: 1: CLR bits	Keep
0	**GPIO32**	GPIO32_SR	**Bitwise CLR operation of GPIO32 SR** 0: 1: CLR bits	Keep

A0020720 GPIO_SIM_SR GPIO SIM SR Control 003F003F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37
Type											RW	RW	RW	RW	RW	RW
Reset											1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37
Type											RW	RW	RW	RW	RW	RW
Reset											1	1	1	1	1	1

Overview: Configures GPIO slew rate control for SIM IO

Bit(s)	Mnemonic	Name	Description	
21	**GPIO42**	GPIO42_SR1	**SR1 control for GPIO42** 0: 1: Enable	Disable
20	**GPIO41**	GPIO41_SR1	**SR1 control for GPIO41** 0: 1: Enable	Disable
19	**GPIO40**	GPIO40_SR1	**SR1 control for GPIO40** 0: 1: Enable	Disable
18	**GPIO39**	GPIO39_SR1	**SR1 control for GPIO39** 0: 1: Enable	Disable
17	**GPIO38**	GPIO38_SR1	**SR1 control for GPIO38** 0: 1: Enable	Disable
16	**GPIO37**	GPIO37_SR1	**SR1 control for GPIO37** 0: 1: Enable	Disable
5	**GPIO42**	GPIO42_SR0	**SR0 control for GPIO42** 0: 1: Enable	Disable
4	**GPIO41**	GPIO41_SR0	**SR0 control for GPIO41** 0:	Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
3	**GPIO40**	GPIO40_SR0	**SR0 control for GPIO40** 0: Disable 1: Enable
2	**GPIO39**	GPIO39_SR0	**SR0 control for GPIO39** 0: Disable 1: Enable
1	**GPIO38**	GPIO38_SR0	**SR0 control for GPIO38** 0: Disable 1: Enable
0	**GPIO37**	GPIO37_SR0	**SR0 control for GPIO37** 0: Disable 1: Enable

A0020724 GPIO_SIM_SR_SET GPIO SIM SR Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37
Type											WO	WO	WO	WO	WO	WO
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37
Type											WO	WO	WO	WO	WO	WO
Reset											0	0	0	0	0	0

Overview: For bitwise access of GPIO_SIM_SR

Bit(s)	Mnemonic	Name	Description
21	**GPIO42**	GPIO42_SR1	**Bitwise SET operation of GPIO42 SR1 control** 0: Keep 1: SET bits
20	**GPIO41**	GPIO41_SR1	**Bitwise SET operation of GPIO41 SR1 control** 0: Keep 1: SET bits
19	**GPIO40**	GPIO40_SR1	**Bitwise SET operation of GPIO40 SR1 control** 0: Keep 1: SET bits
18	**GPIO39**	GPIO39_SR1	**Bitwise SET operation of GPIO39 SR1 control** 0: Keep 1: SET bits
17	**GPIO38**	GPIO38_SR1	**Bitwise SET operation of GPIO38 SR1 control** 0: Keep 1: SET bits
16	**GPIO37**	GPIO37_SR1	**Bitwise SET operation of GPIO37 SR1 control** 0: Keep 1: SET bits
5	**GPIO42**	GPIO42_SR0	**Bitwise SET operation of GPIO42 SR0 control** 0: Keep 1: SET bits

Bit(s)	Mnemonic	Name	Description	
4	**GPIO41**	GPIO41_SR0	**Bitwise SET operation of GPIO41 SR0 control** 0: 1: SET bits	Keep
3	**GPIO40**	GPIO40_SR0	**Bitwise SET operation of GPIO40 SR0 control** 0: 1: SET bits	Keep
2	**GPIO39**	GPIO39_SR0	**Bitwise SET operation of GPIO39 SR0 control** 0: 1: SET bits	Keep
1	**GPIO38**	GPIO38_SR0	**Bitwise SET operation of GPIO38 SR0 control** 0: 1: SET bits	Keep
0	**GPIO37**	GPIO37_SR0	**Bitwise SET operation of GPIO37 SR0 control** 0: 1: SET bits	Keep

A0020728 **GPIO_SIM_SR_CLR** **GPIO SIM SR Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											**GPIO42**	**GPIO41**	**GPIO40**	**GPIO39**	**GPIO38**	**GPIO37**
Type											WO	WO	WO	WO	WO	WO
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											**GPIO42**	**GPIO41**	**GPIO40**	**GPIO39**	**GPIO38**	**GPIO37**
Type											WO	WO	WO	WO	WO	WO
Reset											0	0	0	0	0	0

Overview: For bitwise access of GPIO_SIM_SR

Bit(s)	Mnemonic	Name	Description	
21	**GPIO42**	GPIO42_SR1	**Bitwise CLR operation of GPIO42 SR1 control** 0: 1: CLR bits	Keep
20	**GPIO41**	GPIO41_SR1	**Bitwise CLR operation of GPIO41 SR1 control** 0: 1: CLR bits	Keep
19	**GPIO40**	GPIO40_SR1	**Bitwise CLR operation of GPIO40 SR1 control** 0: 1: CLR bits	Keep
18	**GPIO39**	GPIO39_SR1	**Bitwise CLR operation of GPIO39 SR1 control** 0: 1: CLR bits	Keep
17	**GPIO38**	GPIO38_SR1	**Bitwise CLR operation of GPIO38 SR1 control** 0: 1: CLR bits	Keep
16	**GPIO37**	GPIO37_SR1	**Bitwise CLR operation of GPIO37 SR1 control** 0: 1: CLR bits	Keep

Bit(s)	Mnemonic	Name	Description
5	**GPIO42**	GPIO42_SR0	**Bitwise CLR operation of GPIO42 SR0 control** 0: Keep 1: CLR bits
4	**GPIO41**	GPIO41_SR0	**Bitwise CLR operation of GPIO41 SR0 control** 0: Keep 1: CLR bits
3	**GPIO40**	GPIO40_SR0	**Bitwise CLR operation of GPIO40 SR0 control** 0: Keep 1: CLR bits
2	**GPIO39**	GPIO39_SR0	**Bitwise CLR operation of GPIO39 SR0 control** 0: Keep 1: CLR bits
1	**GPIO38**	GPIO38_SR0	**Bitwise CLR operation of GPIO38 SR0 control** 0: Keep 1: CLR bits
0	**GPIO37**	GPIO37_SR0	**Bitwise CLR operation of GPIO37 SR0 control** 0: Keep 1: CLR bits

A0020800 GPIO_DRV0 GPIO DRV Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DRV0[31:16]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRV0[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: Configures GPIO driving control

Bit(s)	Mnemonic	Name	Description
31:0		DRV0	**GPIO_DRV0** [1: 0]: GPIO_0 [3: 2]: GPIO_1 [5: 4]: GPIO_2 [7: 6]: GPIO_3 [9: 8]: GPIO_4 [11: 10]: GPIO_5 [13: 12]: GPIO_6 [15: 14]: GPIO_7 [17: 16]: GPIO_8 [19: 18]: GPIO_9 [21: 20]: URXD1 [21: 20]: UTXD1 [23: 22]: KCOL4 [25: 24]: KCOL3 [27: 26]: KCOL2 [29: 28]: KCOL1 [31: 30]: KCOL0

A0020804 GPIO_DRV0_SET GPIO DRV Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DRV0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRV0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DRV0

Bit(s)	Mnemonic	Name	Description
31:0		DRV0	**Bitwise SET operation of GPIO_DRV0_SET** 0: Keep 1: SET bits

A0020808 GPIO_DRV0_CLR GPIO DRV Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DRV0[31:16]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRV0[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DRV0

Bit(s)	Mnemonic	Name	Description
31:0		DRV0	**Bitwise CLR operation of GPIO_DRV0_CLR** 0: Keep 1: CLR bits

A0020810 GPIO_DRV1 GPIO DRV Control 00C00000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							DRV1[25:16]									
Type							RW									
Reset							0	0	1	1	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRV1[15:0]															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: Configures GPIO driving control

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
25:0		DRV1	**GPIO_DRV1** [1: 0]: KROW4 [3: 2]: KROW3 [5: 4]: KROW2 [7: 6]: KROW1 [9: 8]: KROW0 [11: 10]: BPI_BUS2 [11: 10]: BPI_BUS1 [11: 10]: BPI_BUS0 [13: 12]: CMRST [13: 12]: CMPDN [13: 12]: CMCSD0 [13: 12]: CMCSD1 [13: 12]: CMMCLK [13: 12]: CMCSK [15: 14]: MCCK [15: 14]: MCCM0 [15: 14]: MCDA0 [15: 14]: MCDA1 [15: 14]: MCDA2 [15: 14]: MCDA3 [17: 16]: SIM1_SIO [17: 16]: SIM1_SRST [17: 16]: SIM1_SCLK [19: 18]: SIM2_SIO [19: 18]: SIM2_SRST [19: 18]: SIM2_SCLK [21: 20]: SCL28 [21: 20]: SDA28 [23: 22]: TESTMODE_D [23: 22]: LSCE_B [23: 22]: LSCK [23: 22]: LSDA [23: 22]: LSA0 [23: 22]:LPTE [25: 24]:RESETB

A0020814 GPIO_DRV1_SET GPIO DRV Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							DRV1[25:16]									
Type							WO									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRV1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DRV1

Bit(s)	Mnemonic	Name	Description
25:0		DRV1	**Bitwise SET operation of GPIO_DRV1_SET** 0: Keep 1: SET bits

A0020818 GPIO_DRV1_CLR GPIO DRV Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							DRV1[25:16]									
Type							WO									
Reset							0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRV1[15:0]															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_DRV1

Bit(s)	Mnemonic	Name	Description
25:0		DRV1	**Bitwise CLR operation of GPIO_DRV1_CLR** 0: Keep 1: CLR bits

A0020900 GPIO_IES0 GPIO IES Control 43C00BFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO30					GPIO25	GPIO24	GPIO23	GPIO22						
Type		RW					RW	RW	RW	RW						
Reset		1					1	1	1	1						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GPIO11		GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type					RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset					1		1	1	1	1	1	1	1	1	1	1

Overview: Configures GPIO input enabling control

Bit(s)	Mnemonic	Name	Description
30	**GPIO30**	GPIO30_IES	**Input buffer for GPIO30** 0: Disable 1: Enable
25	**GPIO25**	GPIO25_IES	**Input buffer for GPIO25** 0: Disable 1: Enable
24	**GPIO24**	GPIO24_IES	**Input buffer for GPIO24** 0: Disable 1: Enable
23	**GPIO23**	GPIO23_IES	**Input buffer for GPIO23** 0: Disable 1: Enable
22	**GPIO22**	GPIO22_IES	**Input buffer for GPIO22** 0: Disable 1: Enable
11	**GPIO11**	GPIO11_IES	**Input buffer for GPIO11** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
9	**GPIO9**	GPIO9_IES	**Input buffer for GPIO9** 0: Disable 1: Enable
8	**GPIO8**	GPIO8_IES	**Input buffer for GPIO8** 0: Disable 1: Enable
7	**GPIO7**	GPIO7_IES	**Input buffer for GPIO7** 0: Disable 1: Enable
6	**GPIO6**	GPIO6_IES	**Input buffer for GPIO6** 0: Disable 1: Enable
5	**GPIO5**	GPIO5_IES	**Input buffer for GPIO5** 0: Disable 1: Enable
4	**GPIO4**	GPIO4_IES	**Input buffer for GPIO4** 0: Disable 1: Enable
3	**GPIO3**	GPIO3_IES	**Input buffer for GPIO3** 0: Disable 1: Enable
2	**GPIO2**	GPIO2_IES	**Input buffer for GPIO2** 0: Disable 1: Enable
1	**GPIO1**	GPIO1_IES	**Input buffer for GPIO1** 0: Disable 1: Enable
0	**GPIO0**	GPIO0_IES	**Input buffer for GPIO0** 0: Disable 1: Enable

A0020904 GPIO_IES0_SETGPIO IES Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO30					GPIO25	GPIO24	GPIO23	GPIO22						
Type		WO					WO	WO	WO	WO						
Reset		0					0	0	0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GPIO11		GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type					WO		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset					0		0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_IES0

Bit(s)	Mnemonic	Name	Description
30	**GPIO30**	GPIO30_IES	**Bitwise SET operation of GPIO30 input buffer** 0: Keep 1: SET bits

Bit(s)	Mnemonic	Name	Description	
25	**GPIO25**	GPIO25_IES	**Bitwise SET operation of GPIO25 input buffer** 0: 1: SET bits	Keep
24	**GPIO24**	GPIO24_IES	**Bitwise SET operation of GPIO24 input buffer** 0: 1: SET bits	Keep
23	**GPIO23**	GPIO23_IES	**Bitwise SET operation of GPIO23 input buffer** 0: 1: SET bits	Keep
22	**GPIO22**	GPIO22_IES	**Bitwise SET operation of GPIO22 input buffer** 0: 1: SET bits	Keep
11	**GPIO11**	GPIO11_IES	**Bitwise SET operation of GPIO11 input buffer** 0: 1: SET bits	Keep
9	**GPIO9**	GPIO9_IES	**Bitwise SET operation of GPIO9 input buffer** 0: 1: SET bits	Keep
8	**GPIO8**	GPIO8_IES	**Bitwise SET operation of GPIO8 input buffer** 0: 1: SET bits	Keep
7	**GPIO7**	GPIO7_IES	**Bitwise SET operation of GPIO7 input buffer** 0: 1: SET bits	Keep
6	**GPIO6**	GPIO6_IES	**Bitwise SET operation of GPIO6 input buffer** 0: 1: SET bits	Keep
5	**GPIO5**	GPIO5_IES	**Bitwise SET operation of GPIO5 input buffer** 0: 1: SET bits	Keep
4	**GPIO4**	GPIO4_IES	**Bitwise SET operation of GPIO4 input buffer** 0: 1: SET bits	Keep
3	**GPIO3**	GPIO3_IES	**Bitwise SET operation of GPIO3 input buffer** 0: 1: SET bits	Keep
2	**GPIO2**	GPIO2_IES	**Bitwise SET operation of GPIO2 input buffer** 0: 1: SET bits	Keep
1	**GPIO1**	GPIO1_IES	**Bitwise SET operation of GPIO1 input buffer** 0: 1: SET bits	Keep
0	**GPIO0**	GPIO0_IES	**Bitwise SET operation of GPIO0 input buffer** 0: 1: SET bits	Keep

A0020908 **GPIO_IES0_CLR** **GPIO IES Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO3					GPIO2	GPIO2	GPIO2	GPIO2						

		0					5	4	3	2						
Type		WO					WO	WO	WO	WO						
Reset		0					0	0	0	0						
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GPIO11		GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
Type					WO		WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset					0		0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_IES0

Bit(s)	Mnemonic	Name	Description
30	**GPIO30**	GPIO30_IES	**Bitwise CLR operation of GPIO30 input buffer** 0: Keep 1: CLR bits
25	**GPIO25**	GPIO25_IES	**Bitwise CLR operation of GPIO25 input buffer** 0: Keep 1: CLR bits
24	**GPIO24**	GPIO24_IES	**Bitwise CLR operation of GPIO24 input buffer** 0: Keep 1: CLR bits
23	**GPIO23**	GPIO23_IES	**Bitwise CLR operation of GPIO23 input buffer** 0: Keep 1: CLR bits
22	**GPIO22**	GPIO22_IES	**Bitwise CLR operation of GPIO22 input buffer** 0: Keep 1: CLR bits
11	**GPIO11**	GPIO11_IES	**Bitwise CLR operation of GPIO11 input buffer** 0: Keep 1: CLR bits
9	**GPIO9**	GPIO9_IES	**Bitwise CLR operation of GPIO9 input buffer** 0: Keep 1: CLR bits
8	**GPIO8**	GPIO8_IES	**Bitwise CLR operation of GPIO8 input buffer** 0: Keep 1: CLR bits
7	**GPIO7**	GPIO7_IES	**Bitwise CLR operation of GPIO7 input buffer** 0: Keep 1: CLR bits
6	**GPIO6**	GPIO6_IES	**Bitwise CLR operation of GPIO6 input buffer** 0: Keep 1: CLR bits
5	**GPIO5**	GPIO5_IES	**Bitwise CLR operation of GPIO5 input buffer** 0: Keep 1: CLR bits
4	**GPIO4**	GPIO4_IES	**Bitwise CLR operation of GPIO4 input buffer** 0: Keep 1: CLR bits
3	**GPIO3**	GPIO3_IES	**Bitwise CLR operation of GPIO3 input buffer** 0: Keep 1: CLR bits
2	**GPIO2**	GPIO2_IES	**Bitwise CLR operation of GPIO2 input buffer** 0: Keep 1: CLR bits

Bit(s)	Mnemonic	Name	Description	
1	**GPIO1**	GPIO1_IES	**Bitwise CLR operation of GPIO1 input buffer** 0: 1: CLR bits	Keep
0	**GPIO0**	GPIO0_IES	**Bitwise CLR operation of GPIO0 input buffer** 0: 1: CLR bits	Keep

A0020910 GPIO_IES1 GPIO IES Control 00001FE0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37					
Type				RW	RW	RW	RW	RW	RW	RW	RW					
Reset				1	1	1	1	1	1	1	1					

Overview: Configures GPIO input enabling control

Bit(s)	Mnemonic	Name	Description	
12	**GPIO44**	GPIO44_IES	**Input buffer for GPIO44** 0: 1: Enable	Disable
11	**GPIO43**	GPIO43_IES	**Input buffer for GPIO43** 0: 1: Enable	Disable
10	**GPIO42**	GPIO42_IES	**Input buffer for GPIO42** 0: 1: Enable	Disable
9	**GPIO41**	GPIO41_IES	**Input buffer for GPIO41** 0: 1: Enable	Disable
8	**GPIO40**	GPIO40_IES	**Input buffer for GPIO40** 0: 1: Enable	Disable
7	**GPIO39**	GPIO39_IES	**Input buffer for GPIO39** 0: 1: Enable	Disable
6	**GPIO38**	GPIO38_IES	**Input buffer for GPIO38** 0: 1: Enable	Disable
5	**GPIO37**	GPIO37_IES	**Input buffer for GPIO37** 0: 1: Enable	Disable

A0020914 GPIO_IES1_SETGPIO IES Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37					
Type				WO	WO	WO	WO	WO	WO	WO	WO					
Reset				0	0	0	0	0	0	0	0					

Overview: For bitwise access of GPIO_IES1

Bit(s)	Mnemonic	Name	Description
12	**GPIO44**	GPIO44_IES	**Bitwise SET operation of GPIO44 input buffer** 0: Keep 1: SET bits
11	**GPIO43**	GPIO43_IES	**Bitwise SET operation of GPIO43 input buffer** 0: Keep 1: SET bits
10	**GPIO42**	GPIO42_IES	**Bitwise SET operation of GPIO42 input buffer** 0: Keep 1: SET bits
9	**GPIO41**	GPIO41_IES	**Bitwise SET operation of GPIO41 input buffer** 0: Keep 1: SET bits
8	**GPIO40**	GPIO40_IES	**Bitwise SET operation of GPIO40 input buffer** 0: Keep 1: SET bits
7	**GPIO39**	GPIO39_IES	**Bitwise SET operation of GPIO39 input buffer** 0: Keep 1: SET bits
6	**GPIO38**	GPIO38_IES	**Bitwise SET operation of GPIO38 input buffer** 0: Keep 1: SET bits
5	**GPIO37**	GPIO37_IES	**Bitwise SET operation of GPIO37 input buffer** 0: Keep 1: SET bits

A0020918 GPIO_IES1_CLR GPIO IES Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				GPIO44	GPIO43	GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37					
Type				WO	WO	WO	WO	WO	WO	WO	WO					
Reset				0	0	0	0	0	0	0	0					

Overview: For bitwise access of GPIO_IES1

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description	
12	**GPIO44**	GPIO44_IES	**Bitwise CLR operation of GPIO44 input buffer** 0: 1: CLR bits	Keep
11	**GPIO43**	GPIO43_IES	**Bitwise CLR operation of GPIO43 input buffer** 0: 1: CLR bits	Keep
10	**GPIO42**	GPIO42_IES	**Bitwise CLR operation of GPIO42 input buffer** 0: 1: CLR bits	Keep
9	**GPIO41**	GPIO41_IES	**Bitwise CLR operation of GPIO41 input buffer** 0: 1: CLR bits	Keep
8	**GPIO40**	GPIO40_IES	**Bitwise CLR operation of GPIO40 input buffer** 0: 1: CLR bits	Keep
7	**GPIO39**	GPIO39_IES	**Bitwise CLR operation of GPIO39 input buffer** 0: 1: CLR bits	Keep
6	**GPIO38**	GPIO38_IES	**Bitwise CLR operation of GPIO38 input buffer** 0: 1: CLR bits	Keep
5	**GPIO37**	GPIO37_IES	**Bitwise CLR operation of GPIO37 input buffer** 0: 1: CLR bits	Keep

A0020A00 GPIO_PUPD0 GPIO PUPD Control 303E0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	**GPIO31**		**GPIO29**	**GPIO28**	**GPIO27**	**GPIO26**					**GPIO21**	**GPIO20**	**GPIO19**	**GPIO18**	**GPIO17**	**GPIO16**
Type	RW		RW	RW	RW	RW					RW	RW	RW	RW	RW	RW
Reset	0		1	1	0	0					1	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GPIO15**	**GPIO14**	**GPIO13**	**GPIO12**		**GPIO10**										
Type	RW	RW	RW	RW		RW										
Reset	0	0	0	0		0										

Overview: Configures GPIO PUPD control

Bit(s)	Mnemonic	Name	Description	
31	**GPIO31**	GPIO31_PUPD	**PUPD for GPIO31** 0: 1: Enable	Disable
29	**GPIO29**	GPIO29_PUPD	**PUPD for GPIO29** 0: 1: Enable	Disable
28	**GPIO28**	GPIO28_PUPD	**PUPD for GPIO28** 0: 1: Enable	Disable
27	**GPIO27**	GPIO27_PUPD	**PUPD for GPIO27** 0:	Disable

Bit(s)	Mnemonic	Name	Description	
			1: Enable	
26	**GPIO26**	GPIO26_PUPD	**PUPD for GPIO26**	
			0:	Disable
			1: Enable	
21	**GPIO21**	GPIO21_PUPD	**PUPD for GPIO21**	
			0:	Disable
			1: Enable	
20	**GPIO20**	GPIO20_PUPD	**PUPD for GPIO20**	
			0:	Disable
			1: Enable	
19	**GPIO19**	GPIO19_PUPD	**PUPD for GPIO19**	
			0:	Disable
			1: Enable	
18	**GPIO18**	GPIO18_PUPD	**PUPD for GPIO18**	
			0:	Disable
			1: Enable	
17	**GPIO17**	GPIO17_PUPD	**PUPD for GPIO17**	
			0:	Disable
			1: Enable	
16	**GPIO16**	GPIO16_PUPD	**PUPD for GPIO16**	
			0:	Disable
			1: Enable	
15	**GPIO15**	GPIO15_PUPD	**PUPD for GPIO15**	
			0:	Disable
			1: Enable	
14	**GPIO14**	GPIO14_PUPD	**PUPD for GPIO14**	
			0:	Disable
			1: Enable	
13	**GPIO13**	GPIO13_PUPD	**PUPD for GPIO13**	
			0:	Disable
			1: Enable	
12	**GPIO12**	GPIO12_PUPD	**PUPD for GPIO12**	
			0:	Disable
			1: Enable	
10	**GPIO10**	GPIO10_PUPD	**PUPD for GPIO10**	
			0:	Disable
			1: Enable	

A0020A04 GPIO_PUPD0_SET GPIO PUPD Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31		GPIO29	GPIO28	GPIO27	GPIO26					GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	WO		WO	WO	WO	WO					WO	WO	WO	WO	WO	WO
Reset	0		0	0	0	0					0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12		GPIO10										
Type	WO	WO	WO	WO		WO										
Reset	0	0	0	0		0										

Overview: For bitwise access of GPIO_PUPD0

Bit(s)	Mnemonic	Name	Description	
31	**GPIO31**	GPIO31_PUPD	**Bitwise SET operation of GPIO31 PUPD**	
			0: 1: SET bits	Keep
29	**GPIO29**	GPIO29_PUPD	**Bitwise SET operation of GPIO29 PUPD**	
			0: 1: SET bits	Keep
28	**GPIO28**	GPIO28_PUPD	**Bitwise SET operation of GPIO28 PUPD**	
			0: 1: SET bits	Keep
27	**GPIO27**	GPIO27_PUPD	**Bitwise SET operation of GPIO27 PUPD**	
			0: 1: SET bits	Keep
26	**GPIO26**	GPIO26_PUPD	**Bitwise SET operation of GPIO26 PUPD**	
			0: 1: SET bits	Keep
21	**GPIO21**	GPIO21_PUPD	**Bitwise SET operation of GPIO21 PUPD**	
			0: 1: SET bits	Keep
20	**GPIO20**	GPIO20_PUPD	**Bitwise SET operation of GPIO20 PUPD**	
			0: 1: SET bits	Keep
19	**GPIO19**	GPIO19_PUPD	**Bitwise SET operation of GPIO19 PUPD**	
			0: 1: SET bits	Keep
18	**GPIO18**	GPIO18_PUPD	**Bitwise SET operation of GPIO18 PUPD**	
			0: 1: SET bits	Keep
17	**GPIO17**	GPIO17_PUPD	**Bitwise SET operation of GPIO17 PUPD**	
			0: 1: SET bits	Keep
16	**GPIO16**	GPIO16_PUPD	**Bitwise SET operation of GPIO16 PUPD**	
			0: 1: SET bits	Keep
15	**GPIO15**	GPIO15_PUPD	**Bitwise SET operation of GPIO15 PUPD**	
			0: 1: SET bits	Keep
14	**GPIO14**	GPIO14_PUPD	**Bitwise SET operation of GPIO14 PUPD**	
			0: 1: SET bits	Keep
13	**GPIO13**	GPIO13_PUPD	**Bitwise SET operation of GPIO13 PUPD**	
			0: 1: SET bits	Keep
12	**GPIO12**	GPIO12_PUPD	**Bitwise SET operation of GPIO12 PUPD**	
			0: 1: SET bits	Keep
10	**GPIO10**	GPIO10_PUPD	**Bitwise SET operation of GPIO10 PUPD**	
			0: 1: SET bits	Keep

A0020A08 GPIO_PUPD0_CLR GPIO PUPD Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31		GPIO29	GPIO28	GPIO27	GPIO26					GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	WO		WO	WO	WO	WO					WO	WO	WO	WO	WO	WO
Reset	0		0	0	0	0					0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12		GPIO10										
Type	WO	WO	WO	WO		WO										
Reset	0	0	0	0		0										

Overview: For bitwise access of GPIO_PUPD0

Bit(s)	Mnemonic	Name	Description
31	**GPIO31**	GPIO31_PUPD	**Bitwise CLR operation of GPIO31 PUPD** 0: Keep 1: CLR bits
29	**GPIO29**	GPIO29_PUPD	**Bitwise CLR operation of GPIO29 PUPD** 0: Keep 1: CLR bits
28	**GPIO28**	GPIO28_PUPD	**Bitwise CLR operation of GPIO28 PUPD** 0: Keep 1: CLR bits
27	**GPIO27**	GPIO27_PUPD	**Bitwise CLR operation of GPIO27 PUPD** 0: Keep 1: CLR bits
26	**GPIO26**	GPIO26_PUPD	**Bitwise CLR operation of GPIO26 PUPD** 0: Keep 1: CLR bits
21	**GPIO21**	GPIO21_PUPD	**Bitwise CLR operation of GPIO21 PUPD** 0: Keep 1: CLR bits
20	**GPIO20**	GPIO20_PUPD	**Bitwise CLR operation of GPIO20 PUPD** 0: Keep 1: CLR bits
19	**GPIO19**	GPIO19_PUPD	**Bitwise CLR operation of GPIO19 PUPD** 0: Keep 1: CLR bits
18	**GPIO18**	GPIO18_PUPD	**Bitwise CLR operation of GPIO18 PUPD** 0: Keep 1: CLR bits
17	**GPIO17**	GPIO17_PUPD	**Bitwise CLR operation of GPIO17 PUPD** 0: Keep 1: CLR bits
16	**GPIO16**	GPIO16_PUPD	**Bitwise CLR operation of GPIO16 PUPD** 0: Keep 1: CLR bits
15	**GPIO15**	GPIO15_PUPD	**Bitwise CLR operation of GPIO15 PUPD** 0: Keep 1: CLR bits

Bit(s)	Mnemonic	Name	Description	
14	**GPIO14**	GPIO14_PUPD	**Bitwise CLR operation of GPIO14 PUPD** 0: 1: CLR bits	Keep
13	**GPIO13**	GPIO13_PUPD	**Bitwise CLR operation of GPIO13 PUPD** 0: 1: CLR bits	Keep
12	**GPIO12**	GPIO12_PUPD	**Bitwise CLR operation of GPIO12 PUPD** 0: 1: CLR bits	Keep
10	**GPIO10**	GPIO10_PUPD	**Bitwise CLR operation of GPIO10 PUPD** 0: 1: CLR bits	Keep

A0020A10 GPIO_PUPD1 GPIO PUPD Control 0007A7FE

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													**GPIO51**	**GPIO50**	**GPIO49**	**GPIO48**
Type													RW	RW	RW	RW
Reset													0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	**GPIO47**	**GPIO46**	**GPIO45**			**GPIO42**	**GPIO41**	**GPIO40**	**GPIO39**	**GPIO38**	**GPIO37**	**GPIO36**	**GPIO35**	**GPIO34**	**GPIO33**	**GPIO32**
Type	RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	1			1	1	1	1	1	1	1	1	1	1	0

Overview: Configures GPIO PUPD control

Bit(s)	Mnemonic	Name	Description	
19	**GPIO51**	GPIO51_PUPD	**PUPD for GPIO51** 0: 1: Enable	Disable
18	**GPIO50**	GPIO50_PUPD	**PUPD for GPIO50** 0: 1: Enable	Disable
17	**GPIO49**	GPIO49_PUPD	**PUPD for GPIO49** 0: 1: Enable	Disable
16	**GPIO48**	GPIO48_PUPD	**PUPD for GPIO48** 0: 1: Enable	Disable
15	**GPIO47**	GPIO47_PUPD	**PUPD for GPIO47** 0: 1: Enable	Disable
14	**GPIO46**	GPIO46_PUPD	**PUPD for GPIO46** 0: 1: Enable	Disable
13	**GPIO45**	GPIO45_PUPD	**PUPD for GPIO45** 0: 1: Enable	Disable
10	**GPIO42**	GPIO42_PUPD	**PUPD for GPIO42** 0:	Disable

Bit(s)	Mnemonic	Name	Description	
			1: Enable	
9	**GPIO41**	GPIO41_PUPD	**PUPD for GPIO41** 0: 1: Enable	Disable
8	**GPIO40**	GPIO40_PUPD	**PUPD for GPIO40** 0: 1: Enable	Disable
7	**GPIO39**	GPIO39_PUPD	**PUPD for GPIO39** 0: 1: Enable	Disable
6	**GPIO38**	GPIO38_PUPD	**PUPD for GPIO38** 0: 1: Enable	Disable
5	**GPIO37**	GPIO37_PUPD	**PUPD for GPIO37** 0: 1: Enable	Disable
4	**GPIO36**	GPIO36_PUPD	**PUPD for GPIO36** 0: 1: Enable	Disable
3	**GPIO35**	GPIO35_PUPD	**PUPD for GPIO35** 0: 1: Enable	Disable
2	**GPIO34**	GPIO34_PUPD	**PUPD for GPIO34** 0: 1: Enable	Disable
1	**GPIO33**	GPIO33_PUPD	**PUPD for GPIO33** 0: 1: Enable	Disable
0	**GPIO32**	GPIO32_PUPD	**PUPD for GPIO32** 0: 1: Enable	Disable

A0020A14 GPIO_PUPD1_SET GPIO PUPD Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GPIO51	GPIO50	GPIO49	GPIO48
Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45			GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	WO	WO	WO			WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0			0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_PUPD1

Bit(s)	Mnemonic	Name	Description	
19	**GPIO51**	GPIO51_PUPD	**Bitwise SET operation of GPIO51 PUPD** 0: 1: SET bits	Keep

Bit(s)	Mnemonic	Name	Description	
18	**GPIO50**	GPIO50_PUPD	**Bitwise SET operation of GPIO50 PUPD** 0: 1: SET bits	Keep
17	**GPIO49**	GPIO49_PUPD	**Bitwise SET operation of GPIO49 PUPD** 0: 1: SET bits	Keep
16	**GPIO48**	GPIO48_PUPD	**Bitwise SET operation of GPIO48 PUPD** 0: 1: SET bits	Keep
15	**GPIO47**	GPIO47_PUPD	**Bitwise SET operation of GPIO47 PUPD** 0: 1: SET bits	Keep
14	**GPIO46**	GPIO46_PUPD	**Bitwise SET operation of GPIO46 PUPD** 0: 1: SET bits	Keep
13	**GPIO45**	GPIO45_PUPD	**Bitwise SET operation of GPIO45 PUPD** 0: 1: SET bits	Keep
10	**GPIO42**	GPIO42_PUPD	**Bitwise SET operation of GPIO42 PUPD** 0: 1: SET bits	Keep
9	**GPIO41**	GPIO41_PUPD	**Bitwise SET operation of GPIO41 PUPD** 0: 1: SET bits	Keep
8	**GPIO40**	GPIO40_PUPD	**Bitwise SET operation of GPIO40 PUPD** 0: 1: SET bits	Keep
7	**GPIO39**	GPIO39_PUPD	**Bitwise SET operation of GPIO39 PUPD** 0: 1: SET bits	Keep
6	**GPIO38**	GPIO38_PUPD	**Bitwise SET operation of GPIO38 PUPD** 0: 1: SET bits	Keep
5	**GPIO37**	GPIO37_PUPD	**Bitwise SET operation of GPIO37 PUPD** 0: 1: SET bits	Keep
4	**GPIO36**	GPIO36_PUPD	**Bitwise SET operation of GPIO36 PUPD** 0: 1: SET bits	Keep
3	**GPIO35**	GPIO35_PUPD	**Bitwise SET operation of GPIO35 PUPD** 0: 1: SET bits	Keep
2	**GPIO34**	GPIO34_PUPD	**Bitwise SET operation of GPIO34 PUPD** 0: 1: SET bits	Keep
1	**GPIO33**	GPIO33_PUPD	**Bitwise SET operation of GPIO33 PUPD** 0: 1: SET bits	Keep
0	**GPIO32**	GPIO32_PUPD	**Bitwise SET operation of GPIO32 PUPD** 0: 1: SET bits	Keep

A0020A18 GPIO_PUPD1_CLR GPIO PUPD Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GPIO51	GPIO50	GPIO49	GPIO48
Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45			GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	WO	WO	WO			WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0			0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_PUPD1

Bit(s)	Mnemonic	Name	Description
19	**GPIO51**	GPIO51_PUPD	**Bitwise CLR operation of GPIO51 PUPD** 0: Keep 1: CLR bits
18	**GPIO50**	GPIO50_PUPD	**Bitwise CLR operation of GPIO50 PUPD** 0: Keep 1: CLR bits
17	**GPIO49**	GPIO49_PUPD	**Bitwise CLR operation of GPIO49 PUPD** 0: Keep 1: CLR bits
16	**GPIO48**	GPIO48_PUPD	**Bitwise CLR operation of GPIO48 PUPD** 0: Keep 1: CLR bits
15	**GPIO47**	GPIO47_PUPD	**Bitwise CLR operation of GPIO47 PUPD** 0: Keep 1: CLR bits
14	**GPIO46**	GPIO46_PUPD	**Bitwise CLR operation of GPIO46 PUPD** 0: Keep 1: CLR bits
13	**GPIO45**	GPIO45_PUPD	**Bitwise CLR operation of GPIO45 PUPD** 0: Keep 1: CLR bits
10	**GPIO42**	GPIO42_PUPD	**Bitwise CLR operation of GPIO42 PUPD** 0: Keep 1: CLR bits
9	**GPIO41**	GPIO41_PUPD	**Bitwise CLR operation of GPIO41 PUPD** 0: Keep 1: CLR bits
8	**GPIO40**	GPIO40_PUPD	**Bitwise CLR operation of GPIO40 PUPD** 0: Keep 1: CLR bits
7	**GPIO39**	GPIO39_PUPD	**Bitwise CLR operation of GPIO39 PUPD** 0: Keep 1: CLR bits
6	**GPIO38**	GPIO38_PUPD	**Bitwise CLR operation of GPIO38 PUPD** 0: Keep 1: CLR bits

Bit(s)	Mnemonic	Name	Description	
5	**GPIO37**	GPIO37_PUPD	**Bitwise CLR operation of GPIO37 PUPD** 0: 1: CLR bits	Keep
4	**GPIO36**	GPIO36_PUPD	**Bitwise CLR operation of GPIO36 PUPD** 0: 1: CLR bits	Keep
3	**GPIO35**	GPIO35_PUPD	**Bitwise CLR operation of GPIO35 PUPD** 0: 1: CLR bits	Keep
2	**GPIO34**	GPIO34_PUPD	**Bitwise CLR operation of GPIO34 PUPD** 0: 1: CLR bits	Keep
1	**GPIO33**	GPIO33_PUPD	**Bitwise CLR operation of GPIO33 PUPD** 0: 1: CLR bits	Keep
0	**GPIO32**	GPIO32_PUPD	**Bitwise CLR operation of GPIO32 PUPD** 0: 1: CLR bits	Keep

A0020B00 GPIO_RESEN00 GPIO R0 Control B83FF400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31		GPIO29	GPIO28	GPIO27	GPIO26					GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	RW		RW	RW	RW	RW					RW	RW	RW	RW	RW	RW
Reset	1		1	1	1	0					1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12		GPIO10										
Type	RW	RW	RW	RW		RW										
Reset	1	1	1	1		1										

Overview: Configures GPIO R0 control

Bit(s)	Mnemonic	Name	Description	
31	**GPIO31**	GPIO31_R0	**R0 for GPIO31** 0: 1: Enable	Disable
29	**GPIO29**	GPIO29_R0	**R0 for GPIO29** 0: 1: Enable	Disable
28	**GPIO28**	GPIO28_R0	**R0 for GPIO28** 0: 1: Enable	Disable
27	**GPIO27**	GPIO27_R0	**R0 for GPIO27** 0: 1: Enable	Disable
26	**GPIO26**	GPIO26_R0	**R0 for GPIO26** 0: 1: Enable	Disable

Bit(s)	Mnemonic	Name	Description
21	**GPIO21**	GPIO21_R0	**R0 for GPIO21** 0: Disable 1: Enable
20	**GPIO20**	GPIO20_R0	**R0 for GPIO20** 0: Disable 1: Enable
19	**GPIO19**	GPIO19_R0	**R0 for GPIO19** 0: Disable 1: Enable
18	**GPIO18**	GPIO18_R0	**R0 for GPIO18** 0: Disable 1: Enable
17	**GPIO17**	GPIO17_R0	**R0 for GPIO17** 0: Disable 1: Enable
16	**GPIO16**	GPIO16_R0	**R0 for GPIO16** 0: Disable 1: Enable
15	**GPIO15**	GPIO15_R0	**R0 for GPIO15** 0: Disable 1: Enable
14	**GPIO14**	GPIO14_R0	**R0 for GPIO14** 0: Disable 1: Enable
13	**GPIO13**	GPIO13_R0	**R0 for GPIO13** 0: Disable 1: Enable
12	**GPIO12**	GPIO12_R0	**R0 for GPIO12** 0: Disable 1: Enable
10	**GPIO10**	GPIO10_R0	**R0 for GPIO10** 0: Disable 1: Enable

A0020B04 GPIO_RESEN0_0_SET GPIO R0 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31		GPIO29	GPIO28	GPIO27	GPIO26					GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	WO		WO	WO	WO	WO					WO	WO	WO	WO	WO	WO
Reset	0		0	0	0	0					0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12		GPIO10										
Type	WO	WO	WO	WO		WO										
Reset	0	0	0	0		0										

Overview: For bitwise access of GPIO_RESEN0_0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description	
31	**GPIO31**	GPIO31_R0	**Bitwise SET operation of GPIO31 R0** 0: 1: SET bits	Keep
29	**GPIO29**	GPIO29_R0	**Bitwise SET operation of GPIO29 R0** 0: 1: SET bits	Keep
28	**GPIO28**	GPIO28_R0	**Bitwise SET operation of GPIO28 R0** 0: 1: SET bits	Keep
27	**GPIO27**	GPIO27_R0	**Bitwise SET operation of GPIO27 R0** 0: 1: SET bits	Keep
26	**GPIO26**	GPIO26_R0	**Bitwise SET operation of GPIO26 R0** 0: 1: SET bits	Keep
21	**GPIO21**	GPIO21_R0	**Bitwise SET operation of GPIO21 R0** 0: 1: SET bits	Keep
20	**GPIO20**	GPIO20_R0	**Bitwise SET operation of GPIO20 R0** 0: 1: SET bits	Keep
19	**GPIO19**	GPIO19_R0	**Bitwise SET operation of GPIO19 R0** 0: 1: SET bits	Keep
18	**GPIO18**	GPIO18_R0	**Bitwise SET operation of GPIO18 R0** 0: 1: SET bits	Keep
17	**GPIO17**	GPIO17_R0	**Bitwise SET operation of GPIO17 R0** 0: 1: SET bits	Keep
16	**GPIO16**	GPIO16_R0	**Bitwise SET operation of GPIO16 R0** 0: 1: SET bits	Keep
15	**GPIO15**	GPIO15_R0	**Bitwise SET operation of GPIO15 R0** 0: 1: SET bits	Keep
14	**GPIO14**	GPIO14_R0	**Bitwise SET operation of GPIO14 R0** 0: 1: SET bits	Keep
13	**GPIO13**	GPIO13_R0	**Bitwise SET operation of GPIO13 R0** 0: 1: SET bits	Keep
12	**GPIO12**	GPIO12_R0	**Bitwise SET operation of GPIO12 R0** 0: 1: SET bits	Keep
10	**GPIO10**	GPIO10_R0	**Bitwise SET operation of GPIO10 R0** 0: 1: SET bits	Keep

A0020B08 GPIO_RESEN0_ GPIO R0 Control 00000000

0_CLR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31		GPIO29	GPIO28	GPIO27	GPIO26					GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	WO		WO	WO	WO	WO					WO	WO	WO	WO	WO	WO
Reset	0		0	0	0	0					0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12		GPIO10										
Type	WO	WO	WO	WO		WO										
Reset	0	0	0	0		0										

Overview: For bitwise access of GPIO_RESEN0_0

Bit(s)	Mnemonic	Name	Description
31	**GPIO31**	GPIO31_R0	**Bitwise CLR operation of GPIO31 R0** 0: Keep 1: CLR bits
29	**GPIO29**	GPIO29_R0	**Bitwise CLR operation of GPIO29 R0** 0: Keep 1: CLR bits
28	**GPIO28**	GPIO28_R0	**Bitwise CLR operation of GPIO28 R0** 0: Keep 1: CLR bits
27	**GPIO27**	GPIO27_R0	**Bitwise CLR operation of GPIO27 R0** 0: Keep 1: CLR bits
26	**GPIO26**	GPIO26_R0	**Bitwise CLR operation of GPIO26 R0** 0: Keep 1: CLR bits
21	**GPIO21**	GPIO21_R0	**Bitwise CLR operation of GPIO21 R0** 0: Keep 1: CLR bits
20	**GPIO20**	GPIO20_R0	**Bitwise CLR operation of GPIO20 R0** 0: Keep 1: CLR bits
19	**GPIO19**	GPIO19_R0	**Bitwise CLR operation of GPIO19 R0** 0: Keep 1: CLR bits
18	**GPIO18**	GPIO18_R0	**Bitwise CLR operation of GPIO18 R0** 0: Keep 1: CLR bits
17	**GPIO17**	GPIO17_R0	**Bitwise CLR operation of GPIO17 R0** 0: Keep 1: CLR bits
16	**GPIO16**	GPIO16_R0	**Bitwise CLR operation of GPIO16 R0** 0: Keep 1: CLR bits
15	**GPIO15**	GPIO15_R0	**Bitwise CLR operation of GPIO15 R0** 0: Keep 1: CLR bits
14	**GPIO14**	GPIO14_R0	**Bitwise CLR operation of GPIO14 R0** 0: Keep 1: CLR bits

Bit(s)	Mnemonic	Name	Description	
13	**GPIO13**	GPIO13_R0	**Bitwise CLR operation of GPIO13 R0** 0: 1: CLR bits	Keep
12	**GPIO12**	GPIO12_R0	**Bitwise CLR operation of GPIO12 R0** 0: 1: CLR bits	Keep
10	**GPIO10**	GPIO10_R0	**Bitwise CLR operation of GPIO10 R0** 0: 1: CLR bits	Keep

A0020B10 GPIO_RESEN01 GPIO R0 Control 0007A7FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GPIO51	GPIO50	GPIO49	GPIO48
Type													RW	RW	RW	RW
Reset													0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45			GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	1			1	1	1	1	1	1	1	1	1	1	1

Overview: Configures GPIO R0 control

Bit(s)	Mnemonic	Name	Description	
19	**GPIO51**	GPIO51_R0	**R0 for GPIO51** 0: 1: Enable	Disable
18	**GPIO50**	GPIO50_R0	**R0 for GPIO50** 0: 1: Enable	Disable
17	**GPIO49**	GPIO49_R0	**R0 for GPIO49** 0: 1: Enable	Disable
16	**GPIO48**	GPIO48_R0	**R0 for GPIO48** 0: 1: Enable	Disable
15	**GPIO47**	GPIO47_R0	**R0 for GPIO47** 0: 1: Enable	Disable
14	**GPIO46**	GPIO46_R0	**R0 for GPIO46** 0: 1: Enable	Disable
13	**GPIO45**	GPIO45_R0	**R0 for GPIO45** 0: 1: Enable	Disable
10	**GPIO42**	GPIO42_R0	**R0 for GPIO42** 0: 1: Enable	Disable

Bit(s)	Mnemonic	Name	Description	
9	**GPIO41**	GPIO41_R0	**R0 for GPIO41** 0: 1: Enable	Disable
8	**GPIO40**	GPIO40_R0	**R0 for GPIO40** 0: 1: Enable	Disable
7	**GPIO39**	GPIO39_R0	**R0 for GPIO39** 0: 1: Enable	Disable
6	**GPIO38**	GPIO38_R0	**R0 for GPIO38** 0: 1: Enable	Disable
5	**GPIO37**	GPIO37_R0	**R0 for GPIO37** 0: 1: Enable	Disable
4	**GPIO36**	GPIO36_R0	**R0 for GPIO36** 0: 1: Enable	Disable
3	**GPIO35**	GPIO35_R0	**R0 for GPIO35** 0: 1: Enable	Disable
2	**GPIO34**	GPIO34_R0	**R0 for GPIO34** 0: 1: Enable	Disable
1	**GPIO33**	GPIO33_R0	**R0 for GPIO33** 0: 1: Enable	Disable
0	**GPIO32**	GPIO32_R0	**R0 for GPIO32** 0: 1: Enable	Disable

A0020B14 **GPIO_RESEN0_1_SET** **GPIO R0 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GPIO51	GPIO50	GPIO49	GPIO48
Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45			GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	WO	WO	WO			WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0			0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_RESEN0_1

Bit(s)	Mnemonic	Name	Description	
19	**GPIO51**	GPIO51_R0	**Bitwise SET operation of GPIO51 R0** 0: 1: SET bits	Keep

Bit(s)	Mnemonic	Name	Description	
18	**GPIO50**	GPIO50_R0	**Bitwise SET operation of GPIO50 R0** 0: 1: SET bits	Keep
17	**GPIO49**	GPIO49_R0	**Bitwise SET operation of GPIO49 R0** 0: 1: SET bits	Keep
16	**GPIO48**	GPIO48_R0	**Bitwise SET operation of GPIO48 R0** 0: 1: SET bits	Keep
15	**GPIO47**	GPIO47_R0	**Bitwise SET operation of GPIO47 R0** 0: 1: SET bits	Keep
14	**GPIO46**	GPIO46_R0	**Bitwise SET operation of GPIO46 R0** 0: 1: SET bits	Keep
13	**GPIO45**	GPIO45_R0	**Bitwise SET operation of GPIO45 R0** 0: 1: SET bits	Keep
10	**GPIO42**	GPIO42_R0	**Bitwise SET operation of GPIO42 R0** 0: 1: SET bits	Keep
9	**GPIO41**	GPIO41_R0	**Bitwise SET operation of GPIO41 R0** 0: 1: SET bits	Keep
8	**GPIO40**	GPIO40_R0	**Bitwise SET operation of GPIO40 R0** 0: 1: SET bits	Keep
7	**GPIO39**	GPIO39_R0	**Bitwise SET operation of GPIO39 R0** 0: 1: SET bits	Keep
6	**GPIO38**	GPIO38_R0	**Bitwise SET operation of GPIO38 R0** 0: 1: SET bits	Keep
5	**GPIO37**	GPIO37_R0	**Bitwise SET operation of GPIO37 R0** 0: 1: SET bits	Keep
4	**GPIO36**	GPIO36_R0	**Bitwise SET operation of GPIO36 R0** 0: 1: SET bits	Keep
3	**GPIO35**	GPIO35_R0	**Bitwise SET operation of GPIO35 R0** 0: 1: SET bits	Keep
2	**GPIO34**	GPIO34_R0	**Bitwise SET operation of GPIO34 R0** 0: 1: SET bits	Keep
1	**GPIO33**	GPIO33_R0	**Bitwise SET operation of GPIO33 R0** 0: 1: SET bits	Keep
0	**GPIO32**	GPIO32_R0	**Bitwise SET operation of GPIO32 R0** 0: 1: SET bits	Keep

A0020B18 **GPIO_RESEN0_1_CLR** **GPIO R0 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GPIO51	GPIO50	GPIO49	GPIO48
Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45			GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	WO	WO	WO			WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0			0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_RESEN0_1

Bit(s)	Mnemonic	Name	Description
19	**GPIO51**	GPIO51_R0	**Bitwise CLR operation of GPIO51 R0** 0: Keep 1: CLR bits
18	**GPIO50**	GPIO50_R0	**Bitwise CLR operation of GPIO50 R0** 0: Keep 1: CLR bits
17	**GPIO49**	GPIO49_R0	**Bitwise CLR operation of GPIO49 R0** 0: Keep 1: CLR bits
16	**GPIO48**	GPIO48_R0	**Bitwise CLR operation of GPIO48 R0** 0: Keep 1: CLR bits
15	**GPIO47**	GPIO47_R0	**Bitwise CLR operation of GPIO47 R0** 0: Keep 1: CLR bits
14	**GPIO46**	GPIO46_R0	**Bitwise CLR operation of GPIO46 R0** 0: Keep 1: CLR bits
13	**GPIO45**	GPIO45_R0	**Bitwise CLR operation of GPIO45 R0** 0: Keep 1: CLR bits
10	**GPIO42**	GPIO42_R0	**Bitwise CLR operation of GPIO42 R0** 0: Keep 1: CLR bits
9	**GPIO41**	GPIO41_R0	**Bitwise CLR operation of GPIO41 R0** 0: Keep 1: CLR bits
8	**GPIO40**	GPIO40_R0	**Bitwise CLR operation of GPIO40 R0** 0: Keep 1: CLR bits
7	**GPIO39**	GPIO39_R0	**Bitwise CLR operation of GPIO39 R0** 0: Keep 1: CLR bits
6	**GPIO38**	GPIO38_R0	**Bitwise CLR operation of GPIO38 R0** 0: Keep 1: CLR bits

Bit(s)	Mnemonic	Name	Description	
5	**GPIO37**	GPIO37_R0	**Bitwise CLR operation of GPIO37 R0** 0: 1: CLR bits	Keep
4	**GPIO36**	GPIO36_R0	**Bitwise CLR operation of GPIO36 R0** 0: 1: CLR bits	Keep
3	**GPIO35**	GPIO35_R0	**Bitwise CLR operation of GPIO35 R0** 0: 1: CLR bits	Keep
2	**GPIO34**	GPIO34_R0	**Bitwise CLR operation of GPIO34 R0** 0: 1: CLR bits	Keep
1	**GPIO33**	GPIO33_R0	**Bitwise CLR operation of GPIO33 R0** 0: 1: CLR bits	Keep
0	**GPIO32**	GPIO32_R0	**Bitwise CLR operation of GPIO32 R0** 0: 1: CLR bits	Keep

A0020B20 GPIO_RESEN10 GPIO R1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31		GPIO29	GPIO28	GPIO27	GPIO26					GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	RW		RW	RW	RW	RW					RW	RW	RW	RW	RW	RW
Reset	0		0	0	0	0					0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12		GPIO10										
Type	RW	RW	RW	RW		RW										
Reset	0	0	0	0		0										

Overview: Configures GPIO R1 control

Bit(s)	Mnemonic	Name	Description	
31	**GPIO31**	GPIO31_R1	**R1 for GPIO31** 0: 1: Enable	Disable
29	**GPIO29**	GPIO29_R1	**R1 for GPIO29** 0: 1: Enable	Disable
28	**GPIO28**	GPIO28_R1	**R1 for GPIO28** 0: 1: Enable	Disable
27	**GPIO27**	GPIO27_R1	**R1 for GPIO27** 0: 1: Enable	Disable
26	**GPIO26**	GPIO26_R1	**R1 for GPIO26** 0: 1: Enable	Disable

Bit(s)	Mnemonic	Name	Description
21	**GPIO21**	GPIO21_R1	**R1 for GPIO21** 0: Disable 1: Enable
20	**GPIO20**	GPIO20_R1	**R1 for GPIO20** 0: Disable 1: Enable
19	**GPIO19**	GPIO19_R1	**R1 for GPIO19** 0: Disable 1: Enable
18	**GPIO18**	GPIO18_R1	**R1 for GPIO18** 0: Disable 1: Enable
17	**GPIO17**	GPIO17_R1	**R1 for GPIO17** 0: Disable 1: Enable
16	**GPIO16**	GPIO16_R1	**R1 for GPIO16** 0: Disable 1: Enable
15	**GPIO15**	GPIO15_R1	**R1 for GPIO15** 0: Disable 1: Enable
14	**GPIO14**	GPIO14_R1	**R1 for GPIO14** 0: Disable 1: Enable
13	**GPIO13**	GPIO13_R1	**R1 for GPIO13** 0: Disable 1: Enable
12	**GPIO12**	GPIO12_R1	**R1 for GPIO12** 0: Disable 1: Enable
10	**GPIO10**	GPIO10_R1	**R1 for GPIO10** 0: Disable 1: Enable

A0020B24 GPIO_RESEN1_0_SET GPIO R1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31		GPIO29	GPIO28	GPIO27	GPIO26					GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	WO		WO	WO	WO	WO					WO	WO	WO	WO	WO	WO
Reset	0		0	0	0	0					0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12		GPIO10										
Type	WO	WO	WO	WO		WO										
Reset	0	0	0	0		0										

Overview: For bitwise access of GPIO_RESEN1_0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description	
31	**GPIO31**	GPIO31_R1	**Bitwise SET operation of GPIO31 R1** 0: 1: SET bits	Keep
29	**GPIO29**	GPIO29_R1	**Bitwise SET operation of GPIO29 R1** 0: 1: SET bits	Keep
28	**GPIO28**	GPIO28_R1	**Bitwise SET operation of GPIO28 R1** 0: 1: SET bits	Keep
27	**GPIO27**	GPIO27_R1	**Bitwise SET operation of GPIO27 R1** 0: 1: SET bits	Keep
26	**GPIO26**	GPIO26_R1	**Bitwise SET operation of GPIO26 R1** 0: 1: SET bits	Keep
21	**GPIO21**	GPIO21_R1	**Bitwise SET operation of GPIO21 R1** 0: 1: SET bits	Keep
20	**GPIO20**	GPIO20_R1	**Bitwise SET operation of GPIO20 R1** 0: 1: SET bits	Keep
19	**GPIO19**	GPIO19_R1	**Bitwise SET operation of GPIO19 R1** 0: 1: SET bits	Keep
18	**GPIO18**	GPIO18_R1	**Bitwise SET operation of GPIO18 R1** 0: 1: SET bits	Keep
17	**GPIO17**	GPIO17_R1	**Bitwise SET operation of GPIO17 R1** 0: 1: SET bits	Keep
16	**GPIO16**	GPIO16_R1	**Bitwise SET operation of GPIO16 R1** 0: 1: SET bits	Keep
15	**GPIO15**	GPIO15_R1	**Bitwise SET operation of GPIO15 R1** 0: 1: SET bits	Keep
14	**GPIO14**	GPIO14_R1	**Bitwise SET operation of GPIO14 R1** 0: 1: SET bits	Keep
13	**GPIO13**	GPIO13_R1	**Bitwise SET operation of GPIO13 R1** 0: 1: SET bits	Keep
12	**GPIO12**	GPIO12_R1	**Bitwise SET operation of GPIO12 R1** 0: 1: SET bits	Keep
10	**GPIO10**	GPIO10_R1	**Bitwise SET operation of GPIO10 R1** 0: 1: SET bits	Keep

A0020B28 GPIO_RESEN1_ GPIO R1 Control 00000000

0_CLR

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO31		GPIO29	GPIO28	GPIO27	GPIO26					GPIO21	GPIO20	GPIO19	GPIO18	GPIO17	GPIO16
Type	WO		WO	WO	WO	WO					WO	WO	WO	WO	WO	WO
Reset	0		0	0	0	0					0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15	GPIO14	GPIO13	GPIO12		GPIO10										
Type	WO	WO	WO	WO		WO										
Reset	0	0	0	0		0										

Overview: For bitwise access of GPIO_RESEN1_0

Bit(s)	Mnemonic	Name	Description
31	**GPIO31**	GPIO31_R1	**Bitwise CLR operation of GPIO31 R1** 0: Keep 1: CLR bits
29	**GPIO29**	GPIO29_R1	**Bitwise CLR operation of GPIO29 R1** 0: Keep 1: CLR bits
28	**GPIO28**	GPIO28_R1	**Bitwise CLR operation of GPIO28 R1** 0: Keep 1: CLR bits
27	**GPIO27**	GPIO27_R1	**Bitwise CLR operation of GPIO27 R1** 0: Keep 1: CLR bits
26	**GPIO26**	GPIO26_R1	**Bitwise CLR operation of GPIO26 R1** 0: Keep 1: CLR bits
21	**GPIO21**	GPIO21_R1	**Bitwise CLR operation of GPIO21 R1** 0: Keep 1: CLR bits
20	**GPIO20**	GPIO20_R1	**Bitwise CLR operation of GPIO20 R1** 0: Keep 1: CLR bits
19	**GPIO19**	GPIO19_R1	**Bitwise CLR operation of GPIO19 R1** 0: Keep 1: CLR bits
18	**GPIO18**	GPIO18_R1	**Bitwise CLR operation of GPIO18 R1** 0: Keep 1: CLR bits
17	**GPIO17**	GPIO17_R1	**Bitwise CLR operation of GPIO17 R1** 0: Keep 1: CLR bits
16	**GPIO16**	GPIO16_R1	**Bitwise CLR operation of GPIO16 R1** 0: Keep 1: CLR bits
15	**GPIO15**	GPIO15_R1	**Bitwise CLR operation of GPIO15 R1** 0: Keep 1: CLR bits
14	**GPIO14**	GPIO14_R1	**Bitwise CLR operation of GPIO14 R1** 0: Keep 1: CLR bits

Bit(s)	Mnemonic	Name	Description	
13	**GPIO13**	GPIO13_R1	**Bitwise CLR operation of GPIO13 R1** 0: 1: CLR bits	Keep
12	**GPIO12**	GPIO12_R1	**Bitwise CLR operation of GPIO12 R1** 0: 1: CLR bits	Keep
10	**GPIO10**	GPIO10_R1	**Bitwise CLR operation of GPIO10 R1** 0: 1: CLR bits	Keep

A0020B30 GPIO_RESEN11 GPIO R1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GPIO51	GPIO50	GPIO49	GPIO48
Type													RW	RW	RW	RW
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45			GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	RW	RW	RW			RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0			0	0	0	0	0	0	0	0	0	0	0

Overview: Configures GPIO R1 control

Bit(s)	Mnemonic	Name	Description	
19	**GPIO51**	GPIO51_R1	**R1 for GPIO51** 0: 1: Enable	Disable
18	**GPIO50**	GPIO50_R1	**R1 for GPIO50** 0: 1: Enable	Disable
17	**GPIO49**	GPIO49_R1	**R1 for GPIO49** 0: 1: Enable	Disable
16	**GPIO48**	GPIO48_R1	**R1 for GPIO48** 0: 1: Enable	Disable
15	**GPIO47**	GPIO47_R1	**R1 for GPIO47** 0: 1: Enable	Disable
14	**GPIO46**	GPIO46_R1	**R1 for GPIO46** 0: 1: Enable	Disable
13	**GPIO45**	GPIO45_R1	**R1 for GPIO45** 0: 1: Enable	Disable
10	**GPIO42**	GPIO42_R1	**R1 for GPIO42** 0: 1: Enable	Disable

Bit(s)	Mnemonic	Name	Description	
9	**GPIO41**	GPIO41_R1	**R1 for GPIO41** 0: 1: Enable	Disable
8	**GPIO40**	GPIO40_R1	**R1 for GPIO40** 0: 1: Enable	Disable
7	**GPIO39**	GPIO39_R1	**R1 for GPIO39** 0: 1: Enable	Disable
6	**GPIO38**	GPIO38_R1	**R1 for GPIO38** 0: 1: Enable	Disable
5	**GPIO37**	GPIO37_R1	**R1 for GPIO37** 0: 1: Enable	Disable
4	**GPIO36**	GPIO36_R1	**R1 for GPIO36** 0: 1: Enable	Disable
3	**GPIO35**	GPIO35_R1	**R1 for GPIO35** 0: 1: Enable	Disable
2	**GPIO34**	GPIO34_R1	**R1 for GPIO34** 0: 1: Enable	Disable
1	**GPIO33**	GPIO33_R1	**R1 for GPIO33** 0: 1: Enable	Disable
0	**GPIO32**	GPIO32_R1	**R1 for GPIO32** 0: 1: Enable	Disable

A0020B34 GPIO_RESEN1_1_SET GPIO R1 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GPIO51	GPIO50	GPIO49	GPIO48
Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45			GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	WO	WO	WO			WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0			0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_RESEN1_1

Bit(s)	Mnemonic	Name	Description	
19	**GPIO51**	GPIO51_R1	**Bitwise SET operation of GPIO51 R1** 0: 1: SET bits	Keep

Bit(s)	Mnemonic	Name	Description	
18	**GPIO50**	GPIO50_R1	**Bitwise SET operation of GPIO50 R1** 0: 1: SET bits	Keep
17	**GPIO49**	GPIO49_R1	**Bitwise SET operation of GPIO49 R1** 0: 1: SET bits	Keep
16	**GPIO48**	GPIO48_R1	**Bitwise SET operation of GPIO48 R1** 0: 1: SET bits	Keep
15	**GPIO47**	GPIO47_R1	**Bitwise SET operation of GPIO47 R1** 0: 1: SET bits	Keep
14	**GPIO46**	GPIO46_R1	**Bitwise SET operation of GPIO46 R1** 0: 1: SET bits	Keep
13	**GPIO45**	GPIO45_R1	**Bitwise SET operation of GPIO45 R1** 0: 1: SET bits	Keep
10	**GPIO42**	GPIO42_R1	**Bitwise SET operation of GPIO42 R1** 0: 1: SET bits	Keep
9	**GPIO41**	GPIO41_R1	**Bitwise SET operation of GPIO41 R1** 0: 1: SET bits	Keep
8	**GPIO40**	GPIO40_R1	**Bitwise SET operation of GPIO40 R1** 0: 1: SET bits	Keep
7	**GPIO39**	GPIO39_R1	**Bitwise SET operation of GPIO39 R1** 0: 1: SET bits	Keep
6	**GPIO38**	GPIO38_R1	**Bitwise SET operation of GPIO38 R1** 0: 1: SET bits	Keep
5	**GPIO37**	GPIO37_R1	**Bitwise SET operation of GPIO37 R1** 0: 1: SET bits	Keep
4	**GPIO36**	GPIO36_R1	**Bitwise SET operation of GPIO36 R1** 0: 1: SET bits	Keep
3	**GPIO35**	GPIO35_R1	**Bitwise SET operation of GPIO35 R1** 0: 1: SET bits	Keep
2	**GPIO34**	GPIO34_R1	**Bitwise SET operation of GPIO34 R1** 0: 1: SET bits	Keep
1	**GPIO33**	GPIO33_R1	**Bitwise SET operation of GPIO33 R1** 0: 1: SET bits	Keep
0	**GPIO32**	GPIO32_R1	**Bitwise SET operation of GPIO32 R1** 0: 1: SET bits	Keep

A0020B38 **GPIO_RESEN1_1_CLR** **GPIO R1 Control** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													GPIO51	GPIO50	GPIO49	GPIO48
Type													WO	WO	WO	WO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO47	GPIO46	GPIO45			GPIO42	GPIO41	GPIO40	GPIO39	GPIO38	GPIO37	GPIO36	GPIO35	GPIO34	GPIO33	GPIO32
Type	WO	WO	WO			WO	WO	WO	WO	WO	WO	WO	WO	WO	WO	WO
Reset	0	0	0			0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_RESEN1_1

Bit(s)	Mnemonic	Name	Description
19	**GPIO51**	GPIO51_R1	**Bitwise CLR operation of GPIO51 R1** 0: Keep 1: CLR bits
18	**GPIO50**	GPIO50_R1	**Bitwise CLR operation of GPIO50 R1** 0: Keep 1: CLR bits
17	**GPIO49**	GPIO49_R1	**Bitwise CLR operation of GPIO49 R1** 0: Keep 1: CLR bits
16	**GPIO48**	GPIO48_R1	**Bitwise CLR operation of GPIO48 R1** 0: Keep 1: CLR bits
15	**GPIO47**	GPIO47_R1	**Bitwise CLR operation of GPIO47 R1** 0: Keep 1: CLR bits
14	**GPIO46**	GPIO46_R1	**Bitwise CLR operation of GPIO46 R1** 0: Keep 1: CLR bits
13	**GPIO45**	GPIO45_R1	**Bitwise CLR operation of GPIO45 R1** 0: Keep 1: CLR bits
10	**GPIO42**	GPIO42_R1	**Bitwise CLR operation of GPIO42 R1** 0: Keep 1: CLR bits
9	**GPIO41**	GPIO41_R1	**Bitwise CLR operation of GPIO41 R1** 0: Keep 1: CLR bits
8	**GPIO40**	GPIO40_R1	**Bitwise CLR operation of GPIO40 R1** 0: Keep 1: CLR bits
7	**GPIO39**	GPIO39_R1	**Bitwise CLR operation of GPIO39 R1** 0: Keep 1: CLR bits
6	**GPIO38**	GPIO38_R1	**Bitwise CLR operation of GPIO38 R1** 0: Keep 1: CLR bits

Bit(s)	Mnemonic	Name	Description	
5	**GPIO37**	GPIO37_R1	**Bitwise CLR operation of GPIO37 R1** 0: 1: CLR bits	Keep
4	**GPIO36**	GPIO36_R1	**Bitwise CLR operation of GPIO36 R1** 0: 1: CLR bits	Keep
3	**GPIO35**	GPIO35_R1	**Bitwise CLR operation of GPIO35 R1** 0: 1: CLR bits	Keep
2	**GPIO34**	GPIO34_R1	**Bitwise CLR operation of GPIO34 R1** 0: 1: CLR bits	Keep
1	**GPIO33**	GPIO33_R1	**Bitwise CLR operation of GPIO33 R1** 0: 1: CLR bits	Keep
0	**GPIO32**	GPIO32_R1	**Bitwise CLR operation of GPIO32 R1** 0: 1: CLR bits	Keep

Key Pad

KCOL0-4

PUPD	R1	R0	WEAK PULL UP/DOWN STATE
0	0	0	Disable both resistors
0	0	1	PU-36K ohms
0	1	0	PU-1200K ohms
0	1	1	PU- 1200K//36K ohms
1	0	0	Disable both resistors
1	0	1	PD-36K ohms
1	1	0	PD-1200K ohms
1	1	1	PD- 1200K//36K ohms

KROW0-4

PUPD	R1	R0	WEAK PULL UP/DOWN STATE
0	0	0	Disable both resistors
0	0	1	PU-36K ohms
0	1	0	PU-1K ohms
0	1	1	PU- 1K//36K ohms
1	0	0	Disable both resistors
1	0	1	PD-36K ohms
1	1	0	PD-1K ohms
1	1	1	PD- 1K//36K ohms

URXD:
CMPDN/CMCSD0/CMCSD1/CMMCLK
MCCK/MCCM0/MCDA0/MCDA1/MCDA2/MCDA3

TESTMODE_D/LSCE_B/LSCK/LSDA/LSA0/LPTE
RESETB:

PUPD	R1	R0	WEAK PULL UP/DOWN STATE
0	0	0	Disable both resistors
0	0	1	PU-47K ohms
0	1	0	PU-47K ohms
0	1	1	PU- 23.5K ohms
1	0	0	Disable both resistors
1	0	1	PD-47K ohms
1	1	0	PD-47K ohms
1	1	1	PD- 23.5K ohms

A0020C00 GPIO_MODE0 GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO7				GPIO6				GPIO5				GPIO4		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO3				GPIO2				GPIO1				GPIO0			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: Configures GPIO aux. mode

Bit(s)	Mnemonic	Name	Description		
30:28		GPIO7	**Aux. mode of GPIO_7**		
			0:	GPIO7	(IO)
			1:	EINT6	(I)
			2:		Reserved
			3:	BPI_BUS5	(O)
			4:		Reserved
			5:		Reserved
			6:		Reserved
			7: Reserved		
26:24		GPIO6	**Aux. mode of GPIO_6**		
			0:	GPIO6	(IO)
			1:	EINT5	(I)
			2:	MCINS	(I)
			3:	BPI_BUS4	(O)
			4:		Reserved
			5:		Reserved
			6:		Reserved
			7: Reserved		
22:20		GPIO5	**Aux. mode of GPIO_5**		
			0:	GPIO5	(IO)
			1:	EINT4	(I)
			2:		Reserved
			3:	BPI_BUS3	(O)
			4:		Reserved
			5:		Reserved
			6:		Reserved

Bit(s)	Mnemonic	Name	Description		
			7: Reserved		
18:16		GPIO4	**Aux. mode of GPIO_4**		
			0:	GPIO4	(IO)
			1:	EINT3	(I)
			2:		Reserved
			3:		Reserved
			4:	U1RTS	(O)
			5:		Reserved
			6:		Reserved
			7: Reserved		
15:12		GPIO3	**Aux. mode of GPIO_3**		
			0:	GPIO3	(IO)
			1:	MCINS	(I)
			2:	YM	(AIO)
			3:		Reserved
			4:	PWM1	(O)
			5:	CMCSD1	(I)
			6:	EDICK	(O)
			7:	JTDO	(O)
			8:	BTJTDO	(O)
			9: FMJTDO (O)		
11:8		GPIO2	**Aux. mode of GPIO_2**		
			0:	GPIO2	(IO)
			1:	EINT2	(I)
			2:	YP	(AIO)
			3:	GPSFSYNC	(O)
			4:	PWM0	(O)
			5:	CMCSD0	(I)
			6:	EDIWS	(O)
			7:	JTRST_B	(I)
			8:	BTJTRSTB	(I)
			9: FMJTRSTB (I)		
7:4		GPIO1	**Aux. mode of GPIO_1**		
			0:	GPIO1	(IO)
			1:	EINT1	(I)
			2:	XM	(AIO)
			3:	U3TXD	(O)
			4:	U1CTS	(I)
			5:	CMMCLK	(O)
			6:	EDIDI	(I)
			7:	JTMS	(I)
			8:	BTJTMS	(I)
			9: FMJTMS (I)		
3:0		GPIO0	**Aux. mode of GPIO_0**		
			0:	GPIO0	(IO)
			1:	EINT0	(I)
			2:	XP	(AIO)
			3:	U3RXD	(I)
			4:	CMCSD2	(I)
			5:	CMCSK	(I)
			6:	EDIDO	(O)
			7:	JTDI	(I)
			8:	BTJTDI	(I)
			9: FMJTDI (I)		

A0020C04 GPIO_MODE0 GPIO Mode Control 00000000

SET

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO7				GPIO6				GPIO5				GPIO4		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO3				GPIO2				GPIO1				GPIO0			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_MODE0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO7	**Bitwise SET operation for Aux. mode of GPIO_7** 0: Keep 1: SET bits
26:24		GPIO6	**Bitwise SET operation for Aux. mode of GPIO_6** 0: Keep 1: SET bits
22:20		GPIO5	**Bitwise SET operation for Aux. mode of GPIO_5** 0: Keep 1: SET bits
18:16		GPIO4	**Bitwise SET operation for Aux. mode of GPIO_4** 0: Keep 1: SET bits
15:12		GPIO3	**Bitwise SET operation for Aux. mode of GPIO_3** 0: Keep 1: SET bits
11:8		GPIO2	**Bitwise SET operation for Aux. mode of GPIO_2** 0: Keep 1: SET bits
7:4		GPIO1	**Bitwise SET operation for Aux. mode of GPIO_1** 0: Keep 1: SET bits
3:0		GPIO0	**Bitwise SET operation for Aux. mode of GPIO_0** 0: Keep 1: SET bits

A0020C08 GPIO_MODE0_CLR GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO7				GPIO6				GPIO5				GPIO4		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO3				GPIO2				GPIO1				GPIO0			
Type	WO				WO				WO				WO			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Overview: For bitwise access of GPIO_MODE0

Bit(s)	Mnemonic	Name	Description
30:28		GPIO7	**Bitwise CLR operation for Aux. mode of GPIO_7** 0: Keep 1: CLR bits
26:24		GPIO6	**Bitwise CLR operation for Aux. mode of GPIO_6** 0: Keep 1: CLR bits
22:20		GPIO5	**Bitwise CLR operation for Aux. mode of GPIO_5** 0: Keep 1: CLR bits
18:16		GPIO4	**Bitwise CLR operation for Aux. mode of GPIO_4** 0: Keep 1: CLR bits
15:12		GPIO3	**Bitwise CLR operation for Aux. mode of GPIO_3** 0: Keep 1: CLR bits
11:8		GPIO2	**Bitwise CLR operation for Aux. mode of GPIO_2** 0: Keep 1: CLR bits
7:4		GPIO1	**Bitwise CLR operation for Aux. mode of GPIO_1** 0: Keep 1: CLR bits
3:0		GPIO0	**Bitwise CLR operation for Aux. mode of GPIO_0** 0: Keep 1: CLR bits

A0020C10 GPIO_MODE1 GPIO Mode Control 00001100

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO15				GPIO14				GPIO13				GPIO12		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO11				GPIO10				GPIO9				GPIO8		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	0		0	0	0

Overview: Configures GPIO aux. mode

Bit(s)	Mnemonic	Name	Description
30:28		GPIO15	**Aux. mode of GPIO_15** 0: GPIO15 (IO) 1: KCOL1 (IO) 2: GPSFSYNC (O) 3: U1CTS (I) 4: FMJTCK (I) 5: JTCK (I) 6: BTJTCK (I) 7: Reserved
26:24		GPIO14	**Aux. mode of GPIO_14** 0: GPIO14 (IO) 1: KCOL2 (IO) 2: EINT12 (I) 3: U1RTS (I)

Bit(s)	Mnemonic	Name	Description		
			4:		Reserved
			5:		Reserved
			6:		Reserved
			7: Reserved		
22:20		GPIO13	**Aux. mode of GPIO_13**		
			0:	GPIO13	(IO)
			1:	KCOL3	(IO)
			2:	EINT11	(I)
			3:	PWM0	(O)
			4:	FMJTMS	(I)
			5:	JTMS	(I)
			6:	BTJTMS	(I)
			7: Reserved		
18:16		GPIO12	**Aux. mode of GPIO_12**		
			0:	GPIO12	(IO)
			1:	KCOL4	(IO)
			2:	U2RXD	(I)
			3:	EDIDI	(I)
			4:	FMJTDI	(I)
			5:	JTDI	(I)
			6:	BTJTDI	(I)
			7: Reserved		
14:12		GPIO11	**Aux. mode of GPIO_11**		
			0:	GPIO11	(IO)
			1:	U1TXD	(O)
			2:	CMPDN	(O)
			3:	EINT10	(I)
			4:		Reserved
			5:		Reserved
			6:		Reserved
			7: Reserved		
10:8		GPIO10	**Aux. mode of GPIO_10**		
			0:	GPIO10	(IO)
			1:	U1RXD	(I)
			2:	CMRST	(O)
			3:	EINT9	(I)
			4:	MCINS	(I)
			5:		Reserved
			6:		Reserved
			7: Reserved		
6:4		GPIO9	**Aux. mode of GPIO_9**		
			0:	GPIO9	(IO)
			1:	EINT8	(I)
			2:	SDA	(IO)
			3:		Reserved
			4:		Reserved
			5:		Reserved
			6:		Reserved
			7: Reserved		
2:0		GPIO8	**Aux. mode of GPIO_8**		
			0:	GPIO8	(IO)
			1:	EINT7	(I)
			2:	SCL	(IO)
			3:		Reserved
			4:		Reserved
			5:		Reserved
			6:		Reserved
			7: Reserved		

A0020C14 GPIO_MODE1_SET GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO15				GPIO14				GPIO13				GPIO12		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO11				GPIO10				GPIO9				GPIO8		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Overview: For bitwise access of GPIO_MODE1

Bit(s)	Mnemonic	Name	Description	
30:28		GPIO15	**Bitwise SET operation for Aux. mode of KCOL1** 0: 1: SET bits	Keep
26:24		GPIO14	**Bitwise SET operation for Aux. mode of KCOL2** 0: 1: SET bits	Keep
22:20		GPIO13	**Bitwise SET operation for Aux. mode of KCOL3** 0: 1: SET bits	Keep
18:16		GPIO12	**Bitwise SET operation for Aux. mode of KCOL4** 0: 1: SET bits	Keep
14:12		GPIO11	**Bitwise SET operation for Aux. mode of UTXD1** 0: 1: SET bits	Keep
10:8		GPIO10	**Bitwise SET operation for Aux. mode of URXD1** 0: 1: SET bits	Keep
6:4		GPIO9	**Bitwise SET operation for Aux. mode of GPIO_9** 0: 1: SET bits	Keep
2:0		GPIO8	**Bitwise SET operation for Aux. mode of GPIO_8** 0: 1: SET bits	Keep

A0020C18 GPIO_MODE1_CLR GPIO Mode Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO15				GPIO14				GPIO13				GPIO12		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO11				GPIO10				GPIO9				GPIO8		
Type		WO				WO				WO				WO		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Overview: For bitwise access of GPIO_MODE1

Bit(s)	Mnemonic	Name	Description
30:28		GPIO15	**Bitwise CLR operation for Aux. mode of KCOL1** 0: Keep 1: CLR bits
26:24		GPIO14	**Bitwise CLR operation for Aux. mode of KCOL2** 0: Keep 1: CLR bits
22:20		GPIO13	**Bitwise CLR operation for Aux. mode of KCOL3** 0: Keep 1: CLR bits
18:16		GPIO12	**Bitwise CLR operation for Aux. mode of KCOL4** 0: Keep 1: CLR bits
14:12		GPIO11	**Bitwise CLR operation for Aux. mode of UTXD1** 0: Keep 1: CLR bits
10:8		GPIO10	**Bitwise CLR operation for Aux. mode of URXD1** 0: Keep 1: CLR bits
6:4		GPIO9	**Bitwise CLR operation for Aux. mode of GPIO_9** 0: Keep 1: CLR bits
2:0		GPIO8	**Bitwise CLR operation for Aux. mode of GPIO_8** 0: Keep 1: CLR bits

A0020C20 GPIO_MODE2 GPIO Mode Control 11000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		GPIO23				GPIO22				GPIO21				GPIO20		
Type		RW				RW				RW				RW		
Reset		0	0	1		0	0	1		0	0	0		0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GPIO19				GPIO18				GPIO17				GPIO16		
Type		RW				RW				RW				RW		
Reset		0	0	0		0	0	0		0	0	0		0	0	0

Overview: Configures GPIO aux. mode

Bit(s)	Mnemonic	Name	Description
30:28		GPIO23	**Aux. mode of GPIO_23** 0: GPIO23 (IO) 1: BPI_BUS1 (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved

Bit(s)	Mnemonic	Name	Description		
26:24		GPIO22	**Aux. mode of GPIO_22**		
			0:	GPIO22	(IO)
			1:	BPI_BUS2	(O)
			2:		Reserved
			3:		Reserved
			4:		Reserved
			5:		Reserved
			6:		Reserved
			7: Reserved		
22:20		GPIO21	**Aux. mode of GPIO_21**		
			0:	GPIO21	(IO)
			1:	KROW0	(IO)
			2:		Reserved
			3:		Reserved
			4:		Reserved
			5:	MCINS	(I)
			6:	BTDBGIN	(I)
			7: Reserved		
18:16		GPIO20	**Aux. mode of GPIO_20**		
			0:	GPIO20	(IO)
			1:	KROW1	(IO)
			2:	EINT14	(I)
			3:	EDIDO	(O)
			4:	BTPRI	(IO)
			5:	JTRCK	(O)
			6:	BTDBGACKN	(O)
			7: Reserved		
14:12		GPIO19	**Aux. mode of GPIO_19**		
			0:	GPIO19	(IO)
			1:	KROW2	(IO)
			2:	PWM1	(O)
			3:	EDIWS	(O)
			4:	FMJTDO	(O)
			5:	JTDO	(O)
			6:	BTJTDO	(O)
			7: Reserved		
10:8		GPIO18	**Aux. mode of GPIO_18**		
			0:	GPIO18	(IO)
			1:	KROW3	(IO)
			2:	EINT13	(I)
			3:	CLKO0	(O)
			4:	FMJTRSTB	(I)
			5:	JTRST_B	(I)
			6:	BTJTRSTB	(I)
			7: Reserved		
6:4		GPIO17	**Aux. mode of GPIO_17**		
			0:	GPIO17	(IO)
			1:	KROW4	(IO)
			2:	U2TXD	(O)
			3:	EDICK	(O)
			4:		Reserved
			5:		Reserved
			6:		Reserved
			7: Reserved		
2:0		GPIO16	**Aux. mode of GPIO_16**		
			0:	GPIO16	(IO)
			1:	KCOL0	(IO)
			2:		Reserved