OPERATIONAL DESCRIPTION

The equipment under test (EUT) is the transmitter of PCD PH3501, a quad-band (850/900/1800/1900)GSM/GPRS/E-GPRS+WCDMA850/1900 mobile phone. The transmitter operates in a half-duplex system according to the GSM standards.

The majority of the phone circuitry consists of a six device chipset; the VC7584 Power Amplifier and VC5318 Power Amplifier, the MT6572 Baseband Processor, the MT6323 POWER manager,the FM/BT/WIFI/GPS 4IN1 MT6627 and the RF Processor MT6166V, the system is powered by a rechargeable lithium-ion battery with a nominal voltage of 3.7volts.

MediaTek MT6572 brings dual-core performance to entry-level smartphones without taking a toll on battery life. Based on the energy-efficient dual-core ARM® Cortex®-A7 processor, MT6572 features a cost-optimised system level design that simplifies product development, reduces manufacturing costs and speeds up the time to market.

MT6572 features wide connectivity options, including Wi-Fi, Bluetooth and GPS. Multimedia features include support for a 960 x 540 display with MediaTek MiraVision™ image enhancement, 720p HD video and a 5-megapixel camera.

MT6166 is a RF transceiver targeted at high speed 2G/3G-FDD multi-mode smart phone and tablet computers implant in 40nm CMOS.The RF transceiver function is fully integrated。 This document briefly introduces the RF macros in MT6166.

MT6627 is a 4-in-1 connectivity chip which contains a Wi-Fi/Bluetooth transcei ver front-end, a GPS receiver front-end and a complete FM receiver, along wit h Integrated Passive Device (IPD) in a QFN40 pacakge.

The transmitter oscillators which comprise the translational loop architecture are internal to the transceiver IC and are phase locked to a 13 MHz reference signal derived from the 26 MHz crystal oscillator. The UHF local oscillator fractional-N phase lock loop operates on a fundamental frequency from 1353 MHz to 1506 MHz. This signal is divided by three for use in the 900 MHz GSM band, and is divided by three then multiplied by two for use as the DCS/PCS local oscillator. The main oscillators operate fundamentally on their respective GSM, DCS, or PCS band. The

phase detector operates at 41 – 50 MHz when tuned to the GSM band, and between 80 – 102 MHz for the DCS/PCS bands.

The main oscillator signals are amplified by the power amplifier, routed to the match net and finally delivered to the antenna. The directional coupler samples the output RF signal which is subsequently detected by a temperature compensated Schottky diode RF detector. The detected signal is used in the integrating power control loop which resides internal to the transceiver IC for setting and controlling the output power. The power settings are calibrated at the factory and stored in the flash memory IC. These settings are used as the reference level for the power control loop. Power ramping functions are also controlled by the mixed signal device.

The GMSK modulation is provided in-loop by quadrature I/Q signals which are sent to the transceiver IC from the mixed-signal device which converted the digital stream from the baseband processor into an analog signal used by the modulator. The mixed signal device is controlled by the baseband processor. The RF performance conforms to the ETSI specifications for spectrum due to modulation, transient switching modulation spectrum, power ramp, and power output, as well as all the other ETSI requirements.

The receiver is a direct-conversion design, therefore an intermediate frequency (IF) SAW filter is not used in this design. The RF preamplifiers are internal to the transceiver and provide the signal to the sub-harmonically (1/2 frequency) pumped mixers. Sallen-Key lowpass filters, variable gain amplifiers, and DC offset correction circuits comprise the remainder of the receiver. The received signals now at baseband frequencies are routed from the transceiver to the mixed-signal device for further processing and ultimately to the baseband processor.

The mixed signal device digitizes the baseband I/Q signals using Sigma-Delta DACs and sends them to the baseband processor through a serial digital interface. This IC also has analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) to directly interface to the handset speaker and microphone. The voiceband Codec section provides a 32 ohm interface to the speaker and microphone and also provides Line In/Out signals for the headset. Additional the mixed signal device contains all required system power supply regulators.

The baseband processor handles all physical layer radio control signals and network interfaces.The 32 kHz clock oscillator operates the baseband IC from a backup

battery when the main battery is removed. The baseband processor is a dual-core device that called dual-core ARM cortex A7 .The DSP handles the physical and layer 1 processing, while the ARM11 executes the layer 2 and layer 3 protocol and the man-machine interface (MMI). The dual cores communicate through a dedicated block of dual port memory. It also communicates with the Subscriber Identity Module (SIM) through an interface to the mixed signal device. The baseband processor also communicates to the calibration system or external devices through a digital serial link that is available on the system connector. The other main signals on the system connector include the digital audio interface (DAI) and allows for an external battery charging voltage.

The MMI completes the phone design and includes the displays, keypads, vibration motor, LEDs, speaker, microphone, and headset. The more details related operations, please refer to the user manual.