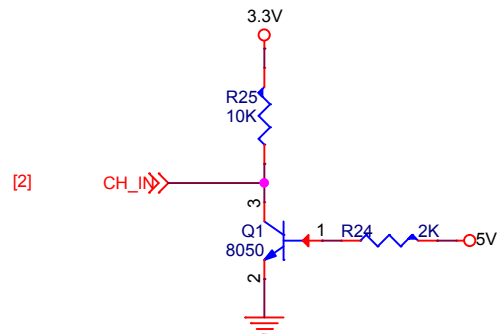
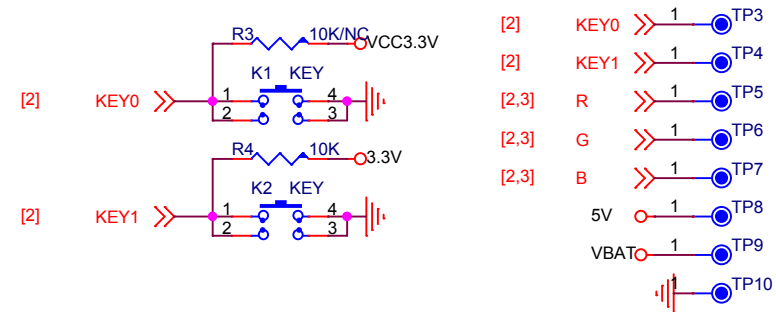
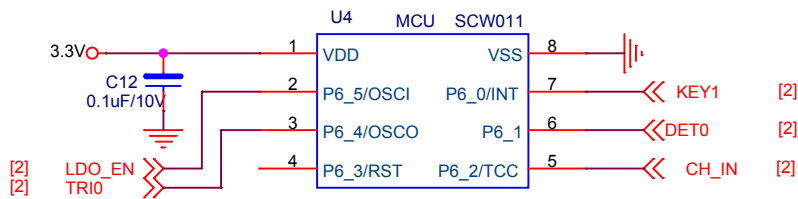
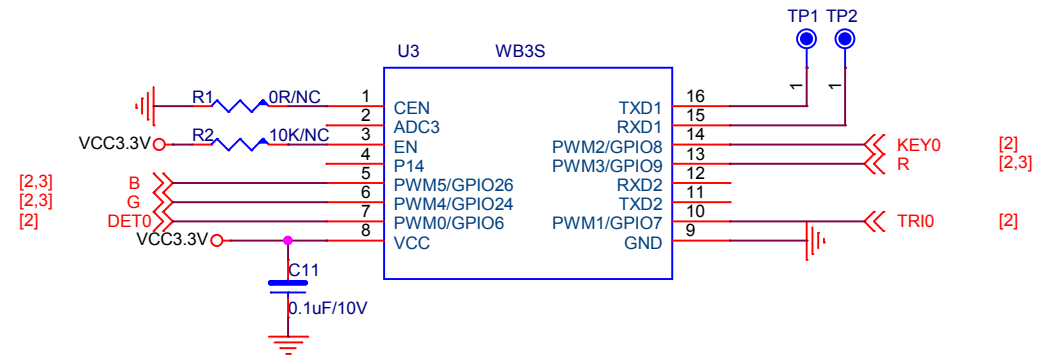
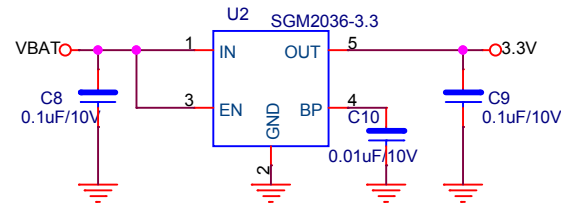
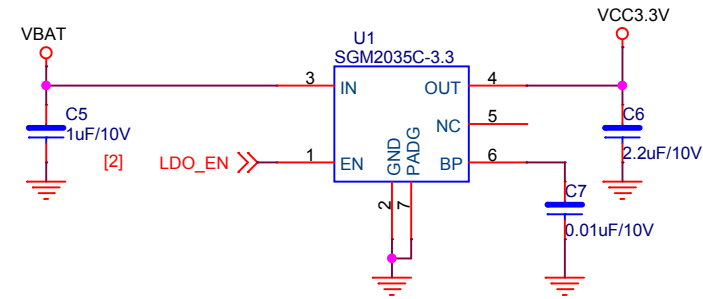
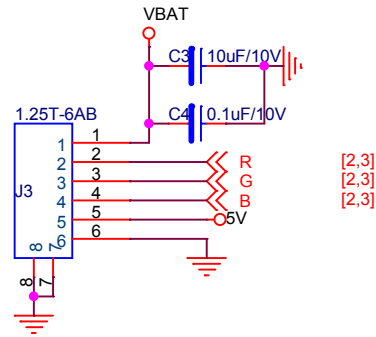
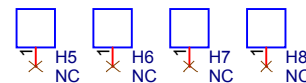
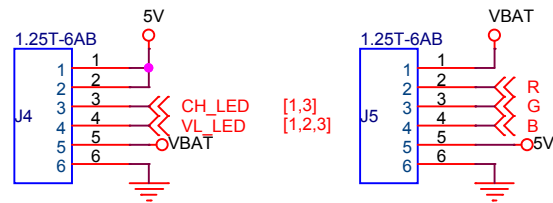




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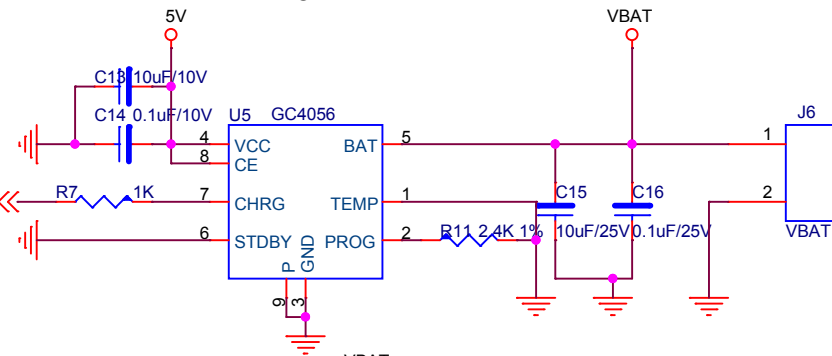


D



[2,3]
[2,3]
[2,3]

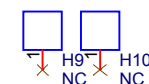
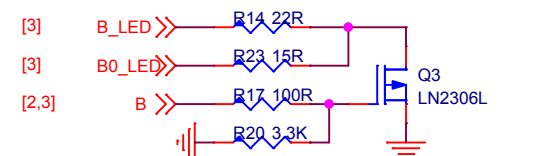
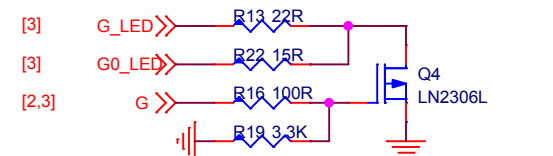
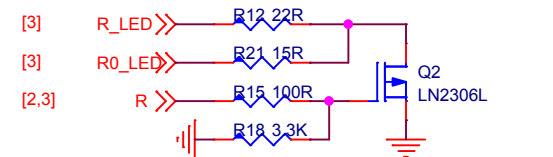
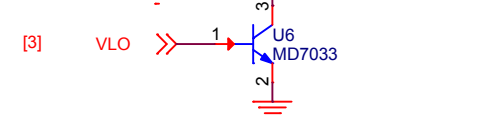
[1,3] CH_LED



[3] VLO >> R5 1K >> VL_LED [1,2,3]

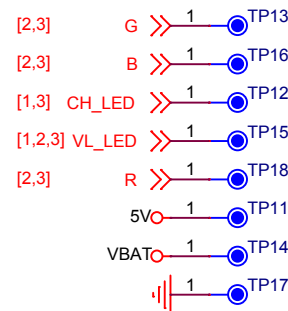
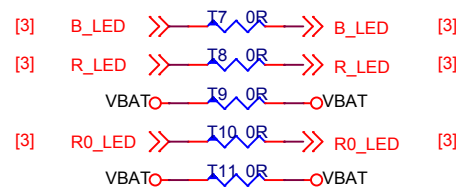
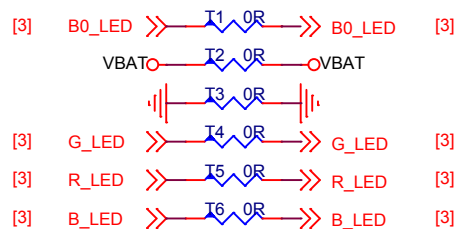
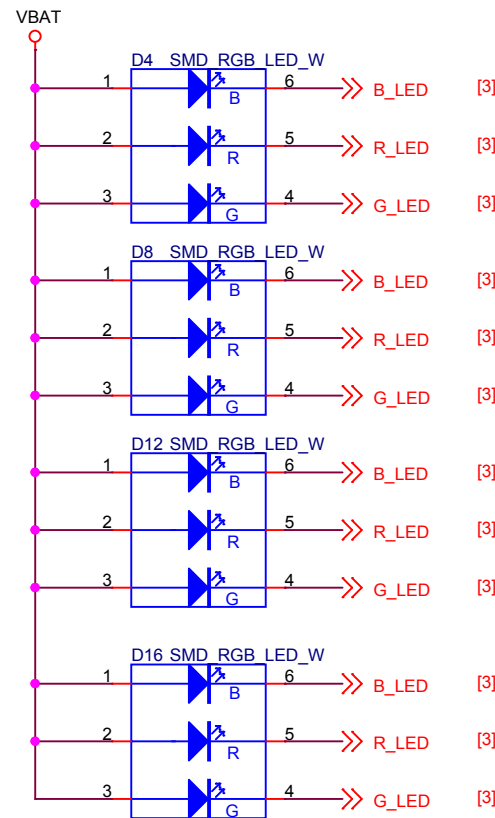
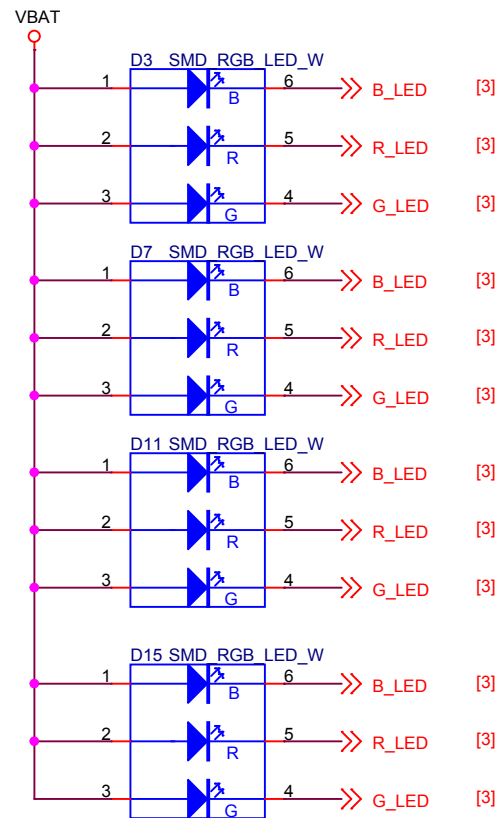
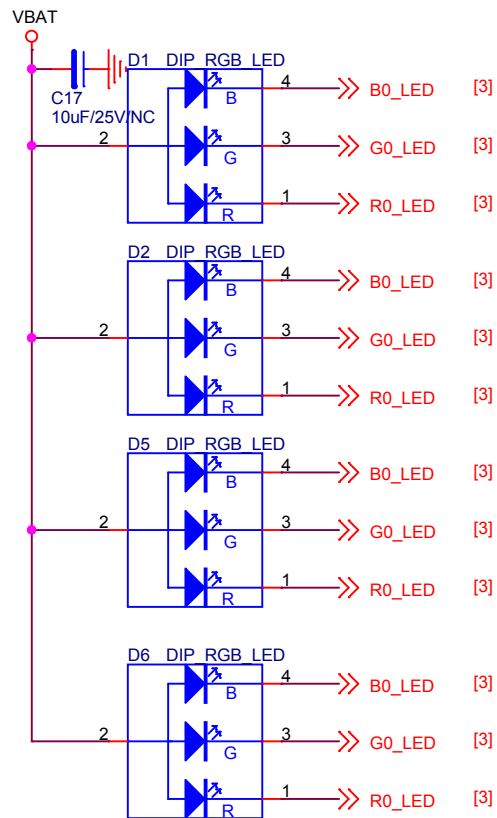
[3] ADC0 >> R6 0R >> VBAT

[3] VLO >> R9 NC >> ADC0 [3]



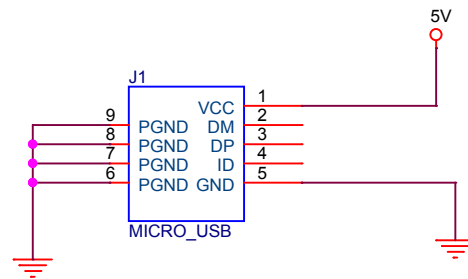
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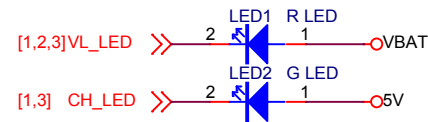
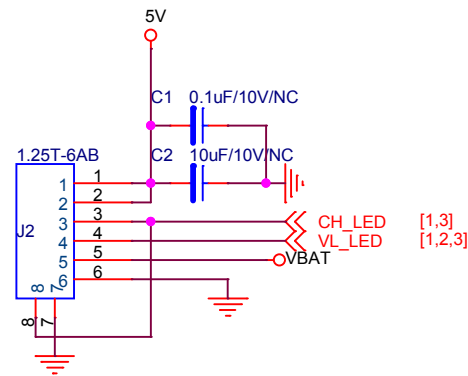


A

D

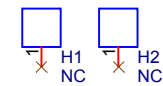


C



B

TP & MARK



A