EC25-AF Hardware Design

Short version

PART OF EC25 LTE Module Series

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About the Document

History

Revision	Date	Author	Description
1.0	2020-08-21	T.Vahtera	Initial version stripped and edited from Quectel version 1.5
1.1	2020-09-07	T.Vahtera	Added FCC and IC notifications
1.2	2020-09-08	T.Vahtera	Corections to regulation part

1 Introduction

This document defines the EC25 module and describes its air interface and hardware interface which are connected with customers' applications.

This document can help customers quickly understand module interface specifications, electrical and mechanical details, as well as other related information of EC25 module. Associated with application note and user guide, customers can use EC25 module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating EC25 module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals supplied with the product. If not so, Quectel assumes no liability for the customers' failure to comply with these precautions.

Full attention must be given to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a hands-free kit) causes distraction and can lead to an accident. You must comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it is switched off. The operation of wireless appliances in an aircraft is forbidden, so as to prevent interference with communication systems. Consult the airline staff about the use of wireless devices on boarding the aircraft, if your device offers an Airplane Mode which must be enabled prior to boarding an aircraft.

Switch off your wireless device when in hospitals, clinics or other health care facilities. These requests are designed to prevent possible interference with sensitive medical equipment.

Cellular terminals or mobiles operating over radio frequency signal and cellular network cannot be guaranteed to connect in all conditions, for example no mobile fee or with an invalid (U)SIM card. While you are in this condition and need emergent help, please remember using emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength.

Your cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency energy. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.

In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

EC25-AF is part of EC25 series of LTE-FDD/LTE-TDD/WCDMA/GSM wireless communication modules which has receive diversity possibility. EC25-AF provides data connectivity on LTE-FDD and WCDMA networks. It also provides optional support for GNSS (GPS, GLONASS, BeiDou/Compass, Galileo, QZSS) and voice functionality (in Telematics version) for customers' specific application. EC25-AF supports following bands LTE FDD: B2/B4//B5/B12/B13/B14/B66/B71 WCDMA: B2/B4/B5.

EC25 series contains six other variants: EC25-E, EC25-A, EC25-V, EC25-J, EC25-AU, EC25-AUT and EC25-AUTL. Customers can choose a dedicated type based on the region or operator.

With a compact profile of 29.0mm × 32.0mm × 2.4mm, EC25 family can meet almost all requirements for M2M applications such as automotive, metering, tracking system, security, router, wireless POS, mobile computing device, PDA phone, tablet PC, etc.

EC25 family is an SMD type module which can be embedded into applications through its 144-pin pads, including 80 LCC signal pads and 64 LGA pads.

2.2. Key Features

The following table describes the detailed features of module.

Table 2: Key Features of EC25 Module

Feature	Details
Power Supply	Supply voltage: 3.3V~4.3V Typical supply voltage: 3.8V
Transmitting Power	Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2dB) for LTE-FDD bands
LTE Features	Support up to non-CA Cat 4 FDD and TDD Support 1.4MHz~20MHz RF bandwidth Support MIMO in DL direction LTE-FDD: Max 150Mbps (DL)/50Mbps (UL)
UMTS Features	Support WCDMA Support QPSK, 16-QAM and 64-QAM modulation WCDMA: Max 384Kbps (DL)/384Kbps (UL)
Internet Protocol Features	Support TCP/UDP/PPP/FTP/HTTP/NTP/PING/QMI/CMUX*/HTTPS*/SMTP*/ MMS*/FTPS*/SMTPS*/SSL*/FILE* protocols Support PAP (Password Authentication Protocol) and CHAP (Challenge Handshake Authentication Protocol) protocols which are usually used for PPP connections
SMS	Text and PDU mode Point to point MO and MT SMS cell broadcast SMS storage: ME by default
(U)SIM Interface	Support USIM/SIM card: 1.8V, 3.0V
Audio Features	Support one digital audio interface: PCM interface WCDMA: AMR/AMR-WB LTE: AMR/AMR-WB Support echo cancellation and noise suppression
PCM Interface	Used for audio function with external codec Support 16-bit linear data format Support long frame synchronization and short frame synchronization Support master and slave modes, but must be the master in long frame synchronization

USB Interface	Compliant with USB 2.0 specification (slave only); the data transfer rate can reach up to 480Mbps Used for AT command communication, data transmission, GNSS NMEA output, software debugging, firmware upgrade and voice over USB*
	Support USB serial drivers for: Windows 7/8/8.1/10, Windows CE 5.0/6.0/7.0*, Linux 2.6/3.x/4.1~4.14, Android 4.x/5.x/6.x/7.x
UART Interface	**Main UART:** Used for AT command communication and data transmission Baud rates reach up to 921600bps, 115200bps by default Support RTS and CTS hardware flow control **Debug** **UART:** Used for Linux console and log output 115200bps baud rate
SD Card Interface	Support SD 3.0 protocol
SGMII Interface	Support 10M/100M/1000M Ethernet work mode Support maximum 150Mbps (DL)/50Mbps (UL) for 4G network
Wireless Connectivity Interfaces	Support a low-power SDIO 3.0 interface for WLAN and UART/PCM interface for Bluetooth*
Rx-diversity	Support LTE/WCDMA Rx-diversity
GNSS Features	Gen8C Lite of Qualcomm Protocol: NMEA 0183
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Network Indication	Two pins including NET_MODE and NET_STATUS to indicate network connectivity status
Antenna Interfaces	Including main antenna interface (ANT_MAIN), Rx-diversity antenna interface (ANT_DIV) and GNSS antenna interface (ANT_GNSS)
Physical Characteristics	Size: (29.0±0.15) mm × (32.0±0.15) mm × (2.4±0.2) mm Weight: approx. 4.9g
Temperature Range	Operation temperature range: -35°C ~ +75°C[1)] Extended temperature range: -40°C ~ +85°C[2)] Storage temperature range: -40°C~ +90°C
Firmware Upgrade	USB interface and DFOTA*
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1] Within operation temperature range, the module is 3GPP compliant.

2. [2] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

2.3. Functional Diagram

The following figure shows a block diagram of EC25 and illustrates the major functional parts.

- Power management
- Baseband
- DDR+NAND flash
- Radio frequency
- Peripheral interfaces

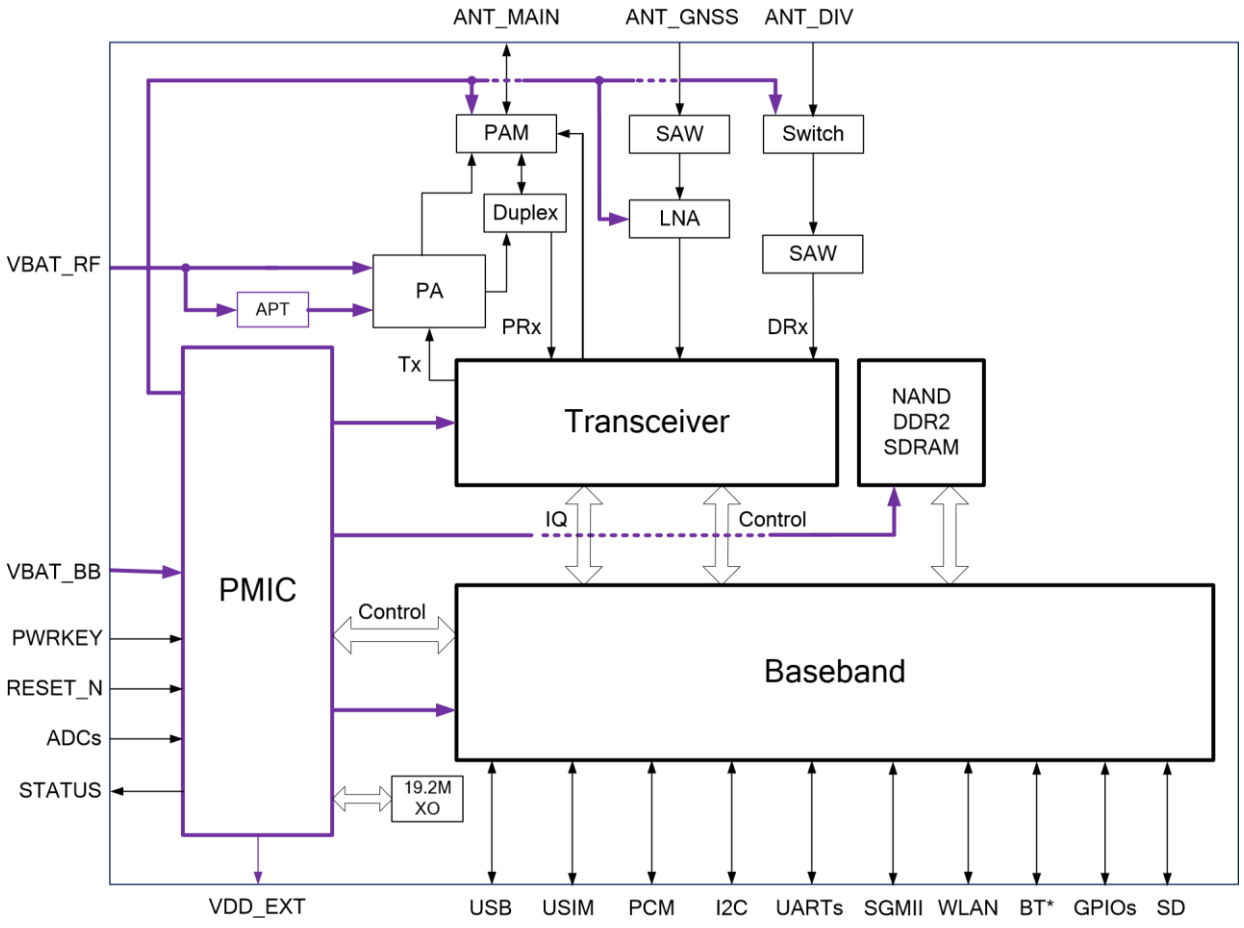

Figure 1: Functional Diagram

NOTE

"*" means under development.

3 Application Interfaces

3.1. General Description

EC25 is equipped with 80 LCC pads plus 64 LGA pads that can be connected to cellular application platform. Sub-interfaces included in these pads are described in detail in the following chapters:

- Power supply
- (U)SIM interface
- USB interface
- UART interfaces
- PCM and I2C interfaces
- SD card interface
- ADC interfaces
- Status indication
- SGMII interface
- Wireless connectivity interfaces
- USB_BOOT interface

3.2. Pin Assignment

The following figure shows the pin assignment of EC25 module.

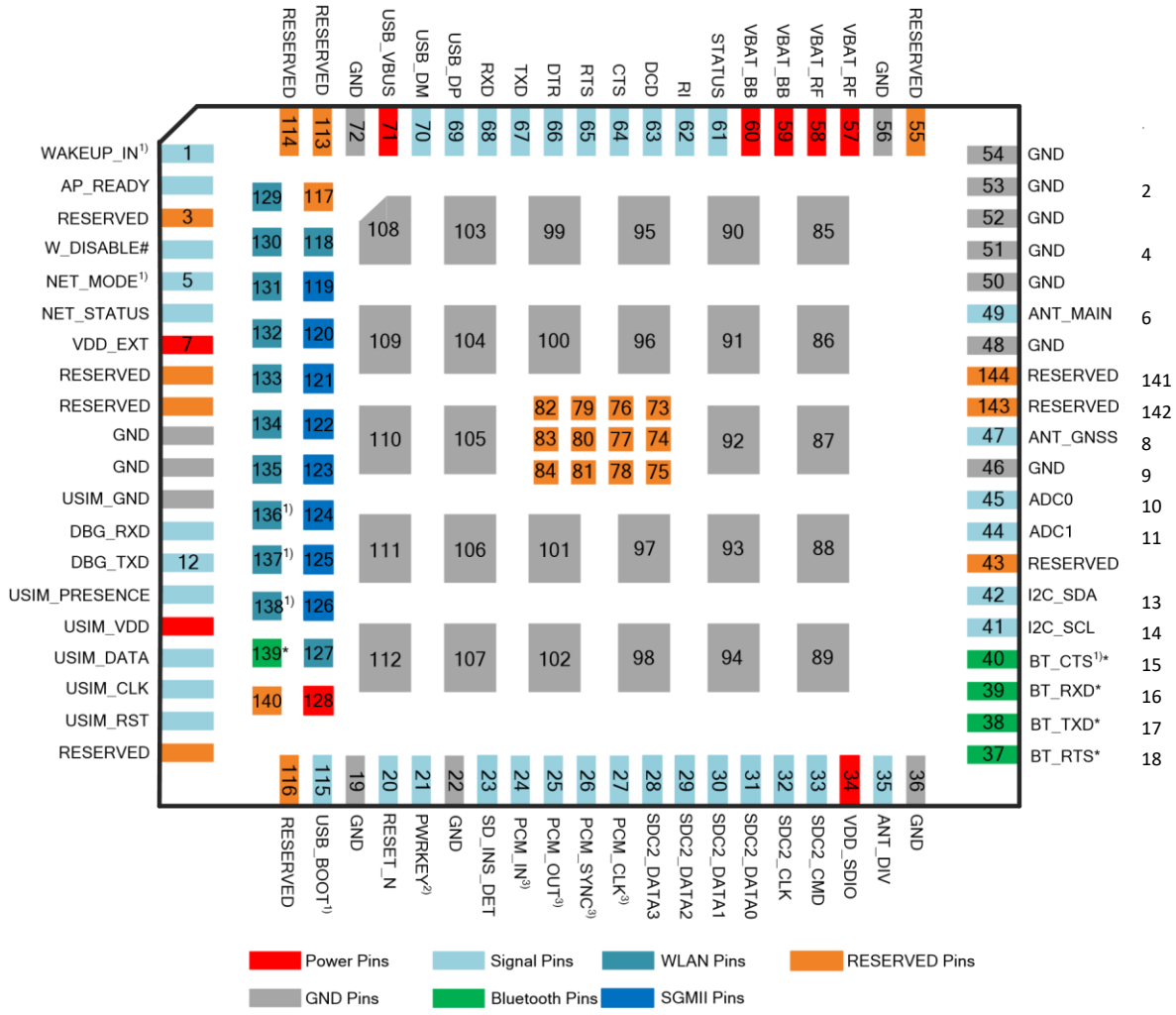

Figure 2: Pin Assignment (Top View)

NOTES

1. 1) means that these pins cannot be pulled up before startup.
2. 2) PWRKEY output voltage is 0.8V because of the diode drop in the Qualcomm chipset.
3. 3) means these interface functions are only supported on **Telematics** version.
4. Pads 37~40, 118, 127 and 129~139 are used for wireless connectivity interfaces, among which pads 118, 127 and 129~138 are WLAN function pins, and the rest are Bluetooth (BT) function pins. BT function is under development.
5. Pads 119~126 and 128 are used for SGMII interface.

6. Pads 24~27 are multiplexing pins used for audio design on the EC25 module and BT function on the BT module.
7. Keep all RESERVED pins and unused pins unconnected.
8. GND pads 85~112 should be connected to ground in the design, and RESERVED pads 73~84 should not be designed in schematic and PCB decal, and these pins should be served as a keep out area.
9. "*" means under development.

3.3. Operating Modes

The table below briefly summarizes the various operating modes referred in the following chapters. These are explained in original document.

Table 5: Overview of Operating Modes

Mode	Details
Normal Operation	Software is active. The module has registered on the network, and it is Idle ready to send and receive data.
	Network connection is ongoing. In this mode, the power consumption is Talk/Data decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN** command can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.
Airplane Mode	**AT+CFUN** command or W_DISABLE# pin can set the module to airplane mode. In this case, RF function will be invalid.
Sleep Mode	In this mode, the current consumption of the module will be reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interface is not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.

3.4. Power Supply

3.4.1. Power Supply Pins

EC25 provides four VBAT pins to connect with the external power supply, and there are two separate voltage domains for VBAT.

- Two VBAT_RF pins for module's RF part
- Two VBAT_BB pins for module's baseband part

The following table shows the details of VBAT pins and ground pins.

Table 6: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF	57, 58	Power supply for module's RF part	3.3	3.8	4.3	V
VBAT_BB	59, 60	Power supply for module's baseband part	3.3	3.8	4.3	V
GND	8, 9, 19, 22, 36, 46, 48, 50~54, 56, 72, 85~112	Ground	-	0	-	V

3.6.2. Decrease Voltage Drop

The power supply range of the module is from 3.3V to 4.3V. Please make sure that the input voltage will never drop below 3.3V. The following figure shows the voltage drop during burst transmission in 2G network. The voltage drop will be less in 3G and 4G networks.

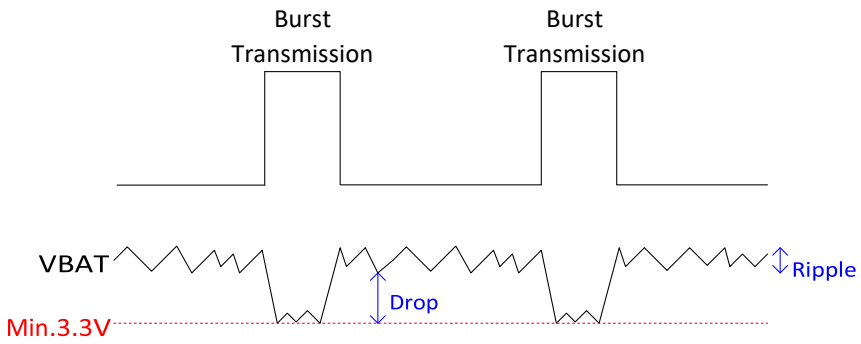

Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100μF with low ESR (ESR=0.7Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It

is recommended to use three ceramic capacitors (100nF, 33pF, 10pF) for composing the MLCC array, and place these capacitors close to VBAT_BB/VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 1mm; and the width of VBAT_RF trace should be no less than 2mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to get a stable power source, it is suggested that a zener diode whose reverse zener voltage is 5.1V and dissipation power is more than 0.5W should be used. The following figure shows the star structure of the power supply.

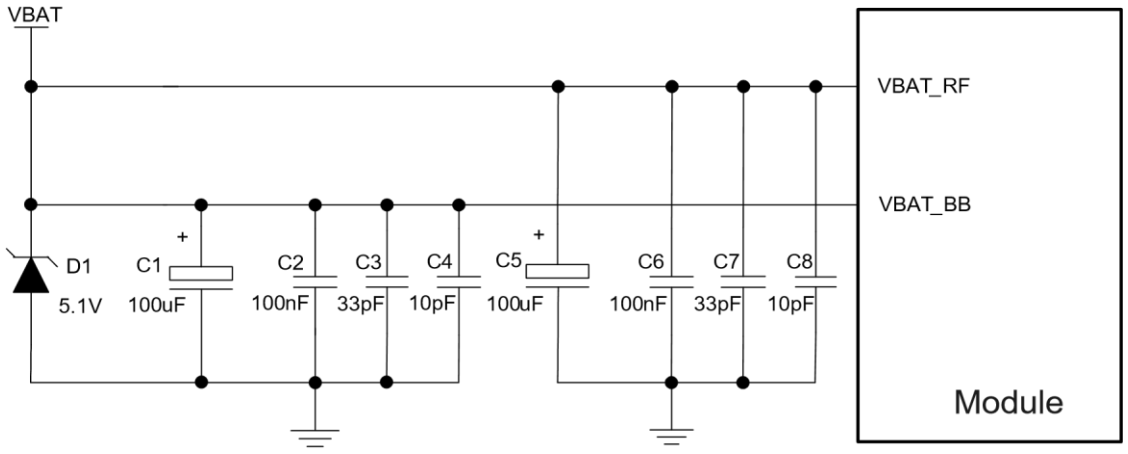

Figure 8: Star Structure of the Power Supply

3.4.3. Reference Design for Power Supply

Power design for the module is very important, as the performance of the module largely depends on the power source. The power supply should be able to provide sufficient current up to 2A at least. If the voltage drop between the input and output is not too high, it is suggested that an LDO should be used to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure shows a reference design for +5V input power source. The typical output of the power supplies about 3.8V and the maximum load current is 3A.

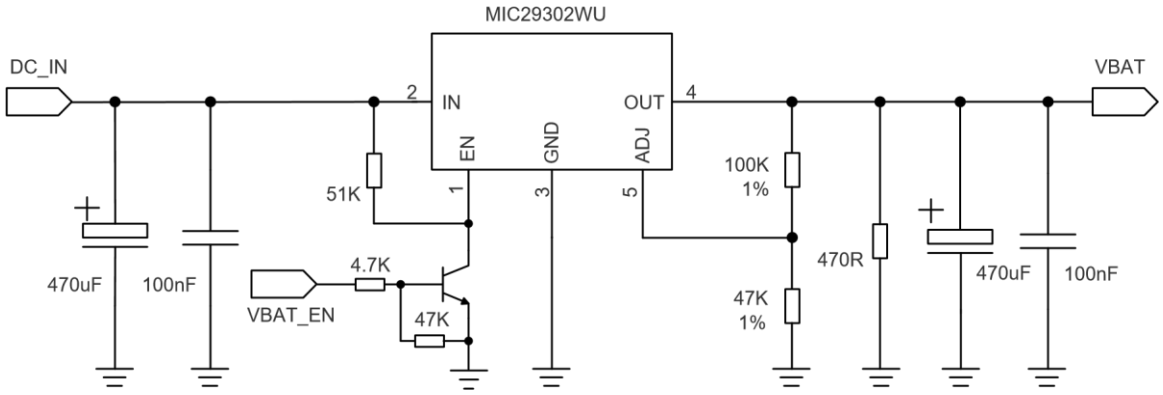

Figure 9: Reference Circuit of Power Supply

NOTE

In order to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shutdown by PWRKEY or AT command, then the power supply can be cut off.

3.5. Turn on and off Scenarios

3.5.1. Turn on Module Using the PWRKEY

The following table shows the pin definition of PWRKEY.

Table 7: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	21	DI	Turn on/off the module	The output voltage is 0.8V because of the diode drop in the Qualcomm chipset.

When EC25 is in power down mode, it can be turned on to normal mode by driving the PWRKEY pin to a low level for at least 500ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS pin (require external pull-up) outputting a low level, PWRKEY pin can be released. A simple reference circuit is illustrated in the following figure.

The turn on scenario is illustrated in the following figure.

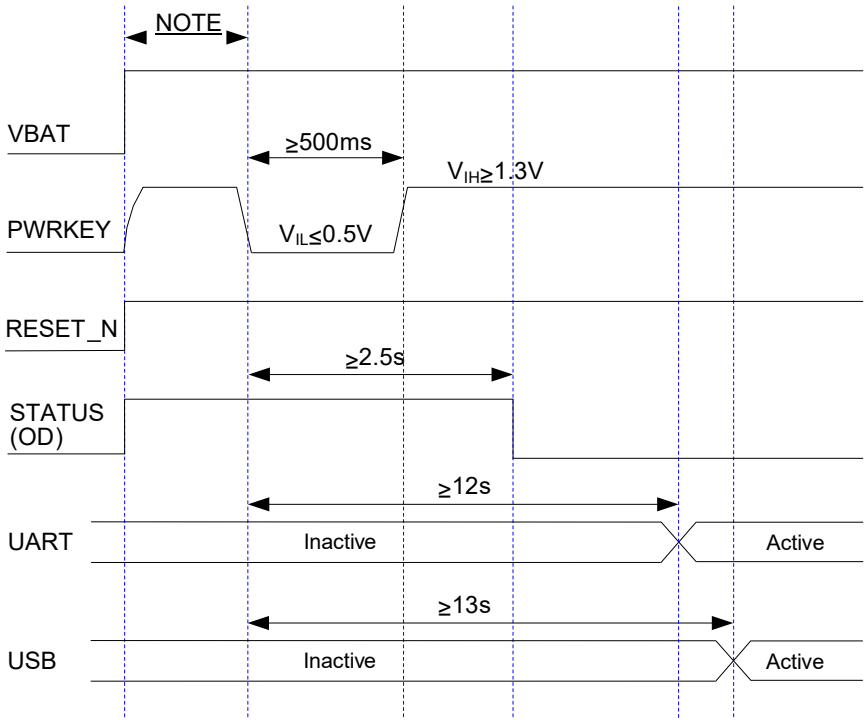

Figure 12: Timing of Turning on Module

NOTE

Please make sure that VBAT is stable before pulling down PWRKEY pin. The time between them should be no no less than 30ms.

3.5.2. Turn off Module

The following procedures can be used to turn off the module:

- Normal power down procedure: Turn off the module using the PWRKEY pin.
- Normal power down procedure: Turn off the module using **AT+QPOWD** command.

3.5.2.1. Turn off Module Using the PWRKEY Pin

Driving the PWRKEY pin to a low level voltage for at least 650ms, the module will execute power-down procedure after the PWRKEY is released. The power-down scenario is illustrated in the following figure.

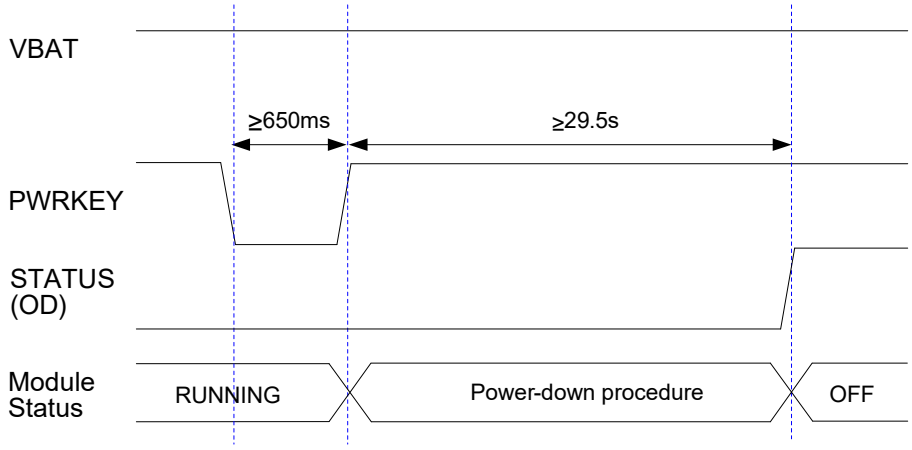

Figure 13: Timing of Turning off Module

3.5.2.2. Turn off Module Using AT Command

It is also a safe way to use **AT+QPOWD** command to turn off the module, which is similar to turning off the module via PWRKEY pin.

Please refer to ***document [2]*** for details about **AT+QPOWD** command.

NOTES

1. Inorder to avoid damaging internal flash, please do not switch off the power supply when the module works normally. Only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.
2. When turn off module with AT command, please keep PWRKEY at high level after the execution of power-off command. Otherwise the module will be turned on again after successfully turn-off.

3.6. Reset the Module

The RESET_N pin can be used to reset the module. The module can be reset by driving RESET_N to a low level voltage for time between 150ms and 460ms.

Table 8: RESET_N Pin Description

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	20	DI	Reset the module	1.8V power domain

The reset scenario is illustrated inthe following figure.

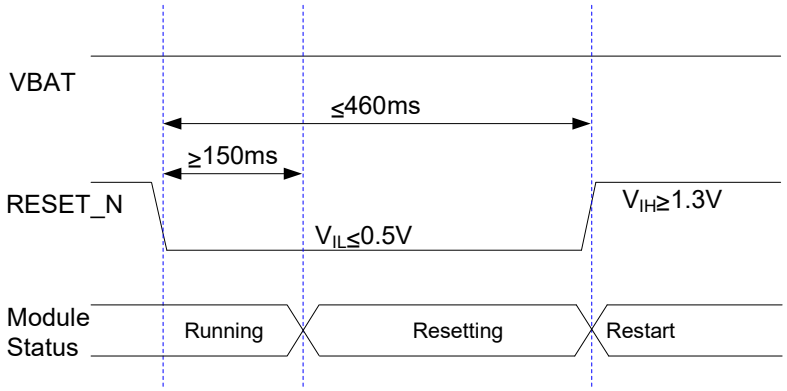

Figure 16: Timing of Resetting Module

NOTES

1. Use RESET_N only when turning off the module by **AT+QPOWD** command and PWRKEY pin failed.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.7. (U)SIM Interface

The(U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8V and 3.0V (U)SIM cards are supported.

Table 9: Pin Definition of the (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	Power supply for (U)SIM card	Either 1.8V or 3.0V is supported by the module automatically.
USIM_DATA	15	IO	Data signal of (U)SIM card	
USIM_CLK	16	DO	Clock signal of (U)SIM card	
USIM_RST	17	DO	Reset signal of (U)SIM card	
USIM_ PRESENCE	13	DI	(U)SIM card insertion detection	
USIM_GND	10		Specified ground for (U)SIM card	

EC25 supports (U)SIM card hot-plug via the USIM_PRESENCE pin. The function supports low level and high level detections, and it is disabled by default

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

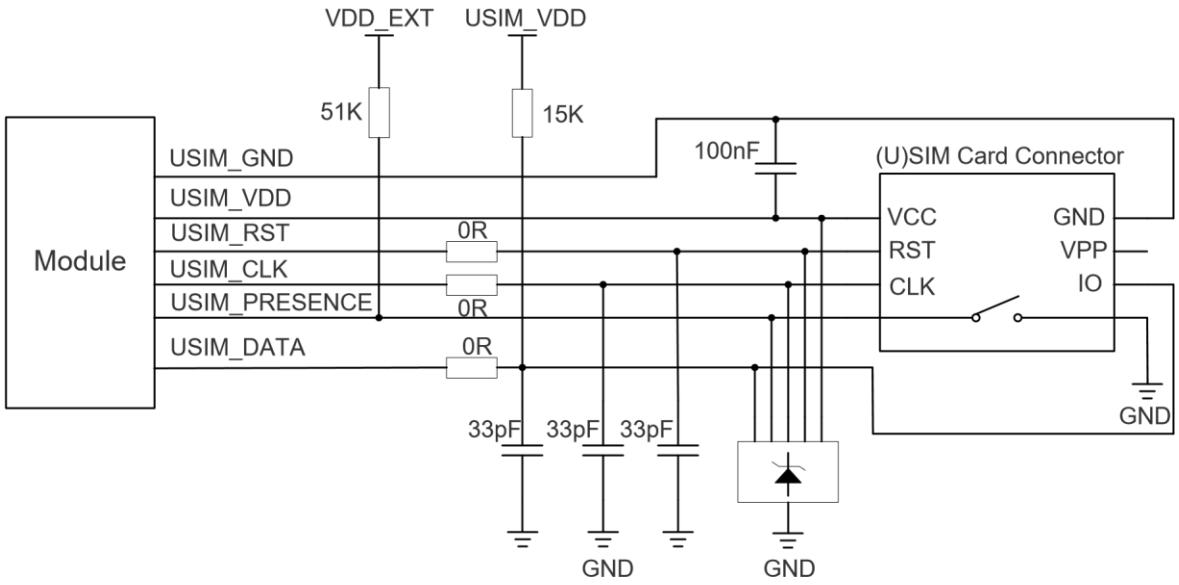

Figure 17: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_PRESENCE unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

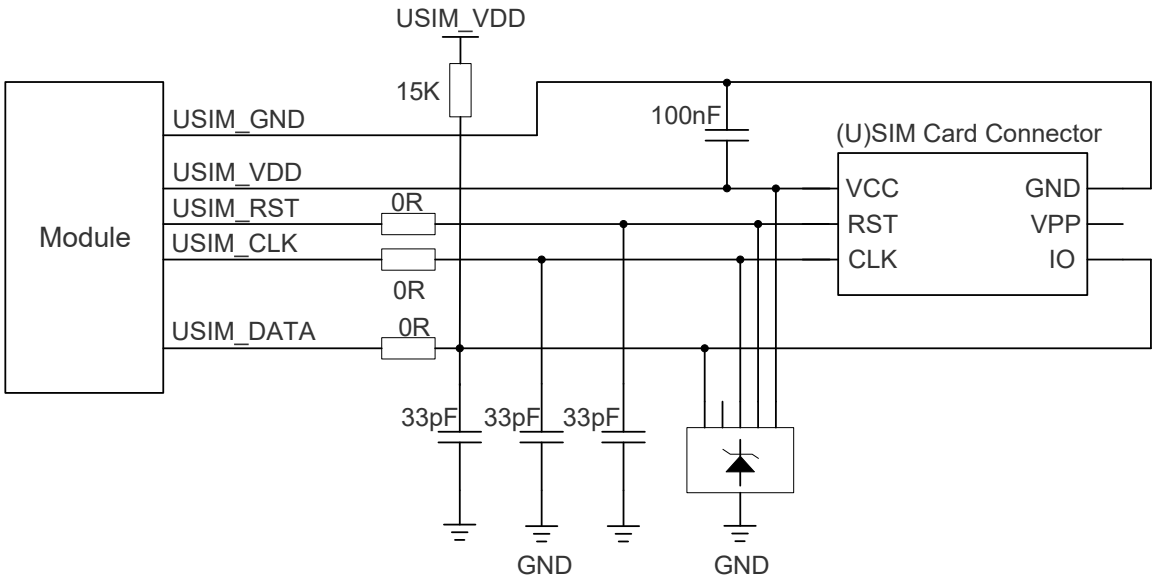

Figure 18: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

In order to enhance the reliability and availability of the (U)SIM card in customers' applications, please follow the criteria below in (U)SIM circuit design:

- Keep placement of (U)SIM card connector to the module as close as possible. Keep the trace length as less than 200mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Assure the ground between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD no less than 0.5mm to maintain the same electric potential. Make sure the bypass capacitor between USIM_VDD and USIM_GND less than 1uF, and place it as close to (U)SIM card connector as possible. If the ground is complete on customers' PCB, USIM_GND can be connected to PCB ground directly.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- In order to offer good ESD protection, it is recommended to add a TVS diode array whose parasitic capacitance should not be more than 15pF. The 0Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33pF capacitors are used for filtering interference of EGSM900. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA line can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and it should be placed close to the (U)SIM card connector.

3.8. USB Interface

EC25 contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480Mbps) and full-speed (12Mbps) modes. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging, firmware upgrade and voice over USB*. The following table shows the pin definition of USB interface.

Table 10: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	69	IO	USB differential data bus (+)	Require differential impedance of 90Ω
USB_DM	70	IO	USB differential data bus (-)	Require differential impedance of 90Ω
USB_VBUS	71	PI	USB connection detection	Typical 5.0V
GND	72		Ground	

For more details about the USB 2.0 specifications, please visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in customers' designs. The following figure shows a reference circuit of USB interface.

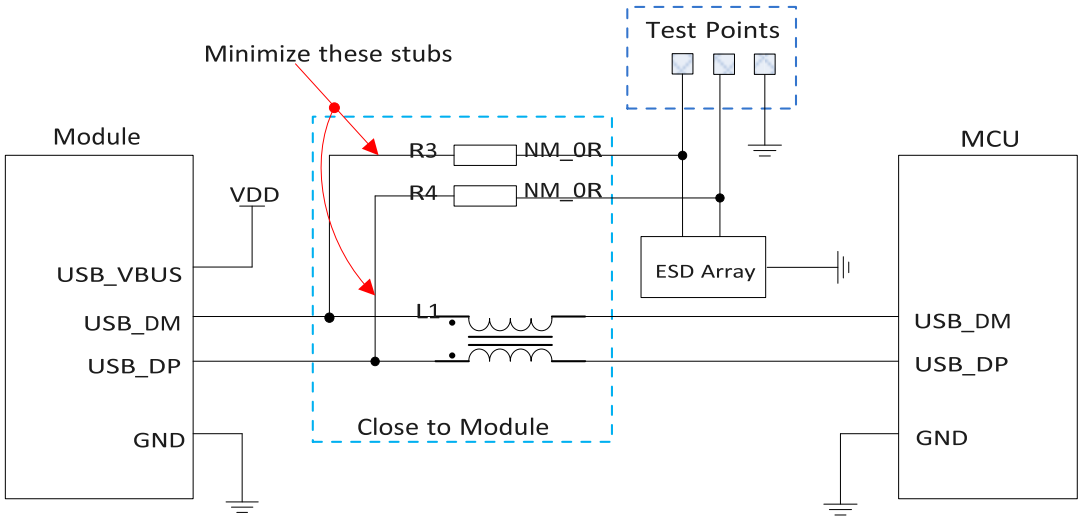

Figure 19: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and customer's MCU in order to suppress EMI spurious transmission. Meanwhile, the 0Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. In order to ensure the integrity of USB data line signal, L1/R3/R4 components must be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles should be complied with when design the USB interface, so as to meet USB 2.0 specification.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2pF.
- Keep the ESD protection components to the USB connector as close as possible.

NOTES

1. EC25 module can only be used as a slave device.
2. "*" means under development.

3.9. UART Interfaces

The module provides two UART interfaces: the main UART interface and the debug UART interface. The following shows their features.

- The main UART interface supports 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps, 460800bps and 921600bps baud rates, and the default is 115200bps. This interface is used for data transmission and AT command communication.
- The debug UART interface supports 115200bps baud rate. It is used for Linux console and log output.

The module provides 1.8V UART interface. A level translator should be used if customers' application is equipped with a 3.3V UART interface. A level translator TXS0108EPWR provided by *Texas Instruments* is recommended. The following figure shows a reference design.

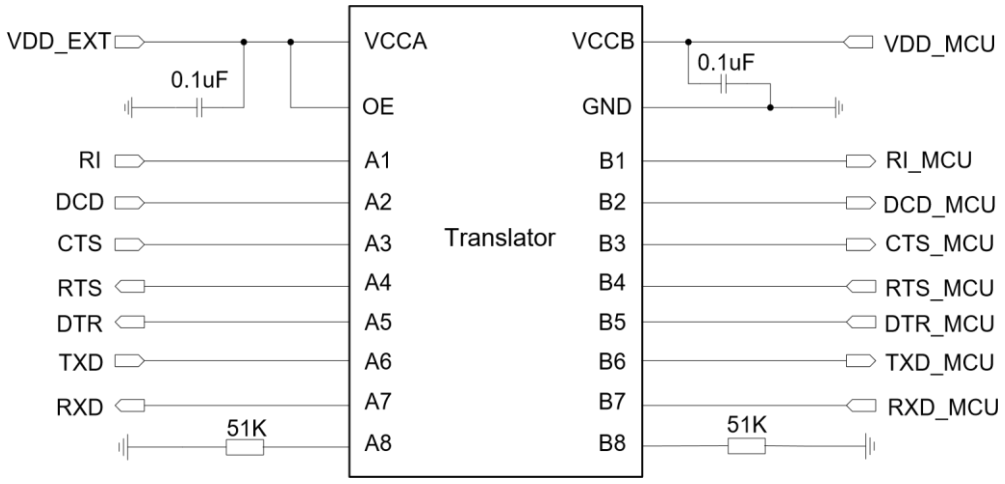

Figure 20: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. The circuit design of dotted line section can refer to the design of solid line section, in terms of both module's input and output circuit designs, but please pay attention to the direction of connection.

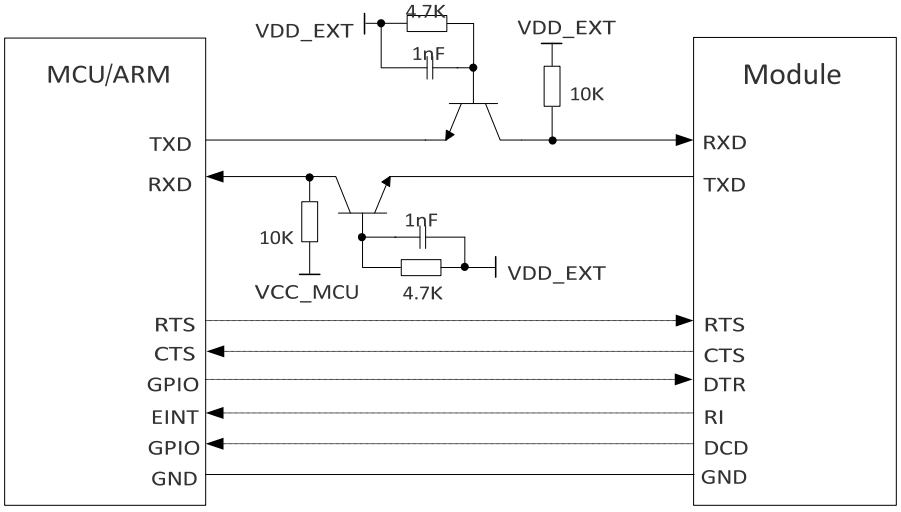

Figure 21: Reference Circuit with Transistor Circuit

NOTE

Transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.

3.10. PCM and I2C Interfaces

EC25 provides one Pulse Code Modulation (PCM) digital interface for audio design, which supports the following modes and one I2C interface:

- Primary mode (short frame synchronization, works as both master and slave)
- Auxiliary mode (long frame synchronization, works as master only)

In primary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256kHz, 512kHz, 1024kHz or 2048kHz PCM_CLK at 8kHz PCM_SYNC, and also supports 4096kHz PCM_CLK at 16kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC rising edge represents the MSB. In this mode, the PCM interface operates with a 256kHz, 512kHz, 1024kHz or 2048kHz PCM_CLK and an 8kHz, 50% duty cycle PCM_SYNC.

EC25 supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8KHz PCM_SYNC and 2048KHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8KHz PCM_SYNC and 256KHz PCM_CLK.

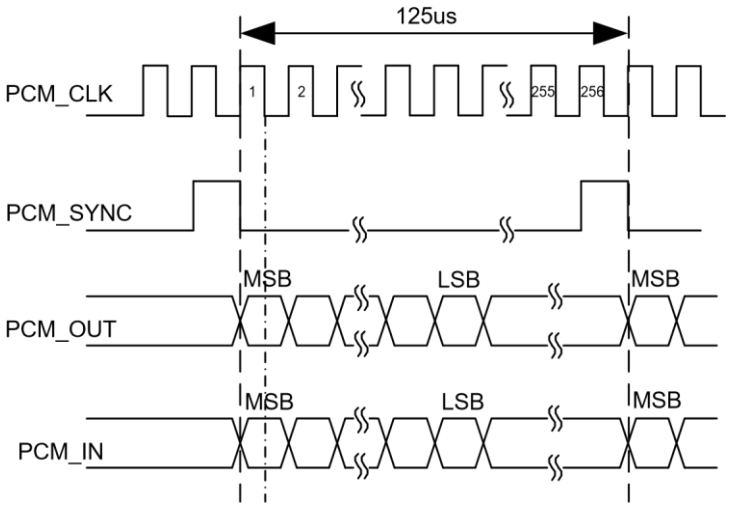

Figure 22: Primary Mode Timing

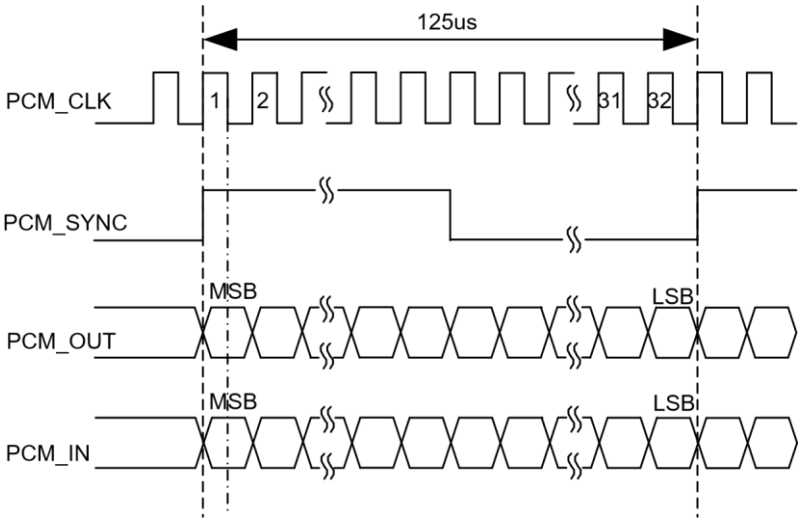

Figure 23: Auxiliary Mode Timing

The following table shows the pin definition of PCM and I2C interfaces which can be applied on audio codec design.

Table 14: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_IN	24	DI	PCM data input	1.8V power domain
PCM_OUT	25	DO	PCM data output	1.8V power domain
PCM_SYNC	26	IO	PCM data frame synchronization signal	1.8V power domain
PCM_CLK	27	IO	PCM data bit clock	1.8V power domain
I2C_SCL	41	OD	I2C serial clock	Require external pull-up to 1.8V
I2C_SDA	42	OD	I2C serial data	Require external pull-up to 1.8V

Clock and mode can be configured by AT command, and the default configuration is master mode using short frame synchronization format with 2048KHz PCM_CLK and 8KHz PCM_SYNC. Please refer to ***document [2]*** for more details about **AT+QDAI** command.

The following figure shows a reference design of PCM interface with external codec IC.

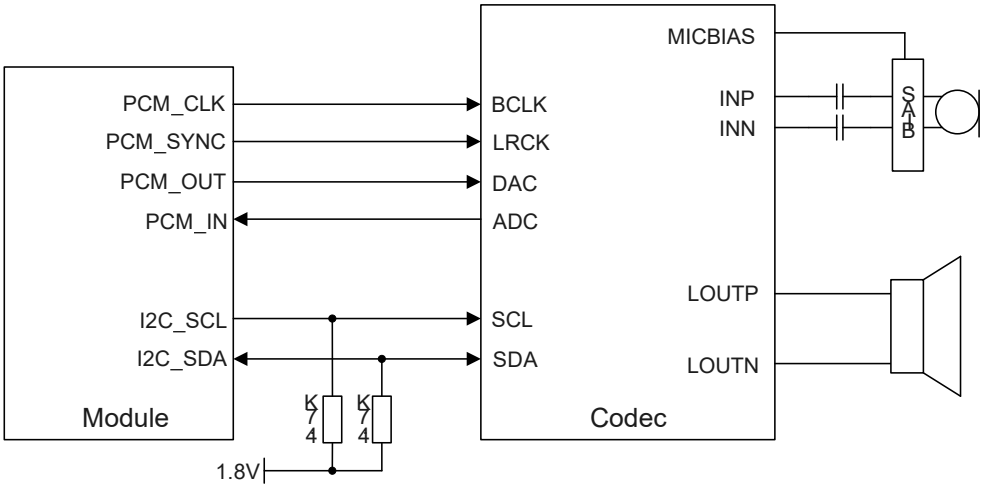

Figure 24: Reference Circuit of PCM Application with Audio Codec

NOTES

1. It is recommended to reserve an RC (R=22 Ω, C= 22pF) circuits on the PCM lines, especially for PCM_CLK.
2. EC25 works as a master device pertaining to I2C interface.

3.11. SD Card Interface

EC25 supports SDIO 3.0 interface for SD card.

The following table shows the pin definition of SD card interface.

Table 15: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SDC2_DATA3	28	IO	SD card SDIO bus DATA3	SDIO signal level can be selected according to SD card supported level, please refer to SD 3.0 protocol for more details. If unused, keep it open.

SDC2_DATA2	29	IO	SD card SDIO bus DATA2	SDIO signal level can be selected according to SD card supported level, please refer to SD 3.0 protocol for more details. If unused, keep it open.
SDC2_DATA1	30	IO	SD card SDIO bus DATA1	SDIO signal level can be selected according to SD card supported level, please refer to SD 3.0 protocol for more details. If unused, keep it open.
SDC2_DATA0	31	IO	SD card SDIO bus DATA0	SDIO signal level can be selected according to SD card supported level, please refer to SD 3.0 protocol for more details. If unused, keep it open.
SDC2_CLK	32	DO	SD card SDIO bus clock	SDIO signal level can be selected according to SD card supported level, please refer to SD 3.0 protocol for more details. If unused, keep it open.
SDC2_CMD	33	IO	SD card SDIO bus command	SDIO signal level can be selected according to SD card supported level, please refer to SD 3.0 protocol for more details. If unused, keep it open.
VDD_SDIO	34	PO	SD card SDIO bus pull up power	1.8V/2.85V configurable. Cannot be used for SD card power. If unused, keep it open.
SD_INS_DET	23	DI	SD card insertion detection	1.8V power domain. If unused, keep it open.

The following figure shows a reference design of SD card.

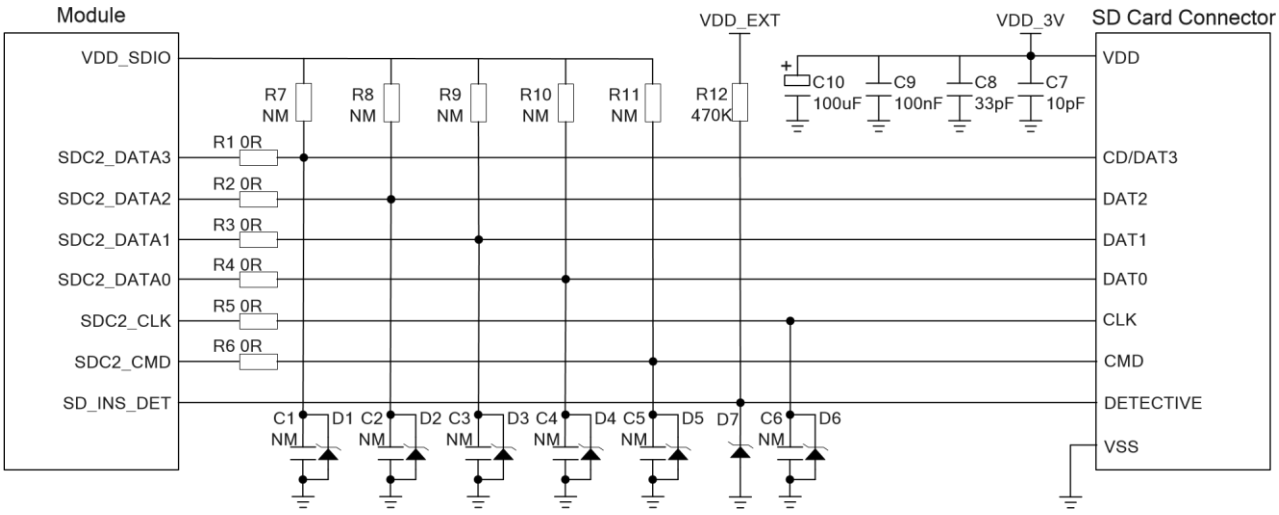

Figure 25: Reference Circuit of SD card

In SD card interface design, in order to ensure good communication performance with SD card, the following design principles should be complied with:

- SD_INS_DET must be connected.
- The voltage range of SD card power supply VDD_3V is 2.7V~3.6V and a sufficient current up to 0.8A should be provided. As the maximum output current of VDD_SDIO is 50mA which can only be used for SDIO pull-up resistors, an externally power supply is needed for SD card.
- To avoid jitter of bus, resistors R7~R11 are needed to pull up the SDIO to VDD_SDIO. Value of these resistors is among 10KΩ~100KΩ and the recommended value is 100KΩ. VDD_SDIO should be used as the pull-up power.
- In order to adjust signal quality, it is recommended to add 0Ω resistors R1~R6 in series between the module and the SD card. The bypass capacitors C1~C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- In order to offer good ESD protection, it is recommended to add a TVS diode on SD card pins near the SD card connector with junction capacitance less than 15pF.
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DCDC signals, etc.
- It is important to route the SDIO signal traces with total grounding. The impedance of SDIO data trace is 50Ω (±10%).
- Make sure the adjacent trace spacing is two times of the trace width and the load capacitance of SDIO bus should be less than 15pF.
- It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm and the total routing length less than 50mm. The total trace length inside the module is 27mm, so the exterior total trace length should be less than 23mm.

3.12. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. **AT+QADC=0** command can be used to read the voltage value on ADC0 pin. **AT+QADC=1** command can be used to read the voltage value on ADC1 pin. For more details about these AT commands, please refer to ***document [2]***.

In order to improve the accuracy of ADC, the trace of ADC should be surrounded by ground.

Table 16: Pin Definition of ADC Interfaces

Pin Name	Pin No.	Description
ADC0	45	General purpose analog to digital converter
ADC1	44	General purpose analog to digital converter

The following table describes the characteristic of ADC function.

Table 17: Characteristic of ADC

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0.3		VBAT_BB	V
ADC1 Voltage Range	0.3		VBAT_BB	V
ADC Resolution		15		Bits

NOTES

1. ADC input voltage must not exceed VBAT_BB.
2. It is prohibited to supply any voltage to ADC pins when VBAT is removed.
3. It is recommended to use a resistor divider circuit for ADC application.

3.13. Network Status Indication

The network indication pins can be used to drive network status indication LEDs. The module provides two pins which are NET_MODE and NET_STATUS. The following tables describe the pin definition and logic level changes in different network status.

Table 18: Pin Definition of Network Connection Status/Activity Indicator

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	5	DO	Indicate the module network registration mode.	1.8V power domain Cannot be pulled up before startup
NET_STATUS	6	DO	Indicate the module network activity status.	1.8V power domain

Table 19: Working State of the Network Connection Status/Activity Indicator

Pin Name	Logic Level Changes	Network Status
NET_MODE	Always High	Registered on LTE network
	Always Low	Others
NET_STATUS	Flicker slowly (200ms High/1800ms Low)	Network searching
	Flicker slowly (1800ms High/200ms Low)	Idle
	Flicker quickly (125ms High/125ms Low)	Data transfer is ongoing
	Always High	Voice calling

3.14. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It can be connected to a GPIO of DTE with a pull-up resistor, or as LED indication circuit as below. When the module is turned on normally, the STATUS will present the low state. Otherwise, the STATUS will present high-impedance state.

Table 20: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	61	OD	Indicate the module's operation status	An external pull-up resistor is required. If unused, keep it open.

The following figure shows different circuit designs of STATUS, and customers can choose either one according to customers' application demands.

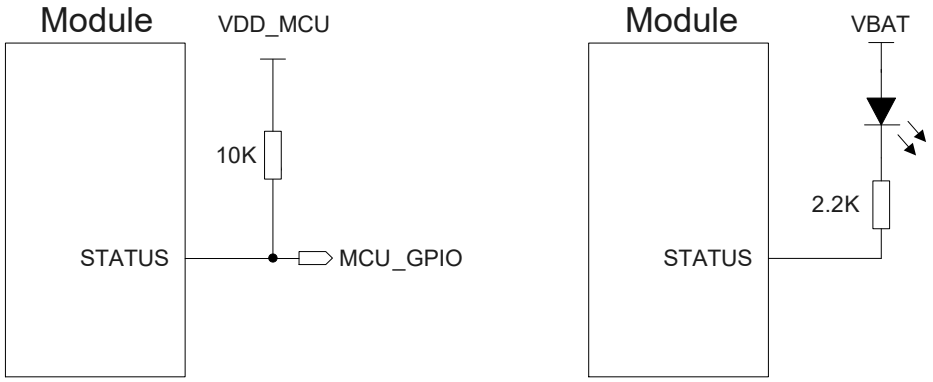

Figure 27: Reference Circuits of STATUS

3.15. SGMII Interface

EC25 includes an integrated Ethernet MAC with an SGMII interface and two management interfaces, key features of the SGMII interface are shown below:

- IEEE802.3 compliance
- Support 10M/100M/1000M Ethernet work mode
- Support maximum 150Mbps (DL)/50Mbps (UL) for 4G network
- Support VLAN tagging
- Support IEEE1588 and Precision Time Protocol (PTP)
- Can be used to connect to external Ethernet PHY like AR8033, or to an external switch
- Management interfaces support dual voltage 1.8V/2.85V

The following table shows the pin definition of SGMII interface.

Table 22: Pin Definition of the SGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
Control Signal Part				
EPHY_RST_N	119	DO	Ethernet PHY reset	1.8V/2.85V power domain
EPHY_INT_N	120	DI	Ethernet PHY interrupt	1.8V power domain
SGMII_MDATA	121	IO	SGMII MDIO (Management Data Input/Output) data	1.8V/2.85V power domain
SGMII_MCLK	122	DO	SGMII MDIO (Management Data Input/Output) clock	1.8V/2.85V power domain
USIM2_VDD	128	PO	SGMII MDIO pull-up power source	Configurable power source. 1.8V/2.85V power domain. External pull-up power source for SGMII MDIO pins.
SGMII Signal Part				
SGMII_TX_M	123	AO	SGMII transmission-minus	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_TX_P	124	AO	SGMII transmission-plus	Connect with a 0.1uF capacitor, close to the PHY side.
SGMII_RX_P	125	AI	SGMII receiving-plus	Connect with a 0.1uF capacitor, close to EC25 module.
SGMII_RX_M	126	AI	SGMII receiving-minus	Connect with a 0.1uF capacitor, close to EC25 module.

The following figure shows the simplified block diagram for Ethernet application.

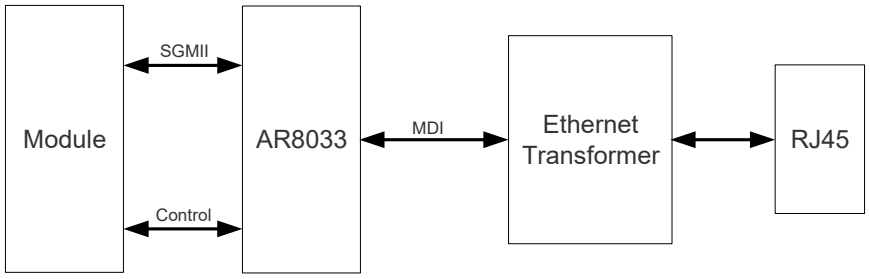

Figure 28: Simplified Block Diagram for Ethernet Application

The following figure shows a reference design of SGMII interface with PHY AR8033 application.

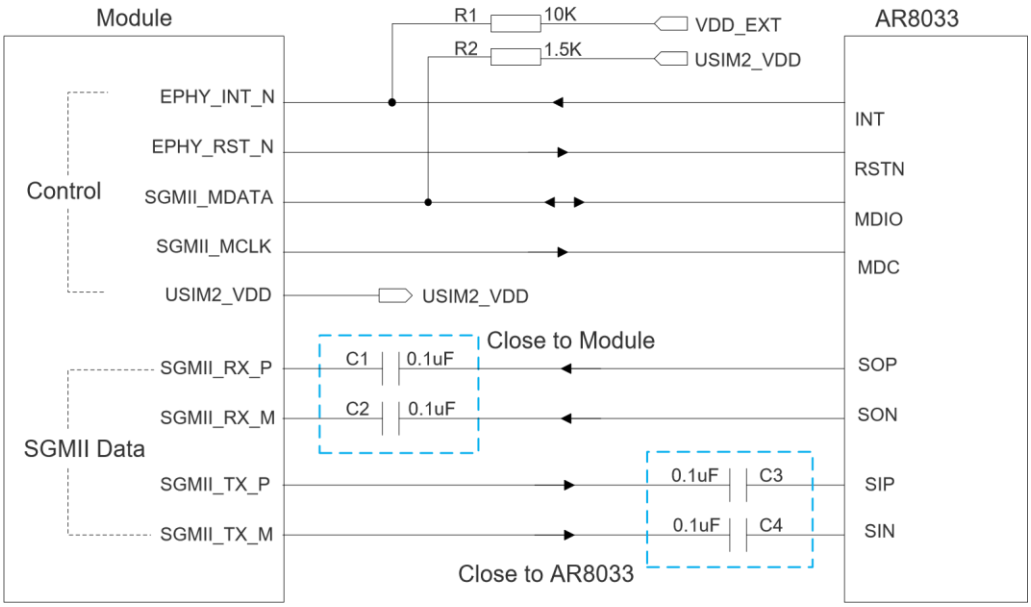

Figure 29: Reference Circuit of SGMII Interface with PHY AR8033 Application

In order to enhance the reliability and availability in customers' applications, please follow the criteria below in the Ethernet PHY circuit design:

- Keep SGMII data and control signals away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DCDC signals, etc.
- Keep the maximum trace length less than 10-inch and keep skew on the differential pairs less than 20mil.
- The differential impedance of SGMII data trace is 100Ω±10%, and the reference ground of the area should be complete.
- Make sure the trace spacing between SGMII RX and TX is at least 3 times of the trace width, and the same to the adjacent signal traces.

3.15. Wireless Connectivity Interfaces

EC25 supports a low-power SDIO 3.0 interface for WLAN and a UART/PCM interface for BT.

The following table shows the pin definition of wireless connectivity interfaces.

Table 23: Pin Definition of Wireless Connectivity Interfaces

Pin Name	Pin No.	I/O	Description	Comment
WLAN Part				
SDC1_DATA3	129	IO	WLAN SDIO data bus D3	1.8V power domain
SDC1_DATA2	130	IO	WLAN SDIO data bus D2	1.8V power domain
SDC1_DATA1	131	IO	WLAN SDIO data bus D1	1.8V power domain
SDC1_DATA0	132	IO	WLAN SDIO data bus D0	1.8V power domain
SDC1_CLK	133	DO	WLAN SDIO bus clock	1.8V power domain
SDC1_CMD	134	IO	WLAN SDIO bus command	1.8V power domain
WLAN_EN	136	DO	WLAN function control via FC20 module.	1.8V power domain. Active high. Cannot be pulled up before startup.
Coexistence and Control Part				
PM_ENABLE	127	DO	External power control	1.8V power domain Active high.
WAKE_ON_ WIRELESS	135	DI	Wake up the host (EC25 module) by FC20 module	1.8V power domain
COEX_UART_RX	137	DI	LTE/WLAN&BT coexistence signal	1.8V power domain. Cannot be pulled up before startup.
COEX_UART_TX	138	DO	LTE/WLAN&BT coexistence signal	1.8V power domain. Cannot be pulled up before startup.
WLAN_SLP_CLK	118	DO	WLAN sleep clock	
BT Part*				

BT_RTS*	37	DI	BT UART request to send	1.8V power domain
BT_TXD*	38	DO	BT UART transmit data	1.8V power domain
BT_RXD*	39	DI	BT UART receive data	1.8V power domain
BT_CTS*	40	DO	BT UART clear to send	1.8V power domain. Cannot be pulled up before startup.
PCM_IN[1)]	24	DI	PCM data input	1.8V power domain
PCM_OUT[1)]	25	DO	PCM data output	1.8V power domain
PCM_SYNC[1)]	26	IO	PCM data frame synchronization signal	1.8V power domain
PCM_CLK[1)]	27	IO	PCM data bit clock	1.8V power domain
BT_EN*	139	DO	BT function control via BT module.	1.8V power domain Active high.

The following figure shows a reference design of wireless connectivity interfaces with Quectel FC20 module.

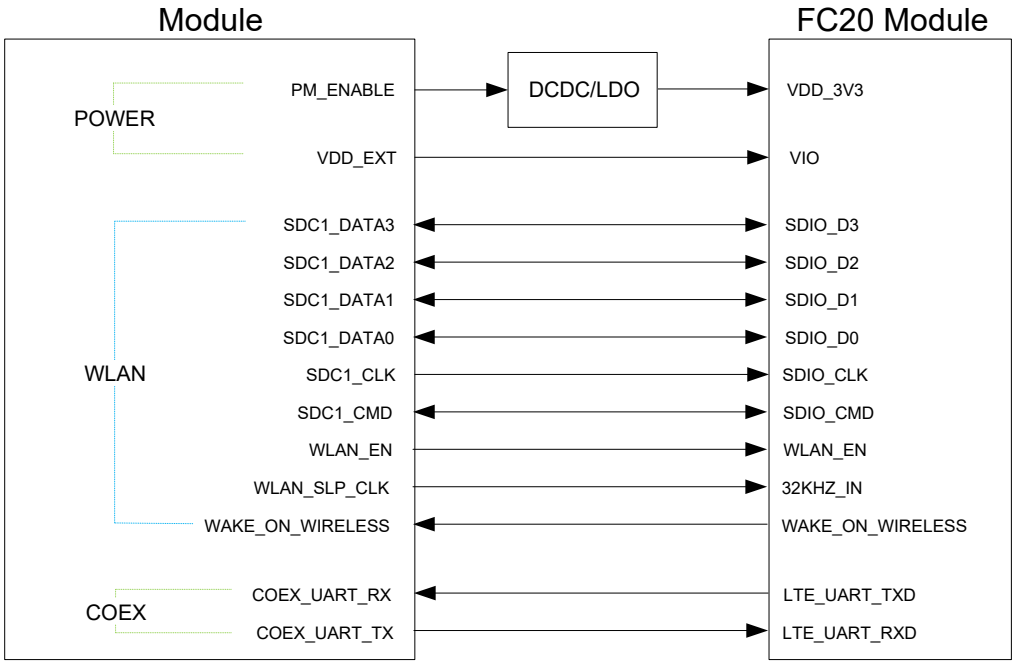

Figure 30: Reference Circuit of Wireless Connectivity Interfaces with FC20 Module

NOTES

1. FC20 module can only be used as a slave device.
2. When BT function is enabled on EC25 module, PCM_SYNC and PCM_CLK pins are only used to output signals.
3. For more information about wireless connectivity interfaces, please refer to ***document [5]***.
4. "*" means under development.
5. [1] Pads 24~27 are multiplexing pins used for audio design on EC25 module and BT function on BT module.

3.16. USB_BOOT Interface

EC25 provides a USB_BOOT pin. Developers can pull up USB_BOOT to VDD_EXT before powering on the module, thus the module will enter into emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 24: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	115	DI	Force the module enter into emergency download mode	1.8V power domain. Active high. It is recommended to reserve test point.

The following figure shows a reference circuit of USB_BOOT interface.

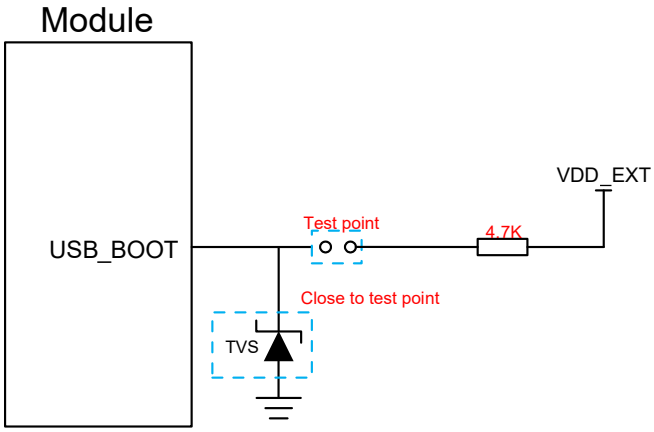

Figure 31: Reference Circuit of USB_BOOT Interface

4 GNSS Receiver

4.1. General Description

EC25 includes a fully integrated global navigation satellite system solution that supports Gen8C-Lite of Qualcomm (GPS, GLONASS, BeiDou, Galileo and QZSS).

EC25 supports standard NMEA-0183 protocol, and outputs NMEA sentences at 1Hz data update rate via USB interface by default.

By default, EC25 GNSS engine is switched off. It has to be switched on via AT command. For more details about GNSS engine technology and configurations, please refer to ***document [3]***.

4.2. GNSS Performance

The following table shows GNSS performance of EC25.

Table 25: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF (GNSS)	Cold start @open sky	Autonomous	35	s
		XTRA enabled	18	s
	Warm start @open sky	Autonomous	26	s
		XTRA enabled	2.2	s
	Hot start @open sky	Autonomous	2.5	s
		XTRA enabled	1.8	s

Accuracy (GNSS)	CEP-50	Autonomous @open sky	<1.5	m

NOTES

1. Tracking sensitivity: the lowest GNSSsignal value at the antenna port on which the module can keep on positioning for 3 minutes.
2. Reacquisition sensitivity: the lowest GNSS signal value at the antenna port on which the module can fix position again within 3 minutes after loss of lock.
3. Cold start sensitivity: the lowest GNSS signal value at the antenna port on which the module fixes position within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in customers' designs.

- Maximize the distance among GNSS antenna, main antenna and Rx-diversity antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module and display connector should be kept away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50Ω characteristic impedance for the ANT_GNSS trace.

Please refer to ***Chapter 5*** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

EC25 antenna interfaces include a main antenna interface, an Rx-diversity antenna interface which is used to resist the fall of signals caused by high speed movement and multipath effect, and a GNSS antenna interface. The impedance of the antenna port is 50Ω.

5.1. Main/Rx-diversity Antenna Interfaces

5.1.1. Pin Definition

The pin definition of main antenna and Rx-diversityantenna interfaces is shown below.

Table 26: Pin Definition of RF Antenna

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	49	IO	Main antenna pad	50Ω impedance
ANT_DIV	35	AI	Receive diversity antenna pad	50Ω impedance If unused, keep it open.

5.1.2. Operating Frequency

Table 27: Module Operating Frequencies

3GPP Band	Transmit	Receive	Unit
GSM850	824~849	869~894	MHz
EGSM900	880~915	925~960	MHz
DCS1800	1710~1785	1805~1880	MHz
PCS1900	1850~1910	1930~1990	MHz
WCDMA B1	1920~1980	2110~2170	MHz
WCDMA B2	1850~1910	1930~1990	MHz
WCDMA B4	1710~1755	2110~2155	MHz
WCDMA B5	824~849	869~894	MHz
WCDMA B6	830~840	875~885	MHz
WCDMA B8	880~915	925~960	MHz
WCDMA B19	830~845	875~890	MHz
LTE FDD B1	1920~1980	2110~2170	MHz
LTE FDD B2	1850~1910	1930~1990	MHz
LTE FDD B3	1710~1785	1805~1880	MHz
LTE FDD B4	1710~1755	2110~2155	MHz
LTE FDD B5	824~849	869~894	MHz

LTE FDD B7	2500~2570	2620~2690	MHz
LTE FDD B8	880~915	925~960	MHz
LTE FDD B12	699~716	729~746	MHz
LTE FDD B13	777~787	746~756	MHZ
LTE FDD B14	788~798	758~768	MHZ
LTE FDD B18	815~830	860~875	MHz
LTE FDD B19	830~845	875~890	MHz
LTE FDD B20	832~862	791~821	MHz
LTE FDD B28	703~748	758~803	MHz
LTE TDD B38	2570~2620	2570~2620	MHz
LTE TDD B40	2300~2400	2300~2400	MHz
LTE TDD B41	2555~2655	2555~2655	MHz
LTE TDD B66	1710~1780	2100~2200	MHz
LTE TDD B71	663~698	617~652	MHz

5.1.3. Reference Design of RF Antenna Interface

A reference design of ANT_MAIN and ANT_DIV antenna pads is shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

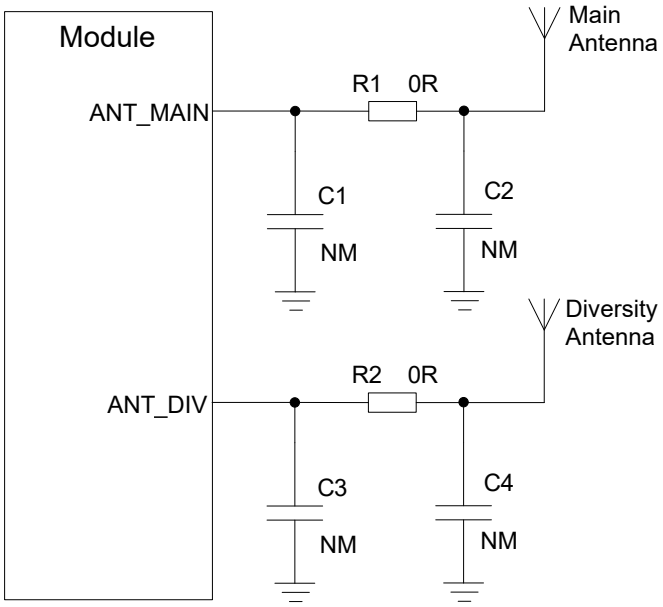

Figure 32: Reference Circuit of RF Antenna Interface

NOTES

1. Keep a proper distance between the main antenna and the Rx-diversity antenna to improve the receiving sensitivity.
2. ANT_DIV function is enabled by default.
3. Place the π-type matching components (R1 &C1&C2, R2 &C3&C4) as close to the antenna as possible.

5.1.4. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the distance between signal layer and reference ground (H), and the clearance between RF trace and ground (S). Microstrip line or coplanar waveguide line is typically used in RF layout for characteristic impedance control. The following are reference designs of microstrip line or coplanar waveguide line with different PCB structures

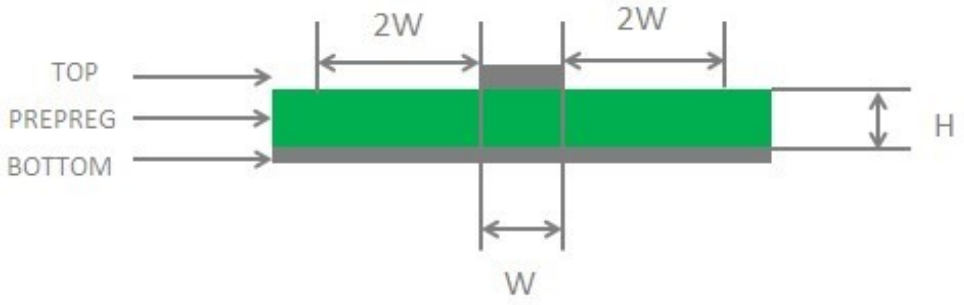

Figure 33: Microstrip Line Design on a 2-layer PCB

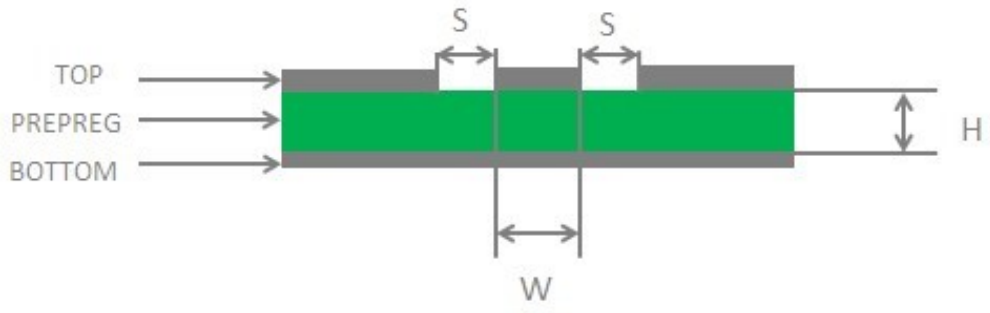

Figure 34: Coplanar Waveguide Line Design on a 2-layer PCB

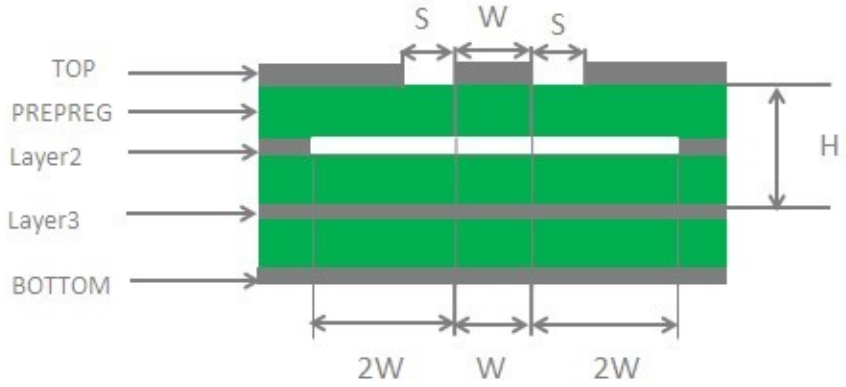

Figure 35: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground)

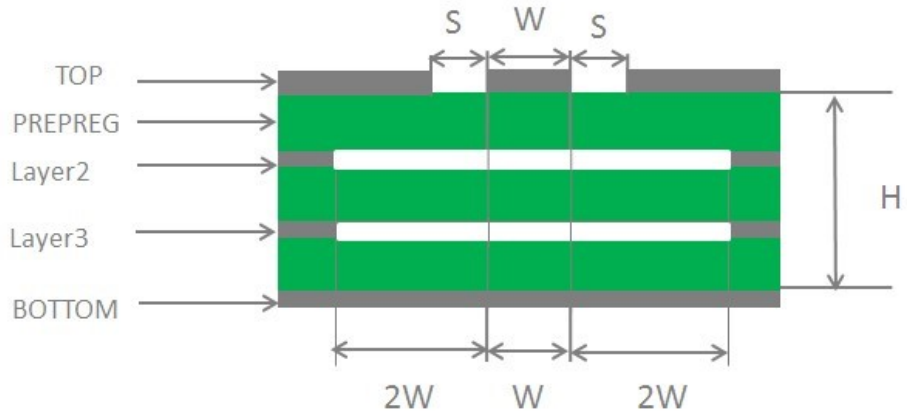

Figure 36: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Please use an impedance simulation tool to control the characteristic impedance of RF traces as 50Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and they should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right angle traces should be changed to curved ones.
- There should be clearance area under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2*W).

For more details about RF layout, please refer to ***document [6]***.

5.2. GNSS Antenna Interface

The following tables show pin definition and frequency specification of GNSS antenna interface.

Table 28: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	47	AI	GNSS antenna	50Ω impedance If unused, keep it open.

Table 29: GNSS Frequency

Type	Frequency	Unit
GPS/Galileo/QZSS	1575.42±1.023	MHz
GLONASS	1597.5~1605.8	MHz
BeiDou	1561.098±2.046	MHz

A reference design of GNSS antenna is shown as below.

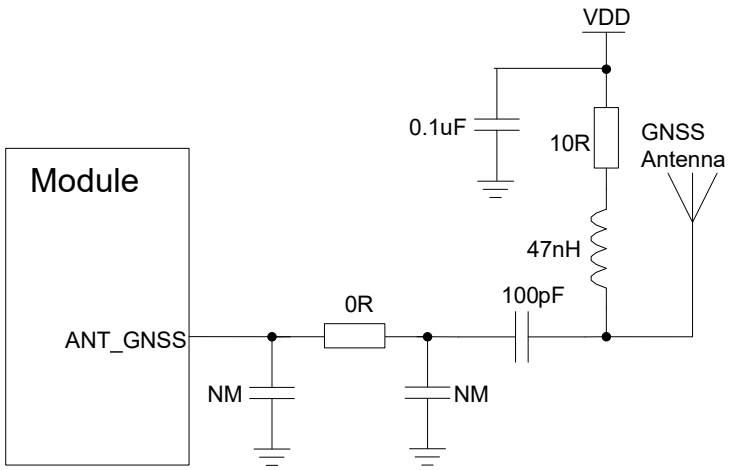

Figure 37: Reference Circuit of GNSS Antenna

NOTES

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. Antenna Installation

5.3.1. Antenna Requirement

The following table shows the requirements on main antenna, Rx-diversity antenna and GNSS antenna.

Table 30: Antenna Requirements

Type	Requirements
GNSS[1)]	Frequency range: 1561MHz~1615MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0dBi Active antenna noise figure: < 1.5dB Active antenna gain: > 0dBi Active antenna embedded LNA gain: < 17 dB
WCDMA/LTE	VSWR: ≤ 2 Efficiency: > 30% Max Input Power: 50W Input Impedance: 50Ω Cable Insertion Loss: < 1dB (WCDMA B5/B6/B8/B19, LTE-FDD B5/B8/B12/B13/B14/B18/B19/B20/B26/B28/B71) Cable Insertion Loss: < 1.5dB (WCDMA B1/B2/B4, LTE-FDD B1/B2/B3/B4/B66) Cable Insertion loss: < 2dB (LTE-FDD B7)

NOTE

[1)] It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

6 Electrical, Reliability and Radio Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 31: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	4.7	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	0	0.8	A
Peak Current of VBAT_RF	0	1.8	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Voltage at ADC1	0	VBAT_BB	V

6.2. Power Supply Ratings

Table 32: The Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.3	V
	Voltage drop during burst transmission	Maximum power control level on EGSM900.			400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level on EGSM900.		1.8	2.0	A
USB_VBUS	USB detection		3.0	5.0	5.25	V

6.3. Operation and Storage Temperatures

The operation and storage temperatures are listed in the following table.

Table 33: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
OperationTemperature Range[1)]	-35	+25	+75	ºC
Extended Operation Range[2)]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1)] Within operation temperature range, the module is 3GPP compliant.
2. [2)] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, emergency call, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

6.4. Current Consumption

The values of current consumption are shown below.

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT}	OFF state	Power down	10	uA
	Sleep state	**AT+CFUN=0** (USB disconnected)	1.0	mA
		WCDMA PF=64 (USB disconnected)	1.8	mA
		WCDMA PF=128 (USB disconnected)	1.4	mA
I_{VBAT}	Idle state	LTE-FDD PF=64 (USB disconnected)	2.2	mA
		LTE-FDD PF=128 (USB disconnected)	1.8	mA
		WCDMA PF=64 (USB disconnected)	23.3	mA
		WCDMA PF=64 (USB connected)	33.4	mA
		LTE-FDD PF=64 (USB disconnected)	17.6	mA
		LTE-FDD PF=64 (USB connected)	29.4	mA
	WCDMA datatransfer (GNSS OFF)	WCDMA B2 HSDPA @22.36dBm	509.0	mA
		WCDMA B2 HSUPA @22.27dBm	511.0	mA
		WCDMA B4 HSDPA @22.22dBm	521.0	mA
		WCDMA B4 HSUPA @22.31dBm	518.0	mA
		WCDMA B5 HSDPA @22.39dBm	496.0	mA
		WCDMA B5 HSUPA @22dBm	502.0	mA
	LTE datatransfer (GNSS OFF)	LTE-FDD B2 @23.2dBm	600.0	mA
		LTE-FDD B4 @23.85dBm	634.0	mA

		LTE-FDD B5 @23.0dBm	600.0	mA
		LTE-FDD B12 @23.08dBm	692.0	mA
		LTE-FDD B13 @23.1dBm	660.0	mA
		LTE-FDD B14 @23.5dBm	676.0	mA
		LTE-FDD B66 @22.9dBm	662.0	mA
		LTE-FDD B71 @22.88dBm	600.0	mA
	WCDMA voice call	WCDMA B2 @23.24dBm	570.0	mA
		WCDMA B4 @23.2dBm	581.0	mA
		WCDMA B5 @23.4dBm	500.0	mA

Table 41: GNSS Current Consumption of EC25 Series Module

Parameter	Description	Conditions	Typ.	Unit
I_{VBAT} (GNSS)	Searching (**AT+CFUN=0**)	Cold start @Passive Antenna	54.0	mA
		Lost state @Passive Antenna	53.9	mA
	Tracking (**AT+CFUN=0**)	Instrument Environment	30.5	mA
		Open Sky @Passive Antenna	33.2	mA
		Open Sky @Active Antenna	40.8	mA

6.5. RF Output Power

The following table shows the RF output power of EC25 module.

Table 42: RF Output Power

Frequency	Max.	Min.
WCDMA bands	24dBm+1/-3dB	<-49dBm
LTE-FDD bands	23dBm±2dB	<-39dBm

NOTE

In GPRS 4 slots TX mode, the maximum output power is reduced by 3dB. The design conforms to the GSM specification as described in ***Chapter 13.16*** of *3GPP TS 51.010-1*.

6.6. RF Receiving Sensitivity

The following table show conducted RF receiving sensitivity of module.

Frequency	Primary	Diversity	SIMO[1)]	3GPP (SIMO)
WCDMA B2	-109.5dBm	-111dbm	-113dbm	-104.7dBm
WCDMA B4	-108dBm	-111dbm	-111.5dbm	-106.7dBm
WCDMA B5	-110.5dBm	-111.5dbm	-114dbm	-104.7dBm
LTE-FDD B2 (10M)	-98.2dBm	-99.1dBm	-101.7dBm	-94.3dBm
LTE-FDD B4 (10M)	-97.3dBm	-98.6dBm	-101.1dBm	-96.3dBm
LTE-FDD B5 (10M)	-99dBm	-100.3dBm	-101.3dBm	-94.3Bm
LTE-FDD B12 (10M)	-99dBm	-99.2dBm	-102.1dBm	-93.3dBm

LTE-FDD B13 (10M)	-98.1dBm	-98.4dBm	-100.2dBm	-93.3dBm
LTE-FDD B14 (10M)	-97.9dBm	-98.6dBm	-99.5dBm	-93.3dBm
LTE-FDD B66 (10M)	-96.7dBm	-98.1dBm	-99.4dBm	-96.5dBm
LTE-FDD B71 (10M)	-99.2dBm	-99.4dBm	-101.5dBm	-94.2dBm

NOTE

[1] SIMO is a smart antenna technology that uses a single antenna at the transmitter side and two antennas at the receiver side, which can improve RX performance.

6.7. Electrostatic Discharge

The module is not protected against electrostatics discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates the module.

The following table shows the module electrostatics discharge characteristics.

Table 51: Electrostatics Discharge Characteristics

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

7 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm. The tolerances for dimensions without tolerance values are ±0.05mm.

7.1. Mechanical Dimensions of the the Module

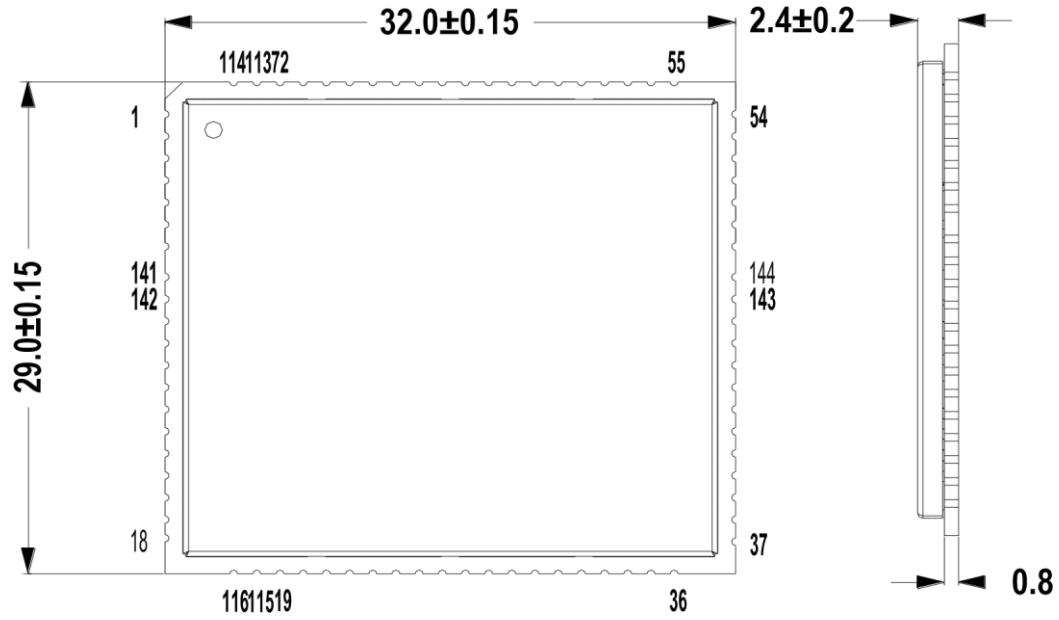

Figure 43: Module Top and Side Dimensions

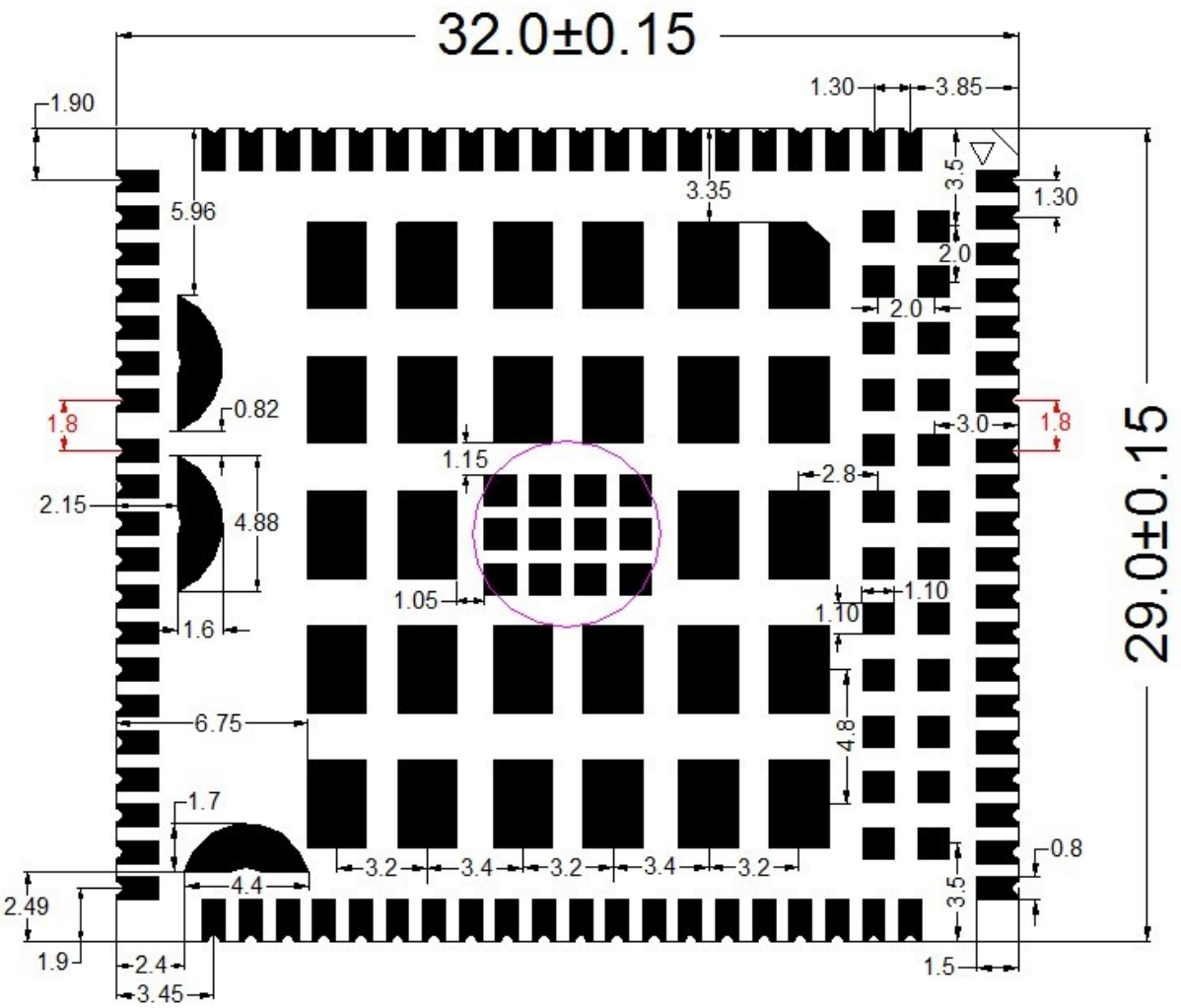

Figure 44: Module Bottom Dimensions (Bottom View)

7.2. Recommended Footprint

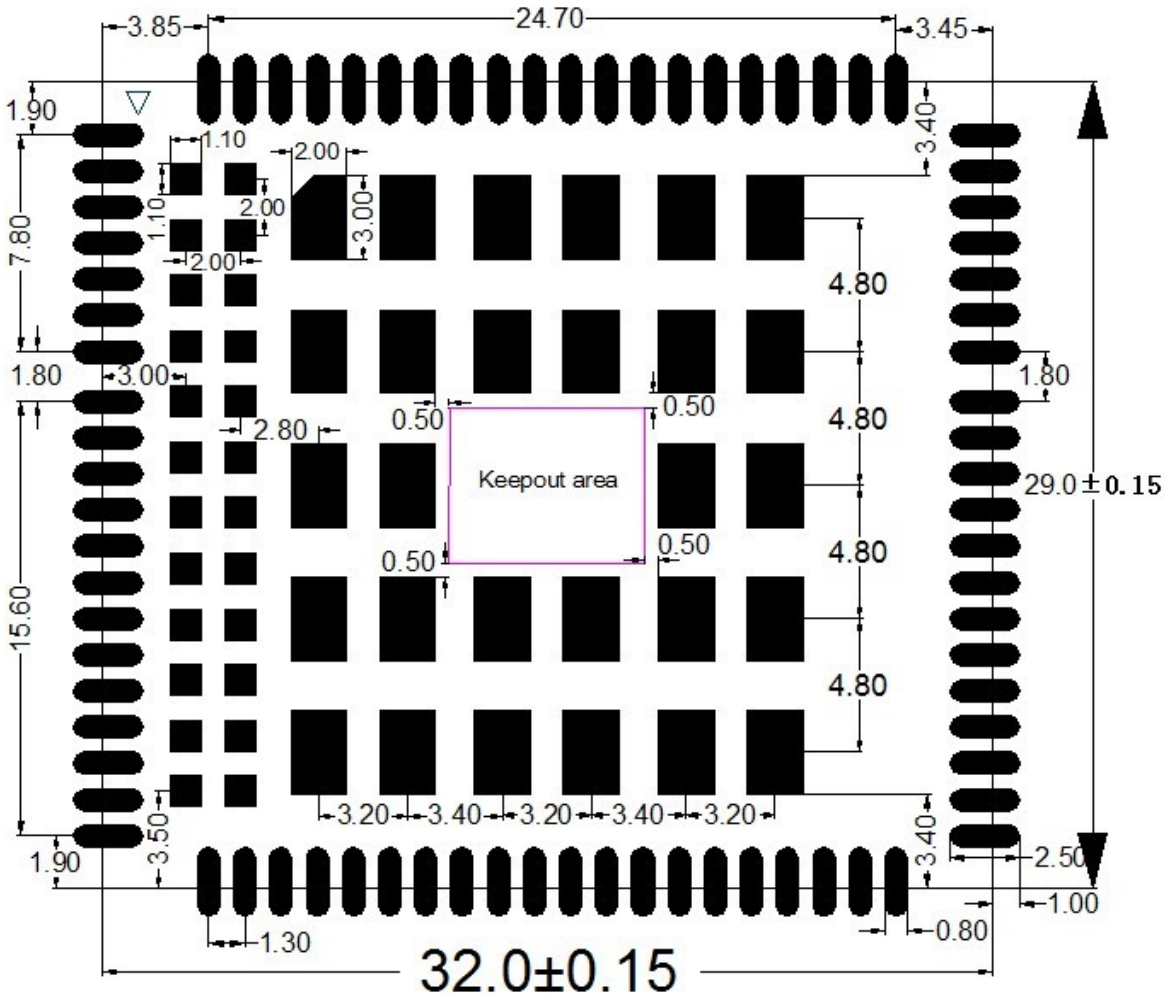

Figure 45: Recommended Footprint (Top View)

NOTES

1. The keepout area should not be designed.
2. For easy maintenance of the module, please keep about 3mm between the module and other components in thehost PCB.

7.3. Design Effect Drawings of the Module

Figure 46: Top View of the Module

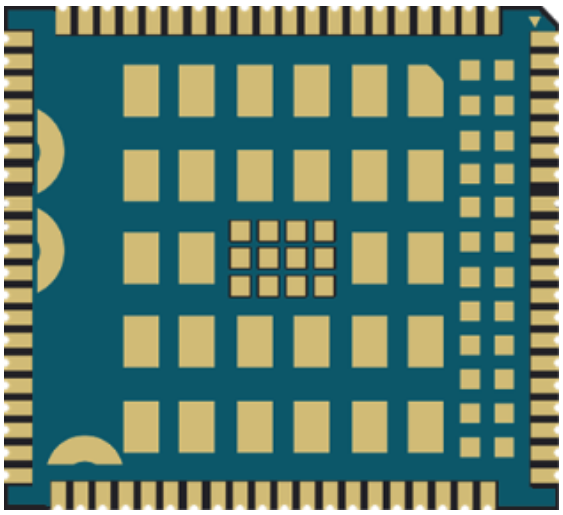

Figure 47: Bottom View of the Module

NOTE

These are design effect drawings of EC25 module. For more accurate pictures, please refer to the module that you get from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage

EC25 is stored in a vacuum-sealed bag. It is rated at MSL 3, and its storage restrictions are listed below.

1. Shelf life in vacuum-sealed bag: 12 months at <40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:

   - Mounted within 168 hours at the factory environment of ≤30ºC/60%RH.
   - Stored at <10% RH.

3. Devices require bake before mounting, if any circumstances below occurs:

   - When the ambient temperature is 23ºC±5ºC and the humidity indicator card shows the humidity is >10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤30ºC/60%RH.

4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic packagecannot be subjected to high temperature, it should be removed from devices before high temperature (120ºC) baking. If shorter baking time is desired, please refer to *IPC/JEDECJ-STD-033* for baking procedure.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly so as to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.20mm.

It is suggested that the peak reflow temperature is 235ºC~245ºC (for SnAg3.0Cu0.5 alloy). The absolute maximum reflow temperature is 260ºC. To avoid damage to the module caused by repeated heating, it is suggested that the module should be mounted after reflow soldering for the other side of PCB has been completed. Recommended reflow soldering thermal profile is shown below:

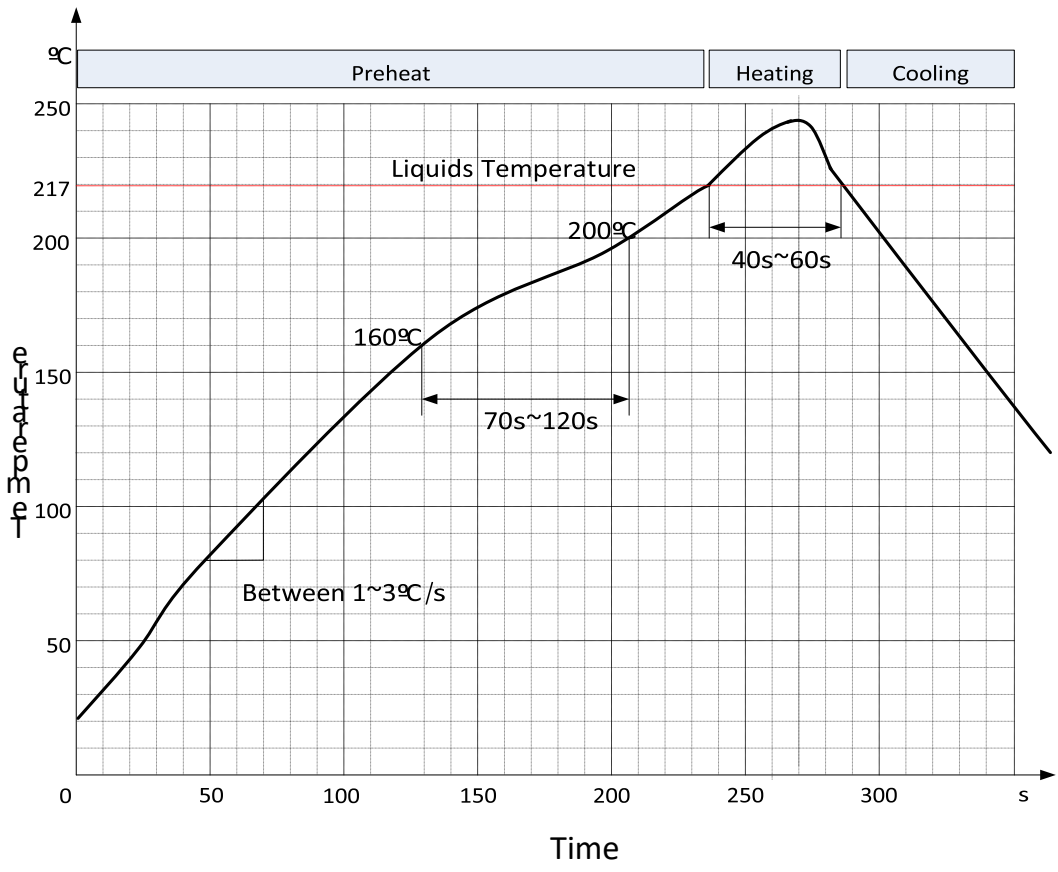

Figure 48: Reflow Soldering Thermal Profile

8.3. Packaging

EC25 is packaged in tap and reel carriers. One reel is 11.88m long and contains 250pcs modules. The figure below shows the package details, measured in mm.

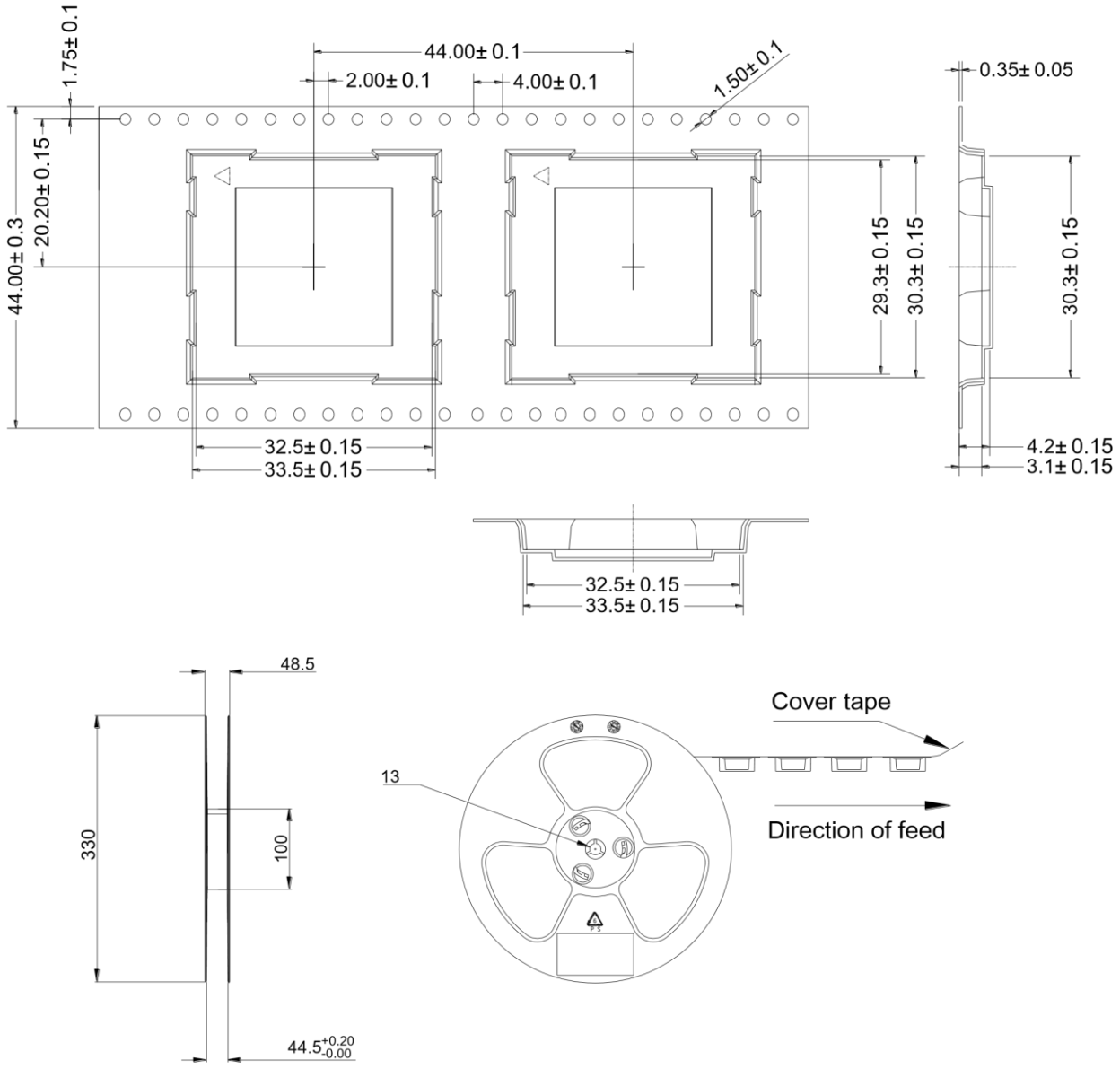

Figure 49: Tape and Reel Specifications

19 Terms and Abbreviations

Table 53: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear To Send
DC-HSPA+	Dual-carrier High Speed Packet Access
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex

FR	Full Rate
GLONASS	GLObalnaya NAvigatsionnaya Sputnikovaya Sistema, the Russian Global Navigation Satellite System
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HR	Half Rate
HSPA	High Speed Packet Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
I/O	Input/Output
Inorm	Normal Current
LED	Light Emitting Diode
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station (GSM engine)
MT	Mobile Terminated

PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SIM	Subscriber Identification Module
SIMO	Single Input Multiple Output
SMS	Short Message Service
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TX	Transmitting Direction
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USIM	Universal Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value

Vmin	Minimum Voltage Value
V_{IH}max	Maximum Input High Level Voltage Value
V_{IH}min	Minimum Input High Level Voltage Value
V_{IL}max	Maximum Input Low Level Voltage Value
V_{IL}min	Minimum Input Low Level Voltage Value
V_{I}max	Absolute Maximum Input Voltage Value
V_{I}min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

10 Regulatory

FCC Certification Requirements

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device. And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and portable applications. The antenna installation and operating configurations of this transmitter, including any applicable source-based time averaging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.

2. The EUT is a mobile and portable device; maintain at least a 2.5cm separation between the EUT and the user's head and 0 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

3.A label with the following statements must be attached to the host end product: This device contains FCC ID: 2AH78201808EC25AF.

4.To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

- WCDMA B2/LTE B2: <8dBi
- WCDMA B4LTE B4/B66: <5dBi
- WCDMA B5/LTE B5: <9.416dBi
- LTE B14: <9.255dBi
- LTE B13: <9.173dBi
- LTE B12: <8.734dBi
- LTE B71: <8.545dBi

5. This module must not transmit simultaneously with any other antenna or transmitter

6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products.

Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: 2AH78201808EC25AF" or "Contains FCC ID: 2AH78201808EC25AF" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

> The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

> To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

IC Statement

IRSS-GEN

"This device complies with Industry Canada’s license-exempt RSSs. Operation is subject to the following two conditions:

1. This device may not cause interference; and
2. This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d’Industrie Canada applicables aux appareils radio exempts de licence.

L’exploitation est autorisée aux deux conditions suivantes :

1. l’appareil ne doit pas produire de brouillage;
2. l’utilisateur de l’appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d’en compromettre le fonctionnement."

Déclaration sur l'exposition aux rayonnements RF

L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 2.5 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

The host product shall be properly labeled to identify the modules within the host product. The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word “Contains” or similar wording expressing the same meaning, as follows:

“Contains IC: 21419-2018EC25AF” or “where: 21419-2018EC25AF is the module’s certification

number”.

Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.

L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installé dans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot « Contient » ou d'un libellé semblable exprimant la même signification, comme suit:

"Contient IC: 21419-2018EC25AF" ou "où: 21419-2018EC25AF est le numéro de certification du module".