STM8670B Datasheet

Revision History

Date	Version	Description	Author
2014-06-16	V0.0	first release	
2014-10-13	V1.0	change the pin definition	
2014-12-23	V1.1	change the pin definition	
2015-01-06	V1.2	change the pin definition	
2015-12-21	V1.3	FCC & CE qualified	

CONTENT

1. INTRODUCTION

The STM8670B Bluetooth® module is a consumer audio solution for wired or wireless applications, such as a soundbar, speaker, headphone or other sound product. It can be connected with any Bluetooth® devices in an operating range. It is slim and light so the designers can have better flexibilities for the product shapes.

The STM8670B Bluetooth® module complies with Bluetooth® specification version 4.0. It supports HSP, HFP, A2DP, AVRCP, PBAP, MAP, SPP and TWS…etc. It integrates an ultra-low-power DSP and application processor with embedded flash memory, a high-performance stereo codec, a power management subsystem, LED and LCD drivers and capacitive touch sensor inputs in a SOC IC. The dual-core architecture with flash memory enables manufactures to easily differentiate your products with new features without extending development cycles. It integrates RF Baseband controller, antenna,… etc. and provide UART interface, programmable I/O, stereo speaker output, microphone input,… etc.

The detail information of STM8670B Bluetooth® module is presented in this document below.

1.1 Block Diagram

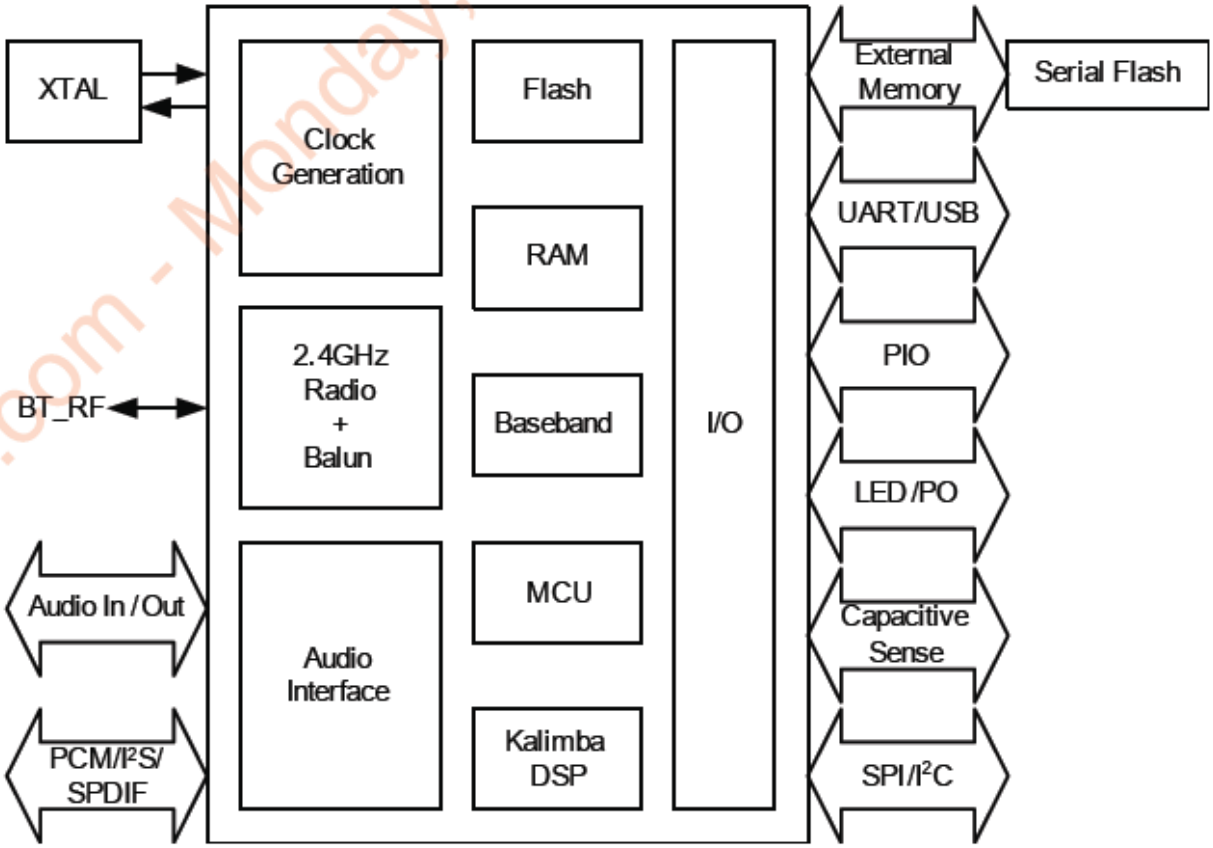


Figure 1

1.2 Features

- ✓ Small overall dimension(19mm x 15mm x 2.3mm)
- ✓ Bluetooth Specification V4.0(Dual Mode)
- ✓ Class1,Class 2 and Class 3 support
- ✓ Physical connection as SMD type
- ✓ 80MHz RISC MCU and 80MIPS Kalimba DSP
- ✓ 16Mb internal flash memory(64-bit wide,45ns);optional support for 64Mb of external SPI flash
- ✓ Stereo codec with 2 channels ADC and up to 6 microphone inputs(include bias generators and digital microphone support)
- ✓ Support for CSR's latest CVC technology for narrow-band and wideband voice connections including wind noise reduction
- ✓ Music Enhancements: SBC,MP3,AAC and AAC+,Faststream codec,atpX,5-band EQ,3D stereo separation and so on.
- ✓ Audio Interfaces: I2S,PCM and SPDIF
- ✓ Serial Interfaces: UART,USB 2.0,I2C and SPI
- ✓ Support HSP, HFP, A2DP, AVRCP, PBAP, MAP, SPP, iAP profile
- ✓ Multipoint support for HFP connection to 2 handsets for voice
- ✓ Multipoint support for A2DP connection to 2 A2DP source for music playback
- ✓ 3 Hardware LED controllers (for RGB) and ability to drive LCD segment display directly
- ✓ Support for up to 6 capacitive touch sensor inputs
- ✓ Built-in RF combo filter, Integrated 26M Crystal.
- ✓ No radio signal interference, support for 802.11 co-existence
- ✓ FCC & CE qualified. FCC ID: 2AGRE000STM8670BV03

※ ***Some features are optional for customization on demand.***

1.3 Application

- ✓ TV
- ✓ Smart remote controllers
- ✓ Wired or wireless soundbar
- ✓ Wired or wireless speakers and headphones
- ✓ Wearable audio with sensors(health and well-bing applications)

2. GENERAL SPECIFICATION

Bluetooth Specification	
Chip Set	CSR8670
Module ID	STM8670B
BT Standard	Bluetooth® V4.0 specification
RF TX Output Power	10dBm (Max)
Sensitivity	-90dBm@0.1%BER
Frequency Band	2.402GHz~2.480GHz ISM Band
Baseband Crystal OSC	26MHz
Hopping	1600hops/sec, 1MHz channel space
RF Input Impedance	50 ohms
Major Interface	• Microphone : Input (Differential) • Speaker : Output (Differential) • UART : Tx/Rx • PIOs
Profile	HSP, HFP, A2DP, AVRCP,PBAP,MAP,SPP
Voice Processor	80MIPS Kalimba with cVc support
Power	
Supply Voltage	3.0V ~ 4.2V DC
Working Current	15mA typical, depends on profiles
Standby Current	<1mA
Operating Environment	
Temperature	-40ºC to +85ºC
Humidity	10%~90% Non-Condensing
Environmental	RoHS Compliant

3. PHYSICAL CHARACTERISTIC

STM8670B Dimension: Top View

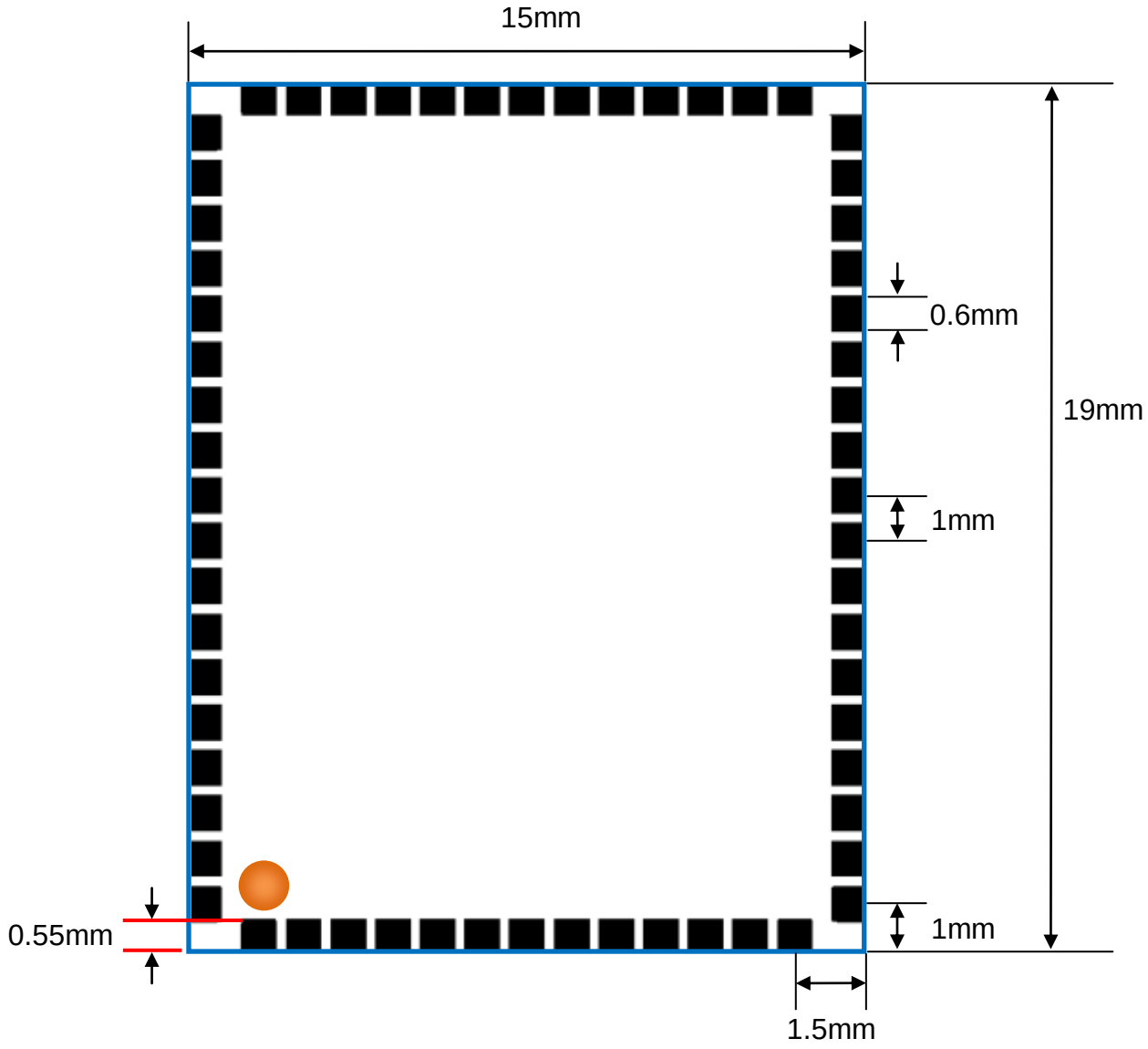


Figure 2

STM8670B Pin Definition: Top View

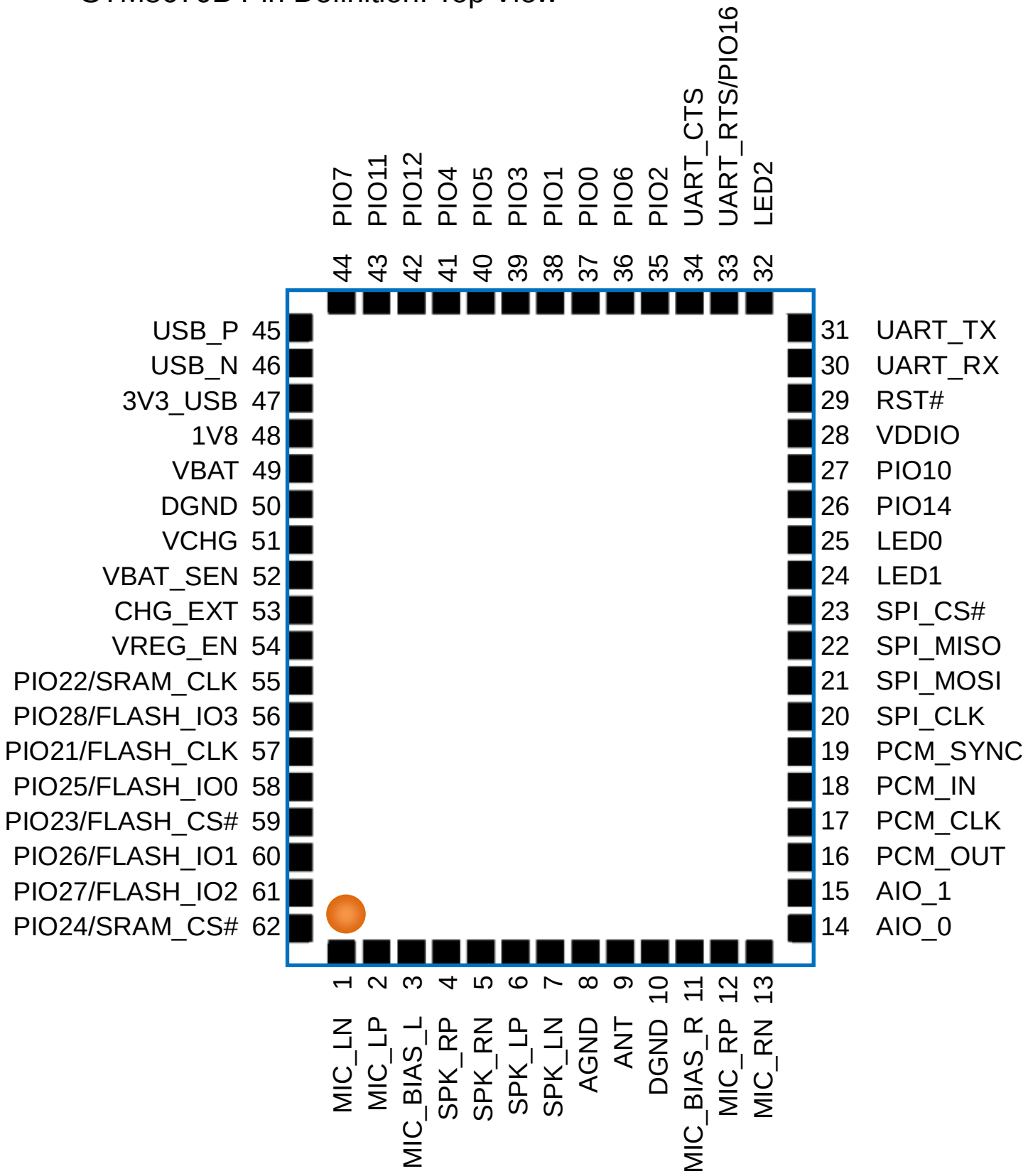


Figure 3

3.1 Pin Description

Pin#	Pin Name	Pad Type	Description
1	MIC_LN	Analogue in	Microphone input negative, left
2	MIC_LP	Analogue in	Microphone input positive, left
3	MIC_BIAS_L	Analogue out	Microphone bias A
4	SPK_RP	Analogue out	Speaker output positive, right
5	SPK_RN	Analogue out	Speaker output negative, right
6	SPK_LP	Analogue out	Speaker output positive, left
7	SPK_LN	Analogue out	Speaker output negative, left
8	AGND	Ground	Analogue Ground
9	ANT		External antenna
10	DGND	Ground	Digital Ground
11	MIC_BIAS_R	Analogue out	Microphone bias R
12	MIC_RP	Analogue in	Microphone input positive, right
13	MIC_RN	Analogue in	Microphone input negative, right
14	AIO_0	Bi-directional	Analogue programmable input / output line
15	AIO_1	Bi-directional	Analogue programmable input / output line
16	PCM_OUT/PIO18	Bi-directional with weak pull down	Synchronous data output. Alternative function PIO[18]
17	PCM_CLK/PIO20	Bi-directional with weak pull down	Synchronous data clock. Alternative function PIO[20]
18	PCM_IN/PIO17	Bi-directional with weak pull down	Synchronous data input. Alternative function PIO[17]
19	PCM_SYNC/PIO19	Bi-directional with weak pull down	Synchronous data sync. Alternative function PIO[19]
20	SPI_CLK	Input with weak pull down	SPI Clock
21	SPI_MOSI	Input with weak pull down	SPI data input

22	SPI_MISO	Output with weak pull down	SPI data output
23	SPI_CS#	Input with strong pull up	Chip select for SPI, active low
24	LED1	Open drain	LED driver Alternative function PIO[30]
25	LED0	Open drain	LED driver Alternative function PIO[29]
26	PIO14	Bi-directional with weak pull down	Programmable input/output line
27	PIO10	Bi-directional with weak pull down	Programmable input/output line
28	VDDIO	VDD	I/O voltage
29	RST#	Input with strong pull up	Reset if low. Input debouced so must be low for >5ms to cause a reset
30	UART_RX	Bi-directional with weak pull up	UART data input
31	UART_TX	Bi-directional with weak pull up	UART data output
32	LED2	Open drain	LED driver Alternative function PIO[31]
33	UART_RTS/PIO16	Bi-directional with weak pull up	UART request to send, active low. Alternative function PIO[16]
34	UART_CTS	Bi-directional with weak pull down	UART clear to send, active low
35	PIO2	Bi-directional with weak pull down	Programmable input/output line
36	PIO6	Bi-directional with weak pull down	Programmable input/output line
37	PIO0	Bi-directional with weak pull down	Programmable input/output line
38	PIO1	Bi-directional with weak pull down	Programmable input/output line
39	PIO3	Bi-directional with weak pull down	Programmable input/output line
40	PIO5	Bi-directional with weak pull down	Programmable input/output line
41	PIO4	Bi-directional with weak pull down	Programmable input/output line
42	PIO12	Bi-directional with weak pull down	Programmable input/output line
43	PIO11	Bi-directional with weak pull down	Programmable input/output line
44	PIO7	Bi-directional with weak pull down	Programmable input/output line
45	USB_P	Bi-directional	USB data plus with selectable internal 1.5kohm pull-up resistor

46	USB_N	Bi-directional	USB data minus
47	3V3_USB		Positive supply for USB ports
48	1V8		1.8V switch-mode power regulator output
49	VBAT	Power supply	Battery positive terminal
50	DGND	Ground	Digital Ground
51	VCHG		Battery charger input
52	VBAT_SEN		Battery charger sense input
53	CHG_EXT		External battery charger control
54	VREG_EN		Regulator enable input
55	PIO22/SRAM_CLK	Bidirectional with strong pull up	RAM clock
56	PIO28/FLASH_IO3	Bidirectional with strong pull down	Serial quad I/O flash data bit 3
57	PIO21/FLASH_CLK	Bidirectional with strong pull down	Flash clock
58	PIO25/FLASH_IO0	Bidirectional with strong pull down	Serial quad I/O flash data bit 0
59	PIO23/FLASH_CSB	Bidirectional with strong pull down	SPI flash chip select
60	PIO26/FLASH_IO1	Bidirectional with strong pull down	Serial quad I/O flash data bit 1
61	PIO27/FLASH_IO2	Bidirectional with strong pull down	Serial quad I/O flash data bit 2.
62	PIO24/SRAM_CSB	Bidirectional with strong pull up	RAM chip select

4. PHYSICAL INTERFACE

4.1 Power Supply

The transient response of the regulator is important. If the power rails of the module are supplied from an external voltage source, the transient response of any regulator used should be 20μs or less.

4.2 Audio Interfaces

The Audio interface circuit consists of:

- Stereo/dual-mono audio codec
- Dual analogue audio inputs
- Dual analogue audio outputs
- 6 digial MEMS microphone inputs
- A configurable PCM,I2S or SPDIF interface

As below shows the functional blocks of the interface.The codec supports stereo/dual-mono playback and recrding of audio signals at multiple sample rates with a 16-bit resolution.The ADC and DAC of the codec each contain 2 independent high-quality channels.Any ADC or DAC channel runs at its own independent sample rate.

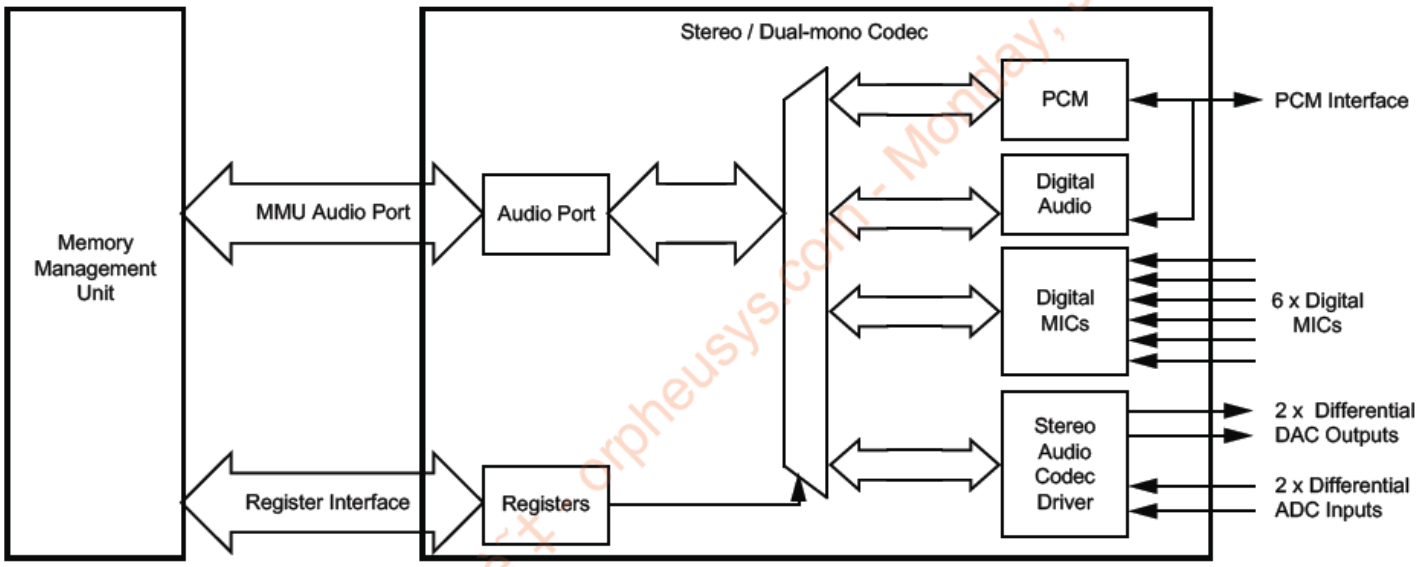


Figure 4

The interface for the digital audio bus shares the same pins as the PCM codec interface described in section as below which means each of the audio buses are mutually exclusive in ther usage.As below lists these alternative functions.

PCM Interface	SPDIF Interface	I²S Interface
PCM_OUT	SPDIF_OUT	SD_OUT
PCM_IN	SPDIF_IN	SD_IN
PCM_SYNC	-	WS
PCM_CLK	-	SCK

4.2.1 Audio Codec Interface

The main features of the interface are:

- Stereo and mono analogue input for voice band and audio band
- Stereo and mono analogue output for voice band and audio band
- Support for stereo digital audio bus standards such as I2S
- Support for IEC-60958 standard stereo digital audio bus standards,e.g.SPDIF and AES3(also known as AES/EBU)
- Support for PCM interfaces including PCM master cedecs that require an external system clock

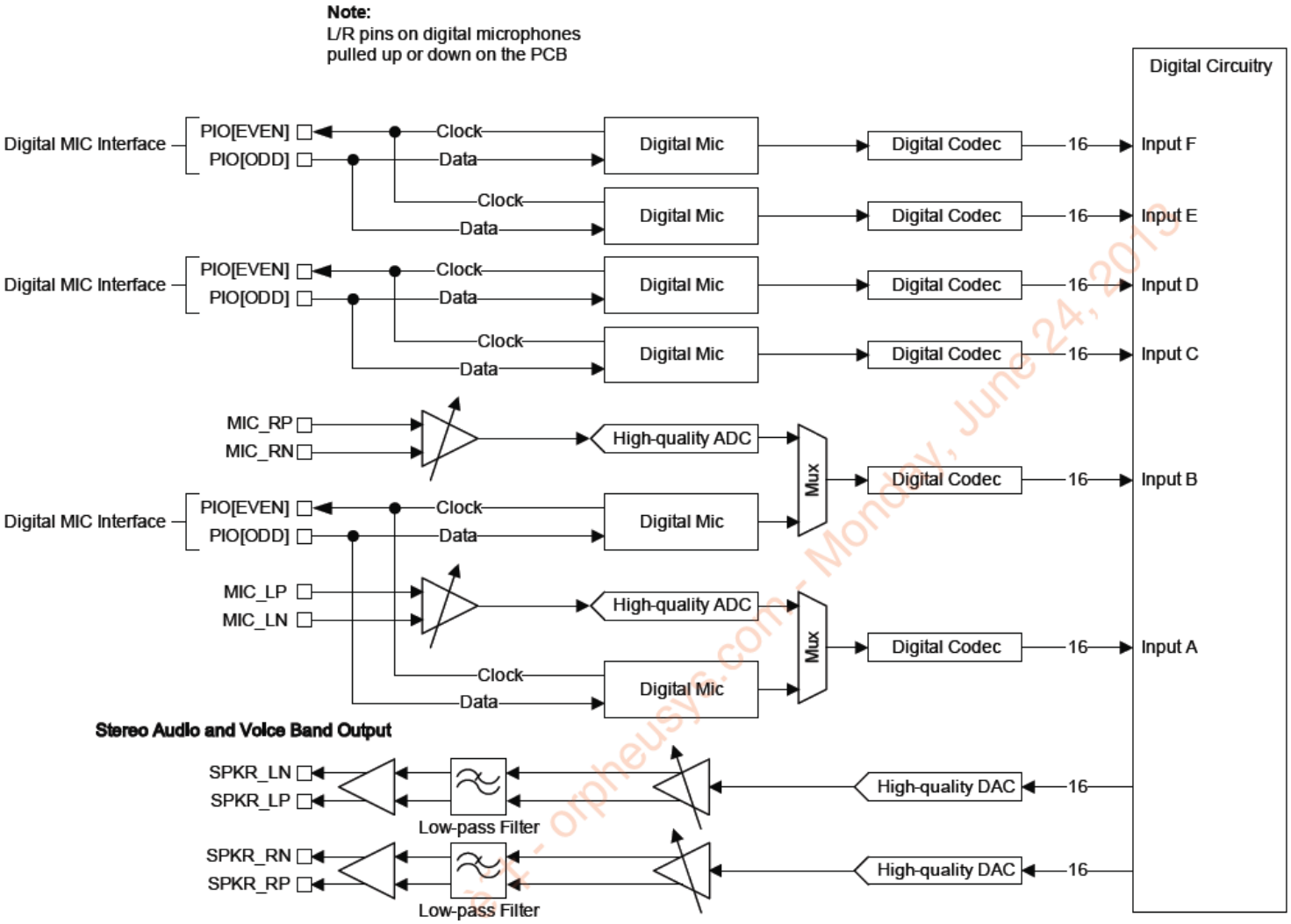


Figure 5

4.2.2 ADC

Figure 5 shows the CSR8670 consists of 2 high-quality ADCs:

- Each ADC has a second-order Sigma-Delta converter
- Each ADC is a separate channel with identical functionality
- There are 2 gain stages for each channel,1 of which is an analogue gain stage and the other is a digital gain stages

4.2.3 ADC Sample Rate Selection

Each ADC supports the following pre-defined sample rates,although other rates are progrmmable,e.g.40kHz:

- 8kHz
- 11.025 kHz
- 16kHz
- 22.050kHz
- 24kHz
- 32 kHz
- 44.1kHz
- 48 kHz

4.2.4 ADC Digital Gain

A digital gain stage inside the ADC varies from -24dB to 21.5dB,see as below,there is also a fine gain interface with 9-bit gain setting allowing gain changes in 1/32 steps. The Firmware controls the audio input gain.

Digital Gain Selection Value	ADC Digital Gain Setting (dB)	Digital Gain Selection Value	ADC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

4.2.5 DAC

The DAC consists of:

- 2 fourth-order Sigma-Delta converters enabling 2 separate channels that are identical functionality,as figure x shows
- 2 gain stages for each channel, 1 of which is an analogue gain stage and the other is a digital gain stage

4.2.6 DAC Sample Rate Selection

- 8kHz
- 11.025kHz
- 16kHz
- 22.050kHz
- 32kHz
- 40kHz
- 44.1kHz
- 48kHz
- 96kHz

4.2.7 DAC Digital Gain

A digital gain stage inside the DAC varies from -24dB to 21.5dB,see as below,there is alse a fine gain interface with 9-bit gain setting enabling gain changes in 1/32 steps. The overall gain control of the ADC is controlled by the firmware.Its setting is a combined function of the digital and analogue amplifier settings

Digital Gain Selection Value	DAC Digital Gain Setting (dB)	Digital Gain Selection Value	DAC Digital Gain Setting (dB)
0	0	8	-24
1	3.5	9	-20.5
2	6	10	-18
3	9.5	11	-14.5
4	12	12	-12
5	15.5	13	-8.5
6	18	14	-6
7	21.5	15	-2.5

4.2.8 DAC Analogue Gain

As below shows that the DAC analogue gain stage consists of 8 gain selection values that represent seven 3dB steps
The firmware controls the overall gain control of the DAC.Its setting is a combined function of the digital and analogue amplifier settings

Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)	Analogue Gain Selection Value	DAC Analogue Gain Setting (dB)
7	0	3	-12
6	-3	2	-15
5	-6	1	-18
4	-9	0	-21

4.2.9 IEC 60958 Interface

The IEC 60958 interface is a digital audio interface that uses bi-phase coding to minimise the DC content of the transmitted signal and enables the receiver to decode the clock information from the transmitted signal.The IEC 60958 specification is based on the 2 industry standards:

- AES3(alse known as AES/EBU)
- Sony and Philips interface specification SPDIF

The interface is compatible with IEC 60958-1, IEC 60958-3 and IEC 60958-4
The SPDIF interface signals are SPDIF-IN and SPDIF-OUT and are shared on the PCM interface pin.

4.2.10 Microphone Input

STM8670B contains 2 independent low-noise microphone bias generators.The microphone bias generators are recommended for biasing electret condensor microphones.A biasing circuit for microphones with a sensitivity between about -40dB to -60dB(0dB=1V/Pa)

4.2.11 Digital Microphone Inputs

The CSR8670 interfaces to 6 digital MEMS microphones.Figure x shows that 4 of the inputs have dedicated codec channels and 2 are multiplexed with the high-quality ADC channels.

4.2.12 Line input

If the pre-amplifier audio input gain is set at a low gain level it acts as an audio line level amplifier.In this line input mode the input impendance varies from 6kohm to 30kohm,depending on the volume setting.

4.2.13 Audio Output Stage

The output digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to a 2Mbits/sec multi-bit stream, which is fed into the analogue output circuitry.

The output circuit comprises a digital to analogue converter with gain setting and output amplifier.Its class-AB output-stage is capable of driving a signal on both channels of up to 2V pk-pk- differential into a load of 16Ω. The output is available as a differential signal between SPK_R_RP and SPK_R_RN for the left channel; and between SPK_L_LP and SPK_L_LN for the right channel. The output is capable of driving a speaker directly if its impedance is at least 8Ω if only one channel is connected or an external regulator is used.

The gain of the output stage is controlled by a 3-bit programmable resistive divider, which sets the gain in steps of approximately 3dB.

The multi-bit stream from the digital circuitry is low pass filtered by a second order bi-quad filter with a pole at 20kHz. The signal is then amplified in the fully differential output stage, which has a gain bandwidth of typically 1MHz.

4.3 PCM Interface

The audio PCM interface on the STM8670B supports:

- On-chip routing to Kalimba DSP
- Continuous transmission and reception of PCM encoded audio data over Bluetooth.
- Processor overhead reduction through hardware support for continual transmmision and reception of PCM data
- A bidirectional digital audio interface that routes directly into the baseband layer of the firmware .It does not pass through the HCI protocal layer.
- Hardware on the STM8670B for sending data to and from a SCO connection.
- Up to 3 SCO connections on the PCM interface at any one time.
- PCM interface master,generating PCM_SYNC and PCM_CLK.
- PCM interface slave,accepting externally generated PCM_SYNC and PCM_CLK.
- Various clock formats including:
  Long Frame Sync
  Short Frame Sync
  GCI timing environments
- 13-bit or 16-bit linear,8-bit u-law or A-law companded sample formats.
- Receives and transmits on any selection of 3 the first 4 slots following PCM_SYNC.

The PCM configuration options are enabled by setting the PS Key PSKEY_PCM_CONFIG32.

4.4 Digital Audio Interface(I2S)

The digital audio interface supports the industry standard formats for I2S,left-justified or right-justified.The interface shares the same pins as the PCM interface,which means each audio bus is mutually exclusive in its usage.Table as below lists these alternative functions

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

4.5 RF Interface

The module integrates a balun filter. The user can connect a 50ohms antenna directly to the RF port.

4.6 General Purpose Analog IO

The general purpose analog IOs can be configured as ADC inputs by software. Do not connect them if not use.

4.7 General Purpose Digital IO

There are nine general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED displays or interrupt signals to host controller, etc. Do not connect them if not use.

4.8 Serial Interfaces

4.8.1 UART

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

When the module is connected to another digital device,UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

Note: The serial port interface(UART)can be used for system debugging.Don’t support to use command set for profile function application by UART,such as HFP/A2DP/AVRCP and so on.These profiles function application can be contolled only by PIO,such as pairing/connect/answer/play/pause/next/previous function application and so on.

4.8.2 I2C Interface

As this I2C interface is software-driven it is suited to relatively slow functions such as driving a dot matrix LCD,keybaord scanner or EEPROM.If it is not used,then PIO[7:6] are available to form a software-driven master I2C interface.

4.8.3 SPI

The synchronous serial port interface (SPI) can be used for system debugging. It can also be used for in-system programming for the flash memory within the module. SPI interface uses the SPI_MOSI, SPI_MISO, SPI_CSB and SPI_CLK pins. Testing points for the SPI interface are reserved on board in case that the firmware shall be updated during manufacture.

The module operates as a slave and thus SPI_MISO is an output of the module. SPI_MISO is not in high-impedance state when SPI_CSB is pulled high. Instead, the module outputs 0 if the processor is running and 1 if it is stopped. Thus the module should NOT be connected in a multi-slave arrangement by simple parallel connection of slave SPI_MISO lines.

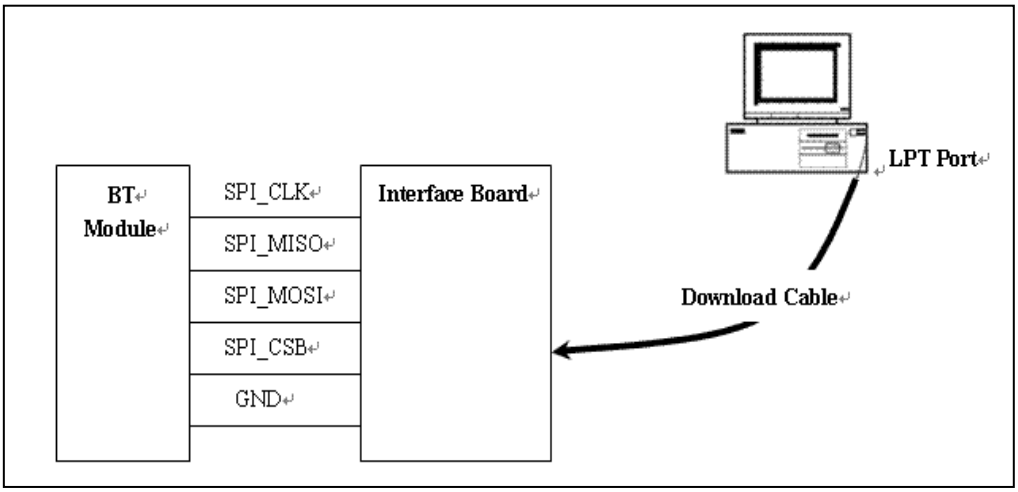


Figure 6

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Rating		Min	Max	Unit
Storage temperature		-40	105	°C
Supply Voltage				
5V(USB VBUS)	VCHG	-0.4	5.75	V
3.3V	SMPS_3V3	-0.4	3.60	V
	VDD_USB	-0.4	3.60	V
Battery	LED[2:0]	-0.4	4.40	V
	SMP_VBAT	-0.4	4.40	V
	VBAT_SENSE	-0.4	5.75	V
	VREGENABLE	-0.4	4.40	V
1.8V	VDD_AUDIO_DRV	-0.4	1.95	V
	VDD_AUX_1V8	-0.4	1.95	V
	VDD_PADS_1	-0.4	3.60	V
	VDD_PADS_2	-0.4	3.60	V
	VDD_PADS_3	-0.4	3.60	V
	SMPS_1V8_SENSE	-0.4	1.95	V
1.35V	SMPS_1V35_SENSE	-0.4	1.45	V
	VDD_AUDIO	-0.4	1.45	V
	VREGIN_DIG	-0.4	1.95	V
Other terminal voltages		VSS - 0.4	VDD + 0.4	V

Table 1

5.2 Recommended Operating Conditions

Rating		Min	Typ	Max	Unit
Operating temperature range		-40	20	85	°C
Supply Voltage					
5V(USB VBUS)	VCHG	4.75 / 3.10	5.00	5.75	V
3.3V	SMPS_3V3	3.10	3.30	3.60	V
	VDD_USB	3.10	3.30	3.60	V
Battery	LED[2:0]	1.10	3.70	4.25	V
	SMP_VBAT	2.50	3.70	4.25	V
	VBAT_SENSE	0	3.70	4.25	V
	VREGENABLE	0	3.70	4.25	V
1.8V	VDD_AUDIO_DRV	1.70	1.80	1.95	V
	VDD_AUX_1V8	1.70	1.80	1.95	V
	VDD_PADS_1	1.70	1.80	3.60	V
	VDD_PADS_2	1.70	1.80	3.60	V
	VDD_PADS_3	1.70	1.80	3.60	
	SMPS_1V8_SENSE	1.70	1.80	1.95.	V
1.35V4	SMPS_1V35_SENSE	1.30	1.35	1.40	V
	VDD_AUDIO	1.30	1.35	1.40	V
	VREGIN_DIG	1.30	1.35 or 1.80	1.95	V

Table 2

5.3 Input/output Terminal Characteristics

5.3.1 Codec: Analogue to Digital Converter

Analogue to Digital Converter						
Parameter	Conditions		Min	Typ	Max	Unit
Resolution	-		-	-	16	Bits
Input Sample Rate, F_{sample}	-		8	-	48	kHz
SNR	f_{in} = 1kHz B/W = 20Hz→F_{sample}/2 (20kHz max) A-Weighted THD+N < 0.1% 1.6V_{pk-pk} input	F_{sample}				
		8kHz	-	93	-	dB
		16kHz	-	92	-	dB
		32kHz	-	92	-	dB
		44.1kHz	-	92	-	dB
		48kHz	-	92	-	dB
THD+N	f_{in} = 1kHz B/W = 20Hz→F_{sample}/2 (20kHz max) 1.6V_{pk-pk} input	F_{sample}				
		8kHz	-	0.004	-	%
		48kHz	-	0.008	-	%
Digital gain	Digital gain resolution = 1/32		-24	-	21.5	dB
Analogue gain	Pre-amplifier setting = 0dB, 9dB, 21dB or 30dB Analogue setting = -3dB to 12dB in 3dB		-3	-	42	dB
Stereo separation(crosstalk)			-	-89	-	dB

Table 3

5.3.2 Codec: Digital to Analogue Converter

Digital to Analogue Converter							
Parameter	Conditions			Min	Typ	Max	Unit
Resolution	-			-	-	16	Bits
Output Sample Rate, F_{sample}	-			8	-	96	kHz
SNR	f_{in} = 1kHz B/W = 20Hz→20kHz A-Weighted THD+N < 0.1% 0dBFS input	F_{sample}	Load				
		48kHz	100kΩ	-	96	-	dB
		48kHz	32Ω	-	96	-	dB
		48kHz	16Ω	-	96	-	dB
THD+N	f_{in} = 1kHz B/W = 20Hz→20kHz 0dBFS input	F_{sample}	Load				
		8kHz	100kΩ	-	0.002	-	%
		8kHz	32Ω	-	0.002	-	%
		8kHz	16Ω	-	0.003	-	%
		48kHz	100kΩ	-	0.003	-	%
		48kHz	32Ω	-	0.003	-	%
		48kHz	16Ω	-	0.004	-	%
Digital Gain	Digital Gain Resolution = 1/32			-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB			-21	-	0	dB
Stereo separation(crosstalk)				-	-88-	-	dB

Table 4

6. RECOMMENDED TEMPERATURE REFLOW PROFILE

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

2F

Friday March 09, 2012 10:21:21

Site:

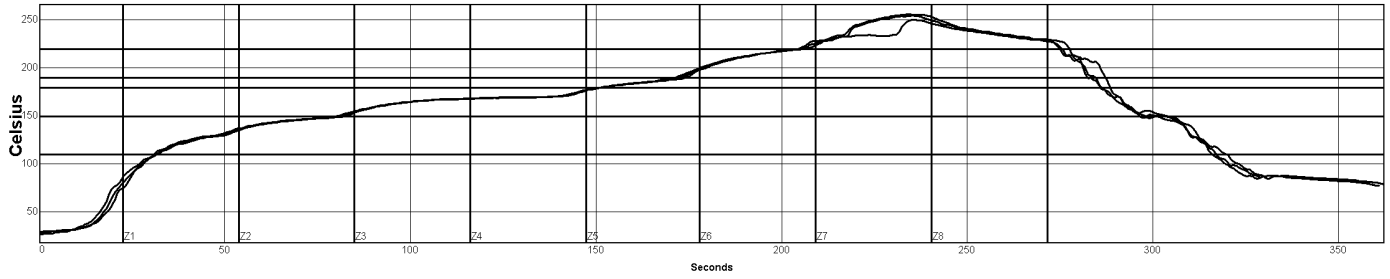
Oven Name: WQ

Process Window Name: RoHS

Setpoints (Celsius)

Zone	1	2	3	4	5	6	7	8
Top	140	150	170	170	190	225	265	230
Bottom	140	150	170	170	190	225	265	230

Conveyor Speed (cm/min): 75.0



PWI= 304%	Max Rising Slope		Preheat 110-190C		Soak Time 150-180C		Reflow Time /220C		Peak Temp	
2	3.9	189%	141.4	157%	70.4	-296%	71.1	111%	254.8	97%
3	4.0	197%	139.7	149%	70.6	-294%	70.3	103%	250.6	11%
4	3.9	192%	142.1	160%	69.6	-304%	71.2	112%	256.5	130%

Process Window:

Solder Paste: SYSTEM DEFAULT

Statistic Name	Low Limit	High Limit	Units
Max Rising Slope (Target=2.0)	0.0	3.0	Degrees/Second
Preheat Time 110-190C	90	130	Seconds
Soak Time 150-180C	90	110	Seconds
Time Above Reflow - 220C	50	70	Seconds
Peak Temperature 245	255		Degrees Celsius

Description:

Figure 7

7. FCC Statement

FEDERAL COMMUNICATIONS COMMISION (FCC) STATEMENT

15.21
You are cautioned that changes or modifications not expressly approved by the part responsible for compliance could void the user's authority to operate the equipment.

15.105(b)
Federal Communications Commission (FCC) Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.
-Increase the separation between the equipment and receiver.
-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1) This device may not cause harmful interference and

2) This device must accept any interference received, including interference that may cause undesired operation of the device.

FCC RF Radiation Exposure Statement:

1. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.
2. This equipment complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance.

End Product Labeling:
The final end product must be labeled in a visible area with the following: "Contains FCC ID: 2AGRE000STM8670BV03"