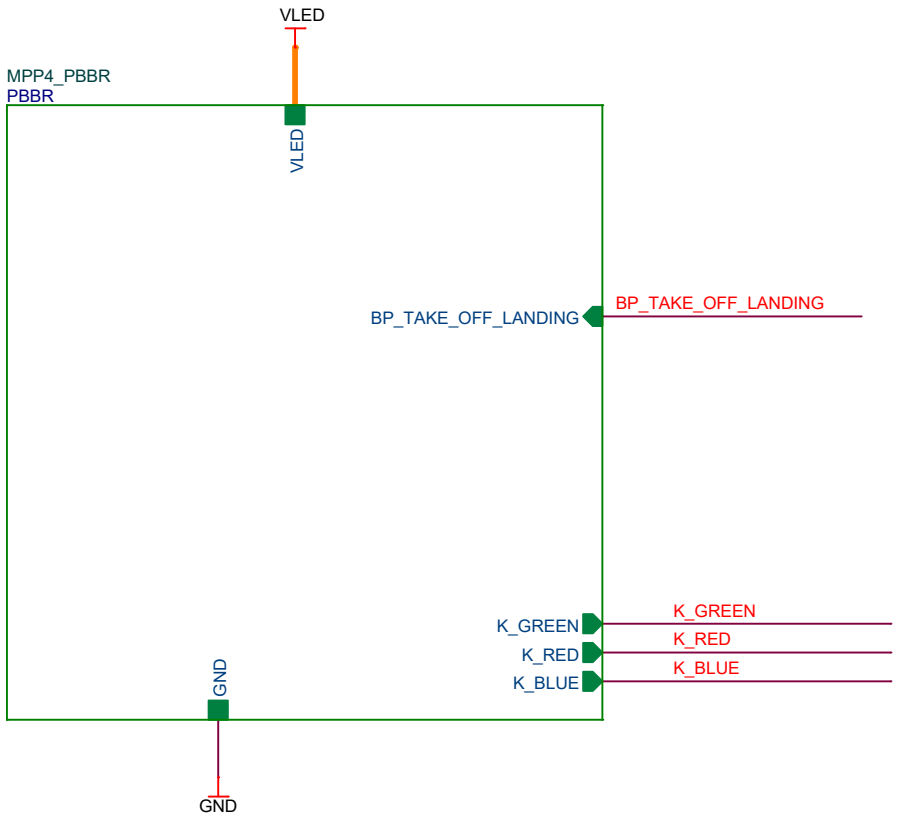


TOP

BASIC

DATE	BoM	AUTHOR	HISTORY

Schematic statut ☒ Draft ☐ Reviewed ☐ Approved

Parrot

Confidential

Author M. NGUEMA

Size A4

Project Name_Gerber_BoM

MPP4_PBBR_HW01

Date: Monday, November 30, 2020

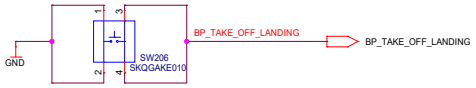
Sheet 1 of 5

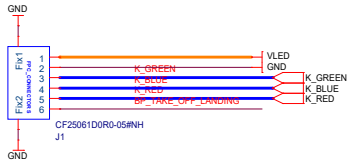
PCB number : MPP4_PBBR_HW01_20200828

BOLD Orange: 75 mA TRACK MINIMUM

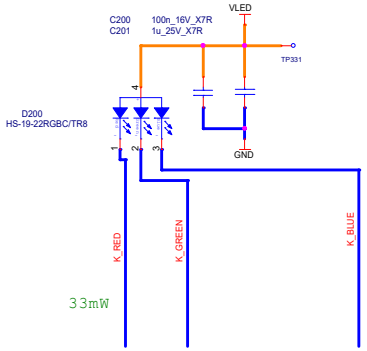
BOLD BLUE : 25 mA TRACK MINIMUM

BUTTONS





ON/OFF LEDs



BASIC

DATE	BoM	AUTHOR	HISTORY

Schematic statut [X] Draft [ ] Reviewed [ ] Approved

Parrot

Confidential

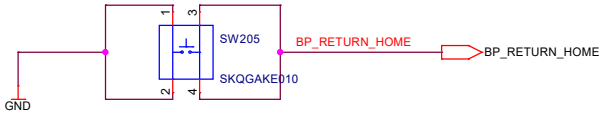
Author M. NGUEMA

Size A4 | Project Name_Gerber_BoM MPP4_PBBR_HW01

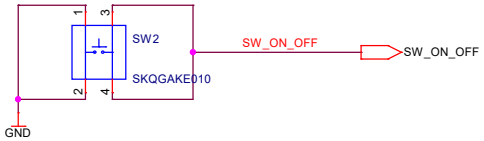
Date: Monday, November 30, 2020 | Sheet 2 of 5

MPP4_PBBL_HW02_20201113

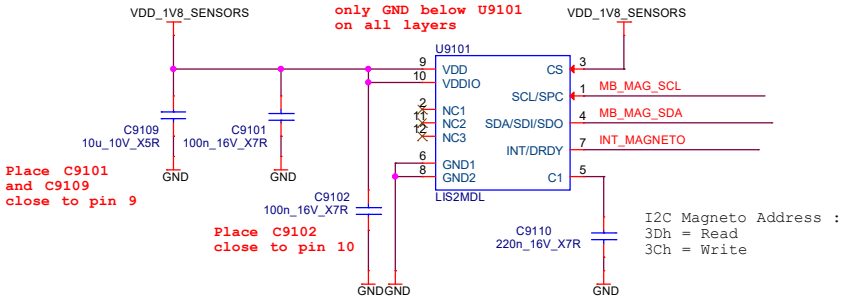
BUTTONS RETURN HOME



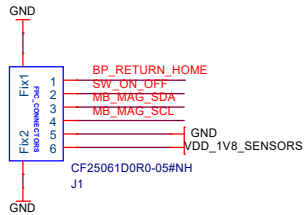
ON/OFF DETECTOR SWITCH



MAGNETOMETER



TO JBL BOARD



BASIC

DATE	BoM	AUTHOR	HISTORY

Schematic statut ☒ Draft ☐ Reviewed ☐ Approved

Parrot

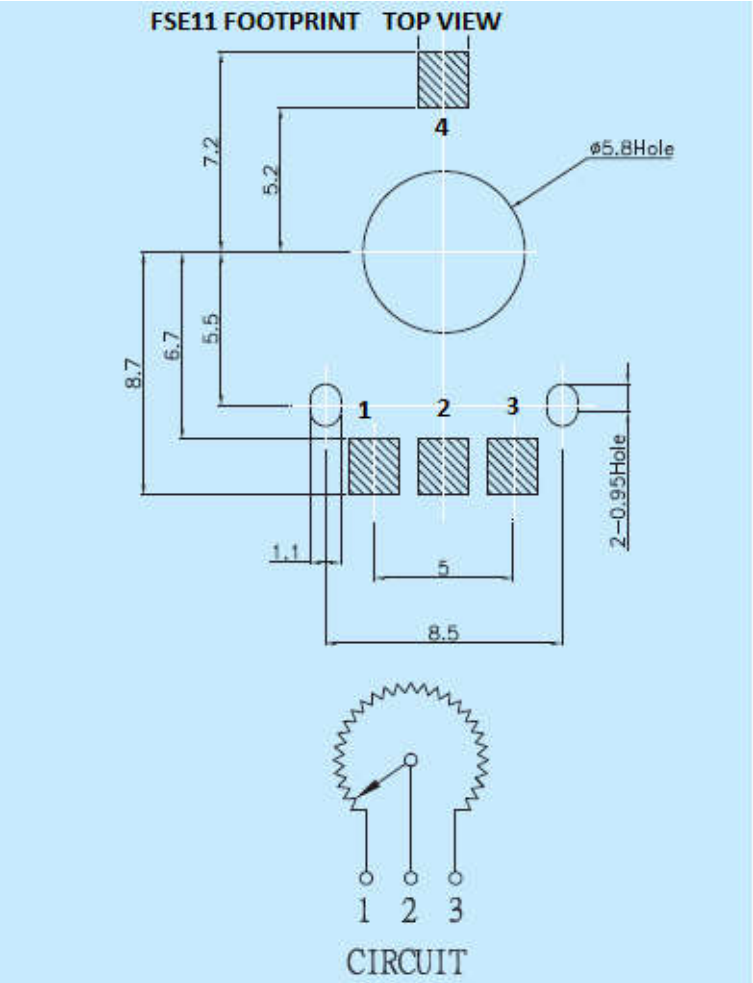
Confidential

Author C. BOUTIN

Size A4 | Project Name_Gerber_BoM MPP4_PBBL_HW01

Date: Monday, November 30, 2020 | Sheet 2 of 5

MPP4_SBL_01



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DATE	BoM	AUTHOR	HISTORY
12/12/2017		G. DOGAN	Delete JP1 Add H1,H2 and H3
12/12/2017		G. DOGAN	Delete JP1 Add H1,H2 and H3

Schematic statut: [X] Draft [ ] Reviewed [ ] Approved

Parrot

Confidential

Author: Marck NGUEMA

Size: A4

Project Name_Gerber_BoM

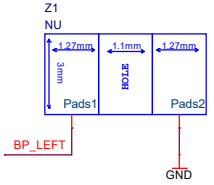
MPP4_SBL_HW01

Date: Monday, August 03, 2020

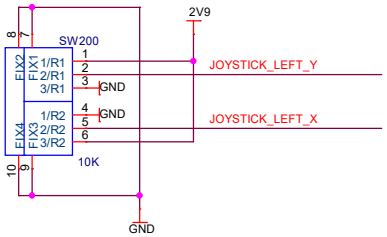
Sheet 1 of 1

MPP4_JBL_HW02_20201113

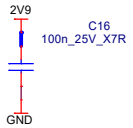
CONNECTOR OF BUTTONS LEFT



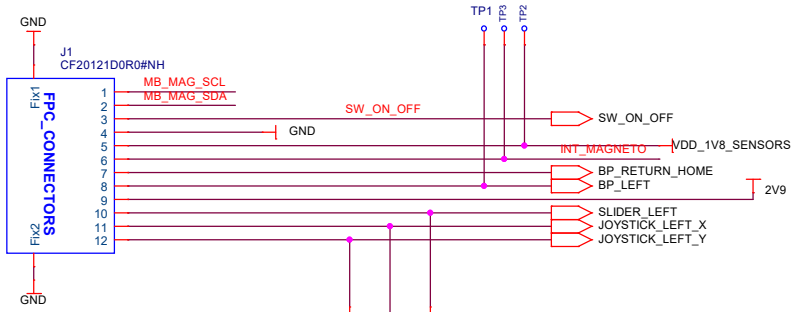
JOYSTICKS



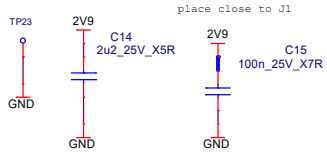
place close to J8208

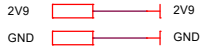


BB connector Left



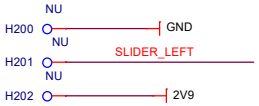
place close to J1



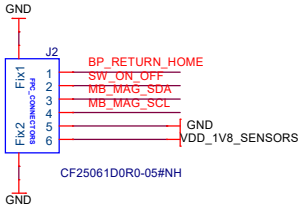


SLIDERS LEFT

SLIDER SOLDERED ON SBL BOARD
SLIDER REFERENCE: FSE11-01DB10KF5



to PBBL BOARD



BASIC

DATE	BoM	AUTHOR	HISTORY

Schematic statut ☒ Draft ☐ Reviewed ☐ Approved

Parrot

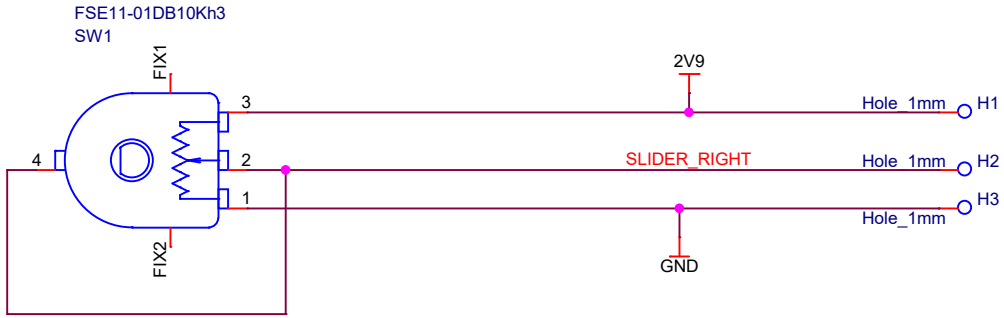
Confidential

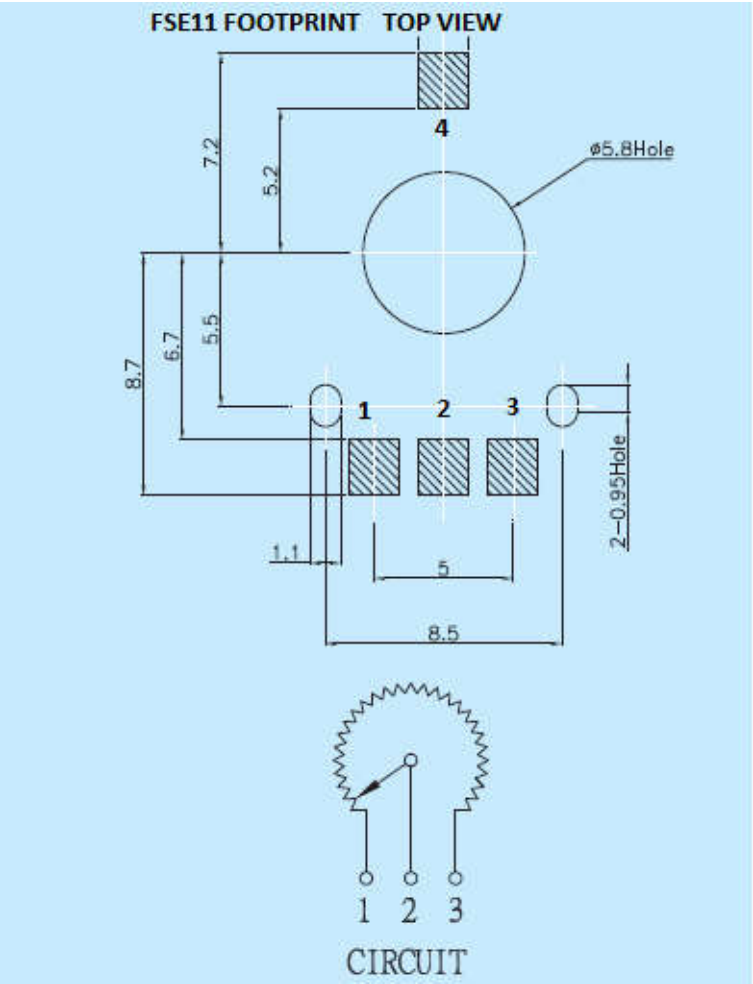
Author C. BOUTIN

Size A4 | Project Name_Gerber_BoM MPP4_JBL_HW01

Date: Monday, November 30, 2020 | Sheet 2 of 5

MPP4_SBR_01





<Variant Name>

DATE	BoM	AUTHOR	HISTORY
12/12/2017		G. DDOGAN	Delete JP2 Add H1, H2 and H3

Schematic statut: [X] Draft [ ] Reviewed [ ] Approved

Parrot

Confidential

Author: Marck NGUEMA

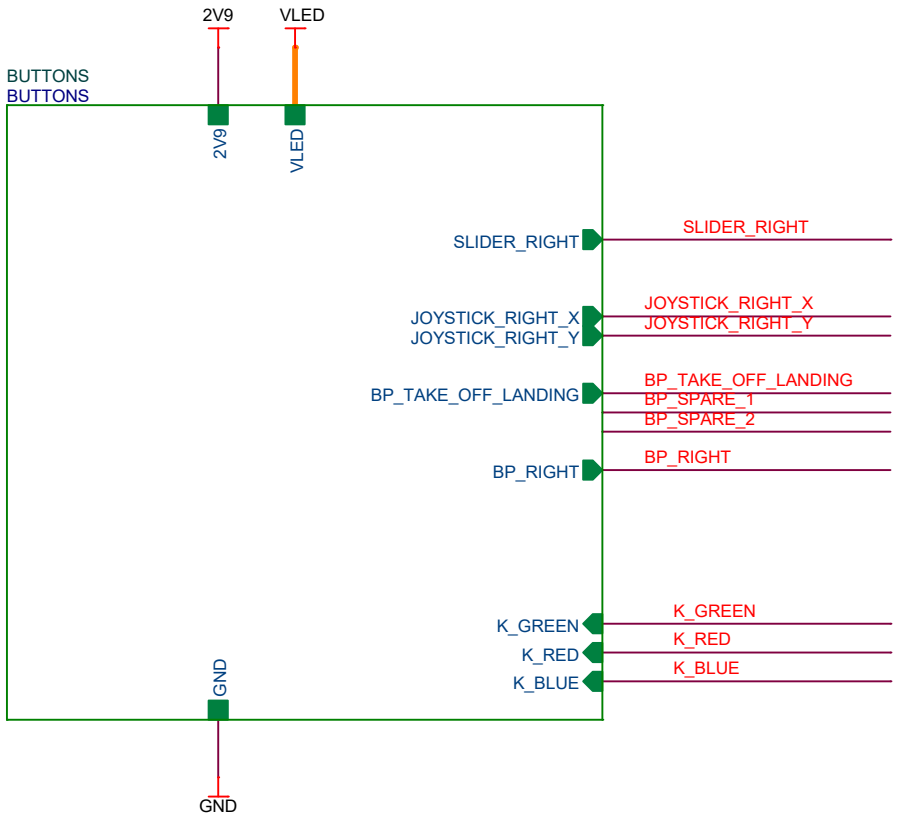
Size: A4

Project Name_Gerber_BoM

MPP4_SBR_HW01

Date: Monday, August 03, 2020

Sheet 1 of 1



TOP

BASIC

DATE	BoM	AUTHOR	HISTORY

Schematic statut ☒ Draft ☐ Reviewed ☐ Approved

Parrot

Confidential

Author M. NGUEMA

Size A4

Project Name_Gerber_BoM

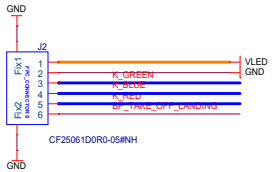
MPP4_JBR_HW01

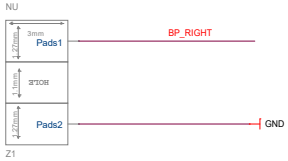
Date: Friday, August 28, 2020

Sheet 1 of 5

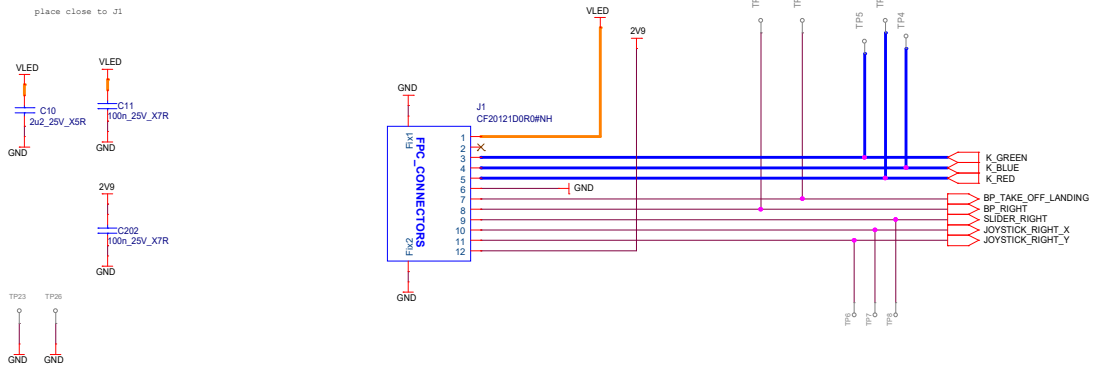
Place test point on BOTTOM side BOLD BLUE : 25 mA TRACK MINIMUM BOLD Orange: 75 mA TRACK MINIMUM

BUTTONS

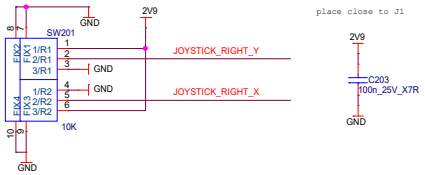




BB connector Right

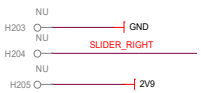


JOYSTICKS



SLIDERS RIGHT

SLIDER SOLDERED ON SBR BOARD
SLIDER REFERENCE: FSE11-01DB10Kh3



BASIC

DATE	BoM	AUTHOR	HISTORY

Schematic statut [X] Draft [ ] Reviewed [ ] Approved

Parrot

Confidential

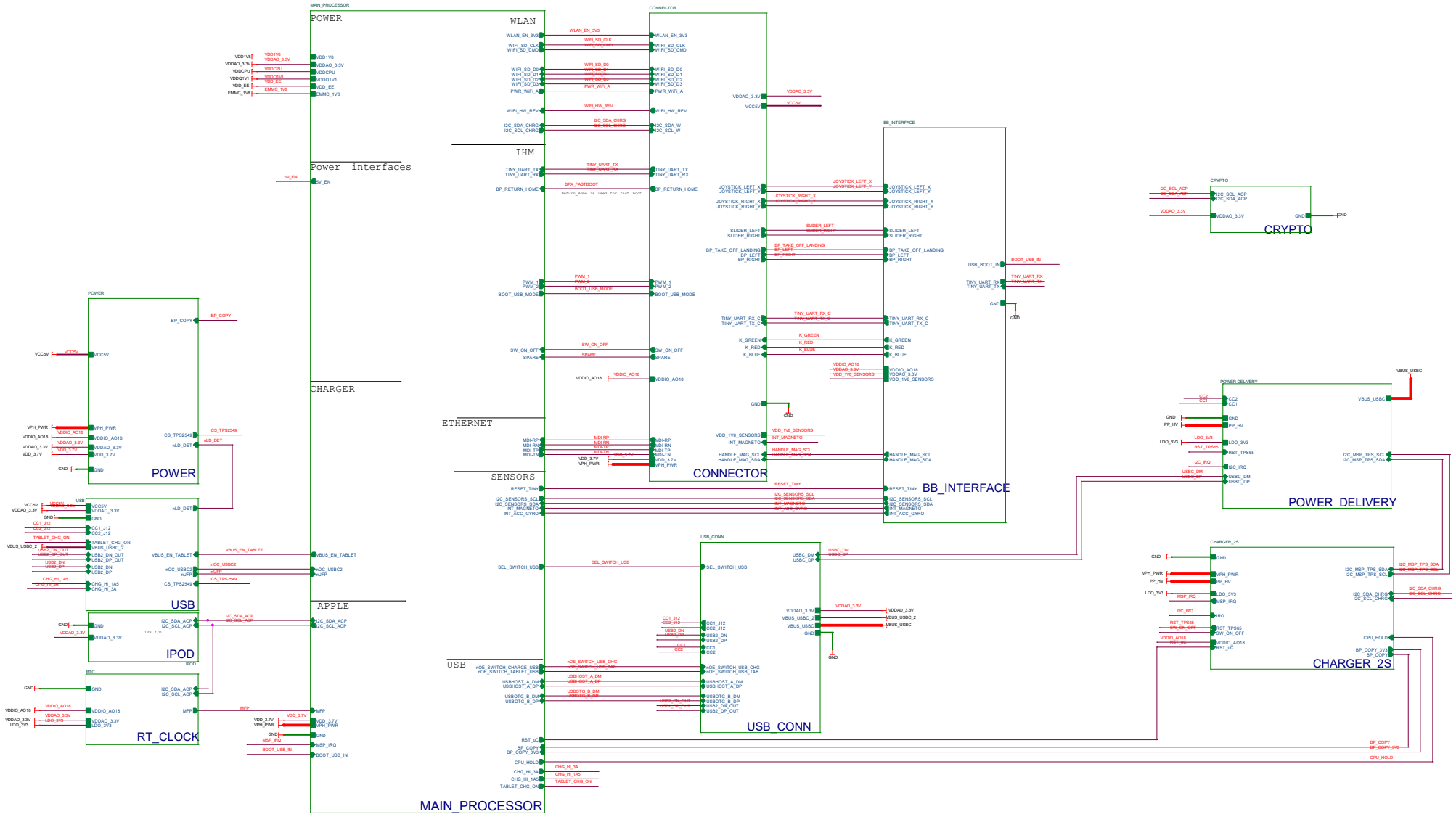
Author M. NGUEMA

Size A4 | Project Name_Gerber_BoM MPP4_JBR_HW01

Date: Friday, August 28, 2020 | Sheet 2 of 5

MPP4_MB_HW03

A2



MPP4

DATE	BoM	AUTHOR	HISTORY

Parrot

Confidential

Author

Project Name_Gerber_Bold

MPP4_MB_HW03

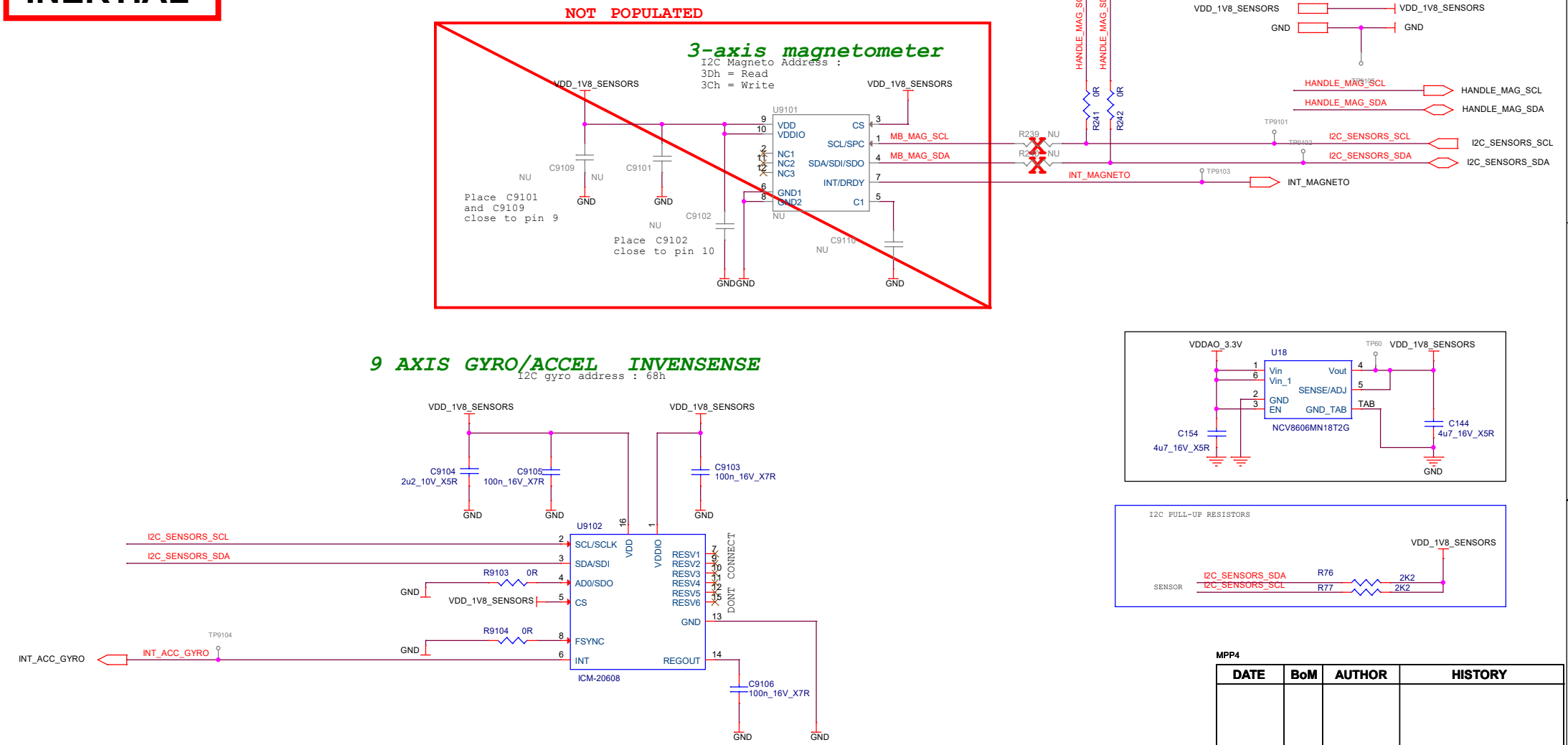
Create date Friday, June 03, 2011

Modify date Wednesday, March 10, 2021

Sheet 1 of 24

Size A2

INERTIAL



MPP4

DATE	BoM	AUTHOR	HISTORY

Parrot

Confidential

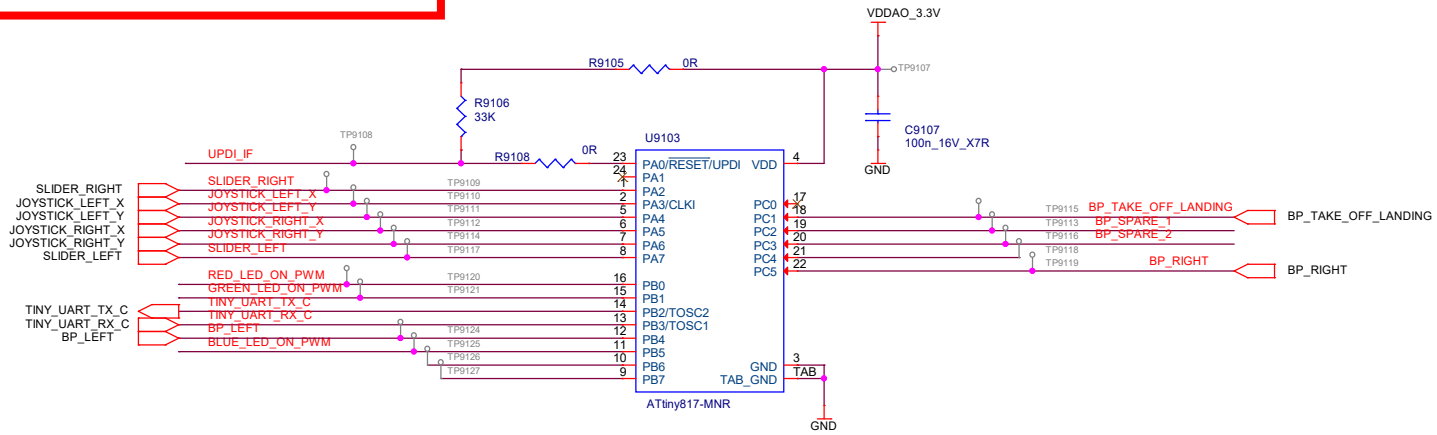
Author

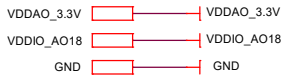
Project Name_Gerber_BoM

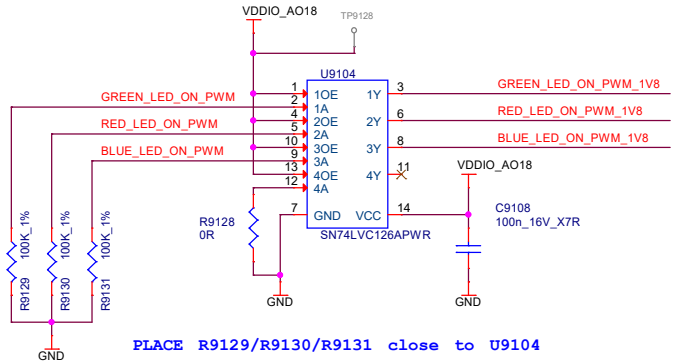
MPP4_MB_HW03

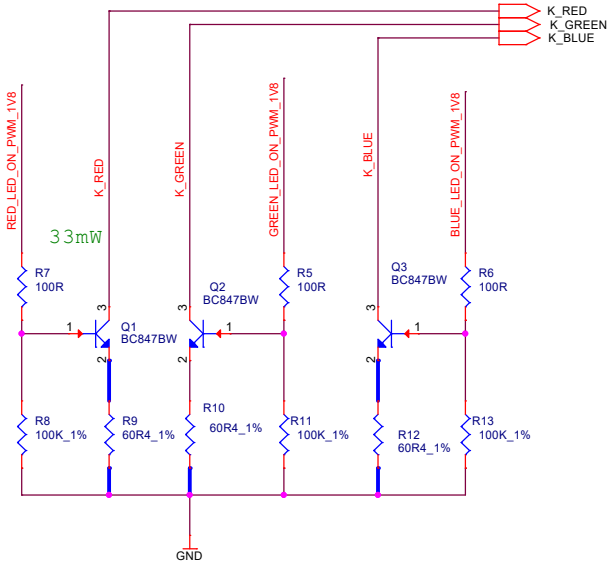
Create date	Tuesday, December 10, 2019	Sheet 2 of 24	Size A3
Modify date	Wednesday, March 10, 2021		

USER INTERFACE









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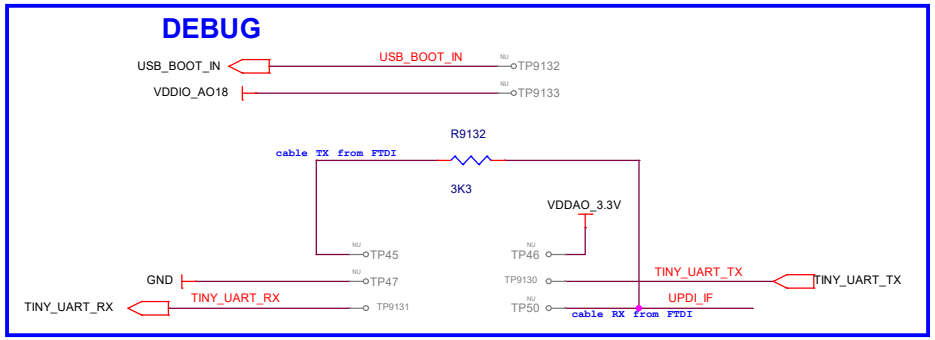
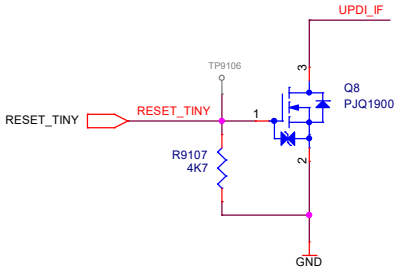




MPP4

DATE	BoM	AUTHOR	HISTORY

Parrot

Confidential

Author

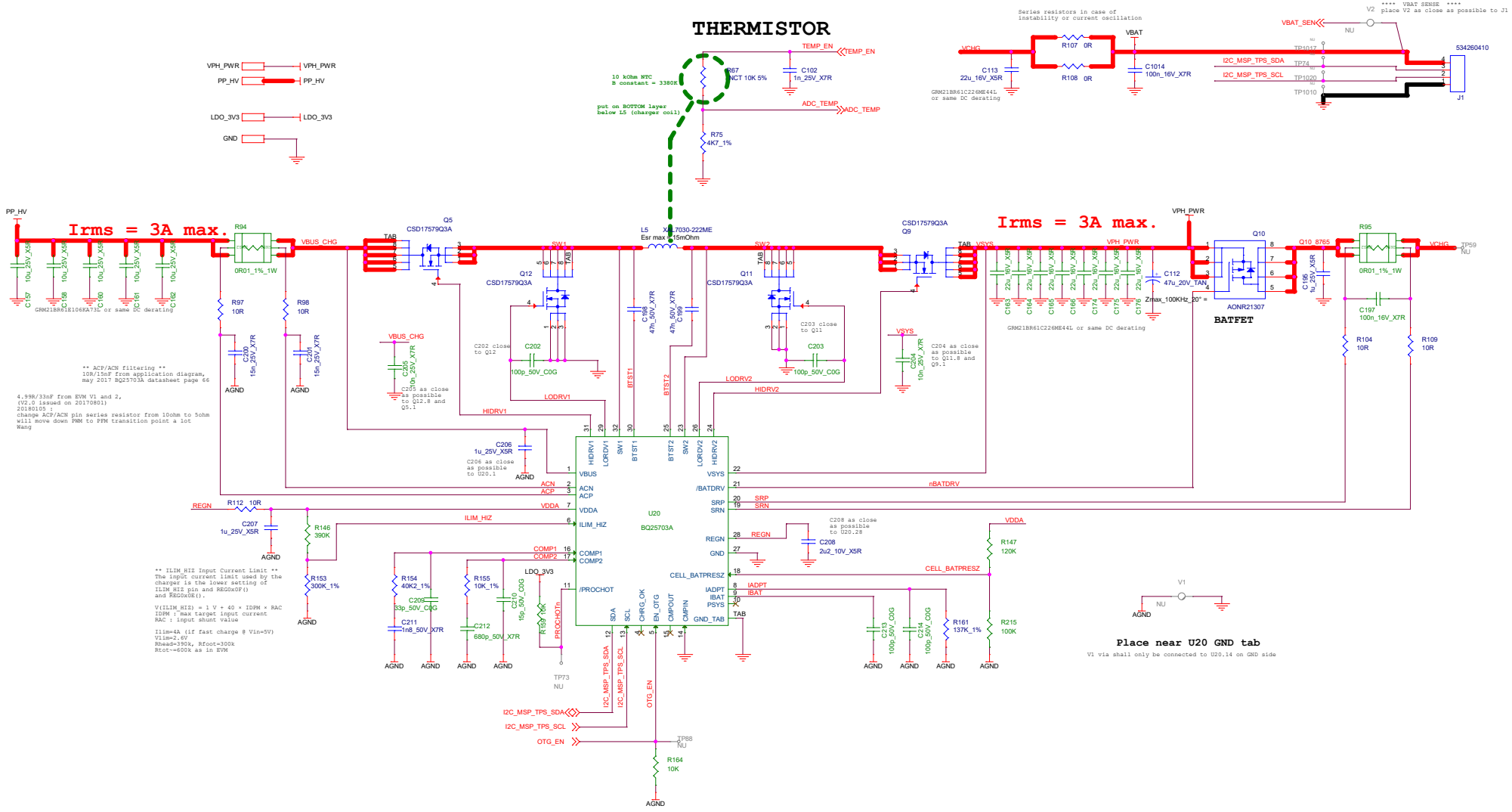
Project Name_Gerber_BoM

MPP4_MB_HW03

Create date	Tuesday, December 10, 2019	Sheet 3 of 24	Size A3
Modify date	Wednesday, March 10, 2021		

Charger

Charger 2S-HV @2.6A



MPP4

DATE	BoM	AUTHOR	HISTORY
29/02/2016	A	G. Lamotte	First draft
20170817	B	C. BOUTIN	Changed comparators compensation
20171002	B	C. BOUTIN	Changed all the stuff in orange
20170315	B	C. BOUTIN	Removed R9

Schematic statut [X] Draft [ ] Reviewed [ ] Approved

Parrot

Confidential

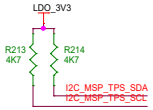
Author M. NGUEMA

Size A4 | Project Name_Gerber_BoM | MPP4_MB_HW03

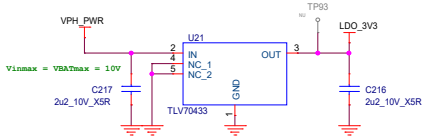
Date: Wednesday, March 10, 2021 | Sheet 5 of 24

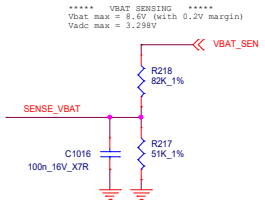
MCU

i²c PULLUPS

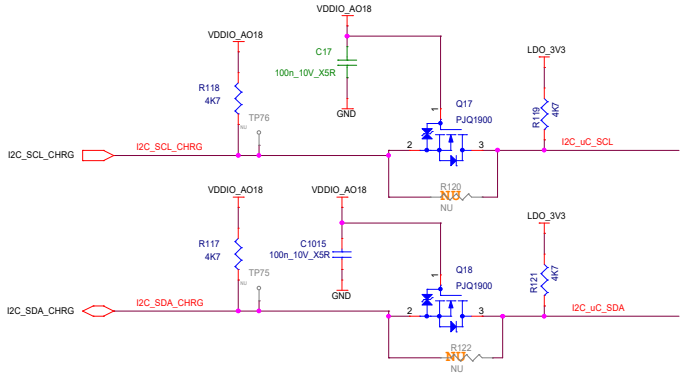


3V3 LDO





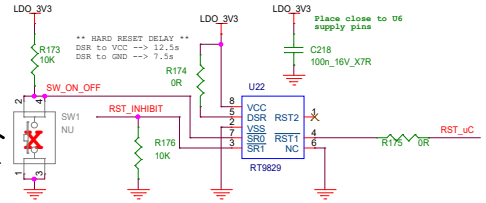
I2C Level Translator/Isolator

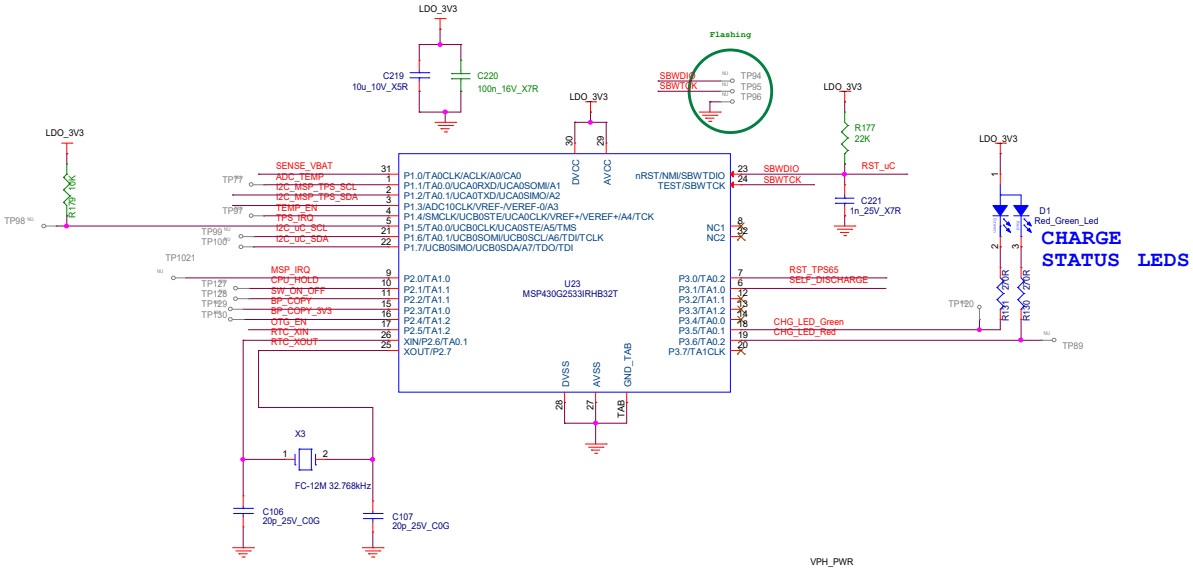


MCU RESET

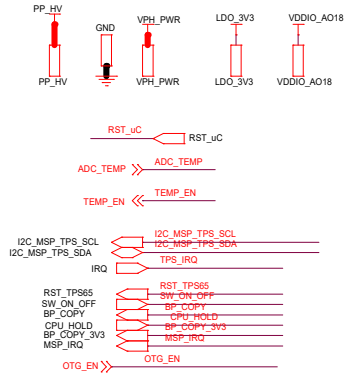
Silkscreen label : ON/OFF/RST

Place on BOTTOM

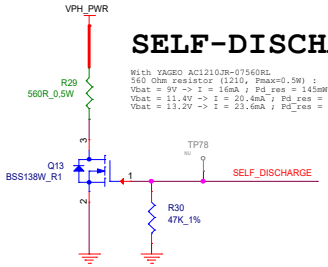




CHARGE STATUS LEDS



SELF-DISCHARGE



With YAGEO AC1210JR-07560RL
560 Ohm resistor (1210, Pmax=0.5W) :
Vbat = 9V -> I = 16mA ; Pd_res = 145mW
Vbat = 11.4V -> I = 20.4mA ; Pd_res = 232mW
Vbat = 13.2V -> I = 23.6mA ; Pd_res = 311mW

MPP4

DATE	BoM	AUTHOR	HISTORY
29/02/2016	A	G. Lamotte	First draft
20170523	A	C. BOUTIN	Changed IRQ signal direction
20171002	B	C. BOUTIN	Changed all the stuff in orange

Schematic statut: [X] Draft [ ] Reviewed [ ] Approved

Parrot

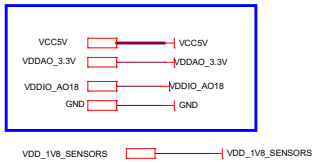
Confidential

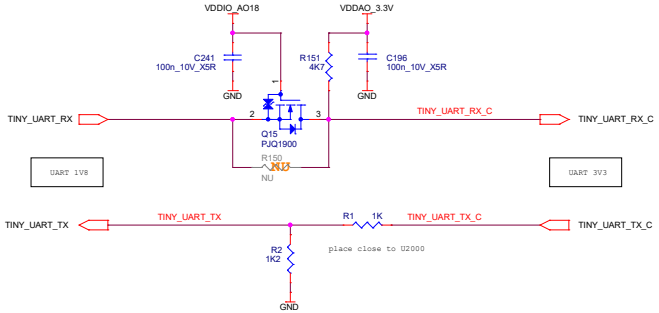
Author: <Author>

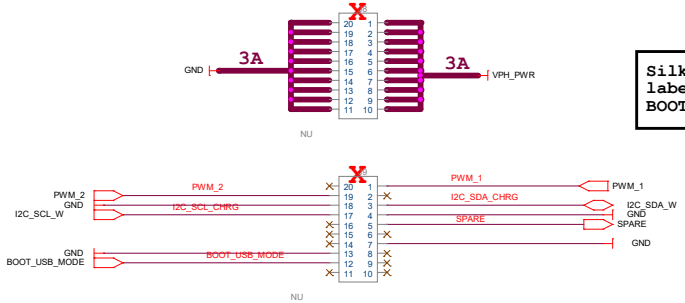
Size: A4 | Project Name_Gerber_BoM: MPP4_MB_HW03

Date: Wednesday, March 10, 2021 | Sheet 6 of 24

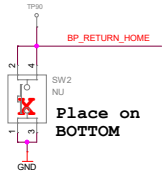
IHM-connector



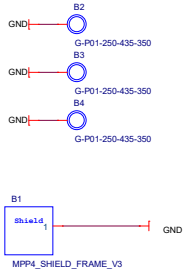




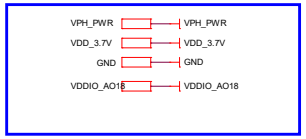
Silkscreen label : BOOT MODE

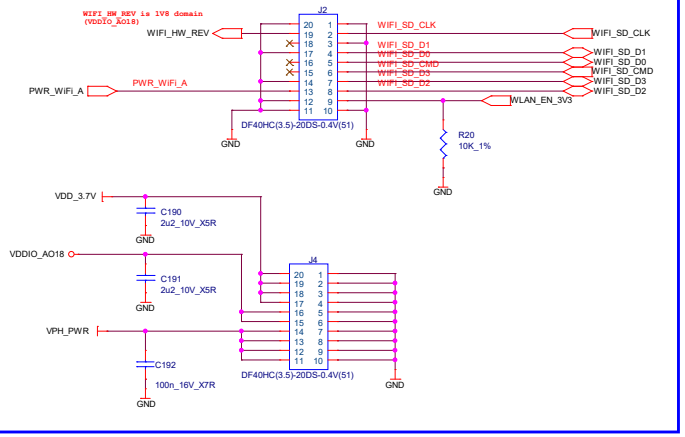


Place on BOTTOM

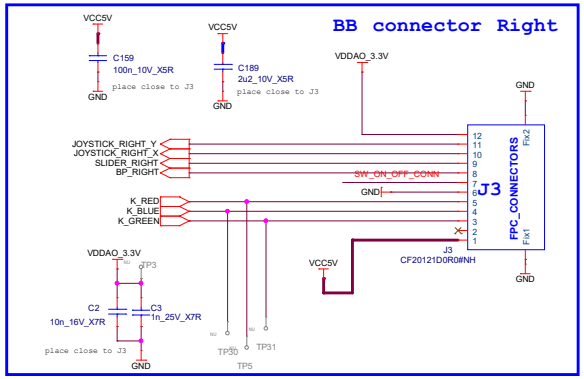


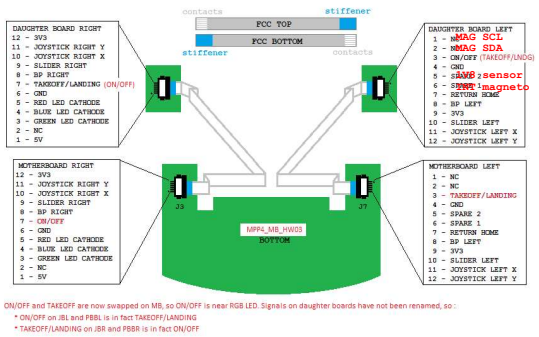
WLAN - IO





BB connector Right

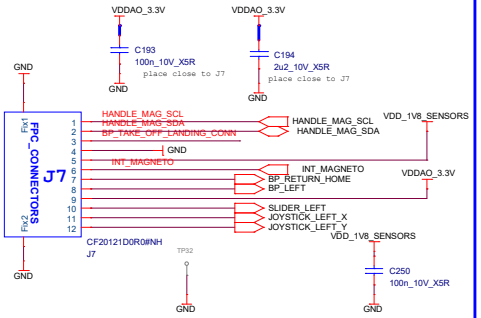




ON/OFF and TAKEOFF are now swapped on MB, so ON/OFF is near RGB LED. Signals on daughter boards have not been renamed, so :

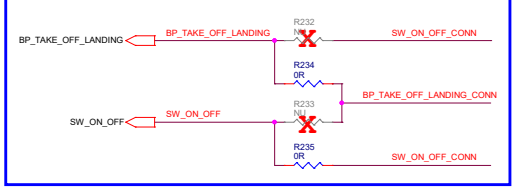
* ON/OFF on JBL and PBBL is in fact TAKEOFF/LANDING
* TAKEOFF/LANDING on JBR and PBBR is in fact ON/OFF

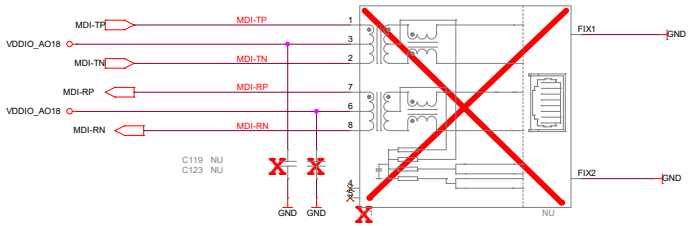
BB connector Left



to put back ON/OFF and TAKEOFF/LANDING as it ws on HW02, populate R232 and R233, and remove R234 and R235

REMAP ON/OFF on TAKEOFF/LANDING





MPP4

DATE	BoM	AUTHOR	HISTORY

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Author <OrgAddr1>

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MPP4_MB_HW03

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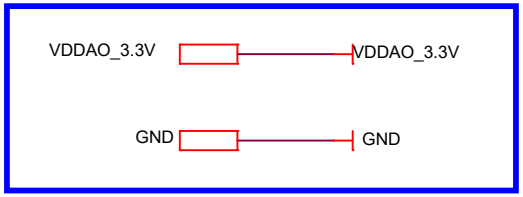
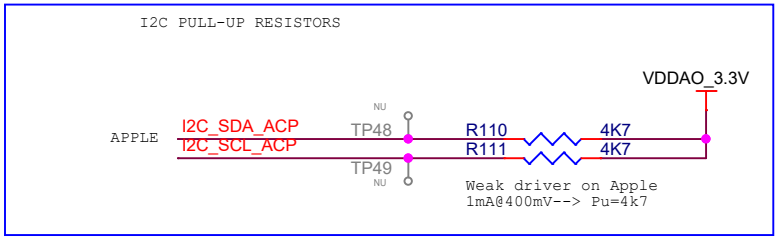
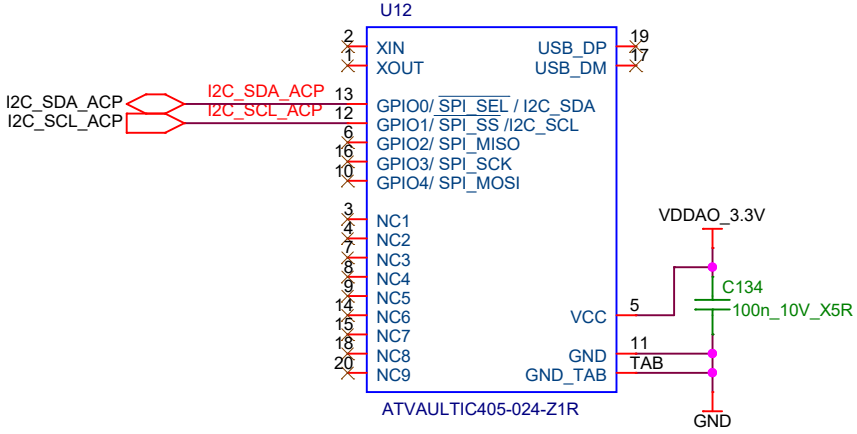
CRYPTO-AUTHENTIFICATION







MPP4

DATE	BoM	AUTHOR	HISTORY

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Author

Project Name_Gerber_BoM

MPP4_MB_HW03

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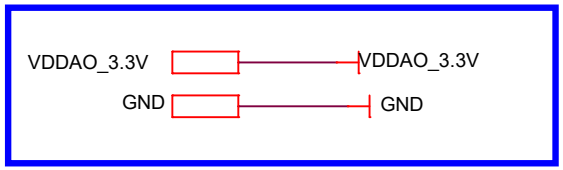
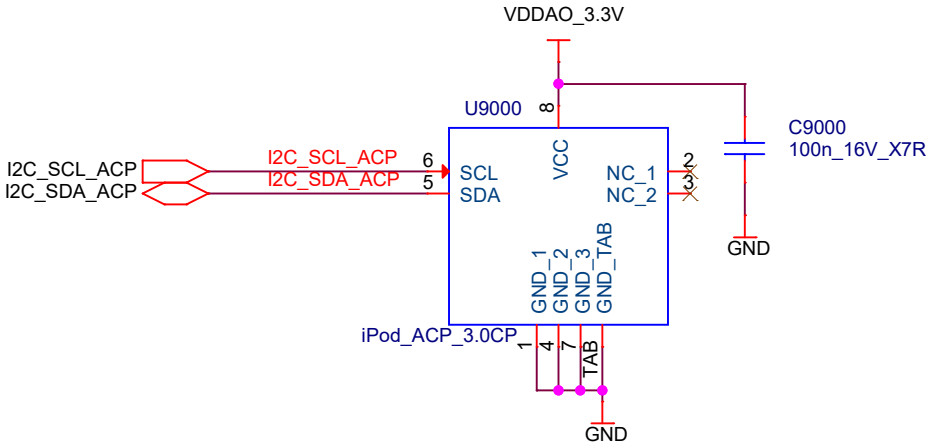
IPOD Controller



I2C address : 0x20/0x21



MPP4

DATE	BoM	AUTHOR	HISTORY

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Author <OrgAddr1>

Project Name_Gerber_BoM

MPP4_MB_HW03

Create date	Tuesday, December 10, 2019	Sheet 9 of 24	Size A
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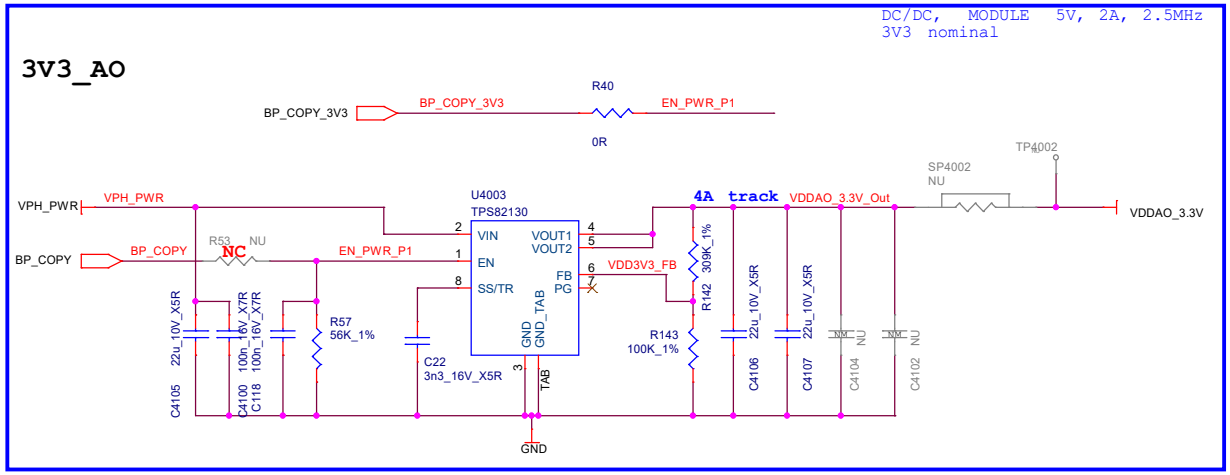

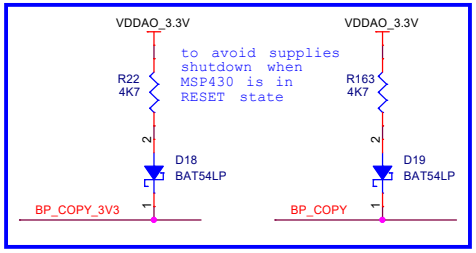

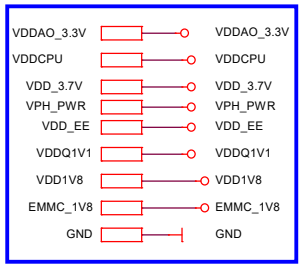

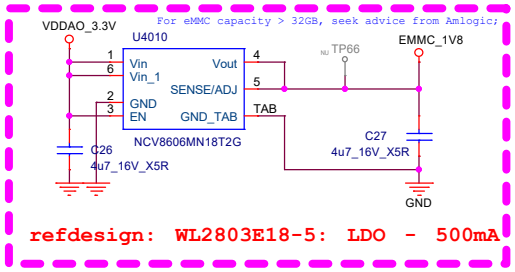

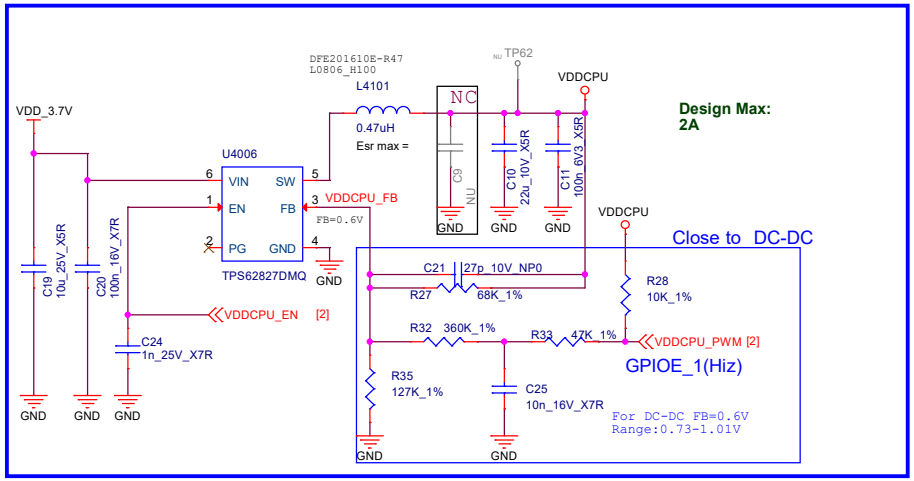

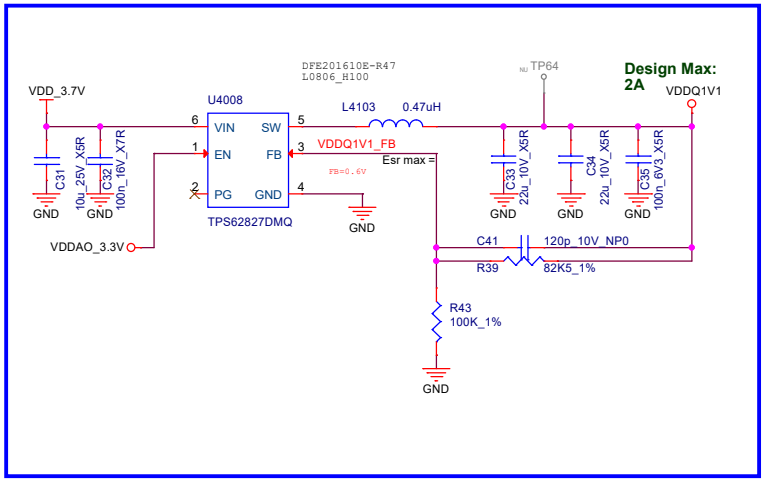

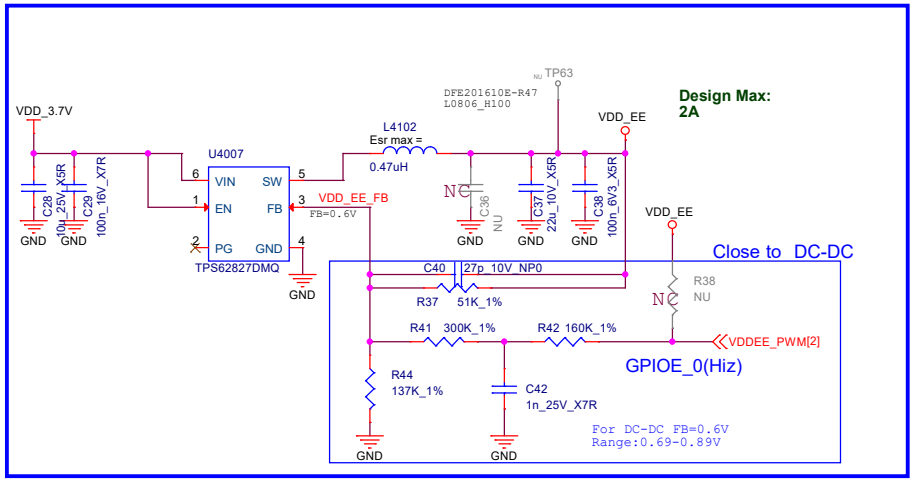

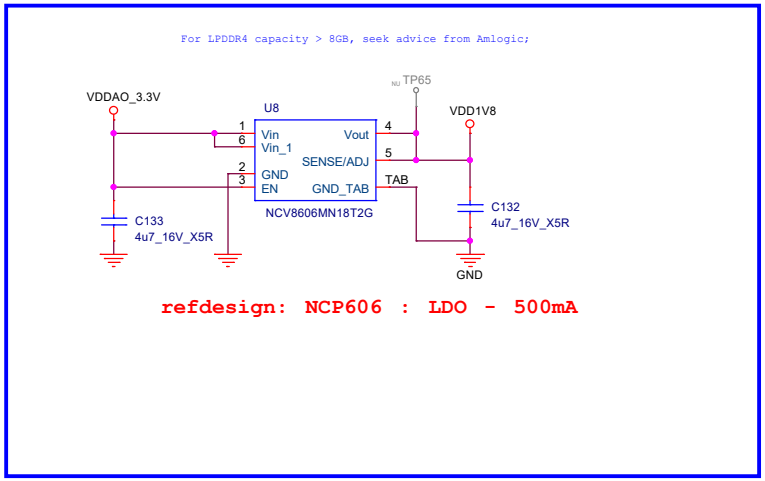

MPP4

DATE	BoM	AUTHOR	HISTORY

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Author

Project Name_Gerber_BoM

MPP4_MB_HW03

Create date	Tuesday, December 03, 2019	Sheet 10 of 24	Size A3
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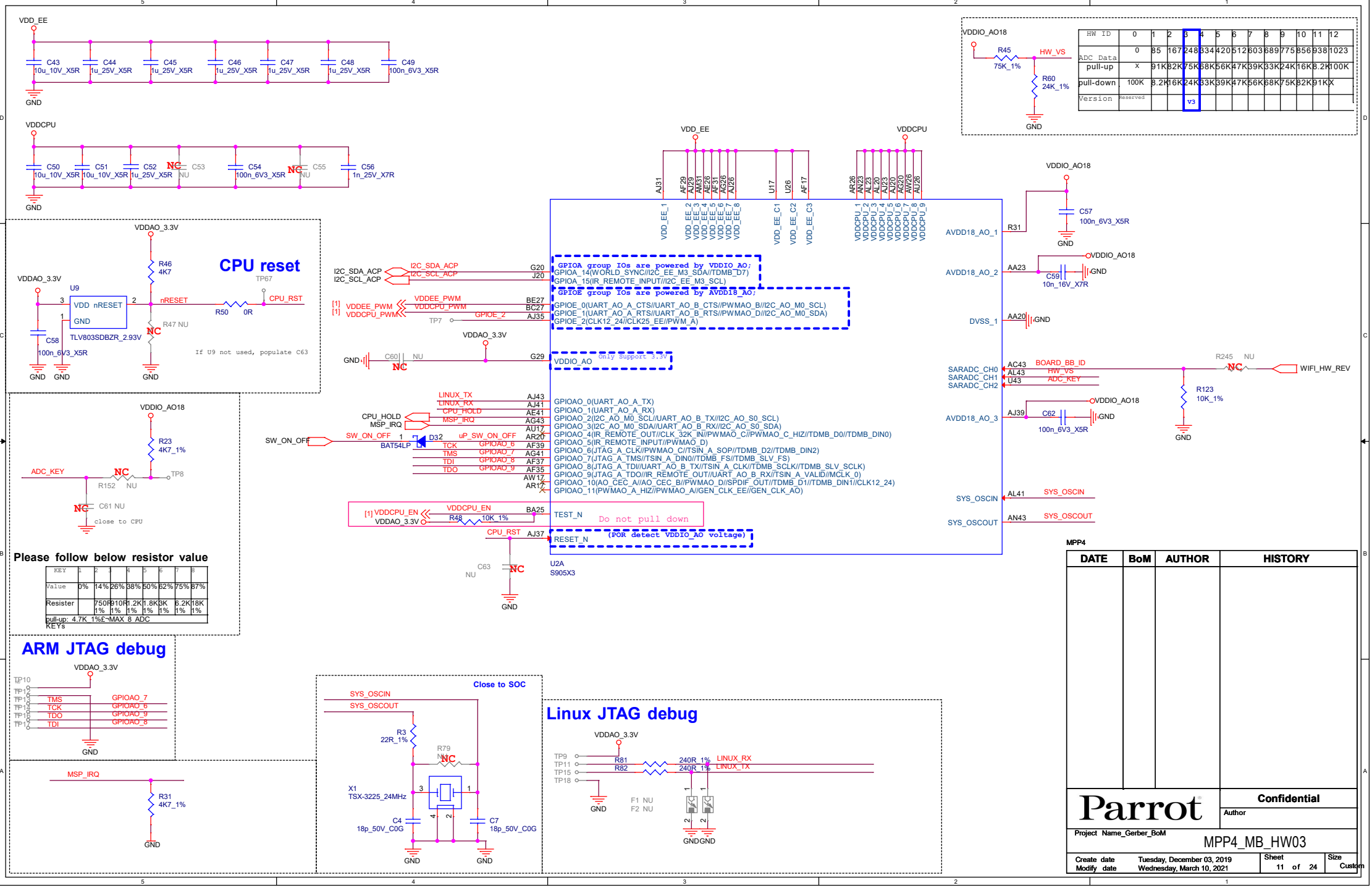
VDD_EE
C43 10u_10V_X5R
C44 1u_25V_X5R
C45 1u_25V_X5R
C46 1u_25V_X5R
C47 1u_25V_X5R
C48 1u_25V_X5R
C49 100n_6V3_X5R
GND
VDDCPU
C50 10u_10V_X5R
C51 10u_10V_X5R
C52 1u_25V_X5R
NC C53 NU
C54 100n_6V3_X5R
NC C55 NU
C56 1n_25V_X7R
VDDIO_AO18
R45 75K_1%
HW_VS
R60 24K_1%
HW ID 0 1 2 3 4 5 6 7 8 9 10 11 12
ADC Data 0 85 167 248 334 420 512 603 689 775 856 938 1023
pull-up X 91K 82K 75K 68K 56K 47K 39K 33K 24K 16K 8.2K 100K
pull-down 100K 8.2K 16K 24K 33K 39K 47K 56K 68K 75K 82K 91K X
Version Reserved v3
CPU reset
VDDAO_3.3V
R46 4K7
U9
VDD nRESET
GND
TLV803SDBZR_2.93V
nRESET
CPU_RST
TP67
R50 0R
R47 NU
NC
C58 100n_6V3_X5R
If U9 not used, populate C63
VDD_EE
VDDCPU
AJ31 AF29 AJ29 AW31 AE26 AE31 AG26 AJ26 U17 U26 AF17
AR26 AN23 AL23 AL20 AJ23 AJ20 AG20 AW26 AU26
VDD_EE_1 VDD_EE_2 VDD_EE_3 VDD_EE_4 VDD_EE_5 VDD_EE_6 VDD_EE_7 VDD_EE_8
VDD_EE_C1 VDD_EE_C2 VDD_EE_C3
VDDCPU_1 VDDCPU_2 VDDCPU_3 VDDCPU_4 VDDCPU_5 VDDCPU_6 VDDCPU_7 VDDCPU_8 VDDCPU_9
AVDD18_AO_1 R31
C57 100n_6V3_X5R
AVDD18_AO_2 AA23
C59 10n_16V_X7R
DVSS_1 AA20
I2C_SDA_ACP G20
I2C_SCL_ACP J20
GPIOA group IOs are powered by VDDIO_AO;
GPIOA_14(WORLD_SYNC//I2C_EE_M3_SDA//TDMB_D7)
GPIOA_15(IR_REMOTE_INPUT//I2C_EE_M3_SCL)
GPIOE group IOs are powered by AVDDI8_AO;
VDDEE_PWM BE27
VDDCPU_PWM BC27
GPIOE_2 AJ35
GPIOE_0(UART_AO_A_CTS//UART_AO_B_CTS//PWMAO_B//I2C_AO_M0_SCL)
GPIOE_1(UART_AO_A_RTS//UART_AO_B_RTS//PWMAO_D//I2C_AO_M0_SDA)
GPIOE_2(CLK12_24//CLK25_EE//PWM_A)
VDDIO_AO G29 Only Support 3.3V
C60 NU
LINUX_TX AJ43
LINUX_RX AJ41
CPU_HOLD AE41
MSP_IRQ AG43
AU17
SW_ON_OFF AR20
TCK AF39
TMS AG41
TDI AF37
TDO AF35
AW17
AR17
GPIOAO_0(UART_AO_A_TX)
GPIOAO_1(UART_AO_A_RX)
GPIOAO_2(I2C_AO_M0_SCL//UART_AO_B_TX//I2C_AO_S0_SCL)
GPIOAO_3(I2C_AO_M0_SDA//UART_AO_B_RX//I2C_AO_S0_SDA)
GPIOAO_4(IR_REMOTE_OUT//CLK_32K_IN//PWMAO_C//PWMAO_C_HIZ//TDMB_D0//TDMB_DIN0)
GPIOAO_5(IR_REMOTE_INPUT//PWMAO_D)
GPIOAO_6(JTAG_A_CLK//PWMAO_C//TSIN_A_SOP//TDMB_D2//TDMB_DIN2)
GPIOAO_7(JTAG_A_TMS//TSIN_A_DIN0//TDMB_FS//TDMB_SLV_FS)
GPIOAO_8(JTAG_A_TDI//UART_AO_B_TX//TSIN_A_CLK//TDMB_SCLK//TDMB_SLV_SCLK)
GPIOAO_9(JTAG_A_TDO//IR_REMOTE_OUT//UART_AO_B_RX//TSIN_A_VALID//MCLK_0)
GPIOAO_10(AO_CEC_A//AO_CEC_B//PWMAO_D//SPDIF_OUT//TDMB_D1//TDMB_DIN1//CLK12_24)
GPIOAO_11(PWMAO_A_HIZ//PWMAO_A//GEN_CLK_EE//GEN_CLK_AO)
SARADC_CH0 AC43 BOARD_BB_ID
SARADC_CH1 AL43 HW_VS
SARADC_CH2 U43 ADC_KEY
R245 NU
WIFI_HW_REV
R123 10K_1%
AVDD18_AO_3 AJ39
C62 100n_6V3_X5R
SYS_OSCIN AL41 SYS_OSCIN
SYS_OSCOUT AN43 SYS_OSCOUT
SW_ON_OFF
D32 BAT54LP
uP_SW_ON_OFF
GPIOAO_6
GPIOAO_7
GPIOAO_8
GPIOAO_9
[1] VDDCPU_EN VDDCPU_EN BA25
R48 10K_1%
TEST_N
Do not pull down
CPU_RST AJ37
RESET_N
(POR detect VDDIO_AO voltage)
C63 NU
U2A
S905X3
VDDIO_AO18
R23 4K7_1%
ADC_KEY
R152 NU
TP8
C61 NU
close to CPU
Please follow below resistor value
KEY 1 2 3 4 5 6 7 8
Value 0% 14% 26% 38% 50% 62% 75% 87%
Resister 750R 1% 910R 1% 1.2K 1% 1.8K 1% 3K 1% 6.2K 1% 18K 1%
pull-up: 4.7K 1%£-MAX 8 ADC KEYs
ARM JTAG debug
VDDAO_3.3V
TP10
TP11
TP12
TP13
TP14
TP15
TMS GPIOAO_7
TCK GPIOAO_6
TDO GPIOAO_9
TDI GPIOAO_8
MSP_IRQ
R31 4K7_1%
Close to SOC
SYS_OSCIN
SYS_OSCOUT
R3 22R_1%
R79 NU
X1 TSX-3225_24MHz
C4 18p_50V_C0G
C7 18p_50V_C0G
Linux JTAG debug
TP9
TP11
TP15
TP18
R81 240R_1% LINUX_RX
R82 240R_1% LINUX_TX
F1 NU
F2 NU
MPP4
DATE BoM AUTHOR HISTORY
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Author
Project Name_Gerber_BoM
MPP4_MB_HW03
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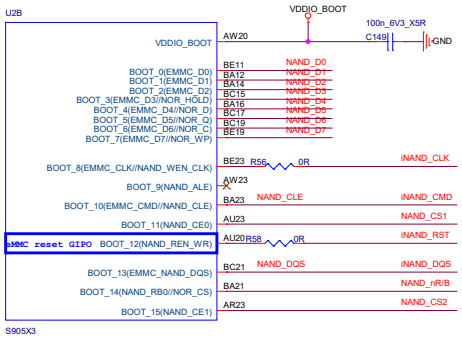
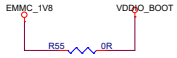
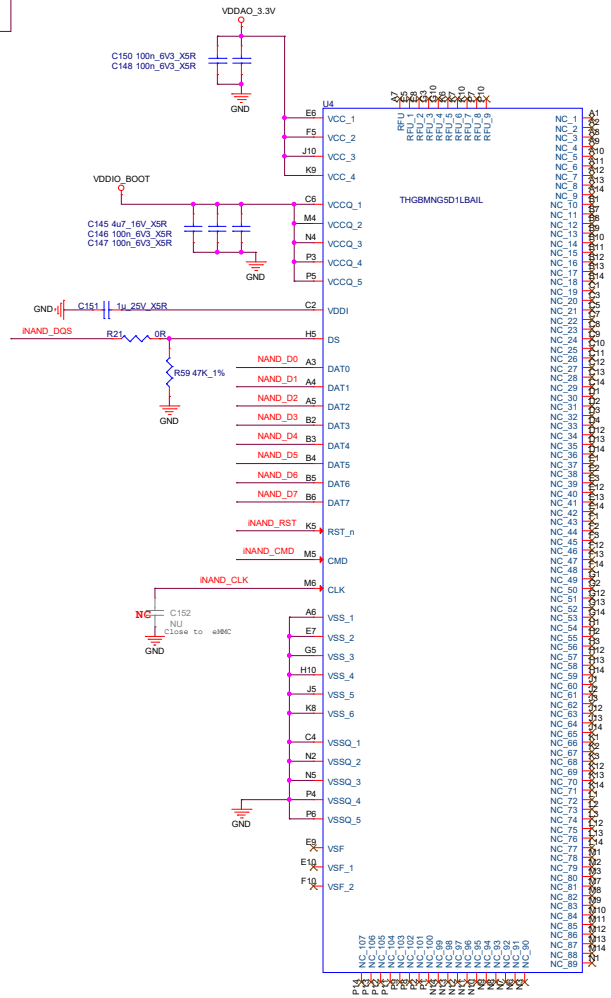
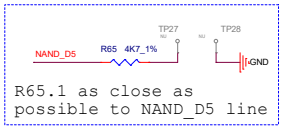


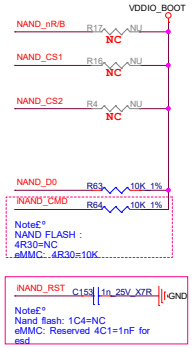




Power ON Config

BOOT_5[NAND_D5]: 0= USB Boot First





eMMC/iNAND

PCB Decal:153pin balls Type(BGA)

VCC = 2.7 -3.6V

eMMC_FLASH
BGA153-INAND

eMMC V5.0
eMMC NC PIN FOR ALLEGRO

MPP4

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Author

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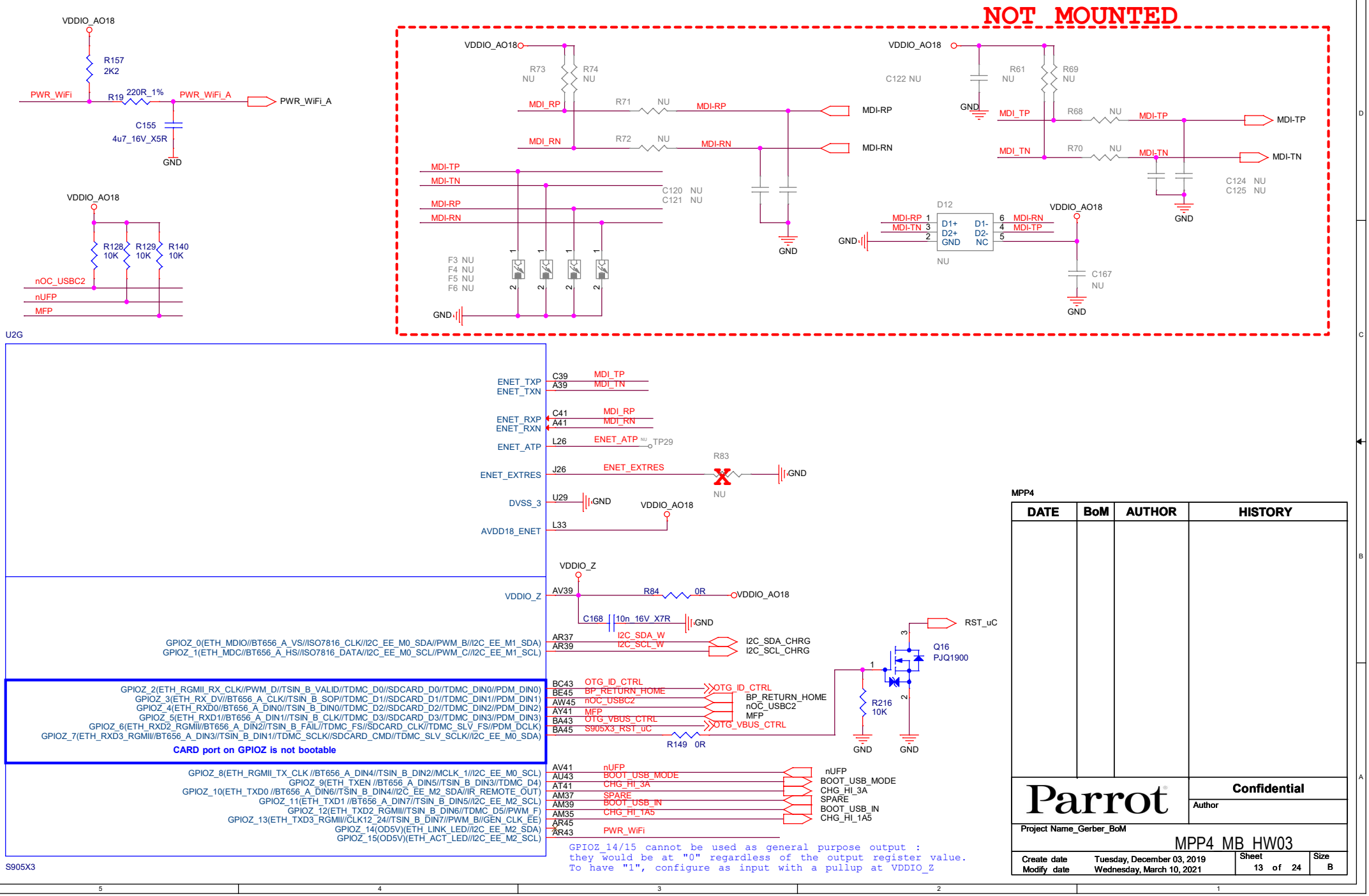
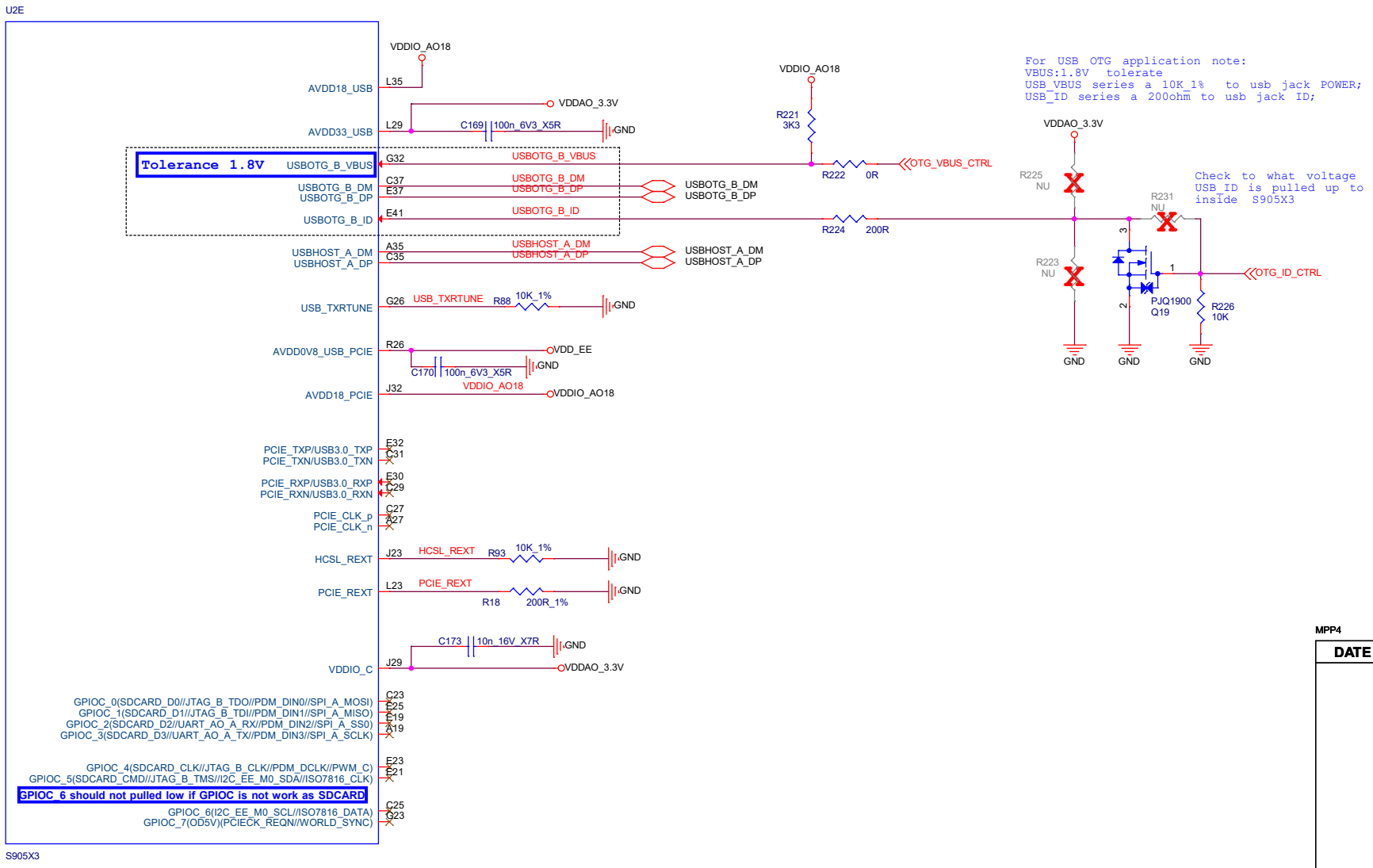

NOT MOUNTED
VDDIO_AO18
R157
2K2
PWR_WiFi
R19
220R_1%
PWR_WiFi_A
C155
4u7_16V_X5R
GND
R128
10K
R129
10K
R140
10K
nOC_USBC2
nUFP
MFP
R73
NU
R74
NU
MDI_RP
MDI_RN
R71
R72
MDI-RP
MDI-RN
MDI-TP
MDI-TN
C120 NU
C121 NU
F3 NU
F4 NU
F5 NU
F6 NU
C122 NU
R61
NU
R69
NU
R68
R70
C124 NU
C125 NU
D12
D1+
D2+
GND
D1-
D2-
NC
C167
NU
U2G
ENET_TXP
ENET_TXN
C39
A39
ENET_RXP
ENET_RXN
C41
A41
ENET_ATP
L26
TP29
ENET_EXTRES
J26
R83
DVSS_3
U29
AVDD18_ENET
L33
VDDIO_Z
AV39
R84
0R
C168
10n 16V X7R
GPIOZ_0(ETH_MDIO//BT656_A_VS//ISO7816_CLK//I2C_EE_M0_SDA//PWM_B//I2C_EE_M1_SDA)
GPIOZ_1(ETH_MDC//BT656_A_HS//ISO7816_DATA//I2C_EE_M0_SCL//PWM_C//I2C_EE_M1_SCL)
AR37
AR39
I2C_SDA_W
I2C_SCL_W
I2C_SDA_CHRG
I2C_SCL_CHRG
GPIOZ_2(ETH_RGMII_RX_CLK//PWM_D//TSIN_B_VALID//TDMC_D0//SDCARD_D0//TDMC_DIN0//PDM_DIN0)
GPIOZ_3(ETH_RX_DV//BT656_A_CLK//TSIN_B_SOP//TDMC_D1//SDCARD_D1//TDMC_DIN1//PDM_DIN1)
GPIOZ_4(ETH_RXD0//BT656_A_DIN0//TSIN_B_DIN0//TDMC_D2//SDCARD_D2//TDMC_DIN2//PDM_DIN2)
GPIOZ_5(ETH_RXD1//BT656_A_DIN1//TSIN_B_CLK//TDMC_D3//SDCARD_D3//TDMC_DIN3//PDM_DIN3)
GPIOZ_6(ETH_RXD2_RGMII//BT656_A_DIN2//TSIN_B_FAIL//TDMC_FS//SDCARD_CLK//TDMC_SLV_FS//PDM_DCLK)
GPIOZ_7(ETH_RXD3_RGMII//BT656_A_DIN3//TSIN_B_DIN1//TDMC_SCLK//SDCARD_CMD//TDMC_SLV_SCLK//I2C_EE_M0_SDA)
CARD port on GPIOZ is not bootable
BC43
BE45
AW45
AY41
BA43
BA45
OTG_ID_CTRL
BP_RETURN_HOME
nOC_USBC2
MFP
OTG_VBUS_CTRL
S905X3_RST_uC
R149 0R
RST_uC
Q16
PJQ1900
R216
10K
GPIOZ_8(ETH_RGMII_TX_CLK //BT656_A_DIN4//TSIN_B_DIN2//MCLK_1//I2C_EE_M0_SCL)
GPIOZ_9(ETH_TXEN //BT656_A_DIN5//TSIN_B_DIN3//TDMC_D4)
GPIOZ_10(ETH_TXD0 //BT656_A_DIN6//TSIN_B_DIN4//I2C_EE_M2_SDA//IR_REMOTE_OUT)
GPIOZ_11(ETH_TXD1 //BT656_A_DIN7//TSIN_B_DIN5//I2C_EE_M2_SCL)
GPIOZ_12(ETH_TXD2_RGMII//TSIN_B_DIN6//TDMC_D5//PWM_F)
GPIOZ_13(ETH_TXD3_RGMII//CLK12_24//TSIN_B_DIN7//PWM_B//GEN_CLK_EE)
GPIOZ_14(OD5V)(ETH_LINK_LED//I2C_EE_M2_SDA)
GPIOZ_15(OD5V)(ETH_ACT_LED//I2C_EE_M2_SCL)
AV41
AU43
AT41
AM37
AM39
AM35
AR45
AR43
nUFP
BOOT_USB_MODE
CHG_HI_3A
SPARE
BOOT_USB_IN
CHG_HI_1A5
PWR_WiFi
GPIOZ_14/15 cannot be used as general purpose output :
they would be at "0" regardless of the output register value.
To have "1", configure as input with a pullup at VDDIO_Z
S905X3
MPP4
DATE
BoM
AUTHOR
HISTORY
Parrot
Confidential
Author
Project Name_Gerber_BoM
MPP4_MB_HW03
Create date
Tuesday, December 03, 2019
Modify date
Wednesday, March 10, 2021
Sheet
13 of 24
Size
B



MPP4

DATE	BoM	AUTHOR	HISTORY

Parrot

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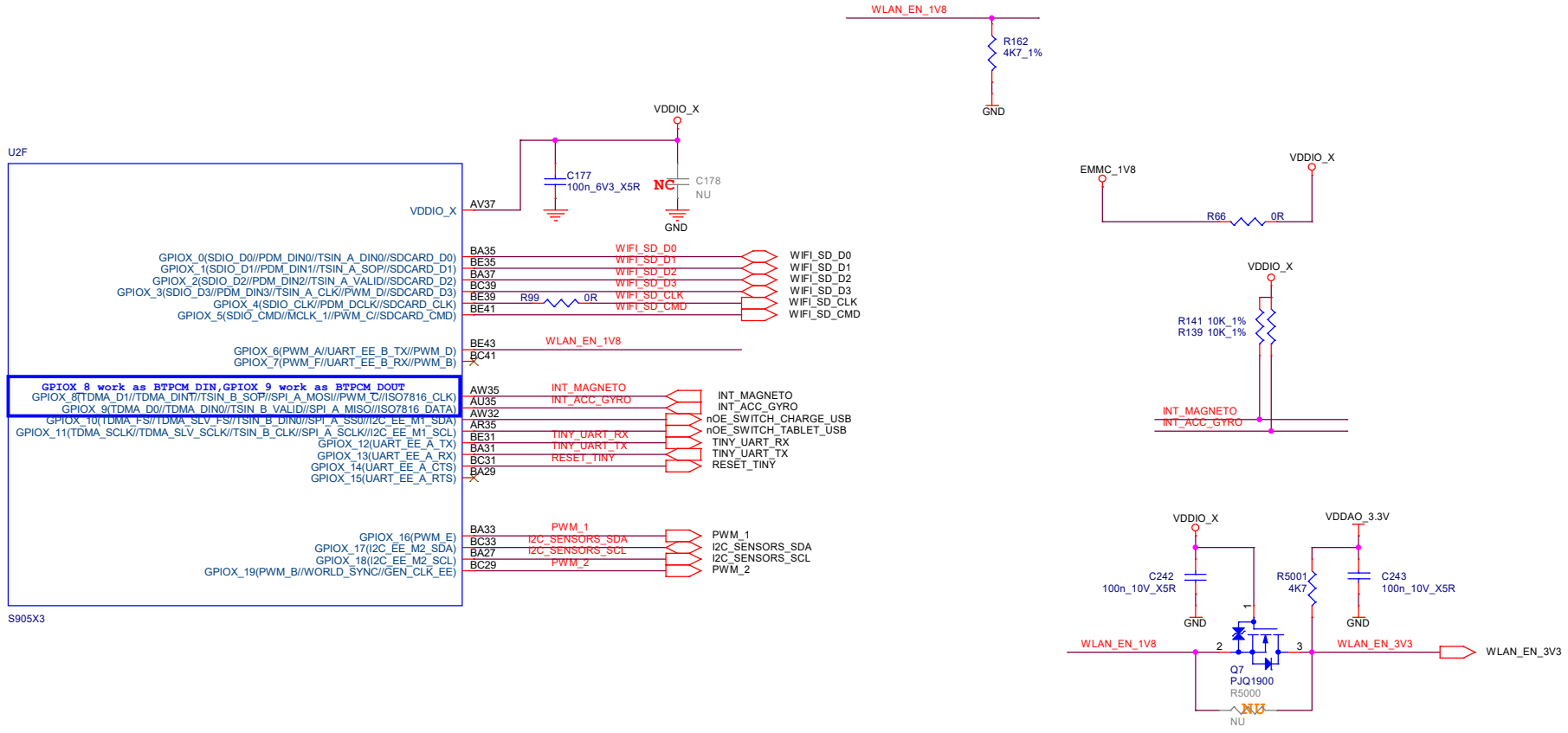
Author

Project Name_Gerber_BoM

MPP4_MB_HW03

Create date	Tuesday, December 03, 2019	Sheet 14 of 24	Size Custom
Modify date	Wednesday, March 10, 2021		



MPP4

DATE	BoM	AUTHOR	HISTORY

Parrot

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Author

Project Name_Gerber_BoM

MPP4_MB_HW03

Create date	Tuesday, December 03, 2019	Sheet 15 of 24	Size A3
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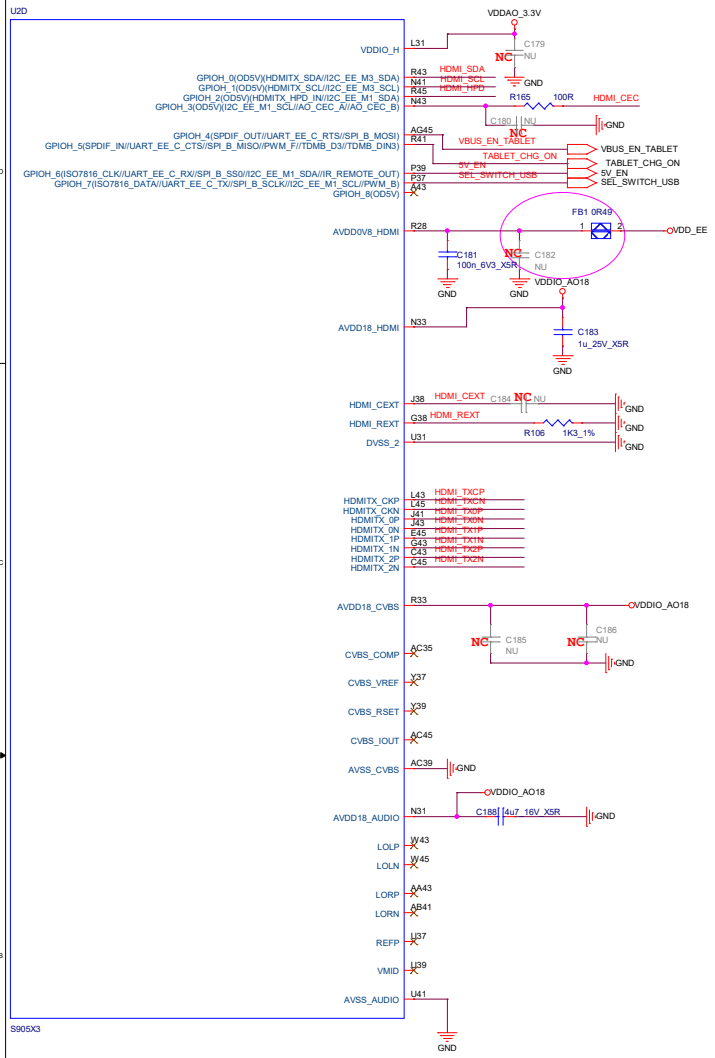
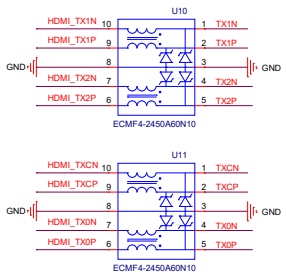
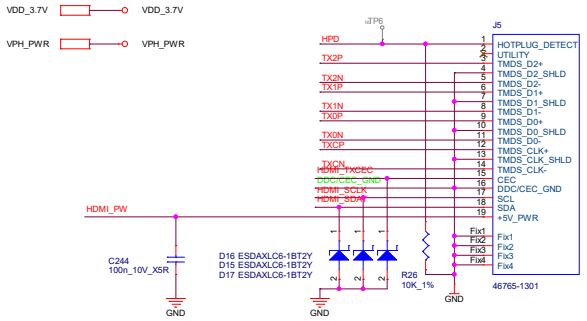
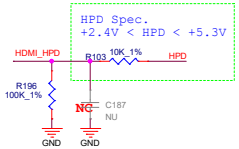
HDMI output

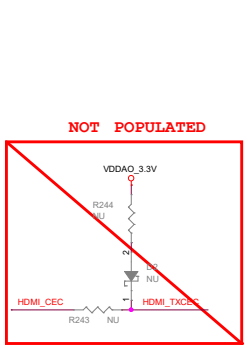




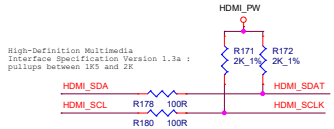


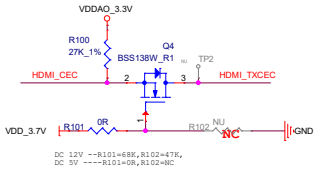


Do not delete 9R16 R103 resistors

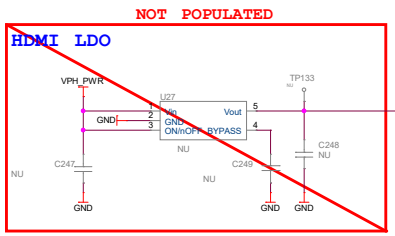


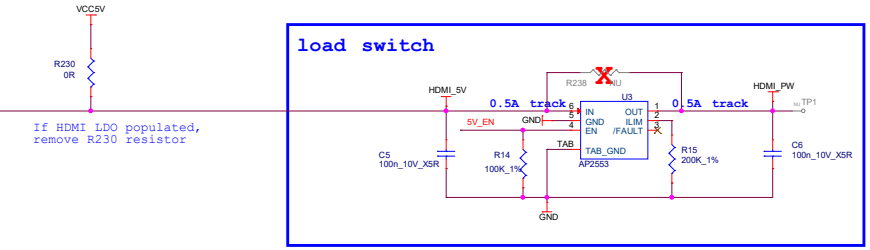
To test as a replacement of current NMOS design
If CEC line capacitance is still too high





DC 12V --R101=68K,R102=47K,
DC 5V ----R101=0R,R102=NC





Required (HDMI certification) :
4.8V < HDMI_PWR < 5.3V
55mA < HDMI_SC_CURRENT < 500mA

***** current limit *****
Rlim min : 10K ; Rlim max : 210K

With 200K - 1%
min : 127mA
typ : 148mA
max : 168mA

MPP4

DATE	BoM	AUTHOR	HISTORY

Parrot

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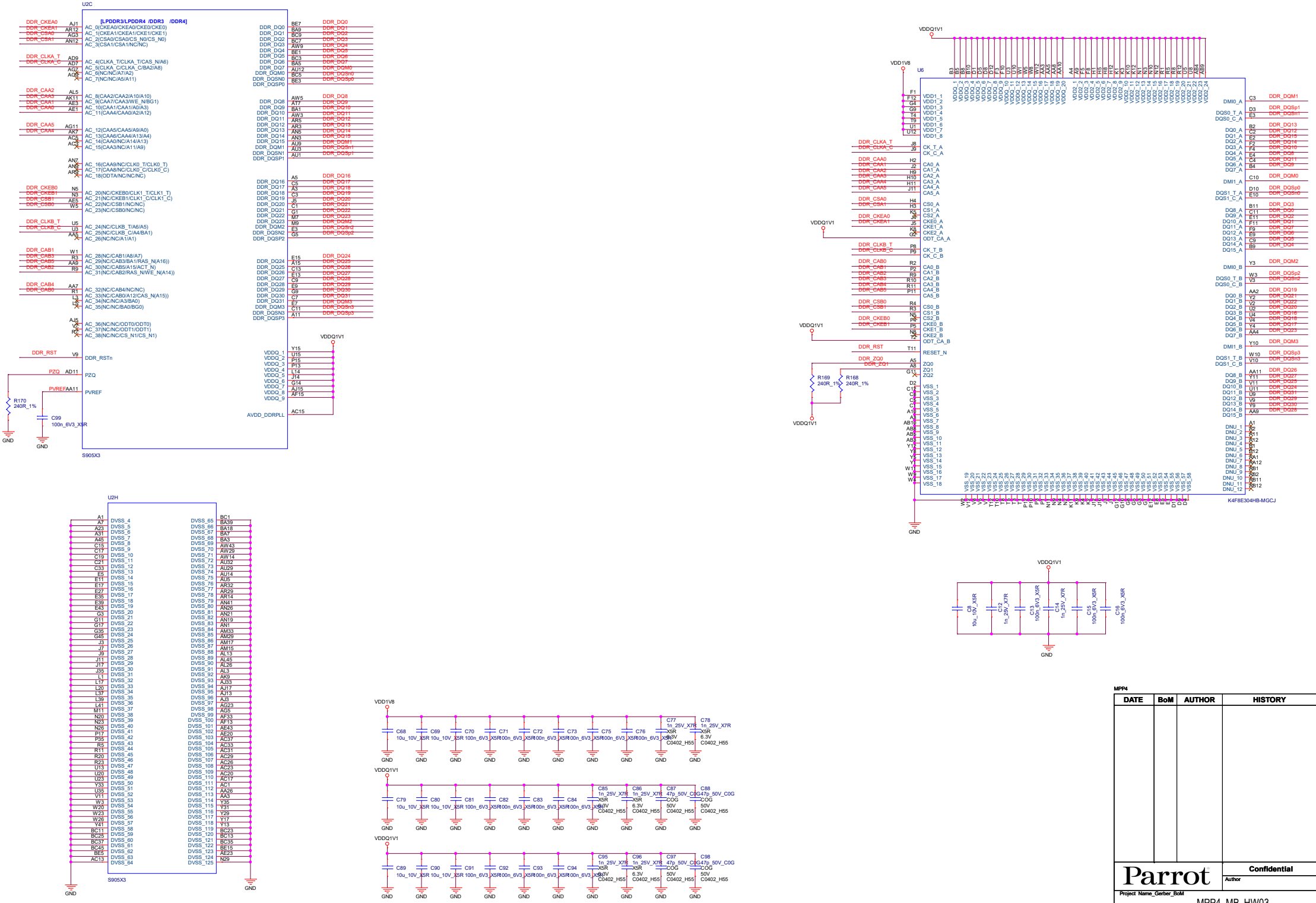
Author

Project Name_Gerber_BoM

MPP4_MB_HW03

Create date	Tuesday, December 03, 2019	Sheet 16 of 24	Size A2
Modify date	Wednesday, March 10, 2021		



MPP4

DATE	BoM	AUTHOR	HISTORY

Parrot

Confidential

Author

Project Name_Gerber_BoM

MPP4 MB HW03

Create date	Tuesday, January 14, 2020	Sheet 17 of 24	Size A2
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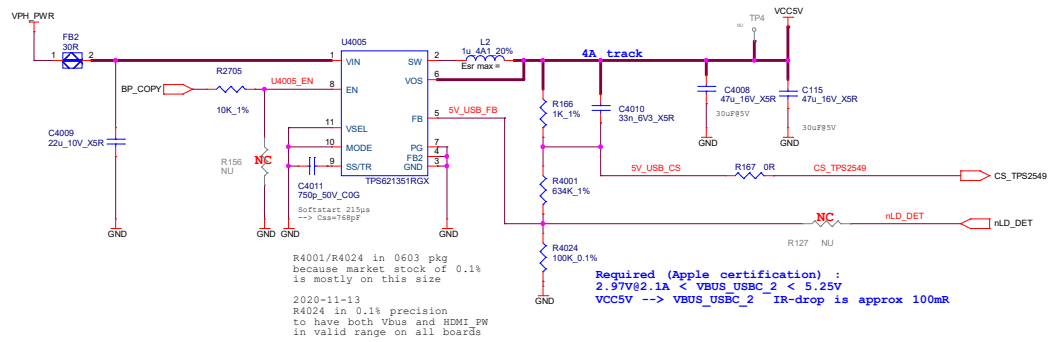
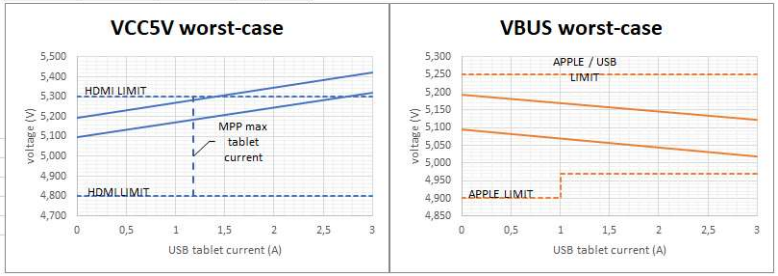
POWER SUPPLY

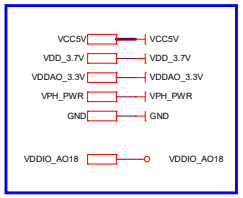
5V USB HDMI



New resistors		tolerance
R166 :	1 kΩ	0,01
R4001 :	634 kΩ	0,01
R4024 :	100 kΩ	0,001

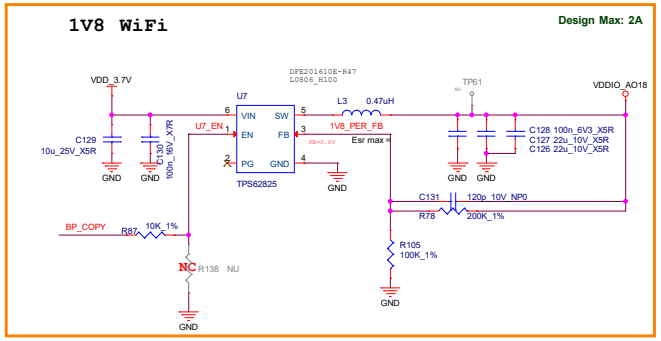


Dotted lines : limits
plain lines : min-max voltages due to feedback resistors tolerance



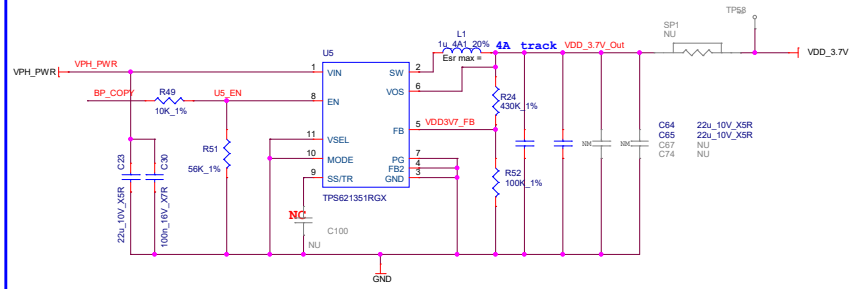
1V8 WiFi

Design Max: 2A



3V7

DC/DC, MODULE 12V, 3.5A, 2.5MHz
3V7 nominal



MPP4

DATE	BoM	AUTHOR	HISTORY

Parrot

Confidential

Author

Project Name_Gerber_BoM MPP4_MB_HW03

Create date Tuesday, December 10, 2019
Modify date Wednesday, March 10, 2021

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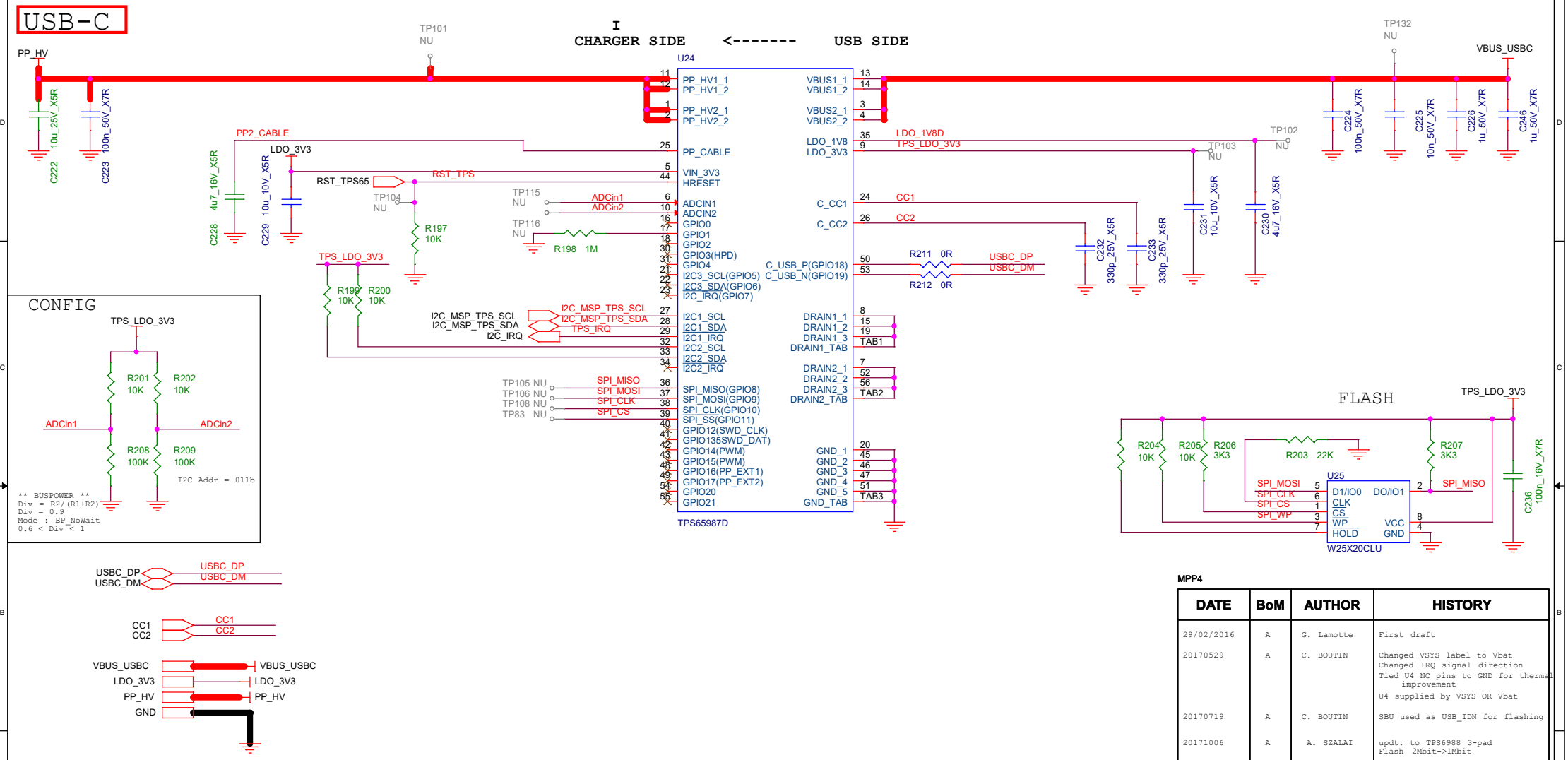
Size A2



MPP4

DATE	BoM	AUTHOR	HISTORY
29/02/2016	A	G. Lamotte	First draft
20170529	A	C. BOUTIN	Changed VSYS label to Vbat Changed IRQ signal direction Tied U4 NC pins to GND for thermal improvement U4 supplied by VSYS OR Vbat
20170719	A	C. BOUTIN	SBU used as USB_IDN for flashing
20171006	A	A. SZALAI	updt. to TPS6988 3-pad Flash 2Mbit->1Mbit
20171026 201710102	A	C. BOUTIN	reverted to 1Mbit for security U8 pin swap for better routing

Schematic statut: [X] Draft [ ] Reviewed [ ] Approved

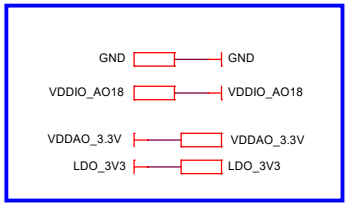
Parrot

Confidential

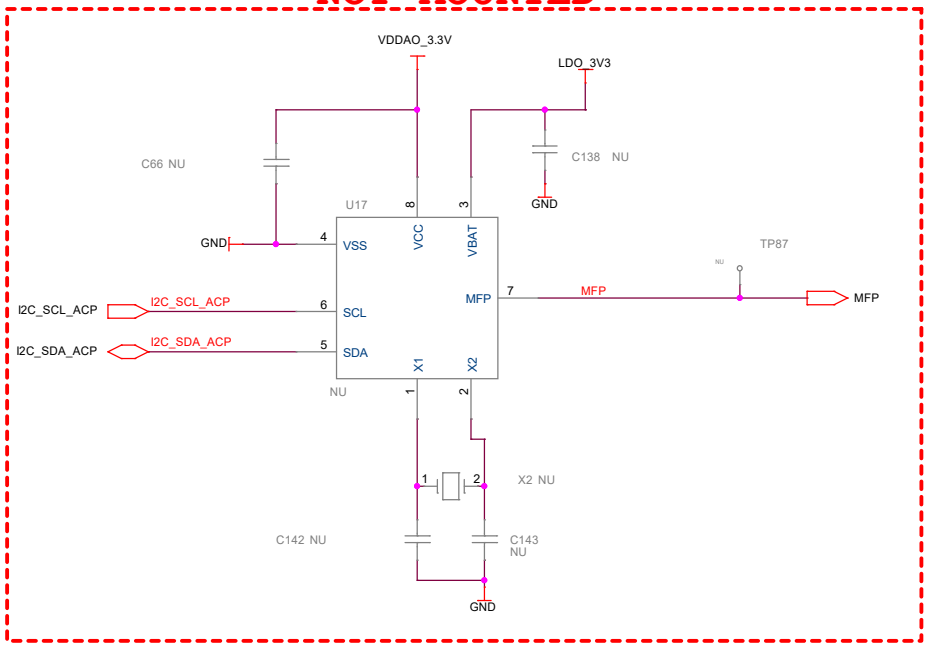
Author <Author>

Size A4 | Project Name_Gerber_BoM | MPP4_MB_HW03

Date: Wednesday, March 10, 2021 | Sheet 19 of 24



NOT MOUNTED



MPP4

DATE	BoM	AUTHOR	HISTORY

Parrot

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Author

Project Name_Gerber_BoM

MPP4_MB_HW03

Create date	Friday, February 07, 2020	Sheet 20 of 24	Size A3
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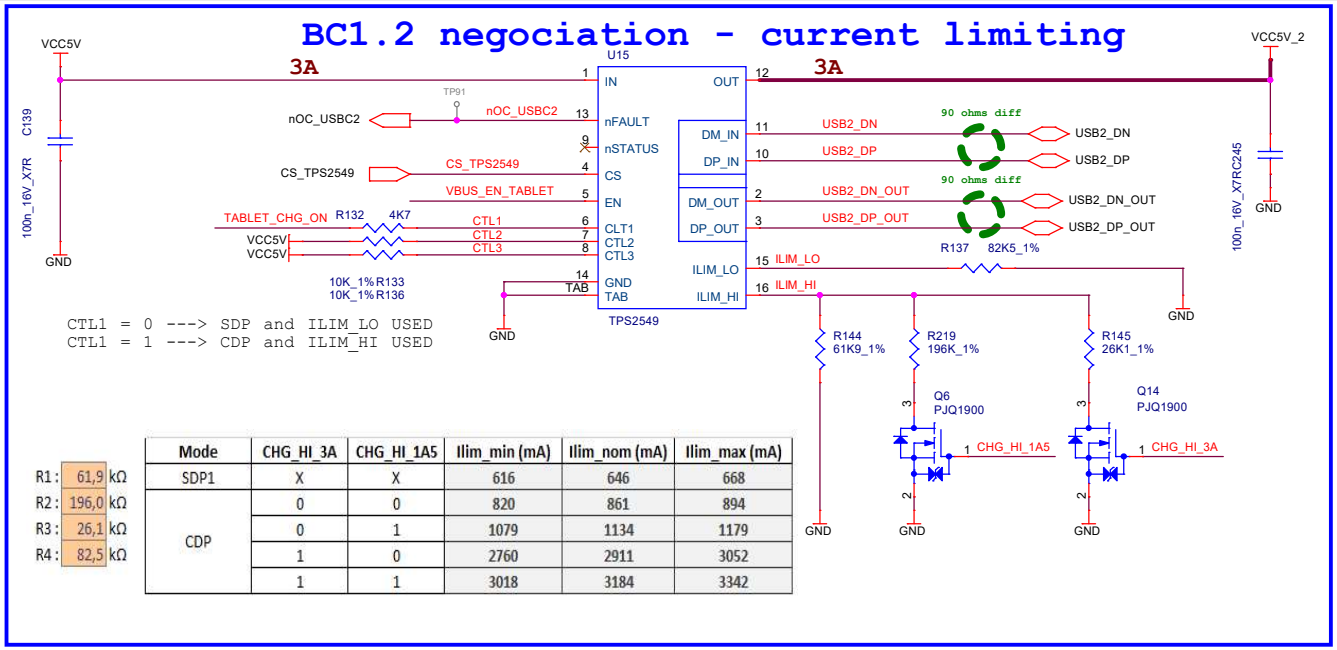
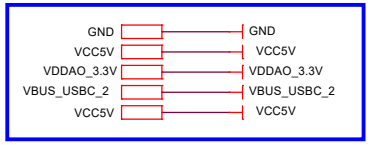
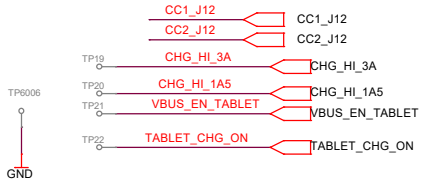
USB

BC1.2 negociation - current limiting

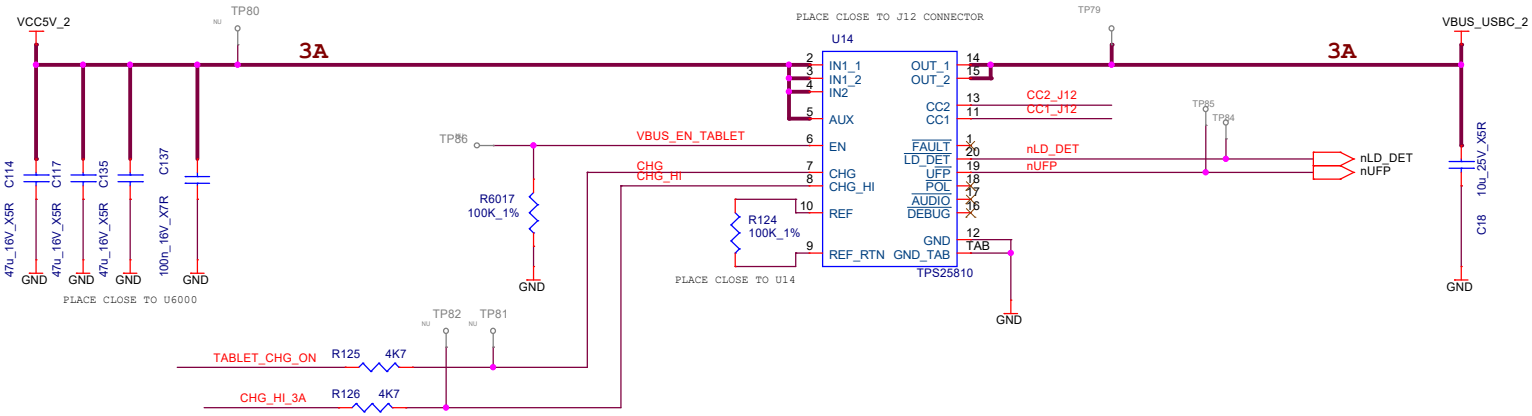


			Mode	CHG_HI_3A	CHG_HI_1A5	Ilim_min (mA)	Ilim_nom (mA)	Ilim_max (mA)
R1 :	61,9	kΩ	SDP1	X	X	616	646	668
R2 :	196,0	kΩ	CDP	0	0	820	861	894
R3 :	26,1	kΩ		0	1	1079	1134	1179
R4 :	82,5	kΩ		1	0	2760	2911	3052
				1	1	3018	3184	3342





PD negociation - load switch



HW03						
GPIOH_5 (TABLET_CHG_ON)	GPIOZ_10 (CHG_HI_3A)	GPIOZ_13 (CHG_HI_1A5)	TPS2549 MODE	TPS2549 CURRENT LIMIT (mA)	TPS25810 CC BROADCAST (mA)	TPS25810 CURRENT LIMIT (mA)
0	X	X	SDP (500mA)	646	500	1700
1	0	0	CDP (1500mA)	861	1500	1700
	0	1		1134	1500	1700
	1	0		2911	3000	3400
	1	1		3184	3000	3400

MPP4

DATE	BoM	AUTHOR	HISTORY

Parrot

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Author <OrgAddr1>

Project Name_Gerber_BoM

MPP4 MB HW03

Create date Tuesday, December 10, 2019

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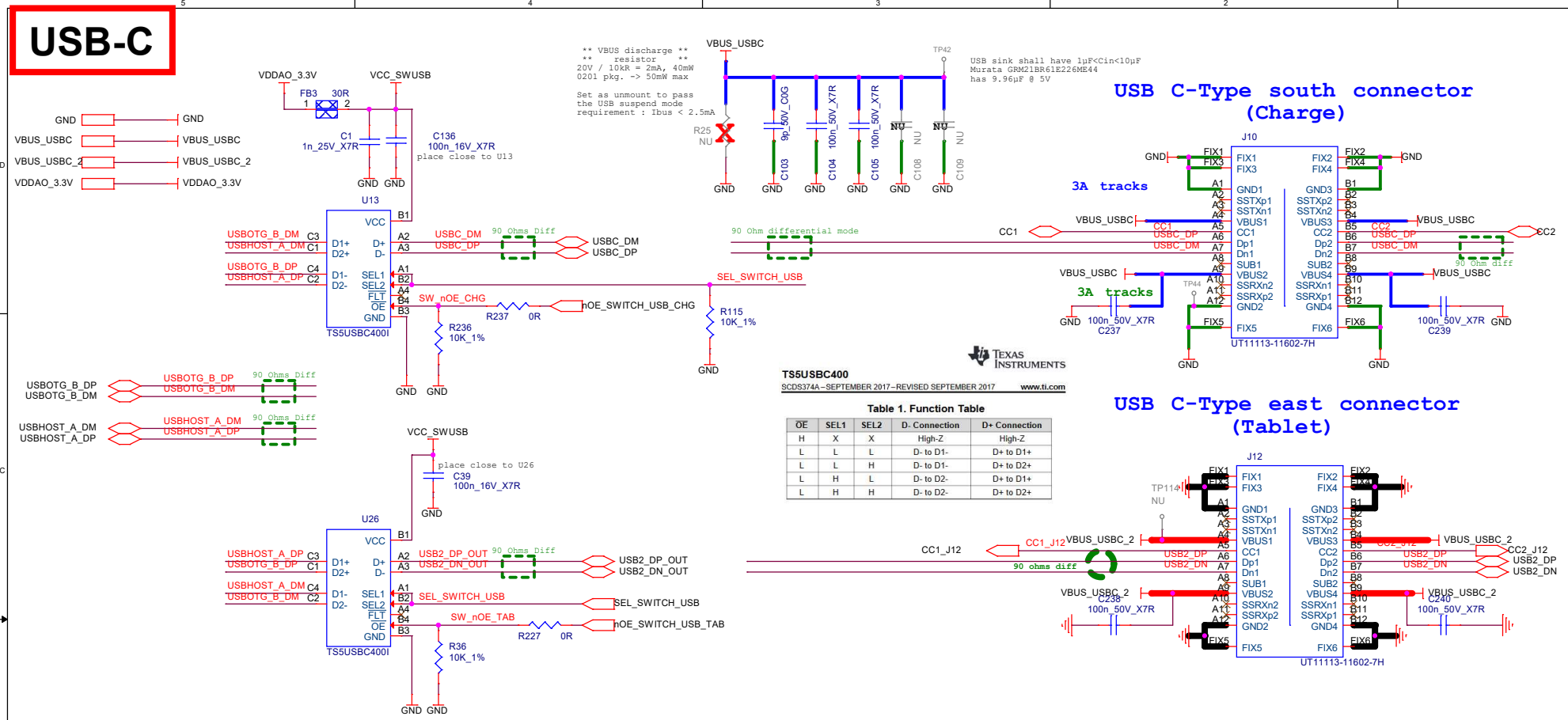
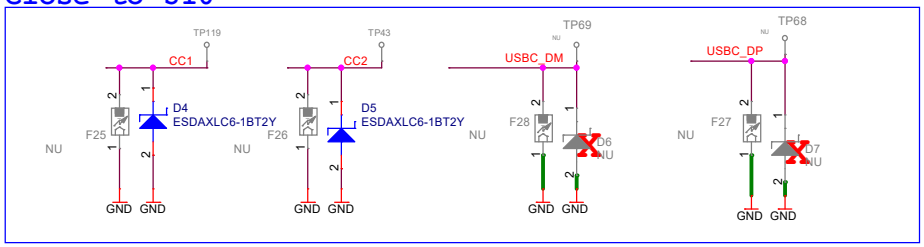
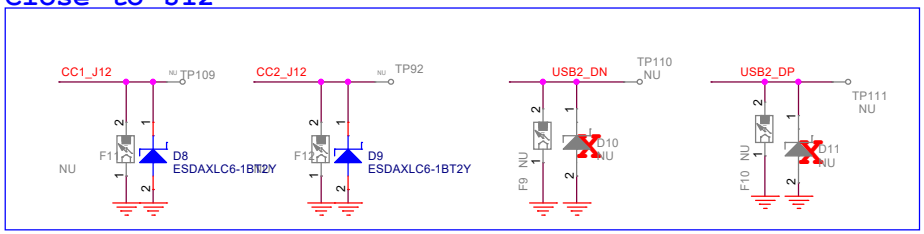
USB-C



Close to J10



Close to J12



MPP4

DATE	BoM	AUTHOR	HISTORY

Parrot

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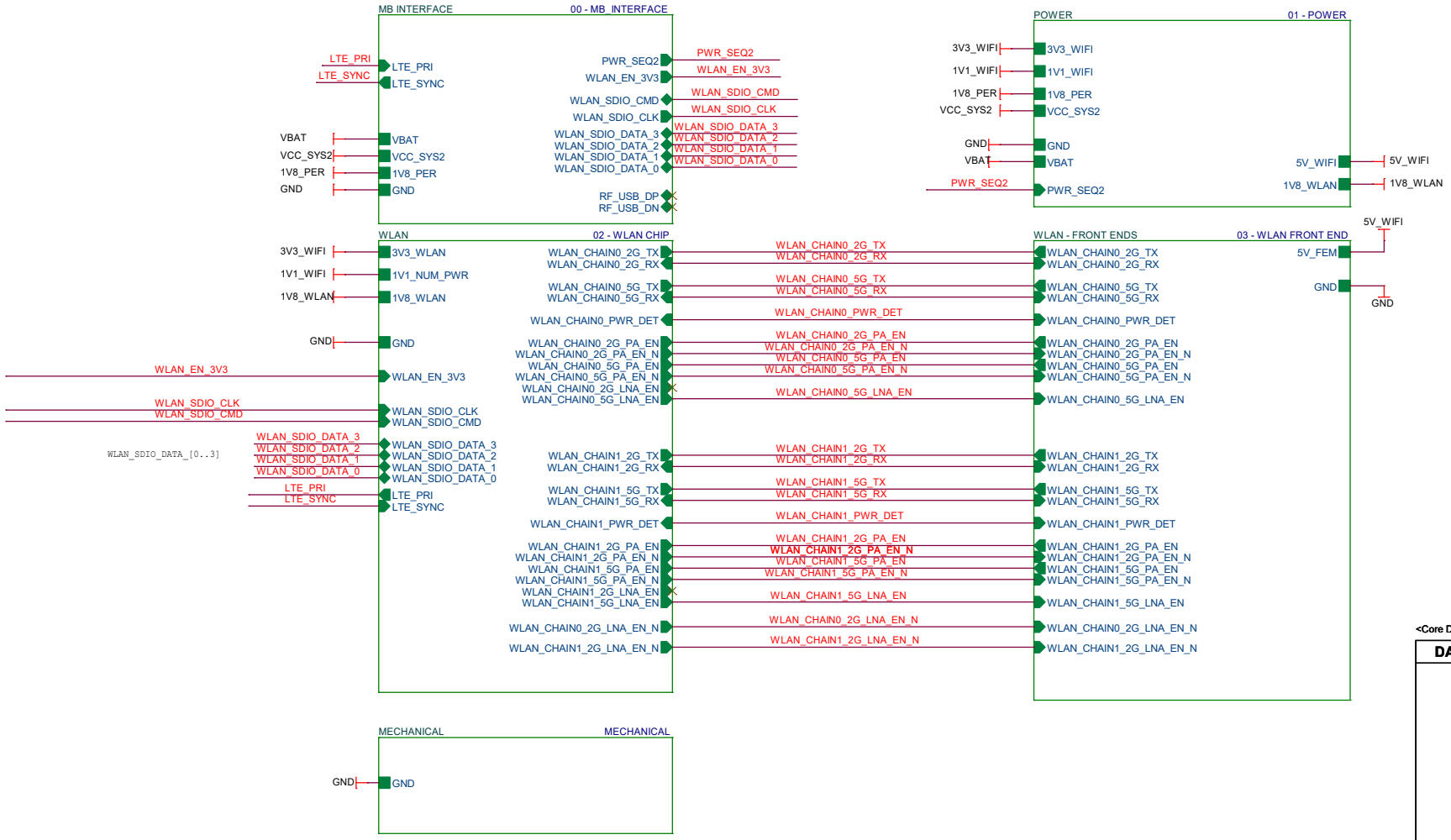
Author

Project Name_Gerber_BoM

MPP4 MB HW03

Create date	Thursday, February 06, 2020	Sheet 24 of 24	Size A3
Modify date	Wednesday, March 10, 2021		

ROOT



<Core Design>

DATE	BoM	AUTHOR	HISTORY

Parrot

Confidential

Author

Project Name_Gerber_BoM

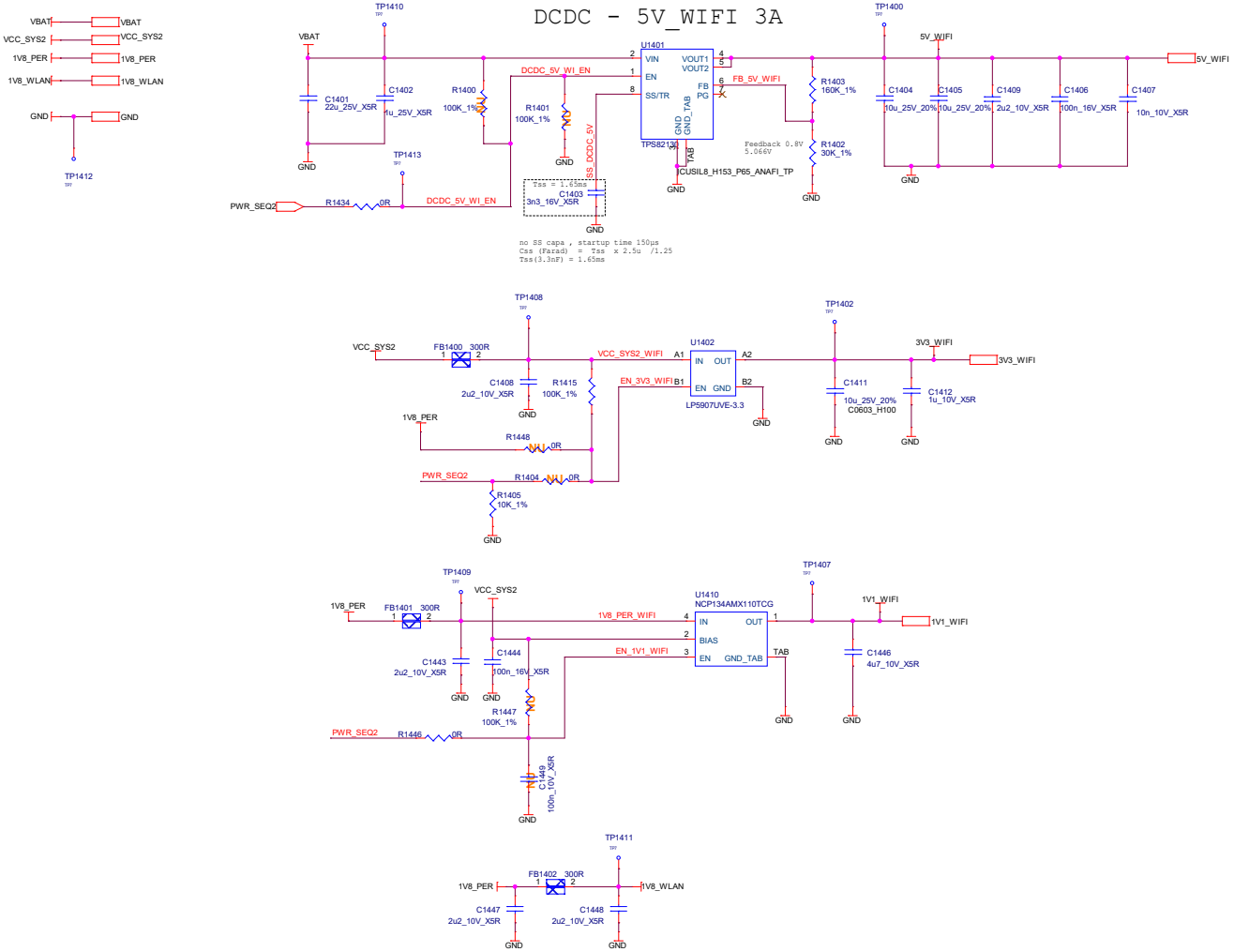
MPP4_DB_WIFI_HW03

Create date	Friday, March 15, 2019	Sheet	Size
Modify date	Tuesday, November 10, 2020	2 of 31	A3

POWER

ref des 1400 => 1499

WIFI



<Core Design>

DATE	BoM	AUTHOR	HISTORY

Schematic statut: [X] Draft [ ] Reviewed [ ] Approved

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Author

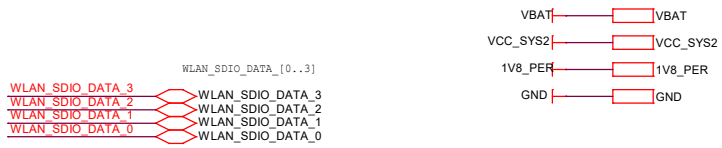
Size A4

Project Name_Gerber_BoM

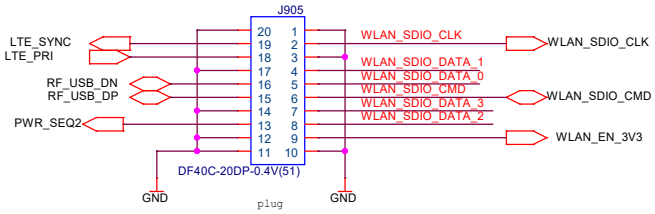
MPP4_DB_WIFI_HW03

Date: Wednesday, November 11, 2020 Sheet 6 of 31

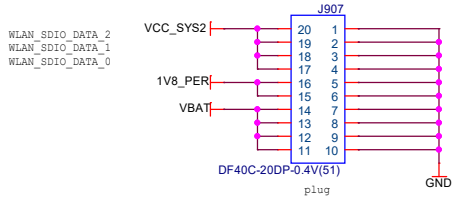
RF Daughter Board SIDE : Plug



Should be place in the left side in Layout according to J900 position in Mother Board



Should be place in the right side in Layout according to J901 position in Mother Board



<Core Design>

DATE	BoM	AUTHOR	HISTORY

Schematic statut [X] Draft [ ] Reviewed [ ] Approved

Parrot

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Author

Size A4

Project Name_Gerber_BoM

MPP4_DB_WIFI_HW03

Date: Wednesday, November 11, 2020

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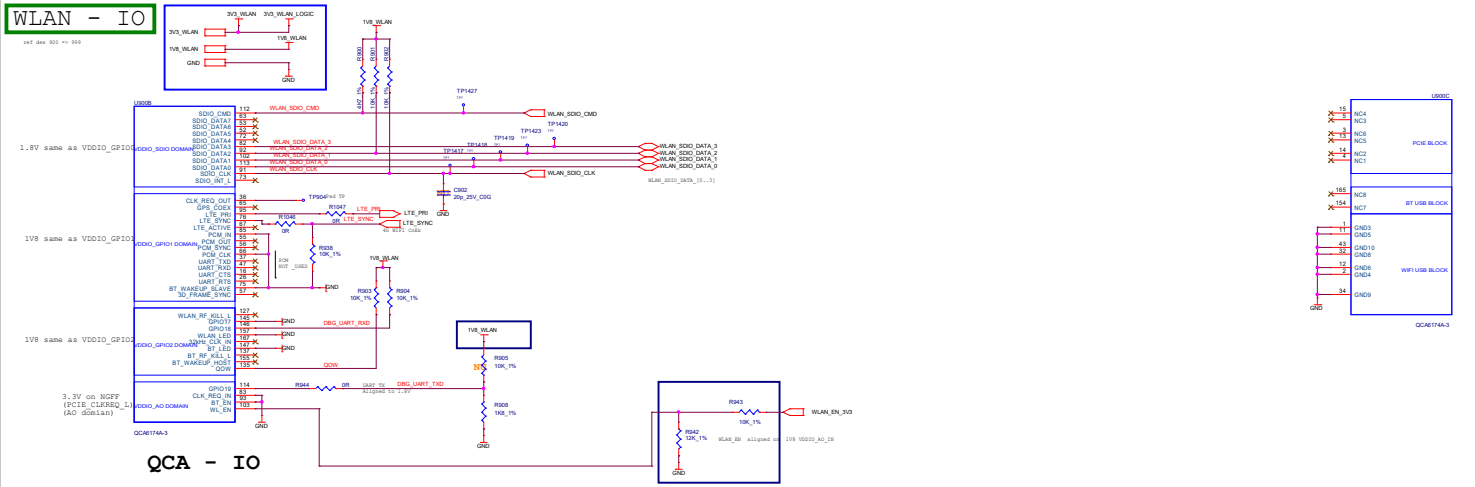
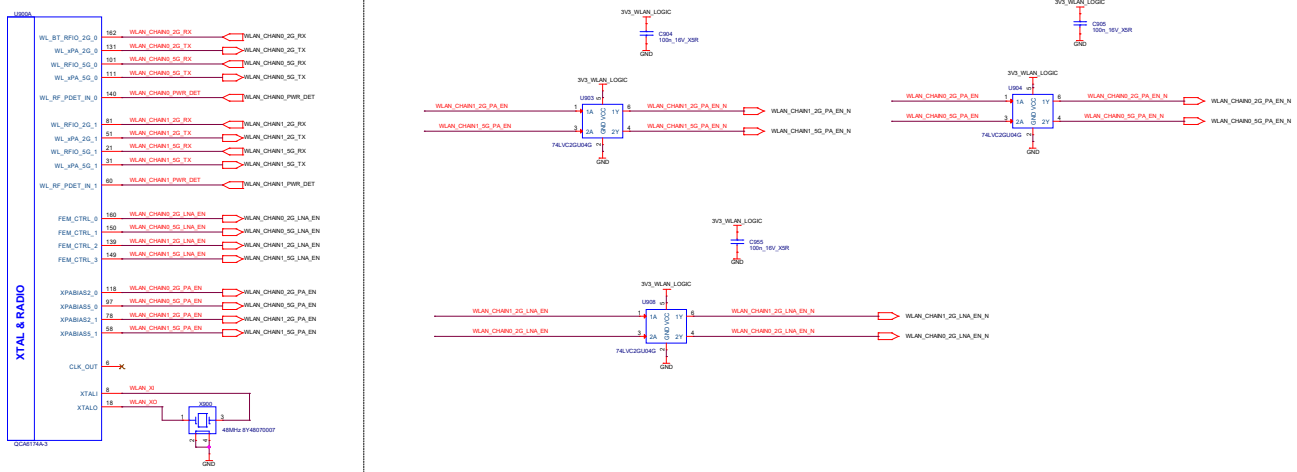
WLAN - IO

ref des 900 => 999



QCA - IO

QCA - LOGIC



2016size

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Mouser 581-CX201409450W91A2

New QC suggested ref :
TXC 8Y48070007

<Core Design>

DATE	BoM	AUTHOR	HISTORY

Parrot

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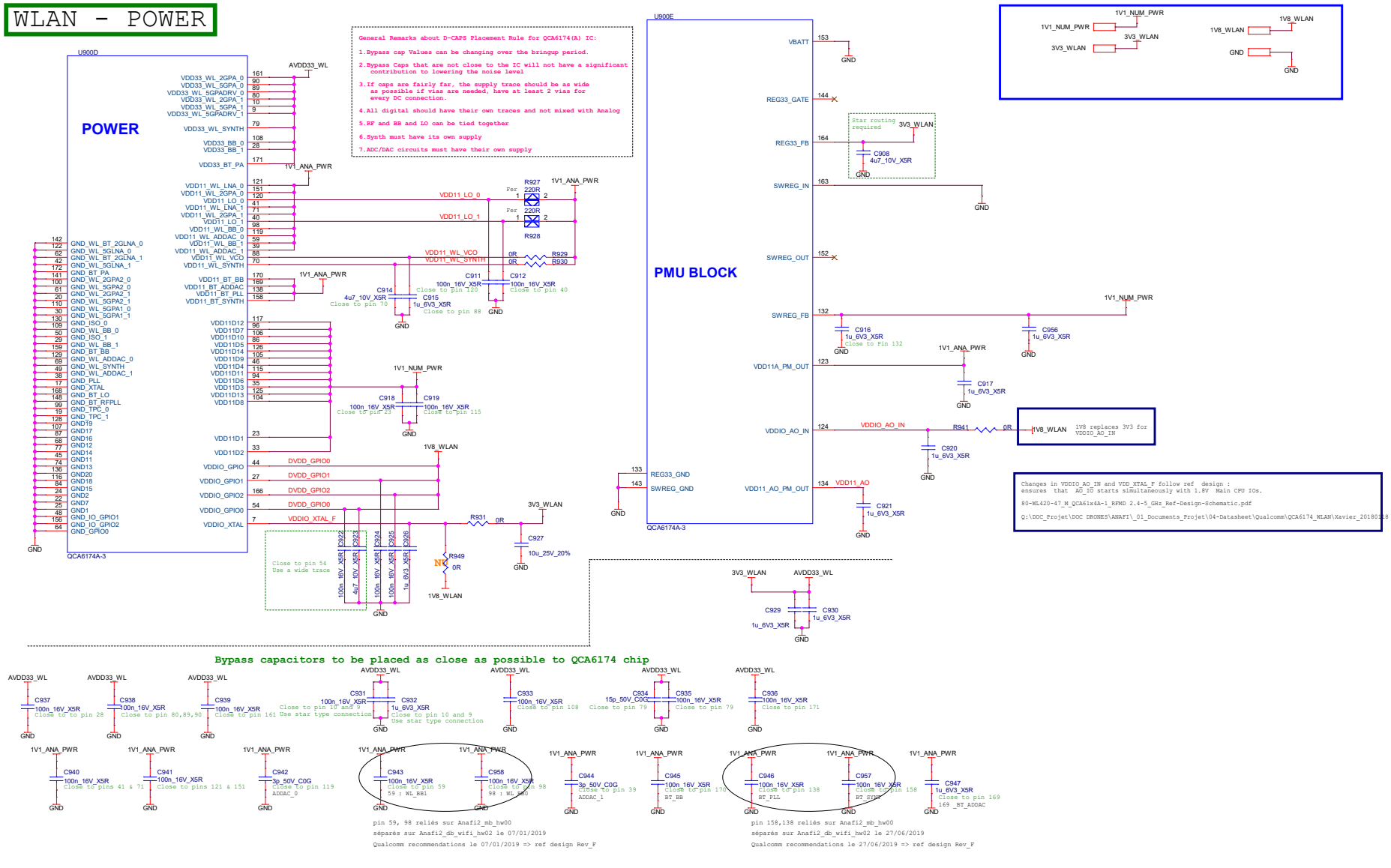
Author

Project Name_Gerber_BoM

MPP4_DB_WIFI_HW03

Create date	Tuesday, July 28, 2015	Sheet 26 of 31	Size A1
Modify date	Wednesday, November 11, 2020		

WLAN - POWER



Bypass capacitors to be placed as close as possible to QCA6174 chip

pin 59, 98 reliés sur Anafi2_mb_hw00
séparés sur Anafi2_db_wifi_hw02 le 07/01/2019
Qualcomm recommendations le 07/01/2019 => ref design Rev_F

pin 158,138 reliés sur Anafi2_mb_hw00
séparés sur Anafi2_db_wifi_hw02 le 27/06/2019
Qualcomm recommendations le 27/06/2019 => ref design Rev_F

<Core Design>

DATE	BoM	AUTHOR	HISTORY
01/10/2018	00_A	JY CASTETS	Initiale release
23/01/2019	01	JY CASTETS	remove internal DCDC 1V1

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Author

Project Name_Gerber_BoM

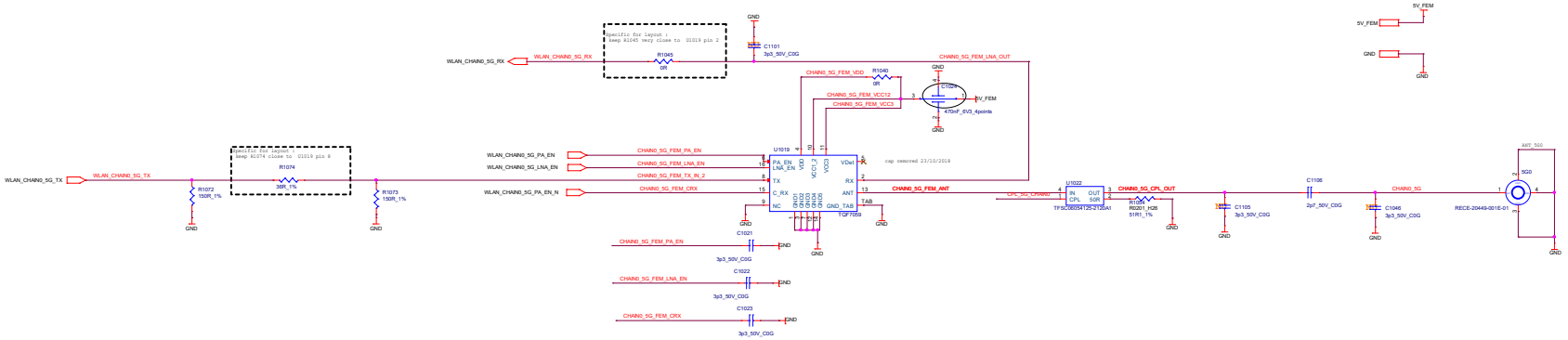
MPP4_DB_WIFI_HW03

Create date	Tuesday, July 26, 2016	Sheet	Size
Modify date	Tuesday, November 10, 2020	27 of 31	A2

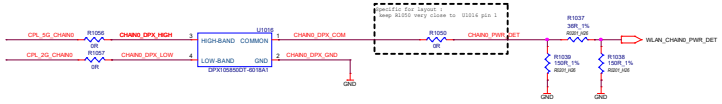
FEM_CHAIN0

Source design for RF CHAIN :
WIFI_HIGH_POWER_QORVO\HW00

WIFI CHAIN0 : 5Ghz



WIFI CHAIN0 : 2.4 & 5 Ghz



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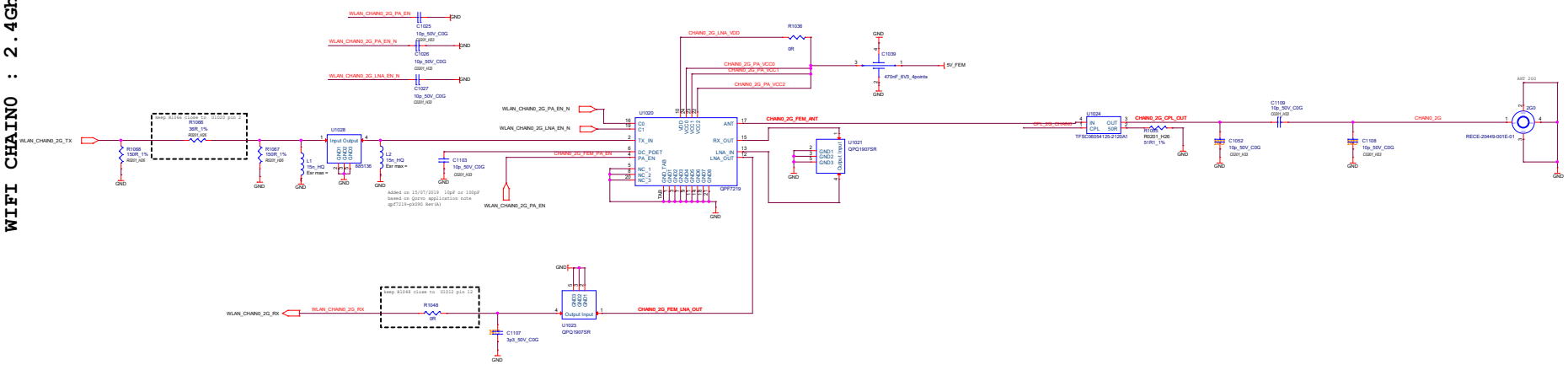

<Core Design>

DATE	BoM	AUTHOR	HISTORY
09Oct2019	A	RF TEAM	First Draft

Schematic status: ☒ Draft ☐ Reviewed ☐ Approved

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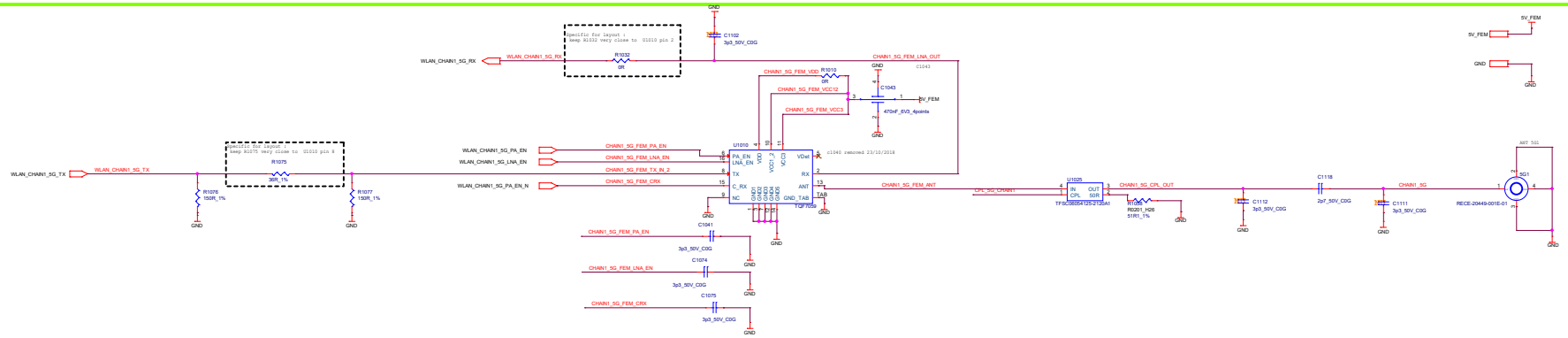
Author: RF TEAM

Size: A4 — Project Name_Gerber_Bold: MPP4_DB_WIFI_HW03

Date: Thursday, November 12, 2020 — Sheet 26 of 31

FEM_CHAIN1

WIFI CHAIN1 : 5Ghz



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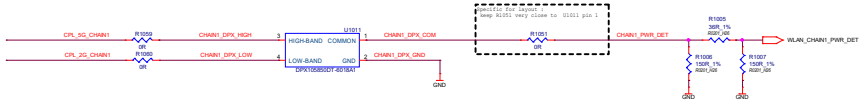

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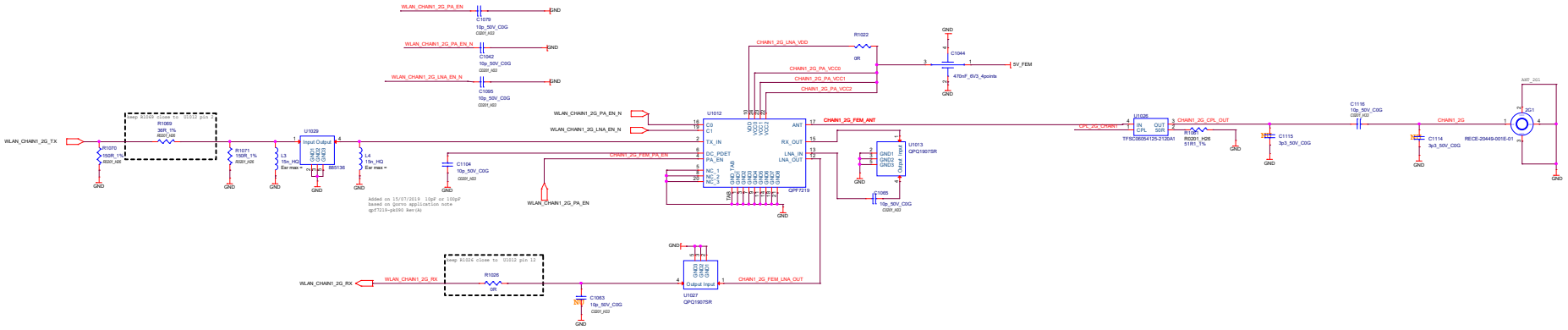

DATE	BoM	AUTHOR	HISTORY
09 Oct.2019	A	RF TEAM	First Draft

Schematic status: ☒ Draft ☐ Reviewed ☐ Approved

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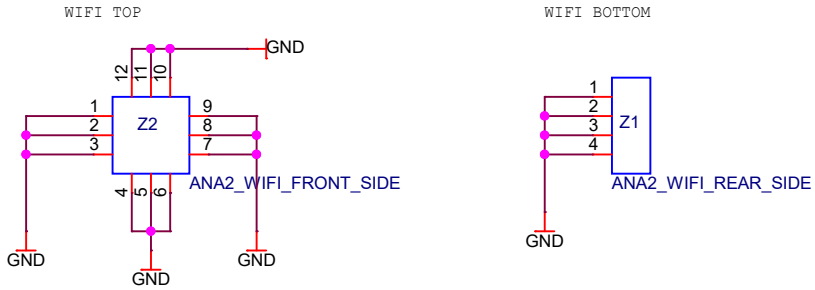
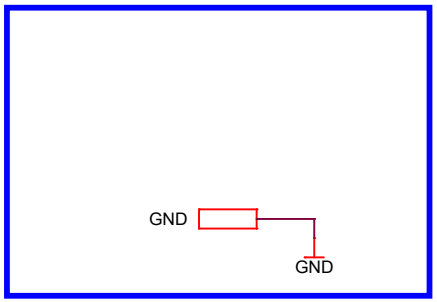
Author: RF TEAM

Size: A4 — Project Name_Gerber_Build: MPP4_DB_WIFI_HW03

Date: Thursday, November 12, 2020 — Sheet 29 of 31





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DATE	BoM	AUTHOR	HISTORY
10/2018	00_A		Creation

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Author

Project Name_Gerber_BoM

MPP4_DB_WIFI_HW03

Create date	Monday, August 08, 2016	Sheet 31 of 31	Size A4
Modify date	Wednesday, November 11, 2020		