

Moku 1.0 Operational Principles

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The Moku is a configurable piece of lab equipment. Its primary purpose is the input and analysis of analogue signals; and the synthesis and output of waveforms. To this end, it contains three circuit boards. The main board contains all processing and power systems, while ADC and DAC circuits have their own daughterboards.

Processing System

The device contains a Zynq ZC7020 combined FPGA and ARM Processor. The processor is clocked from its own internal PLL driven from a 33.3MHz external crystal. The FPGA is clocked as part of the primary clocking system described below.

Clocking System

An AD9517 distributor forms the core of the clocking system. It has an internal PLL at 2GHz, locked to either an on-board 10MHz high stability reference, or an off-board clock supplied through a BNC connector on the rear of the device.

The distributor generates four clock outputs. A 10Mhz output is generated to a back-panel connector, 125MHz for the FPGA fabric, 500MHz for the ADC card and 62.5MHz for the DAC card.

The ADC card buffers this clock signal, but doesn't change the frequency.

The DAC card buffers the clock signal, and each of the two DAC chips has an internal PLL that synthesises 1GHz from the 62.5MHz reference.

The FPGA has two internal PLLs, each of which synthesise 500MHz from the 125MHz reference to use as a data clock to each of the two daughterboards.

Power

The main board generates multiple power rails from the 12V input using monolithic integrated switchmode power supplies.

Peripherals

The main board includes an Ethernet PHY with its own 25MHz oscillator; a USB PHY with its own 24MHz oscillator and a Wifi chip with a 32.768khz oscillator.

Also present are LED drivers, IO expanders, an RTC and Apple Authentication Coprocessor.

Antenna System

The Wifi module operates in the 2.4GHz ISM band and is connected to a Taoglas FXP74 Black Diamond Antenna through a U.FL on-board connector. This part is a shorted-monopole style antenna manufactured on a flexible polymer base (FPCB 0.15t). It has a 4dBi peak gain measured on plastic by the manufacturer but has not been separately profiled for gain in this application.

RF System

The RF system is based on the Taiyo Yuden WYSBCVGXA package, incorporating Marvell Avastar 88W8787 chipset. This chipset supports 802.11b/g/n, Bluetooth and FM functionality; however only 802.11b is enabled in the device. This uses CCK modulation in channels 1 to 11 inclusive (2.412 – 2.462GHz) at a maximum output power at the package of 15dBm. It supports only the standard 802.11b bit rates of 11/5.5/2/1 Mbps.

Labelling

The compliance label will be laser engraved on to the base plate of the device as shown in the bundled graphic. Each logo will be approximately 1.5cm square.