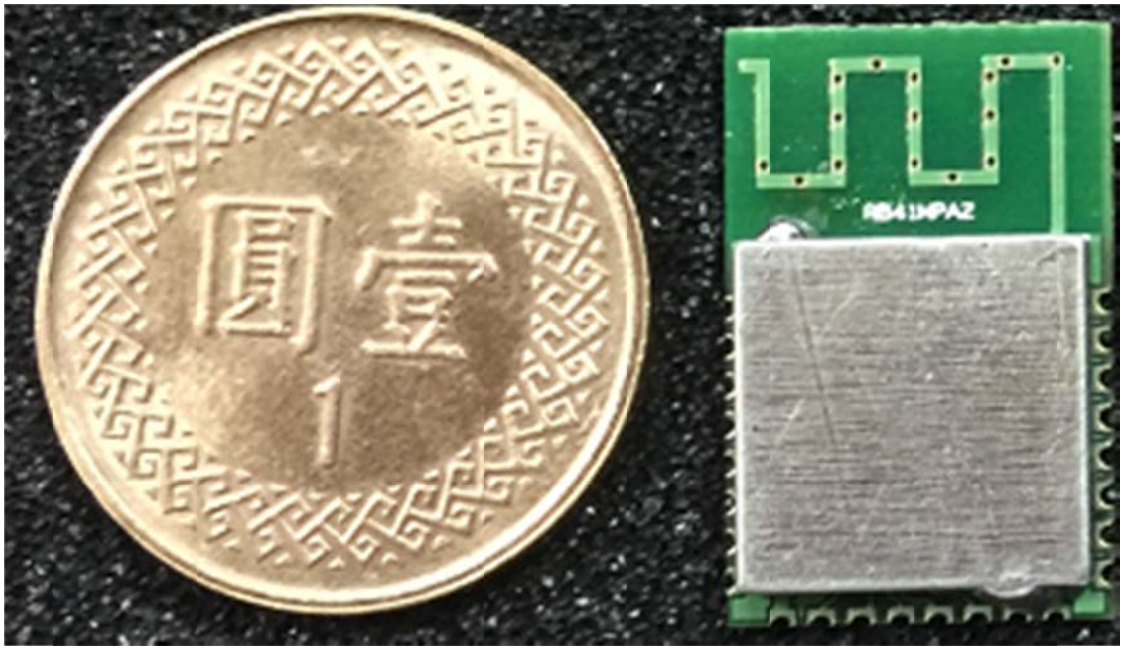
Approval Sheet

Model number: RB41MxA2



Ver 0.2

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1. Introduce

This Product implements Renesas –RL78G1D. The RL78/G1D is a microcomputer incorporating the RL78 CPU core and low power consumption RF transceiver supporting the Bluetooth ver.4.1 (Low Energy Single mode) specifications.

1.1 Features

Ultra-low power consumption technology

- MCU part Standby function HALT mode, STOP mode, SNOOZE mode
- RF part Standby function POWER_DOWN mode, RESET_RF mode, STANDBY_RF mode, IDLE_RF mode,
- DEEP_SLEEP mode, SLEEP_RF mode
- RF transmission (RF normal mode) : 4.3 mA (TYP.) (3.0 V/MCU part: STOP mode)
  (RF Low power mode) : 2.6 mA (TYP.) (3.0 V/MCU part: STOP mode)
- RF reception (RF normal mode) : 3.5 mA (TYP.) (3.0 V/MCU part: STOP mode)
  (RF Low power mode) : 3.3 mA (TYP.) (3.0 V/MCU part: STOP mode)
- RF sleep (POWER_DOWN mode) operation : 0.010mA (TYP.) (3.0 V/MCU part: STOP mode)

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.03125s: @ 32 MHz operation with high-speed on-chip oscillator) to ultra-low speed (30.5s: @ 32.768 kHz operation with subsystem clock)
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 12 to 20 KB

On-chip RF transceiver

- Bluetooth v4.1 Specification (Low Energy Single mode)
- 2.4 GHz ISM band, GFSK modulation, TDMA/TDD frequency hopping (including AES encryption circuit)
- Adaptivity, exclusively for use in operation as a slave device

Code flash memory

- Code flash memory: 128 to 256 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

Data flash memory

- Data flash memory: 8 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V DD = 1.8 to 3.6 V

2. Packaging

TBD

3. Specification

The detail specification is depended on real case. For more example, please contact with sales.

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}	V_{DD}	−0.5 to +6.5	V
	V_{DDRF1}	V_{DD_RF}	−0.5 to +4.0	V
	V_{DDRF2}	AV_{DD_RF}	−0.5 to +4.0	V
	V_{DDRF3}	DCLIN	−0.5 to +4.0	V
	V_{SSRF}	V_{SS_RF}, AV_{SS_RF}	−0.5 to +0.3	V
Input voltage	V_{I1}	P00, P01, P02, P03, P10, P11, P12, P14, P15, P16, P20, P21, P22, P23, P30, P40, P120, P121, P122, P123, P124, P137, P140, P147, RESET	−0.3 to V_{DD}+0.3 Note 1	V
	V_{I2}	P60, P61	−0.3 to +6.5	V
	V_{IRF1}	GPIO0, GPIO1, GPIO2, GPIO3	−0.3 to V_{DD_RF}+0.3 Note 2	V
	V_{IRF2}	ANT	−0.5 to +1.4	V
Output voltage	V_O	P00, P01, P02, P03, P10, P11, P12, P14, P15, P16, P20, P21, P22, P23, P30, P40, P60, P61, P120, P130, P140, P147	−0.3 to V_{DD}+0.3 Note 1	V
	V_{ORF}	GPIO0, GPIO1, GPIO2, GPIO3, DCLOUT	−0.3 to V_{DD_RF}+0.3 Note 2	V
Analog input voltage	V_{AI}	ANI0, ANI1, ANI2, ANI3, ANI16, ANI17, ANI18, ANI19	−0.3 to V_{DD}+0.3 and −0.3 to $V_{REF(+)}$+0.3 Notes 2, 4	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD}+0.3 Note 3	V
IC pin input voltage	V_{IIC}	IC0, IC1	−0.5 to +0.3	V

Notes 1. Must be 6.5 V or lower.

2. Must be 4.0 V or lower.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

4. Do not exceed $AV_{REF(+)}$ + 0.3 V in case of A/D conversion target pin.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	(This is applicable to all pins listed below.)	−40	mA
		Total of all pins −170mA	P00, P01, P02, P03, P40, P120, P130, P140	−70	mA
			P10, P11, P12, P13, P14, P15, P16, P30, P147	−100	mA
	I_{OH2}	Per pin	(This is applicable to all pins listed below.)	−0.5	mA
		Total of all pins	P20, P21, P22, P23	−2	mA
	I_{OHMRF}	Per pin	GPIO0, GPIO1, GPIO2, GPIO3	−17	mA
Output current, low	I_{OL1}	Per pin	(This is applicable to all pins listed below.)	40	mA
		Total of all pins 170mA	P00, P01, P02, P03, P40, P120, P130, P140	70	mA
			P10, P11, P12, P13, P14, P15, P16, P30, P60, P61, P147	100	mA
	I_{OL2}	Per pin	(This is applicable to all pins listed below.)	1	mA
		Total of all pins	P20, P21, P22, P23	5	mA
	I_{OLRF}	Per pin	GPIO0, GPIO1, GPIO2, GPIO3	17	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode		−40 to +85	°C
Storage temperature	Tstg			−65 to +150	°C

4.2 Operating Voltage

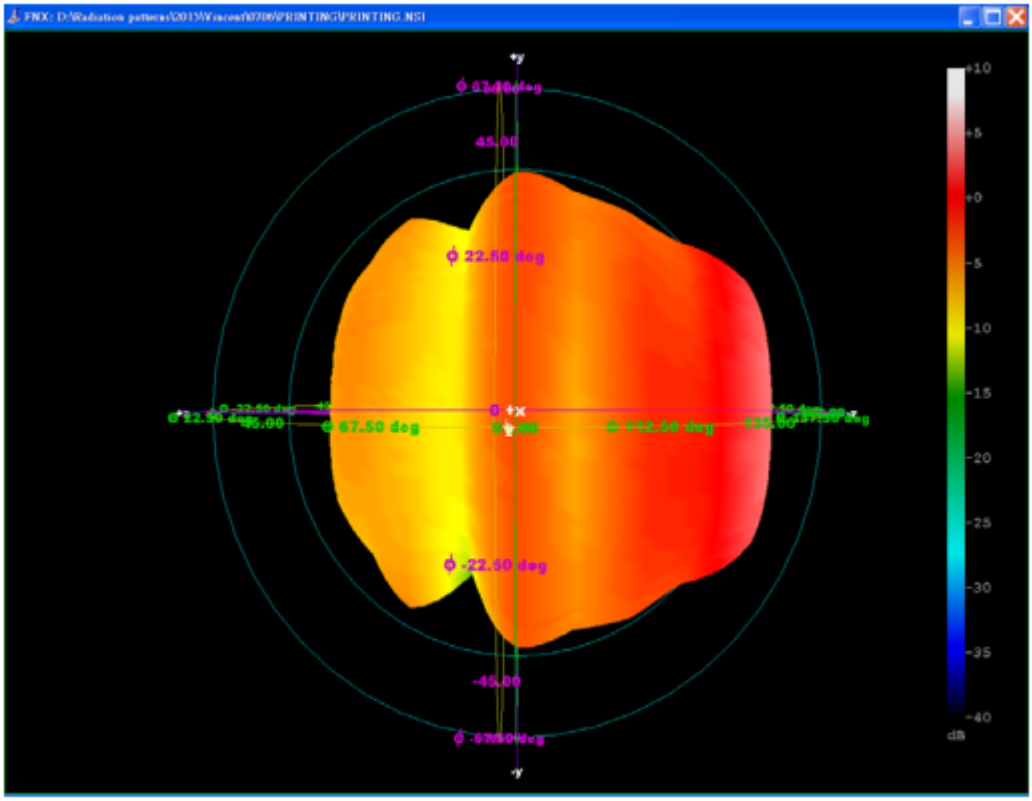
(T_A = −40 to +85°C, V_{DD} = V_{DD_RF} = AV_{DD_RF}, V_{SS} = V_{SS_RF} = AV_{SS_RF} = 0 V)

Clock generator		Flash operation mode	Operation voltage	CPU operation clocks (f_{CLK}) Note 1
Main system clock (f_{MAIN})	High-speed on-chip oscillator (f_{IH})	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 32 MHz
			2.4 V ≤ V_{DD} < 2.7 V	1 MHz to 16 MHz
		LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 8 MHz
		LV (low-voltage main) mode Note 2	1.6 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 4 MHz
	X1 clock oscillator (f_X)	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 20 MHz
		LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 8 MHz
		LV (low-voltage main) mode Note 2	1.6 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 4 MHz
	External main system clock (f_{EX})	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 20 MHz
			2.4 V ≤ V_{DD} < 2.7 V	1 MHz to 16 MHz
		LS (low-speed main) mode	1.8 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 8 MHz
		LV (low-voltage main) mode Note 2	1.6 V ≤ V_{DD} ≤ 3.6 V	1 MHz to 4 MHz
Subsystem clock (f_{SUB})	XT1 clock oscillator (f_{XT})	–	1.6 V ≤ V_{DD} ≤ 3.6 V	32.768 kHz
	External subsystem clock (f_{EXT})	–	1.6 V ≤ V_{DD} ≤ 3.6 V	32.768 kHz

Study case: iBeacon.

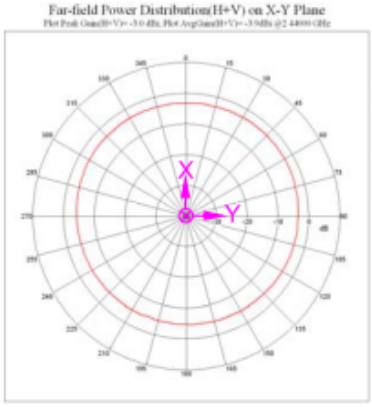
Status	Value
Transmit	5.xmA less than 10mA
Standby	5.xuA(sample 5.7uA) less than 10uA
Receive	3.5mA

4. Antenna



Case2 之輻射場型圖

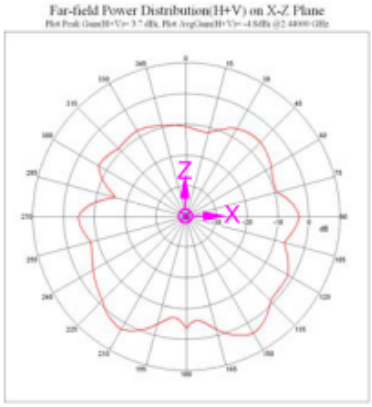
◆XY-plane



Unit : dBi

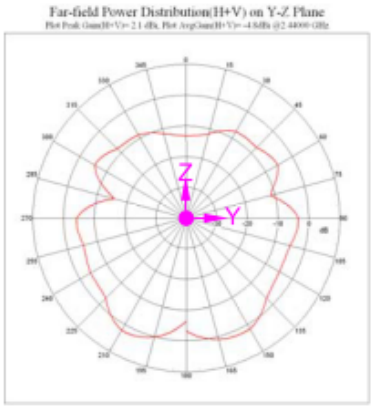
	Peak gain	Avg. gain
XY-plane	-3.0	-3.9

◆XZ-plane



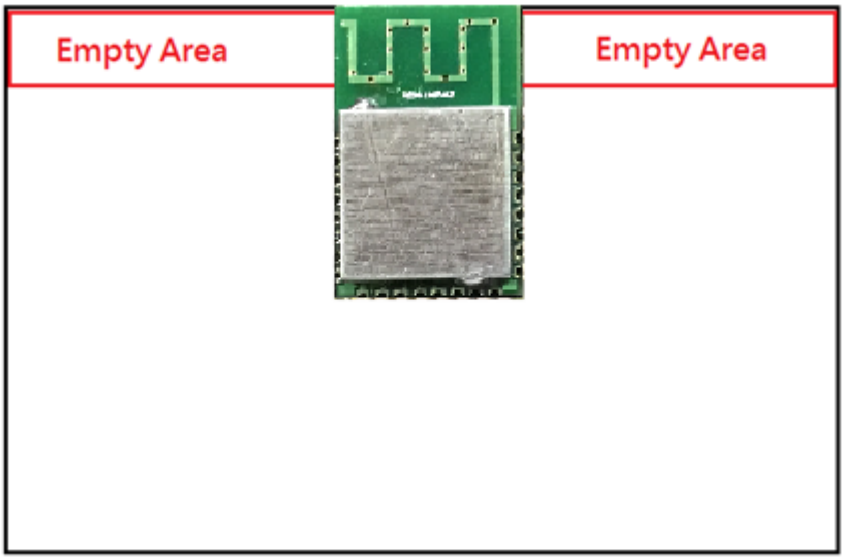
	Peak gain	Avg. gain
XZ-plane	3.7	-4.8

◆YZ-plane



	Peak gain	Avg. gain
YZ-plane	2.1	-4.8

5. Layout Guide



Please do not put any signal or power or ground at Empty Area.

6. Certification

Federal Communications Commission (FCC) Statement

15.21
You are cautioned that changes or modifications not expressly approved by the part responsible for compliance could void the user's authority to operate the equipment.

15.105(b)
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

-Reorient or relocate the receiving antenna.
-Increase the separation between the equipment and receiver.
-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-Consult the dealer or an experienced radio/TV technician for help.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1) this device may not cause harmful interference, and

2) this device must accept any interference received, including interference that may cause undesired operation of the device.

FCC RF Radiation Exposure Statement:
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure

compliance. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Note: The end product shall has the words “Contains Transmitter Module FCC ID: 2AF9GRB41