Technical Description:

The Equipment Under Test (EUT) is a 2.4GHz Bluetooth 3.0 transceiver (Camera Remote Shutter), which is operating at 2402MHz to 2480MHz (79 channels with 1MHz channel spacing). The EUT is powered by 3.0 VDC (1 X 3.0V “CR2025” batteries). The EUT has a power ON/OFF switch and a LED. When the EUT is switched ON, the blue LED will be on. The EUT will pair with the relating Smartphone via Bluetooth function and the blue LED will flash when they are successfully connected. Open the Camera application on the Smartphone, the photo will be taken when pressing the button on the EUT.

Antenna Type: Internal integral antenna
Antenna Gain: 0dBi
Nominal rated field strength: 94.2dBμV/m at 3m
Maximum allowed field strength of production tolerance: +3dB / - 3dB

The functions of main ICs are mentioned below.

1. Bluetooth module BK3231:
a. BK3231 acts as 2.4GHz radio core of Bluetooth module.
b. The 16MHz crystal (X2) and 32.768KHz crystal (X1) provides system clock for CC2540

2. Power Management portion:
a. J2, J3 act as power unit part.

BK3231 Bluetooth HID SoC Datasheet

Preliminary Specification

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1 General Description

The BK3231 chip is a highly integrated single-chip Bluetooth 2.1 HID device. It integrates the high-performance transceiver, rich features baseband processor, and Bluetooth HID profile. The FLASH program memory makes it suitable for customized application, and it is also possible for other Bluetooth aplication such as SPP controller.

2 Features

- Operation voltage from 2.0V to 3.6 V
- Bluetooth 3.0 compliant
- -86dBm sensitivity for 1 Mbps mode and 2 dBm transmit power
- HID v1.0, and other light profile by request
- 16 MHz crystal reference clock
- 56-pin QFN 7mmx7mm package for keyboard
- I2C, SPI and UART interface
- 10-bit Battery monitor ADC
- Three timers with PWM mode

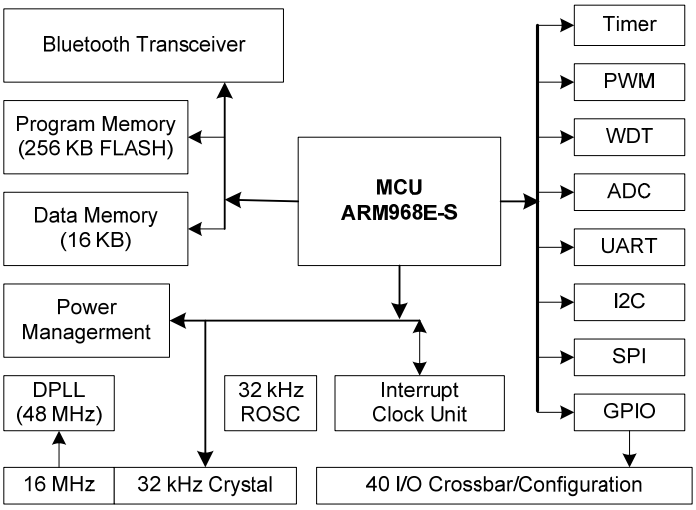


Figure 1 Block Diagram

3 Pin Information

The next diagram shows QFN56 format for the full functions usage.It can be used as keyboard TX part and total 35 GPIO available. Other package type such as QFN40 or even QFN32 is also available by request with less GPIO.

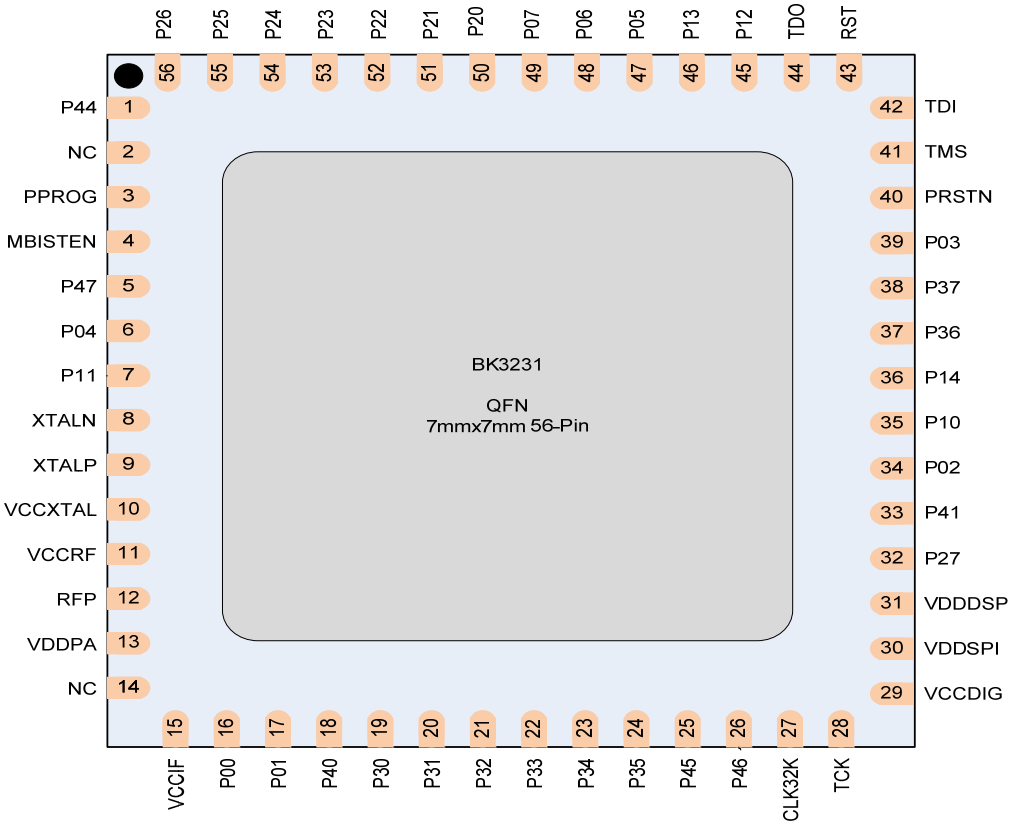


Figure 2 BK3231 QFN56 Pin Assignment

Table 1 BK3231 QFN56 Pin Description

PIN	Name	Pin Function	Description
1	P44	Digital I/O	General I/O
2	NC	NC	Not connected
3	PPROG	Digital I/O	FLASH programming selection
4	MBISTEN	Digital I/O	Test enable
5	P47	Digital I/O	General I/O
6	P04	Digital I/O	General I/O, or MOSI for SPI
7	P11	Digital I/O	General I/O, or input for external active low interrupt
8	XTALN	Analog output	Oscillator output
9	XTALP	Analog input	Oscillator input
10	VCCXTAL	Power supply	3 V supply
11	VCCRF	Power supply	3 V supply
12	RFP	RF port	RF input and output
13	VDDPA	Power output(LDO output)	1.5 V supply to PA
14	NC	NC	Not connected

15	VCCIF	Power supply	3 V supply
16	P00	Digital I/O	General I/O
17	P01	Digital I/O	General I/O
18	P40	Digital I/O	General I/O
19	P30	Digital I/O or analog input	General I/O
20	P31	Digital I/O or analog input	General I/O，or input of ADC1
21	P32	Digital I/O or analog input	General I/O，or input of ADC2
22	P33	Digital I/O or analog input	General I/O
23	P34	Digital I/O or analog input	General I/O，or input of ADC4
24	P35	Digital I/O or analog input	General I/O，or input of ADC5
25	P45	Digital I/O	General I/O
26	P46	Digital I/O	General I/O
27	CLK32K	Analog input	Clock 32 kHz input
28	TCK	Digital I/O	JTAG pin
29	VCCDIG	Power supply	3 V supply
30	VDDSPI	Analog output	Power output, connected with decoupling CAP
31	VDDDSP	Analog output	Power output, connected with decoupling CAP
32	P27	Digital I/O	General I/O，or enable for PWM1
33	P41	Digital I/O	General I/O
34	P02	Digital I/O	General I/O
35	P10	Digital I/O	General I/O，or input for external interrupt 0, active low
36	P14	Digital I/O	General I/O
37	P36	Digital I/O	General I/O, or input of ADC6
38	P37	Digital I/O	General I/O, or input of ADC7
39	P03	Digital I/O	General I/O
40	PRSTN	Digital I/O	Active low whole chip reset
41	TMS	Digital I/O	JTAG pin
42	TDI	Digital I/O	JTAG pin
43	RST	Digital I/O	JTAG reset
44	TDO	Digital I/O	JTAG pin
45	P12	Digital I/O	General I/O
46	P13	Digital I/O	General I/O
47	P05	Digital I/O	General I/O, or MISO for SPI
48	P06	Digital I/O	General I/O, or SCK for SPI
49	P07	Digital I/O	General I/O, or chip select for SPI
50	P20	Digital I/O	General I/O, or input for UART
51	P21	Digital I/O	General I/O, or output for UART
52	P22	Digital I/O	General I/O
53	P23	Digital I/O	General I/O，or clock for SMBUS (I2C)
54	P24	Digital I/O	General I/O，or data I/O for SMBUS (I2C)
55	P25	Digital I/O	General I/O

56	P26	Digital I/O	General I/O, or enable for PWM0

4 Memory Orgnization

Table 1 The Memory Orgnization

	Start Address	End Address	Total (Bytes)
Program Memory			
Flash	0x00000000	0x0003FFFF	256K
Data Memory			
SRAM	0x00400000	0x00403FFF	16K
AHB Peripheral			
(MFC)	0x00800000		
APB Peripheral			
Bluetooth Transceiver	0x00900000		
ICU	0x00920000		
UART	0x00930000		
IIC	0x00940000		
SPI	0x00950000		
GPIO	0x00960000		
WDT	0x00970000		
TIME	0x00980000		
ADC	0x009a0000		

By setting PPROG-pin to 1, the internal FLASH program memory can be written with four GPIO as a SPI slave. To access the FLASH memory with internal program, please refer to MFC section for detail.

5 Interrupt and Clock Unit

There are three main clock sources: 32.768 kHz XTAL, 16 MHz XTAL and 48 MHz DPLL. The MCU clock can be selected from one of them, while the peripherals use only one constantly.

Table 2 Clock Register Mapping - 0x00920000

Register Address	Name	Description
0x0[1:0]	hfsrc	0: 32.768 kHz 1: 16 MHz XTAL clock 2: 48 MHz DPLL 3: 0 MHz
0x1[7:1]	core_clk_divid	MCU clock divided ratio: 0~127
0x1[8]	core_clk_pwd	1: Power down MCU clock 0: Active MCU clock
0x3[8:0]	UART clk's Setting	Same definition as MCU clock setting by REG1[8:0] The UART main clock is 16 MHz
0x4[8:0]	I2C clk's Setting	Same definition as MCU clock setting by REG1[8:0] The I2C main clock is 16 MHz
0x5[8:0]	PWM clk's Setting	Same definition as MCU clock setting by REG1[8:0] The PWM main clock is 32.768 kHz
0x6[8:0]	WDT clk's Setting	Same definition as MCU clock setting by REG1[8:0] The PWM main clock is 32.768 kHz
0x8[8:0]	SPI clk's Setting	Same definition as MCU clock setting by REG1[8:0] The SPI main clock is 16 MHz
0x9[8:0]	ADC clk's Setting	Same definition as MCU clock setting by REG1[8:0] The ADC main clock is 16 MHz

The ARM968E-S supports two interrupt level. The FIRQ has higher priority than nIRQ. In the BK3231, all peripheral interrupts are nIRQ except the Bluetooth transceiver. All interrupt can be enabled, disabled, and cleared. There is two low power modes: MCU stop and deep sleep, and any interrupt can be configured to be a wake up source to let MCU exit low power mode.

Table 3 Interrupt Register Mapping - 0x00920000

Register Address	Name	Description
0xa[9:0]	int_enable[9:0]	Interrupt enable control bit [1]
0xa[10]	irq_enable	Enable ARM nIRQ
0xa[11]	fiq_enable	Enable ARM FIRQ
0xa[14:12]	ext_int0_cfg[2:0]	External interrupt 0 configuration bit[2]: Enable contro bit bit[1:0] 3，posedge trigger

		2，negedge trigger 1，high level trigger 0，low level trigger
0xa[17:15]	ext_int1_cfg[3:0]	External interrupt 1 configuration bit[2]: Enable contro bit bit[1:0] 3，posedge trigger 2，negedge trigger 1，high level trigger 0，low level trigger
0xa[27:18]	int_wakena[9:0]	Wakeup enable control bit [1]
0xb[9:0]	int_clear[9:0]	Interrupt clear control bit [1]
0xc[9:0]	int_status[9:0]	Interrupt status control bit [1]
0x10[31:0]	gpio_deep_waken[31:0]	Enable GPIO[31:0] as wake up source from deep sleep mode
0x11[7:0]	gpio_deep_waken[39:32]	Enable GPIO[39:32] as wake up source from deep sleep mode
0x11[31:16]	gpio_deep_sleep	Write16'h3231 to enable the IC enter deep sleep mode
0x13[0]	gpio_int_enable	Enable the GPIO interrupt [2]
0x13[1]	gpio_int_wakena	Enable GPIO be wake up source from MCU stop mode
0x13[2]	gpio_int_clear	Clear the GPIO interrupt
0x13[3]	gpio_int_status	GPIO interrupt status

Note 1:
The 10 interrupt source is defined as follows.

bit[0]	External Interrupt 0
bit[1]	External Interrupt 1
bit[2]	PWM timer 0
bit[3]	PWM timer 1
bit[4]	PWM timer 2
bit[5]	I2C Interrupt
bit[6]	UART Interrupt
bit[7]	Bluetooth transceiver interrupt
bit[8]	SPI Interrupt
bit[9]	ADC Interrupt

Note 2:
This single bit is combined logic of 40 GPIOs. To clear the single bit status, user should firstly clear the individual bit of the status of each GPIO interrupt in GPIO module

6 MFC

To avoid unintentional FLASH operation, serial strict steps must be executed before write or erase the FLASH. For example, if you want to write the FLASH, the next steps should be executed.

1. Set the right register to point to the space you want to operate firstly
2. Then write the configuration data and address
3. Write the right byte to Remove the protect condition
4. Write the right key number sequentially
5. Set the control bit to start the operation
6. Wait until the start bit change to zero
7. Set the control bit to protect the flash space for avoiding wrong operation

The read and erase process is similar to the write process

In the period of FLASH operation, The ARM will enter into IDLE state until the current operation finished.

You should erase the corresponding FLASH address firstly before program any data into it.

Table 4 Interrupt Register Mapping - 0x00800000

Addrees	Name	Description
0x00[15:0]	KEYWORD	Write “0x58A9” and then “0xA958” to enable FLASH operation; After once operation finished, it will be disabled automatically
0x01[0]	START	write 1 to start operate flash; it will be cleared by hardware after the operation finished
0x01[1]	ERROR	Error happened when =1; write 0 to clear it. Don’t write 1 to this bit.
0x01[4:2]	CONTROL	000: read 001: write 010: sector erase； 011: block erease 111: chip erase others : error happen; START will be cleared now
0x01[6:5]	SPACE control	00: main space 01: NVR space 10: RDN space 11: main space
0x02[15:0]	ADDR	Opearation address

0x03[31:0]	DATA	Data write into flash or the data read from flash
0x04[7:0]	DATA	FLASH W/E protect register 0 (must =0xa5)
0x05[7:0]	DATA	FLASH W/E protect register 2 (must =0xc3)
0x06	DATA	FLASH W/E protect register 3； Write any data into this address will disable W/E, and can't enable except RESET happened. Default enable after power on.
0x07	DATA	FLASH W/E protect register 4； Wite any data into this address will disable ARM directly write fucntion, and can' enable except RESET happened. Default enable after power on.

7 GPIO

There are eight groups total forty general purpose input and output ports. All the four port can be used for general I/O with selectable direction for each bit, or these lines can be used for specialized functions.

When the port is configured as general I/O, the detail function of them can be set by register as follows.

Table 5 GPIO0 Register Mapping - 0x00960000

0x0[0]	GPIO_Input	GPIO0 Input Bits
0x0[1]	GPIO_Output	GPIO0 Output Bits
0x0[2]	GPIO_Input_Ena	Input Enable, High Active
0x0[3]	GPIO_Output_Ena	Output Enable, Low Active
0x0[4]	GPIO_Pull_Mode	1: PullUp, 0: PullDown
0x0[5]	GPIO_Pull_Ena	GPIO0 Pull Up/Down Enable
0x0[6]	GPIO_Fun_Ena	GPIO0 2nd Function Enable
0x0[7]	Input_Monitor	View GPIO0's Inputs Value

GPIO1 to GPIO39 has the same definition but with address from 0x1 to 0x27.

Any GPIO can be interrupt source, and each GPIO has its own control bit as follows.

Table 6 GPIO Interrupt Control Register Mapping - 0x00960000

0x30	INT_EN[31:0]	GPIO[31:0] interrupt enable control bit (1)
0x31	INT_EN[39:32]	GPIO[39:32] interrupt enable control bit (1)
0x32	INT_LEV[31:0]	GPIO[31:0] interrupt trigger level 1: High; 0: Low

0x33	INT_LEV[39:32]	GPIO[39:32] interrupt trigger level 1: High; 0: Low
0x34	INT_STA[31:0]	GPIO[31:0] interrupt status
0x35	INT_STA[39:32]	GPIO[39:32] interrupt status

Most GPIO have special function mapping, and the GPIO will be used as the special functional pin when the contro bit (bit 6 GPIO_Fun_Ena) is enabled.

Table 7 GPIO Functinal Mapping

GPIO Pin Name	PPMODE=1	2nd function Mode	GPIO Mode	GPIO bit number
GPIO00	spi_prog_clk	bb_tx_bit Out	General I/O	GPIO00
GPIO01	spi_miso	bb_rx_bit Out	General I/O	GPIO01
GPIO02			General I/O	GPIO02
GPIO03			General I/O	GPIO03
GPIO04		SPI MOSI	General I/O	GPIO04
GPIO05		SPI MISO	General I/O	GPIO05
GPIO06		SPI SCK	General I/O	GPIO06
GPIO07		SPI CS	General I/O	GPIO07
GPIO08	spi_mosi	External Interupt 0	General I/O	GPIO10
GPIO09	spi_cs	External Interrupt 1	General I/O	GPIO11
GPIO10			General I/O	GPIO12
GPIO11			General I/O	GPIO13
GPIO12			General I/O	GPIO14
GPIO13			General I/O	GPIO15
GPIO14		UART CTS(Out)	General I/O	GPIO16
GPIO15		UART RTS(In)	General I/O	GPIO17
GPIO16		UART_RX	General I/O	GPIO20
GPIO17		UART_TX	General I/O	GPIO21
GPIO18			General I/O	GPIO22
GPIO19		I2C SCLK	General I/O	GPIO23
GPIO20		I2C SDA	General I/O	GPIO24
GPIO21			General I/O	GPIO25
GPIO22		PWM0 Output	General I/O	GPIO26
GPIO23		PWM1 Output	General I/O	GPIO27
GPIO24		ADC0	General I/O	GPIO30
GPIO25		ADC1	General I/O	GPIO31
GPIO26		ADC2	General I/O	GPIO32
GPIO27		ADC3	General I/O	GPIO33
GPIO28		ADC4	General I/O	GPIO34

GPIO29		ADC5	General I/O	GPIO35
GPIO30		ADC6	General I/O	GPIO36
GPIO31		ADC7	General I/O	GPIO37
GPIO32			General I/O	GPIO40
GPIO33			General I/O	GPIO41
GPIO34			General I/O	GPIO42
GPIO35			General I/O	GPIO43
GPIO36			General I/O	GPIO44
GPIO37			General I/O	GPIO45
GPIO38			General I/O	GPIO46
GPIO39			General I/O	GPIO47

8 ADC

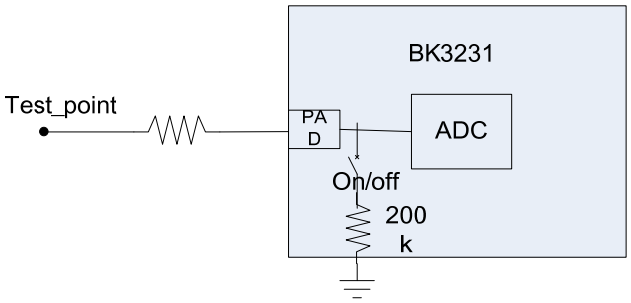
A 10bits SAR ADC is integrated in the BK3231. Total 8 channels can be selected used for ADC transfer. The ADC supports continue mode and single transfer mode, and the sample rate can be 1 kHz to 32 kHz. In single transfer mode, it will generate interrupt every time after transform.

The ADC have four work mode, they are sleep mode, single mode, software mode and continue mode.

- Sleep mode (mode==00): ADC is power down now
- Single mode (mode==01): The system will enter sleep mode when transfer is done and waiting MCU to read the result. You should write mode=1 again for another transfer.
- Controlled by software (mode==10): In this mode, interrupt will be triggered after transfer and wait MCU to read. The interrupt will be cleared after MCU read, and then the transfer will start again.
- Continue mode (mode==11):The ADC will work at the sample rate set by register. The sample rate can be calculated by the next formula:
  - F_sample = input ADC clock/(2^(ADC_CLK_RATE+2) / 36(or 18))
  - The highest sample rate is 32k

The local interrupt flag of ADC need not be cleared by software; it will be set after tranform and be cleared after the result has been read out. But the ADC INT stored ICU should be cleared after the ADC INT service finished.

The range of input voltage is from 0v to 1.5V. If the input voltage more than 1.5V, a resistor can be added to decrease the input voltage like the next diagram.



Note: There are eight GPIO can be ADC input. When used as this:
Voltage=data[9:0]/448; The saturate voltage is 1.5 volt.

Table 8 ADC Register Mapping – 0x009A0000

Address	Name	Description
0x0[1:0]	ADC_MODE	ADC operation mode 00: Sleep mode 01: Single mode10: Software mode 11: Continuous mode
0x0[2]	ADC_EN	Enable ADC
0x0[5:3]	ADC_CHNL	Channel selection
0x0[6]	FIFO_EMPTY	ADC FIFO empty flag The ADC conversion resultis stored at a FIFO with 4 depths
0x0[7]	ADC_BUSY	ADC busy flag
0x0[9:8]	ADC_SAMPLE_RATE	Sample rate setting 2'b00: adc_clk/36 2'b01: adc_clk/18 2'b10: reserved 2'b11: Reserved
0x0[10]	ADC_CLK_WAIT	For ADC mode 1 and mode 2, it will wait 4 (0) or 8(1) ADC_CLK cycle to start coversion after actie ADC clock
0x0[18:16]	ADC_CLK_RATE	ADC clock divided ratio 000: 4 001: 8 010:16 011: 32 100: 64 101: 128 110: 256 111: 512
0x1[9:0]	ADC_DATA	ADC conversion result

9 UART

The UART interface has 128 bytes FIFO for both TX and RX. It will generate interrupt request when there is risk or event of FIFO underflow or overflow. For the RX, it will generate interrupt if found parity bit check error or stop bit check error.

When the UART RX line goes from idle state ('HIGH') to active state ('LOW') for a set UART clock cycle, it will generate wake up interrupt to activate MCU clock.

Table 9 UART Register Mapping – 0x00930000

0x0[0]	UART_TX_ENABLE	UART TX enable (1) or disable (0)
0x0[1]	UART_RX_ENABLE	UART RX enable (1) or disable (0)
0x0[2]	UART_IRDA	0：UART frame structure 1：IRDA frame structure
0x0[4:3]	UART_LEN[1:0]	UART data bit width 00：5 bit 01：6 bit 10：7 bit 11：8 bit
0x0[5]	UART_PAR_EN	Has(1) or not(0)the parity check bit
0x0[6]	UART_PAR_MODE	Odd(0) or even(1) parity check
0x0[7]	UART_STOP_LEN	STOP bit length 0：1 bit 1：2 bits
0x0[20:8]	UART_CLK_DIV[12:0]	UART band rate setting Baud rate=UART_CLK/(UART_CLK_DIV+1) UART_CLK_DIV should be greater than 4
0x0[21]	UART_TX_FIFO_EN	Clear TX FIFO (1)
0x0[22]	UART_RX_FIFO_EN	Clear RX FIFO (1)
0x1[7:0]	TX_FIFO_THRESHOLD [7:0]	When the bytes in TX FIFO is less than this threshold, it will give need write interrupt

0x1[15:8]	RX_FIFO_THRESHOLD[7:0]	When the bytes in RX FIFO is greater than this threshold, it will give need read interrupt
0x2[7:0]	TX_FIFO_COUNT[FIFO_WD-1:0]	Number of bytes in the TX FIFO
0x2[15:8]	RX_FIFO_COUNT[FIFO_WD-1:0]	Number of bytes in the RX FIFO
0x3[7:0]	UART_DOUT	UART TX data
0x3[15:8]	UART_DIN	UART RX data
0x4[0]	UART_TX_FIFO_NEED_WRITE_MASK	Enable TX FIFO need write interrupt
0x4[1]	UART_RX_FIFO_NEED_READ_MASK	Enable RX FIFO need read interrupt
0x4[2]	UART_RX_OV_MASK	Enable RX overflow interrupt
0x4[3]	UART_RX_PAR_ERR_MASK	Enable RX parity check error interrupt
0x4[4]	UART_RX_STOP_ERR_MASK	Enable RX stop bit check error interrupt
0x4[5]	TX_STOP_END_MASK	Enable TX finished interrupt
0x4[6]	UART_RXD_WAKE_PULSE_MASK	Enable RX wake up pulse detected interrupt
0x5[0]	UART_TX_FIFO_NEED_WRITE_WAKEUP	TX FIFO need write interrupt; Will be cleared after interrupt condition disappeared
0x5[1]	UART_RX_FIFO_NEED_READ_WAKEUP	RX FIFO need read interrupt; Will be cleard after interrupt condition disappeared
0x5[2]	UART_RX_OV	RX overflow bit error interrupt status Write 1 to clear
0x5[3]	UART_RX_PAR_ERR	RX parity bit error interrupt status Write 1 to clear
0x5[4]	UART_RX_STOP_ERR	RX stop bit error interrupt status Write 1 to clear
0x5[5]	TX_STOP_END_INT	UART TX finished interrupt status Write 1 to clear
0x5[6]	UART_RXD_WAKE_PULSE	UART wake up pulse interrupt status Write 1 to clear
0x6[6:0]	FLOW_CTL_LOW_CNT[6:0]	UART CTS and RTS flow control rx_fifo low counter threshhold: when rx_fifo_counter < flow_ctl_low_cnt: CTS is set;meaning that UART is ready to receive.

0x6[14:8]	FLOW_CTL_HIGH_CNT[6:0]	UART CTS and RTS flow control rx_fifo high counter threshhold: when rx_fifo_counter > flow_ctl_high_cnt: CTS is clear;meaning that UART is not ready to receive.
0x6[16]	FLOW_CTL_EN	UART CTS and RTS flow control enable
0x7[9:0]	UART_RXD_WAKE_CNT	UART RX waken up pad time threshold and low pulse RX threshold
0x7[19:10]	UART_TXD_WAIT_CNT	UART TX waiting time after sending wake up signal
0x7[20]	UART_RXD_WAKE_EN	UART RX waken up pad enable (1)
0x7[21]	UART_TXD_WAKE_EN	UART low pulse tx enable (1)

10 I2C-SMBus

The I2C I/O interface is a two-wire, bi-directional serial bus. The I2C is compliant with the System Management Bus Specification, version 1.1, and compatible with the I C serial bus. Reads and writes to the interface by the system controller are byte oriented with the I2C interface autonomously controlling the serial transfer of the data.

Data can be transferred at up to 1/10th of the system clock as a master or slave (this can be faster than allowed by the I2C specification, depending on the system clock used). A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The I2C interface may operate as a master and/or slave, and may function on a bus with multiple masters. The I2C provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and START/STOP control and generation.

It is assumed the reader is familiar with the I2C-Bus Specification -- Version 2.0 and system Management Bus Specification -- Version 1.1.

The bi-directional SCL (serial clock) and SDA (serial data) lines must be connected to a positive power supply voltage through a pull-up resistor or similar circuit. Every device connected to the bus must have an open-drain or open-collector output for both the SCL and SDA lines, so that both are pulled high (recessive state) when the bus is free.

Table 10 I2C Register Mapping – 0x00940000

0x0[31]	ENSMB	SMBus Enable

0x0[30]	INH	SMBUS slave mode enable (0)
0x0[29]	SMBFTE	Enable bus idle detection (1) Should be enabled for master mode
0x0[28]	SMBTOE	SCL low time out detection enable (1)
0x0[27:26]	SMBCS	SMBus clock source selection 00: Timer 0 overflow 01: Timer 1 overflow 10：Timer 2 overflow 11：Internal clock (Divided ratio= FREQ_DIV）
0x0[25:16]	SLV_ADDR	SMBUS slave address
0x0[15:6]	FREQ_DIV	SMBUS main clock divided ratio
0x0[5:3]	SCL_CR	SCL active low time out threshold, is power(2, SCL_CR)
0x0[2:0]	IDLE_CR	SMBUS idle detection threshold, is power(2, IDLE_CR)
0x1[31:16]	Reserved	
0x1[15]	BUSY	SMBus busy (1)
0x1[14]	MASTER	MASTER mode (1) or slave mode (0)
0x1[13]	TXMODE	SMBus TX status (1) or RX status (0)
0x1[12]	ACKRQ	SMBus ACK (1) or not (0) at receive mode
0x1[11]	ADDR_MATCH	Address match ok (1) or not (0)
0x1[10]	STA	SMBus start condition enable (1)
0x1[9]	STO	Write: SMBus stop condition send enable (1) Read: SMbus stop condition detected (1)
0x1[8]	ACK	Write: SMBus ACK send enable (1) Read: SMBus ACK received (1)
0x1[7:6]	INT_MODE	Interrupt mode For Sender： 00,01,10,11: Data in TX FIFO is less than 1/4/8/12 byte For Recevier: 00,01,10,11：Data in RX FIFO is greater than 12/8/4/1
0x1[5]	TXFIFO_FULL	TX FIFO Full flag
0x1[4]	RXFIFO_EMPTY	RX FIFO empty flag
0x1[3]	ARBLOST	Multi-master competition failed (1)
0x1[2]	Reserved	
0x1[1]	SCL_TMOT	SCL low time out detected (1)

0x1[0]	SI	SMBus interrupt flag
0x2[31:8]	Reserved	
0x2[7:0]	SMB_DAT	SMBUS TX data (Write) or RX data (Read)

11 SPI

The Enhanced Serial Peripheral Interface (SPI) provides access to a flexible, full-duplex synchronous serial bus. SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select SPI in slave mode, or to disable Master Mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a chip-select output in master mode, or disabled for 3-wire operation. Additional general purpose port I/O pins can be used to select multiple slave.

There are four pins for SPI interface. The master-out, slave-in (MOSI) signal is an output from a master device and an input to slave devices. It is used to serially transfer data from the master to the slave. This signal is an output when SPI is operating as a master and an input when SPI is operating as a slave. Data is transferred most-significant bit first. When configured as a master, MOSI is driven by the MSB of the shift register in both 3- and 4-wire mode.

The master-in, slave-out (MISO) signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. This signal is an input when SPI is operating as a master and an output when SPI is operating as a slave. Data is transferred most-significant bit first. The MISO pin is placed in a high-impedance state when the SPI module is disabled and when the SPI operates in 4-wire mode as a slave that is not selected. When acting as a slave in 3-wire mode, MISO is always driven by the MSB of the shift register.

In slave mode, the data on MOSI are sampled at the middle of period of every bit. In master mode, the data on MISO are sampled at the last clock period to acquire the maximal setup time.

Table 11 SPI Register Mapping – 0x00950000

Address	Name	Description
0x0[23]	SPIEN	Enable SPI (1)
0x0[22]	MSTEN	Master mode (1) or slave mode(0)
0x0[21]	CKPHA	SPI clock phase 0：Sample data at first edge of SCK 1： Sample data at second edge of SCK

0x0[20]	CKPOL	SPI clock polarity SCK is high (1) or low (0) at idle stat 0
0x0[18]	BIT_WDTH	Bit width 0：8bit 1：16bit
0x0[17:16]	NSSMD	Slave mode 00：3-wires mode 01：4-wires mode 1x：4-wires mode single master
0x0[15:8]	SPI_CKR	SPI clock divided ratio
0x0[7]	RXINT_EN	RX interrupt enable
0x0[6]	TXINT_EN	TX interrupt enable
0x0[5]	RXOVR_EN	RX overflow interrupt enable
0x0[4]	TXOVR_EN	TX overflow interrupt enable
0x0[3]	RXFIFO_CLR	Clear RX FIFO
0x0[2]	TXFIFO_CLR	Clear TX FIFO
0x0[1]	RXINT_MODE	RX interrupt setting when number of data in the RX FIFO is greater than 0 (0) or 8 (1)
0x0[0]	TXINT_MODE	TX interrupt setting when number of data in the TX FIFO is 0 (0) or less than 8 (1)
0x1[15]	SPIBUSY	SPI busy flag
0x1[14]	SLVSEL	Slave seleted flag when NSS is 0
0x1[12]	RXOVR	RX overflow flag
0x1[11]	TXOVR	TX overflow flag
0x1[10]	MODF	Master collision detected flag
0x1[9]	RXINT	RX interrupt flag
0x1[8]	TXINT	TX interrupt flag
0x1[3]	RXFIFO_FULL	RX FIFO full flag
0x1[2]	RXFIFO_EMPTY	RX FIFO empty flag
0x1[1]	TXFIFO_FULL	TX FIFO full flag
0x1[0]	TXFIFO_EMPTY	TX FIFO empty flag
0x2[15:0]	SPI_DAT	SPI data entry Write to TX FIFO or read from RX FIFO

12 PWM Timer

There are three timers, two of which is 16 bit and can be works as PWM waveform generator, while the other one is 20bit timer. The PWM waveform can be output to GPIO to drive external device such as LED.

Table 12 PWM Timer Register Mapping – 0x00980000

Address	Namae	Description
0x0[15:0]	PT0_CntMid[15:0]	PWM 0 Active high duration
0x0[31:16]	PT0_CounTo[15:0]	PWM 0 or counter period
0x1[15:0]	PT1_CntMid[15:0]	PWM 1 Active high duration
0x1[31:16]	PT1_CounTo[15:0]	PWM 1 or counter period
0x2[0]	PT0_Mode	0: Timer mode 1: PWM Mode
0x2[1]	PT1_Mode	0: Timer mode 1: PWM Mode
0x2[3:2]		Reserved
0x2[4]	PT0_Enable	PWM timer 0 enable (1)
0x2[5]	PT1_Enable	PWM timer 1 enable(1)
0x2[7:6]		Reserved
0x2[11:8]	PT_Divid[3:0]	PWM timer pre-divide ratio
0x2[12]	PT0_Int_flag	PWM timer 0 interrupt flag, write 1 to clear
0x2[13]	PT1_Int_flag	PWM timer 1 interrupt flag, write 1 to clear
0x3[19:0]	PT2_Counto[19:0]	Timer 2 period
0x3[20]	PT2_Enable	Timer 2 enable (1)
0x3[21]	PT2_Int_flag	Timer 2 interrupt flag,write 1 to clear

13 Watch dog

The watch dog is used to reset the whole chip when the firmware runs out of order.

Table 13 Watch Dog Register Mapping – 0x00970000

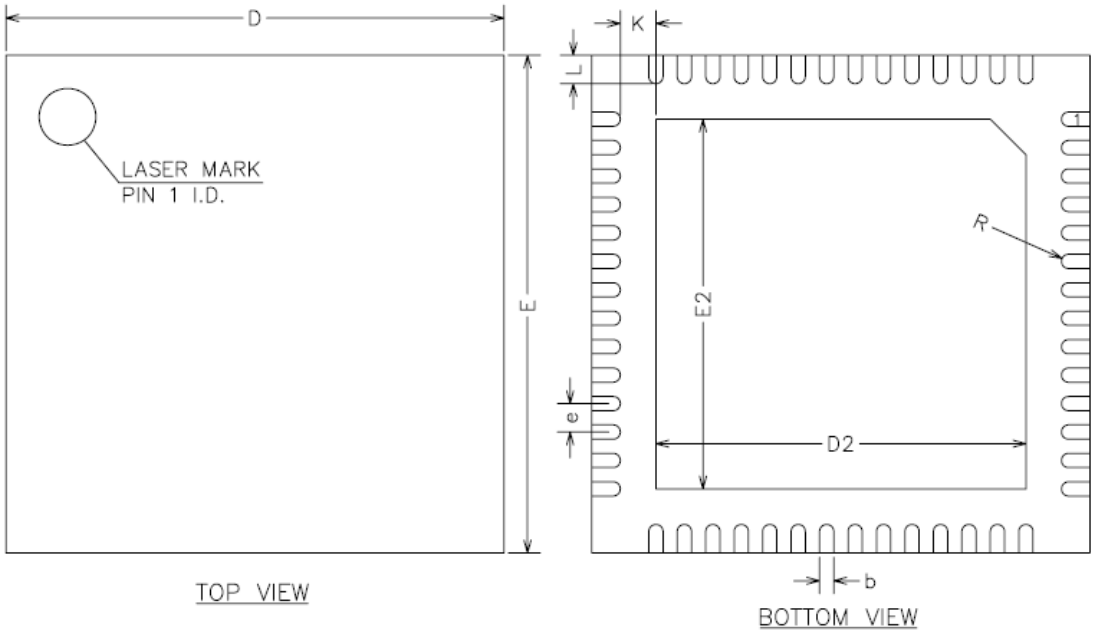
Address	Namae	Description
0x0[23:16]	WDKEY[7:0]	Watch dog key To clear watch dog counter, please write 0x5A, and then write 0xA5
0x0[15:0]	WD_PERIOD[15:0]	Watch dog timer period 1: ~0.6 ms Maximum: ~38.8 second

14 Electrical Specifications

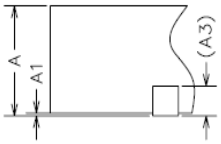
Table 2 RF Characteristics

Name	Parameter (Condition)	Min	Typical	Max	Unit	Comment
	Operating Condition					
VCC	Voltage	2.0	3.0	3.6	V	
TEMP	Temperature	-10	+27	+55	ºC	
	Digital input Pin					
VIH	High level	VCC-0.3		VCC+0.3	V	
VIL	Low level	VSS		VSS+0.3	V	
	Digital output Pin					
VOH	High level (IOH=-0.25mA)	VCC- 0.3		VCC	V	
VOL	Low level(IOL=0.25mA)	VSS		VSS+0.3	V	
	Normal condition					
IVDD	Deep sleep		2		uA	
IVDD	Sleep mode 1 (MCU stopped)		10		uA	
IVDD	Sleep mode 2 (MCU 32 kHz)		100		uA	
IVDD	Active RX		30		mA	
IVDD	Active TX @ 2 dBm output power		22		mA	
	Normal RF condition					
FOP	Operating frequency	2400		2480	MHz	
FXTAL	Crystal frequency		16		MHz	
RFSK	Air data rate		1		Mbps	
	Transmitter					
PRF	Output power	-40	0	5	dBm	
PBW	Modulation 20 dB bandwidth		1		MHz	
PRF1	Out of band emission 2 MHz	-20			dBc	
PRF2	Out of band emission 3 MHz	-40			dBc	
IVDD	Current at -40dBm output power		NA		mA	
IVDD	Current at -30dBm output power		NA		mA	
IVDD	Current at -25dBm output power		NA		mA	
IVDD	Current at -10dBm output power		NA		mA	
IVDD	Current at -5dBm output power		NA		mA	
IVDD	Current at 0dBm output power		NA		mA	
IVDD	Current at 2dBm output power		22		mA	
	Receiver					
Max Input	1 E-3 BER	0			dBm	
RXSENS	1 E-3 BER sensitivity		-86		dBm	
IIP3	IIP3, Pin=-63 dBm; Punwant=-39 dBm; f0=2f1-f2, f2-f1=3 MHz or 4 MHz or 5 MHz		-18		dBm	
C/ICO	Co-channel C/I			11	dB	
C/I1ST	ACS C/I 1MHz			0	dB	
C/I2ND	ACS C/I 2MHz			-30	dB	
C/I3RD	ACS C/I 3MHz			-40	dB	
C/I1STI	ACS C/I Image channel			-9	dB	
C/I2NDI	ACS C/I 1 MHz adjacnet to image channel			-20	dB	

15 Package Information



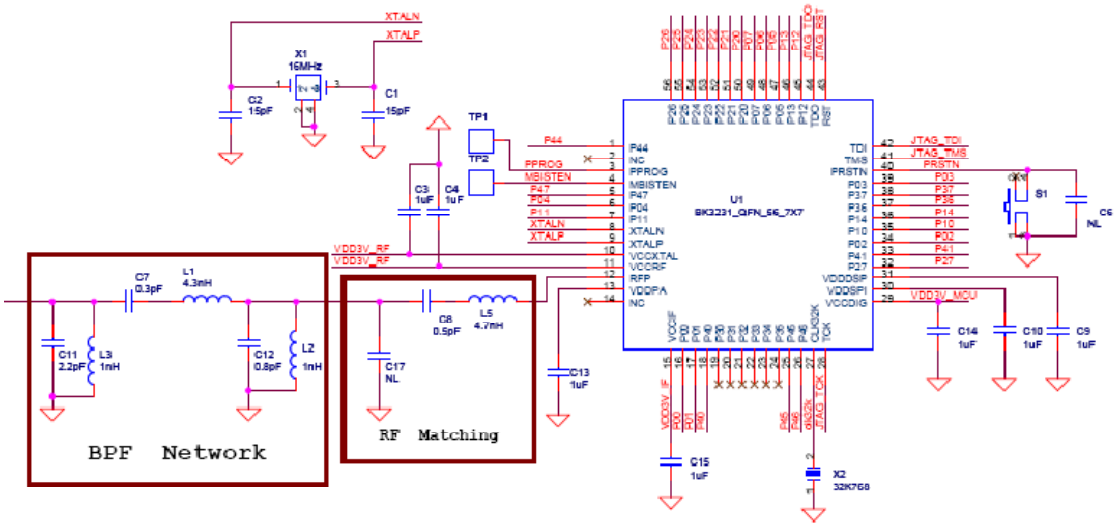
SIDE VIEW



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.05	5.20	5.35
E2	5.05	5.20	5.35
e	0.30	0.40	0.50
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–

16 Application Schematic



17 Order Information

Part number	Package	Packing	Minimum Order Quantity
BK3231QB	QFN7x7-56Pin	Tape Reel	3000