register as 2-bit extended data of the conversion accuracy bits: when the conversion count is set to 16 times, the value added by the A/D conversion result is retained in the ADBUFn register as 4-bit extended data of the conversion accuracy bits.
Even if A/D-converted value addition mode is selected, the extended A/D-converted value is stored in the ADBUFn register according to the settings of the A/D data register format select bits.

44.2.37 A/D Data Storage Buffer Enable Register (ADBUFEN)

Address(es): S12AD.ADBUFEN 0008 90D0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BUFEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	BUFEN	Data Storage Buffer Enable	0: The data storage buffer is not used. 1: The data storage buffer is used.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ADBUFEN register is used to enable the data storage buffer.

BUFEN Bit (Data Storage Buffer Enable)

This bit enables the use of the data storage buffer when using the compare function.
When BUFEN = 1, A/D conversion result (addition result) other than self-diagnosis result is stored in ADBUFn.
Disable the data storage operation (BUFEN = 0) before reading ADBUFn and ADBUFPTR.
Do not use the data storage buffer for data duplexing, continuous scan, or group scan.

44.2.38 A/D Data Storage Buffer Pointer Register (ADBUFPTR)

Address(es): S12AD.ADBUFPTR 0008 90D2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PTROVF	BUFPTR[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	BUFPTR[3:0]	Data Storage Buffer Pointer	These bits indicate the number of data storage buffer to which the next A/D conversion data is transferred.	R/W
b4	PTROVF	Pointer Overflow Flag	0: The data storage buffer pointer has not overflowed. 1: The data storage buffer pointer has overflowed.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ADBUFPTR register is used for the data storage buffer pointer.

BUFPTR[3:0] Bits (Data Storage Buffer Pointer)

These read-only bits indicate the number of data storage buffer to which the next A/D conversion data is transferred. When data has been transferred to data storage buffer 15, the pointer value becomes 0000b and the PTROVF flag is set to 1. When the next data has been transferred, the data in data storage buffer 0 is overwritten.
Writing 00h to this register clears the value of these bits. Writing a value other than 00h is disabled.

PTROVF Flag (Pointer Overflow Flag)

This read-only flag indicates whether the data storage buffer pointer has overflowed. This flag is set to 1 when the pointer value becomes 0000b (overflow).
Writing 00h to this register clears this flag value. Writing a value other than 00h is disabled.

44.3 Operation

44.3.1 Scanning Operation

In scanning, A/D conversion is performed sequentially on the analog inputs of the specified channels.
A scan conversion is performed in three operating modes: single scan mode, continuous scan mode, and group scan mode. Also, conversion modes are divided into high-speed conversion mode and normal conversion mode. In single scan mode, one or more specified channels are scanned once. In continuous scan mode, one or more specified channels are scanned repeatedly until the ADCSR.ADST bit is cleared to 0 from 1 by software. In group scan mode, the selected channels of group A and the selected channels of group B are scanned once after starting to be scanned according to the respective synchronous trigger.
In single scan mode and continuous scan mode, A/D conversion is performed for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n. In group scan mode, A/D conversion is performed for ANn channels of group A and group B selected by the ADANSA0, ADANSA1, ADANSB0, and ADANSB1 registers, respectively, starting from the channel with the smallest number n.
When self-diagnosis is selected, it is executed once at the beginning of each scan and one of the three voltages internally generated in the 12-bit A/D converter is converted.
When performing A/D conversion of the temperature sensor output or internal reference voltage, execute scanning individually.
Double trigger mode is to be used with single scan mode or group scan mode. With double trigger mode being enabled, A/D conversion data of a channel selected by the ADCSR.DBLANS[4:0] bits is duplicated only if the conversion is started by the synchronous trigger selected by the ADSTRGR.TRSA[5:0] bits.

44.3.2 Single Scan Mode

44.3.2.1 Basic Operation

In basic operation of single scan mode, A/D conversion is performed once on the analog input of the specified channels as below.

(1) When the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, synchronous trigger, or asynchronous trigger input, A/D conversion is performed for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(2) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(3) When A/D conversion of all the selected channels is completed, an S12ADI0 interrupt request is generated if the ADCSR.ADIE bit is 1 (S12ADI0 interrupt upon scanning completion enabled).
(4) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a wait state.

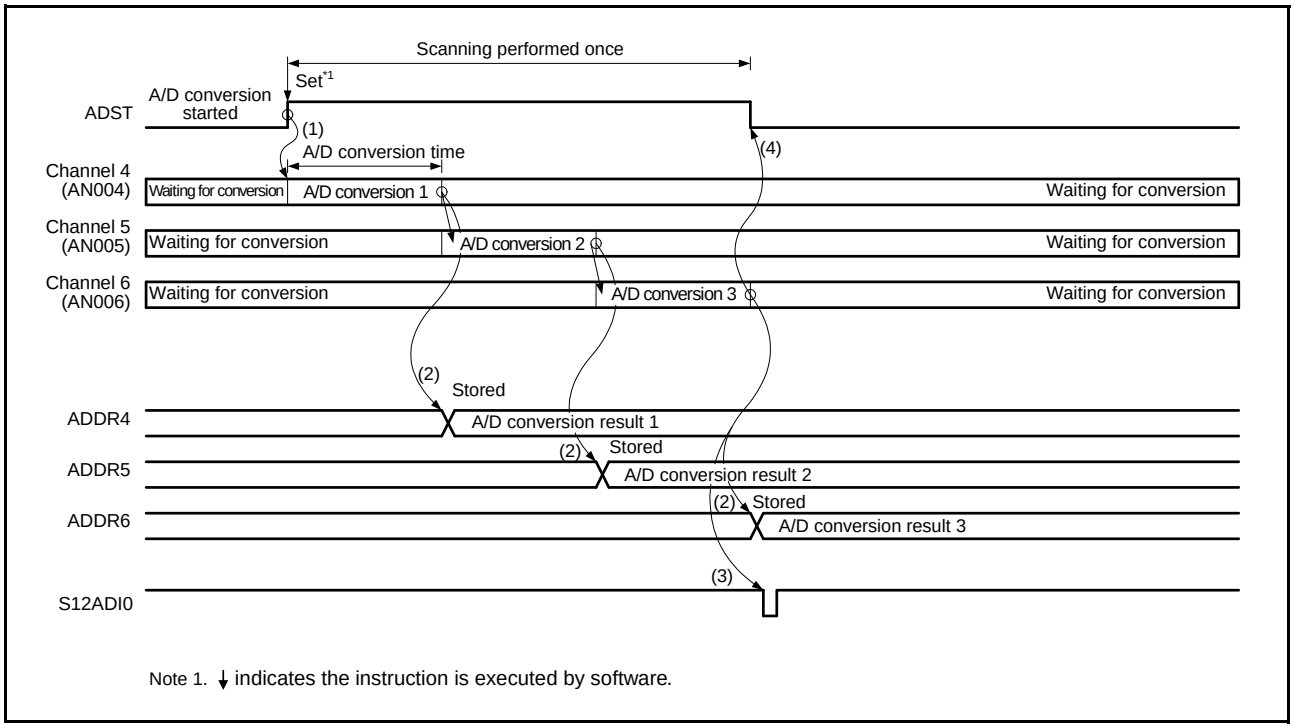


Figure 44.5 Example of Operation in Single Scan Mode (Basic Operation: AN004, AN005, AN006 Selected)

44.3.2.2 Channel Selection and Self-Diagnosis

When channels and self-diagnosis are selected, A/D conversion is performed once for the reference voltage VREFH0 supplied to the 12-bit A/D converter as below. After that, A/D conversion is performed only once on the analog input of the selected channels.

(1) A/D conversion for self-diagnosis is started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, synchronous trigger, or asynchronous trigger input.
(2) When A/D conversion for self-diagnosis is completed, A/D conversion result is stored into the A/D self-diagnosis data register (ADRD), and A/D conversion is performed for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(3) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(4) When A/D conversion of all the selected channels is completed, an S12ADI0 interrupt request is generated if the ADCSR.ADIE bit is 1 (S12ADI0 interrupt upon scanning completion enabled).
(5) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels is completed. Then the 12-bit A/D converter enters a wait state.

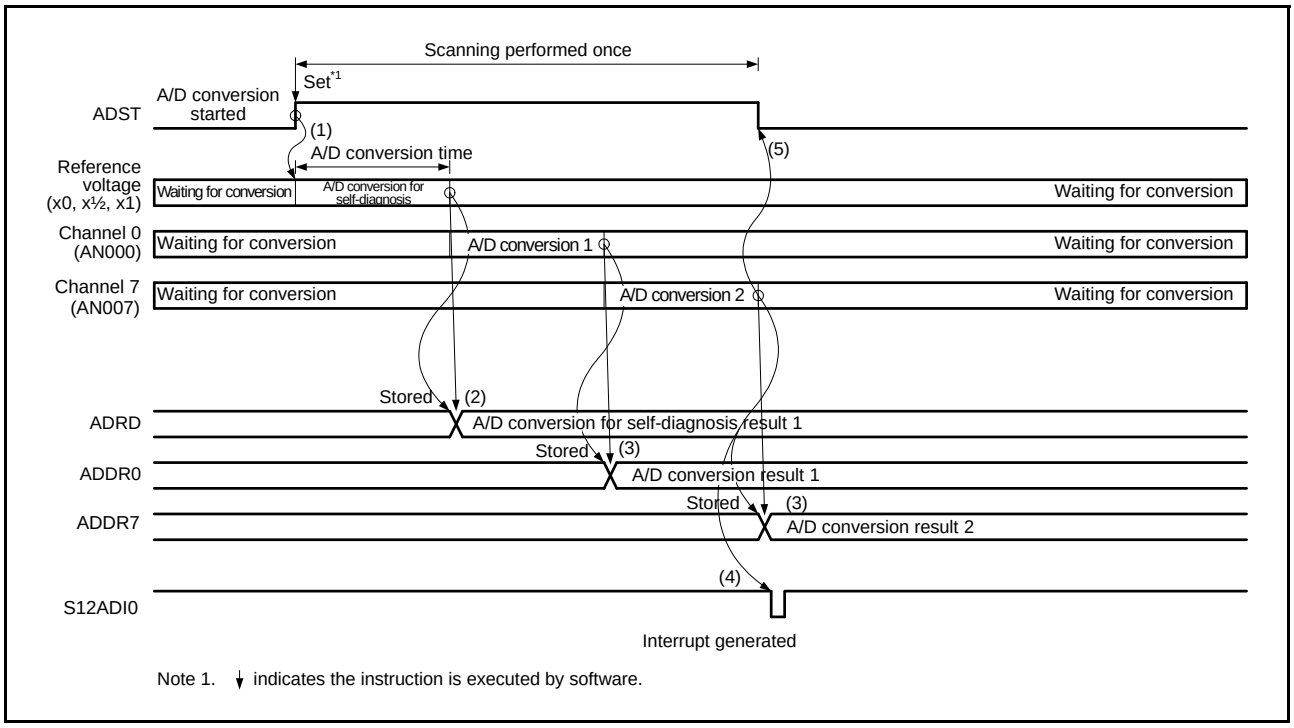


Figure 44.6 Example of Operation in Single Scan Mode (Basic Operation: AN000, AN007 Selected + Self-Diagnosis)

44.3.2.3 A/D Conversion of Temperature Sensor Output/Internal Reference Voltage

A/D conversion of the temperature sensor output and internal reference voltage is performed in single scan mode as below.

All channels should be deselected (by setting the ADANSA0 and ADANSA01 register bits to all 0 and the ADCSR.DBLE bit to 0). When selecting A/D conversion of the temperature sensor output, the A/D conversion select bit for the internal reference voltage (ADEXICR.OCSA) should be set to 0 (deselected). When selecting A/D conversion of the internal reference voltage, the A/D conversion select bit for the temperature sensor output (ADEXICR.TSSA) should be set to 0 (deselected).

(1) Set the sampling time to 5 µs or longer.
(2) After switching to A/D conversion of the internal reference voltage or the temperature sensor output, start A/D conversion by setting the ADST bit to 1.
(3) When A/D conversion is completed, the conversion result is stored into the corresponding A/D temperature sensor data register (ADTSDR) or A/D internal reference voltage data register (ADOCDR). If the ADCSR.ADIE bit is 1 (S12ADI0 interrupt upon scanning completion enabled), an S12ADI0 interrupt request is generated.
(4) The ADST bit remains 1 during A/D conversion, and is automatically cleared to 0 upon completion of A/D conversion. Then the 12-bit A/D converter enters a wait state.

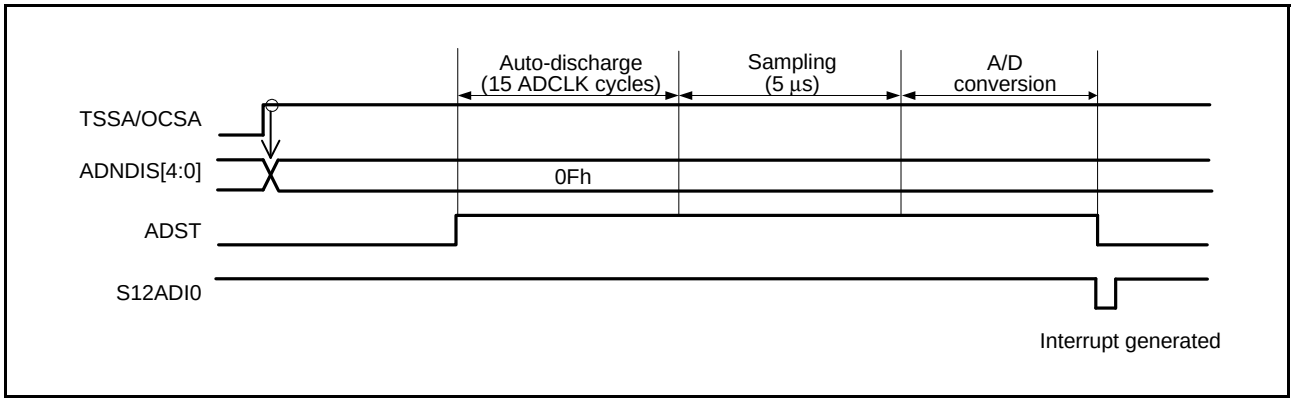


Figure 44.7 Example of Operation in Single Scan Mode (Temperature Sensor Output or Internal Reference Voltage Selected)

44.3.2.4 A/D Conversion in Double Trigger Mode

In single scan mode with double trigger mode, single scan operation started by synchronous trigger is performed twice as below.
Self-diagnosis should be deselected, and the temperature sensor output A/D conversion select bit (ADEXICR.TSSA) and the internal reference voltage A/D conversion select bit (ADEXICR.OCSA) should be set to 0.
Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated to the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1. When the DBLE bit in ADCSR is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid. In double trigger mode, synchronous triggers should be selected using the ADSTRGR.TRSA[5:0] bits, the ADCSR.EXTRG bit should be set to 0, and the ADCSR.TRGE bit should be set to 1. Software trigger should not be used.

(1) When the ADCSR.ADST bit is set to 1 (A/D conversion start) by synchronous trigger input, A/D conversion is started on the single channel selected by the ADCSR.DBLANS[4:0] bits.
(2) When A/D conversion is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(3) The ADST bit is automatically cleared to 0 and the 12-bit A/D converter enters a wait state. Here, an S12ADI0 interrupt request is not generated irrespective of the ADCSR.ADIE bit setting (S12ADI0 interrupt upon scanning completion enabled).
(4) When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the second trigger input, A/D conversion is started on the single channel selected by the ADCSR.DBLANS[4:0] bits.
(5) When A/D conversion is completed, the A/D conversion result is stored into the A/D data duplication register (ADDBLDR), which is exclusively used in double trigger mode.
(6) If the ADCSR.ADIE bit is 1 (S12ADI0 interrupt upon scanning completion enabled), an S12ADI0 interrupt request is generated.
(7) The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion is completed. Then the 12-bit A/D converter enters a wait state.

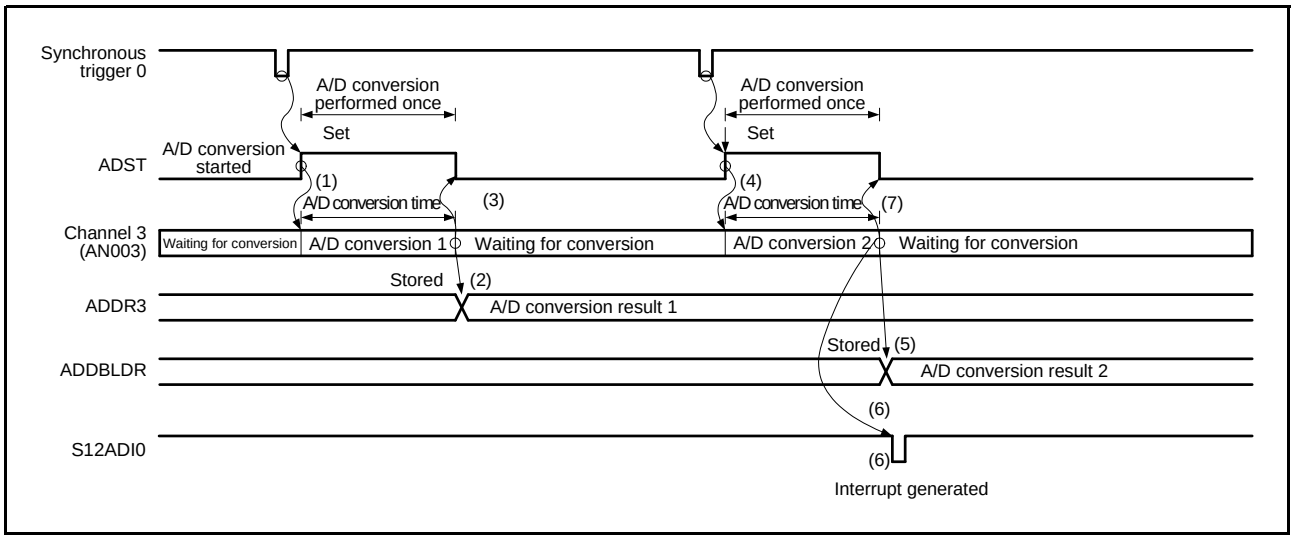


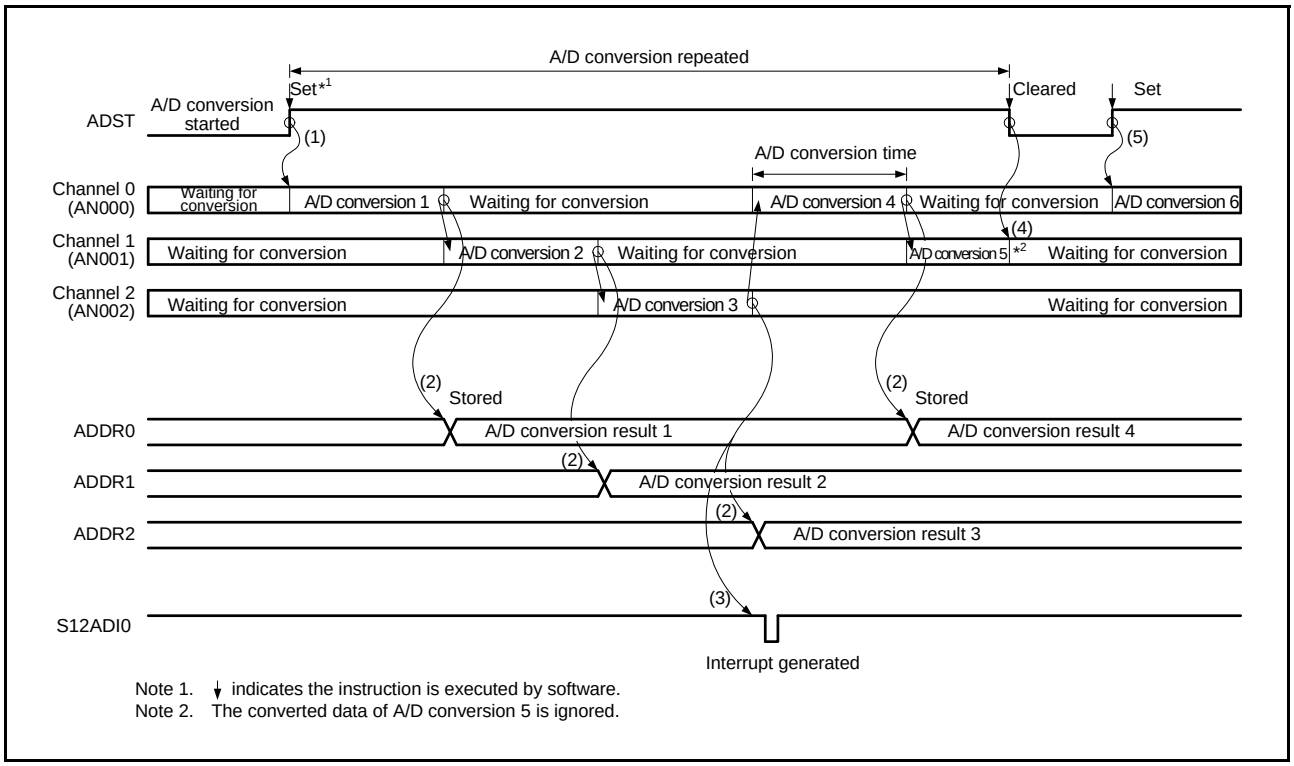
Figure 44.8 Example of Operation in Single Scan Mode (Double Trigger Mode Selected; AN003 Duplicated)

44.3.3 Continuous Scan Mode

44.3.3.1 Basic Operation

In basic operation of continuous scan mode, A/D conversion is performed repeatedly on the analog input of the specified channels as below.
In continuous scan mode, the temperature sensor output A/D conversion select bit (ADEXICR.TSSA) and the internal reference voltage A/D conversion select bit (ADEXICR.OCSA) should be set to 0 (deselected).

(1) When the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, synchronous trigger, or asynchronous trigger input, A/D conversion is performed for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(2) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(3) When A/D conversion of all the selected channels is completed, an S12ADI0 interrupt request is generated if the ADCSR.ADIE bit is 1 (S12ADI0 interrupt upon scanning completion enabled).
The 12-bit A/D converter sequentially starts A/D conversion for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(4) The ADCSR.ADST bit is not automatically cleared to 0 and steps 2 and 3 are repeated as long as the bit remains 1 (A/D conversion start). When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the 12-bit A/D converter enters a wait state.
(5) When the ADST bit is later set to 1 (A/D conversion start), A/D conversion is started again for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.



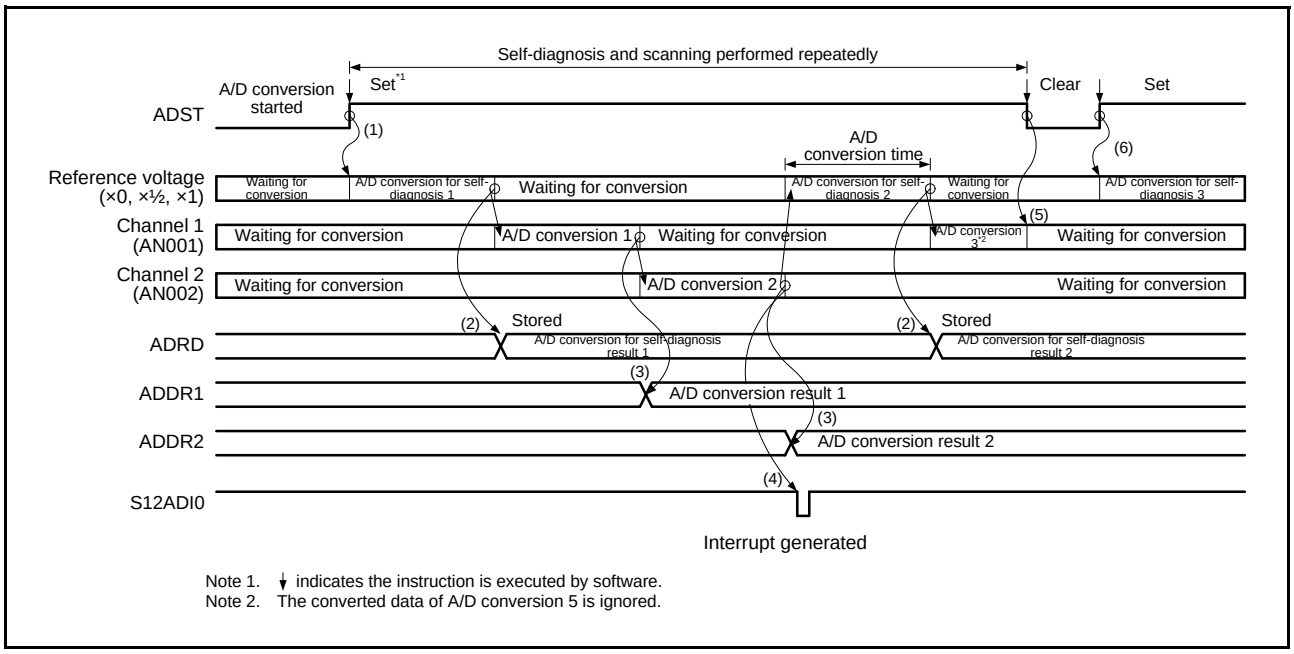
Note 1. ↓ indicates the instruction is executed by software.
Note 2. The converted data of A/D conversion 5 is ignored.

Figure 44.9 Example of Operation in Continuous Scan Mode (Basic Operation: AN000 to AN002 Selected)

44.3.3.2 Channel Selection and Self-Diagnosis

When channels and self-diagnosis are selected at the same time, A/D conversion is first performed for the reference voltage VREFH0 supplied to the 12-bit A/D converter, and then A/D conversion is performed on the analog input of the selected channels, which sequence is repeated as below. In continuous scan mode, the temperature sensor output A/D conversion select bit (ADEXICR.TSSA) and the internal reference voltage A/D conversion select bit (ADEXICR.OCSA) should be set to 0 (deselected).

(1) When the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, synchronous trigger, or asynchronous trigger input, A/D conversion for self-diagnosis is started first.
(2) When A/D conversion for self-diagnosis is completed, the A/D conversion result is stored into the A/D self-diagnosis data register (ADRD). A/D conversion is then performed for ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(3) Each time A/D conversion of a single channel is completed, the A/D conversion result is stored into the corresponding A/D data register (ADDRy).
(4) When A/D conversion of all the selected channels is completed, an S12ADI0 interrupt request is generated if the ADCSR.ADIE bit is 1 (S12ADI0 interrupt upon scanning completion enabled). At the same time, the 12-bit A/D converter starts A/D conversion for self-diagnosis and then starts A/D conversion on ANn channels selected by the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(5) The ADST bit is not automatically cleared and steps 2 to 4 are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the 12-bit A/D converter enters a wait state.
(6) When the ADST bit is later set to 1 (A/D conversion start), the A/D conversion for self-diagnosis is started again.



Note 1. ↓ indicates the instruction is executed by software.
Note 2. The converted data of A/D conversion 5 is ignored.

Figure 44.10 Example of Operation in Continuous Scan Mode (Basic Operation; AN001 and AN002 Selected + Self-Diagnosis)

44.3.4 Group Scan Mode

44.3.4.1 Basic Operation

In basic operation of group scan mode, A/D conversion is performed once on the analog inputs of all the specified channels in group A and group B after scanning is started by a synchronous trigger as below. Scan operation of each group is similar to the scan operation in single scan mode.
The synchronous triggers of group A and B can be selected using the TRSA[5:0] and TRSB[5:0] bits in ADSTRGR, respectively. The different triggers should be used for group A and group B to prevent simultaneous A/D conversion of group A and group B. Software trigger should not be used.
The group A channels to be A/D-converted are selected using the ADANSA0 and ADANSA1 registers while the group B channels to be A/D-converted are selected using the ADANSB0 and ADANSB1 registers. The same channels cannot be selected for both groups.
In group scan mode, the temperature sensor output A/D conversion select bit (ADEXICR.TSSA) and the internal reference voltage A/D conversion select bit (ADEXICR.OCSA) should be set to 0 (deselected).
When self-diagnosis is selected in group scan mode, self-diagnosis is separately executed for group A and group B.
The following describes operation in group scan mode using a trigger from the MTU. The TRG4AN and TRG4BN triggers from the MTU are assumed to be used to start conversion of group A and group B, respectively.

(1) Scanning of group A is started by the TRG4AN trigger from the MTU.
(2) When group A scanning is completed, an S12ADI0 interrupt is generated if the ADCSR.ADIE bit is 1 (S12ADI0 interrupt upon scanning completion enabled).
(3) Scanning of group B is started by the TRG4BN trigger from the MTU.
(4) When group B scanning is completed, a GBADI interrupt is generated if the ADCSR.GBADIE bit is 1 (GBADI interrupt upon scanning completion enabled).

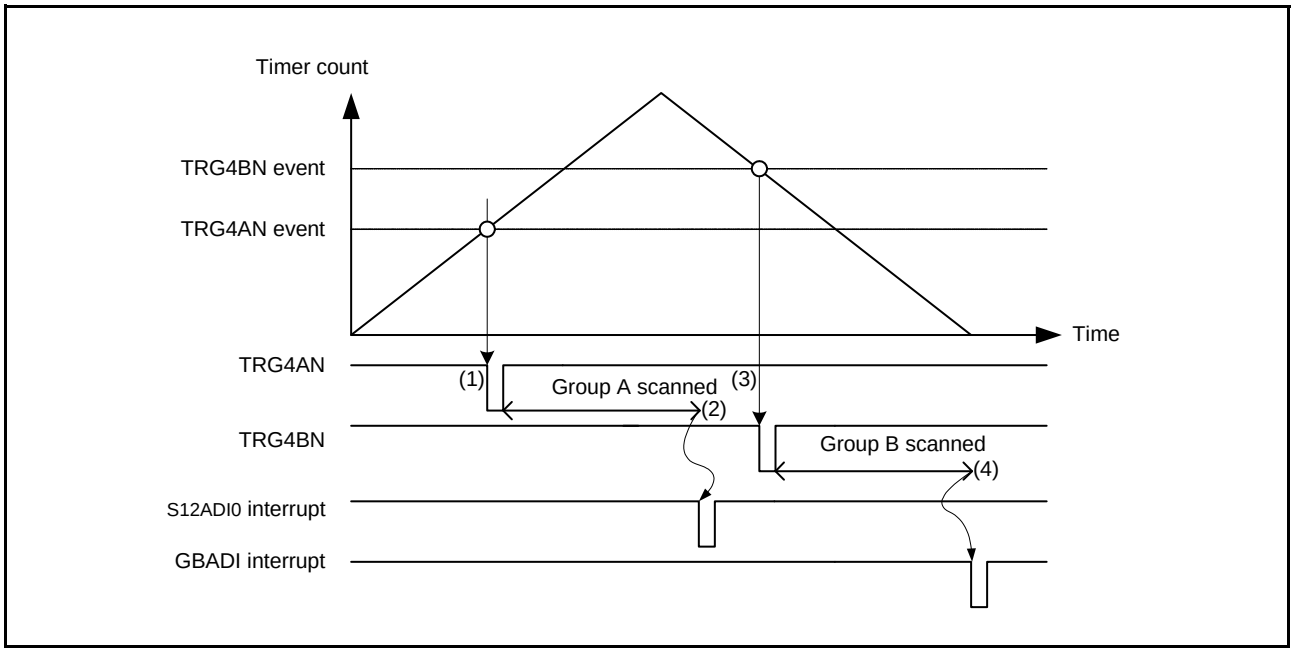


Figure 44.11 Example of Operation in Group Scan Mode (Basic Operation: Synchronous Triggers from MTU Used)

44.3.4.2 A/D Conversion in Double Trigger Mode

When double trigger mode is selected in group scan mode, two rounds of single scan operation started by a synchronous trigger are performed as a sequence for group A. For group B, single scan operation started by a synchronous trigger is performed once.
In group scan mode, the synchronous triggers of group A and B can be selected using the TRSA[5:0] and TRSB[5:0] bits in ADSTRGR, respectively. The different triggers should be used for group A and group B to prevent simultaneous A/D conversion of group A and group B. Software trigger and asynchronous trigger should not be used.
The group A and group B channels to be A/D-converted are selected using the ADCSR.DBLANS[4:0] bits and the ADANSB0 and ADANSB1 registers, respectively. The same channels cannot be selected for both groups.
In group scan mode, the temperature sensor output A/D conversion select bit (ADEXICR.TSSA) and the internal reference voltage A/D conversion select bit (ADEXICR.OCSA) should be set to 0 (deselected).
When double trigger mode is selected in group scan mode, self-diagnosis cannot be selected.
Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated to the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1.
The following describes operation in group scan mode with double trigger mode using a synchronous trigger from the MTU. The TRG4ABN and TRG0AN triggers from the MTU are assumed to be used to start conversion of group A and group B, respectively.

(1) Scanning of group B is started by the TRG0AN trigger from the MTU.
(2) When group B scanning is completed, a GBADI interrupt is generated if the ADCSR.GBADIE bit is 1 (GBADI interrupt upon scanning completion enabled).
(3) The first scanning of group A is started by the first TRG4ABN trigger from the MTU.
(4) When the first scanning of group A is completed, the conversion result is stored into the corresponding A/D data register (ADDRy); an S12ADI0 interrupt request is not generated irrespective of the ADIE bit setting in ADCSR.
(5) The second scanning of group A is started by the second TRG4ABN trigger from the MTU.
(6) When the second scanning of group A is completed, the conversion result is stored into ADDBLDR. An S12ADI0 interrupt is generated if the ADCSR.ADIE bit is 1 (S12ADI0 interrupt upon scanning completion enabled).

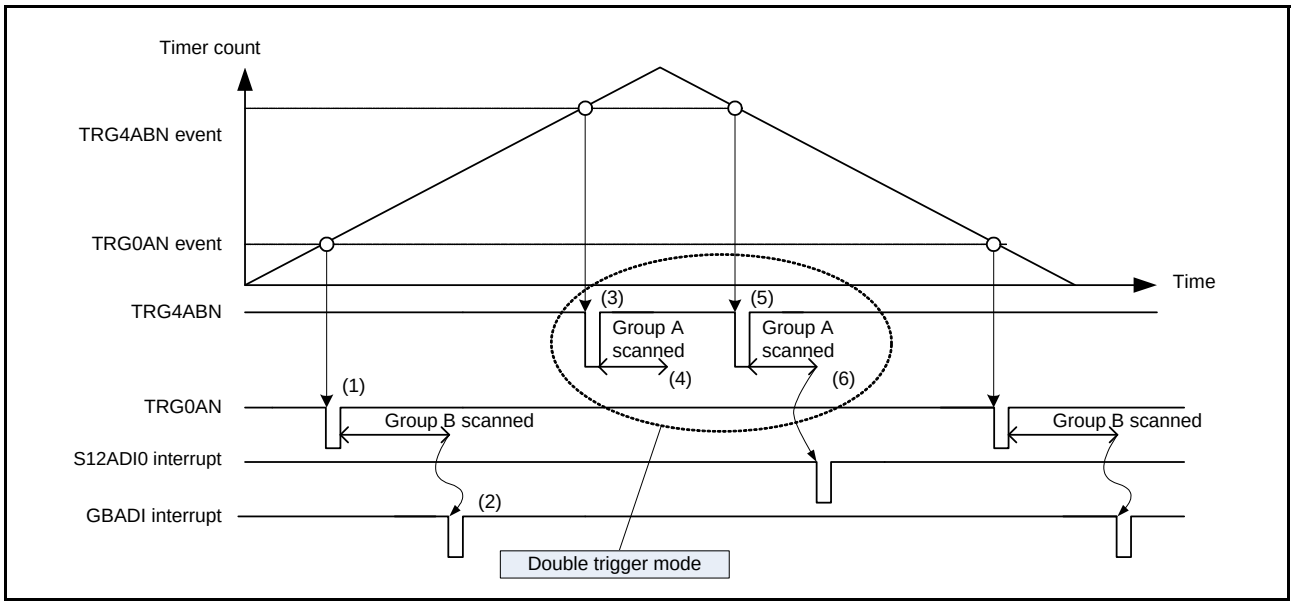


Figure 44.12 Example of Operation in Group Scan Mode with Double Trigger Mode (Basic Operation: Synchronous Triggers from MTU Used)

44.3.4.3 Operation under Group-A Priority Control

Setting the PGS bit in the A/D group scan priority control register (ADGSPCR) to 1 in group scan mode makes operation proceed under group-A priority control. When setting the PGS bit in the ADGSPCR register to 1, follow the procedure described in Figure 44.13. If the procedure is not followed, A/D conversion operation and stored data are not guaranteed.
In operation in basic group scan mode, input of the trigger for the other group during operation for A/D conversion in group A or group B is ignored. Under group-A priority control, if a group-A trigger is input during A/D conversion for group B, A/D conversion for group B is discontinued and A/D conversion for group A proceeds. If the setting of the ADGSPCR.GBRSCN bit is 0, the converter enters a wait state on completion of the A/D conversion for group A. If the setting of the ADGSPCR.GBRSCN bit is 1, the converter automatically restarts scanning for group B from the head of the group after completion of the A/D conversion for group A. Table 44.9 summarizes operations in response to the input of a trigger during A/D conversion with the settings of the ADGSPCR.GBRSCN bit.

Scan operations in group A or group B are the same in single scan mode. Furthermore, single scanning continues to proceed if the ADGSPCR.GBRP bit is set to 1 during scanning operations for group B.

For the trigger settings in group scan mode, select a synchronous trigger for group A using the ADSTRGR.TRSA[5:0] bits and select a synchronous trigger different from that of group A for group B using the ADSTRGR.TRSB[5:0] bits. Set the ADSTRGR.TRSB[5:0] bits to 3Fh when setting the ADGSPCR.GBRP bit to 1. Furthermore, as targets for A/D conversion, select channels for group A using the ADANSA0 and ADANSA1 registers, and for group B, select channels different from those for group A using the ADANSB0 and ADANSB1 registers.

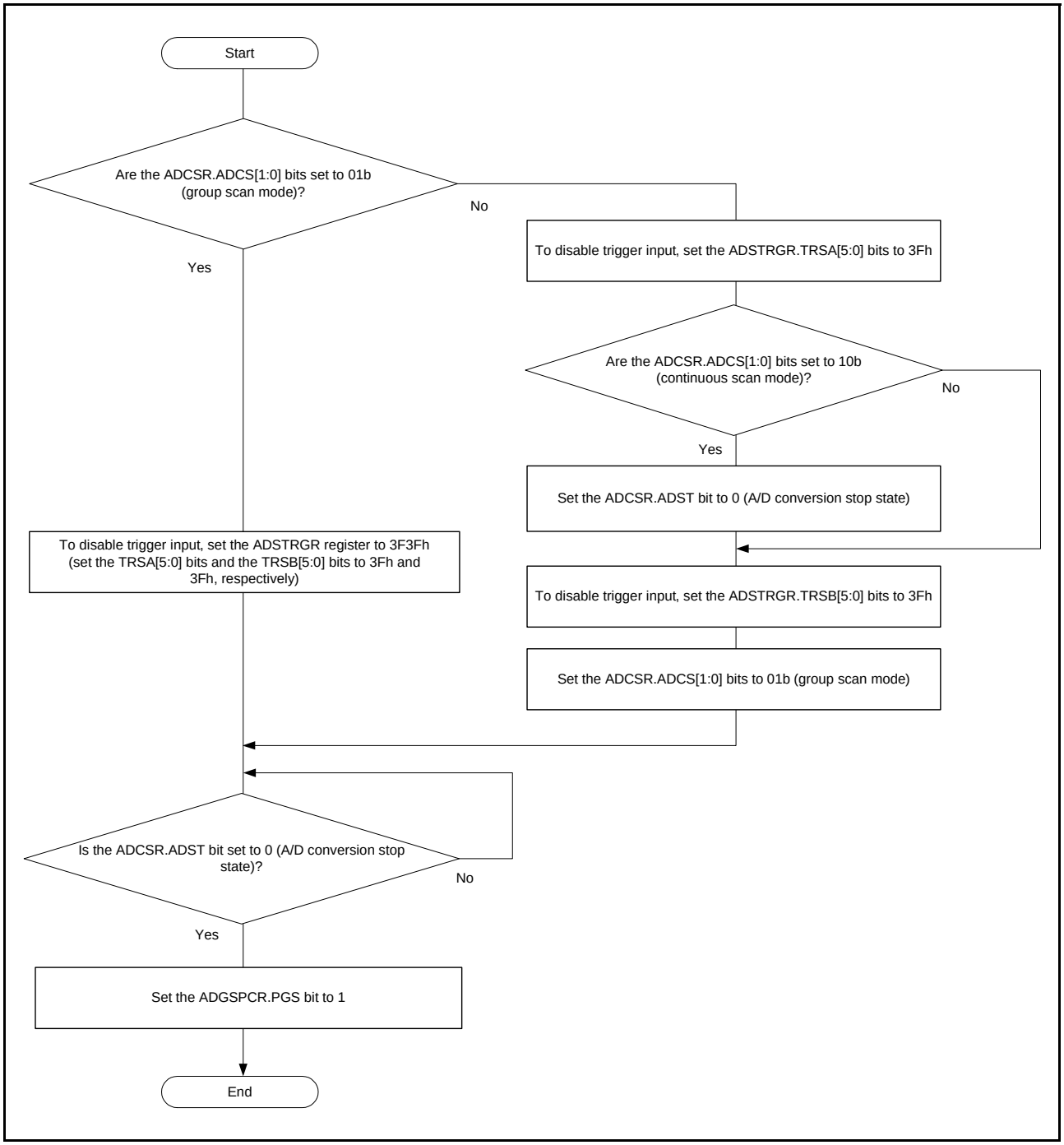


Figure 44.13 Flow of Setting the ADGSPCR.PGS Bit

Table 44.9 Control of A/D Conversion Operations According to the Settings of the ADGSPCR.GBRSCN Bit

A/D Conversion Operation	Trigger Input	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
When A/D conversion for group A is in progress	Input of trigger for group A	Trigger input is ineffective.	Trigger input is ineffective.
	Input of trigger for group B	Trigger input is ineffective.	A/D conversion is performed on group B after A/D conversion on group A is completed.
When A/D conversion for group B is in progress	Input of trigger for group A	Conversion for group B that is in progress is discontinued and conversion for group A starts.	• Conversion in progress for group B is discontinued and conversion for group A starts. • Conversion for group B starts after conversion for group A is completed.
	Input of trigger for group B	Trigger input is ineffective.	Trigger input is ineffective.

The following describes the operations in group scan mode under group-A priority control (i.e. ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0) when channel 0 is selected for group A and channels 1 to 3 are selected for group B.

(1) When input of a trigger for group B sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers, starting from the channel with the smallest number n.
(2) On completion of A/D conversion, the result is stored in the corresponding A/D data register (ADDRy).
(3) The ADCSR.ADST bit is cleared on the input of a trigger for group A while operation for A/D conversion in group B is in progress, and the latter is discontinued. After that, the ADCSR.ADST bit is set to 1 (A/D conversion start), and conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(4) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(5) An S12ADI0 interrupt request is generated if the setting of the ADCSR.ADIE bit is 1 (S12ADI0 interrupt upon scanning completion enabled).
(6) After the ADST bit is automatically cleared, again, the bit is automatically set to 1 (A/D conversion start) and conversion for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers, starting from the channel with the smallest number n.
(7) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(8) A GBADI interrupt request is generated if the setting of the ADCSR.GBADIE bit is 1 (GBADI interrupt upon group B scanning completion enabled).
(9) The ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically cleared on completion of conversion, after which the A/D converter enters a wait state.

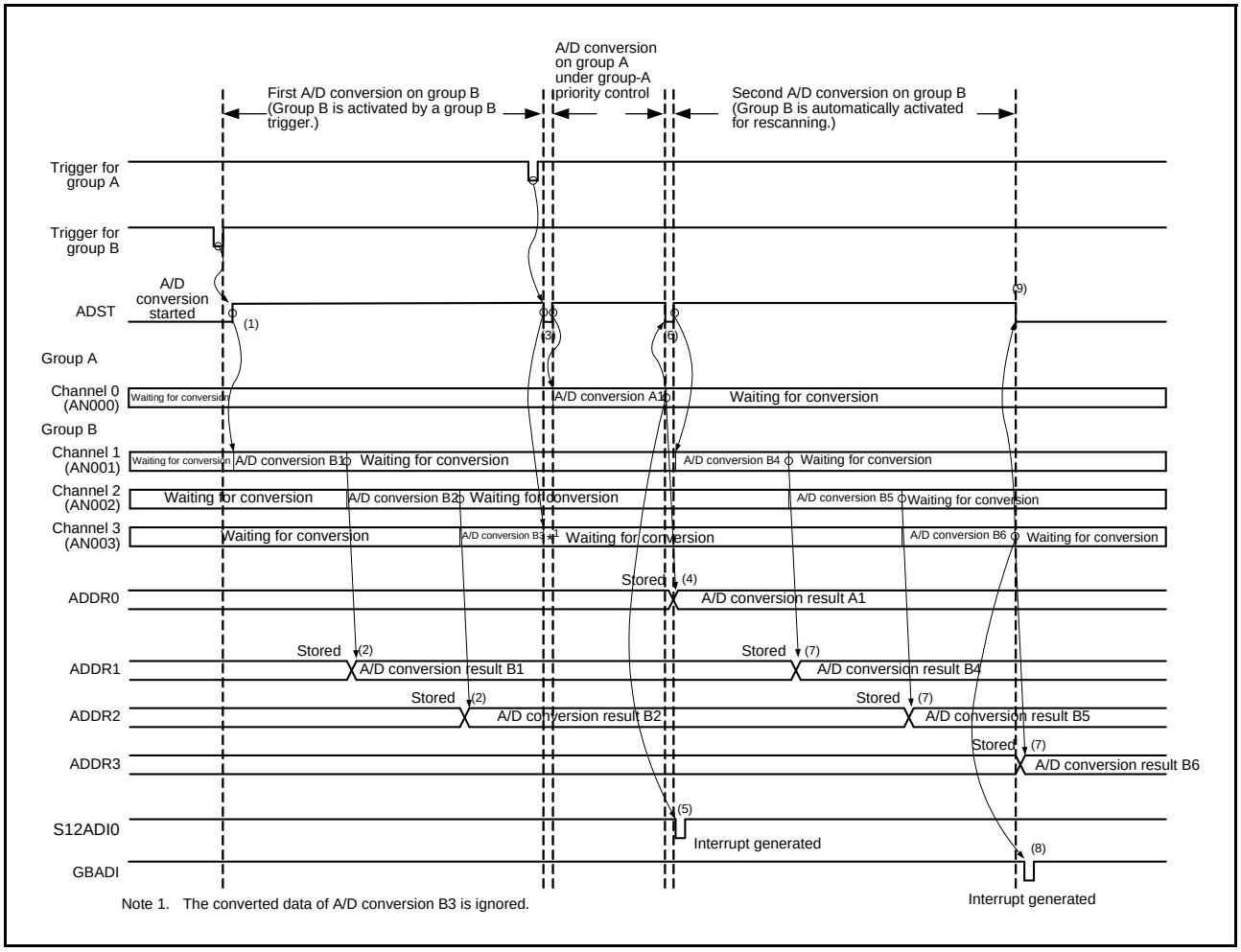


Figure 44.14 Example of Operations under Group-A Priority Control (1) (when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0)

The following is an example when a group A trigger is input again during rescanning operation on group B. In this example, channel 0 is selected for group A and channels 1 to 3 are selected for group B when operation on group A is given priority (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0).

(1) When a group B trigger input sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the lowest number n.
(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(3) The ADCSR.ADST bit is cleared to 0 (A/D conversion stop) on the input of a trigger for group A while operation for A/D conversion in group B is in progress, and the latter is discontinued.
(4) After that, the ADCSR.ADST bit is set to 1 automatically and A/D conversion for the ANn group A channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the lowest number n.
(5) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(6) An S12ADI0 interrupt request is generated if the setting of the ADCSR.ADIE bit is 1 (S12ADI0 interrupt upon scanning completion enabled).

(7) On completion of A/D conversion on the group A, rescanning operation on group B sets the ADCSR.ADST bit to 1 automatically if the setting of the ADGSPCR.GBRSCN bit is 1 (rescanning operation enabled). After that, A/D conversion for the ANn group B channels selected in the ADANSB0 and ADANSB1 registers starts again in order from the channel with the lowest number n.

(8) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).

(9) If a group A trigger is input during A/D conversion on group B for rescanning, the ADCSR.ADST bit is cleared to 0 (A/D conversion stop) and the ongoing A/D conversion on group B is stopped.

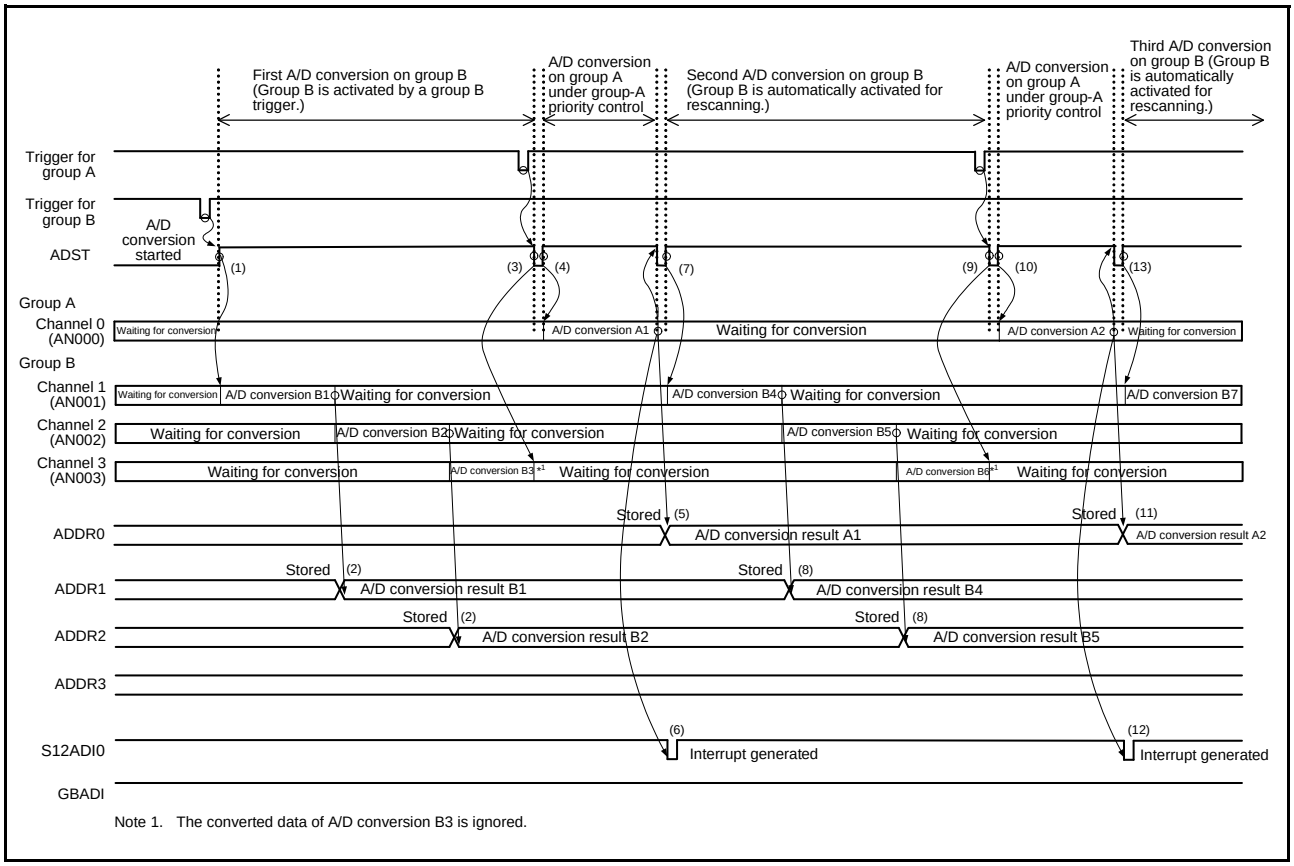
(10) After that, the ADCSR.ADST bit is set to 1 automatically and A/D conversion for the ANn group A channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the lowest number n.

(11) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).

(12) An S12ADI0 interrupt request is generated if the setting of the ADCSR.ADIE bit is 1 (S12ADI0 interrupt upon scanning completion enabled).

(13) On completion of A/D conversion on group A, rescanning operation on group B sets the ADCSR.ADST bit to 1 automatically if the setting of the ADGSPCR.GBRSCN bit is 1 (rescanning operation enabled). After that, A/D conversion for the ANn group B channels selected in the ADANSB0 and ADANSB1 registers starts again in order from the channel with the lowest number n.

(14) If a group A trigger is input during A/D conversion on group B for rescanning, steps 9 to 13 are repeated. If a group A trigger is not input, the ADCSR.ADST bit is cleared automatically on completion of A/D conversion on group B and the 12-bit A/D converter enters a wait state.



Note 1. The converted data of A/D conversion B3 is ignored.

Figure 44.15 Example of Operations under Group-A Priority Control (2) (when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0)

The following is an example of a rescanning operation in which a group B trigger is input during A/D conversion on group A. In this example, channels 1 to 3 are selected for group A and channel 0 is selected for group B when operation on group A is given priority (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0).

(1) When input of a trigger for group A sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(3) If a group B trigger is input during A/D conversion on group A, A/D conversion on group B can be performed after the A/D conversion on group A is completed. (However, if group A triggers are input continuously, the scan operation on group B is canceled by group A and is not performed.)
(4) On completion of the A/D conversion on the group A, an S12ADI0 interrupt request is generated if the setting of the ADCSR.ADIE bit is 1 (S12ADI0 interrupt upon scanning completion enabled).
(5) On completion of the A/D conversion on the group A, activation of group B for rescanning sets the ADCSR.ADST bit to 1 automatically.
After that, conversion for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers, starting from the channel with the smallest number n.
(6) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(7) On completion of the rescanning operation on the group B, a GBADI interrupt request is generated if the setting of the ADCSR.GBADIE bit is 1 (GBADI interrupt upon scanning completion enabled).
(8) The ADST bit retains the value 1 (A/D conversion start) during A/D conversion and is automatically cleared on completion of conversion, after which the A/D converter enters a wait state.

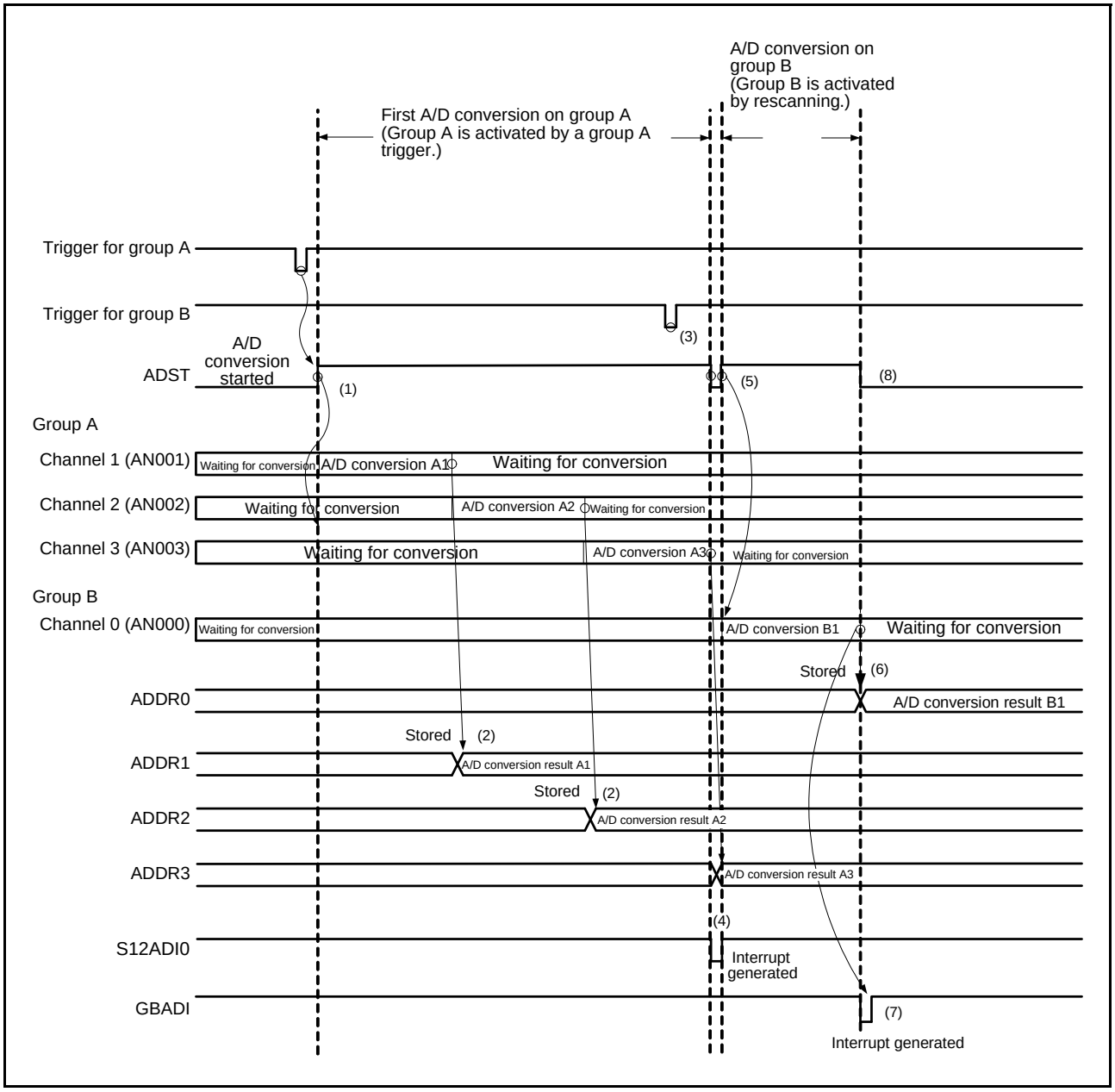
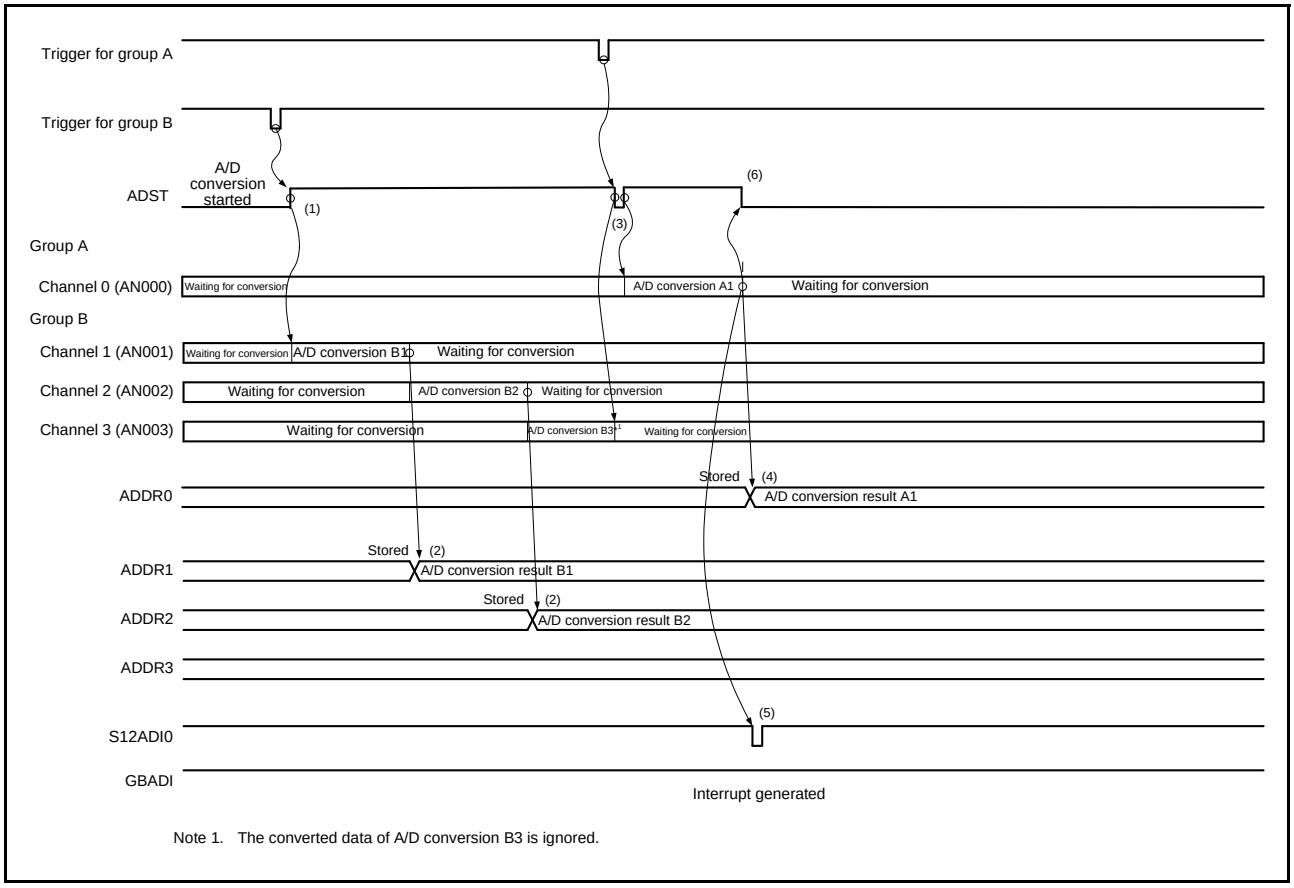


Figure 44.16 Example of Operations under Group-A Priority Control (3) (when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0)

The following is an example of operation under group-A priority control in which channel 0 is selected for group A and channels 1 to 3 are selected for group B (ADGSPCR.GBRSCN = 0, ADGSPCR.GBRP = 0).

(1) When input of a trigger for group B sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers, starting from the channel with the smallest number n.
(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(3) If a group A trigger is input during A/D conversion on group B, the ADCSR.ADST bit is cleared to 0 and the ongoing A/D conversion on group B is stopped. After that, the ADCSR.ADST bit is set to 1 (A/D conversion start) and conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(4) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(5) An S12ADI0 interrupt request is generated if the setting of the ADCSR.ADIE bit is 1 (S12ADI0 interrupt upon scanning completion enabled).
(6) The ADCSR.ADST bit retains the value 1 (A/D conversion start) during A/D conversion and is cleared on completion of conversion, after which the A/D converter enters a wait state.

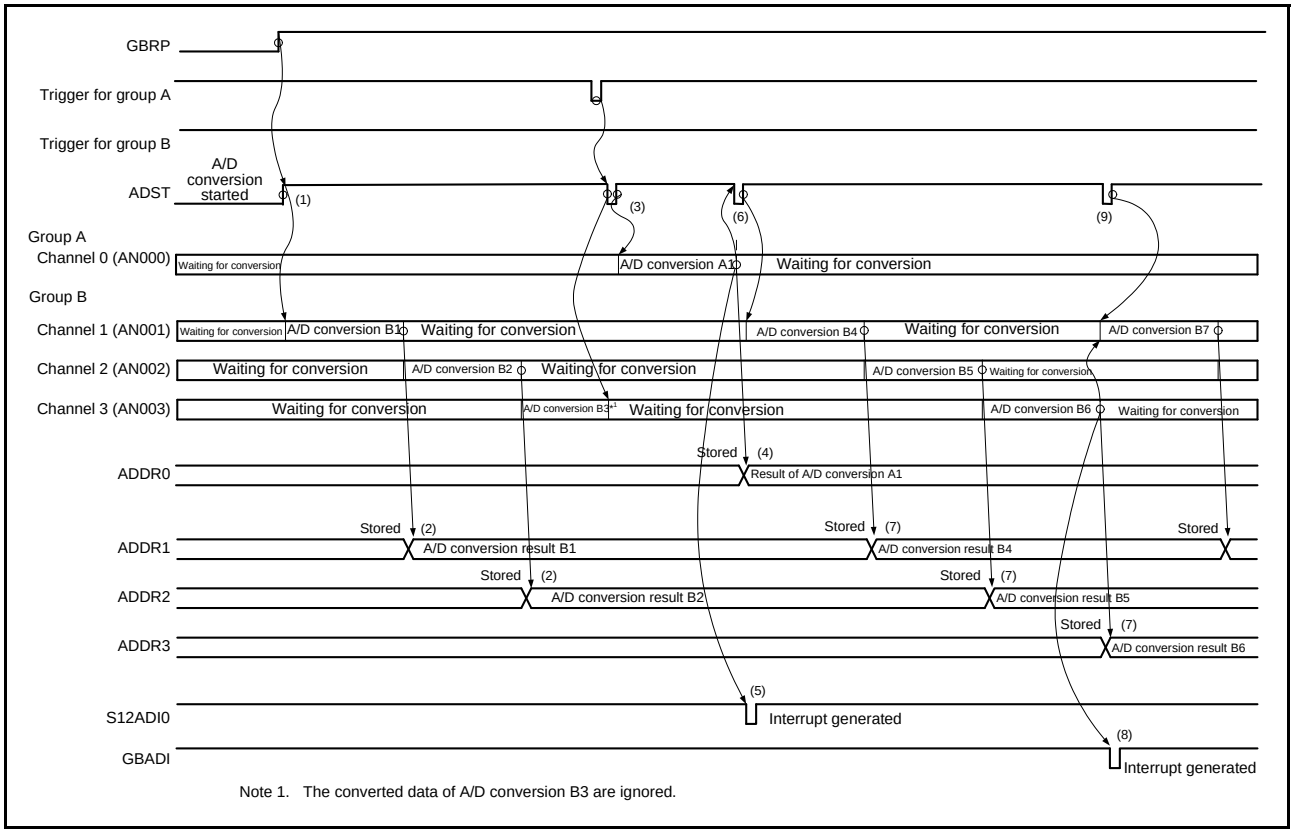


Note 1. The converted data of A/D conversion B3 is ignored.

Figure 44.17 Example of Operation under Group-A Priority Control (4) (when ADGSPCR.GBRSCN = 0 and ADGSPCR.GBRP = 0)

The following is an example of operation under group-A priority control in which channel 0 is selected for group A and channels 1 to 3 are selected for group B (ADGSPCR.GBRP = 1).

(1) The ADCSR.ADST bit is set to 1 (A/D conversion start) when ADGSPCR.GBRP is set to 1, and conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers, starting from the channel with the smallest number n.
(2) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(3) If a group A trigger is input during A/D conversion on group B, the ADCSR.ADST bit is cleared to 0 and the ongoing A/D conversion on group B is stopped. After that, the ADCSR.ADST bit is set to 1 (A/D conversion start) and conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
(4) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(5) An S12ADI0 interrupt request is generated if the setting of the ADCSR.ADIE bit is 1 (S12ADI0 interrupt upon scanning completion enabled).
(6) After the ADST bit is automatically cleared, again, the ADCSR.ADST bit is automatically set to 1 (A/D conversion start) and conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers, starting from the channel with the smallest number n.
(7) On completion of A/D conversion on a single channel, the result is stored in the corresponding A/D data register (ADDRy).
(8) A GBADI interrupt request is generated if the setting of the ADCSR. GBADIE bit is 1.
(9) After the ADST bit is automatically cleared, again, the bit is automatically set to 1 (A/D conversion start) and conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers, starting from the channel with the smallest number n. Steps 6 to 9 are repeated as long as the ADGSPCR.GBRP bit remains 1.
Clearing of the ADCSR.ADST bit to 0 is prohibited while the ADGSPCR.GBRP bit is set to 1. To forcibly stop A/D conversion when ADGSPCR.GBRP = 1, follow the procedures for clear operation by software through the ADCSR.ADST bit shown in section 44.8.2, Notes on Stopping A/D Conversion.



Note 1. The converted data of A/D conversion B3 are ignored.

Figure 44.18 Example of Operation under Group-A Priority Control (5) (when ADGSPCR.GBRP = 1)

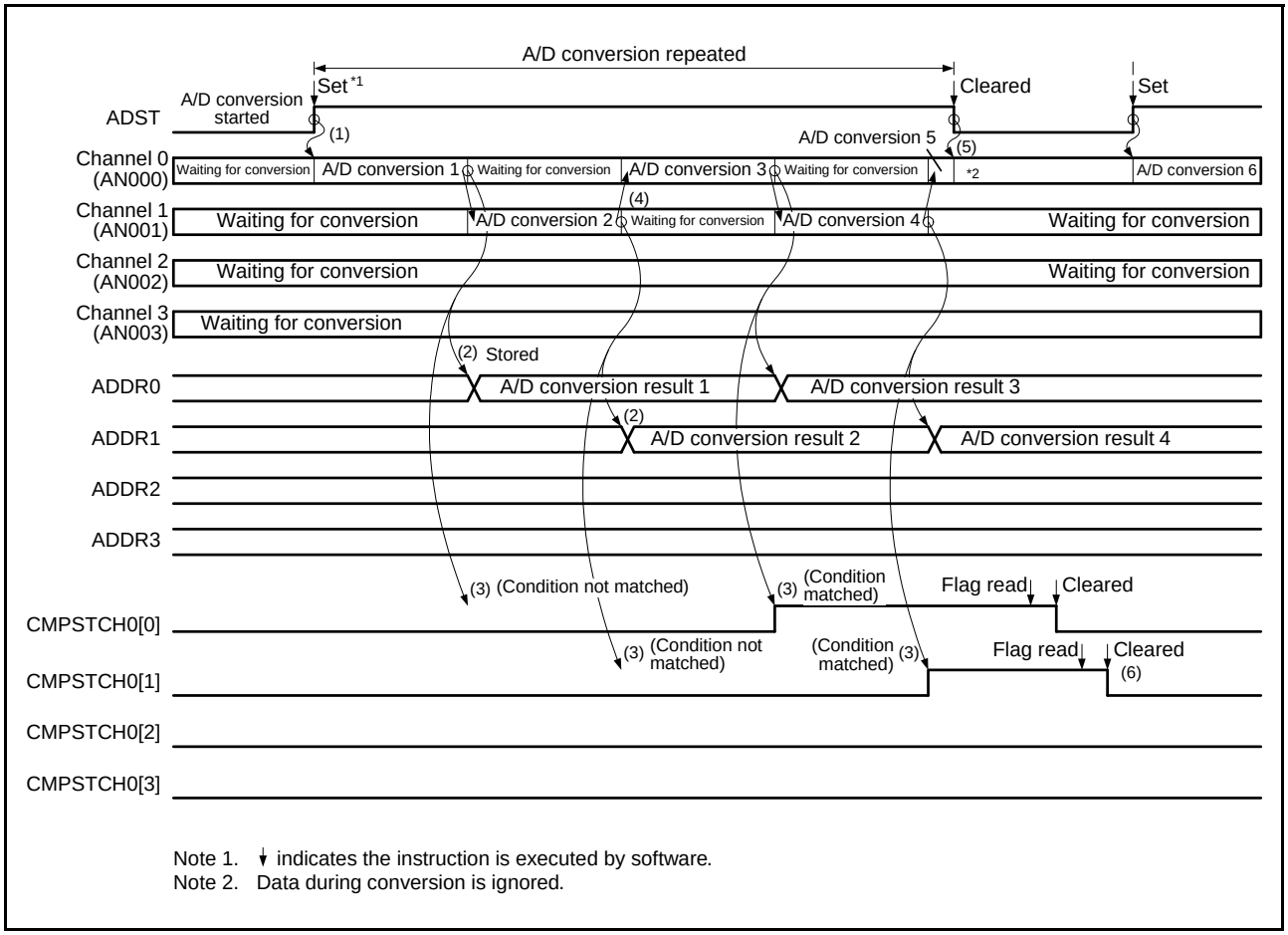
44.3.5 Compare Function (Window A, Window B)

44.3.5.1 Compare Function Window A/B

The compare function compares the reference value set in the register with the A/D conversion result. The reference value can be set for window A and window B independently. When the compare function is in use, the self-diagnosis function and double trigger mode cannot be used. Big differences between window A and window B are different interrupt output signals and that window B can select only one channel.

The following describes operations in combination of continuous scan mode and the compare function.

(1) When the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, synchronous trigger, or asynchronous trigger input A/D conversion starts in the order of the selected channel.
(2) Upon completion of A/D conversion, the result is stored in the corresponding A/D data register (ADDRy, ADTSDR, or ADOCDR). When ADCMPCR.CMPAE is 1, if the ADCMPANSRy register or the ADCMPANSER register is set for window A, the results of A/D conversion are to be compared with the values set in the ADCMPDR0 and ADCMPDR1 registers. When ADCMPCR.CMPBE is 1, if the ADCMPBNSR register is set for window B, the results of A/D conversion are to be compared with the values set in the ADWINULB and ADWINLLB registers.
(3) As a result of the comparison, when window A meets the condition set in ADCMPDR0, ADCMPDR1 or ADCMPLER, the compare window A flag (ADCMPSR0.CMPSTCHA0n, ADCMPSR1.CMPSTCHA1n, ADCMPSER.CMPSTTSA, or ADCMPSER.CMPSTOCA) is set to 1. In the same way, when window B meets the condition set in ADCMPBNSR.CMPLB, the compare window B flag (ADCMPBSR.CMPSTB) is set to 1.
(4) Upon completion of all selected A/D conversions and comparisons, scan restarts.
(5) Set the ADCSR.ADST bit to 0 (A/D conversion stop), and execute processing for the channel with the compare flag set to 1.
(6) Clear all compare flags after processing is competed. To perform comparison again, restart A/D conversion.



Note 1. ↓ indicates the instruction is executed by software.
Note 2. Data during conversion is ignored.

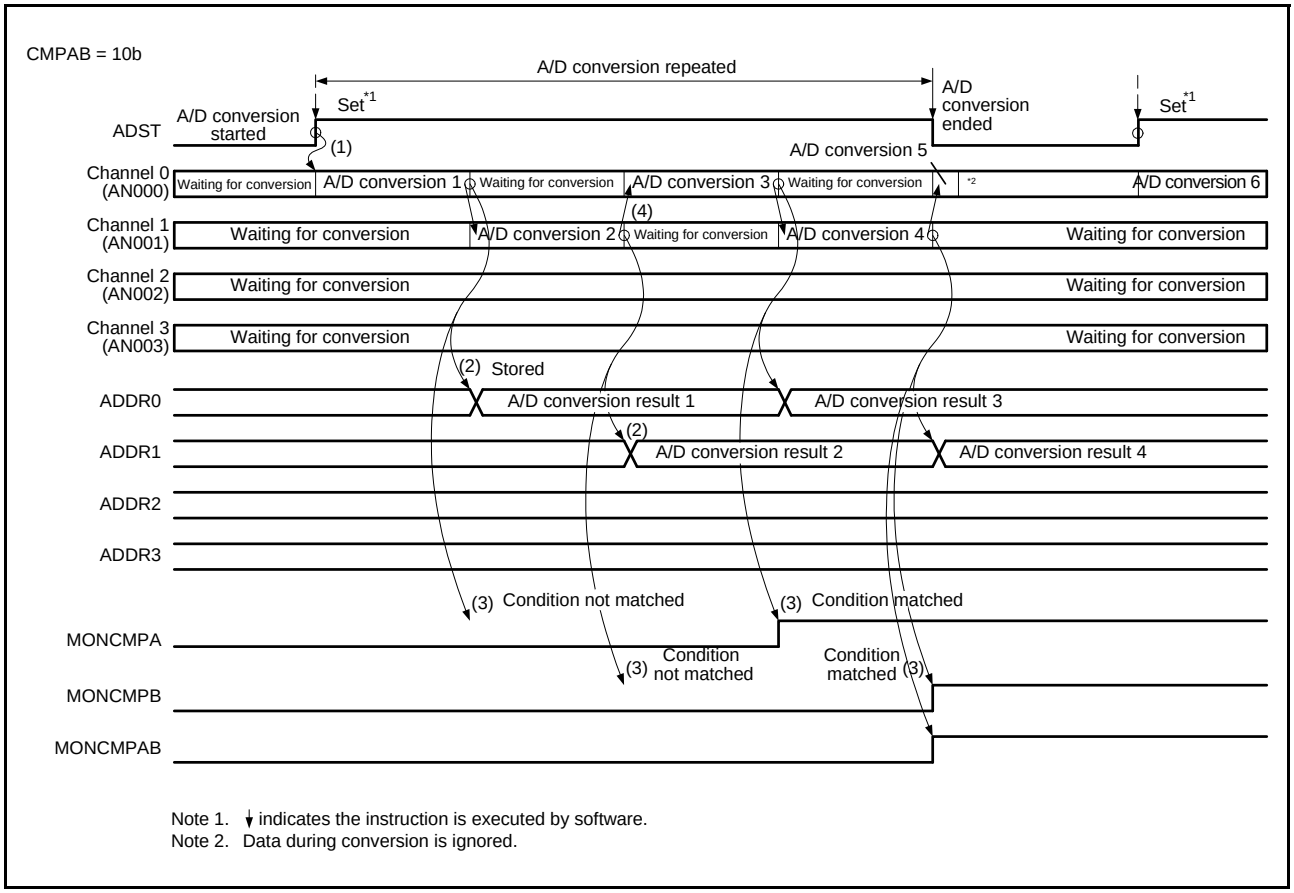
Figure 44.19 Operation Example of Comparison (AN000 to AN003 Compared)

44.3.5.2 ELC Output of Compare Function

The ELC output of the compare function is used to specify the high-side reference value and the low-side reference value for window A and window B respectively, and to compare the A/D converted value of the selected channel with the high/low-side reference value. Depending on whether the comparison conditions for window A and window B are met or not met, the ELC event (S12ADWMELC/S12ADWUMELC) is output according to the event conditions (A or B, A and B, A exor B).
If multiple channels are selected for window A, when the comparison conditions for any of the channels are met, it is recognized that the comparison conditions for window A are met.

When using this function, perform A/D conversion in single scan mode.
Any channels from AN000 to AN007, AN016 to AN020, AN027, internal reference voltage, and temperature sensor output are selectable for window A.
However, when selecting the internal reference voltage or the temperature sensor output, it cannot be selected together with any other channel. Any channels from AN000 to AN007, AN016 to AN020, AN027, internal reference voltage, and temperature sensor output are selectable for window B.
The setting procedure is as follows when this function is to be used. The setting procedure required for normal A/D conversion in single scan mode is omitted.

(1) Confirm that the value of the ADCSR.ADCS[1:0] bits is 00b (single scan mode).
(2) Select channels (from among AN000 to AN007, AN016 to AN020, AN027, temperature sensor, and internal reference voltage) in the ADCMPANSR0/ADCMPANSR1 or ADCMPANSER register (for window A) and in the ADCMPBNSR register (for window B).
(3) Set window comparison conditions in the ADCMPLR0, ADCMPLR1, ADCMPLER, and ADCMPBNSR registers, and set the upper-limit and lower-limit reference values in the ADCMPDR0, ADCMPDR1, ADWINULB, and ADWINLLB registers.
(4) Set composite conditions for window A/B, window A/B operation enable, and interrupt output enable in the ADCMPCR register. A scan end event (S12ADELC) is output to the ELC at the end of each single scan. In addition, a match or mismatch event (S12ADWMELC or S12ADWUMELC) is output with a delay of one PCLK cycle depending on the ADCMPCR.CMPAB[1:0] setting.
Since match and mismatch events are mutually exclusive, these are not output at the same time.



Note 1. ↓ indicates the instruction is executed by software.
Note 2. Data during conversion is ignored.

Figure 44.20 Example of Window Compare Function Operation (AN000 to AN003 Compared)

44.3.5.3 Using Data Buffers

This S12ADE is provided with a ring buffer function consisting of 16 A/D data buffers. This function sequentially stores A/D conversion results other than self-diagnosis result (including addition/average results) in data buffers (ADBUFn, n = 0 to 15) when the compare function is used.

Each conversion result is stored at the timing when the A/D conversion result is stored in the data register, and most recent 16 conversion result data are retained.

The following shows the schematic of data buffers, pointer, and overflow flag operations. When the BUFEN bit is set to1, the A/D conversion result is transferred at each end of A/D conversion. The pointer indicates the number of data buffer to which the next transferred data is to be written. When data is written to up to buffer 15, the pointer is reset to 0000b and the overflow flag is set to 1. Subsequently transferred data overwrites the previously written data. The pointer and overflow flag are reset to the initial value by writing 00h to the ADBUFPTR register.

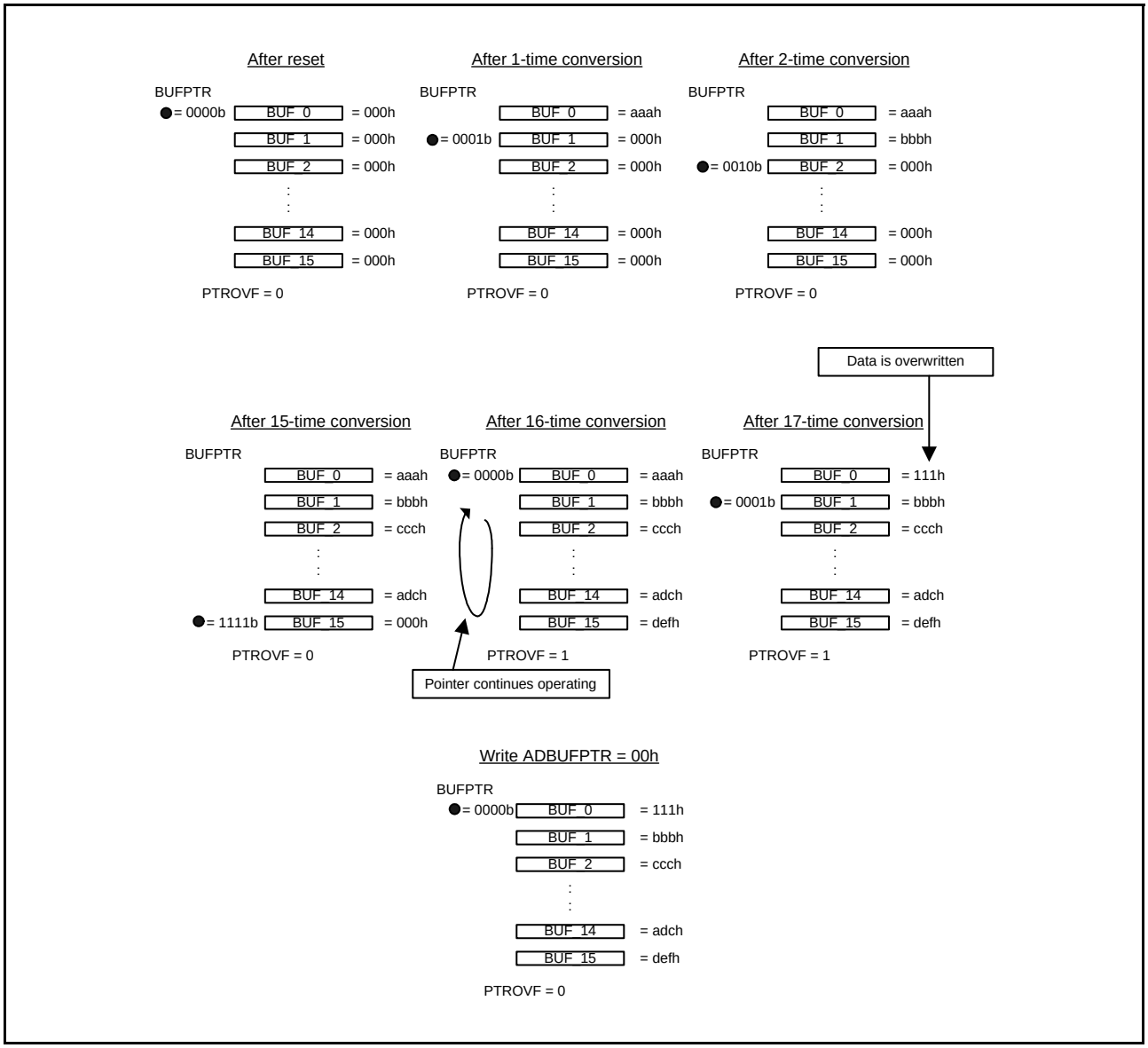


Figure 44.21 Schematic of Data Buffers, Pointer, and Overflow Flag Operations

44.3.5.4 Restrictions for Compare Function

The following restrictions are provided for the compare function.

1. The compare function must not be used together the self-diagnosis function or double trigger mode. (The compare function is not available for the ADRD register and the ADDBLDR register.)
2. Specify single scan mode when using match/mismatch event outputs.
3. When temperature sensor or internal reference voltage is selected for window A, window B operations are disabled.
4. When temperature sensor or internal reference voltage is selected for window B, window A operations are disabled.
5. It is prohibited to set the same channel for window A and window B.
6. When using the buffer function, specify single scan mode. (It is also prohibited to use double trigger mode together.)
7. Set the reference voltage values so that the high-side reference voltage value is equal to or larger than the low-side reference voltage value.

44.3.6 Analog Input Sampling Time and Scan Conversion Time

Scan conversion can be activated either by software, synchronous trigger, or asynchronous trigger input. After the start-of-scanning-delay time (t_D) has elapsed, processing for disconnection detection assistance and processing of conversion for self-diagnosis proceed, and this is followed by processing for A/D conversion.
Figure 44.22 shows the scan conversion timing in single scan mode, in which scan conversion is activated by software or a synchronous trigger. Figure 44.23 shows the scan conversion timing in single scan mode, in which scan conversion is activated by an asynchronous trigger. The scan conversion time (t_{SCAN}) includes the start-of-scanning-delay time (t_D), disconnection detection assistance processing time (t_{DIS})*1, self-diagnosis A/D conversion processing time (t_{DIAG})*2, A/D conversion processing time (t_{CONV}), and end-of-scanning-delay time (t_{ED}).
The A/D conversion processing time (t_{CONV}) consists of sampling time (t_{SPL}) and time for conversion by successive approximation (t_{SAM}). The sampling time (t_{SPL}) is used to charge sample-and-hold circuits in the A/D converter. If there is not sufficient sampling time due to the high impedance of an analog input signal source, or if the A/D conversion clock (ADCLK) is slow, sampling time can be adjusted using the ADSSTRn register.
The time for conversion by successive approximation (t_{SAM}) is at 32 ADCLK states during high-speed conversion operation, and 41 ADCLK states during low-current conversion operation. Table 44.10 shows the scan conversion time.

The scan conversion time (t_{SCAN}) in single scan mode for which the number of selected channels is n can be determined as follows:

$$t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n)^{*3} + t_{ED}$$

The scan conversion time for the first cycle in continuous scan mode is t_{SCAN} for single scan minus t_{ED}.
The scan conversion time for the second and subsequent cycles in continuous scan mode is fixed to $(t_{DIS} \times n) + t_{DIAG} + t_{DSD} + (t_{CONV} \times n)$.

Note 1. When disconnection detection assistance is not selected, $t_{DIS} = 0$. The auto-discharge period of 15 ADCLK states is inserted only when the temperature sensor or internal reference voltage is A/D-converted.
Note 2. When the self-diagnosis function is not used, $t_{DIAG} = 0$, $t_{DSD} = 0$.
Note 3. $t_{CONV} \times n$ when the sampling time (t_{SPL}) of selected channels is the same, but it is the total of the sampling time of each channel and time for conversion by successive approximation (t_{SAM}).

Table 44.10 Times for Conversion during Scanning (in Numbers of Cycles of ADCLK and PCLK)

Item			Symbol		Type/Conditions: Synchronous Trigger *5	Type/Conditions: Asynchronous Trigger	Type/Conditions: Software Trigger	Unit
Scan start processing time*1, *2	A/D conversion on group A under group-A priority control.	Group B is to be stopped. (Group A is activated after group B is stopped due to an A/D conversion source of group A.)	t_D		3 PCLK + 6 ADCLK	—	—	Cycle
		Group B is not to be stopped. (Activation by an A/D conversion source of group A.)			2 PCLK + 4 ADCLK	—	—	
	A/D conversion when self-diagnosis is enabled	A/D conversion for self-diagnosis is to be started.			2 PCLK + 6 ADCLK	4 PCLKB + 6 ADCLK	6 ADCLK	
	Other than above				2 PCLK + 4 ADCLK	4 PCLKB + 4 ADCLK	4 ADCLK	
Disconnection detection assistance processing time			t_{DIS}		The setting of ADNDIS[3:0] (initial value = 00h) × ADCLK*3			
Self-diagnosis conversion processing time*1	Sampling time		t_{DIAG}	t_{SPL}	The setting of ADSSTR0 (initial value = 0Dh) × ADCLK*4			
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	32 ADCLK (during high-speed conversion operation)			
					41 ADCLK (during low-current conversion operation)			
	Normal A/D conversion is to be started after completion of self-diagnosis conversion.			t_{DED}	2 ADCLK			
	A/D conversion for self-diagnosis is to be started after completion of conversion for continuous scan on the last channel specified.			t_{DSD}	2 ADCLK			
A/D conversion processing time*1	Sampling time		t_{CONV}	t_{SPL}	The setting of ADSSTRn (n = 0 to 7, L, T, O) (initial value = 0Dh) × ADCLK*4			
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	32 ADCLK (during high-speed conversion operation)			
					41 ADCLK (during low-current conversion operation)			
Scan end processing time*1			t_{ED}		1 PCLKB + 3 ADCLK*6			

Note 1. For t_D, t_{DIAG}, t_{CONV}, and t_{ED}, see Figure 44.22 and Figure 44.23.
Note 2. This is the maximum time required from software writing or trigger input to A/D conversion start.
Note 3. The value is fixed to 0Fh (15 ADCLK) when the temperature sensor output or internal reference voltage is A/D-converted.
Note 4. The required sampling time (ns) is specified according to the voltage conditions. See section 51.5, A/D Conversion Characteristics.
Note 5. This does not include the time consumed in the path from timer output to trigger input.
Note 6. 2 PCLK + 3 ADCLK when ADCLK is faster than PCLK (PCLK to ADCLK frequency ratio = 1:2 or 1:4).

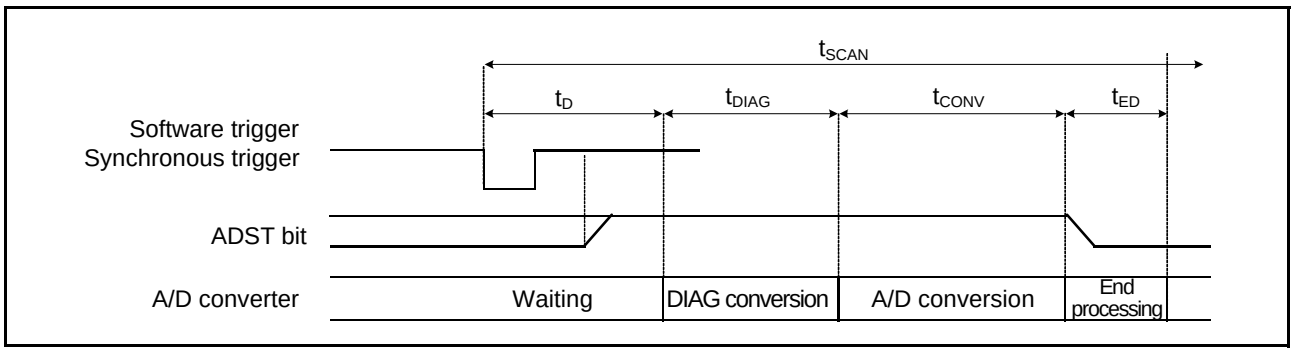


Figure 44.22 Scan Conversion Timing (Activated by Software or Synchronous Trigger)

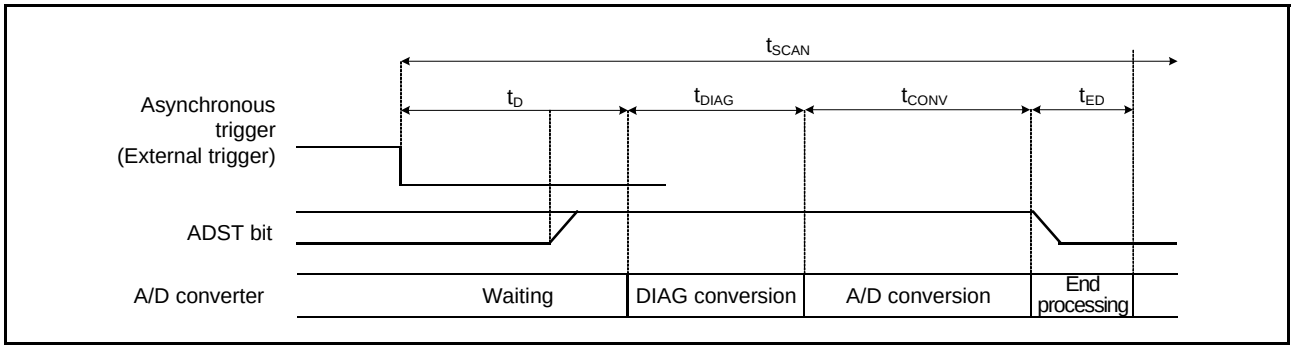


Figure 44.23 Scan Conversion Timing (Activated by Asynchronous Trigger)

44.3.7 Usage Example of A/D Data Register Automatic Clearing Function

Setting the ADCER.ACE bit to 1 automatically clears the A/D data registers (ADDRy, ADRD, ADTSDR, ADOCDR, ADDBLDR) to 0000h when the A/D data registers are read by the CPU, DTC, or DMACA.
The ring buffer (ADBUFn: n = 0 to 15) is not subject to auto-clearing.
This function enables detection of update failures of the A/D data registers (ADDRy, ADRD, ADTSDR, ADOCDR, ADDBLDR). The following describes the examples in which the function to automatically clear the ADDRy register is enabled and disabled.
In a case where the ADCER.ACE bit is 0 (automatic clearing disabled), if the A/D conversion result (0222h) is not written to the ADDRy register for some reason, the old data (0111h) will be the ADDRy value. Furthermore, if this ADDRy value is read into a general register using an A/D scan end interrupt, the old data (0111h) can be saved in the general register. When checking whether there is an update failure, it is necessary to frequently save the old data in the RAM or a general register.
In a case where the ADCER.ACE bit is 1 (automatic clearing enabled), when ADDRy = 0111h is read by the CPU, DTC, or DMACA, ADDRy is automatically cleared to 0000h. After that, if the A/D conversion result 0222h cannot be transferred to ADDRy for some reason, the cleared data (0000h) remains as the ADDRy value. If this ADDRy value is read into a general register using an A/D scan end interrupt at this point, 0000h will be saved in the general register. Occurrence of an ADDRy update failure can be determined by simply checking that the read data value is 0000h.

44.3.8 A/D-Converted Value Addition/Average Mode

In A/D-converted value addition mode, the same channel is A/D-converted 2, 3, 4, or 16 consecutive times and the sum of the converted values is stored in the data register. In A/D-converted value average mode, the same channel is A/D-converted two or four consecutive times and the mean of the converted values is stored in the data register. The use of the average of these results can improve the accuracy of A/D conversion, depending on the types of noise components that are present. This function, however, cannot always guarantee an improvement in A/D conversion accuracy.
The A/D-converted value addition or average mode can be specified when A/D conversion of the channel select analog input, temperature sensor output, or internal reference voltage is selected.

44.3.9 Disconnection Detection Assist Function

This converter incorporates the function to fix the charge for sampling capacitance to the specified state (reference voltage selected by the A/D high-potential/low-potential reference voltage control register) before start of A/D conversion. This function enables disconnection detection in wiring of analog inputs.
Figure 44.24 illustrates the A/D conversion operation when the disconnection detection assist function is used. Figure 44.25 shows an example of disconnection detection when precharge is selected. Figure 44.26 shows an example of disconnection detection when discharge is selected.

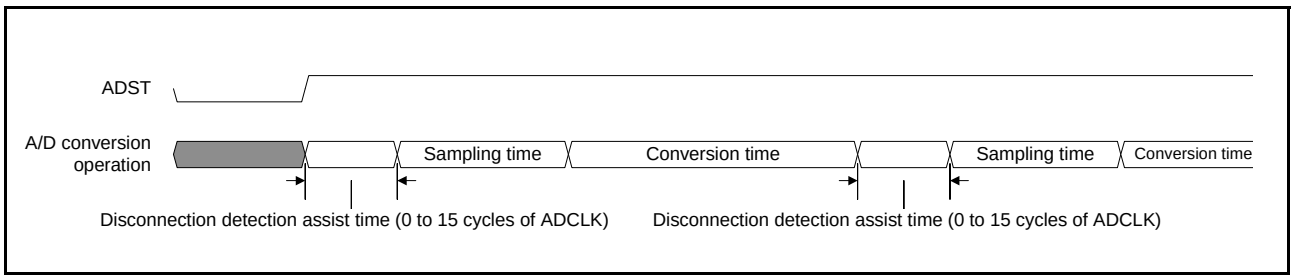
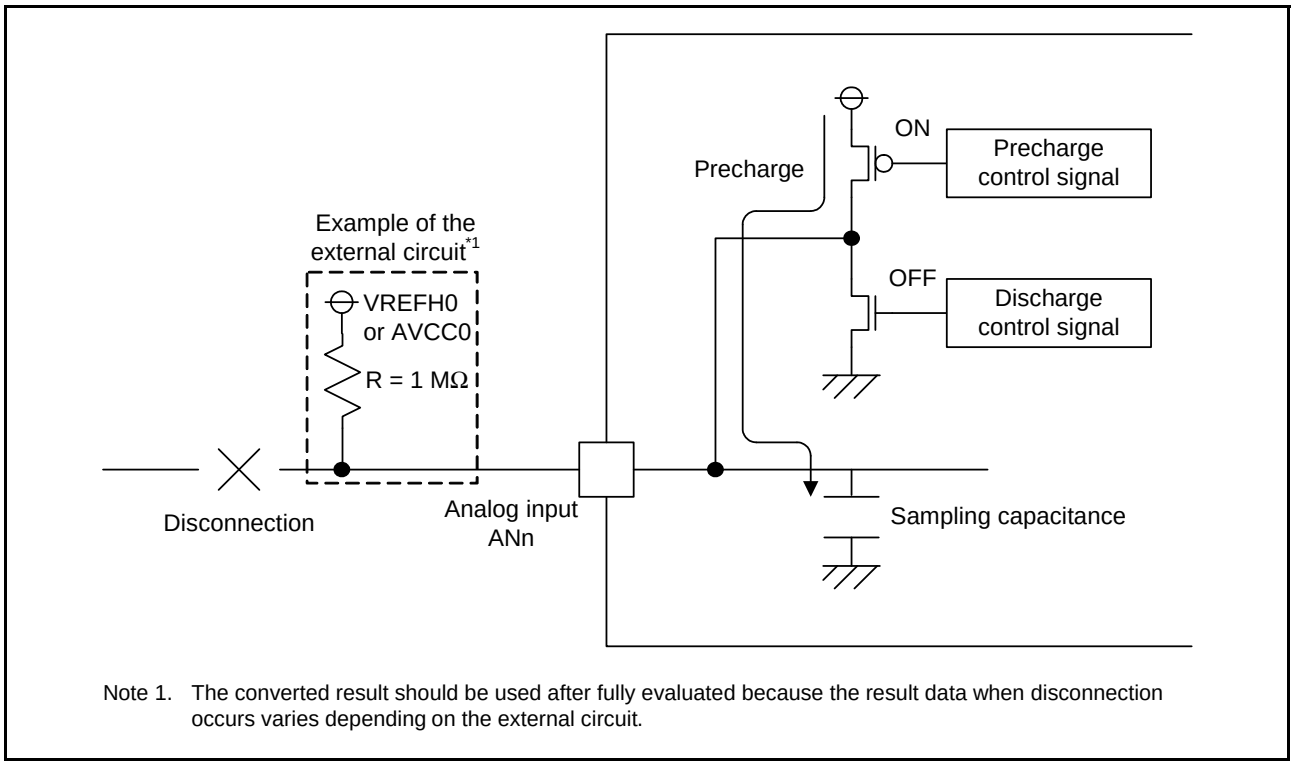
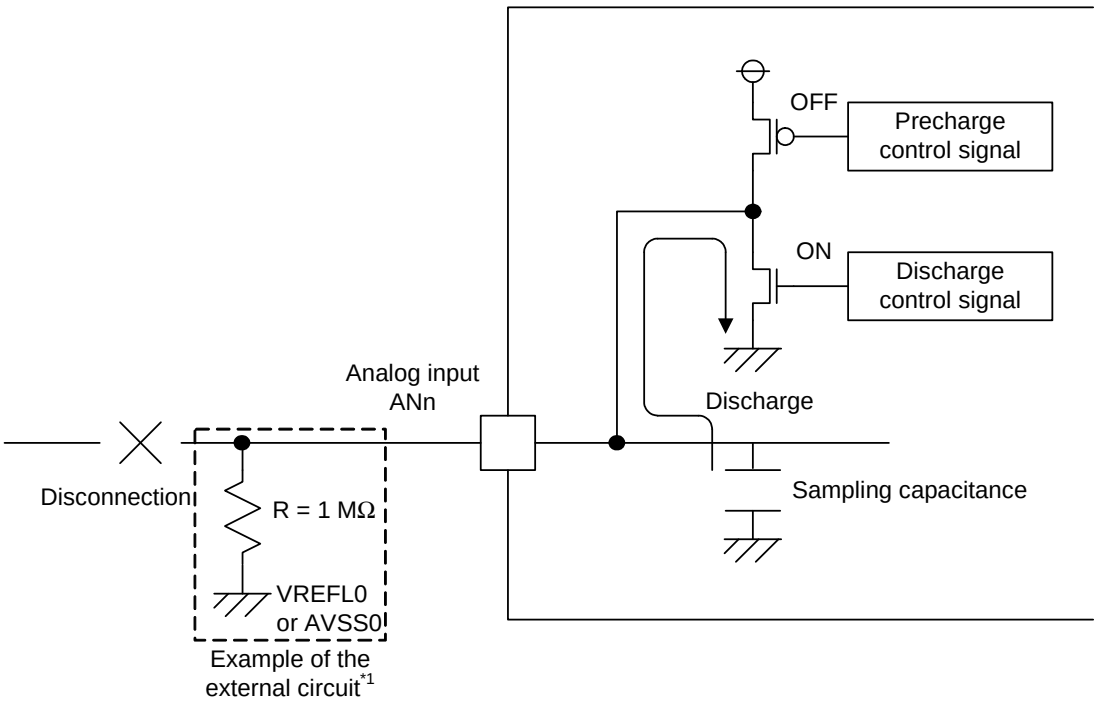


Figure 44.24 Operation of A/D Conversion When the Disconnection Detection Assist Function is Used



Note 1. The converted result should be used after fully evaluated because the result data when disconnection occurs varies depending on the external circuit.

Figure 44.25 Example of Disconnection Detection When Precharge is Selected



Note 1. The converted result should be used after fully evaluated because the result data when disconnection occurs varies depending on the external circuit.

Figure 44.26 Example of Disconnection Detection When Discharge is Selected

44.3.10 Starting A/D Conversion with Asynchronous Trigger

The A/D conversion can be started by the input of an asynchronous trigger. To start up the A/D converter by an asynchronous trigger, the A/D conversion start trigger select bits (ADSTRGR.TRSA[5:0]) should be set to 000000b, and a high-level signal should be input to the asynchronous trigger (ADTRG0# pin). Then, the ADCSR.TRGE and ADCSR.EXTRG bits should be set to 1. Figure 44.27 shows a timing of the asynchronous trigger input.
For the time from when the ADST bit is set to 1 until conversion starts, refer to section 44.8.3, A/D Conversion Restarting Timing and Termination Timing. An asynchronous trigger cannot be selected for group B used in group scan mode.

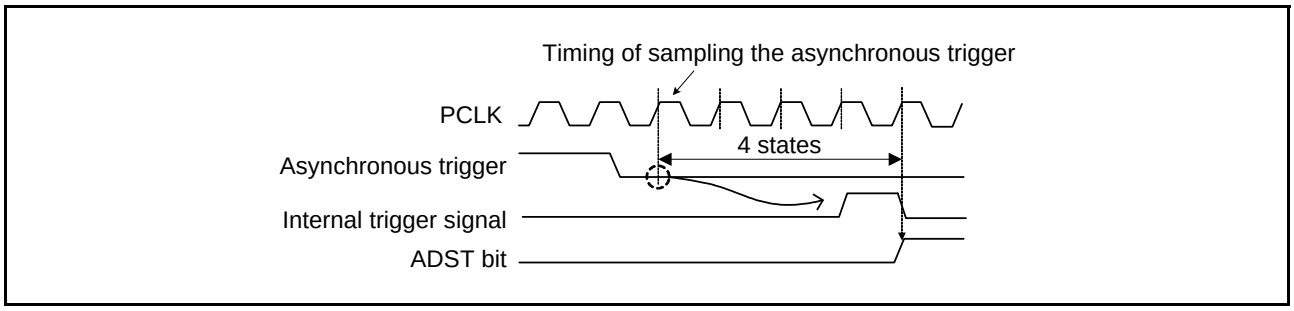


Figure 44.27 Timing of Sampling Asynchronous Trigger

44.3.11 Starting A/D Conversion with Synchronous Trigger from Peripheral Module

The A/D conversion can be started by a synchronous trigger. To start the A/D conversion by a synchronous trigger, the ADCSR.TRGE bit should be set to 1, the ADCSR.EXTRG bit should be cleared to 0, and the relevant sources should be selected by the ADSTRGR.TRSA[5:0] and ADSTRGR.TRSB[5:0] bits.

44.4 Interrupt Sources and DTC/DMAC Transfer Requests

44.4.1 Interrupt Requests

The 12-bit A/D converter can send scan end interrupt requests S12ADI0 and GBADI to the CPU.
Setting the ADCSR.ADIE bit to 1 and 0 enables and disables an S12ADI0 interrupt, respectively; similarly, setting the ADCSR.GBADIE bit to 1 and 0 enables and disables a GBADI interrupt, respectively.
In addition, the DTC or DMACA can be activated when an S12ADI0 or a GBADI interrupt is generated. Using an S12ADI0 or a GBADI interrupt to allow the DTC or DMACA to read the converted data enables continuous conversion without burden on software.
For details on DTC settings, see section 19, Data Transfer Controller (DTCa), and for details on DMACA settings, see section 18, DMA Controller (DMACA).

44.5 Event Link Function

44.5.1 Event Output to the ELC

The ELC uses the S12ADI0 interrupt request signal as an event signal (S12ADELC), enabling link operation for the preset module. An event signal is generated under the conditions set by the event link control bits (ADELCCR.ELCC[1:0] bits).
The event signal can be output regardless of the setting of the corresponding interrupt request enable bit.
The 12-bit A/D converter outputs the A/D conversion end event (S12ADELC), window function compare match event (S12ADWMELC), and mismatch event (S12ADWUMELC).
The scan end event (S12ADELC) is output to the ELC at the same time as the interrupt output (S12ADI0) regardless of the ADCSR.ADIE setting.
The compare match/mismatch event (S12ADWMELC/S12ADWUMELC) is output to the ELC with a delay of one PCLK cycle from the interrupt output (S12ADI0) regardless of the ADCSR.ADIE setting.
When using compare match/mismatch events (S12ADWMELC/S12ADWUMELC) to the ELC, specify single scan mode.

44.5.2 12-Bit A/D Converter Operation by Event from the ELC

The 12-bit A/D converter can be started by the predetermined event by setting ELSRn of the ELC.

44.5.3 Note on 12-Bit A/D Converter When an Event Is Input from the ELC

If an event occurs during A/D conversion, the event is disabled.

44.6 Selecting Reference Voltage

For the A/D converter, the high-potential reference voltage can be selected from VREFH0 and AVCC0, and the low-potential reference voltage can be selected from VREFL0 and AVSS0, respectively. Set these before starting A/D conversion. For details of this setting, see section 44.2.30, A/D High-Potential/Low-Potential Reference Voltage Control Register (ADHVREFCNT).

44.7 Allowable Impedance of Signal Source

To achieve high-speed conversion of 0.83 µs, the analog input pins of this MCU are designed so that the conversion accuracy is guaranteed if the impedance of the input signal source is 0.5 kΩ or less. If an external capacitor of large capacitance is attached in the application in which only a single pin input is converted in single scan mode, the only load on input is virtually 2.6 kΩ of the internal input resistor; therefore, the impedance of the signal source can be ignored. Being a low-pass filter, however, an analog input circuit may not follow the analog signal with a large differential coefficient. When high-speed analog signals are to be converted or multiple pins are to be converted in scan mode, a low-impedance buffer should be used.

Figure 44.28 shows an equivalent circuit of an analog input pin and an external sensor.

To perform A/D conversion accurately, charging of the internal capacitor C shown in Figure 44.28 must be completed within the specified period of time. This specified period is referred to as sampling time.

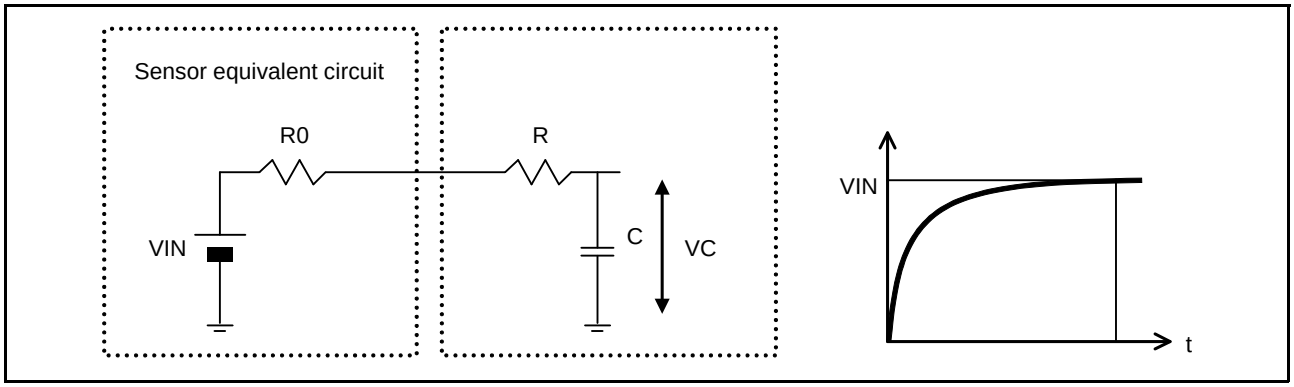


Figure 44.28 Equivalent Circuit of Analog Input Pin and External Sensor

44.8 Usage Notes

44.8.1 Notes on Reading Data Registers

Read the A/D data registers, A/D data duplication register, A/D data duplication register A, A/D data duplication register B, A/D temperature sensor data register, A/D internal reference voltage data register, and A/D self-diagnosis data register in word units. If a register is read twice in byte units, that is, the higher-order byte and lower-order byte are separately read, the A/D-converted value having been read first may disagree with the A/D-converted value having been read for the second time. To prevent this, the data registers should never be read in byte units.

44.8.2 Notes on Stopping A/D Conversion

To stop A/D conversion when an asynchronous trigger or a synchronous trigger has been selected as the condition for starting A/D conversion, follow the procedure in Figure 44.29.

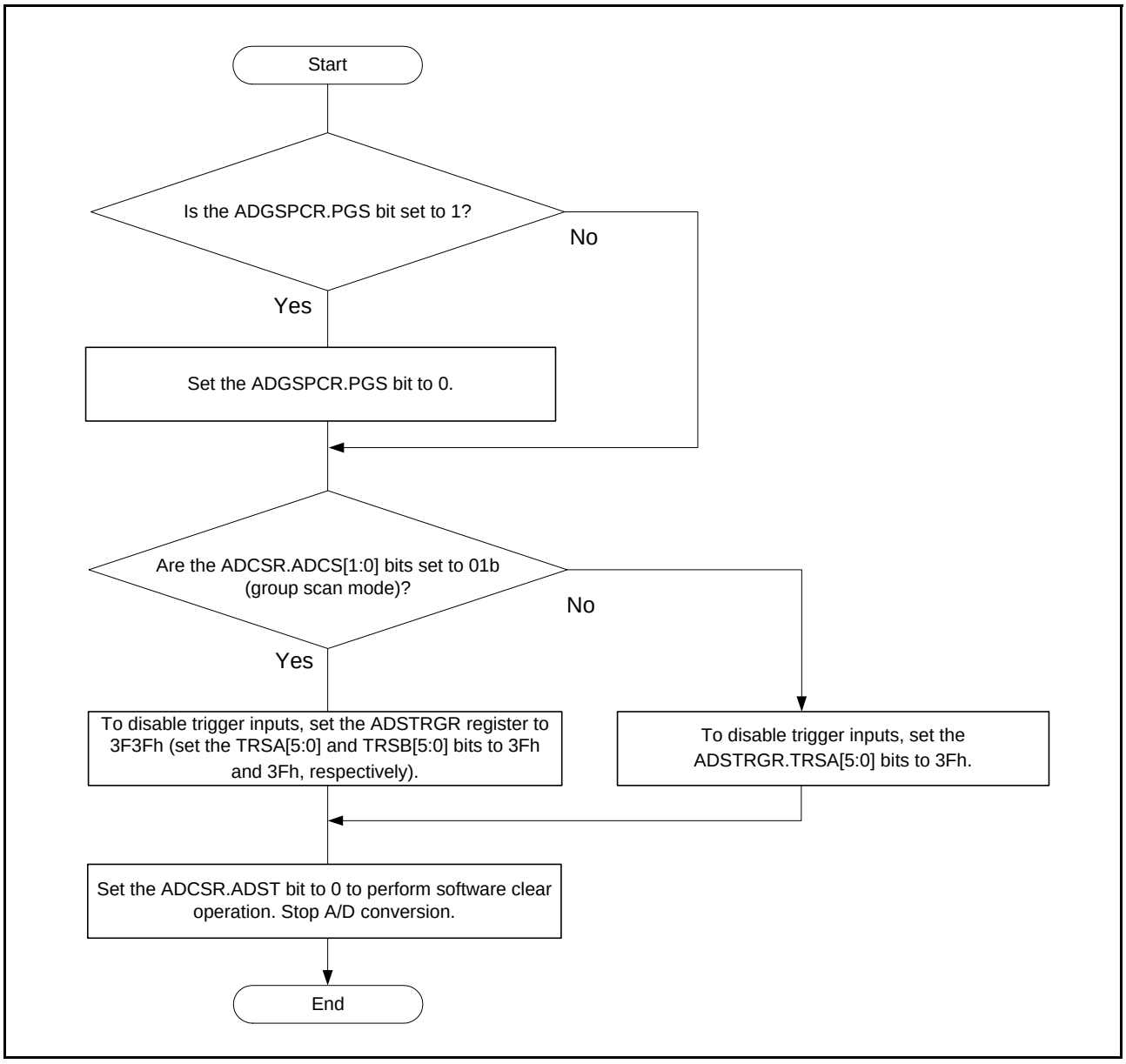


Figure 44.29 Procedure for Clear Operation by Software through the ADCSR.ADST Bit

44.8.3 A/D Conversion Restarting Timing and Termination Timing

It takes a maximum of six ADCLK cycles for the idle analog unit of the 12-bit A/D converter to be restarted by setting the ADCSR.ADST bit to 1. It takes a maximum of three ADCLK cycles for the operating analog unit of the 12-bit A/D converter to be terminated by setting the ADCSR.ADST bit to 0.

44.8.4 Notes on Scan End Interrupt Handling

When scanning the same analog input twice using any trigger, the first A/D-converted data is overwritten with the second A/D-converted data in the case that the CPU does not complete reading the A/D-converted data by the time the A/D conversion of the first analog input for the second scan ends after the first scan end interrupt is generated.

44.8.5 Module Stop Function Setting

Operation of the 12-bit A/D converter can be disabled or enabled by setting module stop control register A (MSTPCRA). The initial setting is for operation of the 12-bit A/D converter to be halted. Register access is enabled by releasing the module stop state.
After the module stop state is released, wait for 1 µs to start A/D conversion. For details, refer to section 11, Low Power Consumption.

44.8.6 Notes on Entering Low Power Consumption States

Before entering the module stop state or software standby mode, make sure to stop A/D conversion. Here, set the ADCSR.ADST bit to 0, and secure certain period of time until the analog unit of the 12-bit A/D converter is stopped. Follow the procedure given below to secure this time.
Follow the procedure for clear operation by software through the ADCSR.ADST bit, shown in Figure 44.29. After that, wait for two clock cycles of ADCLK before entering the peripheral module stop state or software standby mode.

44.8.7 Notes on Canceling Software Standby Mode

After software standby mode is canceled, wait until the crystal oscillation stabilization time or the PLL circuit stabilization time elapses, and then wait for 1 µs before starting A/D conversion. For details, refer to section 11, Low Power Consumption.

44.8.8 Pin Setting when the 12-bit A/D Converter is Used

When the 12-bit A/D converter is used, do not set any pin of port 4 as output.
Output from any of the pins may affect on A/D conversion accuracy because analog power supply is used in the part of the port 4 circuit.

44.8.9 Error in Absolute Accuracy When Disconnection Detection Assistance is in Use

Using disconnection detection assistance leads to an error in absolute accuracy of the A/D converter. This is because an error voltage is input to the analog input pins due to the resistive voltage division between the pull-up or pull-down resistor (Rp) and the resistance of the signal source (Rs). This error in absolute accuracy is calculated from the following formula. Only use disconnection detection assistance after thorough evaluation.

Maximum error in absolute accuracy (LSB) = 4095 × Rs / Rp

44.8.10 ADHSC Bit Rewriting Procedure

Before rewriting the A/D conversion select bit (ADCSR.ADHSC) from 0 to 1 or from 1 to 0, the 12-bit A/D converter must be in the standby state. Carry out steps 1 to 3 below to modify the ADCSR.ADHSC bit. After the sleep bit (ADHVREFCNT.ADSLP) is cleared to 0, wait for at least 1 µs and then start A/D conversion.

ADHSC Bit Rewriting Procedure:

1. Set the sleep bit (ADHVREFCNT.ADSLP) to 1.
2. Wait for at least 0.2 µs, and then modify the A/D conversion select bit (ADCSR.ADHSC).
3. Wait for at least 4.8 µs, and then clear the sleep bit (ADHVREFCNT.ADSLP) to 0.

Note: It is prohibited to set the ADHVREFCNT.ADSLP bit to 1 except for modifying the A/D conversion select bit (ADCSR.ADHSC).

44.8.11 Voltage Range of Analog Power Supply Pins

If this MCU is used with the voltages outside the following ranges, the reliability of the MCU may be affected.

- Analog input voltage range
  Voltage applied to analog input pins ANn: AVSS0 ≤ VAN ≤ AVCC0
  Reference voltage range applied to pins VREFH0 and VREFL0: VREFH0 ≤ AVCC0, VREFL0 = AVSS0
  Conversion will not succeed if the voltage applied to analog input pins ANn is greater than VREFH0 (see Figure 44.30).

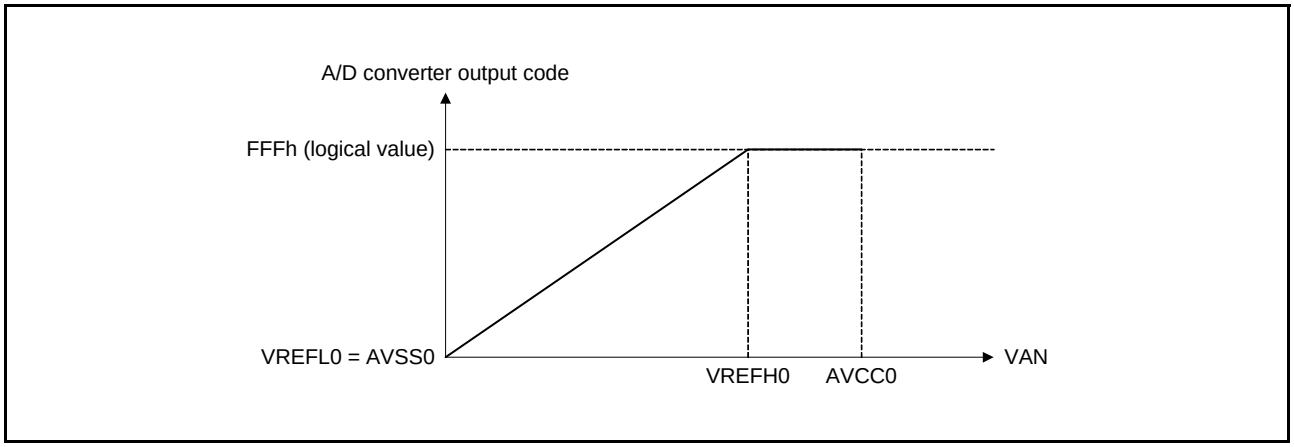


Figure 44.30 Relationship Between Voltage Applied to Analog Input Pins and Output Code

- Relationship between power supply pin pairs (AVCC0–AVSS0, VREFH0–VREFL0, VCC–VSS)
  The following condition should be satisfied: AVSS0 = VSS. When performing A/D conversion of analog input pin ANn (n = 016 to 020, 027), the following condition should be satisfied: AVCC0 = VCC. A 0.1-µF capacitor should be connected between each pair of power supply pins to create a closed loop with the shortest route possible as shown in Figure 44.31, and connection should be made so that the following conditions are satisfied at the supply side.
  VREFL0 = AVSS0 = VSS
  When the 12-bit A/D converter is not used, the following conditions should be satisfied.
  VREFH0 = AVCC0 = VCC and VREFL0 = AVSS0 = VSS

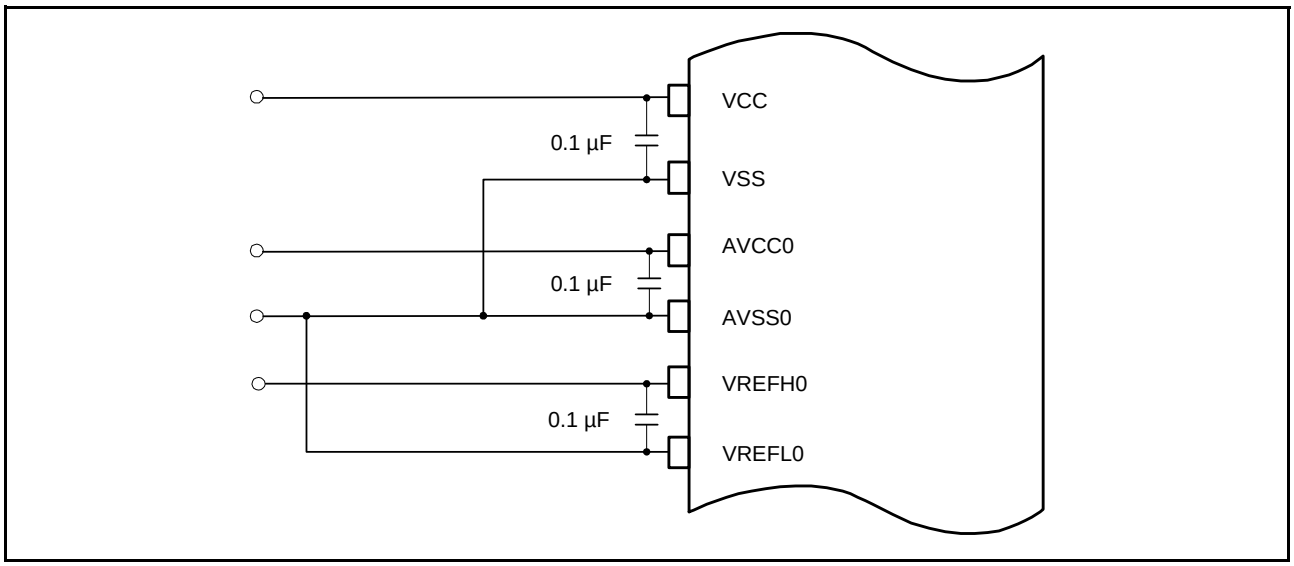


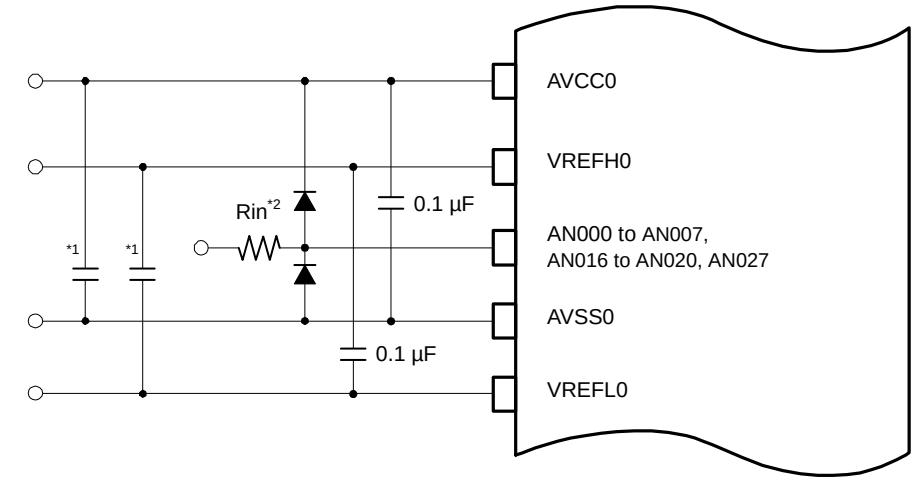
Figure 44.31 Power Supply Pin Connection Example

44.8.12 Notes on Board Design

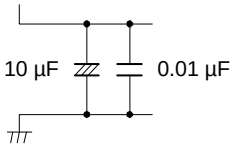
The board should be designed so that digital circuits and analog circuits are separated from each other as far as possible. In addition, digital circuit signal lines and analog circuit signal lines should not intersect or placed near each other. If these rules are not followed, noise will be produced on analog signals and A/D conversion accuracy will be affected. The analog input pins (AN000 to AN007, AN016 to AN020, AN027), reference power supply pin (VREFH0), reference ground pin (VREFL0), and analog power supply (AVCC0) should be separated from digital circuits using the analog ground (AVSS0). The analog ground (AVSS0) should be connected to a stable digital ground (VSS) on the board (single-point ground plane connection).

44.8.13 Notes on Noise Prevention

To prevent the analog input pins (AN000 to AN007, AN016 to AN020, AN027) from being destroyed by abnormal voltage such as excessive surge, a capacitor should be inserted between AVCC0 and AVSS0 and between VREFH0 and VREFL0, and a protection circuit should be connected to protect the analog input pins (AN000 to AN007, AN016 to AN020, AN027) as shown Figure 44.32.



Note 1. The values shown here are reference values.



Note 2. Rin: Signal source impedance

Figure 44.32 Sample Protection Circuit for Analog Inputs

45. 12-Bit D/A Converter (R12DAA)

45.1 Overview

This MCU includes two channels of 12-bit D/A converter.
Table 45.1 lists the specifications of the 12-bit D/A converter and Figure 45.1 shows a block diagram of the 12-bit D/A converter.

Table 45.1 Specifications of 12-Bit D/A Converter

Item	Specifications
Resolution	12 bits
Output channels	Two channels
Measure against mutual interference between analog modules	Measure against interference between D/A and A/D conversion D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal from the 12-bit A/D converter. Therefore, the degradation of A/D conversion accuracy due to interference is reduced by controlling the timing in which the 12-bit D/A converter inrush current occurs, with the enable signal.
Low power consumption function	Module stop state can be set.
Event link function (input)	DA0 conversion can be started when an event signal is input.

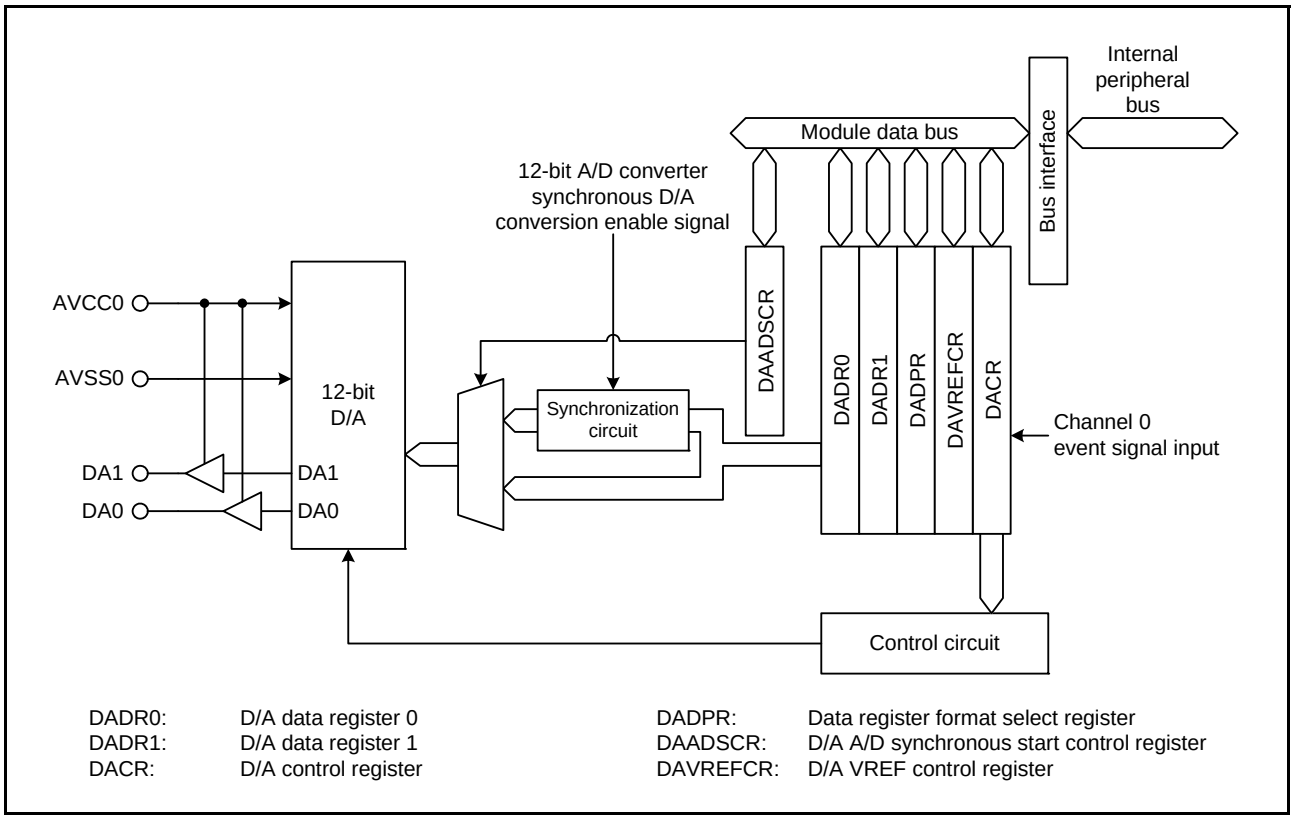


Figure 45.1 Block Diagram of 12-Bit D/A Converter

Table 45.2 lists the pin configuration of the 12-bit D/A converter.

Table 45.2 Pin Configuration of 12-Bit D/A Converter

Pin Name	I/O	Function
AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter and 12-bit D/A converter. Connect this pin to VCC when not using the 12-bit A/D converter and 12-bit D/A converter.
AVSS0	Input	Analog ground pin for the 12-bit A/D converter and 12-bit D/A converter. Connect this pin to VSS when not using the 12-bit A/D converter and 12-bit D/A converter.
DA0	Output	Channel 0 analog output pin
DA1	Output	Channel 1 analog output pin

45.2 Register Descriptions

45.2.1 D/A Data Register m (DADRm) (m = 0, 1)

Address(es): DA.DADR0 0008 8040h, DA.DADR1 0008 8042h

• DADPR.DPSEL bit = 0 (data is right-justified)

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—												
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

• DADPR.DPSEL bit = 1 (data is left-justified)

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
													—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The DADRm register is a 16-bit readable/writable register, which stores data to which D/A conversion is to be performed. Whenever an analog output is enabled, the values in DADRm are converted and output from the D/A converter.

12-bit data can be relocated by setting the DADPR.DPSEL bit.

Bits “—” are read as 0. The write value should be 0.

45.2.2 D/A Control Register (DACR)

Address(es): DA.DACR 0008 8044h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAOE1	DAOE0	—	—	—	—	—	—
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Bit Name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R
b6	DAOE0	D/A Output Enable 0	0: Analog output of channel 0 (DA0) is disabled. 1: D/A conversion of channel 0 is enabled. Analog output of channel 0 (DA0) is enabled.	R/W
b7	DAOE1	D/A Output Enable 1	0: Analog output of channel 1 (DA1) is disabled. 1: D/A conversion of channel 1 is enabled. Analog output of channel 1 (DA1) is enabled.	R/W

This register should be set when the DAADSCR.DAADST bit is 1 (measure against interference between D/A and A/D conversion is enabled) while the 12-bit A/D converter is halted (the ADCSR.ADST bit is 0). At that time, the software trigger should be selected for the 12-bit A/D converter trigger to securely stop the 12-bit A/D converter.

DAOE0 Bit (D/A Output Enable 0)

The DAOE0 bit controls the D/A conversion and analog output.

The event link function can be used to set the DAOE0 bit to 1. The DAOE0 bit becomes 1 when the event specified by setting the ELSR16 register of the ELC occurs, and output of the D/A conversion results starts.

DAOE1 Bit (D/A Output Enable 1)

The DAOE1 bit controls the D/A conversion and analog output.

45.2.3 Data Register Format Select Register (DADPR)

Address(es): DA.DADPR 0008 8045h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSEL	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DPSEL	Format Select	0: Data is right-justified. 1: Data is left-justified.	R/W

45.2.4 D/A A/D Synchronous Start Control Register (DAADSCR)

Address(es): DA.DAADSCR 0008 8046h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAADST	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DAADST	D/A A/D Synchronous Conversion	0: 12-bit D/A converter operation does not synchronize with 12-bit A/D converter operation. (measure against interference between D/A and A/D conversion is disabled) 1: 12-bit D/A converter operation synchronizes with 12-bit A/D converter operation. (measure against interference between D/A and A/D conversion is enabled)	R/W

As a measure against interference between D/A and A/D conversion, the DAADSCR register selects whether or not the timing for starting 12-bit D/A conversion is synchronized with the 12-bit A/D converter synchronous D/A conversion enable signal from the 12-bit A/D converter.
This register should be set while the 12-bit A/D converter is halted (while the ADCSR.ADST bit is 0 after selecting software trigger as the 12-bit A/D converter trigger).

DAADST Bit (D/A A/D Synchronous Conversion)

Setting the DAADST bit to 0 allows the DADRm register value (m = 0, 1) to be converted into analog data at any time.
Setting the DAADST bit to 1 allows synchronous D/A conversion with the 12-bit A/D converter synchronous D/A conversion enable signal from the 12-bit A/D converter. Therefore, even if the DADRm register value is modified, D/A conversion does not start until the 12-bit A/D converter completes A/D conversion.
Set this bit while the ADCSR.ADST bit is set to 0. At this time, the software trigger should be selected for the 12-bit A/D converter trigger to securely stop the 12-bit A/D converter.
The event link function cannot be used when the DAADST bit is set to 1. Stop the event link function by setting the ELSR16 register of the ELC. The setting of the DAADST bit is common to channels 0 and 1 of the 12-bit D/A converter.

45.2.5 D/A VREF Control Register (DAVREFCR)

Address(es): DA.DAVREFCR 0008 8047h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	REF[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	REF[2:0]	D/A Reference Voltage Select	b2 b0 0 0 0: Not selected 0 0 1: AVCC0/AVSS0 0 1 1: Internal reference voltage/AVSS0 Settings other than above are prohibited.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The DAVREFCR register selects the reference voltage of the 12-bit D/A converter.

REF[2:0] Bits (D/A Reference Voltage Select)

The REF[2:0] bits select the reference voltage of the 12-bit D/A converter 0 and 1. When changing the value of these bits, write 000b to the DAVREFCR.REF[2:0] bits in advance. Read the REF[2:0] bits after changing their value, and confirm that it has been changed. When selecting the internal reference voltage, set the DADR0 and DADR1 registers to 0000h and discharge the VREF path before switching the voltage. As the path remains discharged after the reset is released, the internal reference voltage can be selected. For details on discharging, refer to section 45.3.2, Notes on Using the Internal Reference Voltage as the Reference Voltage. Do not rewrite this register during A/D conversion using the 12-bit A/D converter. If this register is rewritten, the accuracy of A/D conversion is not guaranteed.
When the internal reference voltage is selected, the voltage generation circuit operates and current increases by about 75 µA. This circuit is not automatically turned off even if the MCU enters software standby mode with the internal reference voltage selected.

45.3 Operation

The 12-bit D/A converter includes D/A conversion circuits for two channels, each of which can operate independently. When the DACR.DAOEm bit (m = 0, 1) is set to 1, D/A converter is enabled and the conversion result is output. An operation example of D/A conversion on channel 0 is shown below. Figure 45.2 shows the timing of this operation.

(1) Set the data for D/A conversion in the DADPR.DPSEL bit and the DADR0 register.

(2) Set the DACR.DAOE0 bit to 1 to start D/A conversion. The DA0 output settles to the voltage corresponding to the setting value after the conversion time tDCONV has elapsed. The DA0 output voltage is held at this level until the DADR0 register is updated or the DAOE0 bit is set to 0. The output voltage (reference) is expressed by the following formula:

$$\frac{\text{Value of DADRm register}}{4096} \times \text{Reference voltage}$$

Because the D/A converter output is buffered with an amplifier, the output voltage does not reach AVSS0 or AVCC0. Refer to section 51, Electrical Characteristics for the output voltage range.

(3) When the DADR0 register is updated, the conversion starts. The DA0 output settles at the new output voltage after the conversion time tDCONV has elapsed.
When the DAADSCR.DAADST bit is 1 (measure against interference between D/A and A/D conversion is enabled), it takes a maximum of one A/D conversion time for D/A conversion to start. When ADCLK is faster than the peripheral module clock, it may take longer than one A/D conversion time.

(4) When the DAOE0 bit is set to 0, analog output is disabled.

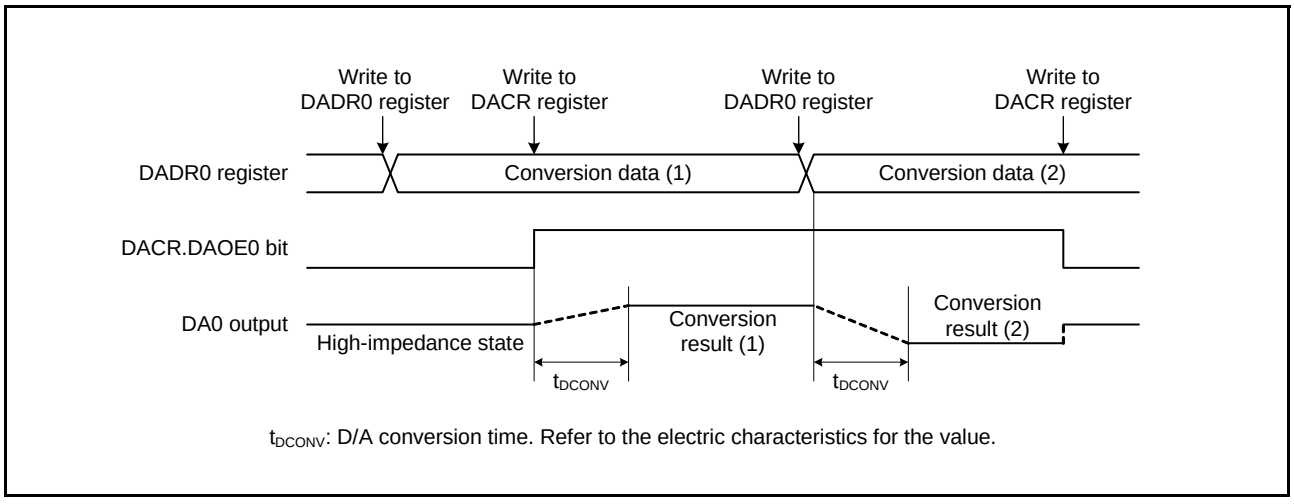


Figure 45.2 Example of 12-Bit D/A Converter Operation

45.3.1 Measure against Interference between D/A and A/D Conversion

When D/A conversion starts, an inrush current occurs to the 12-bit D/A converter. Since the same analog power supply is shared by the 12-bit D/A converter and 12-bit A/D converter, the inrush current may interfere with the proper operation of the 12-bit A/D converter.

With the DAADSCR.DAADST bit being 1, even if the DADRm register data (m = 0, 1) is modified during 12-bit A/D converter operation, D/A conversion does not start immediately but starts synchronously with A/D conversion completion. It takes a maximum of one A/D conversion time for the DADRm register data update to be reflected as the D/A conversion circuit input. Before reflection, the DADRm register value does not correspond to the analog output value.

When this function is enabled, it is impossible to check by any software means whether the DADRm register value has been D/A converted or not.

Even with the DAADSCR.DAADST bit being 1, when the DADRm register data is modified while the 12-bit A/D converter is halted, D/A conversion starts in one PCLKB cycle.

Figure 45.3 shows an example of channel 0 D/A conversion, in which the 12-bit D/A converter operates synchronously with the 12-bit A/D converter.

(1) Confirm that the 12-bit A/D converter is halted. Set the DAADSCR.DAADST bit to 1.
(2) Confirm that the 12-bit A/D converter is halted. Set the DACR.DAOE0 bit to 1.
(3) Set the DADR0 register. When ADCLK is faster than the peripheral module clock, it may take longer than one A/D conversion time.

- If the 12-bit A/D conversion is halted (ADCSR.ADST bit = 0) when the DADR0 register is modified, D/A conversion starts in one PCLKB cycle.
- If the 12-bit A/D conversion is in progress (ADCSR.ADST bit = 1) when the DADR0 register is modified, D/A conversion starts upon A/D conversion completion. If the DADR0 register is modified twice during A/D conversion, the first update may not be converted.

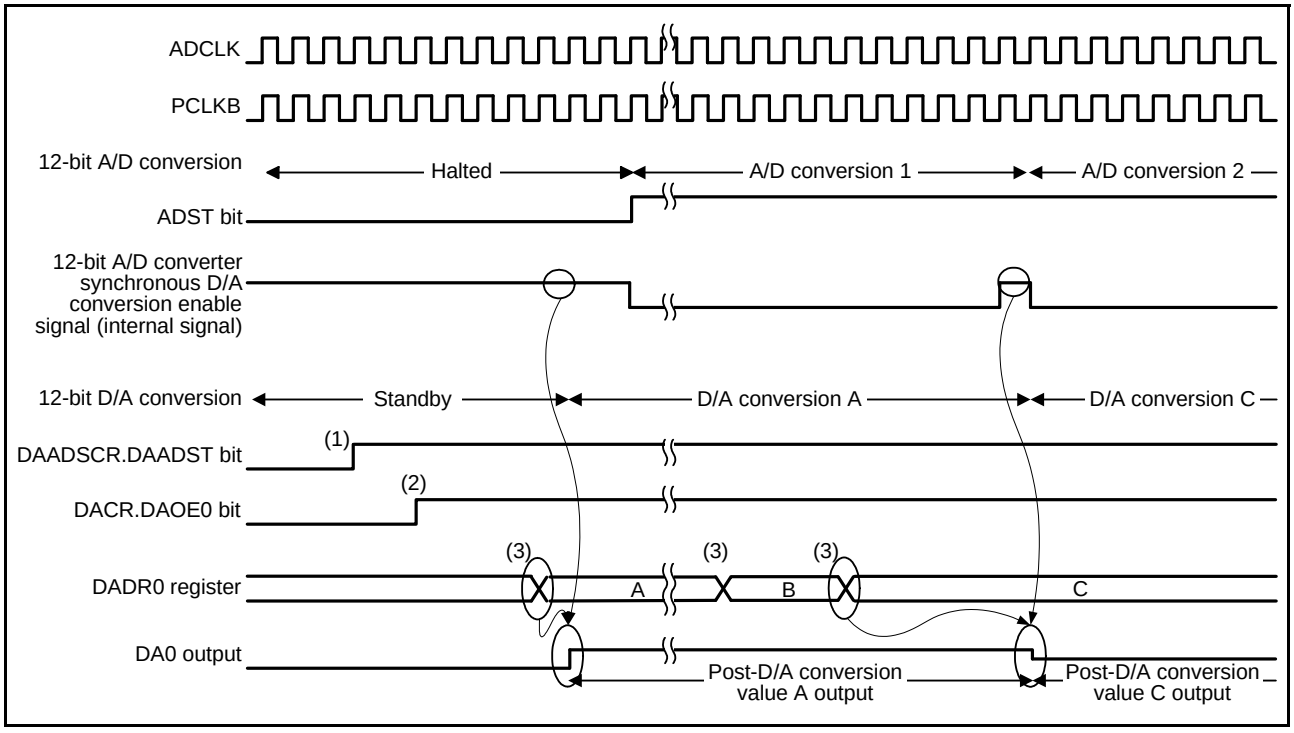


Figure 45.3 Example of Conversion When the 12-Bit D/A Converter is Synchronized with the 12-Bit A/D Converter

When ADCLK is faster than PCLKB, the 12-bit D/A converter may not be able to capture a 12-bit A/D converter synchronous D/A conversion enable signal for one ADCLK cycle which is output between A/D conversion 1 and A/D conversion 2. Figure 45.4 shows example when the 12-bit D/A converter cannot capture the 12-bit A/D converter synchronous D/A conversion enable signal. In this case, the DA0 output is held at the level of the post-D/A conversion value A.

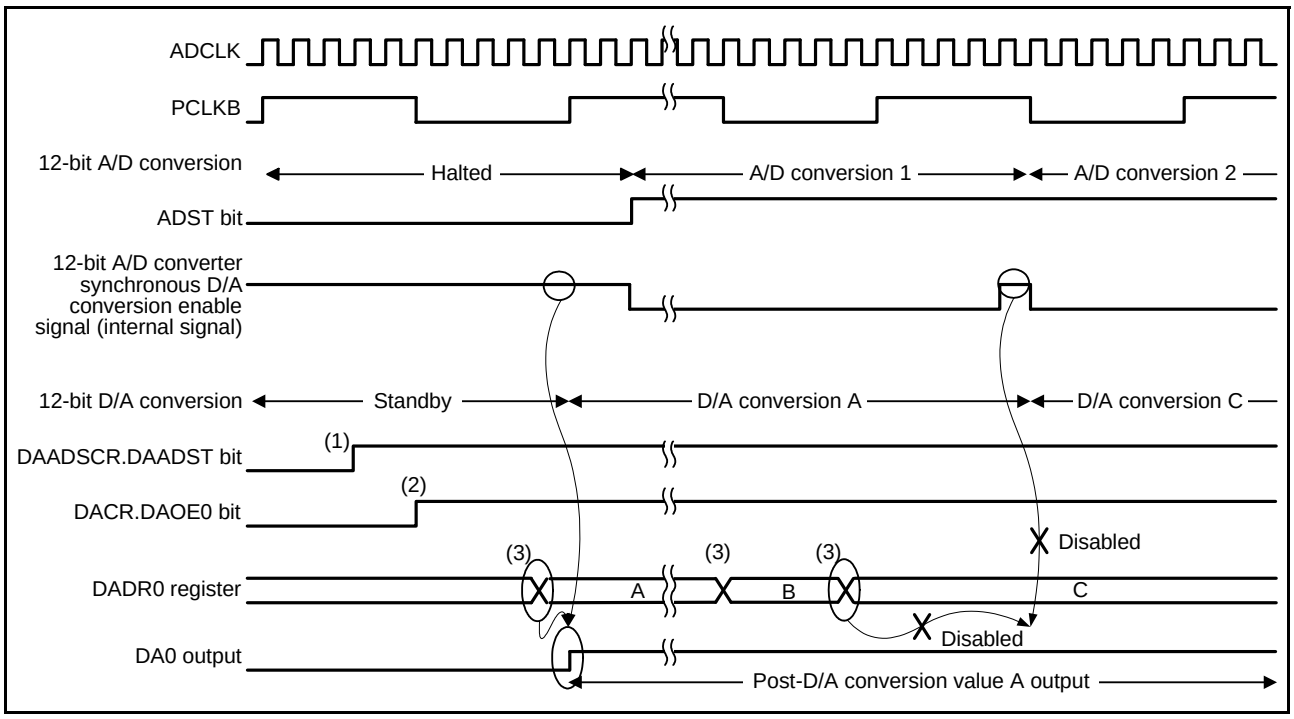


Figure 45.4 Example When the 12-Bit D/A Converter Cannot Capture the 12-Bit A/D Converter Synchronous D/A Conversion Enable Signal

45.3.2 Notes on Using the Internal Reference Voltage as the Reference Voltage

When setting the DAVREFCR.REF[2:0] bits to 011b to use the internal reference voltage/AVSS0 as the reference voltage, the VREF path needs to be discharged before selecting the voltage. The following shows the discharging procedure.

(1) Write 000b to the REF[2:0] bits.
(2) Set the DADR0 register to 0000h and the DADR1 register to 0000h.
(3) Keep the state of step (2) for 10 µs (discharging).
(4) After discharging is completed, write 011b to the REF[2:0] bits and select the internal reference voltage/AVSS0.
(5) Set the DACR.DAOEm bit to 1 (m = 0, 1) and wait for the stabilization wait time (5 µs) of the internal reference voltage.
(6) Write data to the DADRm register and start D/A conversion.

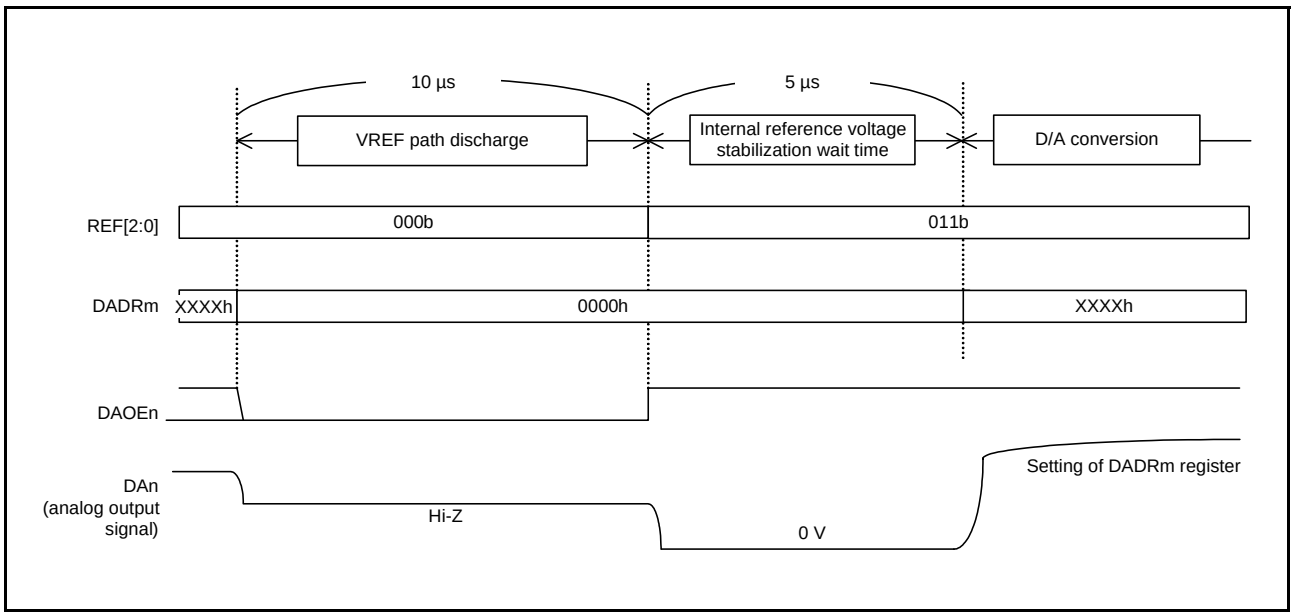


Figure 45.5 Procedure for Selecting the Internal Reference Voltage as the Reference Voltage

45.4 Event Link Operation Setting Procedure

The event link operation procedure is described below.

(1) Set the DADPR.DPSEL bit and set the data for D/A conversion in the DADR0 register.
(2) Set the bit value of the ELSR16 setting event signal to link the ELSR16 register of the ELC.
(3) Set the ELCR.ELCON bit to 1. This procedure enables event link operation for all modules with the event link function selected.
(4) Set the event output source module to activate the event link. After the event is output from the module, the DACR.DAOE0 bit becomes 1, and D/A conversion on channel 0 starts.
(5) Set the ELSR16.ELS[7:0] bits to 0000 0000b to stop event link operation of 12-bit D/A converter channel 0. All event link operation is stopped when the ELCR.ELCON bit is set to 0.

45.5 Usage Notes on Event Link Operation

(1) When the event specified by the ELSR16 register is generated while the write cycle is performed to the DACR.DAOE0 bit, the write cycle is stopped, and the setting to 1 by the generated event takes precedence.
(2) Use of the event link function is prohibited when the DAADSCR.DAADST bit is set to 1 as the measure against an interfere between D/A and A/D conversions.

45.6 Usage Notes

45.6.1 Module Stop Function Setting

Operation of the 12-bit D/A converter can be disabled or enabled using the module stop control register. The initial setting is for operation of the 12-bit D/A converter to be stopped. Register access is enabled by releasing the module stop state. For details, refer to section 11, Low Power Consumption.

45.6.2 Operation of the D/A Converter in Module Stop State

When the MCU enters the module stop state with D/A conversion enabled, the D/A converter outputs are retained, and the analog power supply current is the same as during D/A conversion. If the analog power supply current has to be reduced in the module stop state, disable D/A conversion by setting the DACR.DAOE1, and DAOE0 bits to 0.

45.6.3 Operation of the D/A Converter in Software Standby Mode

When the MCU enters software standby mode with D/A conversion enabled, the D/A converter outputs are retained, and the analog power supply current is the same as during D/A conversion. If the analog power supply current has to be reduced in software standby mode, disable D/A conversion by setting the DACR.DAOE1, and DAOE0 bits to 0.

45.6.4 Note on Usage When Measure against Interference between D/A and A/D Conversion is Enabled

When the DAADSCR.DAADST bit is 1 (measure against interference between D/A and A/D conversion is enabled), do not place the 12-bit A/D converter in the module stop state. It may halt D/A conversion in addition to A/D conversion.

46. Temperature Sensor (TEMPSA)

46.1 Overview

This MCU includes a temperature sensor. The temperature sensor outputs a voltage which varies with the temperature. The user can obtain the temperature surrounding the MCU using the 12-bit A/D converter to convert the voltage output from the temperature sensor into a digital value.

Table 46.1 lists the specifications of the temperature sensor. Figure 46.1 shows a overall block diagram of the temperature sensor system.

Table 46.1 Temperature Sensor Specifications

Item	Description
Temperature sensor voltage output	The temperature sensor voltage is output to the 12-bit A/D converter.

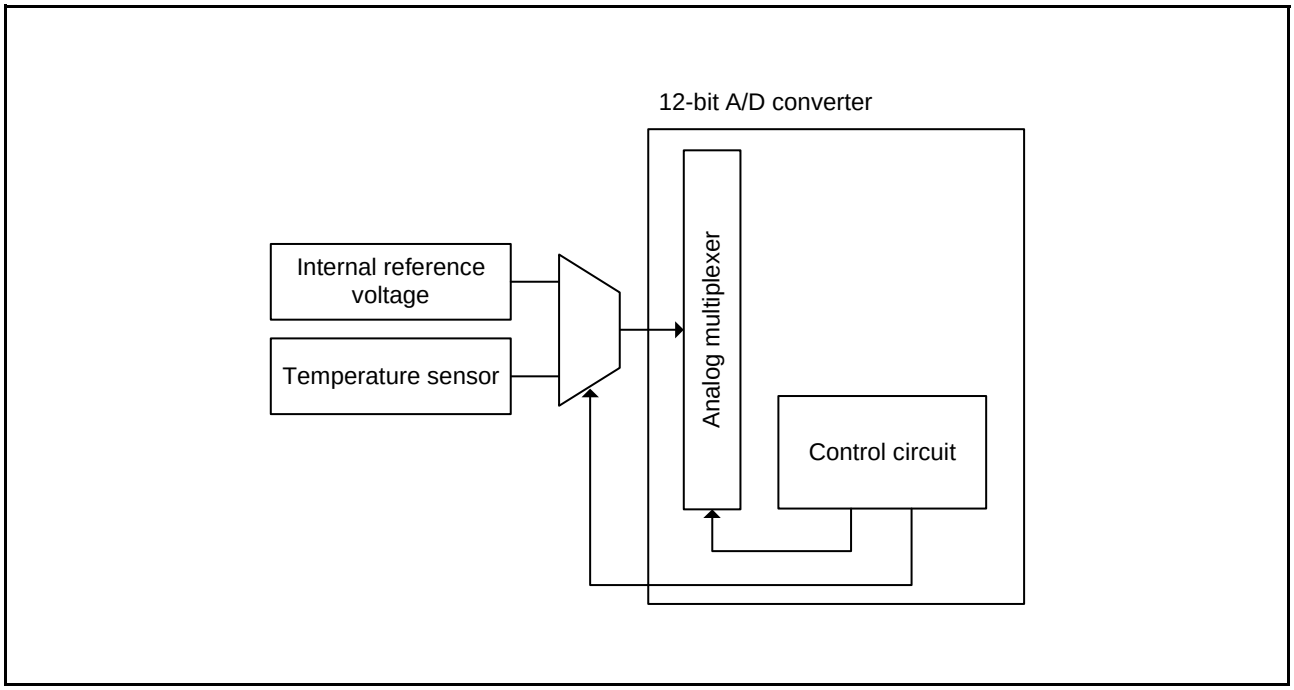


Figure 46.1 Block Diagram of Temperature Sensor System

46.2 Register Descriptions

46.2.1 Temperature Sensor Calibration Data Register (TSCDRH, TSCDRL)

Address(es): TEMPSCONST.TSCDRL 007F C0ACh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	Unique value for each chip							

Address(es): TEMPSCONST.TSCDRH 007F C0ADh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	Unique value for each chip							

The TSCDRH and TSCDRL registers store temperature sensor calibration data measured for each chip at factory shipment.
Temperature sensor calibration data consists of the high and low bytes of the overall value (CAL_{88}) obtained by using the 12-bit A/D converter to convert the voltage output by the temperature sensor under the condition of Ta = Tj = 88°C and AVCC0 = VREFH0 = 3.3 V. The TSCDRH register stores the higher 4 bits of the converted value, and the TSCDRL register stores the lower 8 bits.

The voltage V1 output by the temperature sensor under the condition of Ta = Tj = 88°C can be calculated from the converted value CAL_{88} according to the formula below.

$V1 = 3.3 \times CAL_{88}/4096 \quad (V)$

Note that voltage V1 is independent of both the AVCC0 and VREFH0 voltages.

46.3 Using the Temperature Sensor

The temperature sensor outputs a voltage which varies with the temperature. The user can obtain the temperature surrounding the MCU using the 12-bit A/D converter to convert this voltage into a digital value.

46.3.1 Before Using the Temperature Sensor

Perform a calibration of the temperature sensor as shown below. The voltage output by the temperature sensor is proportional to the temperature, which can be calculated according to the formula below.

Formula for the temperature characteristic:
T = (Vs – V1)/Slope + T1

T: Measured temperature (°C)
Vs: Voltage output by the temperature sensor when the temperature is measured (V)
T1: Sample temperature measurement at first point (°C)
V1: Voltage output by the temperature sensor when T1 is measured (V)
T2: Sample temperature measurement at second point (°C)
V2: Voltage output by the temperature sensor when T2 is measured (V)
(V2 – V1)/(T2 – T1) = Slope: Temperature gradient of the temperature sensor (V/°C)

Characteristics vary from sensor to sensor. Therefore, it is recommended that two different sample temperatures are measured.
Use the 12-bit A/D converter to measure the voltage V1 output by the temperature sensor at temperature T1.
Again, using the 12-bit A/D converter, measure the voltage V2 output by the temperature sensor at a different temperature T2. Obtain the temperature gradient (Slope = (V2 – V1)/(T2 – T1)) from these results.
Subsequently, obtain temperatures by substituting the slope into the formula for the temperature characteristic (T = (Vs – V1)/Slope + T1).

If you are using the temperature gradient given in section 51, Electrical Characteristics, use the A/D converter to measure the voltage V1 output by the temperature sensor at temperature T1, and then calculate the temperature characteristic by using the formula below.
However, this method produces less accurate temperatures than measurement at two points.

T = (Vs – V1)/Slope + T1

In this MCU, the TSCDRH and TSCDRL registers store the temperature value (CAL_{88}) of the temperature sensor measured under the condition of Ta = Tj = 88°C and AVCC0 = VREFH0 = 3.3 V. By using this value as the sample measurement result at the first point, preparation before using the temperature sensor can be omitted.
This measured value CAL_{88} can be calculated as follows:

CAL_{88} = (TSCDRH register value << 8) + TSCDRL register value

If V1 is calculated from CAL_{88},

$V1 = 3.3 \times CAL_{88}/4096$ (V)

Using this, the measured temperature can be calculated according to the formula below.

T = (Vs – V1)/Slope + 88 (°C)

T: Measured temperature (°C)
Vs: Voltage output by the temperature sensor when the temperature is measured (V)
V1: Voltage output by the temperature sensor when Ta = Tj = 88°C and AVCC0 = VREFH0 = 3.3 V (V)
Slope: Temperature gradient listed in Table 51.56 ÷ 1000 (V/°C)

Error in the measured temperature (the range of variation is 3σ) is shown in Figure 46.2.

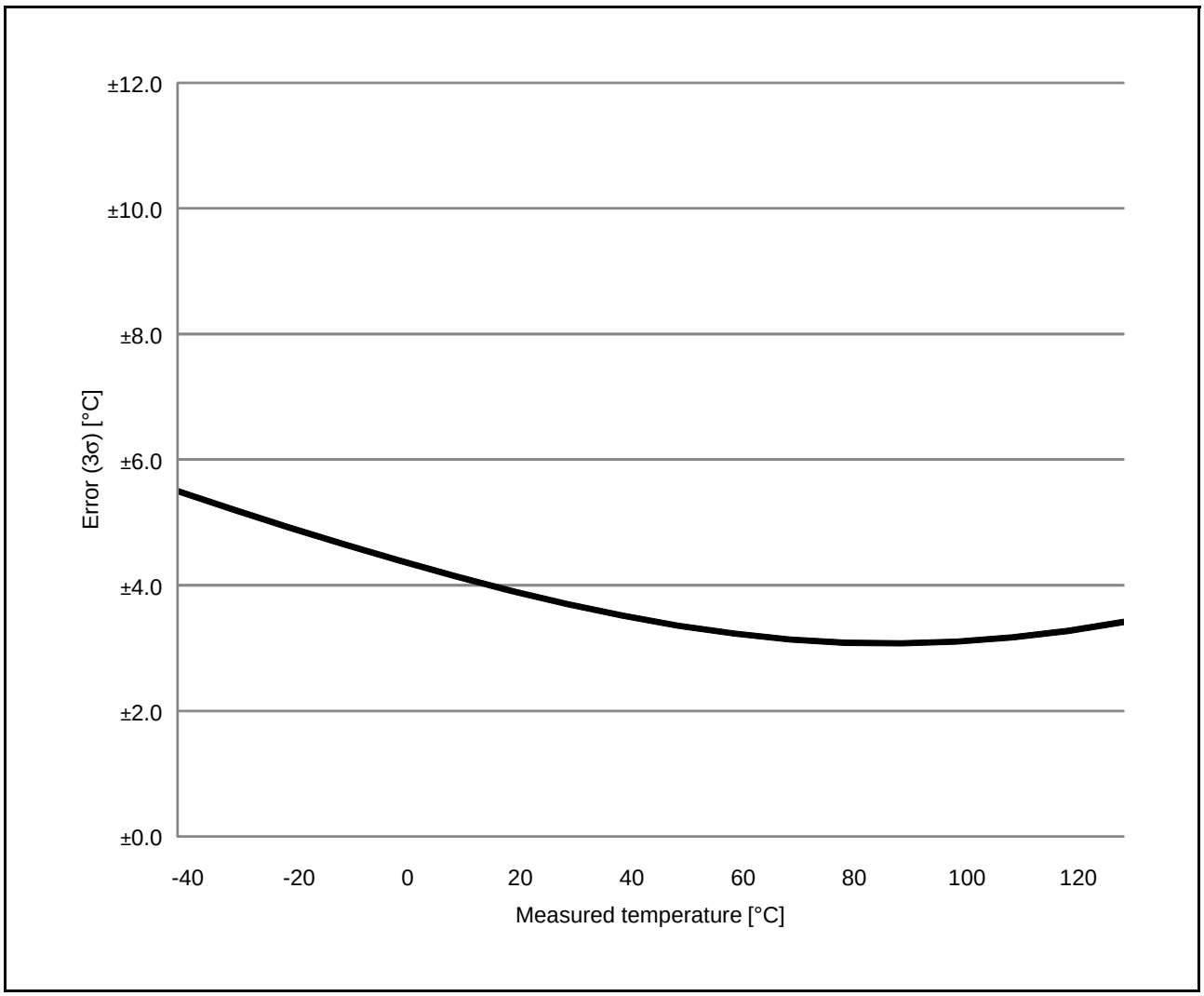


Figure 46.2 Error in the Measured Temperature (Designed Value)

46.3.2 Setting the 12-Bit A/D Converter

For details, refer to section 44, 12-Bit A/D Converter (S12ADE).

47. Comparator B (CMPBa)

Comparator B compares a reference input voltage and an analog input voltage. comparator B2 and comparator B3 operate independently.
In this section, “PCLK” is used to refer to PCLKB.

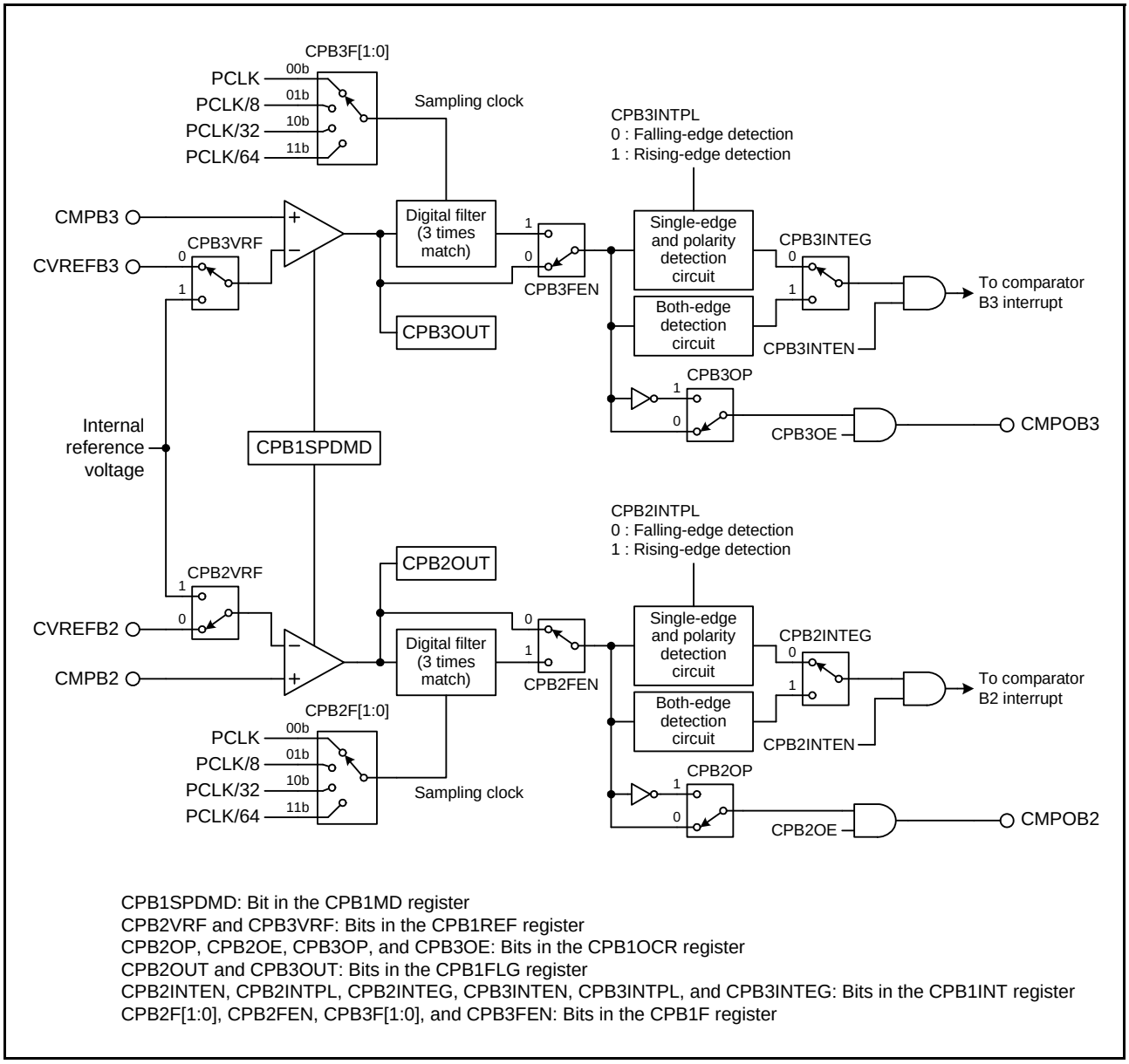
47.1 Overview

The comparison result of the reference input voltage and analog input voltage can be read by software. The comparison result can also be output externally. The reference input voltage can be selected from either an input to the CVREFBn pin (n = 2, 3) or the internal reference voltage generated internally in the MCU.
The comparator B response speed can be set before starting an operation. Setting high-speed mode decreases the response delay time, but increases current consumption. Setting low-speed mode increases the response delay time, but decreases current consumption.
Table 47.1 lists the specifications of comparator B, Figure 47.1 shows a block diagram of comparators B2 and B3 when the window function is disabled, and Figure 47.2 shows a block diagram of comparators B2 and B3 when the window function is enabled. Table 47.2 lists the I/O pins of comparator B.

Table 47.1 Comparator B Specifications (n = 2, 3)

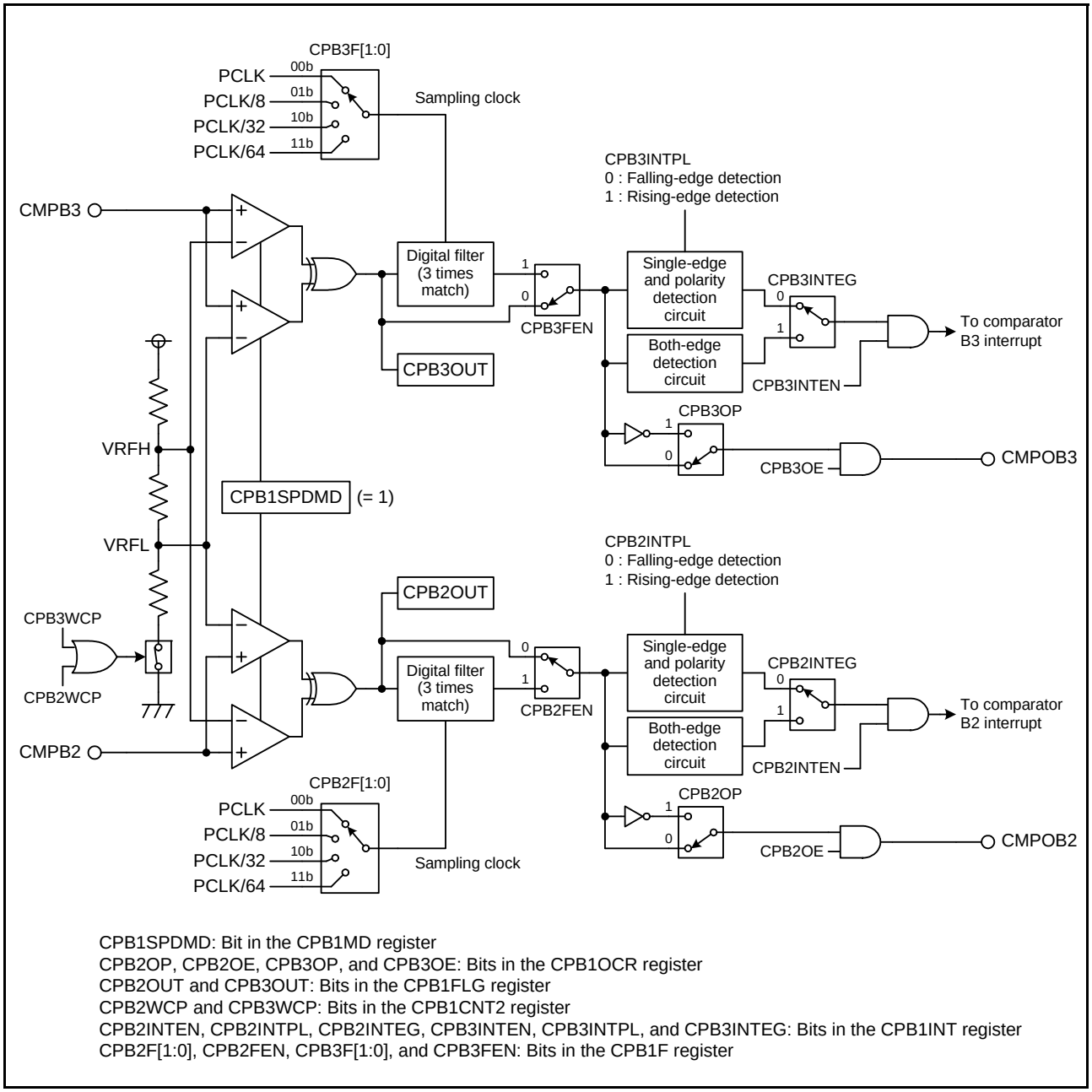
Item	Specification
Analog input voltage	Input voltage to the CMPBn pin
Reference input voltage	Input voltage to the CVREFBn pin or internal reference voltage
Comparison result	Read from the CPBFLG.CPBnOUT flag The comparison result can be output to the CMPOBn pin.
Interrupt request generation timing	When comparator B2 comparison result changes When comparator B3 comparison result changes
Selectable function	• Digital filter function Whether the digital filter is applied or not, and the sampling frequency can be selected. • Window function Whether the window function is enabled or disabled (VRFL < CMPBn < VRFH)*1 can be selected. • Reference input voltage CVREFBn pin input or internal reference voltage (generated internally) can be selected. • Comparator B response speed High-speed mode/low-speed mode can be selected.
Low power consumption function	Module stop state can be set.

Note 1. VRFL: low-side reference voltage, VRFH: high-side reference voltage



CPB1SPDMD: Bit in the CPB1MD register
CPB2VRF and CPB3VRF: Bits in the CPB1REF register
CPB2OP, CPB2OE, CPB3OP, and CPB3OE: Bits in the CPB1OCR register
CPB2OUT and CPB3OUT: Bits in the CPB1FLG register
CPB2INTEN, CPB2INTPL, CPB2INTEG, CPB3INTEN, CPB3INTPL, and CPB3INTEG: Bits in the CPB1INT register
CPB2F[1:0], CPB2FEN, CPB3F[1:0], and CPB3FEN: Bits in the CPB1F register

Figure 47.1 Block Diagram of Comparators B2 and B3 When Window Function is Disabled



CPB1SPDMD: Bit in the CPB1MD register
CPB2OP, CPB2OE, CPB3OP, and CPB3OE: Bits in the CPB1OCR register
CPB2OUT and CPB3OUT: Bits in the CPB1FLG register
CPB2WCP and CPB3WCP: Bits in the CPB1CNT2 register
CPB2INTEN, CPB2INTPL, CPB2INTEG, CPB3INTEN, CPB3INTPL, and CPB3INTEG: Bits in the CPB1INT register
CPB2F[1:0], CPB2FEN, CPB3F[1:0], and CPB3FEN: Bits in the CPB1F register

Figure 47.2 Block Diagram of Comparators B2 and B3 When Window Function is Enabled

Table 47.2 I/O Pins of Comparator B

Pin Name	I/O	Function
CMPB2	Input	Comparator B2 analog pin
CVREFB2	Input	Comparator B2 reference input voltage pin
CMPB3	Input	Comparator B3 analog pin
CVREFB3	Input	Comparator B3 reference input voltage pin
CMPOB2	Output	Comparator B2 output
CMPOB3	Output	Comparator B3 output

47.2 Register Descriptions

47.2.1 Comparator B1 Control Register 1 (CPB1CNT1)

Address: 0008 C5A0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CPB3INI	—	—	—	CPB2INI
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CPB2INI	Comparator B2 Power Enable	0: Disabled 1: Enabled (comparator powered on)	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	CPB3INI	Comparator B3 Power Enable	0: Disabled 1: Enabled (comparator powered on)	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

47.2.2 Comparator B1 Control Register 2 (CPB1CNT2)

Address: 0008 C5A1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CPB3WCP	—	—	—	CPB2WCP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CPB2WCP	Comparator B2 Window Function Enable	0: Disabled 1: Enabled	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	CPB3WCP	Comparator B3 Window Function Enable	0: Disabled 1: Enabled	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

47.2.3 Comparator B1 Flag Register (CPB1FLG)

Address: 0008 C5A2h

	b7	b6	b5	b4	b3	b2	b1	b0
	CPB3OUT	—	—	—	CPB2OUT	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	CPB2OUT	Comparator B2 Monitor Flag	When the window function is disabled 0: CMPB2 < CVREFB2, CMPB2 < internal reference voltage, or comparator B2 operation disabled 1: CMPB2 > CVREFB2, or CMPB2 > internal reference voltage When the window function is enabled*1 0: CMPB2 < VRFL, CMPB2 > VRFH, or comparator B2 operation disabled 1: VRFL < CMPB2 < VRFH	R
b6 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	CPB3OUT	Comparator B3 Monitor Flag	When the window function is disabled 0: CMPB3 < CVREFB3, CMPB3 < internal reference voltage, or comparator B3 operation disabled 1: CMPB3 > CVREFB3, or CMPB3 > internal reference voltage When the window function is enabled*1 0: CMPB3 < VRFL, CMPB3 > VRFH, or comparator B3 operation disabled 1: VRFL < CMPB3 < VRFH	R

Note 1. VRFL: low-side reference voltage, VRFH: high-side reference voltage

47.2.4 Comparator B1 Interrupt Control Register (CPB1INT)

Address: 0008 C5A3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	CPB3INTPL	CPB3INTEG	CPB3INTEN	—	CPB2INTPL	CPB2INTEG	CPB2INTEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CPB2INTEN	Comparator B2 Interrupt Enable	0: Disabled 1: Enabled	R/W
b1	CPB2INTEG	Comparator B2 Interrupt Edge Select*1	0: Single edge 1: Both edges	R/W
b2	CPB2INTPL	Comparator B2 Interrupt Edge Polarity Select*2	0: Falling edge 1: Rising edge	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	CPB3INTEN	Comparator B3 Interrupt Enable	0: Disabled 1: Enabled	R/W
b5	CPB3INTEG	Comparator B3 Interrupt Edge Select*1	0: Single edge 1: Both edges	R/W
b6	CPB3INTPL	Comparator B3 Interrupt Edge Polarity Select*2	0: Falling edge 1: Rising edge	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. The IR104.IR flag may become 1 (interrupt request is generated) when the CPB0INTPL bit is modified, and the IR105.IR flag may become 1 (interrupt request is generated) when the CPB1INTPL bit is modified. For details, refer to section 15, Interrupt Controller (ICUb).

Note 2. The CPBnINTPL bit setting is valid only when the CPBnINTEG bit is 0 (single edge is selected as the comparator interrupt edge).

47.2.5 Comparator B1 Filter Select Register (CPB1F)

Address: 0008 C5A4h

	b7	b6	b5	b4	b3	b2	b1	b0
	CPB3F[1:0]		—	CPB3FEN	CPB2F[1:0]		—	CPB2FEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CPB2FEN	Comparator B2 Filter Enable/Disable Select*1	0: Filter is disabled. 1: Filter is enabled.	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	RW
b3, b2	CPB2F[1:0]	Comparator B2 Filter Select*1	b3 b2 0 0: Sampling at PCLK 0 1: Sampling at PCLK/8 1 0: Sampling at PCLK/32 1 1: Sampling at PCLK/64	R/W
b4	CPB3FEN	Comparator B3 Filter Enable/Disable Select*1	0: Filter is disabled. 1: Filter is enabled.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	RW
b7, b6	CPB3F[1:0]	Comparator B3 Filter Select*1	b7 b6 0 0: Sampling at PCLK 0 1: Sampling at PCLK/8 1 0: Sampling at PCLK/32 1 1: Sampling at PCLK/64	R/W

Note 1. The CPBnF[1:0] bits are enabled only when the CPBnFEN bit = 1 (filter is enabled).

47.2.6 Comparator B1 Mode Select Register (CPB1MD)

Address: 0008 C5A5h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CPB1SPDMD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CPB1SPDMD	Comparator B Speed Select	0: High-speed mode 1: Low-speed mode*1	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	RW

Note 1. When rewriting the CPB1SPDMD bit, be sure to set the CPBnINI bit (n = 2, 3) in the CPB1CNT1 register to 0 in advance.

47.2.7 Comparator B1 Reference Input Voltage Select Register (CPB1REF)

Address: 0008 C5A6h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CPB3VRF	—	—	—	CPB2VRF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CPB2VRF	Comparator B2 Reference Input Voltage Select	0: Comparator B2 reference input voltage is CVREFB2 input 1: Comparator B2 reference input voltage is internal reference voltage*1, *2, *3	R/W*4
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	RW
b4	CPB3VRF	Comparator B3 Reference Input Voltage Select	0: Comparator B3 reference input voltage is CVREFB3 input 1: Comparator B3 reference input voltage is internal reference voltage*1, *2, *3	R/W*4
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	RW

Note 1. Enabled only when the window function is disabled. When the window function is enabled, the internal reference voltage of comparator B is selected regardless of the setting of this bit.
Note 2. When the internal reference voltage is selected, the temperature sensor output cannot be selected for the A/D converter.
Note 3. When the internal reference voltage is selected, the voltage generation circuit operates and current increases by about 75 µA. This circuit is not automatically turned off even if the MCU enters software standby mode with the internal reference voltage selected.
Note 4. Do not rewrite the CPBnVRF bit when CPB1CNT2.CPBnWCP = 0.

[Notes on changing the reference input voltage]

♦ When changing the reference input voltage from CVREFBn (n = 2, 3) to the internal reference voltage, use the following procedure.

1. Set the CPB1CNT1.CPBnINI bit to 1.
2. Set the CPB1CNT2.CPBnWCP bit to 1.
3. Set the CPB1REF.CPBnVRF bit to 1 to select the internal reference voltage.
4. Set the analog select bit (ASEL) in the pin function control register of the port that is used as the CVREFBn pin to 0.
5. Wait for the comparator stabilization time (min. 100 µs).
6. Set the CPB1CNT2.CPBnWCP bit to 0.

♦ When changing the reference input voltage from the internal reference voltage to CVREFBn (n = 2, 3), use the following procedure.

1. Set the CPB1CNT1.CPBnINI bit to 1.
2. Set the CPB1CNT2.CPBnWCP bit to 1.
3. Set the CPB1REF.CPBnVRF bit to 0 to select the CVREFBn pin input.
4. Set the analog select bit (ASEL) in the pin function control register of the port that is used as the CVREFBn pin to 1.
5. Wait for the comparator stabilization time (min. 100 µs).
6. Set the CPB1CNT2.CPBnWCP bit to 0.

47.2.8 Comparator B1 Output Control Register (CPB1OCR)

Address: 0008 C5A7h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CPB3OP	CPB3OE	—	—	CPB2OP	CPB2OE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	CPB2OE	CMPOB2 Pin Output Enable	0: Comparator B2 CMPOB2 pin output disabled*1 1: Comparator B2 CMPOB2 pin output enabled	R/W
b1	CPB2OP	CMPOB2 Output Polarity Select	0: Comparator B2 output is output to CMPOB2 1: Inverted comparator B2 output is output to CMPOB2	RW
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	RW
b4	CPB3OE	CMPOB3 Pin Output Enable	0: Comparator B3 CMPOB3 pin output disabled*1 1: Comparator B3 CMPOB3 pin output enabled	RW
b5	CPB3OP	CMPOB3 Output Polarity Select	0: Comparator B3 output is output to CMPOB3 1: Inverted comparator B3 output is output to CMPOB3	RW
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	RW

Note 1. When the CPBnOE bit (n = 2, 3) is set to 0 to disable the CMPOBn pin output, 0 is output to CMPOBn regardless of the value of the CPBnOP bit.

47.3 Operation

Comparator B2 and comparator B3 operate independently, and their operations are the same. Operation is not guaranteed when the values of registers are changed during comparator operation. Table 47.3 shows the procedure of setting comparator B associated registers when the window function is disabled. Table 47.4 shows the procedure of setting comparator B associated registers when the window function is enabled.

Table 47.3 Procedure for Setting Registers Associated with Comparator B When Window Function is Disabled (n = 2, 3)

Step No.	Register	Bit	Setting	
1	PijPFS of the port to which the CMPBn pin is assigned	ASEL	1	
2	CPB1MD	CPBSPDMD	Select the comparator response speed (0: High-speed mode/1: Low-speed mode)	
3	CPB1CNT1	CPBnINI	Powered on: 1	
4	CPB1CNT2	CPBnWCP	1*1	
5	CPB1REF	CPBnVRF	0: Reference input voltage = CVREFBn input*1	1: Reference input voltage = Internal reference voltage
6	PijPFS of the port to which the CVREFBn pin is assigned	ASEL	1	0
7	Waiting for the comparator stabilization time (min. 100 µs)*1			
8	CPB1CNT2	CPBnWCP	0*1	
9	CPB1F	Select whether to enable or disable the filter and select the sampling clock.		
10	Waiting for the comparator stabilization time (min. 100 µs)			
11	CPB1OCR	CPBnOP, CPBnOE	Set the CMPOBn output (select the polarity and set output enabled or disabled).	
12	CPB1INT	CPBnINTEN	When using an interrupt: 1 (interrupt enabled)	
		CPBnINTEG	When using an interrupt or the ELC: Select the input edge (1 = both edges or 0 = single edge).	
		CPBnINTPL	When using an interrupt or the ELC: For CPBnINTEG = 0 (single edge selected), select the input polarity (1 = rising edge or 0 = falling edge).	
13	IPR104 (comparator B2), IPR105 (comparator B3)	IPR[3:0]	When using an interrupt: Select the interrupt priority level.	
	IR104 (comparator B2), IR105 (comparator B3)	IR	When using an interrupt: 0 (no interrupt requested: initialization)	
	IER07	IEN0 (comparator B2), IEN1 (comparator B3)	When using an interrupt: 1 (interrupt is enabled on the interrupt controller (ICU) side)	

Note 1. This setting is necessary when changing the reference input voltage from the CVREFBn input to the internal reference voltage or from the internal reference voltage to the CVREFBn input. When selecting the CVREFBn input after the reset is released, steps 4, 5, 7, and 8 are not necessary because the initial value of the CPB1REF.CPBnVRF bit is 0.

Table 47.4 Procedure for Setting Registers Associated with Comparator B When Window Function is Enabled (n = 2, 3)

Step No.	Register	Bit	Setting
1	PijPFS of the port to which the CMPBn pin is assigned	ASEL	1
2	CPB1MD	CPBSPDMD	0 (always specify high-speed mode)
3	CPB1CNT1	CPBnINI	Powered on: 1
4	CPB1F	Select whether to enable or disable the filter and select the sampling clock.	
5	CPB1CNT2	CPBnWCP	1 (operation enabled)
6	Waiting for the comparator stabilization time (min. 100 µs)		
7	CPB1OCR	CPBnOP, CPBnOE	Set the CMPOBn output (select the polarity and set output enabled or disabled).
8	CPB1INT	CPBnINTEN	When using an interrupt: 1 (interrupt enabled)
		CPBnINTEG	When using an interrupt or the ELC: Select the input edge (1 = both edges or 0 = single edge).
		CPBnINTPL	When using an interrupt or the ELC: For CPBnINTEG = 0 (single edge selected), select the input polarity (1 = rising edge or 0 = falling edge).
9	IPR104 (comparator B2), IPR105 (comparator B3)	IPR[3:0]	When using an interrupt: Select the interrupt priority level.
	IR104 (comparator B2), IR105 (comparator B3)	IR	When using an interrupt: 0 (no interrupt requested: initialization)
	IER07	IEN0 (comparator B2), IEN1 (comparator B3)	When using an interrupt: 1 (interrupt enabled)

Figure 47.3 shows an operating example of comparator Bn (n = 2, 3) when window function is disabled.
The reference input voltage (CVREFB2/CVREFB3 or internal reference voltage) and the analog input voltage are compared. If the analog input voltage is higher than the reference input voltage, the CPB1FLG.CPBnOUT bit is set to 1. If the analog input voltage is lower than the reference input voltage, the CPBnOUT bit is set to 0.
To use the comparator Bn interrupt, set the CPB1INT.CPBnINTEN bit to 1 (interrupt enabled). If the comparison result changes at this time, a comparator Bn interrupt request is generated. For details on interrupts, refer to section 47.4, Comparator B2 and Comparator B3 Interrupts.
The values of the registers should not be changed during comparison.

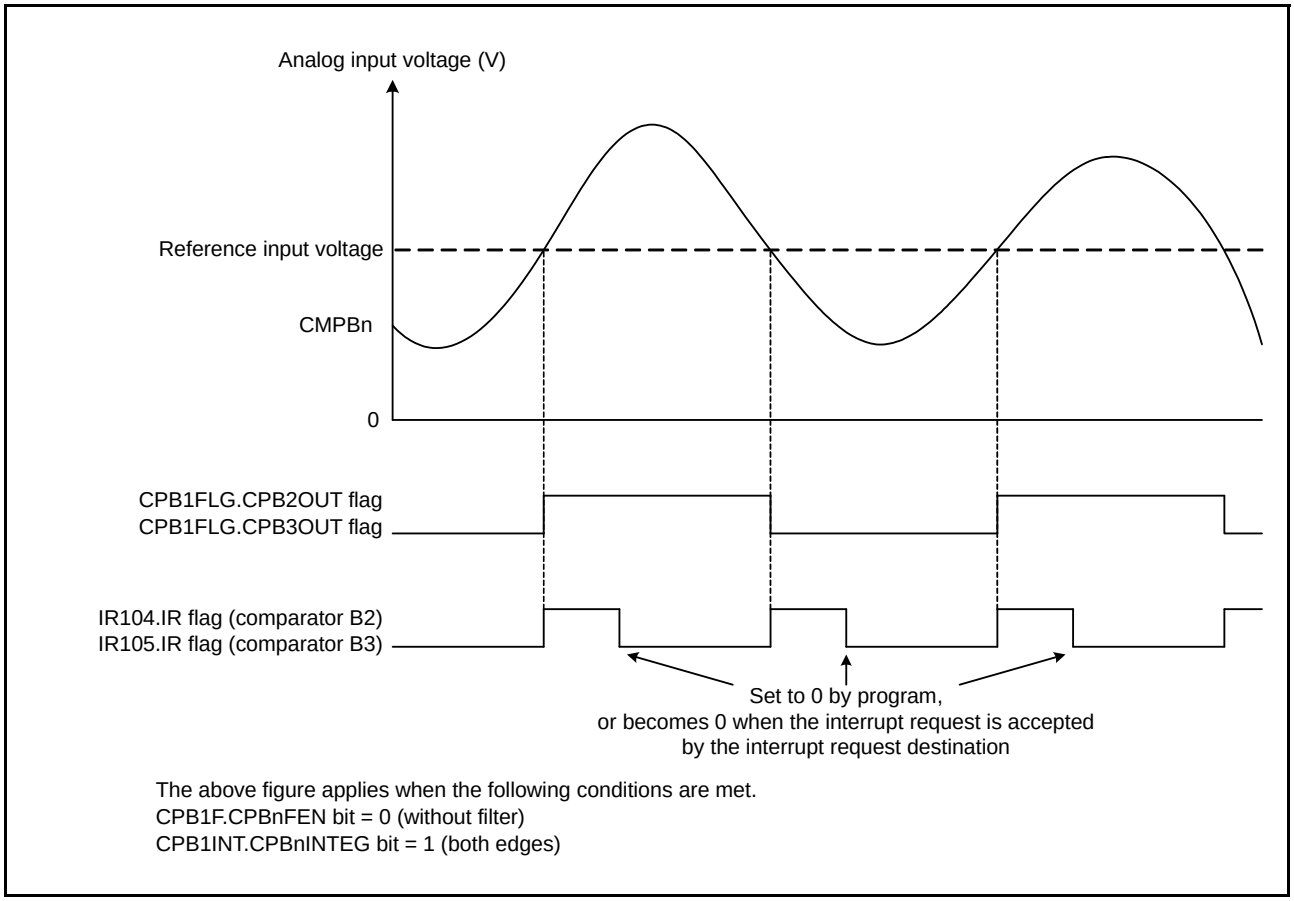


Figure 47.3 Operating Example of Comparator Bn When Window Function is Disabled (n = 2, 3)

Figure 47.4 shows an operation example of comparator Bn (n = 2, 3) when the window function is enabled.
The internal reference voltage (VRFH/VRFL) for the window function and the analog input voltage are compared. The CPBnOUT bit is set to 1 when VRFL < the analog input voltage < VRFH, and the CPBnOUT bit is set to 0 when the analog input voltage < VRFL, or VRFH < the analog input voltage.
To use the comparator Bn interrupt, set the CPB1INT.CPBnINTEN bit to 1 (interrupt enabled). If the comparison result changes at this time, a comparator Bn interrupt request is generated. For details on interrupts, refer to section 47.4, Comparator B2 and Comparator B3 Interrupts.
The values of the registers should not be changed during comparison.

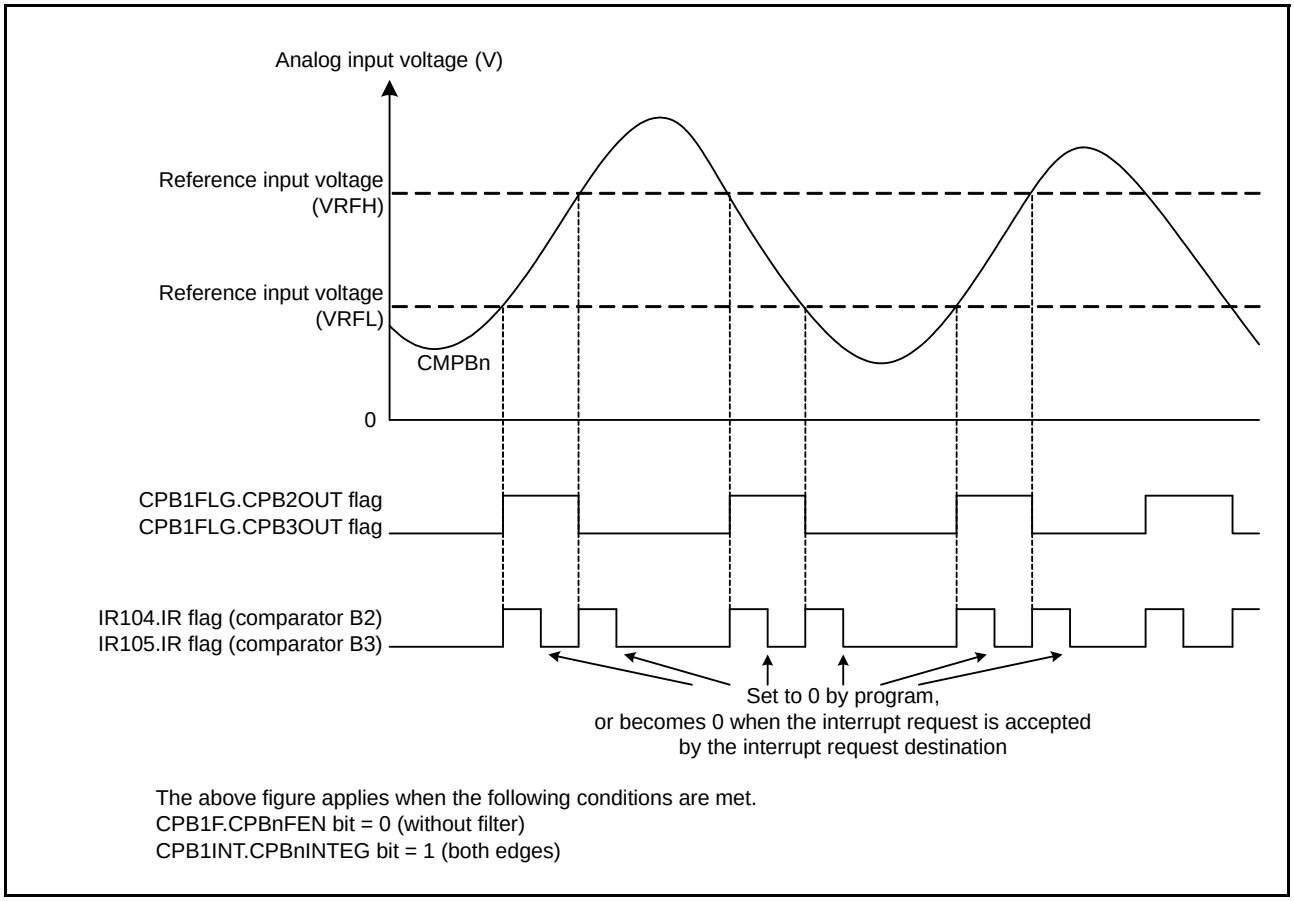


Figure 47.4 Operating Example of Comparator Bn When Window Function is Enabled (n = 2, 3)

47.3.1 Comparator Bn Digital Filter (n = 2, 3)

The sampling clock can be selected by the CPB1F.CPBnF[1:0] bits. The CPBnOUT signal (internal signal) output from comparator Bn is sampled at every sampling clock cycle. At the next clock timing after the level matches three times, the IR104.IR flag (when comparator B2 selected) or IR105.IR flag (when comparator B3 selected) is set to 1 (interrupt requested).

Figure 47.5 shows the configuration of the comparator Bn digital filter, and Figure 47.6 shows an operating example of the comparator Bn digital filter.

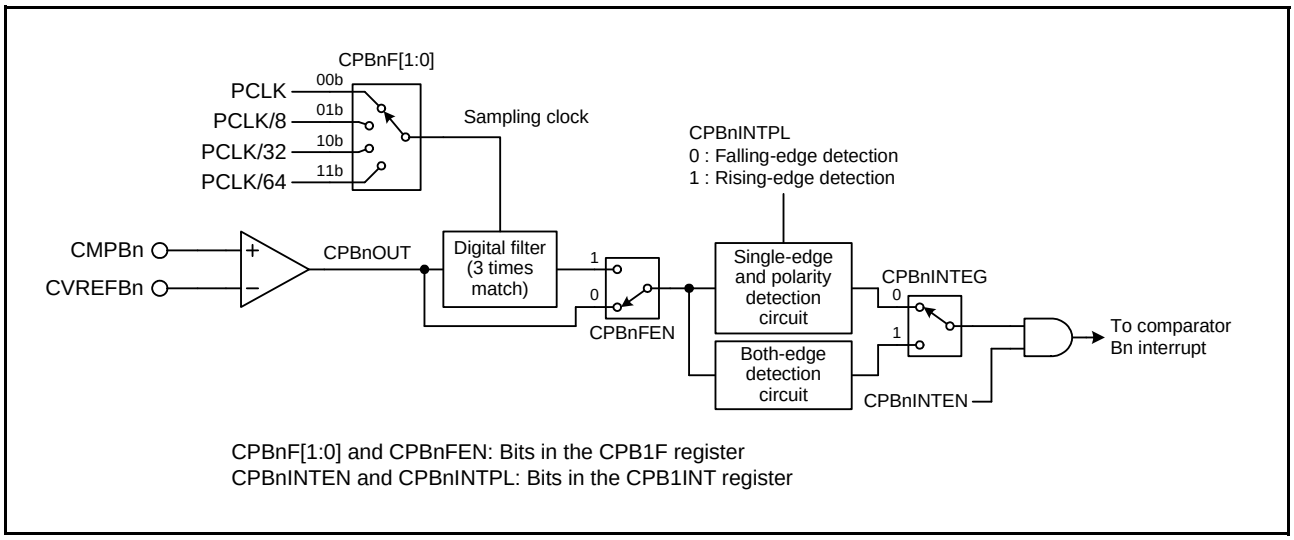


Figure 47.5 Configuration of Comparator Bn Digital Filter (n = 2, 3)

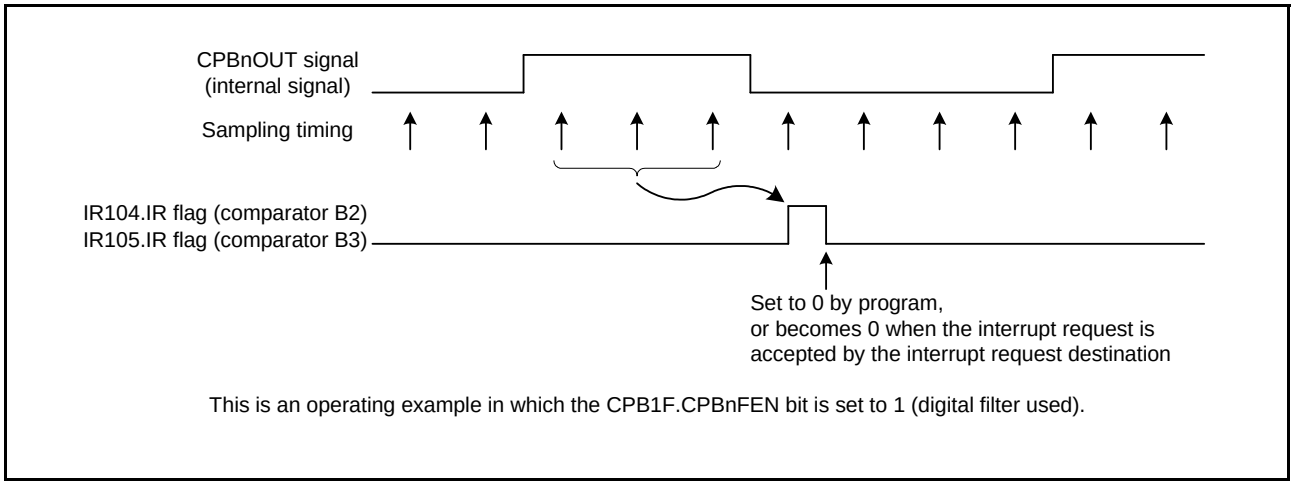


Figure 47.6 Operating Example of Comparator Bn Digital Filter (n = 2, 3)

47.3.2 Comparator Bn Output Function (n = 2, 3)

The comparison result from comparator B can be output to external pins. The CPB1OCR.CPBnOP and CPB1OCR.CPBnOE bits can be used to set the output polarity (non-inverted output or inverted output) and output enabled or disabled. For the register settings and corresponding comparator output, refer to section 47.2.8, Comparator B1 Output Control Register (CPB1OCR).

To output the comparator B comparison result to the CMPOB2 or CMPOB3 output pin, use the following procedure to make port settings. Note that the ports are set to input after a reset.

(1) Set the mode and input for comparator B (steps 1 to 10 listed in Table 47.3 and steps 1 to 6 listed in Table 47.4).
(2) Select the polarity of the CMPOB2 or CMPOB3 output and enable the output (set the CPB1OCR.CPBnOP and CPB1OCR.CPBnOE bits).
(3) Set the port mode register and pin function control register corresponding to the CMPOB2 or CMPOB3 output pin (start outputting from the pin).

47.3.3 Example of Using Comparator B to Exit Software Standby Mode

The following shows an example of using comparator B2 output to exit software standby mode.
In this example, it is assumed that the reference input voltage (CVREFB2) > analog input voltage (CMPB2).

Set the following steps (1) to (3) before entering software standby mode.

(1) Set the registers associated with comparator B2 according to section 47.3, Operation.
However, set the CPB1F.CPB2FEN bit to ‘filter is disabled’, the CPB1OCR.CPB2OE bit to ‘output enabled’, and the CPB1OCR.CPB2OP bit to ‘comparator B2 output is output to CMPOB2’.
(2) Make the IRQ7 interrupt settings according to section 15.4.8, External Pin Interrupts.
However, set the IRQFLTE0.FLTEN7 bit to 0 (digital filter disabled) and set the IRQCR7.IRQMD[1:0] bits to the same polarity as that of comparator B2 output.
In this example, a rising edge is selected.
(3) Set the multi-function pin controller to select the CMPOB2 function and enable IRQ7.

When exiting software standby mode, input a voltage from the comparator B2 analog pin (CMPB2) so that the reference input voltage (CVREFB2) is less than the analog input voltage (CMPB2). This allows the IRQ7 interrupt to be generated through the comparator B2 output pin (CMPOB2) and the MCU exits software standby mode.

47.4 Comparator B2 and Comparator B3 Interrupts

Comparator B generates two interrupt requests from sources, comparator B2 and . The comparator Bn interrupt (n = 2, 3) uses the IR104.IR flag, IR105.IR flag, IPR104.IPR[3:0] bits, IPR105.IPR[3:0] bits, and the respective single interrupt vector.

To use the comparator Bn interrupt, set the CPB1INT.CPBnINTEN bit to 1 (interrupt enabled). In addition, select either single-edge detection or both-edge detection using the CPB1INT.CPBnINTEG bit. When single-edge detection is selected, select the polarity using the CPB1INT.CPBnINTPL bit.

Inputs can also be passed through the digital filter with four different sampling clocks.

47.5 Usage Note

47.5.1 Module Stop Function Setting

Operation of comparator B can be enabled or disabled by setting a bit in the module stop control register B (MSTPCRB). Comparator B is initially disabled after a reset. Registers only become accessible after it has been released from the module stop state. For details, refer to section 11, Low Power Consumption.

48. Data Operation Circuit (DOC)

48.1 Overview

The data operation circuit (DOC) is used to compare, add, or subtract 16-bit values.
Table 48.1 lists the specifications of the DOC and Figure 48.1 is a block diagram of the DOC.
An interrupt can be generated if the result of 16-bit comparison meets one of the set interrupt conditions.

Table 48.1 DOC Specifications

Item	Description
Data operation function	16-bit data comparison, addition, and subtraction
Lower power consumption function	The DOC can be placed in a module-stop state.
Interrupts	• The result of data comparison meets the detection condition. • The result of data addition is greater than FFFFh, which is an overflow. • The result of data subtraction is less than 0000h, which is an underflow.
Event link function (output)	• The result of data comparison meets the detection condition. • The result of data addition is greater than FFFFh, which is an overflow. • The result of data subtraction is less than 0000h, which is an underflow.

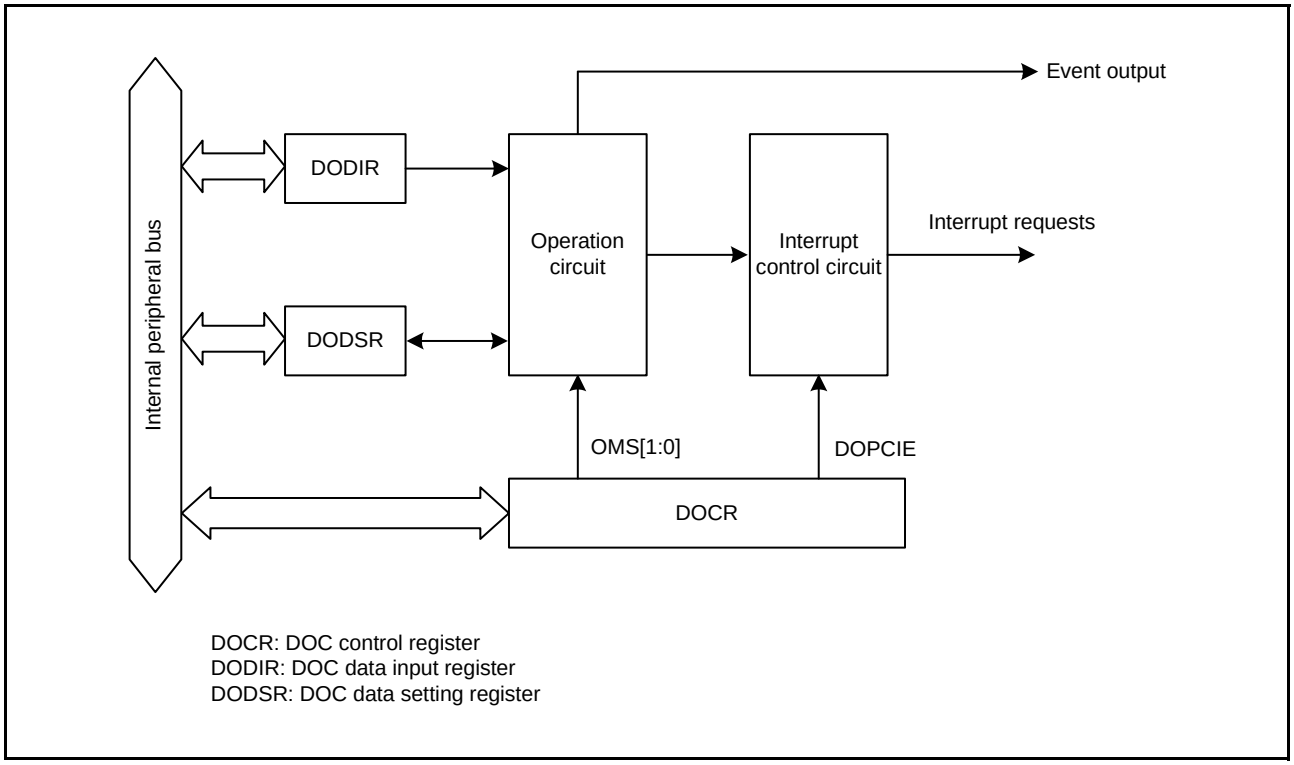


Figure 48.1 DOC Block Diagram

48.2 Register Descriptions

48.2.1 DOC Control Register (DOCR)

Address(es): DOC.DOCR 0008 B080h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DOPCFCL	DOPCF	DOPCIE	—	DCSEL	OMS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	OMS[1:0]	Operating Mode Select	b1 b0 0 0: Data comparison mode 0 1: Data addition mode 1 0: Data subtraction mode 1 1: Setting prohibited	R/W
b2	DCSEL	Detection Condition Select*1	0: ‘Not equal to’ is to be detected. 1: ‘Equal to’ is to be detected.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	DOPCIE	Data Operation Circuit Interrupt Enable	0: Interrupt disabled 1: Interrupt enabled	R/W
b5	DOPCF	Data Operation Result Flag	Indicates the result of an operation.	R
b6	DOPCFCL	Data Operation Result Clear	0: Retain the value of the DOPCF flag. 1: Clears the DOPCF flag.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Valid only when data comparison mode is selected.

The DOCR register specifies the operation of DOC, or enabling or disabling of the interrupt.

OMS[1:0] Bits (Operating Mode Select)

These bits select the operating mode of the DOC.

DCSEL Bit (Detection Condition Select)

This bit is valid only when data comparison mode is selected.

This bit selects the condition for detection in data comparison mode.

DOPCIE Bit (Data Operation Circuit Interrupt Enable)

Setting this bit to 1 enables interrupts from the DOC.

DOPCF Flag (Data Operation Result Flag)

[Setting conditions]

- The condition selected by the DCSEL bit is met
- A result of data addition is greater than FFFFh
- A result of data subtraction is less than 0000h

[Clearing condition]

- Writing 1 to the DOPCFCL bit

DOPCFCL Bit (Data Operation Result Clear)

Writing 1 to this bit clears the DOPCF flag.

This bit is read as 0.

48.2.2 DOC Data Input Register (DODIR)

Address(es): DOC.DODIR 0008 B082h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The DODIR register is a readable and writable register that holds values for use in operations.

48.2.3 DOC Data Setting Register (DODSR)

Address(es): DOC.DODSR 0008 B084h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The DODSR register is a readable and writable register that holds values for use in comparison or the results of other operations.

In data comparison mode, store the standard value for use in comparison in this register.

In data addition or data subtraction mode, this register holds the results of operations.

48.3 Operation

48.3.1 Data Comparison Mode

Figure 48.2 shows an example of the steps involved in data comparison mode operation by the DOC.
An example of operation when DCSEL is set to 0 (‘not equal to’ is to be detected as the result of data comparison) is shown below.

(1) Writing 00b to the DOCR.OMS[1:0] bits places the DOC in the data comparison mode.
(2) Specify the standard value for comparison in the DODSR register.
(3) Write the value for comparison in the DODIR register.
(4) Write all values for use in comparison to the DODIR register.
(5) If the value written to the DODIR register is not equal to the value set in the DODSR register, the DOCR.DOPCF flag becomes 1. If the DOCR.DOPCIE bit is 1, a data operation circuit interrupt is also issued.

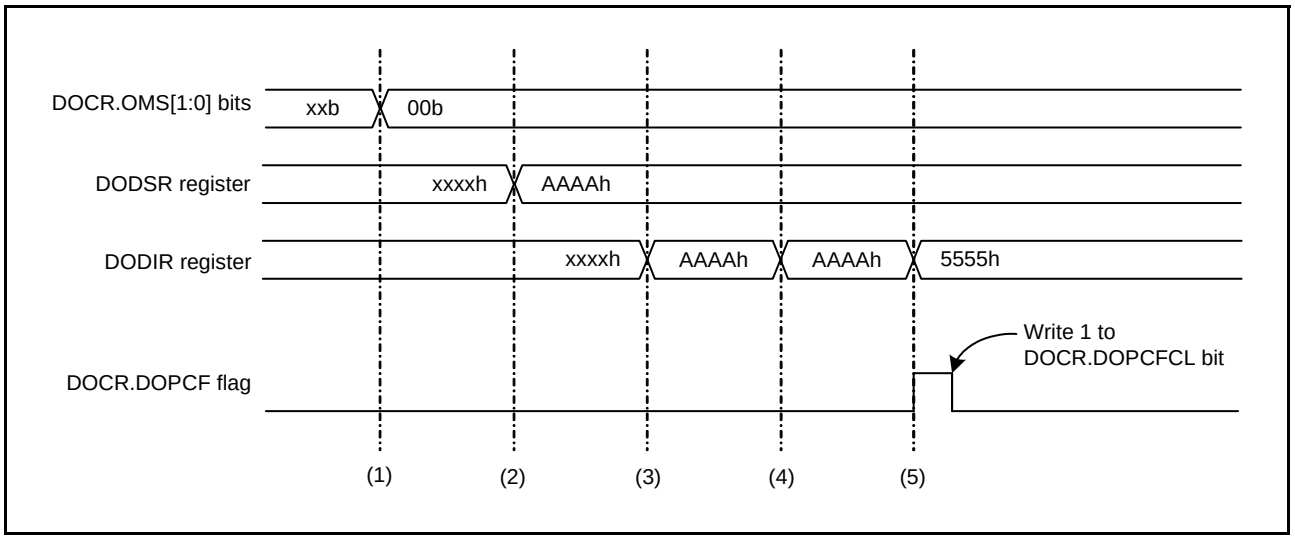


Figure 48.2 Example of Operation in Data Comparison Mode

48.3.2 Data Addition Mode

Figure 48.3 shows an example of the steps involved in data addition mode operation by the DOC.

(1) Writing 01b to the DOCR.OMS[1:0] bits selects data addition mode.
(2) Set the initial value in the DODSR register.
(3) Write the value for addition in the DODIR register. The result of the operation is stored in DODSR.
(4) Write all values for use in addition to the DODIR register.
(5) If the result of the operation is greater than FFFFh, the DOCR.DOPCF flag becomes 1. If the DOCR.DOPCIE bit is 1, a data operation circuit interrupt is also issued.

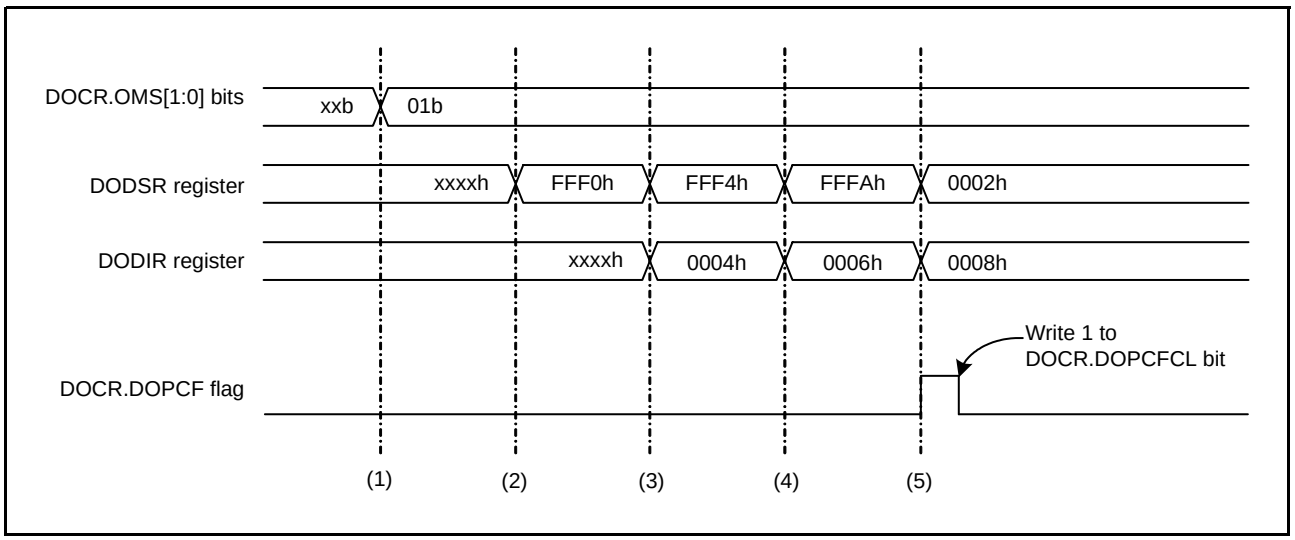


Figure 48.3 Example of Operation in Data Addition Mode

48.3.3 Data Subtraction Mode

Figure 48.4 shows an example of the steps involved in data subtraction mode operation by the DOC.

(1) Writing 10b to the DOCR.OMS[1:0] bits selects data subtraction mode.
(2) Set the initial value in the DODSR register.
(3) Write the value for subtraction in the DODIR register. The result of the operation is stored in DODSR.
(4) Write all values for use in subtraction to the DODIR register.
(5) If the result of the operation is less than 0000h, the DOCR.DOPCF flag becomes 1. If the DOCR.DOPCIE bit is 1, a data operation circuit interrupt is also issued.

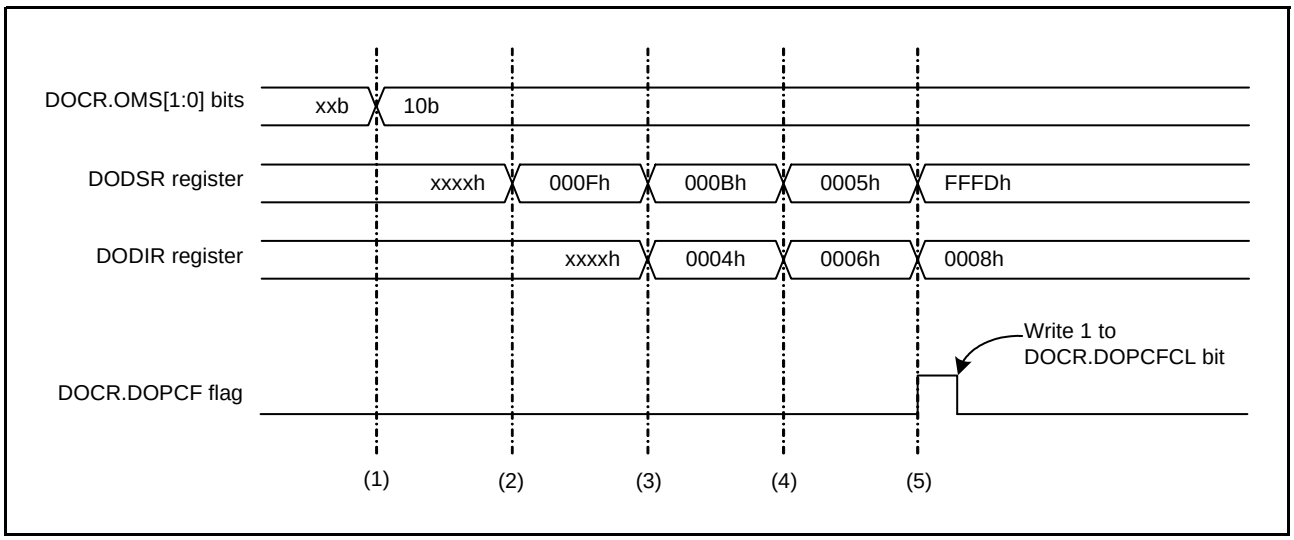


Figure 48.4 Example of Operation in Data Subtraction Mode

48.4 Interrupt Requests

The data operation circuit interrupt (DOPCI) is the interrupt request generated by the DOC. The DOCR.DOPCF flag becomes 1 when the interrupt source condition is satisfied.
Table 48.2 lists the details of the interrupt request.

Table 48.2 Interrupt Request from DOC

Interrupt Request	Data Operation Result Flag	Interrupt Generation Timing
Data operation circuit interrupt (DOPCI)	DOPCF	• The result of data comparison meets the detection condition. • The result of data addition is greater than FFFFh. • The result of data subtraction is less than 0000h.

48.5 Event Link Output

The DOC outputs event signals for the event link controller (ELC) under the following conditions, and these can be used to initiate operations by other modules selected in advance.

- The result of data comparison meets the detection condition.
- The result of data addition is greater than FFFFh.
- The result of data subtraction is less than 0000h.

48.5.1 Interrupt Handling and Event Linking

The DOC has a bit to enable or disable interrupts. When an interrupt source condition is satisfied while the interrupt is enabled, the interrupt request signal is issued to the CPU.
In contrast, an event link output signal is sent to other modules as an event signal via the ELC when an interrupt source is generated, regardless of the setting of the corresponding interrupt enable bit.

48.6 Usage Note

48.6.1 Module Stop Function Setting

Operation of the DOC can be enabled or disabled by setting the MSTPB6 bit in module stop control register B (MSTPCRB). The DOC is initially disabled after a reset. Register access is enabled by releasing the module stop state. For details, refer to section 11, Low Power Consumption.

49. RAM

This MCU has an on-chip high-speed static RAM.

49.1 Overview

Table 49.1 lists the specifications of the RAM.

Table 49.1 Specifications of RAM

Item	Description
Capacity	64 Kbytes (0000 0000h to 0000 FFFFh)
Access	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.*1
Low power consumption function	Transitions to the module stopped state are possible.

Note 1. Selectable by the RAME bit in SYSCR1. For details on SYSCR1, see section 3.2.2, System Control Register 1 (SYSCR1).

49.2 Operation

49.2.1 Low Power Consumption Function

Power consumption can be reduced by setting module stop control register C (MSTPCRC) to stop supply of the clock signal to the RAM.
Setting the MSTPCRC.MSTPC0 bit to 1 stops supply of the clock signal to RAM.
Stopping supply of the clock signal places the RAM in the module stop state. The RAM operates after initialization by a reset.
The RAM is not accessible in the module stop state. Do not allow transitions to the module stop state while access to RAM is in progress.
For details on the MSTPCRC register, see section 11, Low Power Consumption.

49.2.2 Notes on Self-Diagnosis of the RAM

A write buffer is mounted for the RAM. When the same address is read after a write operation, data in the write buffer, rather than in the memory cell of the RAM may be read. When the RAM is self-diagnosed, confirm that the data have been written by following the procedure below so that data will not be read from the write buffer.

(1) Write data to the address targeted for diagnosis.
(2) Write data to an address which is at least 4 addresses away from the that in (1).
(3) Read the data from the address in (1).

50. Flash Memory (FLASH)

This MCU has packages with 384 and 512 Kbyte flash memory (ROM) for storing code and 8-Kbyte flash memory (E2 DataFlash) for storing data.
In this section, “PCLK” is used to refer to PCLKB.

50.1 Overview

Table 50.1 lists the Flash Memory Specifications.
Table 50.7 lists the I/O Pins Used in Boot Mode.

Table 50.1 Flash Memory Specifications

Item	Description
Memory space	• User area: Up to 512 Kbytes • Data area: 8 Kbytes • Extra area: Stores the start-up area information, access window information, and unique ID
Software commands	• The following commands are implemented: Program, blank check, block erase, and all-block erase • The following commands are implemented for programming the extra area: Start-up area information program and access window information program
Value after erasure	• ROM: FFh • E2 DataFlash: FFh
Interrupt	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.
On-board programming	Boot mode (SCI Interface)*1 • Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. • The user area and data area are rewritable. Boot mode (FINE interface)*1 • The FINE is used. • The user area and data area are rewritable. Boot mode (USB interface)*1 • Channel 0 of the USB 2.0 function (USB0) module is used. • The user area and data area are rewritable. • The flash memory can be rewritable in self-powered or bus-powered mode. • A personal computer can be connected using only a USB cable. Self-programming in single-chip mode • The user area and data area are rewritable using the flash rewrite routine in the user program.
Off-board programming	The user area and data area are rewritable using a flash programmer compatible with this MCU.
ID code protection	• Connection with the serial programmer can be enabled or disabled using ID codes in boot mode. • Connection with the on-chip debugging emulator can be enabled or disabled using ID codes.
Start-up program protection	This function is used to safely rewrite block 0 to block 7.
Area protection	This function enables rewriting only the selected blocks in the user area and disables the other blocks during self-programming.
Background Operation (BGO)	Programs on the ROM can be executed while rewriting the E2 DataFlash.

Note 1. Refer to the manual of each serial programmer and “Renesas Flash Programmer Flash memory programming software User’s Manual” for more details.

50.2 ROM Area and Block Configuration

The maximum ROM size of this MCU is 512 Kbytes. The ROM area is divided into blocks. A block is 2-Kbyte area. When executing the block erase command, the memory is erased by the block. Figure 50.1 shows the ROM Area and Block Configuration.

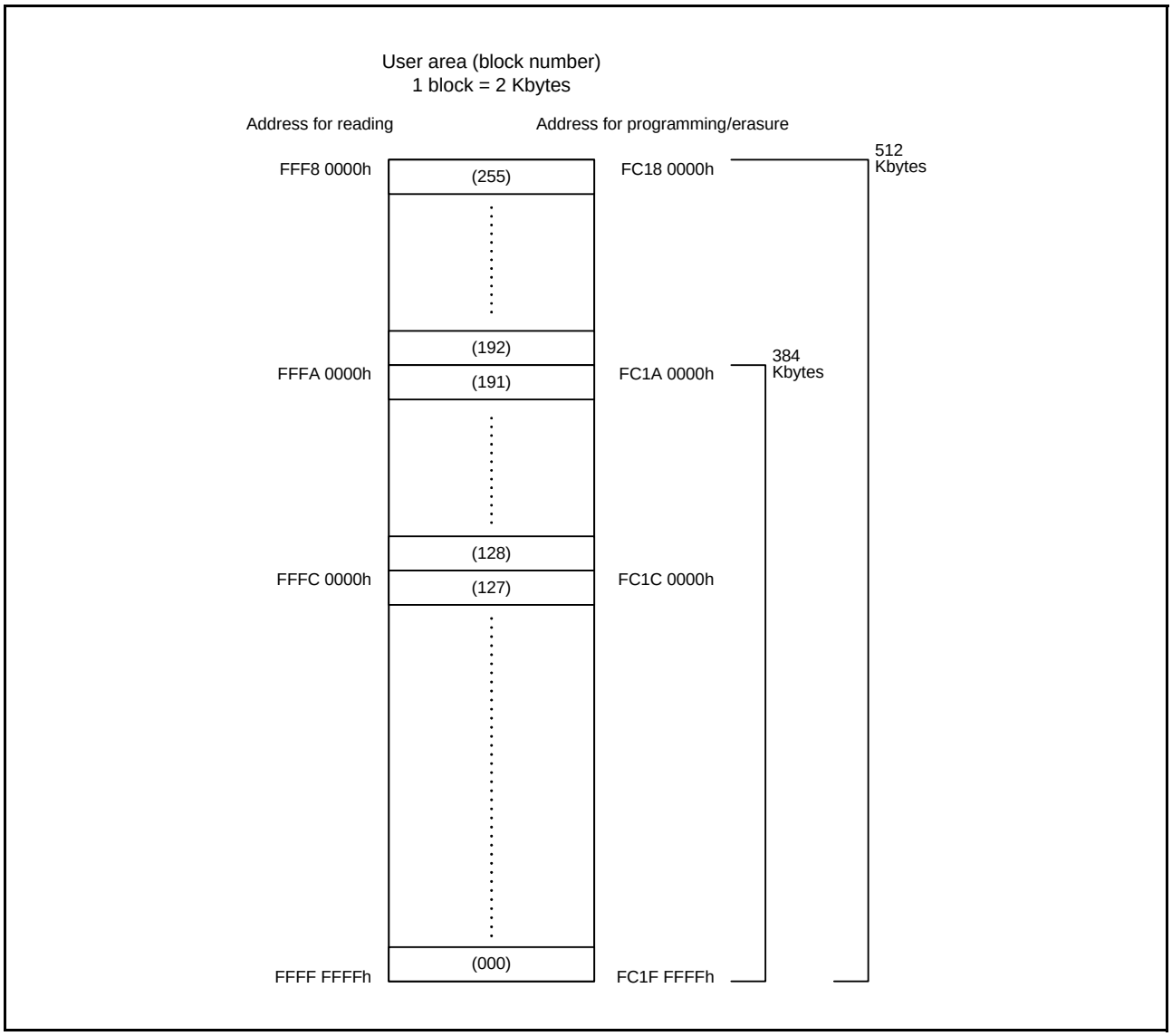


Figure 50.1 ROM Area and Block Configuration

Table 50.2 Correspondence Between ROM Capacity and Addresses for Reading

ROM Capacity	Addresses for Reading
512 Kbytes	FFF8 0000h to FFFF FFFFh
384 Kbytes	FFFA 0000h to FFFF FFFFh

50.3 E2 DataFlash Area and Block Configuration

The E2 DataFlash is 8 Kbytes in the MCU. The E2 DataFlash is divided into blocks and erased in block units. Figure 50.2 shows the E2 DataFlash Area and Block Configuration.

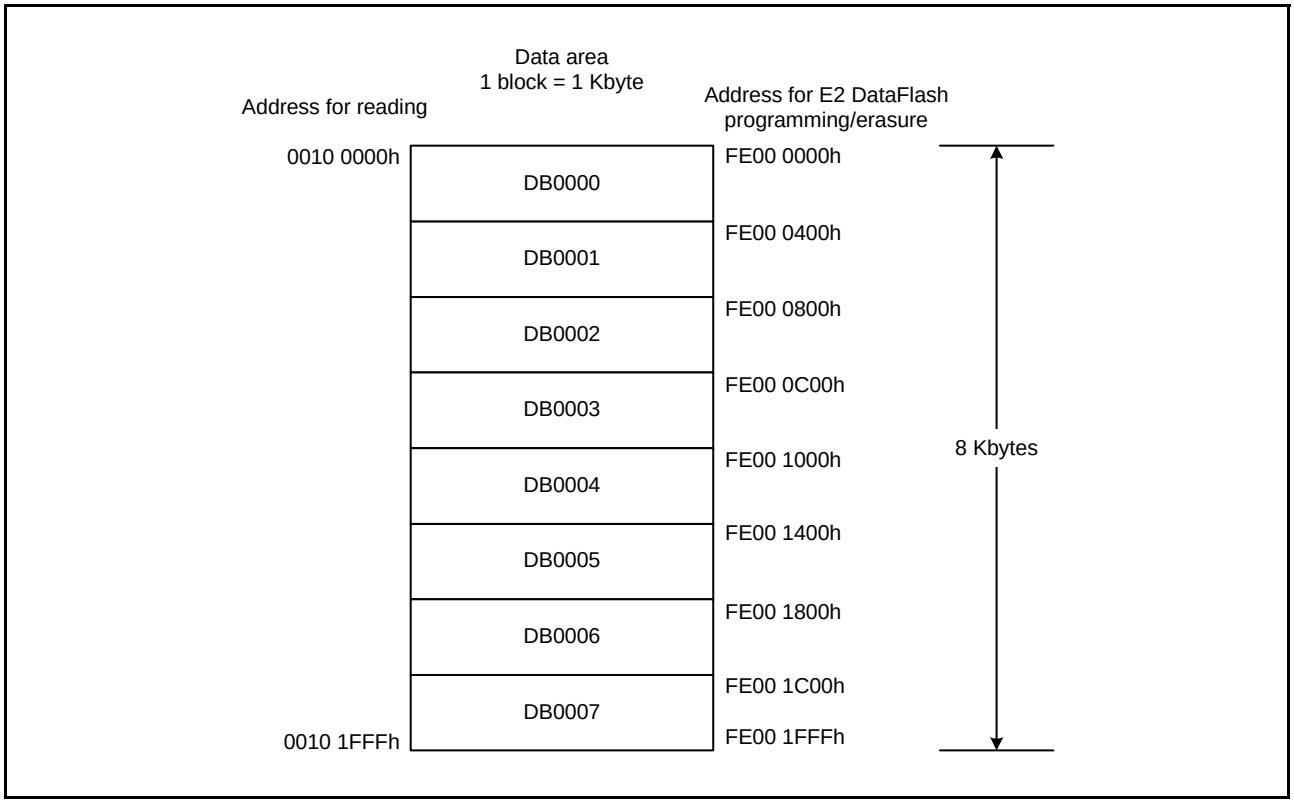


Figure 50.2 E2 DataFlash Area and Block Configuration

50.4 Register Descriptions

50.4.1 E2 DataFlash Control Register (DFLCTL)

Address(es): FLASH.DFLCTL 007F C090h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DFLEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	DFLEN	E2 DataFlash Access Enable	0: Access to E2 DataFlash and access to the extra area in P/E mode*1 disabled 1: Access to E2 DataFlash and access to the extra area in P/E mode*1 enabled	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Start-up area information program and access window information program

The DFLCTL register is used to enable or disable access (read, program, and erase) to the E2 DataFlash and access (start-up area information program, and access window information program) to the extra area in P/E mode.
When reading, programming, and erasing the E2 DataFlash, set the DFLCTL.DFLEN bit to 1 and wait for the E2 DataFlash STOP recovery time (tDSTOP) to elapse before reading the E2 DataFlash and entering E2 DataFlash P/E mode. Do not read the E2 DataFlash or enter E2 DataFlash P/E mode until tDSTOP has elapsed.
Refer to section 50.7.1, Sequencer Modes for details on E2 DataFlash P/E mode. Refer to section 51, Electrical Characteristics for E2 DataFlash STOP recovery time (tDSTOP).

50.4.2 Flash P/E Mode Entry Register (FENTRYR)

Address(es): FLASH.FENTRYR 007F FFB2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FEKEY[7:0]								FENTRYD	—	—	—	—	—	—	FENTRY0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FENTRY0	ROM P/E Mode Entry 0	0: ROM is in read mode. 1: ROM can be placed in P/E mode.	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	FENTRYD	E2 DataFlash P/E Mode Entry	0: E2 DataFlash is in read mode. 1: E2 DataFlash can be placed in P/E mode.	R/W
b15 to b8	FEKEY[7:0]	Key Code	The FEKEY[7:0] bits are used to control rewriting of the FENTRYR register. When rewriting the value of the lower 8 bits, set the FEKEY[7:0] bits to AAh at the same time (write this register in 16 bits). The FEKEY[7:0] bits are read as 00h.	R/W

To rewrite the ROM or E2 DataFlash, the FENTRYD or FENTRY0 bit must be set to 1 to place the ROM or E2 DataFlash in P/E mode.
When returning to read mode, set the FENTRYR register and confirm that its value has been rewritten before reading the ROM or E2 DataFlash.
Refer to section 50.7.1, Sequencer Modes for details on P/E mode and read mode.

FENTRY0 Bit (ROM P/E Mode Entry 0)

This bit is used to place the ROM in P/E mode.
[Setting condition]

- AA01h is written to the FENTRYR register when the FENTRYR register is 0000h.

Note: When entering ROM P/E mode, the instruction fetch address must be transferred to an area other than the ROM so that instruction fetching is not executed to the ROM. Copy necessary instruction code to the internal RAM and jump to the RAM. Note that E2 DataFlash can be rewritten by a program in the ROM.

[Clearing condition]

- AA00h is written to the FENTRYR register.

FENTRYD Bit (E2 DataFlash P/E Mode Entry)

This bit is used to place the E2 DataFlash in P/E mode.
[Setting condition]

- AA80h is written to the FENTRYR register when the FENTRYR register is 0000h.

[Clearing condition]

- AA00h is written to the FENTRYR register.

50.4.3 Protection Unlock Register (FPR)

Address(es): FLASH.FPR 007F C180h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

This write-only register is used to protect the FPMCR register from being rewritten inadvertently when the CPU runs out of control. Writing to the FPMCR register is enabled only when the following procedure is used to access the register.

Procedure to unlock protection

(1) Write A5h to the FPR register.
(2) Write a set value to the FPMCR register.
(3) Write the inverted set value to the FPMCR register.
(4) Write a set value to the FPMCR register again.

When a procedure other than the above is used to write data, the FPSR.PERR flag is set to 1.

50.4.4 Protection Unlock Status Register (FPSR)

Address(es): FLASH.FPSR 007F C184h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	PERR	Protect Error Flag	0: No error 1: An error occurs.	R
b7 to b1	—	Reserved	These bits are read as 0.	R

PERR Flag (Protect Error Flag)

When the FPMCR register is not accessed as described in the procedure to unlock protection, data is not written to the register and this flag is set to 1.

[Setting condition]

- The FPMCR register is not accessed as described in the procedure to unlock protection.

[Clearing condition]

- The FPMCR register is accessed according to the procedure to unlock protection described in section 50.4.3, Protection Unlock Register (FPR).

50.4.5 Flash P/E Mode Control Register (FPMCR)

Address(es): FLASH.FPMCR 007F C100h

	b7	b6	b5	b4	b3	b2	b1	b0
	FMS2	LVPE	—	FMS1	RPDIS	—	FMS0	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	FMS0	Flash Operating Mode Select 0	FMS2 FMS1 FMS0 0 0 0: ROM/E2 DataFlash read mode 0 1 0: E2 DataFlash P/E mode 0 1 1: Discharge mode 1 1 0 1: ROM P/E mode 1 1 1: Discharge mode 2 Settings other than above are prohibited.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	RPDIS	ROM P/E Disable	0: ROM programming/erasure enabled 1: ROM programming/erasure disabled	R/W
b4	FMS1	Flash Operating Mode Select 1	See the FMS0 bit.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	LVPE	Low-Voltage P/E Mode Enable	0: Low-voltage P/E mode disabled 1: Low-voltage P/E mode enabled	R/W
b7	FMS2	Flash Operating Mode Select 2	See the FMS0 bit.	R/W

The FPMCR register is used to set the operating mode of the flash memory.
This register is protected. Set its value using the procedure to unlock protection. For details, refer to section 50.4.3, Protection Unlock Register (FPR).
When entering discharge mode 2 or ROM P/E mode, or during either of these modes, an instruction must be executed on the RAM.

FMS0, FMS1, and FMS2 Bits (Flash Operating Mode Select 0 to Flash Operating Mode Select 2)

These bits are used to set the operating mode of the flash memory.
[Transition from read mode to ROM P/E mode]
Set the FMS2 bit = 0, the FMS1 bit = 1, the FMS0 bit = 1, and the RPDIS bit = 0.
Wait for ROM mode transition wait time 1 (tDIS, refer to section 51, Electrical Characteristics).
Set the FMS2 bit = 1, the FMS1 bit = 1, the FMS0 bit = 1, and the RPDIS bit = 0.
Set the FMS2 bit = 1, the FMS1 bit = 0, the FMS0 bit = 1, and the RPDIS bit = 0.
Wait for ROM mode transition wait time 2 (tMS, refer to section 51, Electrical Characteristics).
[Transition from ROM P/E mode to read mode]
Set the FMS2 bit = 1, the FMS1 bit = 1, the FMS0 bit = 1, and the RPDIS bit = 0.
Wait for ROM mode transition wait time 1 (tDIS, refer to section 51, Electrical Characteristics).
Set the FMS2 bit = 0, the FMS1 bit = 1, the FMS0 bit = 1, and the RPDIS bit = 0.
Set the FMS2 bit = 0, the FMS1 bit = 0, the FMS0 bit = 0, and the RPDIS bit = 1.
Wait for ROM mode transition wait time 2 (tMS, refer to section 51, Electrical Characteristics).
[Transition from read mode to E2 DataFlash P/E mode]
Set the FMS2 bit = 0, the FMS1 bit = 1, the FMS0 bit = 0, and the RPDIS bit = 0.
[Transition from E2 DataFlash P/E mode to read mode]
Set the FMS2 bit = 0, the FMS1 bit = 0, the FMS0 bit = 0, and the RPDIS bit = 1.

Wait for ROM mode transition wait time 2 (tMS, refer to section 51, Electrical Characteristics).

RPDIS Bit (ROM P/E Disable)

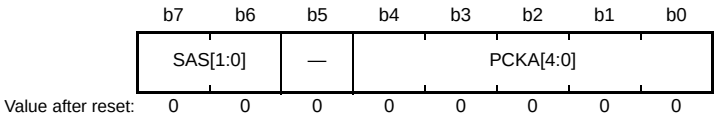
This bit is used to disable the execution of ROM programming/erasure with software.

LVPE Bit (Low-Voltage P/E Mode Enable)

Set this bit to 0 for programming/erasure in high-speed mode, and set this bit to 1 for programming/erasure in middle-speed mode.

50.4.6 Flash Initial Setting Register (FISR)

Address(es): FLASH.FISR 007F C1D8h



Bit	Symbol	Bit Name	Description	R/W
b4 to b0	PCKA[4:0]	Peripheral Clock Notification	These bits are used to set the frequency of the FlashIF clock (FCLK).	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7, b6	SAS[1:0]	Start-Up Area Select	b7 b6 0 x: The start-up area is selected according to the start-up area settings of the extra area. 1 0: The start-up area is switched to the default area temporarily. 1 1: The start-up area is switched to the alternate area temporarily.	R/W

x: Don’t care

Data can be written to the FISR register in ROM P/E mode or E2 DataFlash P/E mode.

PCKA[4:0] Bits (Peripheral Clock Notification)

These bits are used to set the frequency of the FlashIF clock (FCLK) when programming/erasing the ROM/E2 DataFlash.

Set the FCLK frequency in the PCKA[4:0] bits before programming/erasure. Do not change the frequency during programming/erasure of the ROM/E2 DataFlash.

[When FCLK is higher than 4 MHz]

Set a rounded-up value for a non-integer frequency.

For example, set 32 MHz (PCKA[4:0] bits = 11111b) when the frequency is 31.5 MHz.

[When FCLK is 4 MH or lower]

Do not use a non-integer frequency.

Use the FCLK at a frequency of 1, 2, 3, or 4 MHz.

Note: When the PCKA[4:0] bits are set to a frequency different from the FCLK, the data in the ROM/E2 DataFlash may be damaged.

Table 50.3 Example of FlashIF Clock Frequency Settings

FlashIF Clock Frequency (MHz)	PCKA[4:0] Bit Setting	FlashIF Clock Frequency (MHz)	PCKA[4:0] Bit Setting	FlashIF Clock Frequency (MHz)	PCKA[4:0] Bit Setting
32	11111b	31	11110b	30	11101b
29	11100b	28	11011b	27	11010b
26	11001b	25	11000b	24	10111b
23	10110b	22	10101b	21	10100b
20	10011b	19	10010b	18	10001b
17	10000b	16	01111b	15	01110b
14	01101b	13	01100b	12	01011b
11	01010b	10	01001b	9	01000b
8	00111b	7	00110b	6	00101b
5	00100b	4	00011b	3	00010b
2	00001b	1	00000b	—	—

SAS[1:0] Bits (Start-Up Area Select)

These bits are used to select the start-up area. To change the start-up area, the following three methods can be used.

(1) When selecting the start-up area according to the start-up area settings of the extra area

With the SAS[1:0] bits set to 00b or 01b, the start-up area is selected according to the start-up area settings of the extra area. The settings are enabled after a reset is released.

(2) When switching the start-up area to the default area temporarily

When 10b is written to the SAS[1:0] bits, the start-up area is switched to the default area immediately after data is written to the register, regardless of the start-up area settings of the extra area.
When a reset is generated after this, the area is selected according to the start-up area settings of the extra area.

(3) When switching the start-up area to the alternative area temporarily

When 11b is written to the SAS[1:0] bits, the start-up area is switched to the alternative area, regardless of the start-up area settings of the extra area.
When a reset is generated after this, the area is selected according to the start-up area settings of the extra area.

50.4.7 Flash Reset Register (FRESETR)

Address(es): FLASH.FRESETR 007F C124h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	FRESET
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	FRESET	Flash Reset	0: Flash control circuit reset is released. 1: Flash control circuit is reset.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FRESET Bit (Flash Reset)

When this bit is set to 1, registers FASR, FSARH, FSARL, FEARH, FEARL, FWB0, FWB1, FWB2, FWB3, FCR, and FEXCR are reset. Also, the values of registers FEAMH and FEAML are undefined. Do not access these registers during a reset. To release the reset, set this bit to 0.

Do not write to this register while executing a software command or rewriting the extra area.

50.4.8 Flash Area Select Register (FASR)

Address(es): FLASH.FASR 007F C104h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EXS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	EXS	Extra Area Select	0: User area or data area 1: Extra area	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Data can be written to the FASR register in ROM P/E mode or E2 DataFlash P/E mode.

This register is initialized by a reset or setting the FRESETR.FRESET bit to 1.

Data cannot be written to this register while the FRESETR.FRESET bit is 1.

EXS Bit (Extra Area Select)

Set this bit to 1 before issuing a software command (start-up area information program or access window information program) for the extra area. Set this bit to 0 before issuing a software command (program, blank check, block erase, or all-block erase) for the user area.

After issuing a software command, do not change the value until changing it for issuing the next software command.

50.4.9 Flash Control Register (FCR)

Address(es): FLASH.FCR 007F C114h

	b7	b6	b5	b4	b3	b2	b1	b0
	OPST	STOP	—	—	CMD[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b3 to b0	CMD[3:0]	Software Command Setting	b3 b0 0 0 0 1: Program 0 0 1 1: Blank check 0 1 0 0: Block erase 0 1 1 0: All-block erase Settings other than above are prohibited.*1	R/W
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	STOP	Forced Processing Stop	When this bit is set to 1, the processing being executed can be forcibly stopped.	R/W
b7	OPST	Processing Start	0: Processing stops. 1: Processing starts.	R/W

Note 1. This does not include set the FCR register to 00h when the FSTATR1.FRDY flag is 1.

Data can be written to the FCR register when in ROM P/E mode and the ROM can be programmed/erased or in E2 DataFlash P/E mode.
This register is initialized by a reset or setting the FRESETR.FRESET bit to 1. Data cannot be written to this register while the FRESETR.FRESET bit is 1.
Note that this register cannot be initialized by the FRESETR.FRESET bit while a software command is being executed.

CMD[3:0] Bits (Software Command Setting)

These bits are used to set a software command (program, blank check, block erase, or all-block erase).
The function of each command is described below.
[Program]

- Write the value set in registers FWB0, FWB1, FWB2, and FWB3 to the address set in registers FSARH and FSARL.

[Blank check]

- Check whether there is data in the area from the address set in registers FSARH and FSARL to the address set in registers FEARH and FEARL. Confirm that data is not programmed in the area. This command does not guarantee whether the area remains erased.

[Block erase]

- Erase consecutive areas specified in the flash memory by the blocks. Set the beginning address of the block in registers FSARH and FSARL and the end address in registers FEARH and FEARL.

[All-block erase]

- Erase all blocks in the ROM or E2 DataFlash.
  All-block erase requires less time to erase the memory compared to block erase. When erasing the whole of the ROM area, set the beginning address of the ROM area in registers FSARH and FSARL, and the end address in registers FEARH and FEARL. Table 50.4 lists the setting address for all-block erase.

Table 50.4 Setting Address for All-Block Erase

Target	Memory Size	FSARH/FSARL	FEARH/FEARL
ROM	512 Kbytes	FC18 0000h	FC1F FFF8h
	384 Kbytes	FC1A 0000h	FC1F FFF8h
E2 DataFlash	8 Kbytes	FE00 0000h	FE00 1FFFh

STOP Bit (Forced Processing Stop)

This bit is used to forcibly stop the processing (blank check, block erase, or all-block erase) being executed.
After setting this bit to 1, wait until the FSTATR1.FRDY flag is 1 (processing completed) before setting the OPST bit to 0.

OPST Bit (Processing Start)

This bit is used to execute the command set in the CMD[2:0] bits.
This bit is not set to 0 again even when the processing is completed. Confirm that the FSTATR1.FRDY flag is 1 (processing completed) before setting the OPST bit to 0 again. After that, confirm that the FRDY flag is 0 before executing the next processing.

50.4.10 Flash Extra Area Control Register (FEXCR)

Address(es): FLASH.FEXCR 007F C1DCh

	b7	b6	b5	b4	b3	b2	b1	b0
	OPST	—	—	—	—	CMD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b2 to b0	CMD[2:0]	Software Command Setting	b2 b0 0 0 1: Start-up area information program 0 1 0: Access window information program Settings other than above are prohibited.*1	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	OPST	Processing Start	0: Processing stops. 1: Processing starts.	R/W

Note 1. This does not include set the FEXCR register to 00h when the FSTATR1.EXRDY flag is 1.

Data can be written to the FEXCR register when in ROM P/E mode and the ROM can be programmed/erased.
This register is initialized by a reset or setting the FRESETR.FRESET bit to 1. Data cannot be written to this register while the FRESETR.FRESET bit is 1.
Note that this register cannot be initialized by the FRESETR.FRESET bit while a software command is being executed.

CMD[2:0] Bits (Software Command Setting)

These bits are used to set a software command (start-up area information program or access window information program).
The details of each command are described below.
[Start-up area information program]
This command is used to switch the start-up area used for start-up program protection.

- When setting the start-up area to the default area
  Set registers FWB0, FWB1, FWB2, and FWB3 to FFFFh, and execute this command.
- When setting the start-up area to the alternative area
  Set the FWB0 register to FEFFh, set registers FWB1, FWB2, and FWB3 to FFFFh, and execute this command.

When registers FWB0, FWB1, FWB2, and FWB3 are set to values other than the above, do not execute the start-up area information program.
[Access window information program]
This command is used to set the access window used for area protection.
Set the access window in block units.
Specify the access window start address, which is the beginning address of the access window in the FWB0 register, specify the access window end address, which is the next address of the last address of the access window in the FWB1 register, and issue this command. Set bit 21 to bit 10 of the address for programming/erasure in each register.
If the same value is set as the start address and end address, all areas can be accessed. Do not set the start address to a value larger than the value of the end address.

OPST Bit (Processing Start)

This bit is used to execute the command set in the CMD[2:0] bits.
This bit is not set to 0 again even when the processing is completed. Confirm that the FSTATR1.EXRDY flag is 1 (processing completed) before setting the OPST bit to 0 again. After that, confirm that the FSTATR1.EXRDY flag is 0 before executing the next processing.

Writing to the extra area is started by writing 1 to the OPST bit. Do not write to the CMD[2:0] bits while a software command is being executed.

50.4.11 Flash Processing Start Address Register H (FSARH)

Address(es): FLASH.FSARH 007F C110h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
								—	—	—	—					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The FSARH register is used to set the target processing address or the start address of the target processing range in the flash memory when a software command is executed.
Set bit 31 to bit 25 and bit 20 to bit 16 of the flash memory address for programming/erasure in this register.
Data can be written to this register in ROM P/E mode or E2 DataFlash P/E mode.
This register is initialized by a reset or setting the FRESETR.FRESET bit to 1. Data cannot be written to this register while the FRESETR.FRESET bit is 1.
If this register is read while executing a software command set by the FEXCR register, an undefined value is read.
Refer to Figure 50.1 and Figure 50.2 for details on the addresses of the flash memory.

50.4.12 Flash Processing Start Address Register L (FSARL)

Address(es): FLASH.FSARL 007F C108h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The FSARL register is used to set the target processing address or the start address of the target processing range in the flash memory when a software command is executed.
Set bit 15 to bit 0 of the flash memory address for programming/erasure in this register.
When the target is the ROM, set bit 2 to bit 0 to 000b.
Data can be written to this register in ROM P/E mode or E2 DataFlash P/E mode.
This register is initialized by a reset or setting the FRESETR.FRESET bit to 1. Data cannot be written to this register while the FRESETR.FRESET bit is 1.
This register is incremented by 8h if the ROM is specified and 1h if the E2 DataFlash is specified after a program command is executed. Therefore, it is not necessary to set the target address to be written to this register when executing a program command sequentially.
If this register is read while executing a software command set by the FEXCR register, an undefined value is read.
Refer to Figure 50.1 and Figure 50.2 for details on the addresses of the flash memory.

50.4.13 Flash Processing End Address Register H (FEARH)

Address(es): FLASH.FEARH 007F C120h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
								—	—	—	—					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The FEARH register is used to set the end address of the target processing range in the flash memory when a software command is executed.
Set bit 31 to bit 25 and bit 20 to bit 16 of the flash memory address for programming/erasure in this register.
Data can be written to this register in ROM P/E mode or E2 DataFlash P/E mode.
This register is initialized by a reset or setting the FRESETR.FRESET bit to 1. Data cannot be written to this register while the FRESETR.FRESET bit is 1.
If this register is read while executing a software command set by the FEXCR register, an undefined value is read.
Refer to Figure 50.1 and Figure 50.2 for details on the addresses of the flash memory.

50.4.14 Flash Processing End Address Register L (FEARL)

Address(es): FLASH.FEARL 007F C118h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The FEARH register is used to set the end address of the target range for processing when a software command is executed.
Set bit 15 to bit 0 of the flash memory address for programming/erasure in this register.
When the target is the ROM, set bit 2 to bit 0 to 000b.
Data can be written to this register in ROM P/E mode or E2 DataFlash P/E mode.
This register is initialized by a reset or setting the FRESETR.FRESET bit to 1. Data cannot be written to this register while the FRESETR.FRESET bit is 1.
If this register is read while executing a software command set by the FEXCR register, an undefined value is read.
Refer to Figure 50.1 and Figure 50.2 for details on the addresses of the flash memory.

50.4.15 Flash Write Buffer Register n (FWBn) (n = 0 to 3)

Address(es): FLASH.FWB0 007F C130h, FLASH.FWB1 007F C138h, FLASH.FWB2 007F C140h, FLASH.FWB3 007F C144h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register is used to set the data for programming the ROM, E2 DataFlash, or extra area. The data can be written in ROM P/E mode or E2 DataFlash P/E mode.

This register is initialized by a reset or setting the FRESETR.FRESET bit to 1. Data cannot be written to this register while the FRESETR.FRESET bit is 1.

The read value of this register is undefined while executing a software command set by the FCR register or the FEXCR register.

When programming the extra area, set the 4-byte data for programming in registers FWB0 and FWB1.

When programming the E2 DataFlash, set the data for programming in the lower 8 bits in the FWB0 register.

When programming the ROM, set the 8-byte data for programming in registers FWB0 to FWB3. Figure 50.3 shows the relationship between the addresses indicated by registers FSARH and FSARL and the data set in the FWBn register.

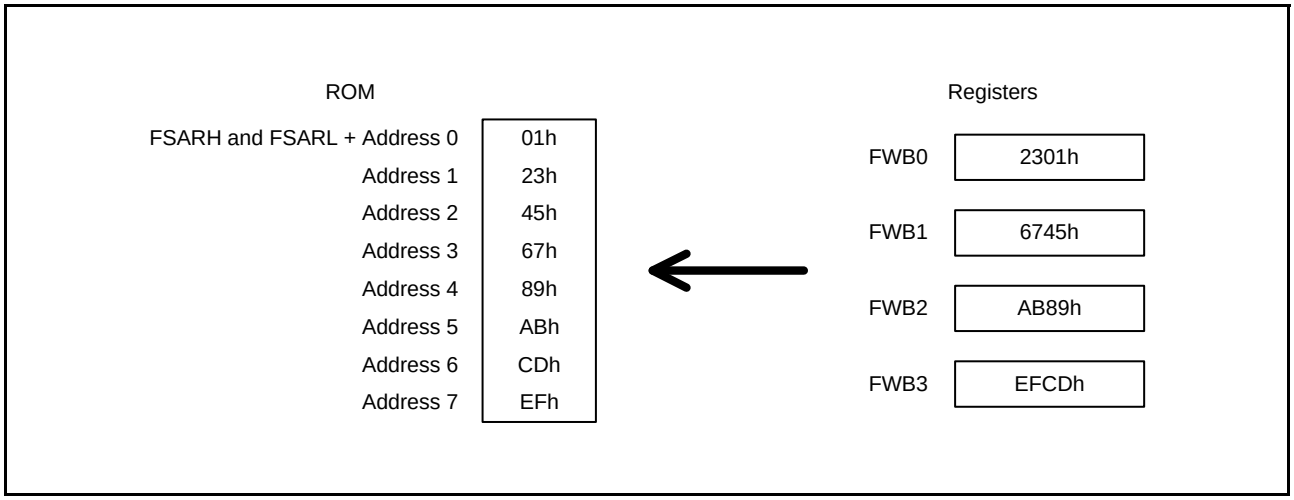


Figure 50.3 FWBn Register Setting Values and Data Allocation in the ROM

50.4.16 Flash Status Register 0 (FSTATR0)

Address(es): FLASH.FSTATR0 007F C1F0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	EILGLERR	ILGLERR	BCERR	—	PRGERR	ERERR
Value after reset:	x	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	ERERR	Erase Error Flag	0: Erasure terminates normally. 1: An error occurs during erasure.	R
b1	PRGERR	Program Error Flag	0: Programming terminates normally. 1: An error occurs during programming.	R
b2	—	Reserved	The read value is undefined.	R
b3	BCERR	Blank Check Error Flag	0: Blank checking terminates normally. 1: An error occurs during blank checking.	R
b4	ILGLERR	Illegal Command Error Flag	0: No illegal software command or illegal access is detected. 1: An illegal command or illegal access is detected.	R
b5	EILGLERR	Extra Area Illegal Command Error Flag	0: No illegal command or illegal access to the extra area is detected. 1: An illegal command or illegal access to the extra area is detected.	R
b7, b6	—	Reserved	The read value is undefined.	R

This register is a status register used to confirm the result of executing a software command. Each error flag is set to 0 when the next software command is executed.

ERERR Flag (Erase Error Flag)

This flag indicates the result of the erase processing for the ROM/E2 DataFlash.
[Setting condition]

- An error occurs during erasure.

[Clearing condition]

- The next software command is executed.
  The value read from this flag is undefined when the FCR.STOP bit is set to 1 (processing is forcibly stopped) during erasure.

PRGERR Flag (Program Error Flag)

This flag indicates the result of the program processing for the ROM/E2 DataFlash.
[Setting condition]

- An error occurs during programming.

[Clearing condition]

- The next software command is executed.

BCERR Flag (Blank Check Error Flag)

This flag indicates the result of the blank check processing for the ROM/E2 DataFlash.
[Setting condition]

- An error occurs during blank checking.

[Clearing condition]

- The next software command is executed.
  The value read from this flag is undefined when the FCR.STOP bit is set to 1 (processing is forcibly stopped) during blank checking.

ILGLERR Flag (Illegal Command Error Flag)

This flag indicates the result of executing a software command.
[Setting conditions]

- Programming/erasure is executed to an area other than the access window range.
- A blank check or block erase command is executed when the set value of registers FSARH and FSARL is larger than the set value of registers FEARH and FEARL.
- Program and block erase commands are executed when the FASR.EXS bit is 1.
- An all-block erase command is executed while the access window is set.
- An all-block erase command is executed without setting registers FSARH and FSARL and registers FEARH and FEARL properly.
- The E2 DataFlash address is set in registers FSARH and FSARL and a software command is executed when the ROM is in P/E mode.
- The ROM address is set in registers FSARH and FSARL and a software command is executed when the E2 DataFlash is in P/E mode.
- The ROM and E2 DataFlash are set to P/E mode and a software command is executed.

[Clearing condition]

- The next software command is executed.

EILGLERR Flag (Extra Area Illegal Command Error Flag)

This flag indicates the result of executing a software command for the extra area.
[Setting condition]

- A software command for the extra area is executed when the FASR.EXS bit is 0.

[Clearing condition]

- The next software command is executed.

50.4.17 Flash Status Register 1 (FSTATR1)

Address(es): FLASH.FSTATR1 007F C12Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	EXRDY	FRDY	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0.	R
b2	—	Reserved	This bit is read as 1.	R
b5 to b3	—	Reserved	These bits are read as 0.	R
b6	FRDY	Flash Ready Flag	0: Other than below 1: 00h can be written to the FCR register (processing to complete the software command).	R
b7	EXRDY	Extra Area Ready Flag	0: Other than below 1: 00h can be written to the FEXCR register (processing to complete the software command).	R

This register is a status register used to confirm the result of executing a software command. Each flag is set to 0 when the next software command is executed.

FRDY Flag (Flash Ready Flag)

This flag is used to confirm whether a software command is executed.
This flag becomes 1 when processing of the executed software command or the forced stop processing is completed, and this flag becomes 0 when setting the FCR.OPST bit to 0.
Also, an interrupt (FRDYI) is generated when this flag becomes 1.

EXRDY Flag (Extra Area Ready Flag)

This flag is used to confirm whether a software command for the extra area is executed.
This flag is set to 1 when processing of the executed software command is completed, and 0 when the FEXCR.OPST bit is set to 0.
Also, an interrupt (FRDYI) is generated when this flag becomes 1.

50.4.18 Flash Error Address Monitor Register H (FEAMH)

Address(es): FLASH.FEAMH 007F C1E8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
								—	—	—	—					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register is used to check the address where the error has occurred if an error occurs during processing of a software command. This register stores bit 31 to bit 25 and bit 20 to bit 16 of the address where the error has occurred for the program command or blank check command, or it stores bit 31 to bit 25 and bit 20 to bit 16 of the beginning address of the area where the error has occurred for the block erase command or all-block erase command.
Since this register value becomes undefined if setting the FRESETR.FRESET bit to 1, read the value before error processing.
If the software command terminates normally, this register stores bit 31 to bit 25 and bit 20 to bit 16 of the end address at execution of the command.
Refer to Figure 50.1 and Figure 50.2 for details on the addresses of the flash memory.

50.4.19 Flash Error Address Monitor Register L (FEAML)

Address(es): FLASH.FEAML 007F C1E0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register is used to check the address where the error has occurred if an error occurs during processing of a software command. This register stores bit 15 to bit 0 of the address where the error has occurred for the program command or blank check command, or it stores bit 15 to bit 0 of the beginning address of the area where the error has occurred for the block erase command or all-block erase command.
Since this register value becomes undefined if setting the FRESETR.FRESET bit to 1, read the value before error processing.
When the software command is normally completed, this register stores bit 15 to bit 0 of the last address at execution of the command.
When executing a software command for the ROM, lower 3 bits become 000b.
Refer to Figure 50.1 and Figure 50.2 for details on the addresses of the flash memory.

50.4.20 Flash Start-Up Setting Monitor Register (FSCMR)

Address(es): FLASH.FSCMR 007F C1C0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SASMF	—	—	—	—	—	—	—	—
Value after reset:	0	1	1	1	0	1	1	Value set by user*1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0.	R
b8	SASMF	Start-Up Area Setting Monitor Flag	0: Setting to start up using the alternative area 1: Setting to start up using the default area	R
b10, b9	—	Reserved	These bits are read as 1. Writing to these bits has no effect.	R
b11	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R
b14 to b12	—	Reserved	These bits are read as 1. Writing to these bits has no effect.	R
b15	—	Reserved	This bit is read as 0. Writing to this bit has no effect.	R

Note 1. The value of the blank product is 1. It is set to the same value set in bit 8 in the FWB1 register after the start-up area information program command is executed.

SASMF Flag (Start-Up Area Setting Monitor Flag)

This flag is used to confirm the settings of the start-up area.

When this flag is 0, the user program is set to start up using the alternative area.

When this flag is 1, the user program is set to start up using the default area.

50.4.21 Flash Access Window Start Address Monitor Register (FAWSMR)

Address(es): FLASH.FAWSMR 007F C1C8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—												
Value after reset:	0	0	0	0	The value set by the user*1											

Note 1. The value of the blank product is 1. It is set to the same value set in bit 11 to bit 0 the FWB0 register after the access window information program command is executed.

This register is used to confirm the set value of the access window start address used for area protection.

50.4.22 Flash Access Window End Address Monitor Register (FAWEMR)

Address(es): FLASH.FAWEMR 007F C1D0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—												
Value after reset:	0	0	0	0	The value set by the user*1											

Note 1. The value of the blank product is 1. It is set to the same value set in bit 11 to bit 0 in the FWB1 register after the access window information program command is executed.

This register is used to confirm the set value of the access window end address used for area protection.

50.4.23 Unique ID Register n (UIDRn) (n = 0 to 3)

Address(es): FLASHCONST.UIDR0 007F C350h, FLASHCONST.UIDR1 007F C354h, FLASHCONST.UIDR2 007F C358h, FLASHCONST.UIDR3 007F C35Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	Unique value for each chip															

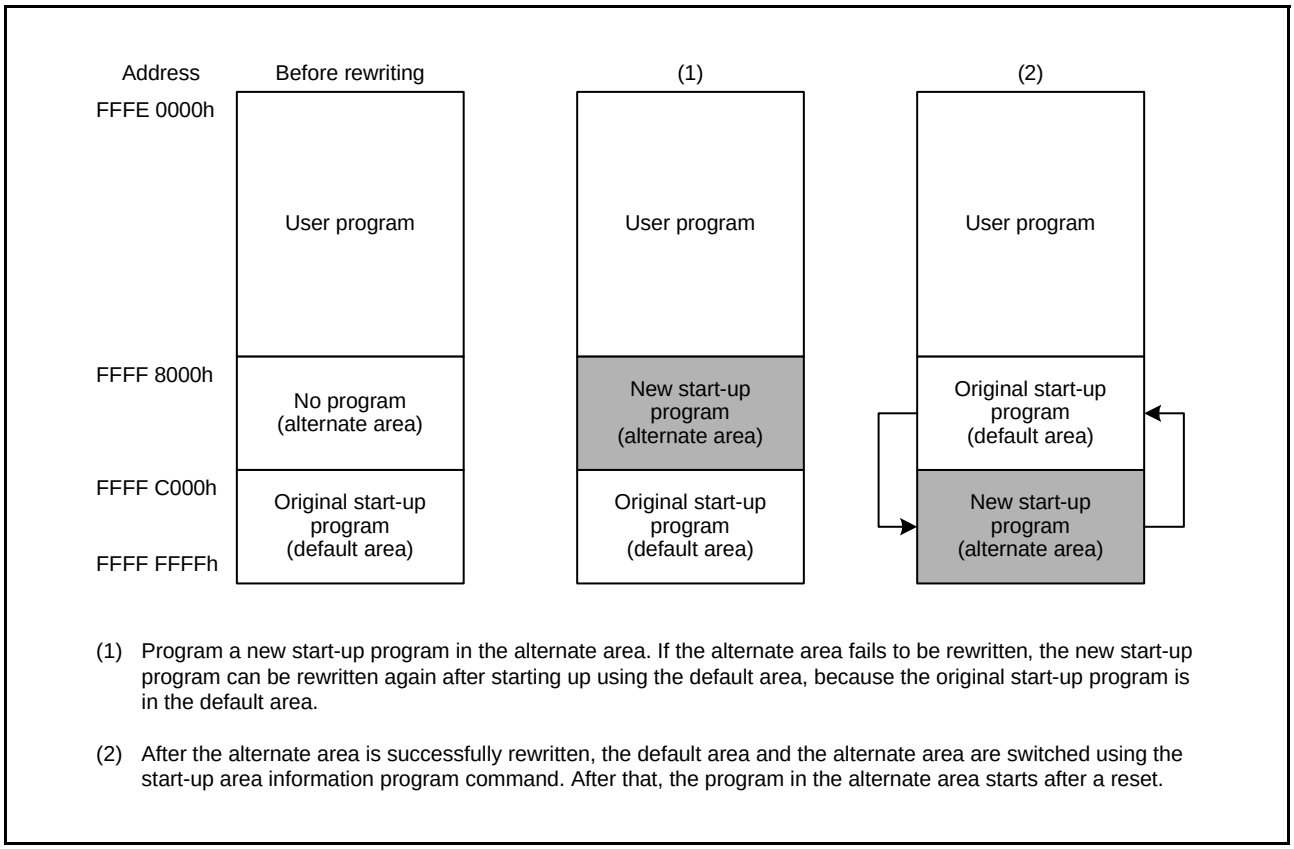
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	Unique value for each chip															

The UIDRn register stores a 16-byte ID code (unique ID) for identifying the individual MCU.
The unique ID is stored in the extra area of the flash memory and cannot be rewritten by the user.

50.5 Start-Up Program Protection

When rewriting the start-up program*1 by self-programming, if the rewrite operation is interrupted due to temporary blackout, the start-up program may not be successfully programmed and the user program may not start properly. This problem can be avoided by rewriting the start-up program without erasing the existing start-up program using the start-up program protection. This function is available in products with a 32-Kbyte or larger ROM.
Figure 50.4 shows the Overview of the Start-Up Program Protection. In this figure, the default area indicates block 0 to block 7, and the alternate area indicates block 8 to block 15.

Note 1. Program to perform operation to start the user program. It includes the fixed vector table.



(1) Program a new start-up program in the alternate area. If the alternate area fails to be rewritten, the new start-up program can be rewritten again after starting up using the default area, because the original start-up program is in the default area.

(2) After the alternate area is successfully rewritten, the default area and the alternate area are switched using the start-up area information program command. After that, the program in the alternate area starts after a reset.

Figure 50.4 Overview of the Start-Up Program Protection

50.6 Area Protection

Area protection enables rewriting only the selected blocks (access window) in the user area and disables rewriting the other blocks during self-programming. The access window cannot be set in the data area.
Specify the start address and end address to set the access window. While the access window can be set in boot mode or by self-programming, area protection is enabled only during self-programming in single-chip mode.
Figure 50.5 shows the Area Protection Overview (When Blocks 4 to 6 are Set as the Access Window in Products with 128-Kbyte ROM).

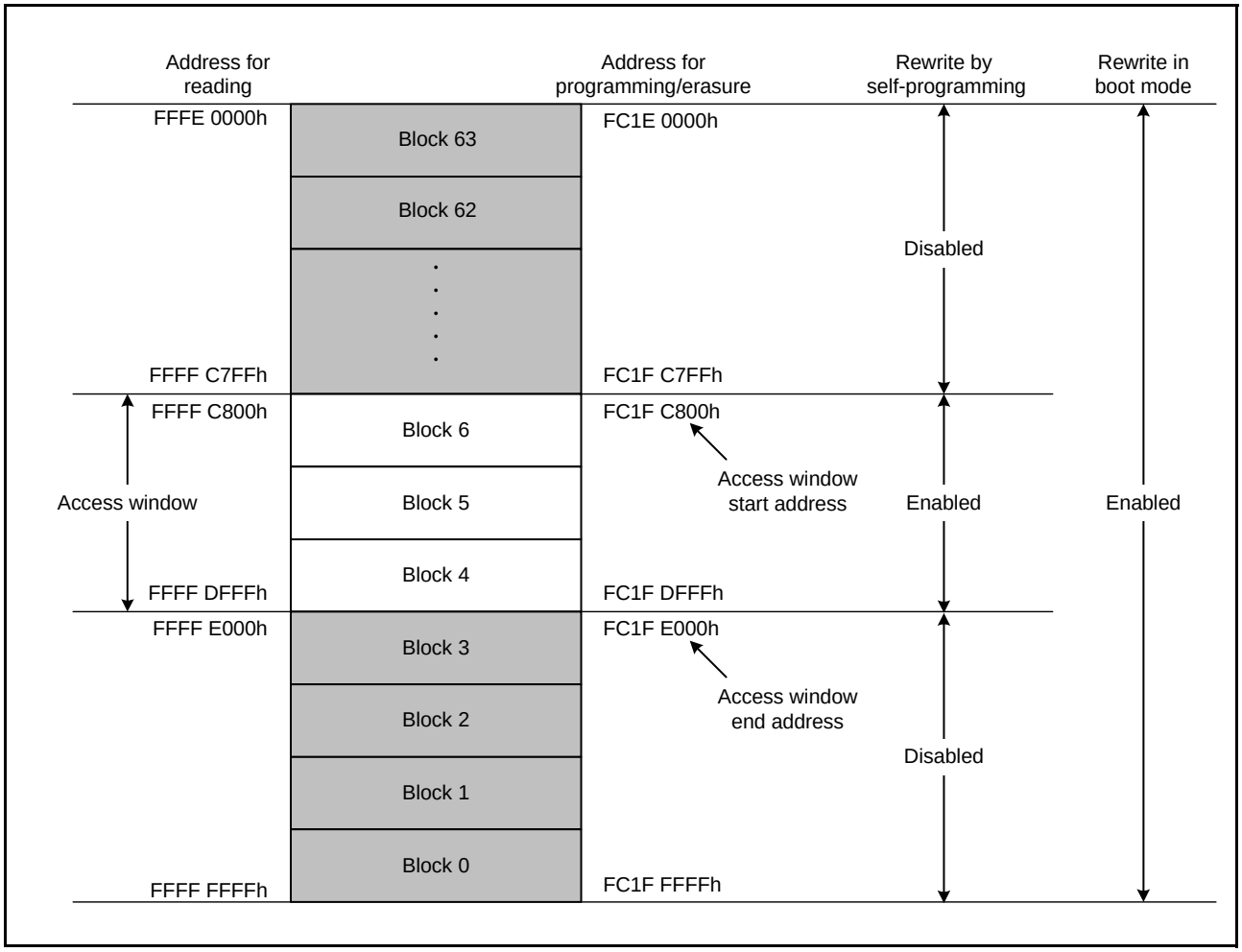


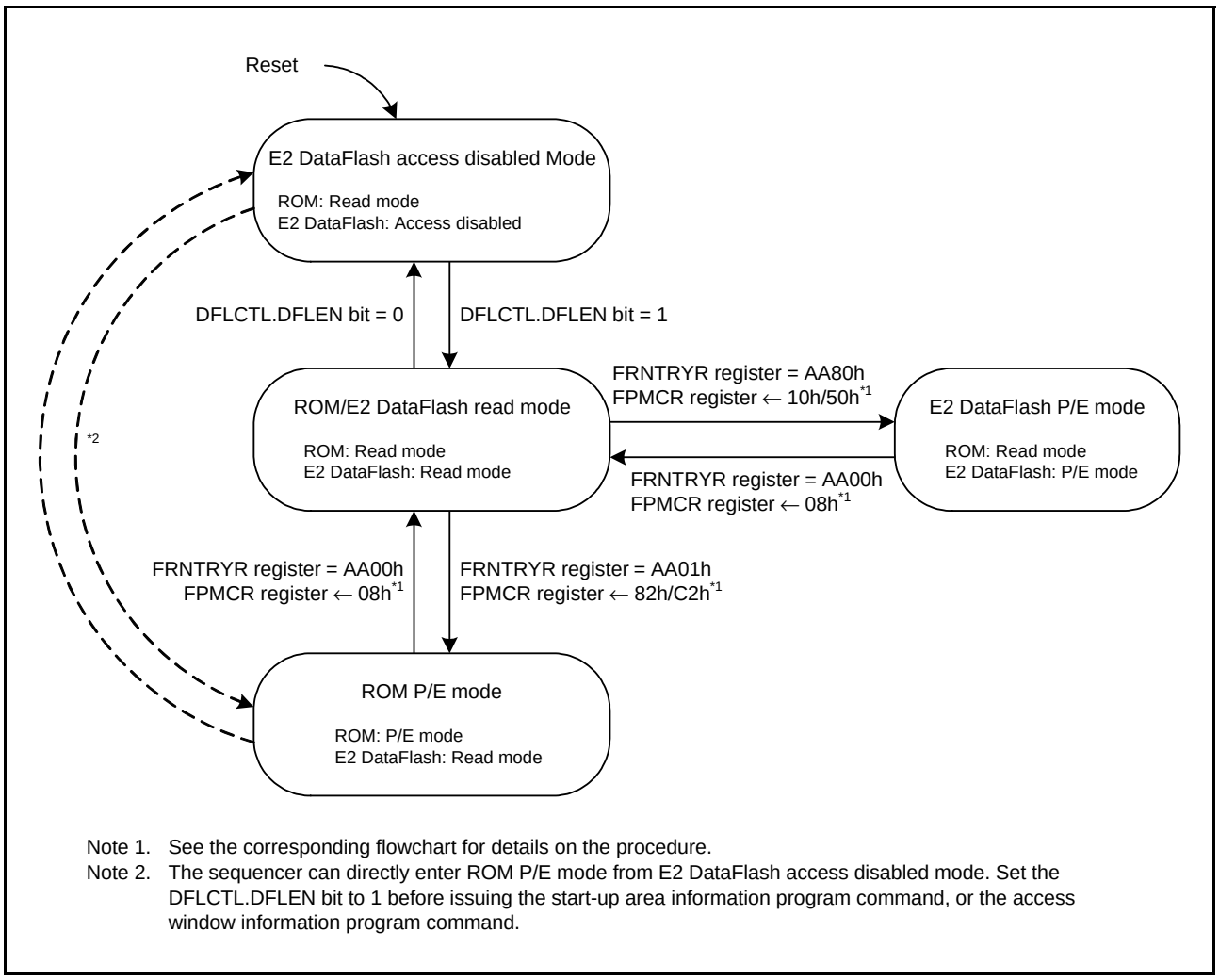
Figure 50.5 Area Protection Overview (When Blocks 4 to 6 are Set as the Access Window in Products with 128-Kbyte ROM)

50.7 Programming and Erasure

The ROM and E2 DataFlash can be programmed and erased by changing the mode of the dedicated sequencer for programming and erasure, and by issuing commands for programming and erasure.
The mode transitions and commands required to program or erase the ROM and E2 DataFlash are described below. The descriptions apply in common to boot mode and single-chip mode.

50.7.1 Sequencer Modes

The sequencer has four modes. Transitions between modes are caused by writing to the DFLCTL and FENTRYR registers and setting the FPMCR register. Figure 50.6 is a diagram of mode transitions of the flash memory.



Note 1. See the corresponding flowchart for details on the procedure.
Note 2. The sequencer can directly enter ROM P/E mode from E2 DataFlash access disabled mode. Set the DFLCTL.DFLEN bit to 1 before issuing the start-up area information program command, or the access window information program command.

Figure 50.6 Mode Transitions of the Flash Memory

50.7.1.1 E2 DataFlash Access Disabled Mode

In E2 DataFlash access disabled mode, access to the E2 DataFlash is disabled. After a reset, the sequencer enters this mode.
When setting the DFLCTL.DFLEN bit to 1, the E2 DataFlash is placed in read mode.

50.7.1.2 Read Mode

Read mode is for high-speed reading of the ROM/E2 DataFlash. Reading from a ROM address for reading can be accomplished in one ICLK clock.

(1) ROM/E2 DataFlash Read Mode

In this mode, both the ROM and E2 DataFlash are in read mode. The sequencer enters this mode from P/E mode when setting the FPMCR register to 08h, setting the FENTRYR.FENTRYD bit to 0, and setting the FENTRYR.FENTRY0 bit to 0.

50.7.1.3 P/E Modes

The P/E mode is for programming and erasure of the ROM/E2 DataFlash.

(1) ROM P/E Mode

In this mode, the ROM is in P/E mode, and the E2 DataFlash is in read mode. The sequencer enters this mode when setting the FENTRYR.FENTRYD to 0, setting the FENTRYR.FENTRY0 bit to 1, and setting the FPMCR register 82h or C2h.

(2) E2 DataFlash P/E Mode

In this mode, the ROM is in read mode, and the E2 DataFlash is in P/E mode. The sequencer enters this mode when the setting the FENTRYR.FENTRYD to 1, setting the FENTRYR.FENTRY0 bit to 0, and setting the FPMCR register 10h or 50h.

50.7.2 Mode Transitions

50.7.2.1 Transition from E2 DataFlash Access Disable Mode to Read Mode

Reading of the E2 DataFlash requires switching from E2 DataFlash access disabled mode to ROM/E2 DataFlash read mode.

Set the DFLCTL.DFLEN bit to 1 to switch to ROM/E2 DataFlash read mode.

Figure 50.7 shows the Procedure for Transition from E2 DataFlash Access Disabled Mode to ROM/E2 DataFlash Read Mode.

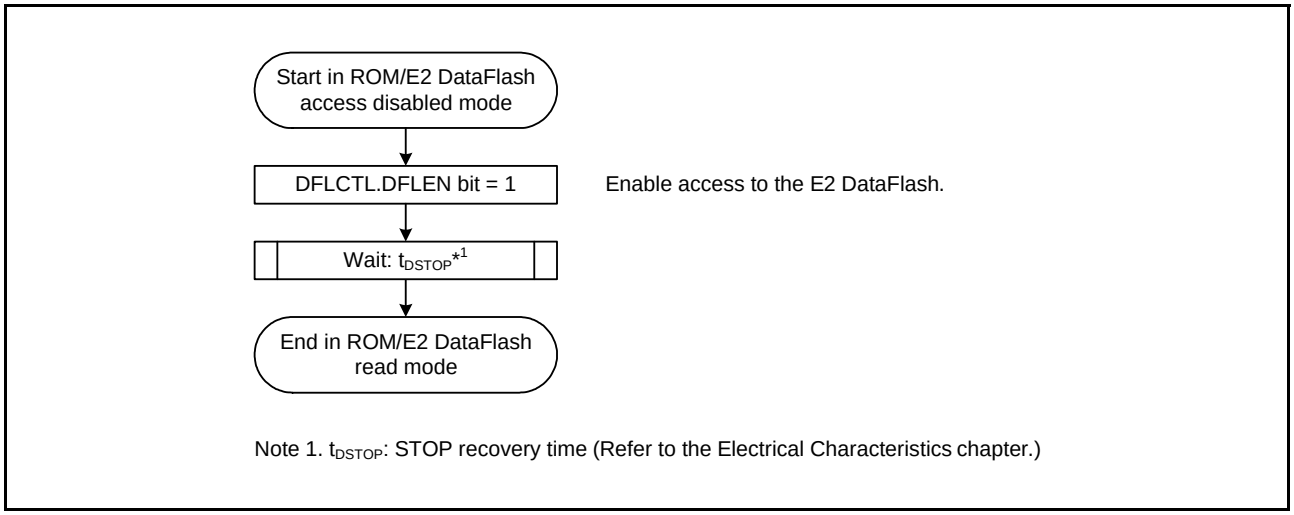
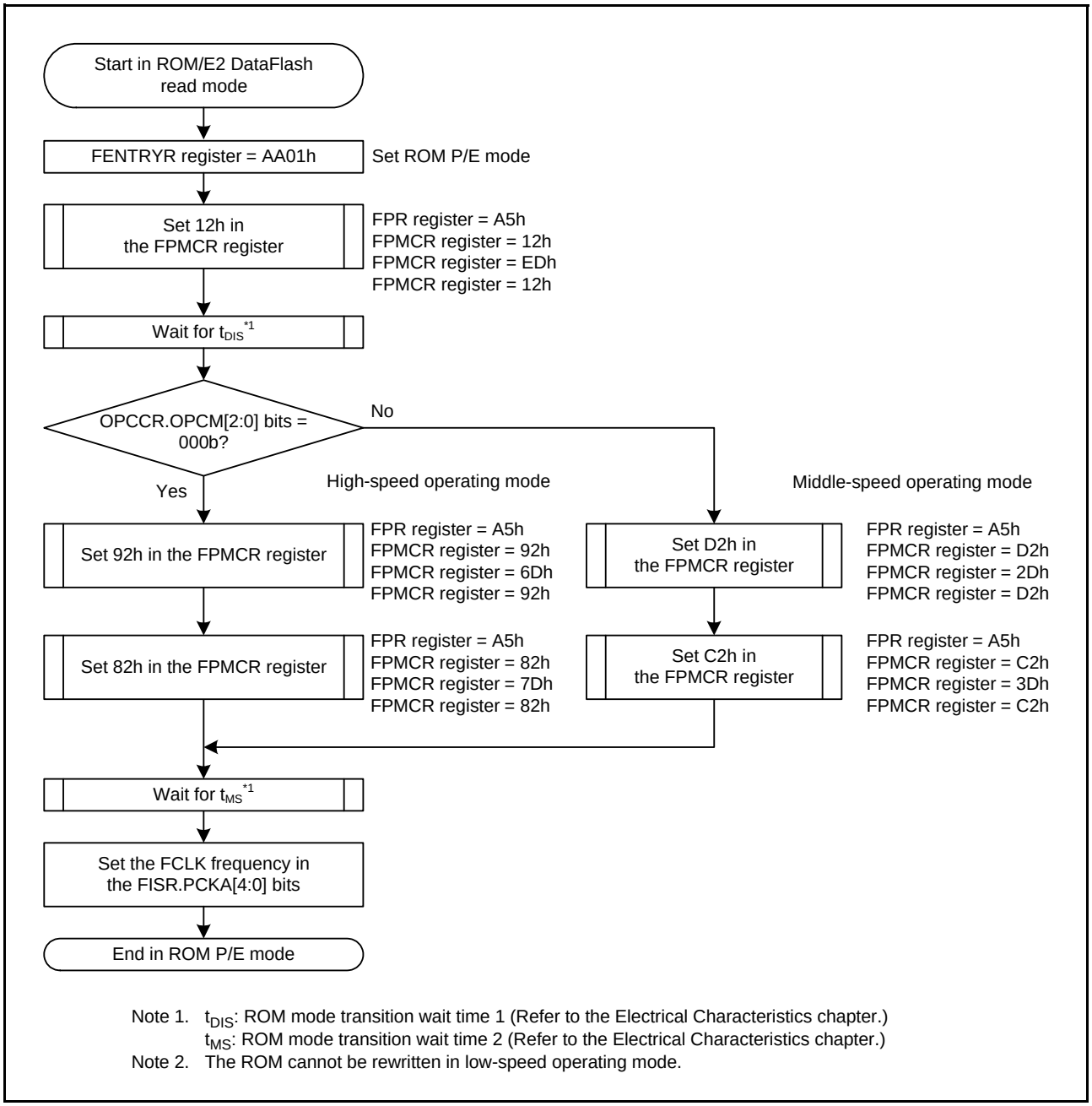


Figure 50.7 Procedure for Transition from E2 DataFlash Access Disabled Mode to ROM/E2 DataFlash Read Mode

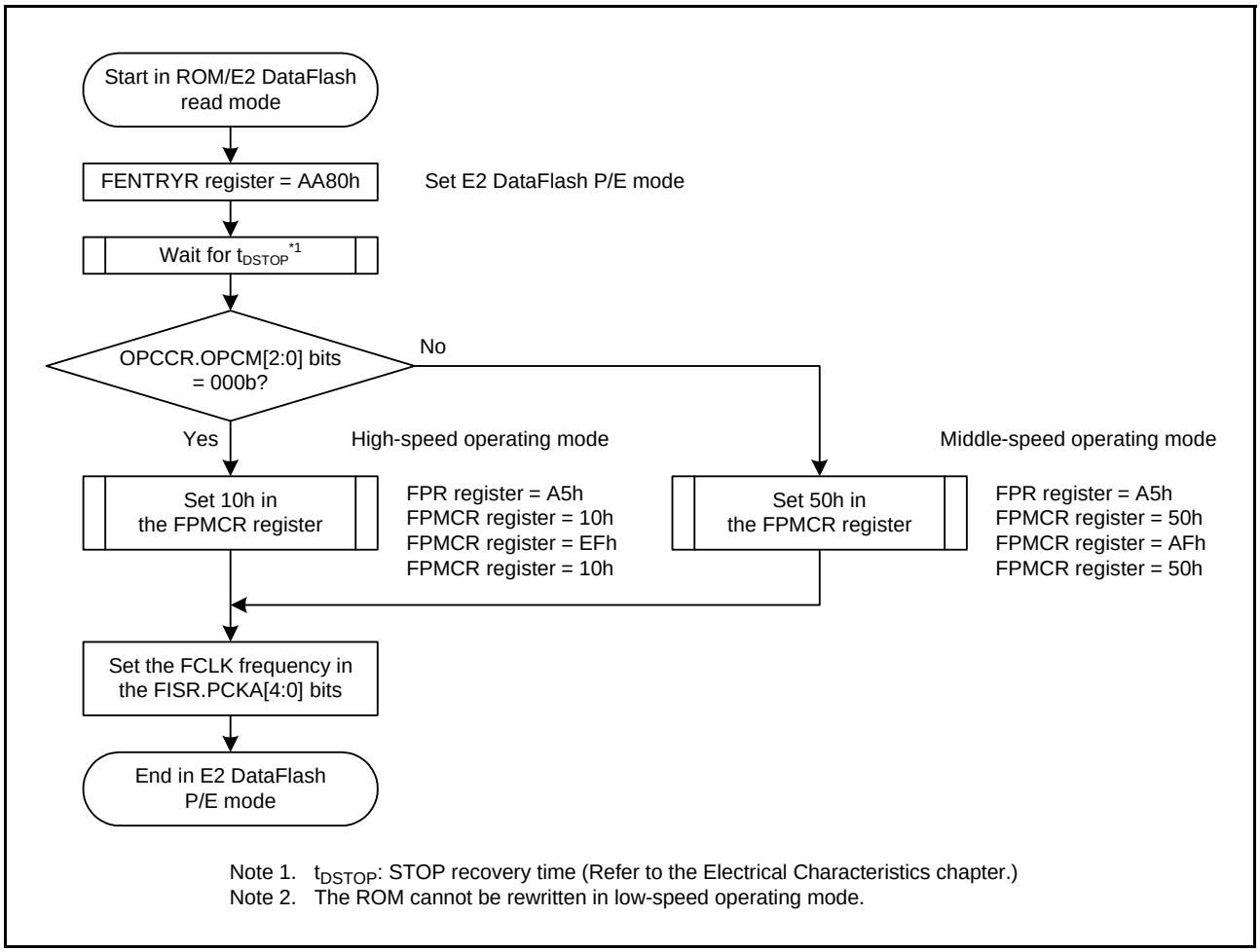
50.7.2.2 Transition from Read Mode to P/E Mode

Switching to ROM P/E mode is required before executing a software command for the ROM.
Figure 50.8 shows the Procedure for Transition from ROM/E2 DataFlash Read Mode to ROM P/E Mode. Figure 50.9 shows the Procedure for Transition from ROM/E2 DataFlash Read Mode to E2 DataFlash P/E Mode.



Note 1. t_{DIS}: ROM mode transition wait time 1 (Refer to the Electrical Characteristics chapter.)
t_{MS}: ROM mode transition wait time 2 (Refer to the Electrical Characteristics chapter.)
Note 2. The ROM cannot be rewritten in low-speed operating mode.

Figure 50.8 Procedure for Transition from ROM/E2 DataFlash Read Mode to ROM P/E Mode

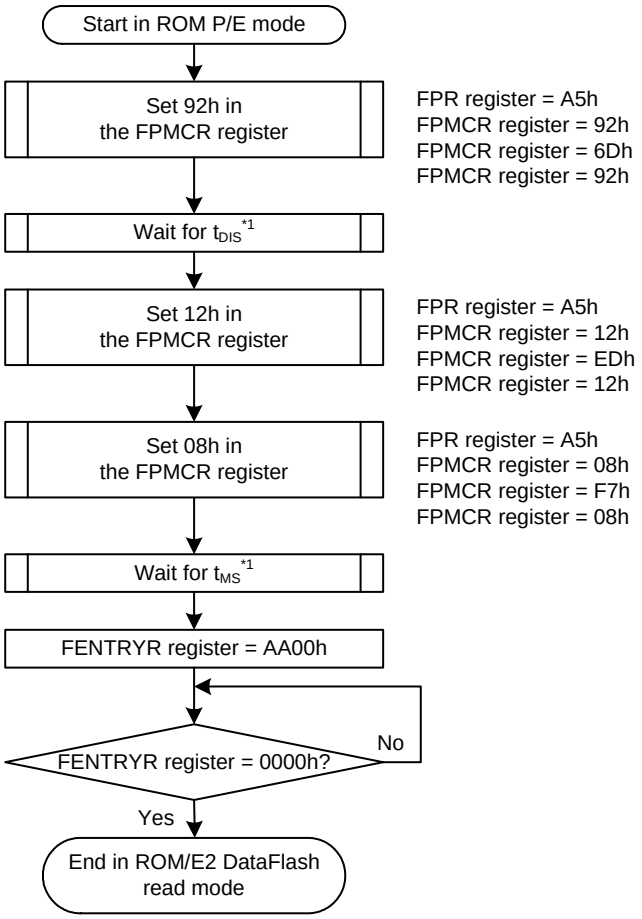


Note 1. t_{DSTOP}: STOP recovery time (Refer to the Electrical Characteristics chapter.)
Note 2. The ROM cannot be rewritten in low-speed operating mode.

Figure 50.9 Procedure for Transition from ROM/E2 DataFlash Read Mode to E2 DataFlash P/E Mode

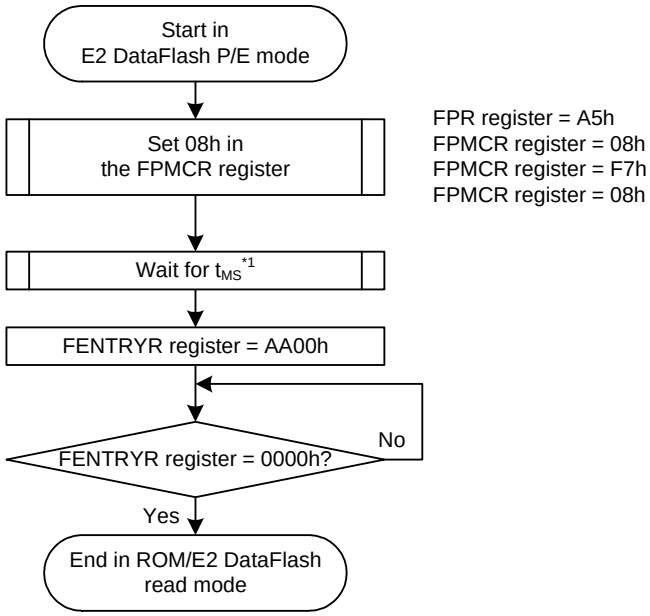
50.7.2.3 Transition from P/E Mode to Read Mode

High-speed reading of the ROM requires switching to ROM/E2 DataFlash read mode.
Figure 50.10 shows the Procedure for Transition from ROM P/E Mode to ROM/E2 DataFlash Read Mode. Figure 50.11 shows the Procedure for Transition from E2 DataFlash P/E Mode to ROM/E2 DataFlash Read Mode.



Note 1. t_{DIS}: ROM mode transition wait time 1 (Refer to the Electrical Characteristics chapter.)
t_{MS}: ROM mode transition wait time 2 (Refer to the Electrical Characteristics chapter.)

Figure 50.10 Procedure for Transition from ROM P/E Mode to ROM/E2 DataFlash Read Mode



Note 1. t_{MS}: ROM mode transition wait time 2 (Refer to the Electrical Characteristics chapter.)

Figure 50.11 Procedure for Transition from E2 DataFlash P/E Mode to ROM/E2 DataFlash Read Mode

50.7.3 Software Commands

Software commands consist of commands for programming and erasure and commands for programming start-up program area information and access window information. Table 50.5 lists the software commands for use with the flash memory.

Table 50.5 Software Commands

Command	Function
Program	• ROM programming (8 bytes) • E2 DataFlash programming (1 byte)
Block erase	ROM/E2 DataFlash erasure
All-block erase	Erasure of all blocks in the ROM/E2 DataFlash
Blank check	Check whether the specified area is blank. Confirm that data is not programmed in the area. This command does not guarantee whether the area remains erased.
Start-up area information program	Rewrite the start-up area switching information used for start-up program protection.
Access window information program	Set the access window used for area protection.

50.7.4 Software Command Usage

This section describes how to use each software command, using flowcharts.

50.7.4.1 Program

Figure 50.12 and Figure 50.13 show the procedure to issue the program command.

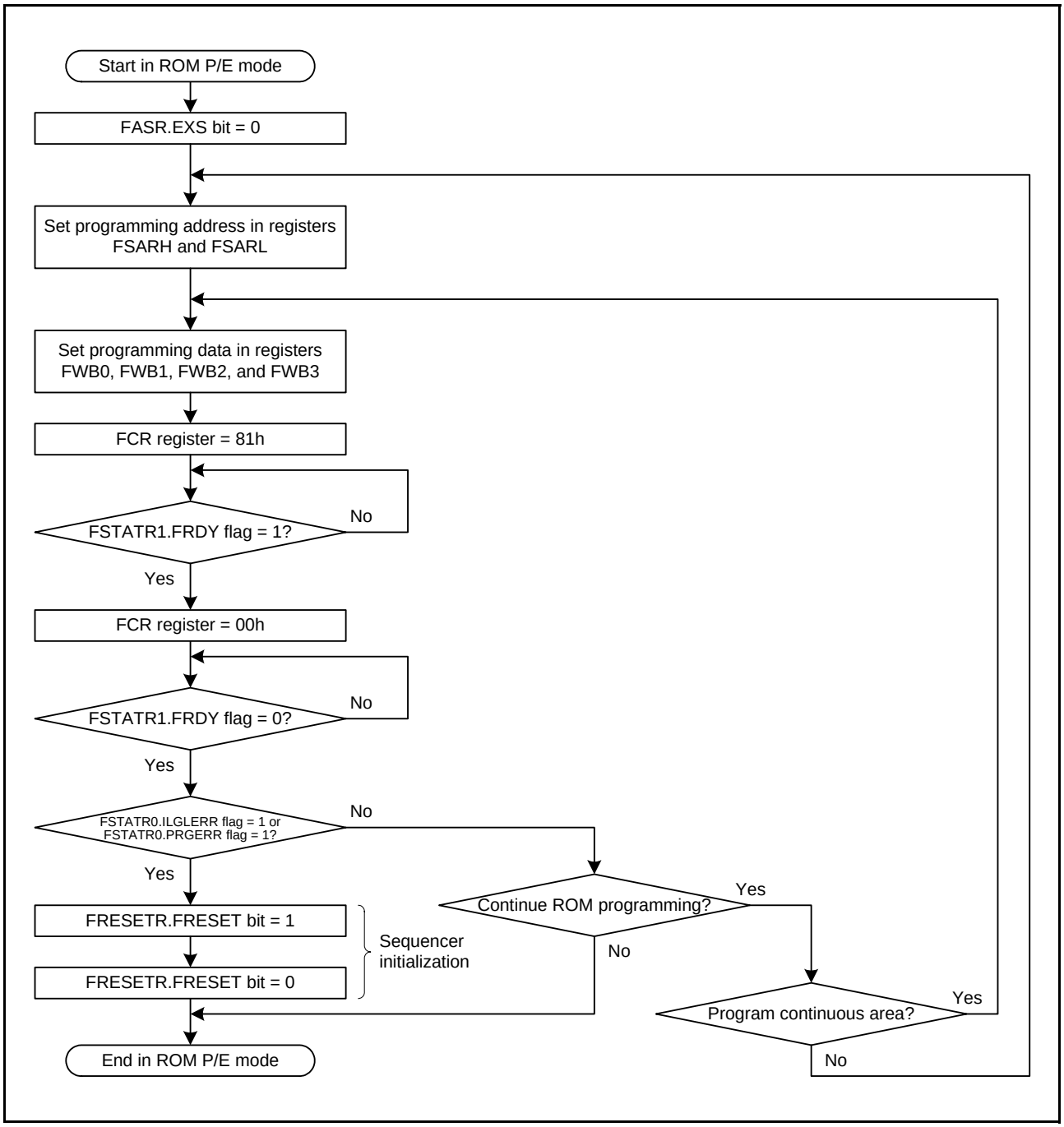


Figure 50.12 Procedure to Issue the Program Command for the ROM

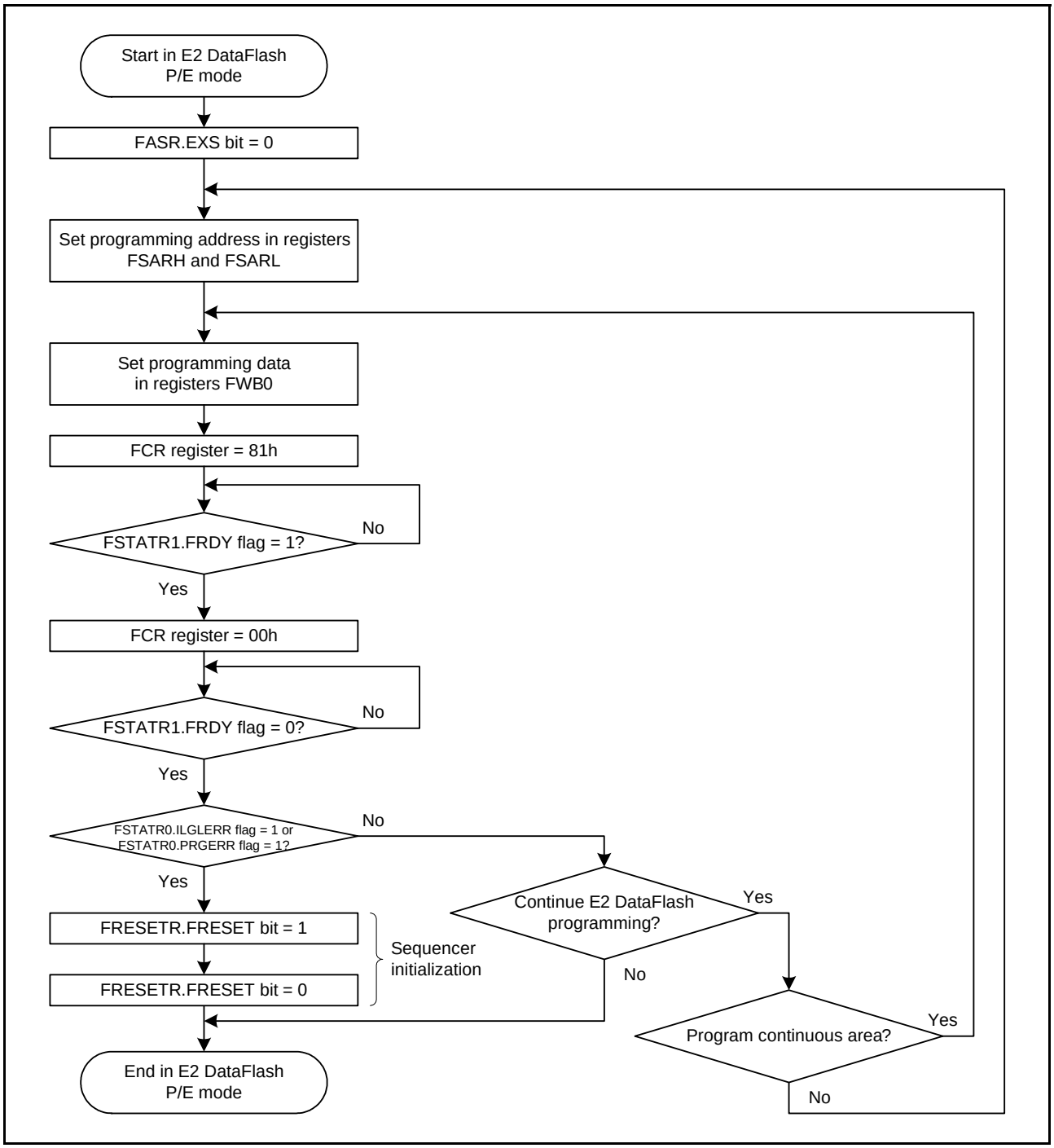


Figure 50.13 Procedure to Issue the Program Command for the E2 DataFlash

50.7.4.2 Block Erase

Figure 50.14 and Figure 50.15 show the procedure to issue the block erase command.

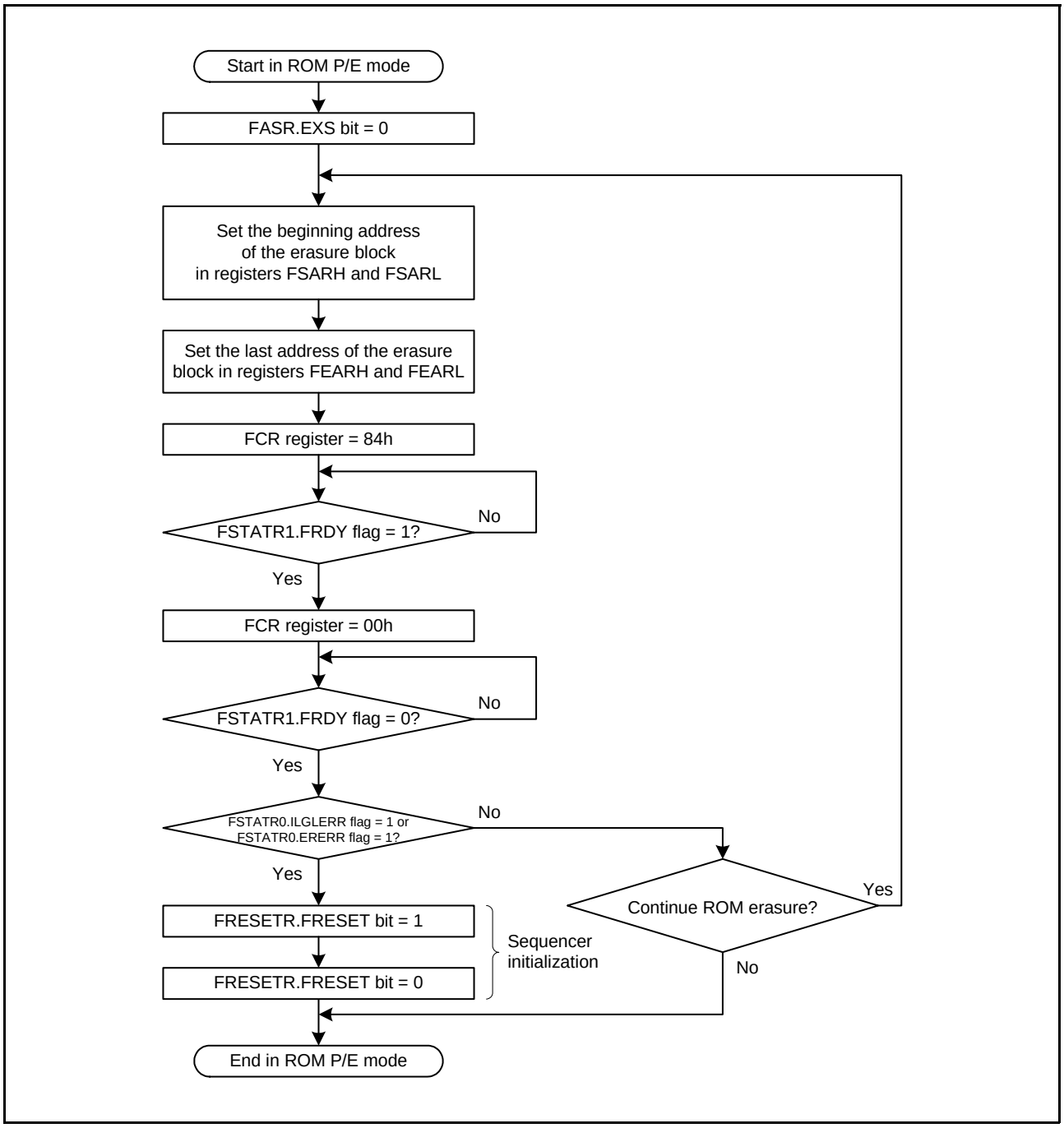


Figure 50.14 Procedure to Issue the Block Erase Command for the ROM

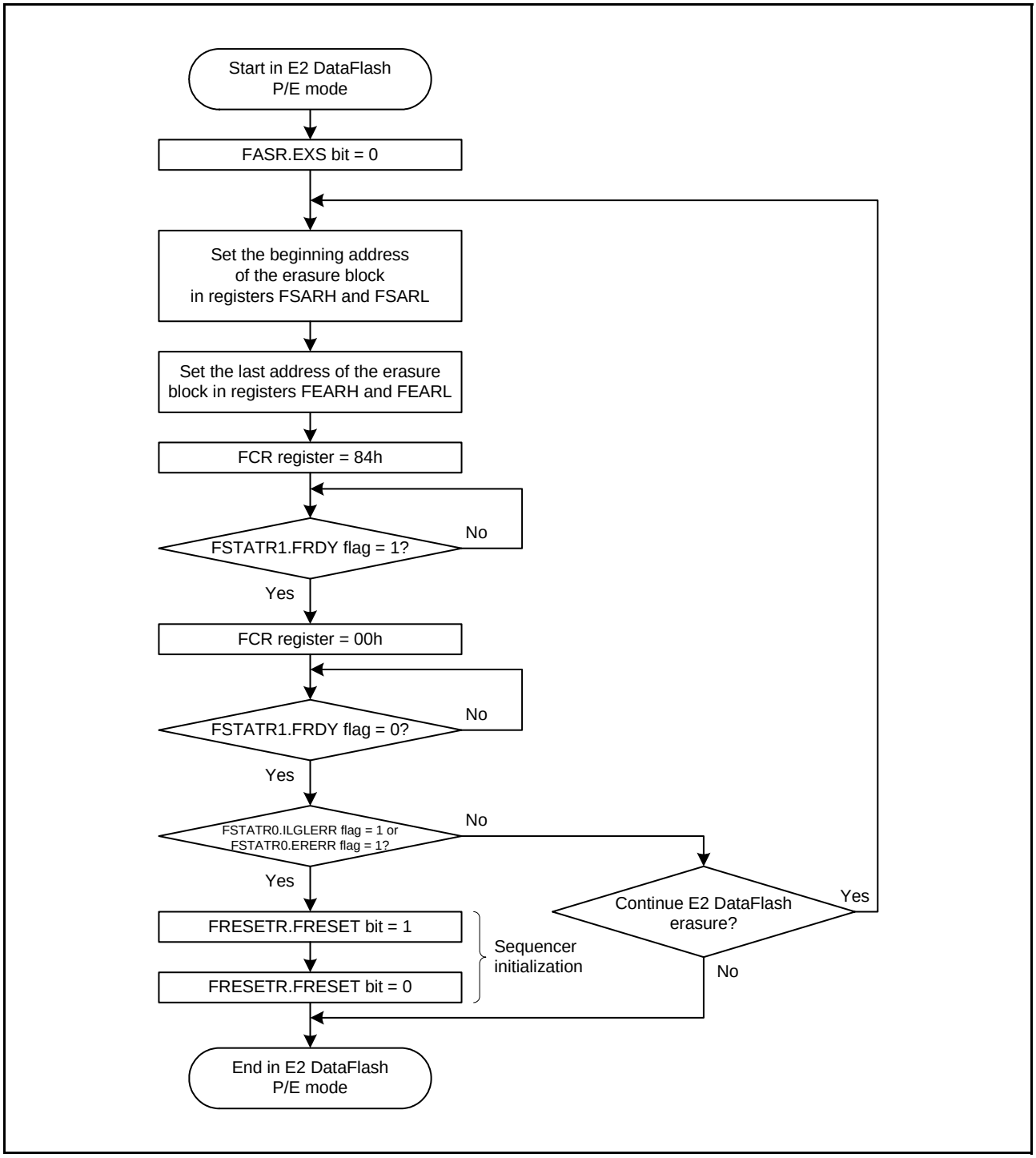


Figure 50.15 Procedure to Issue the Block Erase Command for the E2 DataFlash

50.7.4.3 All-Block Erase

Figure 50.16 and Figure 50.17 show the procedure to issue the all-block erase command.

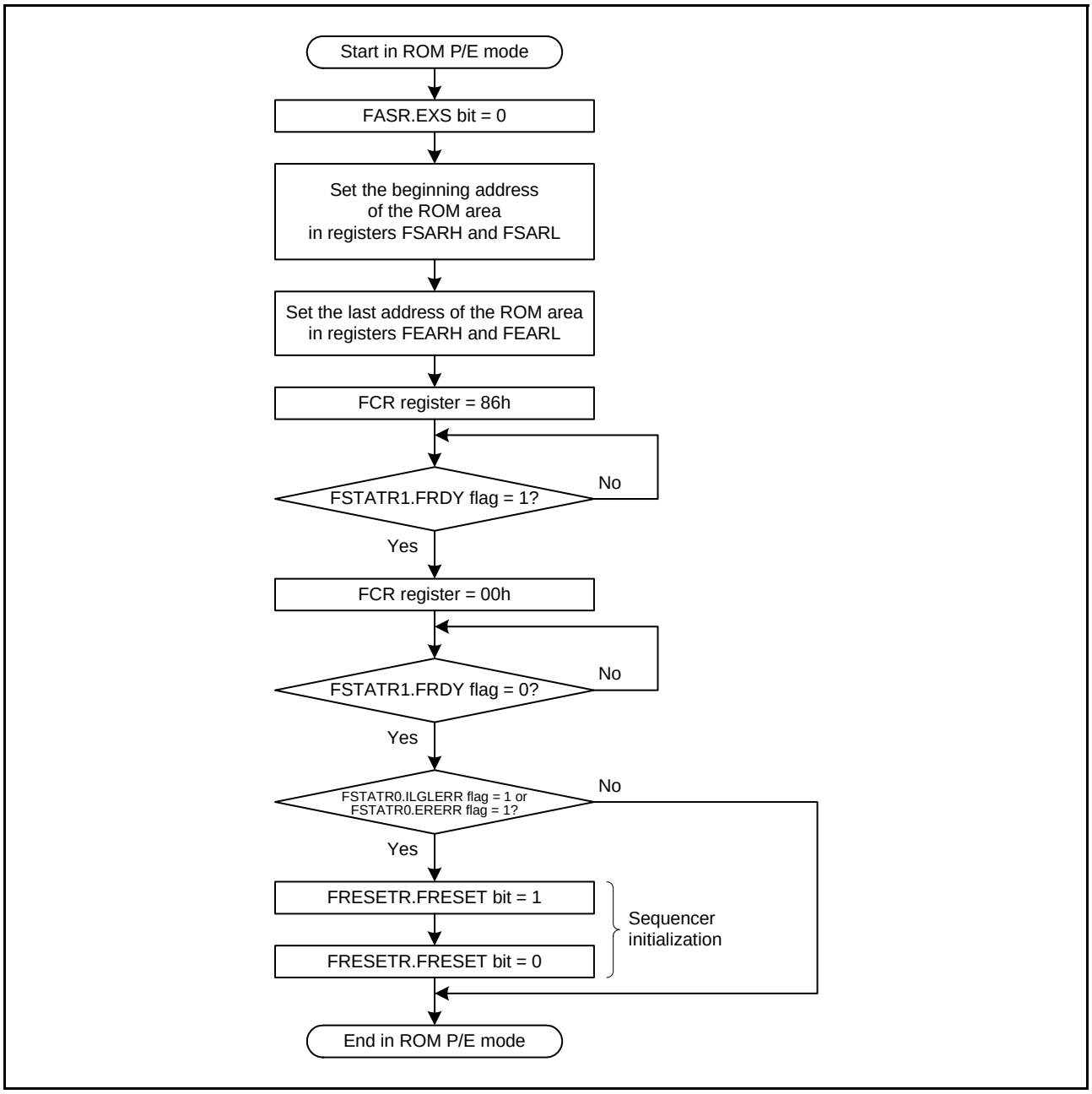


Figure 50.16 Procedure to Issue the All-Block Erase Command for the ROM

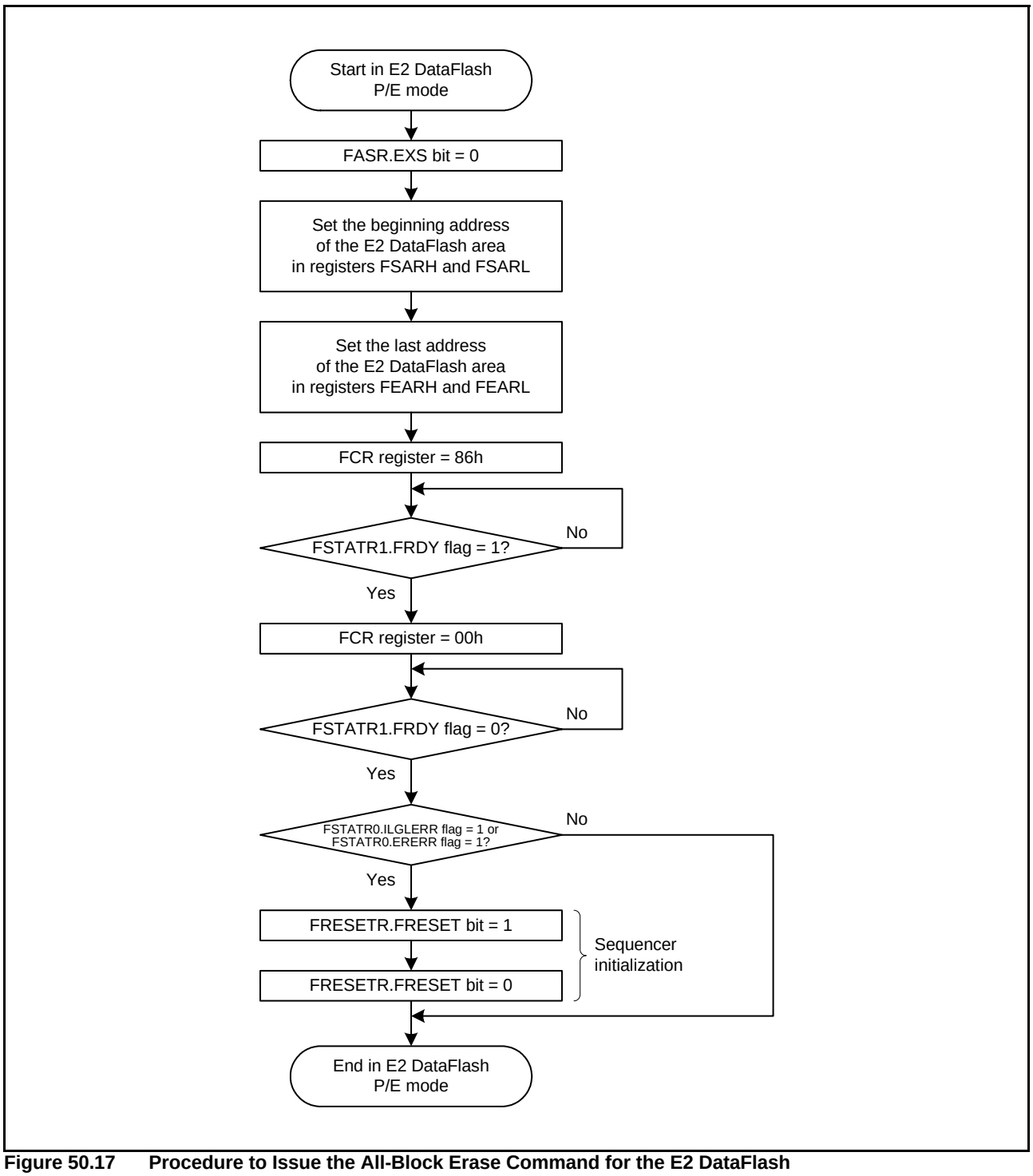


Figure 50.17 Procedure to Issue the All-Block Erase Command for the E2 DataFlash

50.7.4.4 Blank Check

Figure 50.18 and Figure 50.19 show the procedure to issue the blank check command.

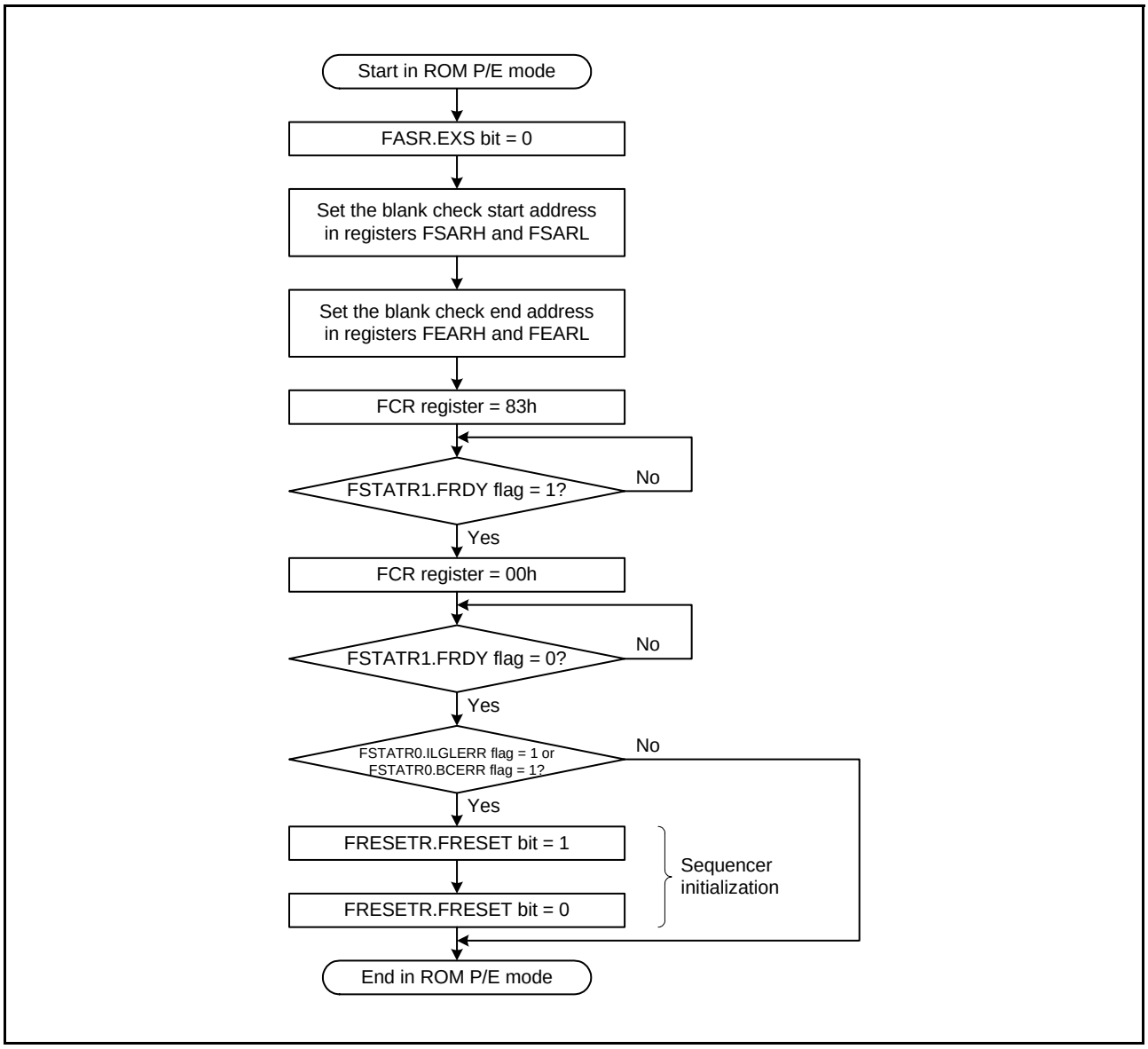


Figure 50.18 Procedure to Issue the Blank Check Command for the ROM

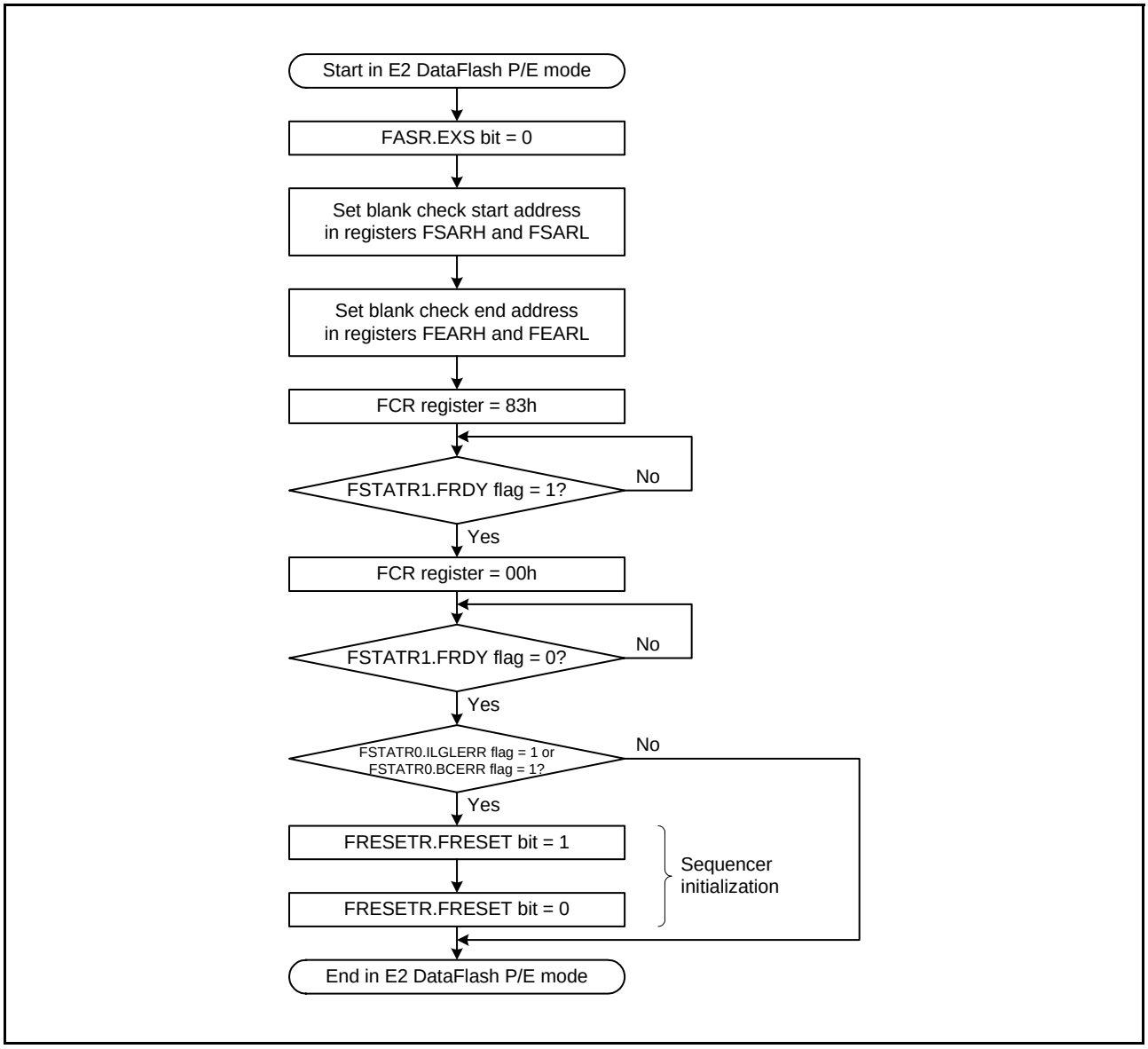


Figure 50.19 Procedure to Issue the Blank Check Command for the E2 DataFlash

50.7.4.5 Start-Up Area Information Program/Access Window Information Program

Figure 50.20 shows the procedure to issue the start-up area information program command and access window information program command.

When the sequencer has directly entered ROM/PE mode from E2 DataFlash access disabled mode, set the DFLCTL.DFLEN bit to 1 at the beginning of the procedure.

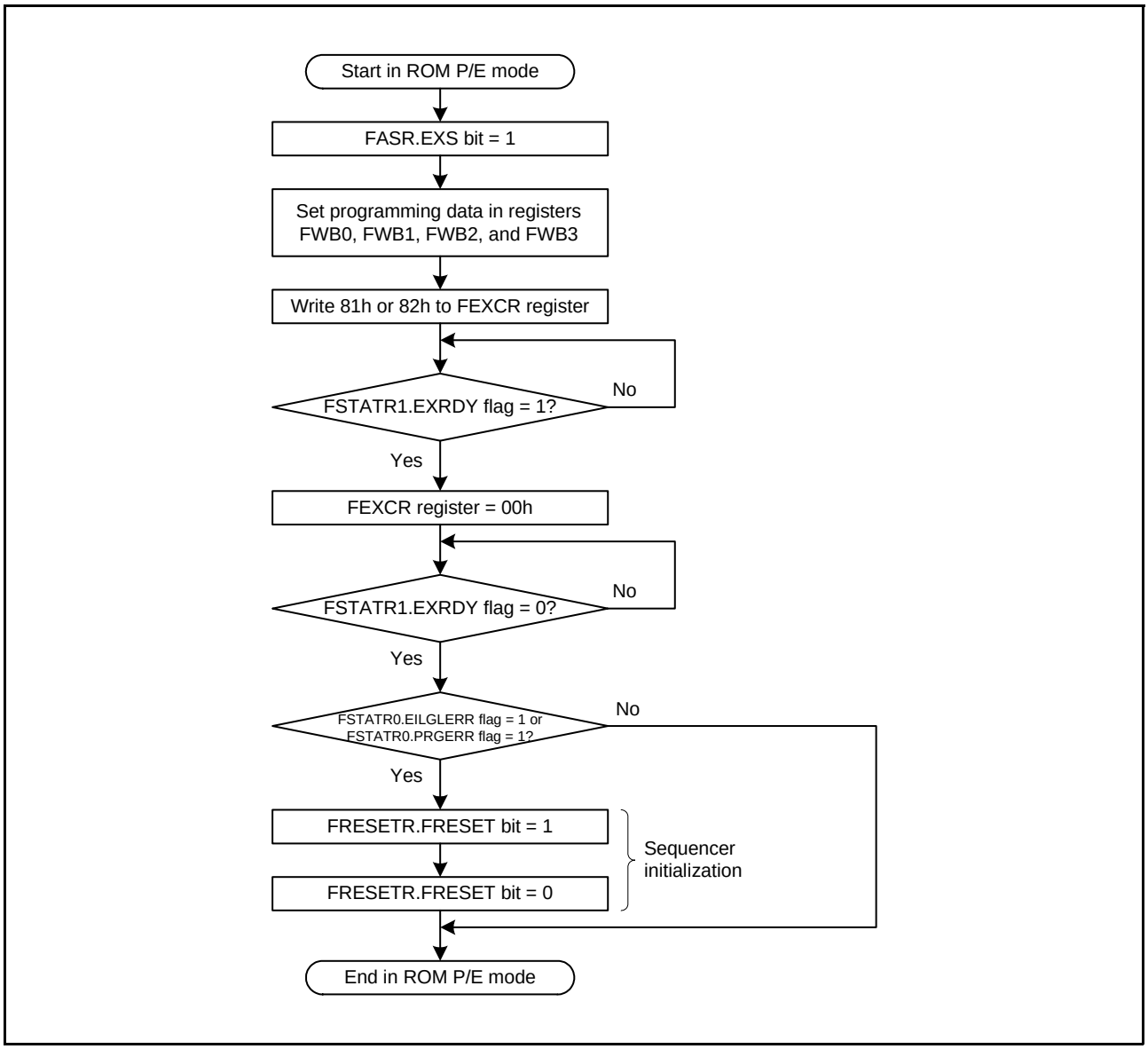


Figure 50.20 Procedure to Issue the Start-Up Area Information Program Command/Access Window Information Program Command

50.7.4.6 Forced Stop of Software Commands

Perform the procedure shown in Figure 50.21 to forcibly stop the blank check command or block erase command. When the command processing is forcibly stopped, registers FEAMH and FEAML store the address at the time of the forced stop. For blank check, the stopped processing can be continued by copying the FEAMH and FEAML register values to registers FSARH and FSARL.

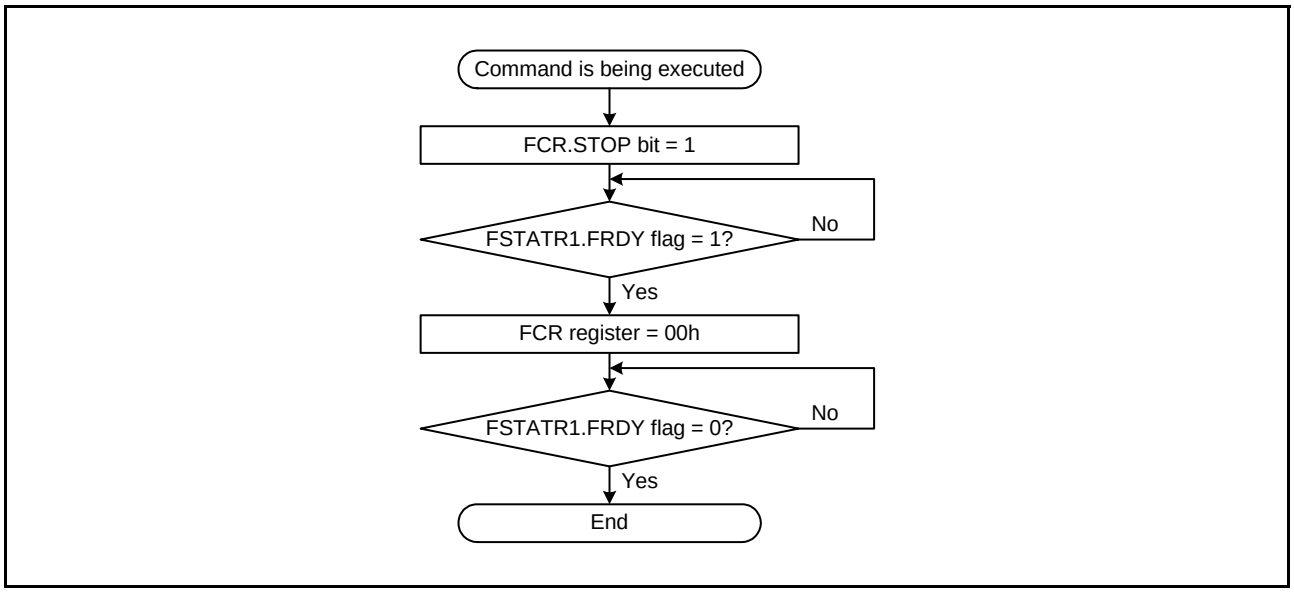


Figure 50.21 Procedure for Forced Stop of Software Commands

50.7.5 Interrupt

When software command processing or forced stop processing is completed, an interrupt (FRDYI) is generated.
When the FSTATR1.FRDY flag becomes 0 by setting the FCR.OPST bit to 0 and the FSTATR1.EXRDY flag becomes 0 by setting the FEXCR.OPST bit to 0, the next interrupt (FRDYI) can be accepted.
Clear the IRn.IR flag before setting the IERm.IEN bit of the ICU corresponding to this interrupt.

50.8 Boot Mode

The USB interface, SCI, or FINE interface is used in boot mode.
Table 50.6 lists the Programmable and Erasable Areas and Peripheral Modules Used in Boot Mode. Table 50.7 lists the I/O Pins Used in Boot Mode.

Table 50.6 Programmable and Erasable Areas and Peripheral Modules Used in Boot Mode

	Boot Mode		
Item	**USB Interface**	**SCI Interface**	**FINE Interface**
Programmable and erasable areas	User area Data area	User area Data area	User area Data area
Peripheral module	USB0	SCI1 (asynchronous serial communication)	FINE

Table 50.7 I/O Pins Used in Boot Mode

Pin Name	I/O	Mode	Description
PC7/UB	Input	Boot mode	Select operating mode (refer to section 3, Operating Modes).
MD	Input		Select operating mode (refer to section 3, Operating Modes).
MD/FINED	I/O	Boot mode (FINE interface)	Select operating mode/FINE data I/O
USB0_DP, USB0_DM	I/O	Boot mode (USB interface)	USB data I/O
P16/USB0_VBUS	Input		Detect USB cable connection/disconnection
P35/UPSEL	Input		Set bus-powered mode or self-powered mode
P30/RXD1	Input	Boot mode (SCI interface)	Receive data*1
P26/TXD1	Output		Transmit data*1

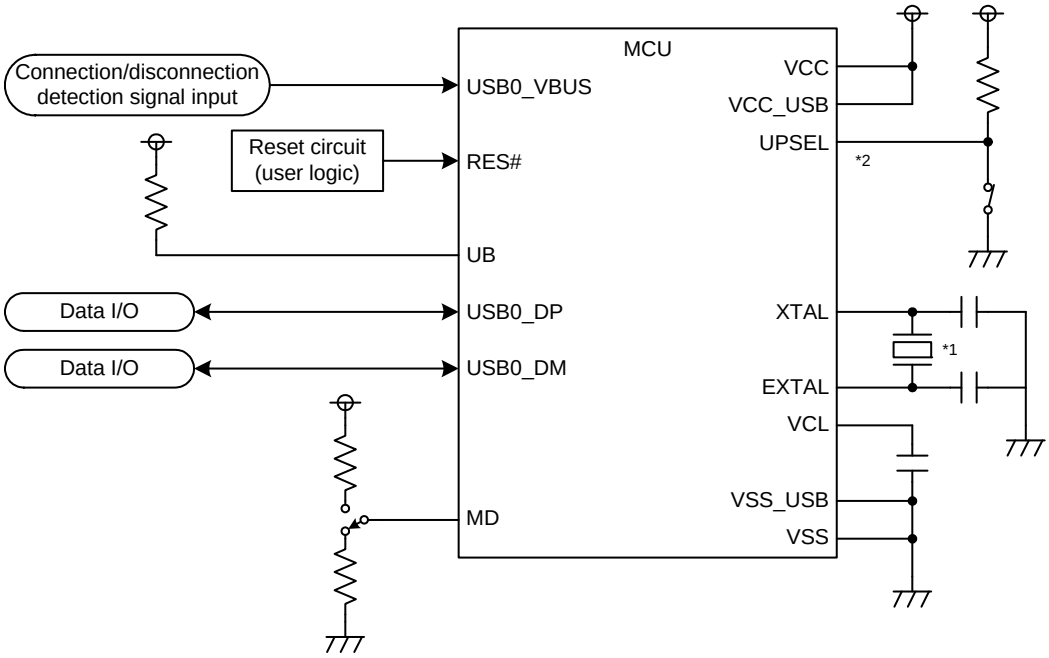
Note 1. When using the SCI, connect (pull up) this pin to VCC via a resistor.

50.8.1 Boot Mode (USB Interface)

The flash memory can be programmed and erased using the USB interface in boot mode (USB interface). The user area and data area can be rewritten.
When a reset is released while the MD pin is low and the UB pin is high, the MCU starts in boot mode (USB interface). Self-powered or bus-powered can be selected in accordance with the state of the UPSEL pin. When a reset is released while the UPSEL pin is low, self-powered mode is selected. When a reset is released while the UPSEL pin is high, bus-powered mode is selected.
Contact the manufacturer for details on the serial programmer (USB programmer).

50.8.1.1 Operating Conditions in Boot Mode (USB Interface)

USB0 is used for communication with the serial programmer in boot mode (USB interface).
4, 6, 8, 12, or 16 MHz can be used as the frequency input to the main clock oscillator. The operating voltage range is between 3.0 V and 3.6 V.
Connect the UB pin to VCC directly or VCC via a resistor (pull up).
Figure 50.22 shows an Example of Pin Connections in Boot Mode (USB Interface) When Self-Powered. Table 50.8 lists Pin Handling in Boot Mode (USB Interface) When Self-Powered. Figure 50.23 shows an Example of Pin Connections in Boot Mode (USB Interface) When Bus-Powered. Table 50.9 lists Pin Handling in Boot Mode (USB Interface) in Bus-Powered Mode.
Examples of pin connections shown in Figure 50.22 and Figure 50.23 are simplified circuits. Operations are not guaranteed in all systems.



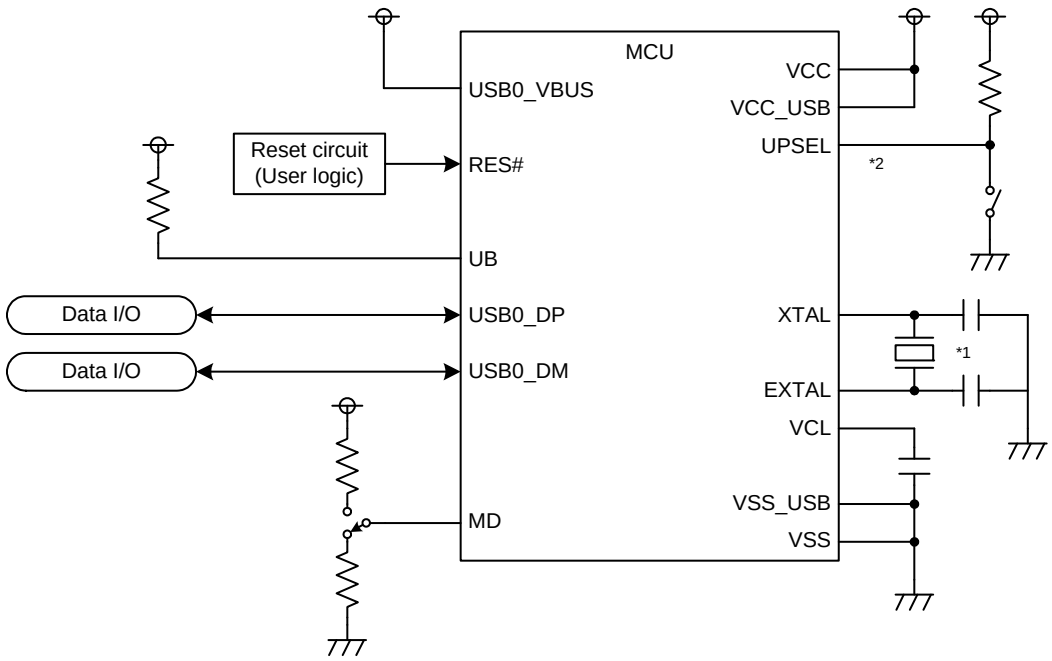
Note 1. Connect a 4, 6, 8, 12, or 16 MHz crystal, ceramic resonator or oscillator to the main clock oscillator.
Note 2. UPSEL is assigned to the same pin as NMI. This is an example when the falling edge is selected by the NMI detection set bit.

Figure 50.22 Example of Pin Connections in Boot Mode (USB Interface) When Self-Powered

Table 50.8 Pin Handling in Boot Mode (USB Interface) When Self-Powered

Pin Name	Name	I/O	Function
VCC, VSS	Power supply	—	Input the voltage between 3.0 V and 3.6 V to the VCC pin. Input 0 V to the VSS pin.
VCC_USB, VSS_USB	USB power supply	—	Connect the VCC_USB pin to the VCC pin. Connect the VSS_USB pin to the VSS pin.
AVCC0, AVSS0	12-bit A/D converter power supply	—	Connect the AVCC0 pin to the VCC pin. Connect the AVSS0 pin to the VSS pin.
VCL	Decoupling capacitor connect pin	—	Connect to the VSS pin via a decoupling capacitor for stabilizing the internal voltage.
XTAL, EXTAL	Main clock I/O pin	I/O	Connect a 4, 6, 8, 12, or 16 MHz crystal or ceramic resonator or oscillator.
MD	Operating mode control	Input	Input low.
PC7/UB	Operating mode control	Input	Input high.*1
P35/UPSEL	USB power mode control	Input	Input low.
RES#	Reset input	Input	Reset pin. Connect to the reset circuit.
USB0_DP	USB on-chip transceiver D+ I/O pin	I/O	Connect to the circuit described in section 32, USB 2.0 Host/Function Module (USBc).
USB0_DM	USB on-chip transceiver D– I/O pin	I/O	Connect to the circuit described in section 32, USB 2.0 Host/Function Module (USBc).
P16/USB0_VBUS	USB cable connection monitor pin	Input	Connect to the circuit described in section 32, USB 2.0 Host/Function Module (USBc).

Note 1. Maintain the input level for 2 ms or longer after a reset is released.



Note 1. Connect a 4, 6, 8, 12, or 16 MHz crystal, ceramic resonator or oscillator to the main clock oscillator.
Note 2. UPSEL is assigned to the same pin as NMI. This is an example when the falling edge is selected by the NMI detection set bit.

Figure 50.23 Example of Pin Connections in Boot Mode (USB Interface) When Bus-Powered

Table 50.9 Pin Handling in Boot Mode (USB Interface) in Bus-Powered Mode

Pin Name	Name	I/O	Function
VCC, VSS	Power supply	—	Input the voltage between 3.0 V and 3.6 V to the VCC pin. Input 0 V to the VSS pin.
VCC_USB, VSS_USB	USB power supply	—	Connect the VCC_USB pin to the VCC pin. Connect the VSS_USB pin to the VSS pin.
AVCC0, AVSS0	12-bit A/D converter power supply	—	Connect the AVCC0 pin to the VCC pin. Connect the AVSS0 pin to the VSS pin.
VCL	Decoupling capacitor connect pin	—	Connect to the VSS pin via a decoupling capacitor for stabilizing the internal voltage.
XTAL, EXTAL	Main clock I/O pin	I/O	Connect a 4, 6, 8, 12, or 16 MHz crystal or ceramic resonator or oscillator.
MD	Operating mode control	Input	Input low.
PC7/UB	Operating mode control	Input	Input high.*1
P35/UPSEL	USB power mode control	Input	Input high.
RES#	Reset input	Input	Reset pin. Connect to the reset circuit.
USB0_DP	USB on-chip transceiver D+ I/O pin	I/O	Connect to the circuit described in section 32, USB 2.0 Host/Function Module (USBc).
USB0_DM	USB on-chip transceiver D– I/O pin	I/O	Connect to the circuit described in section 32, USB 2.0 Host/Function Module (USBc).
P16/USB0_VBUS	USB cable connection monitor pin	Input	Connect to the USB0_VBUS pin to the VCC pin.

Note 1. Maintain the input level for 2 ms or longer after a reset is released.

50.8.2 Boot Mode (SCI Interface)

The flash memory can be programmed and erased using asynchronous serial communication in boot mode (SCI interface). The user area and data area can be rewritten.
When a reset is released while the MD pin and the UB pin are low, the MCU starts in boot mode (SCI interface).
Contact the manufacturer for details on the serial programmer.

50.8.2.1 Operating Conditions in Boot Mode (SCI Interface)

SCI1 is used to communicate with the serial programmer in boot mode (SCI interface).
Figure 50.24 shows an Example of Pin Connections in Boot Mode (SCI Interface). Table 50.10 lists Pin Handling in Boot Mode (SCI Interface).
An example of pin connections shown in Figure 50.24 is a simplified circuit. Operations are not guaranteed in all systems.

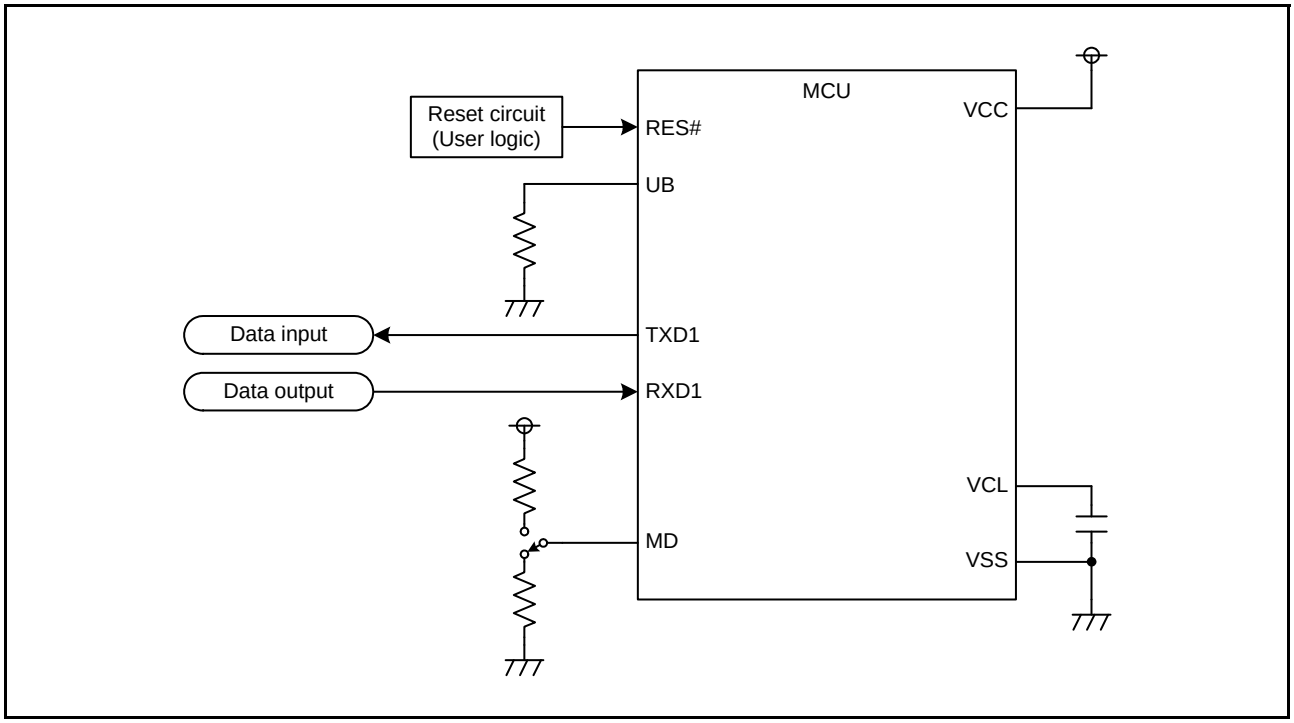


Figure 50.24 Example of Pin Connections in Boot Mode (SCI Interface)

Table 50.10 Pin Handling in Boot Mode (SCI Interface)

Pin Name	Name	I/O	Function
VCC, VSS	Power supply	—	Input 1.8 V or higher to the VCC pin. Input 0 V to the VSS pin.
VCL	Decoupling capacitor connect pin	—	Connect to the VSS pin via a decoupling capacitor for stabilizing the internal voltage.
MD	Operating mode control	Input	Input low.
PC7/UB	Operating mode control	Input	Input low.*1
RES#	Reset input	Input	Reset pin. Connect to the reset circuit.
P30/RXD1	Data input RXD	Input	Input pin for serial data
P26/TXD1	Data output TXD	Output	Output pin for serial data

Note 1. Maintain the input level for 2 ms or longer after a reset is released.

As shown in Figure 50.25, set the format to 8-bit data, 1 stop bit, no parity, and LSB first to communicate with the serial programmer.

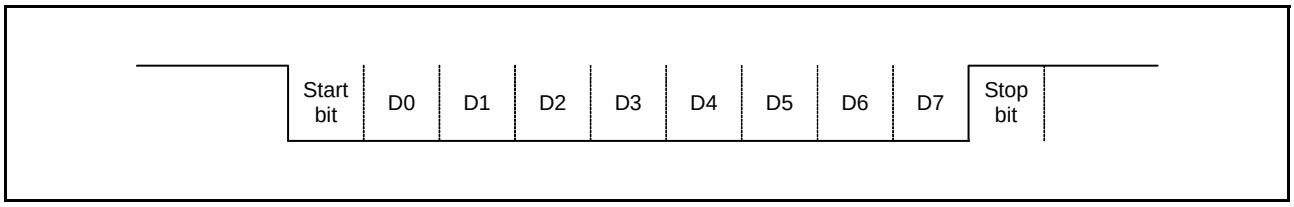


Figure 50.25 Communication Format

Initial communication with the programmer is performed at 9,600 or 19,200 bps. The communication bit rate can be changed after the MCU is connected with the programmer.
Table 50.11 lists the maximum communication bit rates for communication in boot mode (SCI interface).

Table 50.11 Conditions for Communication

Operating Voltage	Maximum Communication Bit Rate
Lower than 3.0 V	500 kbps
3.0 V or higher	2 Mbps

50.8.2.2 Starting Up in Boot Mode (SCI Interface)

To start the MCU in boot mode (SCI interface), a reset must be released by changing the RES# pin from low to high while both of the MD pin and UB pin are low. After starting up in boot mode (SCI interface), wait at least 400 ms until communication with the MCU is enabled in boot mode (SCI interface).
As shown in Figure 50.26, keep the signal of each pin unchanged for 400 ms after the reset is released. Use resets according to the range described in section 51.3.2, Reset Timing.

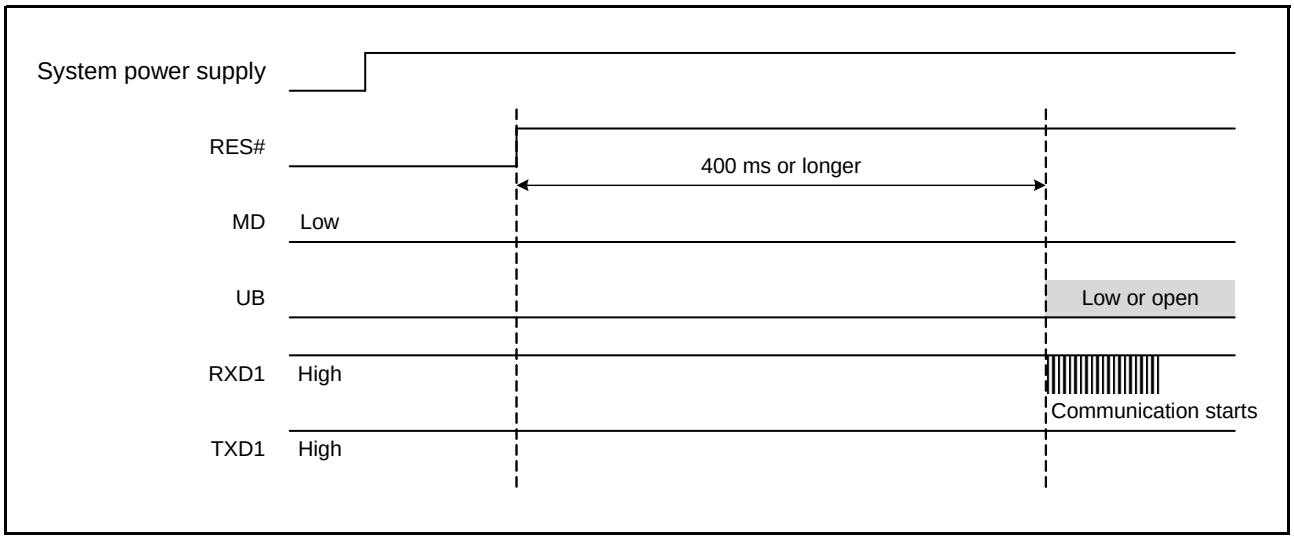


Figure 50.26 Wait Time until Communication Becomes Possible in Boot Mode (SCI Interface)

50.8.3 Boot Mode (FINE Interface)

The flash memory can be programmed and erased using the FINE in boot mode (FINE interface). The user area and data area can be rewritten.
Contact the manufacturer for details on the serial programmer.

50.8.3.1 Operating Conditions in Boot Mode (FINE Interface)

FINE is used to communicate with the serial programmer in boot mode (FINE Interface).
Figure 50.27 shows an Example of Pin Connections in Boot Mode (FINE Interface). Table 50.12 lists Pin Handling in Boot Mode (FINE Interface).
An example of pin connections shown in Figure 50.27 is a simplified circuit. Operations are not guaranteed in all systems.

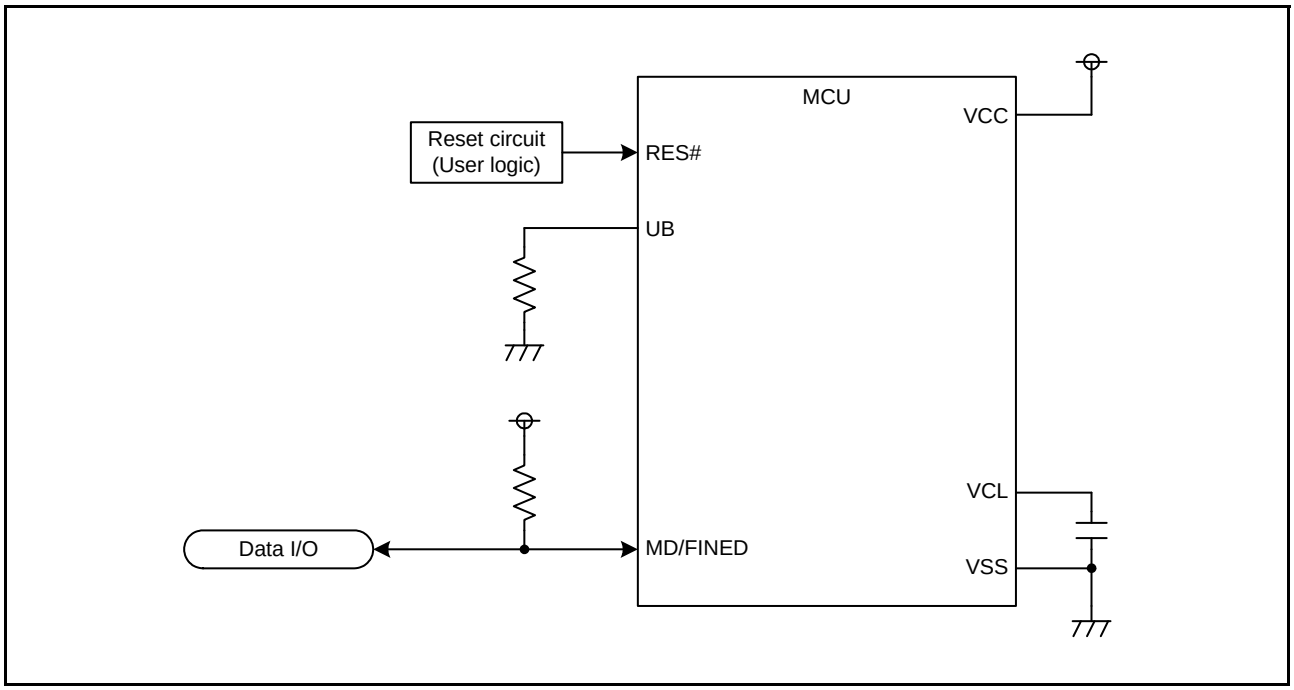


Figure 50.27 Example of Pin Connections in Boot Mode (FINE Interface)

Table 50.12 Pin Handling in Boot Mode (FINE Interface)

Pin Name	Name	I/O	Function
VCC, VSS	Power supply	—	Input 1.8 V or higher to the VCC pin. Input 0 V to the VSS pin.
VCL	Decoupling capacitor connect pin	—	Connect to the VSS pin via a decoupling capacitor for stabilizing the internal voltage.
MD/FINED	Operating mode control/data I/O	I/O	Connect to the VCC pin via a resistor (pull up).
PC7/UB	Operating mode control	Input	Input low.*1
RES#	Reset input	Input	Reset pin. Connect to the reset circuit.

Note 1. Maintain the input level for 2 ms or longer after a reset is released.

50.9 Flash Memory Protection

Flash memory protection prevents the flash memory from being read or rewritten by the third party.
The boot mode ID code protection is for connecting the serial programmer, and the on-chip debugging emulator ID code protection is for connecting the on-chip debugging emulator.

50.9.1 ID Code Protection

There are two types of ID code protection: Boot mode ID code protection for connecting the serial programmer and on-chip debugging emulator ID code protection is for connecting the on-chip debugging emulator. The same ID codes are used for both functions, but operations differ.
ID codes consist of the control code and ID code 1 to ID code 15. Set ID codes to four 32-bit data in 32-bit units. Figure 50.28 shows the ID Code Configuration.

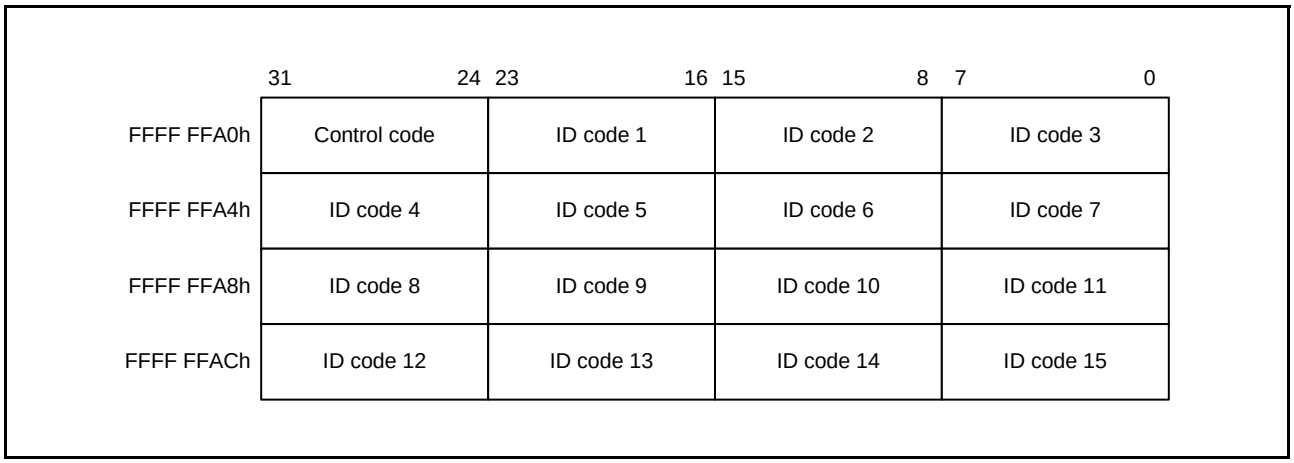


Figure 50.28 ID Code Configuration

The following shows a program example for setting ID codes.
This is an example when setting the control code to 45h and setting ID codes to 01h, 02h, 03h, 04h, 05h, 06h, 07h, 08h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, and 0Fh (from the ID code 1 field to the ID code 15 field).

C language:

```
#pragma address ID_CODE = 0xFFFFFFA0
const unsigned long ID_CODE [4] = {0x45010203, 0x04050607,0x08090A0B, 0x0C0D0E0F};
```

Assembly language:

```
.SECTION ID_CODE,CODE
.ORG 0FFFFFFA0h
.LWORD 45010203h
.LWORD 04050607h
.LWORD 08090A0Bh
.LWORD 0C0D0E0Fh
```

50.9.1.1 Boot Mode ID Code Protection

Boot mode ID code protection disables reading and programming of the user area and data area when the serial programmer is connected by the third party.
When the control code indicates 45h or 52h (boot mode ID code protection is enabled), the MCU compares 16-byte ID code sent from the serial programmer with the ID code in the user area. According to the comparison result, reading and programming the user area and data area are enabled.
When the control code indicates a value other than 45h and 52h (boot mode ID code protection is disabled), all blocks in the user area and data area are erased, and reading and programming the user area and data area are enabled.

The control code is used to enable or disable protection. Table 50.13 lists the specifications of boot mode ID code protection, and Figure 50.29 shows the authentication flow of boot mode ID code protection.
ID code 1 to ID code 15 can be set to any desired value.
However, only when disabling connection with the serial programmer, the ID codes must be set to 50h, 72h, 6Fh, 74h, 65h, 63h, 74h, FFh, FFh, FFh, FFh, FFh, FFh, FFh, and FFh (from the ID code 1 field to the ID code 15 field).

Table 50.13 Boot Mode ID Code Protection Specifications

ID Code				
Control Code	**ID Code 1 to ID Code 15**	**Protection**	**ID Code Matching Result**	**Operation**
45h	Any desired value	Enabled	Matched	Exit the boot mode ID code authentication state and enter the program/erase host command wait state.
			Not matched	Continue the boot mode ID code authentication state.
			Not matched three times consecutively	Erase all blocks in the user area and data area, and continue boot mode ID code authentication state.
52h	50h, 72h, 6Fh, 74h, 65h, 63h, 74h, FFh, ..., and FFh (8 bytes are all FFh)	Enabled	N/A	Disable reading or rewriting of the flash memory, regardless of the codes sent from the serial programmer.
	Other than above		Matched	Exit the boot mode ID code authentication state and enter the program/erase state.
			Not matched	Continue the boot mode ID code authentication state.
Other than above	Any desired value	Disabled	N/A	Erase all blocks in the user area and data area.

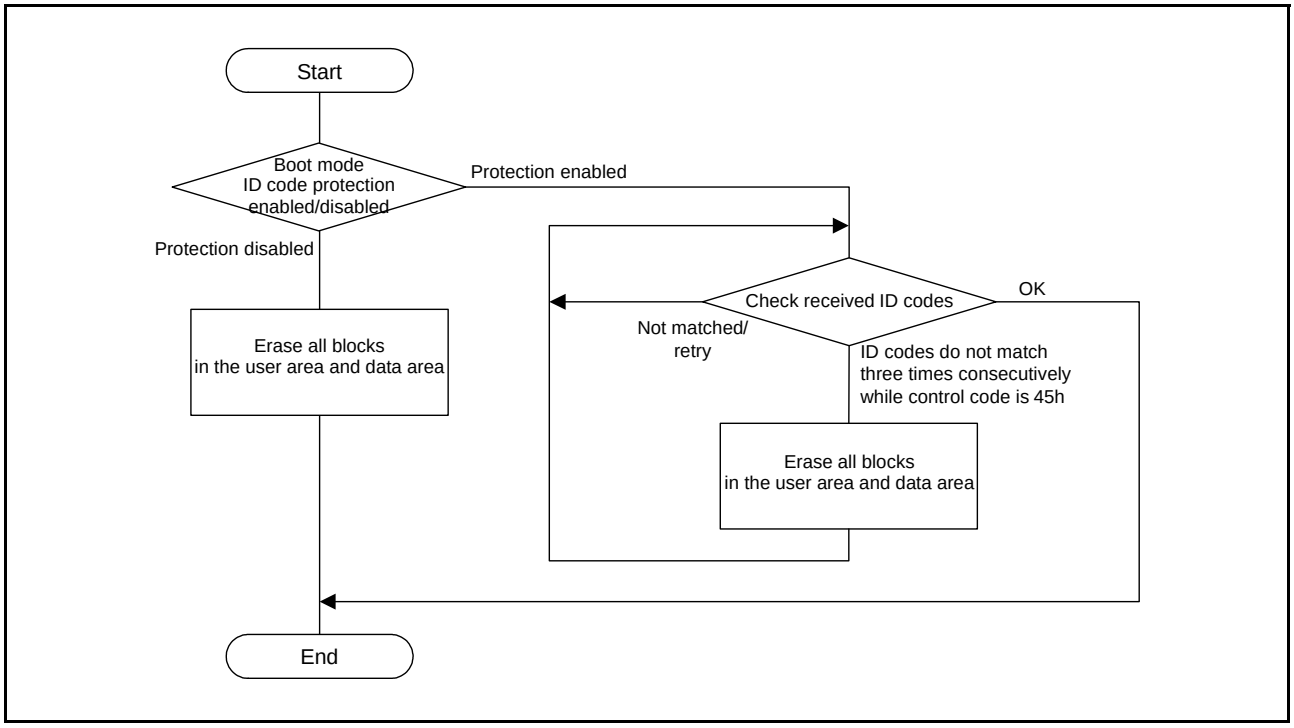


Figure 50.29 Authentication for Boot Mode ID Code Protection

50.9.1.2 On-Chip Debugging Emulator ID Code Protection

On-chip debugging emulator ID code protection enables or disables connection with the on-chip debugging emulator. When the on-chip debugging emulator ID code protection is disabled, connection with the on-chip debugging emulator is enabled. When 16-byte ID codes sent from the on-chip debugging emulator and ID codes in the user area match while on-chip debugging emulator ID code protection is enabled, connection with the on-chip debugging emulator is also enabled.

Table 50.14 lists the specifications of on-chip debugging emulator ID code protection.

Table 50.14 On-Chip Debugging Emulator ID Code Protection Specifications

ID Code				
Control Code	ID Code 1 to ID Code 15	Protection	ID Code Matching Result	Operation
FFh	FFh,…, and FFh (15 bytes are all FFh)	Disabled	N/A	Enable connection with the on-chip debugging emulator.
52h	50h, 72h, 6Fh, 74h, 65h, 63h, and 74h + any 8 bytes	Enabled	N/A	Disable connection with the on-chip debugging emulator, regardless of the codes sent from the on-chip debugging emulator.
Other than above	Other than above	Enabled	Matched	Enable connection with the on-chip debugging emulator.
			Not matched	Continue the ID code wait state.

50.10 Communication Protocol

This section describes the protocol used in boot mode. When developing a serial programmer, control with this communication protocol.

50.10.1 State Transition in Boot Mode (SCI Interface)

Figure 50.30 shows the Boot Mode (SCI Interface) State Transition.

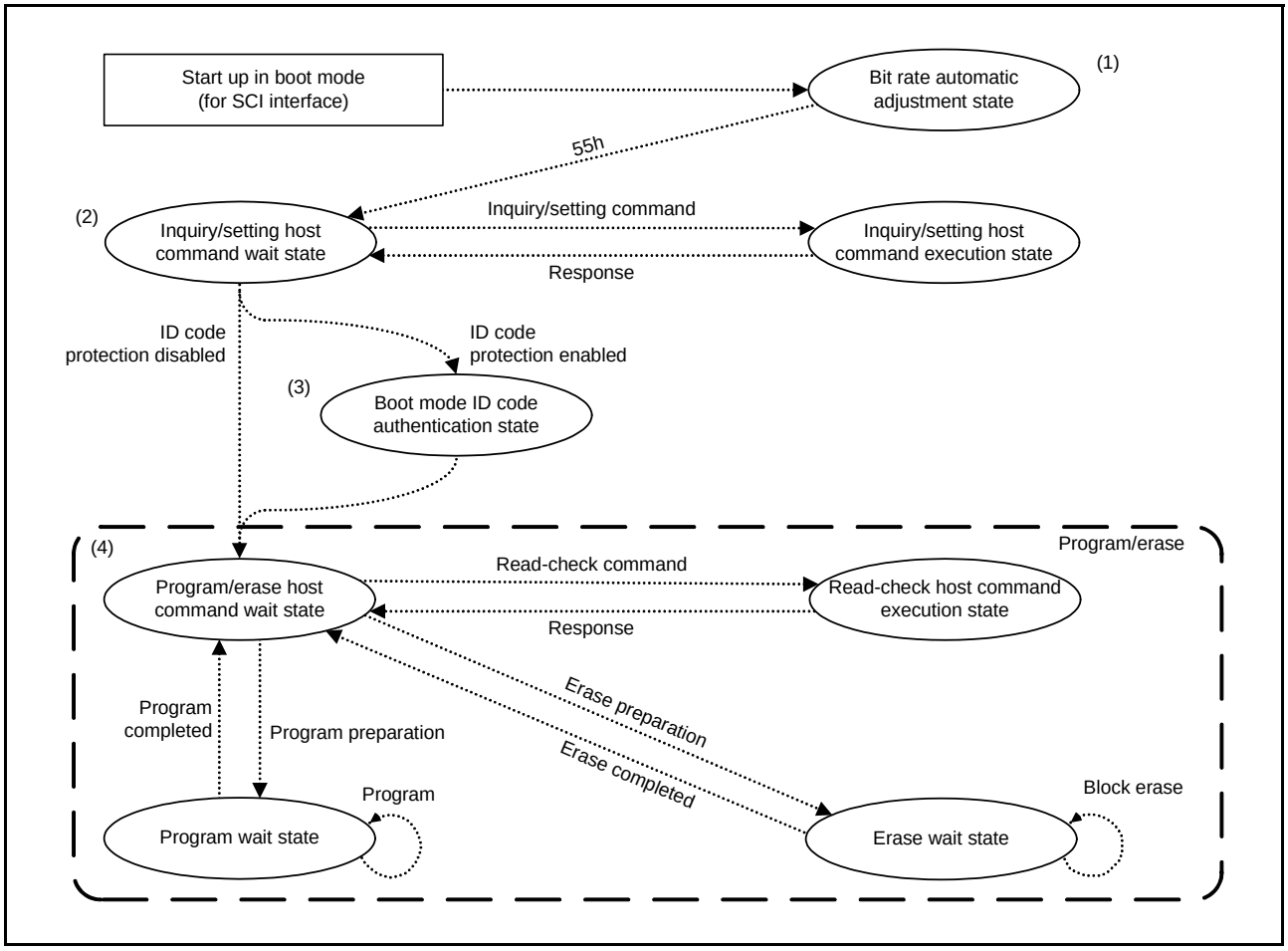


Figure 50.30 Boot Mode (SCI Interface) State Transition

(1) Bit rate automatic adjustment state

In this state, the bit rate is automatically adjusted to 9,600 or 19,200 bps for communication with the host.

When the bit rate adjustment is completed, the MCU sends 00h to the host. After that, when the MCU receives 55h sent from the host, the MCU sends E6h to the host, and enters the inquiry/setting host command wait state.

The host must not send data until 400 ms elapse after a reset of the MCU is released.

(2) Inquiry/setting host command wait state

In this state, the host can make inquiries for the MCU information including block configuration, size, and addresses where the user area and data area are allocated, and select the endian of data and a bit rate.

When the MCU receives the program/erase host state transition command from the host, it determines whether boot mode ID code protection is enabled or disabled. If boot mode ID code protection is disabled, the MCU enters the inquiry/setting host command wait state. If boot mode ID code protection is enabled, the MCU enters the boot mode ID code authentication state.

Refer to section 50.10.5, Inquiry Commands and section 50.10.6, Setting Commands for details on inquiry/setting commands.

(3) Boot mode ID code authentication state
In this state, the MCU accepts the ID code authentication command.
When boot mode ID codes do not match, the MCU remains in the boot mode ID code authentication state.
Refer to section 50.9.1.1, Boot Mode ID Code Protection for details on boot mode ID code protection. Refer to section 50.10.7, ID Code Authentication Command for details on the ID code authentication command.

(4) Program/erase state
In this state, the MCU executes program/erase or read-check commands according to commands sent from the host.
Refer to section 50.10.8, Program/Erase Commands for details on program/erase commands. Refer to section 50.10.9, Read-Check Commands for details on read-check commands.

50.10.2 Command and Response Configuration

The communication protocol is composed of a “Command” sent from the host to the MCU and a “Response” sent from the MCU to the host. Commands include 1-byte commands and multiple-byte commands. Responses include 1-byte responses, multiple-byte responses, and error responses.
A multiple-byte command and multiple-byte response have “Size” for informing the number of transmit/receive data bytes and “SUM” for detecting communication errors.
“Size” indicates the number of transmit/receive data bytes excluding Command code (the first byte), Size, and SUM.
“SUM” indicates byte data that is calculated so the total bytes of Command or Response becomes 00h.
The flash memory addresses for reading are used as the following addresses: the program address specified in the program command, the block start address specified in the block erase command, the AW start and end addresses specified in the access window information program command, and the AW start and end addresses received in the access window read command.

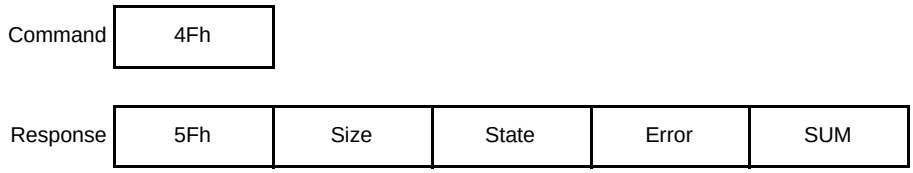
50.10.3 Response to Undefined Commands

When the MCU receives an undefined command, it sends a command error as a response. The contents of the response are shown below. “Command code” in the error response stores the first byte of the command sent from the MCU.

Error response	80h	Command code

50.10.4 Boot Mode Status Inquiry

This command is used to check the current state and which type of an error occurred immediately after a command issued in the boot program.
Table 50.15 and Table 50.16 list a state or error that the MCU responds to.
The boot mode status inquiry command can be used in the inquiry/setting host command wait state and program/erase host command wait state.



Size (1 byte): Total bytes of “State” and “Error” (the value is always 02h)
State (1 byte): MCU’s current state (see Table 50.15)
Error (1 byte): Information about the error occurred in response to a command issued immediately before (see Table 50.16)
SUM (1 byte): Value that is calculated so the sum of response data is 00h

Table 50.15 Information Regarding the States

Code	State*1	Description
11h	Inquiry/setting host command wait state	Device selection wait state
12h/13h		Operating frequency selection wait state
1Fh		Program/erase host command wait state transition command wait state
31h	Boot mode ID code authentication state	The user area and data area are being erased
3Fh	Program/erase host command wait state	Program/erase command wait state
4Fh		Program data reception wait state
5Fh		Block erase specification wait state

Note 1. Refer to Figure 50.30 for details on the state transitions.

Table 50.16 Error Information

Code	Description
00h	No error
11h	SUM error
21h	Device code error
24h	Bit rate selection error
29h	Block start address error
2Ah	Address error
2Bh	Data length error
51h	Erase error
52h	Not blank (blank check error)
53h	Program error
61h	ID code do not match
63h	ID code do not match and erase error
80h	Command error
FFh	Bit rate automatic adjustment error

50.10.5 Inquiry Commands

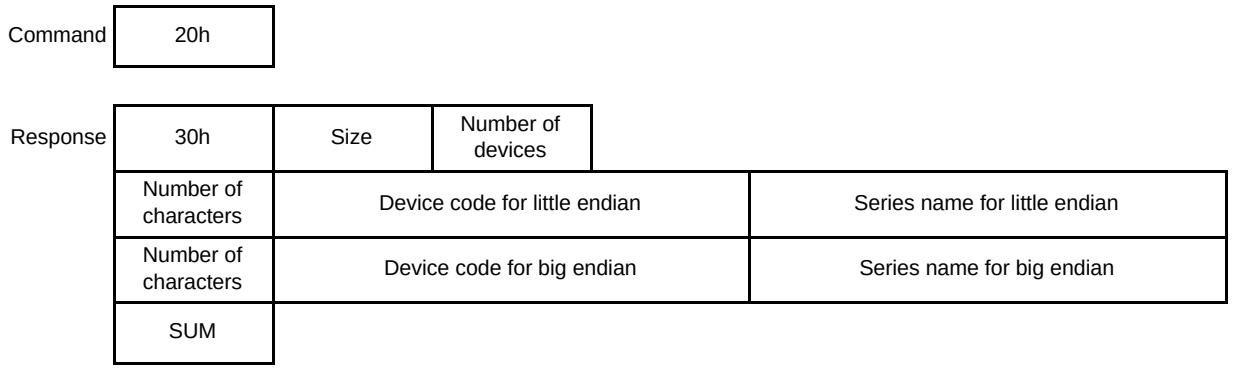
Inquiry commands are used to obtain necessary information for sending setting commands, program/erase commands, and read-check commands. Table 50.17 lists the inquiry commands. These commands can only be used in the inquiry/setting host command wait state.

Table 50.17 Inquiry Commands

Command	Description
Supported device inquiry	Inquiry for the device code and series name
Data area availability inquiry	Inquiry for the availability of the data area
User area information inquiry	Inquiry for the number of user areas, and the start and end addresses of the user area
Data area information inquiry	Inquiry for the number of data areas, and the start and end addresses of the data area
Block information inquiry	Inquiry for the start address, the block size, and the number of blocks of each of the user and data areas

50.10.5.1 Supported Device Inquiry

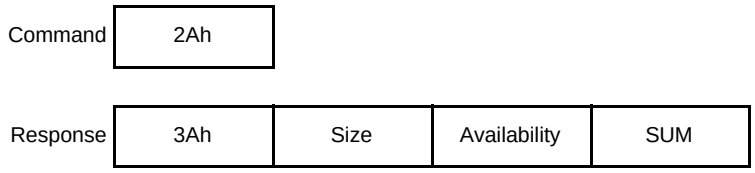
This command is used to obtain the device information for identifying the endian of developed software.
After the MCU receives this command, it sends the device information when developed software uses little endian data and the device information when developed software uses big endian data in this order.



Size (1 byte): Total bytes of Number of Devices, Characters, Device code, and Series name
Number of devices (1 byte): Number of endian types that the MCU supports (the value is always 02h)
Number of characters (1 byte): Number of characters for the device code and device name
Device code (4 bytes): Identification code indicating the endian of developed software
Series name (n bytes): The series name of the MCU (ASCII code) and the classification of little endian/big endian
SUM (1 byte): Value that is calculated so the sum of response data is 00h

50.10.5.2 Data Area Availability Inquiry

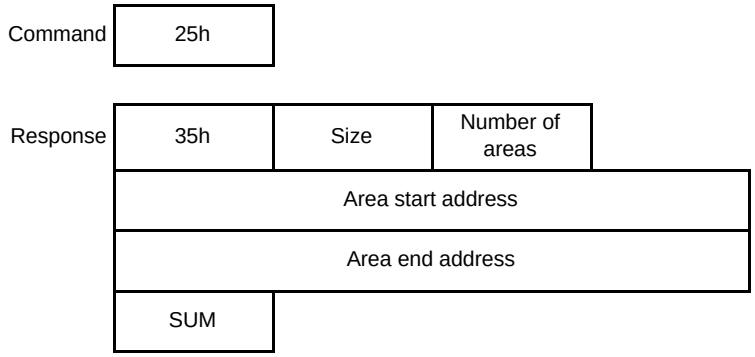
When the MCU receives this command, it sends the result indicating that the data area is available, area protection can be used, and the data area program command is available.



Size (1 byte): Number of characters of Availability (the value is always 01h)
Availability (1 byte): Availability of the data area (the value is always 1Dh)
1Dh represents the data area is available, area protection can be used, and data area program command is available.
SUM (1 byte): Value that is calculated so the sum of response data is 00h (the value is always A8h)

50.10.5.3 User Area Information Inquiry

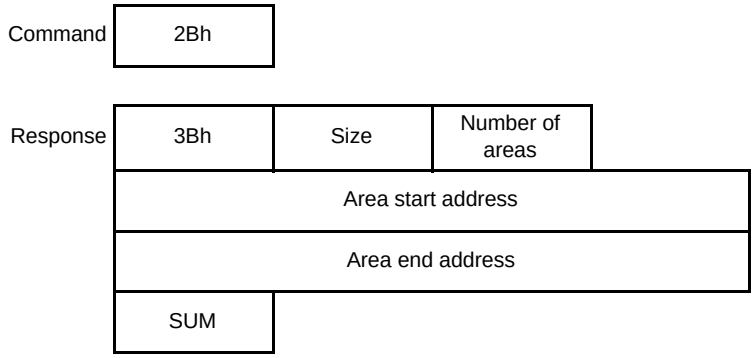
When the MCU receives this command, it sends the number of user areas and addresses.



Size (1 byte): Total bytes of Number of areas, Area start address, and Area end address (the value is always 09h)
Number of areas (1 byte): Number of user areas (the value is always 01h)
Area start address (4 bytes): Start address of the user area
Area end address (4 bytes): End address of the user area
SUM (1 byte): Value that is calculated so the sum of the response data is 00h

50.10.5.4 Data Area Information Inquiry

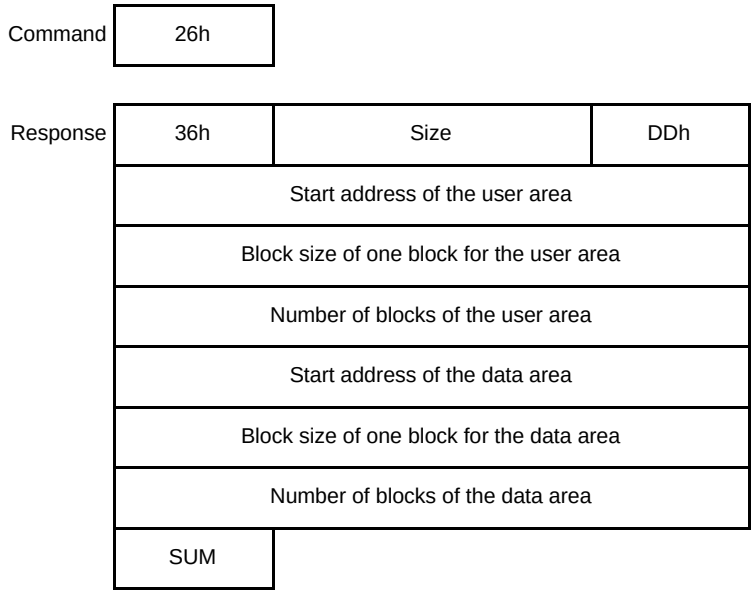
When the MCU receives this command, it sends the number of data areas and addresses.



Size (1 byte): Total bytes of data of Number of areas, Area start address, and Area end address (the value is always 09h)
Number of areas (1 byte): Number of areas in the data area (the value is always 01h)
Area start address (4 bytes): Start address of the data area (the value is always 0010 0000h)
Area end address (4 bytes): End address of the data area (the value is always 0010 1FFFh)
SUM (1 byte): Value that is calculated so the sum of the response data is 00h (the value is always 7Dh)

50.10.5.5 Block Information Inquiry

When the MCU receives this command, it sends the start address, the size of one block, and the number of blocks in the user area and data area.



Size (2 bytes): Total bytes of data from DDh to Number of blocks of the data area (the value is always 00 19h)
Start address of the user area (4 bytes): Start address of the user area
Block size of one block for the user area (4 bytes): Memory size of one block (the value is always 00 00 08 00h)
Number of blocks of the user area (4 bytes): Number of blocks in the user area
Start address of the data area (4 bytes): Start address of the data area (the value is always 00 10 00 00h)
Block size of one block for the data area (4 bytes): Memory size of one block (the value is always 00 00 04 00h)
Number of blocks of the data area (4 bytes): Number of blocks in the data area (the value is always 00 00 00 08h)
SUM (1 byte): Value that is calculated so the sum of response data is 00h

50.10.6 Setting Commands

Setting commands are used to configure the settings necessary to execute program/erase commands in the MCU. Table 50.18 lists Setting Commands. These commands can be used only in the inquiry/setting host command wait state.

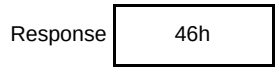
Table 50.18 Setting Commands

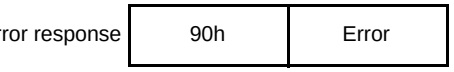
Command	Function
Device select	Select a device code.
Operating frequency select	Change the bit rate for communication.
Program/erase host command wait state transition	Enter the program/erase host command wait state or boot mode ID code authentication state.

50.10.6.1 Device Select

This command is used to specify the endian of developed software. Select a device code from among the device codes obtained in the response to the support device inquiry command.
If the received device code matches the supported device, the MCU sends a response (46h).
If the device is not supported or the SUM of the received command does not match, the MCU sends an error response.

Size (1 byte): Number of characters of the device code (the value is always 04h)
Device code (4 bytes): Identification code to identify an endian of the developed software
(code in the response to the support device inquiry command)
SUM (1 byte): Value that is calculated so the sum of command data is 00h





Error (1 byte): Error code
11h: SUM error
21h: Device code error

50.10.6.2 Operating Frequency Select

This command is used to specify the operating frequency of the MCU and a bit rate for communication with the flash memory programmer. The bit rate selected in this command should be set to a value with error of less than 4% compared to the bit rate obtained by dividing 32 or 8 MHz that corresponds to the operating voltage.
If the specified settings can be supported, the MCU sends a response (06h). If the bit rate error is 4% or more or the SUM of the received command does not match, the MCU sends an error response.

After the host receives a response, wait for at least a 1-bit period at the old bit rate, and send communication confirmation data at the new bit rate.
If the MCU successfully receives communication confirmation data, the MCU sends a response (06h). If the MCU fails to receive the communication confirmation data, the MCU sends an error response.

Command	3Fh	Size	Bit rate	Dummy data
	Number of clocks	Multiplier 1	Multiplier 2	
	SUM			

Size (1 byte): Total bytes of data of Bit rate, Dummy data, Number of clocks, and Multiplier (the value is always 07h)
Bit rate (2 bytes): New bit rate
The value is calculated by dividing the bit rate by 100 (Example: Set 00C0h for 19200 bps)
Dummy data (2 bytes): The value should always be set to 0000h
Number of clocks (1 byte): Types of clocks for multiplier setting (the value is always 02h)
Multiplier 1 (1 byte): Multiplier of the system clock (ICLK) (the value is always 01h)
Multiplier 2 (1 byte): Multiplier of the peripheral module clock (PCLK) (the value is always 01h)
SUM (1 byte): Value that is calculated so the sum of command data including dummy data is 00h

Response	06h	

Error response	BFh	Error

Error (1 byte): Error code
11h: SUM error
24h: Bit rate selection error

Communication confirmation	06h

Response	06h

Error response	FFh

- Bit rate selection error

A bit rate selection error occurs when the bit rate specified with the operating frequency select command cannot be set to a value with error of less than 4%. When the new bit rate specified with the operating frequency select command is B, and 32 (MHz) or 8 (MHz) corresponding to the operating voltage is Pφ, the bit rate error is calculated by the following formula:

$$\text{Error}(\%) = \left(\frac{P\varphi \times 10^6}{B \times 32 \times N} - 1\right) \times 100$$

$$N = \text{INT}\left(\frac{P\varphi \times 10^6}{B \times 32}\right)$$

Pφ: 32 (MHz) when the operating voltage is 3.0 V or above
8 (MHz) when the operating voltage is below 3.0 V
B: New bit rate (bps)
N: Ratio between Pφ and the new bit rate multiplied by 32 (however, 1 ≤ N ≤ 256)

50.10.6.3 Program/Erase Host Command Wait State Transition

This command is used for the transition from the inquiry/setting host command wait state to the program/erase host command wait state.
When the MCU receives this command, it determines whether boot mode ID code protection is enabled or disabled.

When boot mode ID code protection is disabled, all blocks in the user area and data area are erased.
When all blocks are successfully erased, the MCU sends a response (06h) and enters the program/erase host command wait state. If not all blocks are successfully erased, the MCU sends an error response.
When boot mode ID code protection is enabled, the MCU sends a response (16h) and enters boot mode ID code authentication state.

Command	40h

Response	ACK

ACK (1 byte): ACK code
06h: ID code protection is disabled.
16h: ID code protection is enabled.

Error response	C0h	Error

Error (1 byte): Error code
51h: Erase error

50.10.7 ID Code Authentication Command

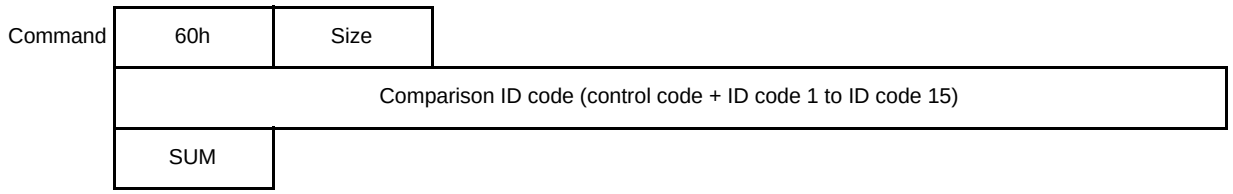
This command is used for ID code authentication when boot mode ID code protection is enabled.
Table 50.19 lists ID code authentication command. This command can be used only in the boot mode ID code authentication state.

Table 50.19 ID Code Authentication Command

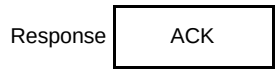
Command	Function
ID code check	Compare the 16-byte code sent from the host and ID code.

50.10.7.1 ID Code Check

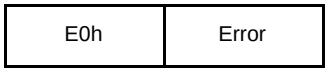
This command is used to unlock boot mode ID code protection.
The comparison ID code specified with the command should be set to the same value as the control code and ID code 1 to ID code 15.
If the comparison ID code sent from the host matches the ID code programmed in the user area, the MCU sends a response (06h) and enters program/erase host command wait state.
If the codes do not match or the SUM of the received command does not match, the MCU sends an error response.
When the ID codes do not match three times consecutively while the control code is 45h, all blocks in the user area and data area are erased. If an error occurs during erasure, the MCU sends an error response.
Also, even if all blocks are successfully erased, the MCU sends an error response and continues the boot mode ID code state. Reset the MCU to enter the program/erase host command wait state.



Size (1 byte): Number of bytes of ID codes (the value is always 10h)
ID code (16 bytes): Control code (1 byte) + ID code 1 to ID code 15 (15 bytes)
SUM (1 byte): Value that is calculated so the sum of the command data is 00h



ACK (1 byte): ACK code
06h: The MCU enters the program/erase host command wait state.



Error (1 byte): Error code
11h: SUM error
61h: ID codes do not match
63h: ID codes do not match and erase error

50.10.8 Program/Erase Commands

Program/erase commands are used to program or erase the user area or data area based on the response to inquiry commands. Table 50.20 lists commands used in each of the program/erase host command wait state, program wait state, and erase wait state. Table 50.21 lists commands that can be accepted in each state.
When a command that is not listed in Table 50.21 is received in each state, the MCU sends a command error response.

Table 50.20 Program/Erase Commands

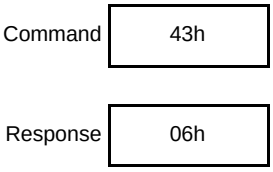
Command	Function
User/data area program preparation	Select the user area or data area to program, and enter the program wait state.
Program	Program the specified data to the selected area in the user area or data area. Or enter the program/erase host command wait state (end of program).
Data area program	Program the specified-size data to the selected area in the data area. Or enter the program/erase host command wait state (end of program).
Erase preparation	Enter the erase wait state.
Block erase	Erase the selected block, or enter the program/erase host command wait state (end of erase).

Table 50.21 Acceptable Commands for Each State

State	Acceptable Command
Program/erase host command wait state	User/data area program preparation command, and erase preparation command
Program wait state	Program command, and data area program command
Erase wait state	Block erase command

50.10.8.1 User/Data Area Program Preparation

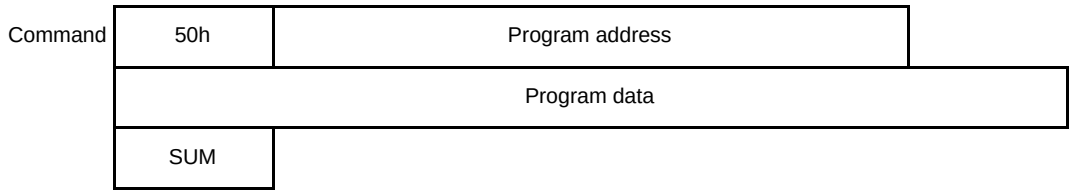
This command is used to prepare for accepting the program command and the data area program command.
When the MCU receives this command, it recognizes that an instruction to prepare for the program command is issued from the host. Then, the MCU enters the program wait state, where only the program command to the user area or data area can be accepted, and sends a response (06h).



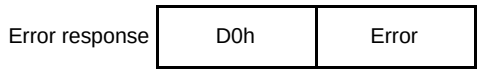
50.10.8.2 Program

This command is used to program the specified data to the user area or data area. Set the lower 8 bits to 0 for the program address selected in this command. When the data length is shorter than 256 bytes, the data cannot be programmed. Fill the gaps with FFh.
When the program from the selected address is successfully completed, the MCU sends a response (06h). If the SUM of the received command does not match or an error occurs during a program operation, the MCU sends an error response.

To enter the program/erase host command wait state after the program operation ends, send 50h FFh FFh FFh FFh B4h from the host. The MCU sends a response (06h), and enters the program/erase host command wait state.



Program address (4 bytes): Address for program destination
Set the lower 8 bits to 0
Set FFFF FFFFh for end of program
Program data (n bytes): Program data (n = 256, 0 for end of program)
When the program data is less than n bytes, set FFh for the missing data.
No program data for the end of program
SUM (1 byte): Value that is calculated so the sum of command data is 00h



Error (1 byte): Error code
11h: SUM error
2Ah: Address error (the address is not in the selected area.)
53h: Program error (the data cannot be programmed.)

50.10.8.3 Data Area Program

This command is used to program the specified data to the data area. Set the lower 2 bits to 0 for the program address selected in this command. When the data length is shorter than 4 bytes, the data cannot be programmed. Fill the gaps with FFh.
When the program from the selected address is successfully completed, the MCU sends a response (06h). If the SUM of the received command does not match or an error occurs during a program operation, the MCU sends an error response.

To enter the program/erase host command wait state after the program operation ends, send 51h FFh FFh FFh FFh B4h from the host. The MCU sends a response (06h), and enters the program/erase host command wait state.

Command	51h	Program address	Program data length
	Program data		
	SUM		

Program address (4 bytes): Address for program destination
Set the lower 2 bits of the selected address to 0
Set FFFF FFFFh for end of data area program
Program data length (1 byte): Size of program data
Set 4-byte data
Set 00h for end of data area program
Program data (n bytes): Program data for the data area (n = program data length, 0 for end of program)
Set data of the program data length
When the program is less than n bytes, set FFh for the missing data.
No program data for the end of data area program
SUM (1 byte): Value that is calculated so the sum of command data is 00h

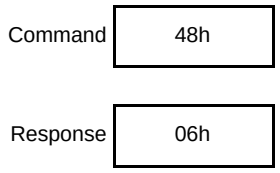
Response	06h

Error response	D1h	Error

Error (1 byte): Error code
11h: SUM error
2Ah: Address error (the address is not in the selected area.)
2Bh: Program data length error
53h: Program error (the data or program data cannot be programmed.)

50.10.8.4 Erase Preparation

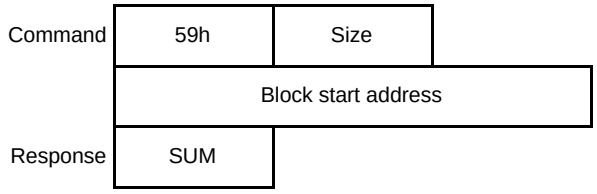
This command is used to prepare for accepting the block erase command. When the MCU receives this command, it recognizes that an instruction to prepare for the erase command is issued from the host. Then, the MCU enters the erase wait state, where only the block erase command can be accepted, and sends a response (06h).



50.10.8.5 Block Erase

This command is used to erase the selected block in the user area or data area. Specify the block start address selected in the command by calculating the address based on the response to the block information inquiry command.
When the block selected in the block start address is successfully erased, the MCU sends an error response (06h). If the SUM of the received command does not match or an error occurs during an erase operation, the MCU sends an error response.

To enter the program/erase host command wait state after the erase operation ends, send 59h 04h FFh FFh FFh FFh A7h from the host. The MCU enters the program/erase host command wait state and sends a response (06h).



Size (1 byte): Total bytes of Block start address (the value is always 04h)
Block start address (4 bytes): Start address of the block that is erased
Set FFFF FFFFh for end of erase
SUM (1 byte): Value that is calculated so the sum of response data is 00h

Error (1 byte): Error code
11h: SUM error
29h: Block start address error
51h: Erase error (the selected block cannot be erased)

50.10.9 Read-Check Commands

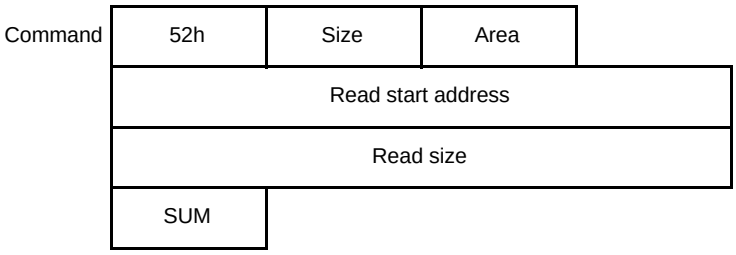
Read-check commands are used to read data or check whether data is programmed in the user area or data area in the MCU based on the response to inquiry commands.
Table 50.22 lists read-check commands used in the program/erase host command wait state.

Table 50.22 Read-Check Commands

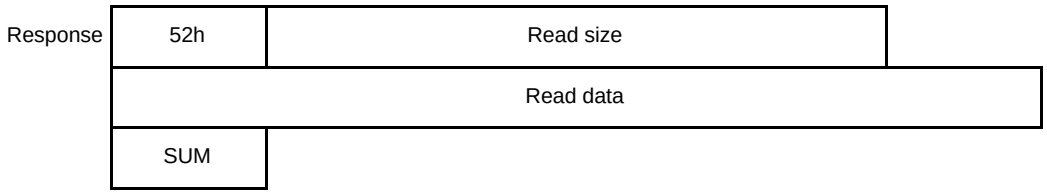
Command	Function
Memory read	Read data from the user area or data area.
User area checksum	Obtain the checksum of the entire user area.
Data area checksum	Obtain the checksum of the entire data area.
User area blank check	Check whether data is programmed in the user area.
Data area blank check	Check whether data is programmed in the data area.
Access window information program	Set the access window.
Access window read	Read the settings of the access window.

50.10.9.1 Memory Read

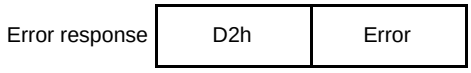
This command is used to read data programmed in the user area or data area. For a read start address selected in the command, set a value within the range from the area start address to the area end address received in the response to the user area information inquiry command or the data area information inquiry command.
For a read size selected in the command, set a value so the sum of the read start address and the read size is within the range from the area start address to the area end address in the response to the user area information inquiry command or the data area information inquiry command.
When the MCU performs a read successfully, it sends data of the specified range. If the SUM of the received command does not match or the MCU fails to perform a read successfully, it sends an error response.



Size (1 byte): Total bytes for Read start address and Read size
Area (1 byte): Area that is read
01h: User area or data area
Read start address (4 bytes): Start address of the area that is read
Read size (4 bytes): Size of data that is read (in bytes)
SUM (1 byte): Value that is calculated so the sum of response data is 00h



Read size (4 bytes): Size of Data that is read (in bytes)
Read data (n bytes): Data read from the specified range (n = read size)
SUM (1 byte): Value that is calculated so the sum of response data is 00h

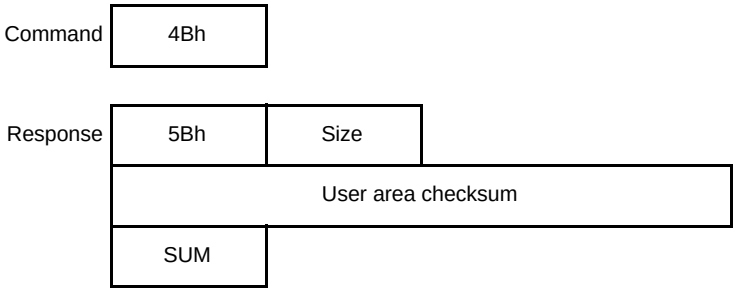


Error (1 byte): Error code
11h: SUM error
2Ah: Address error
- A value other than 01h is set for the “Area” field.
- The read start address is not in the selected area.

2Bh: Size error
- The read size is set to 0000 0000h.
- The read size exceeds the area size.
- The address calculated from the read start address and read size is not in the selected area.

50.10.9.2 User Area Checksum

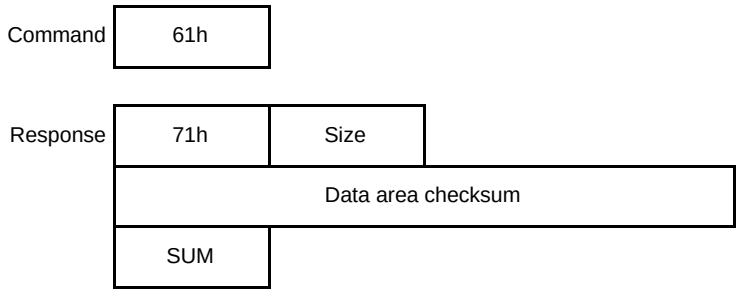
This command used to obtain the checksum of the entire user area. When the MCU receives this command, it adds data from the start address to the end address in bytes in the user area, and sends the calculated result (checksum) as a response.



Size (1 byte): Number of bytes for checksum of the user area (the value is always 04h)
User area checksum (4 bytes): Calculated result of the data in the user area in bytes
SUM (1 byte): Value that is calculated so the sum of response data is 00h

50.10.9.3 Data Area Checksum

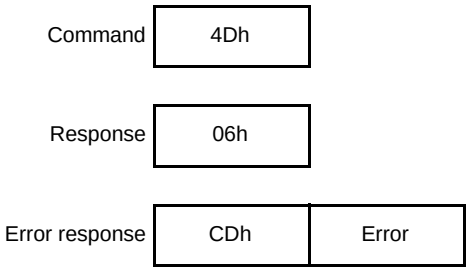
This command used to obtain the checksum of the entire data area. When the MCU receives this command, it adds data from the start address to the end address in bytes in the data area, and sends the calculated result (checksum) as a response.



Size (1 byte): Number of bytes for checksum of the data area (the value is always 04h)
Data area checksum (4 bytes): Calculated result of the data in the data area in bytes
SUM (1 byte): Value that is calculated so the sum of response data is 00h

50.10.9.4 User Area Blank Check

This command is used to check whether data is programmed in the user area.
When the MCU receives this command, it checks whether there is data in the entire user area. If there is no programmed data, the MCU sends a response (06h). If there is at least 1 byte of programmed data, the MCU sends an error response.



Error (1 byte): Error code
52h: Not blank

50.10.9.5 Data Area Blank Check

This command is used to check whether data is programmed in the user area.
When the MCU receives this command, it checks whether there is programmed data in the entire user area. If there is no programmed data, the MCU sends a response (06h). If there is at least 1 byte of programmed data, the MCU sends an error response.

Command	62h	
Response	06h	
Error response	E2h	Error

Error (1 byte): Error code
52h: Not blank

50.10.9.6 Access Window Information Program

This command is used to set the access window used for area protection. For the access window start address selected in the command, set the start address of the start block. For the access window end address, set the end address of the end block.
When the specified access window settings are successfully completed, the MCU sends a response (06h). If the SUM of the received command does not match or an error occurs during the access window settings, the MCU sends an error response.
For details on the access window, see section 50.6, Area Protection.

Command	74h	05h	Access window	
	Access window start address LH	Access window start address HL	Access window end address LH	Access window end address HL
	SUM			

Access window (1 byte): Set the access window or clear the access window settings
Set 00h to set the access window
Set FFh to clear the access window settings
Access window start address LH (1 byte): Start address of the access window (A15 to A8)
Set A15 to A8 of the start address of the start block.
Set FFh to clear the access window settings
Access window start address HL (1 byte): Start address of the access window (A23 to A16)
Set A23 to A16 of the start address of the start block.
Set FFh to clear the access window settings
Access window end address LH (1 byte): End address of the access window (A15 to A8)
Set A15 to A8 of the end address of the end block.
Set FFh to clear the access window settings
Access window end address HL (1 byte): End address of the access window (A23 to A16)
Set A23 to A16 of the end address of the end block.
Set FFh to clear the access window settings
SUM (1 byte): Value that is calculated so the sum of response data is 00h

Response	06h	
Error response	F4h	Error

Error (1 byte): Error code
11h: SUM error
2Ah: Address error (specified address is not in the area)
53h: Program error (access window cannot be set)

50.10.9.7 Access Window Read

This command is used to check the set range of the access window.
When the MCU successfully obtains the access window range, the MCU sends the access window start address and end address that it read. If the SUM of the received command does not match, the MCU sends an error response.

Command	73h	01h	FFh	8Dh

Response	73h	05h		
	Access window start address LH	Access window start address HL	Access window end address LH	Access window end address HL
	FFh			
	SUM			

Access window start address LH (1 byte): Start address of the access window range (A15 to A8)
Access window start address HL (1 byte): Start address of the access window range (A23 to A16)
Access window end address LH (1 byte): End address of the access window range (A15 to A8)
Access window end address HL (1 byte): End address of the access window range (A23 to A16)
SUM (1 byte): Value that is calculated so the sum of response data is 00h

Error response	F3h	Error

Error (1 byte): Error code
11h: SUM error

50.11 Serial Programmer Operation in Boot Mode (SCI Interface)

The following describes the procedure for the serial programmer to program/erase the user area and data area in boot mode (SCI Interface).

1. Automatically adjust the bit rate
2. Receive the MCU information*1
3. Select the device and change the bit rate
4. Enter the program/erase host command wait state
5. Unlock boot mode ID code protection
6. Erase the user area and data area*2, *3
7. Program the user area and data area*2, *3
8. Check data in the user area*2
9. Check data in the data area*2
10. Set the access window in the user area
11. Reset the MCU

Note 1. If the necessary information has been already received, step 2 can be skipped.
Note 2. Processing steps from 6 to 10 can be proceeded as necessary, and their order can be changed.
Note 3. When a timeout occurs or invalid response data is received, stop the operation and perform step 11 (reset the MCU).

Refer to section 50.10.5, Inquiry Commands, section 50.10.6, Setting Commands, section 50.10.7, ID Code Authentication Command, section 50.10.8, Program/Erase Commands, and section 50.10.9, Read-Check Commands for details on the commands used in the above steps 2 to 10.

50.11.1 Bit Rate Automatic Adjustment Procedure

The MCU measures the low width of data 00h that is sent from the serial programmer at 9,600 or 19,200 bps to automatically adjust the bit rate.

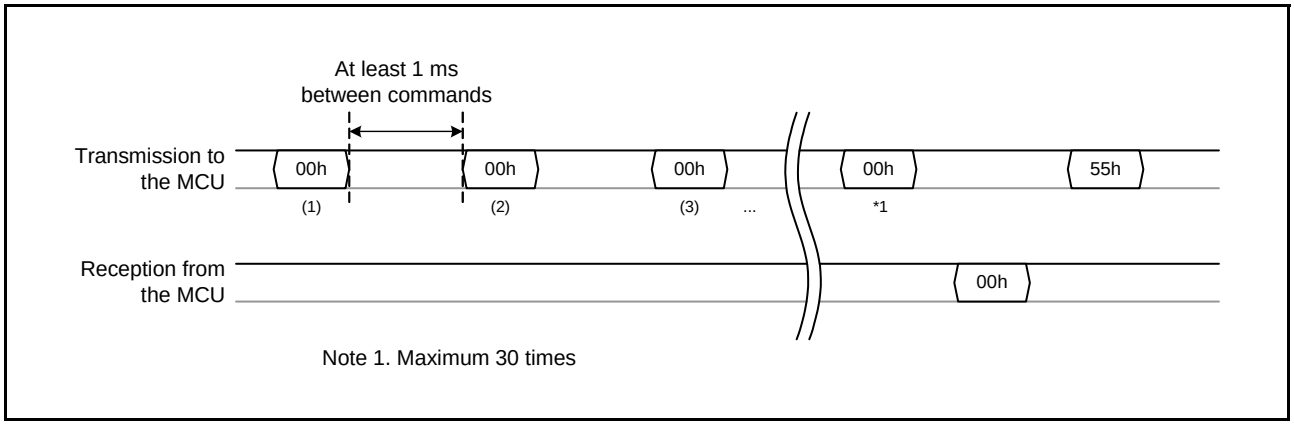


Figure 50.31 Transmit/Receive Data for Bit Rate Automatic Adjustment

After starting up in boot mode, wait for at least 400 ms and then send 00h to the MCU from the serial programmer. When the bit rate adjustment is completed, the MCU sends 00h to the programmer. When the programmer receives 00h, send 55h to the MCU from the programmer. When the programmer can not receive 00h, wait for at least 1 ms and send 00h to the MCU again. When the programmer fails to receive 00h even if it send 00h 30 times, restart the MCU in boot mode and perform the automatic adjustment for the bit rate again.
When the MCU receives 55h, the MCU sends E6h and enters the inquiry/setting command wait state. If the MCU fails to receive 55h, the MCU sends FFh. When the programmer receives FFh, restart the MCU in boot mode, and perform the automatic adjustment for the bit rate again.

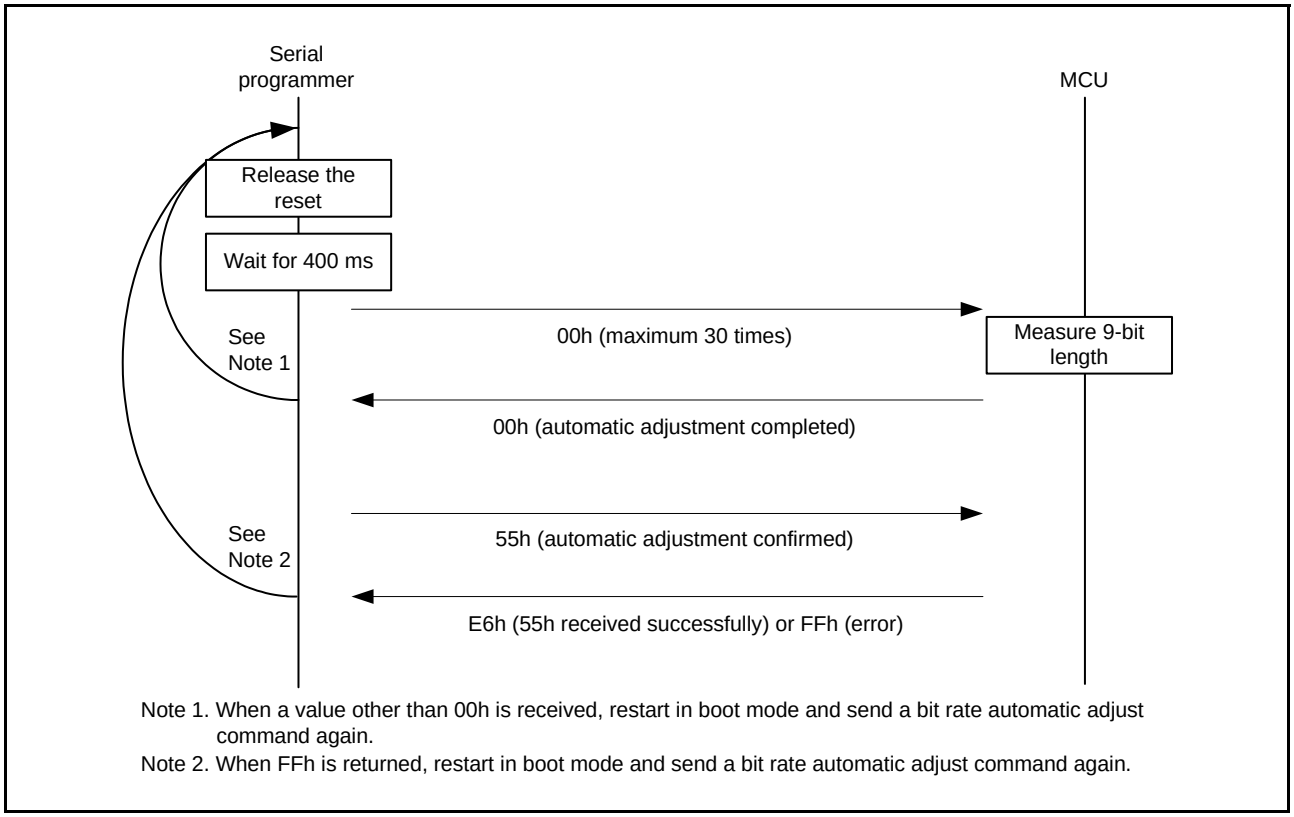


Figure 50.32 Bit Rate Automatic Adjustment Procedure

50.11.2 Procedure to Receive the MCU Information

Procedure to send inquiry commands, and receive the information necessary to send setting commands, program/erase commands, and read-check commands is as follows.

(1) Send a support device inquiry command (20h) to check what type of endianness the MCU supports. The MCU returns all device codes and series names that it supports.
(2) Send a user area information inquiry command (25h) to check the start and end addresses of the user area. The MCU returns the start and end addresses of the user area.
(3) Send a block information inquiry command (26h) to check the block configuration. The MCU returns the start address, the size of one block, and the number of blocks for the user area and data area.
(4) Send a data area information inquiry command (2Bh) to check the start and end addresses of the data area. The MCU returns the start and end addresses of the data area.

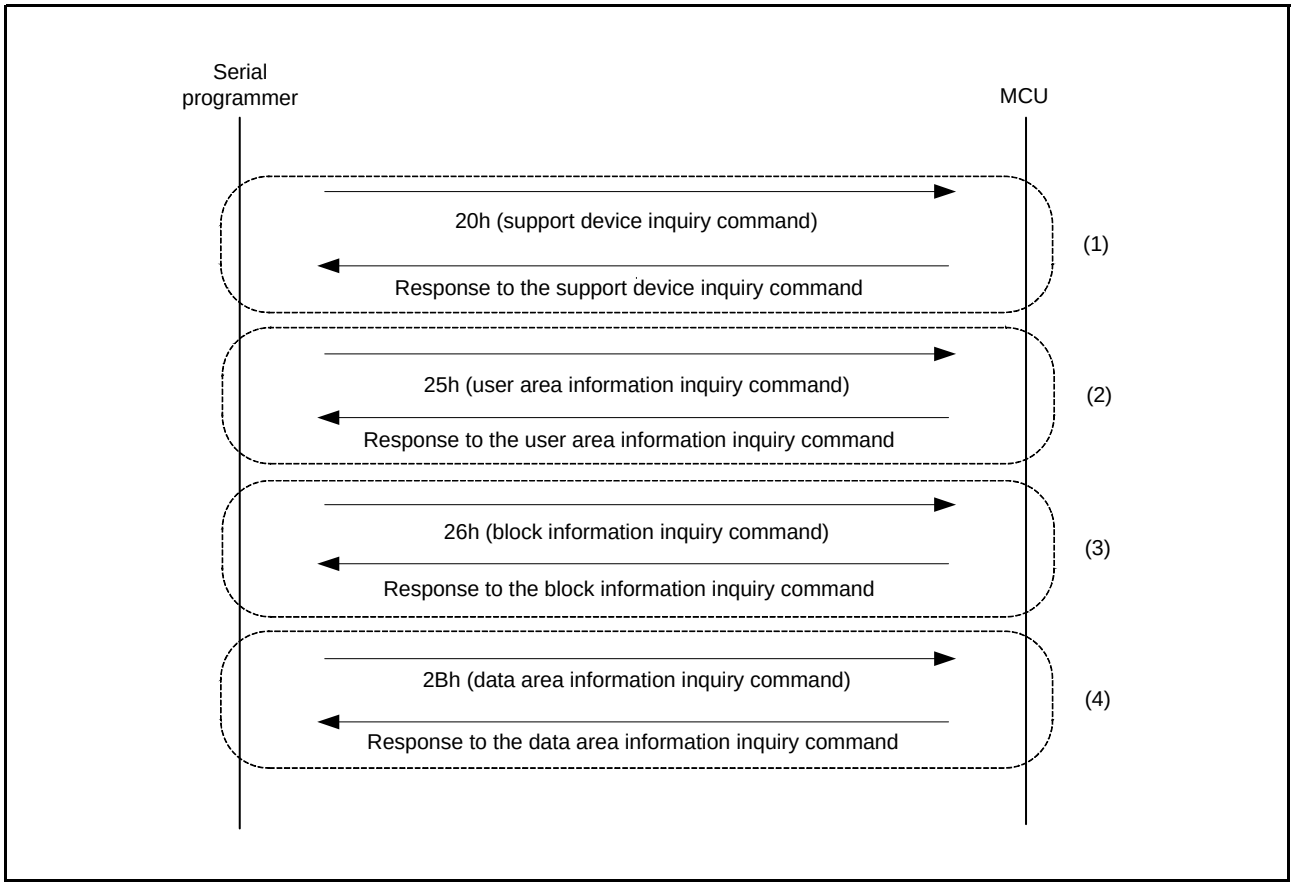


Figure 50.33 Procedure to Receive the MCU Information

50.11.3 Procedure to Select the Device and Change the Bit Rate

Procedure to select the device to connect with the serial programmer and to change the bit rate for communication is as follows.

(1) Send the device select command (10h). Select the device code according to the endian of developed software.
(2) Send the operating frequency select command (3Fh) to change the communication bit rate from 9,600 or 19,200 bps.

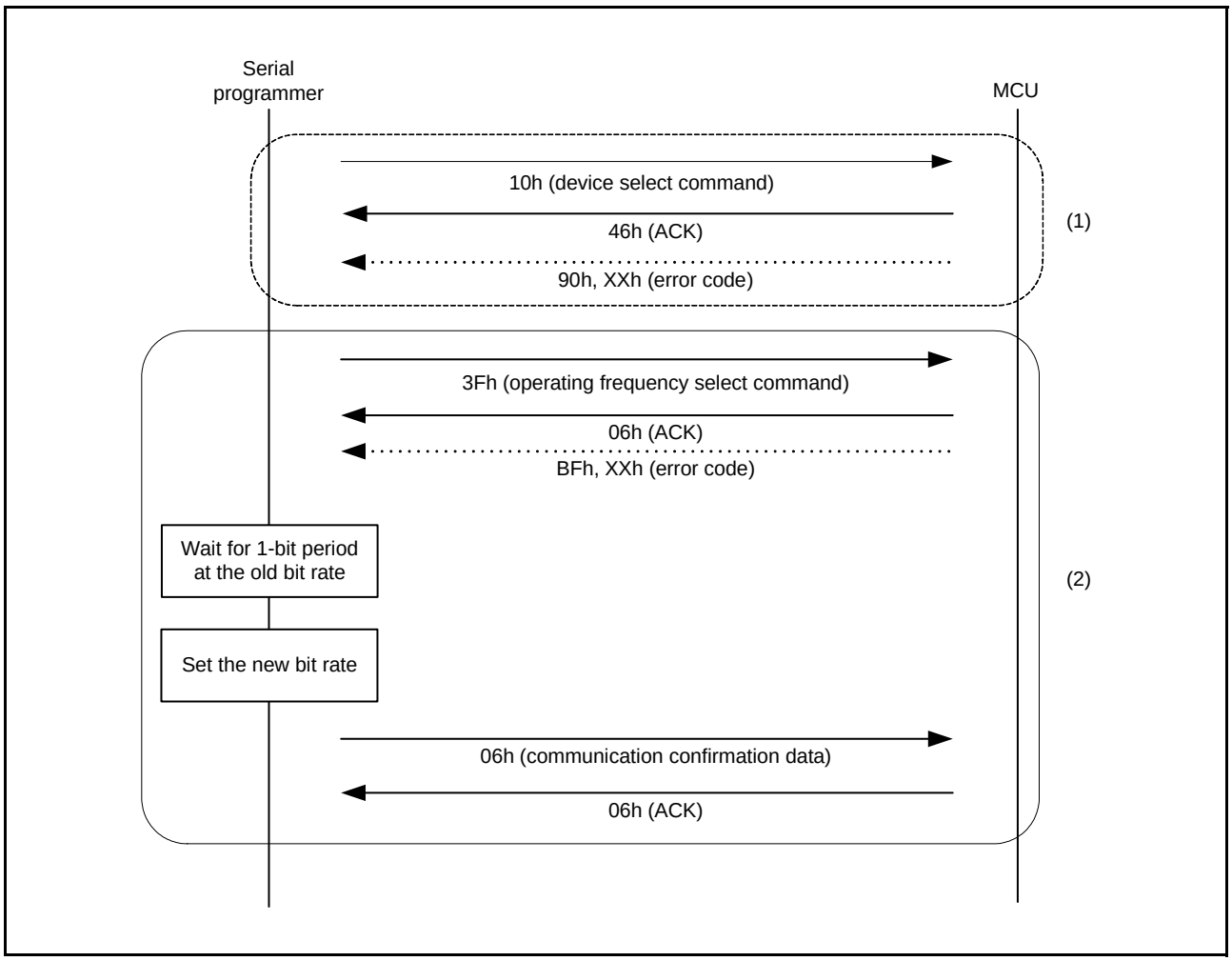


Figure 50.34 Procedure to Select the Device and Change the Bit Rate

50.11.4 Procedure for Transition to the Program/Erase Host Command Wait State

Send the program/erase host command wait state transition command to perform program/erase operations. The MCU sends a response according to whether boot mode ID code protection is enabled or disabled.

(1) When boot mode ID code protection is disabled, the MCU sends a response (06h), and enters the program/erase host command wait state. Use the serial programmer to start from the operation described in section 50.11.6, Procedure to Erase the User Area and Data Area.

(2) When the boot mode ID code protection is enabled, the MCU sends a response (16h), and enters the ID code authentication wait state. Use the serial programmer to start from the operation described in section 50.11.5, Procedure to Unlock Boot Mode ID Code Protection.

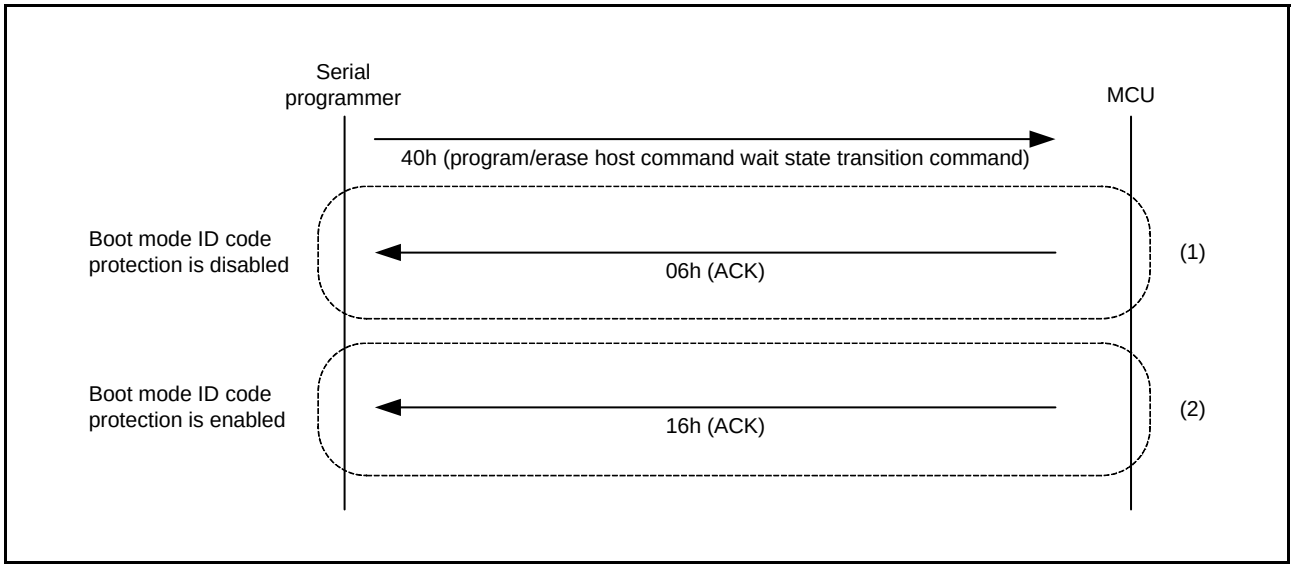


Figure 50.35 Procedure to Transition to the Program/Erase Host Command Wait State

50.11.5 Procedure to Unlock Boot Mode ID Code Protection

Send the ID code check command to unlock boot mode ID code protection.

(1) When ID codes match, the MCU enters the program/erase host command wait state. Data in the user area and data area are not erased. Use the serial programmer to start from the operation described in section 50.11.6, Procedure to Erase the User Area and Data Area.

(2) If ID codes do not match consecutively, the MCU remains in the boot mode ID code authentication state. Reset the MCU, and then use the serial programmer to start again from section 50.11.1, Bit Rate Automatic Adjustment Procedure.

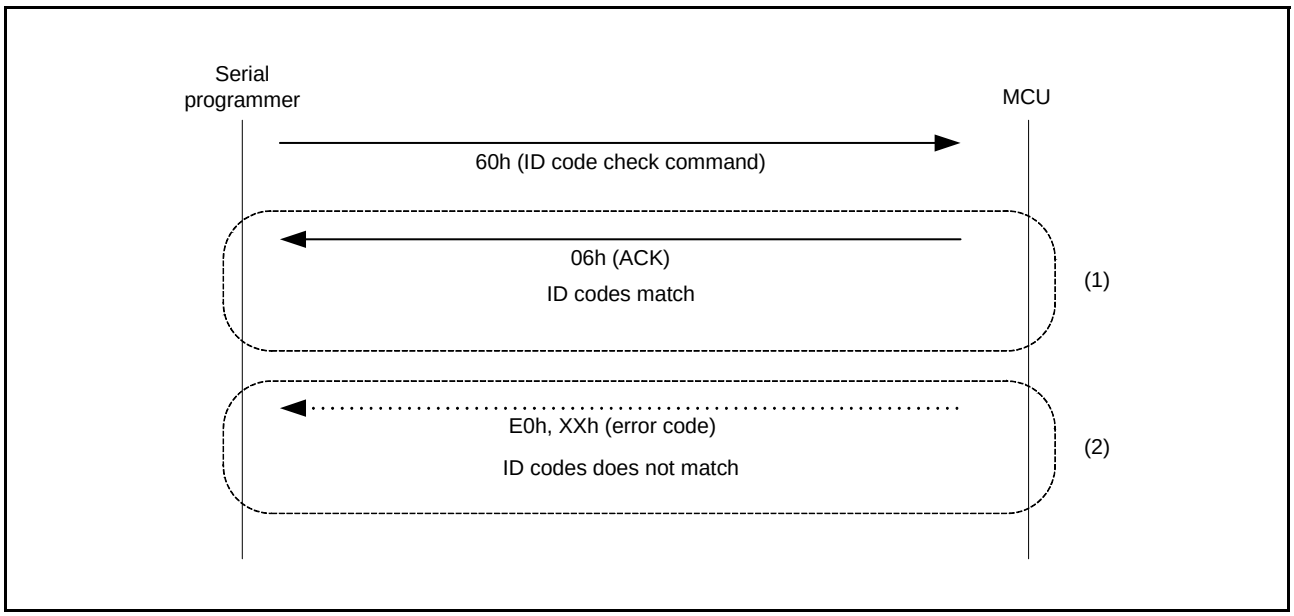


Figure 50.36 Procedure to Unlock ID Code Protection

50.11.6 Procedure to Erase the User Area and Data Area

Procedure to erase blocks that are programmed in the user area and data area to program a user program and data is as follows.

(1) Send an erase preparation command (48h).
(2) Send a block erase command (59h).
(3) To place the MCU in the program/erase host command wait state, send a block erase command for ending the erasure (59h 04h FFh FFh FFh FFh A7h).

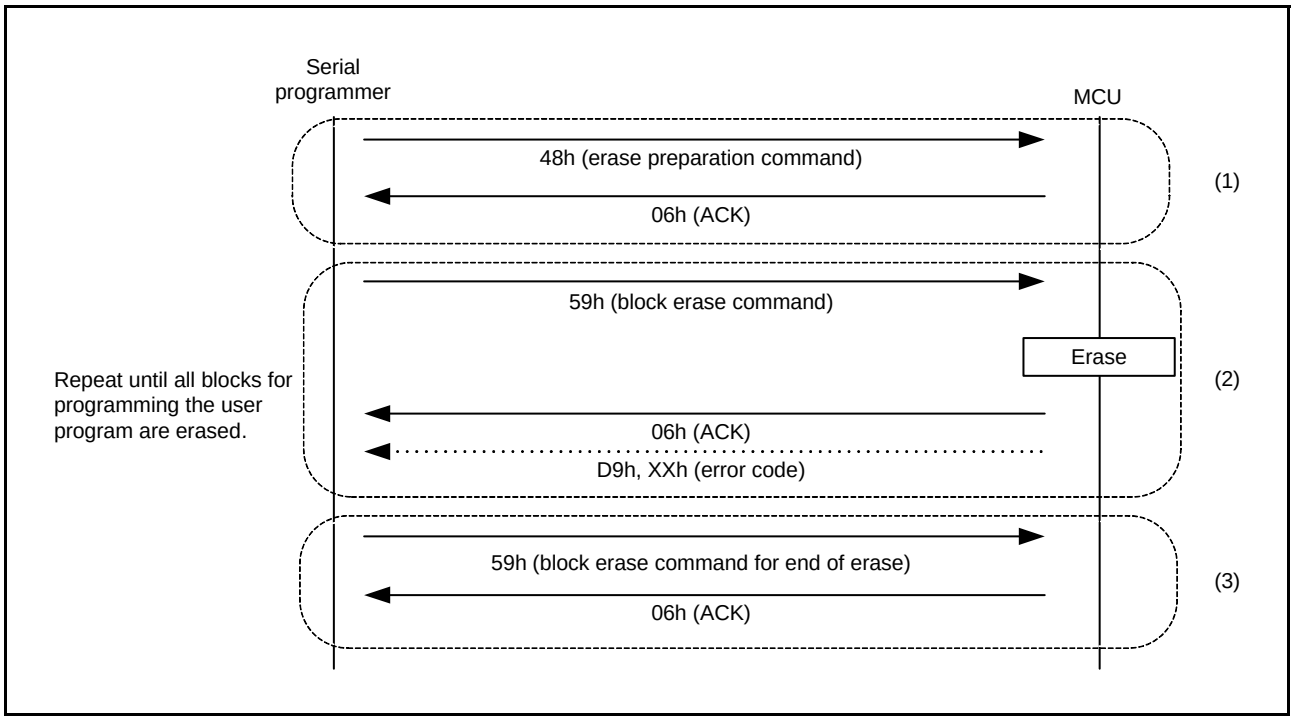


Figure 50.37 Procedure to Erase the User Area and Data Area

50.11.7 Procedure to Program the User Area and Data Area

Procedure to program a user program and data in the user area and data area is as follows.

(1) Send the user/data area program preparation command (43h).
(2) Send the program command (50h) or the data area program command (51h).
(3) To place the MCU in the program/erase host command wait state, send the program command (50h FFh FFh FFh FFh B4h) or the data area program command (51h FFh FFh FFh FFh 00h B3h) for ending the programming.

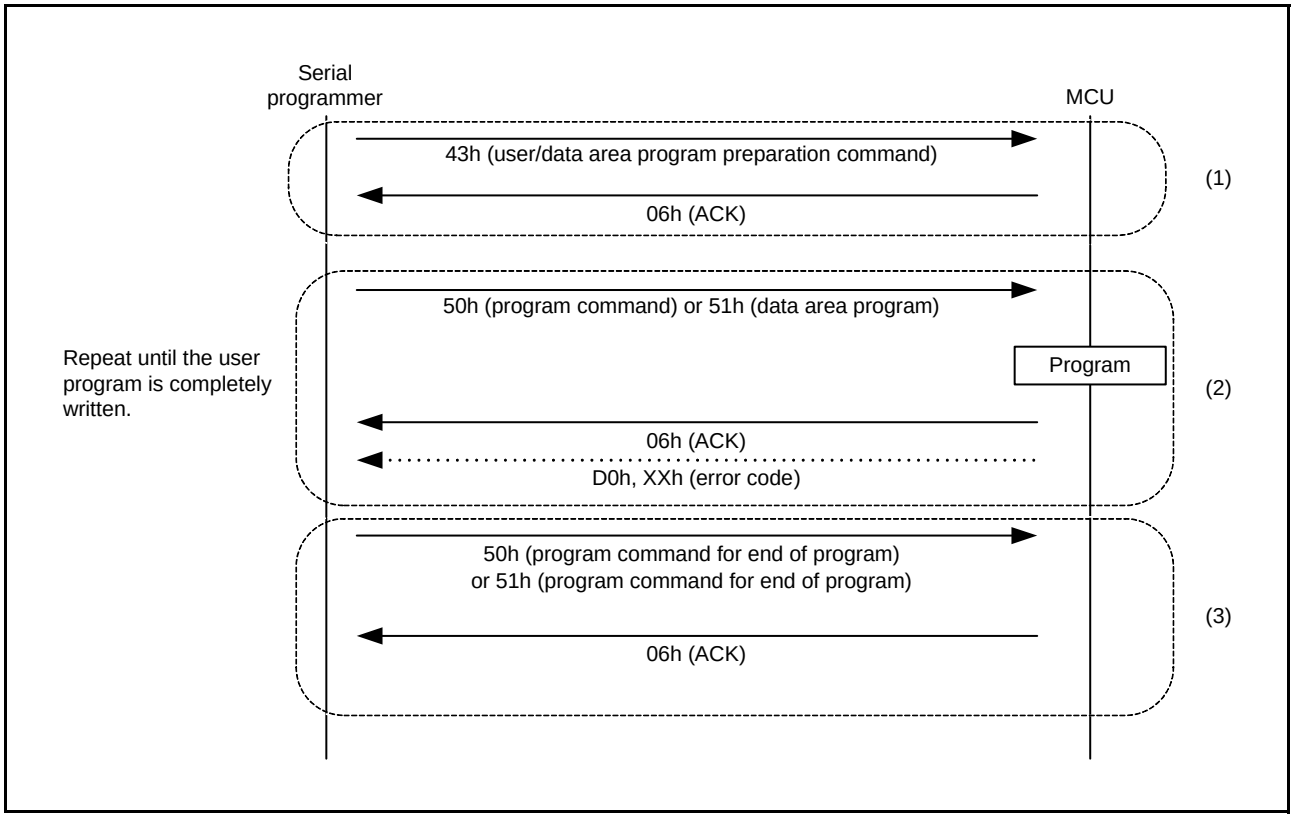


Figure 50.38 Procedure to Program the User Area and Data Area

50.11.8 Procedure to Check Data in the User Area

Procedure to read and check, checksum, and blank check the user area to check the programmed data in the user area is as follows.

(1) The read and check operation is used to read data in the user area and compare the read data with the programmed data to check if the program operation is performed successfully. Send a memory read command (52h) to read data in the user area.
(2) Send the user area checksum command (4Bh) to check program data using the checksum of user area.
(3) Send a user area blank check command (4Dh) to check if the user area has data.

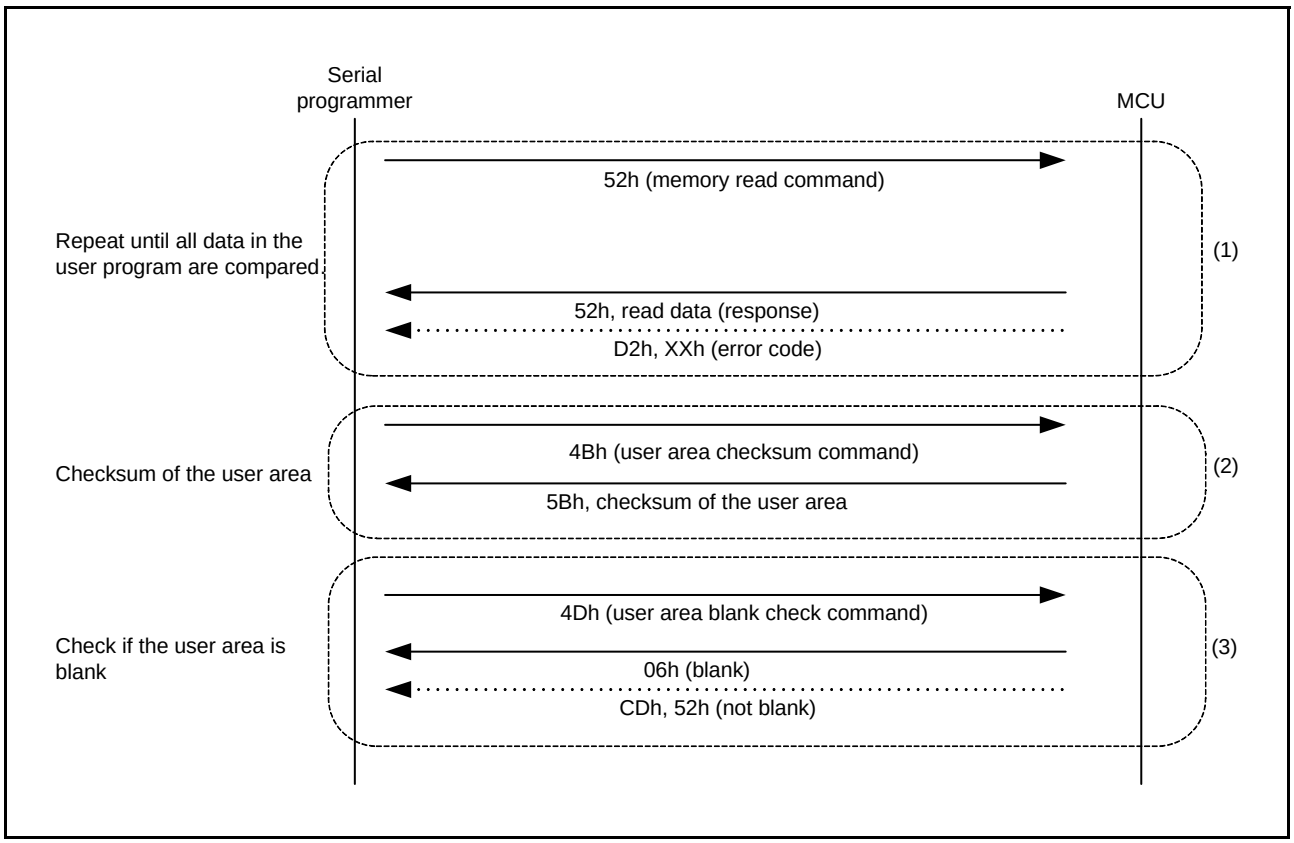


Figure 50.39 Procedure to Check Data in the User Area

50.11.9 Procedure to Check Data in the Data Area

Procedure to read and check, checksum, and blank check the data area to check the programmed data in the data area is as follows.

(1) The read and check operation is used to read data in the data area and compare the read data with the programmed data to check if the program operation is performed successfully. Send a memory read command (52h) to read data in the data area.
(2) Send the data area checksum command (61h) to check program data using the checksum of data area.
(3) Send the data area blank check command (62h) to check if the data area has data.

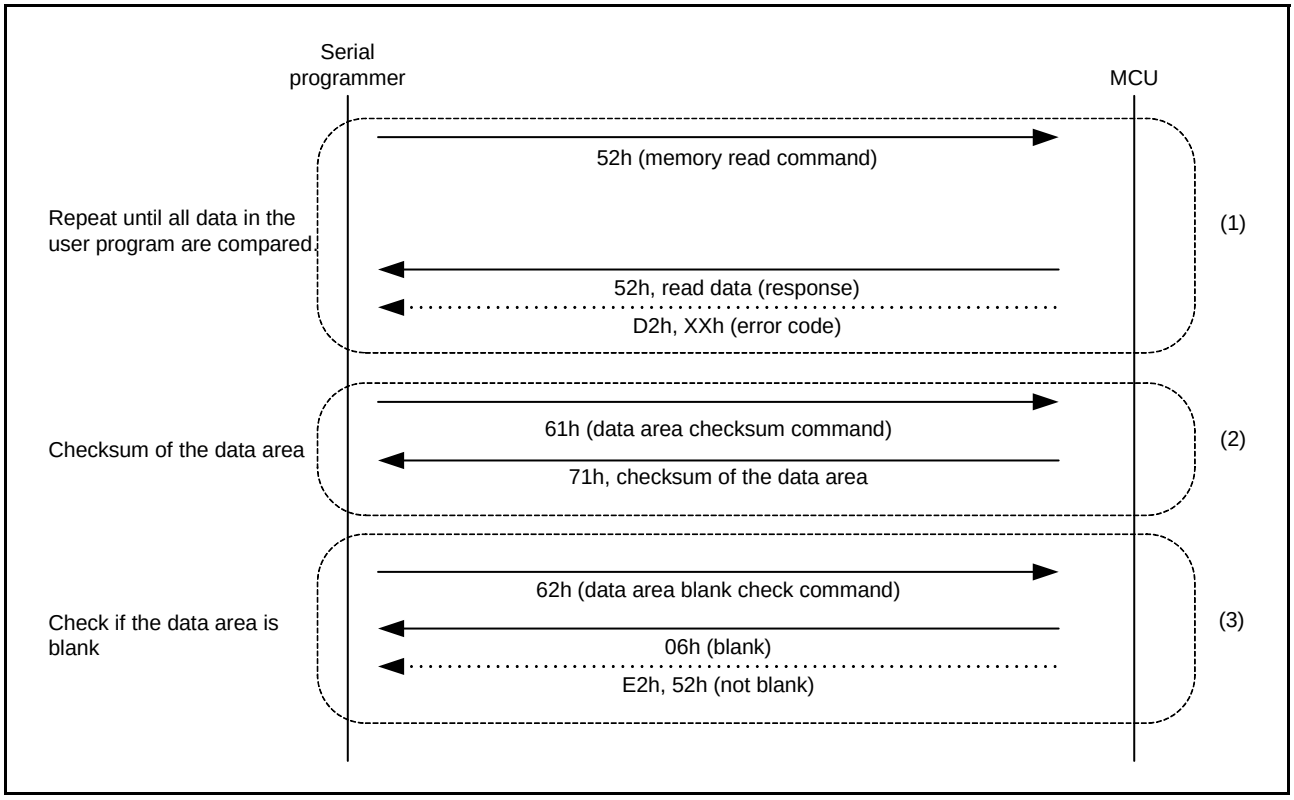


Figure 50.40 Procedure to Check Data in the Data Area

50.11.10 Procedure to Set the Access Window in the User Area

Procedure to set the access window to avoid unintentionally rewriting the user area during the self-programming is as follows.

(1) Send the access window program command (74h) to set the access window settings.
(2) Send the access window read command (73h) to confirm the access window settings.

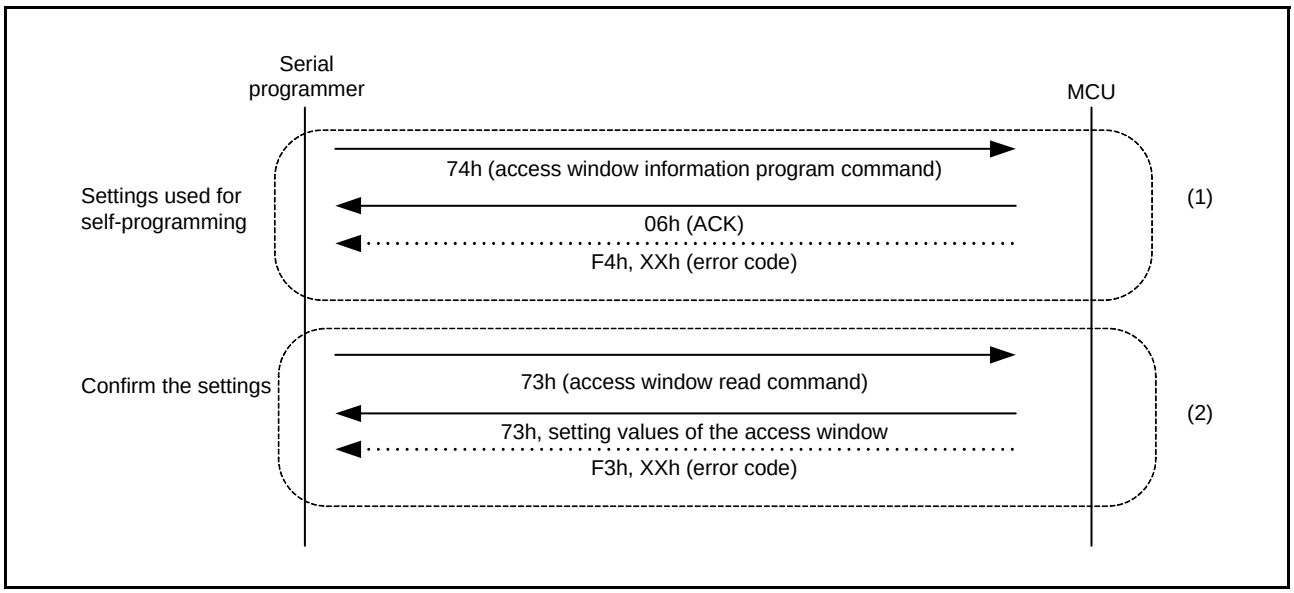
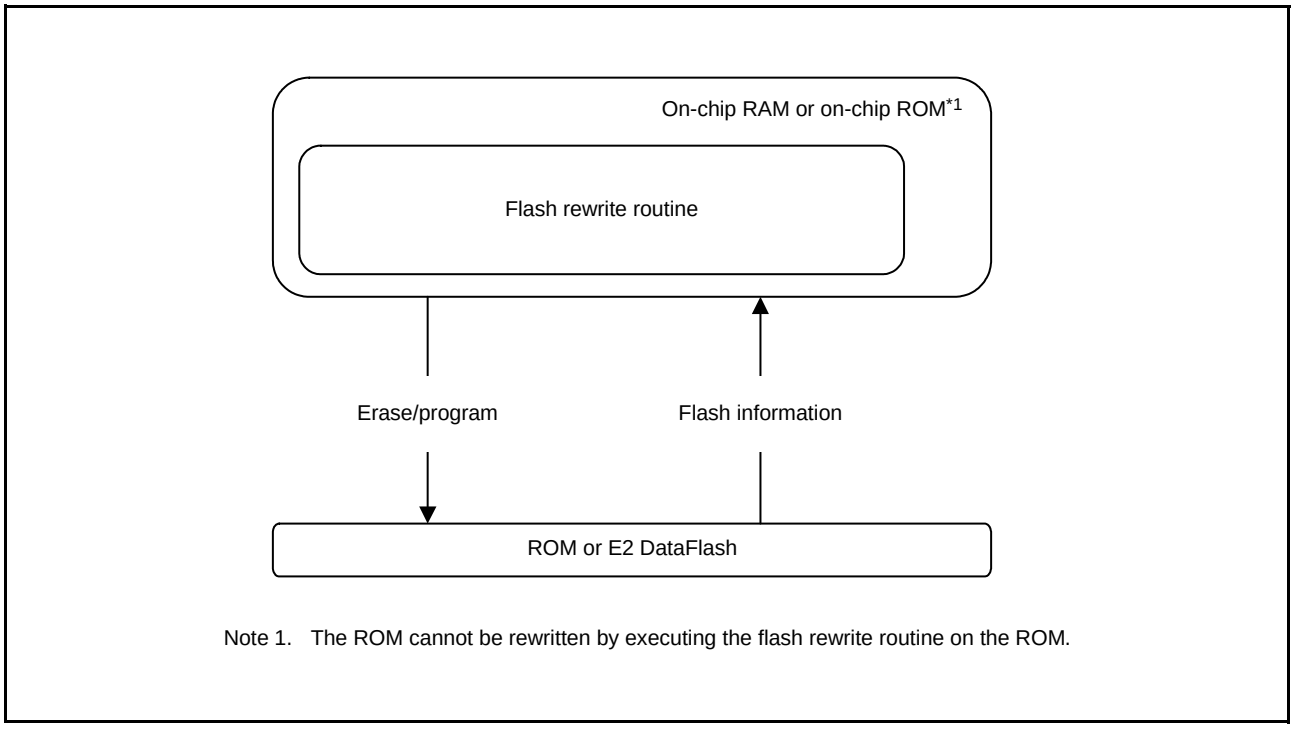


Figure 50.41 Procedure to Set the Access Window in the User Area

50.12 Rewriting by Self-Programming

50.12.1 Overview

The MCU supports rewriting of the flash memory by the user program. The ROM and E2 DataFlash can be rewritten by preparing a routine to rewrite the flash memory (flash rewrite routine) in the user program.
When rewriting the E2 DataFlash, the BGO can be used to execute the flash rewrite routine on the ROM. The E2 DataFlash can also be rewritten by executing the flash rewrite routine that is transferred on the RAM in advance.



Note 1. The ROM cannot be rewritten by executing the flash rewrite routine on the ROM.

Figure 50.42 Self-Programming Overview

50.13 Usage Notes

(1) Access the Block Where Erase Operation is Forcibly Stopped
When forcibly stopping an erase operation, data in the block where the erase operation is aborted is undefined. To avoid malfunctions caused by reading undefined data, do not execute instructions or read data in the block where an erase operation is forcibly stopped.

(2) Processing After Forced Stop of Erase Operation
When an erase operation is forcibly stopped, issue a block erase command again to the same block.

(3) Additional Programming Disabled
The same address cannot be programmed more than once. When programming an area that has been already programmed, erase the area first.

(4) Reset during Program/Erase
If inputting a reset from the RES# pin, release the reset after reset input time of at least tRESW (refer to section 51, Electrical Characteristics) within the range of the operating voltage defined in the electrical characteristics.
The IWDT reset and software reset can be used regardless of tRESW.

(5) Location of Interrupt Vectors and Exception Vectors during Program/Erase Operation
When an interrupt or an exception occurs during a program/erase operation, the vector may be fetched from the ROM. To avoid fetching the vector from the ROM, allocate the interrupt vector table and exception vector table to the area other than the ROM with the INTB and EXTB registers in the CPU.

(6) Program/Erase in Low-Speed Operating Mode
Do not program or erase the flash memory when low-speed operating mode is selected by the SOPCCR register for low-power consumption functions.

(7) Abnormal Termination during Program/Erase
When the voltage exceeds the range of the operating voltage during a program/erase operation or when a program/erase operation is not completed successfully due to a reset or prohibited actions described in (8), erase the area again.

(8) Actions Prohibited during Program/Erase
To prevent the damage to the flash memory, comply with the following instructions.

- Do not use the MCU power supply that is outside the operating voltage range.
- Do not update the value of the OPCCR.OPCM[2:0] bits.
- Do not update the value of the SOPCCR.SOPCM bit.
- Do not change the clock source select bit in the SCKCR3 register.
- Do not enable switching clock sources by setting the RSTCKCR.RSTCKEN bit when exiting sleep mode.
- Do not change the division ratio of the flash interface clock (FCLK).
- Do not place the MCU in deep sleep mode or software standby mode.
- Do not access the E2 DataFlash during a program/erase operation to the ROM.
- Do not change the DFLCTL.DFLEN bit value during a program/erase operation to the E2 DataFlash.

(9) FCLK during Program/Erase
For programming/erasure by self-programming, set the frequency of the FlashIF clock (FCLK), and specify an integer FCLK frequency (MHz) in FISR.PCKA[4:0] bits. Note that when the FCLK is 4 to 32 MHz, a rounded-up value should be set for a non-integer frequency such as 12.5 MHz (i.e. 12.5 MHz should be set rounded up to 13 MHz). If the FCLK is equal to or less than 4 MHz, only 1, 2, 3, or 4 MHz can be used.

50.14 Usage Notes in Boot Mode

(1) Notes on Communication Errors in Boot Mode
When communication with the MCU cannot be performed properly, reset and start up in boot mode again.

(2) Notes on Power Supply Voltage in Boot Mode (SCI Interface)
When the bit rate exceeds 500 kbps in boot mode (SCI Interface), use a voltage that is 3.0 V or higher.

(3) Notes on Option-Setting Memory in Boot Mode
The settings of option function select register 0 (OFS0), option function select register 1 (OFS1), and endian select register (MDE) are disabled in boot mode.

(4) Notes on Clocks in Boot Mode (USB Interface)
When USB interface mode is selected, externally input a clock to the EXTAL or XTAL pin, or connect a crystal or ceramic resonator to supply a clock.
Use a 4, 6, 8, 12, or 16 MHz external clock in boot mode (USB interface). An clock other than a 4, 6, 8, 12, or 16 MHz external clock cannot be used.

(5) Notes on Power Supply Voltage in Boot Mode (USB Interface)
Use a voltage between 3.0 V and 3.6 V in boot mode (USB interface). A voltage that is lower than 3.0 V cannot be used.

(6) Notes on Switching the Start-Up Area
Switch the start-up area by self-programming.

51. Electrical Characteristics

51.1 Absolute Maximum Ratings

Table 51.1 Absolute Maximum Ratings

Conditions: VSS = AVSS0 = VREFL0 = VSS_USB = VSS_RF = 0 V

Item		Symbol	Value	Unit
Power supply voltage		VCC, VCC_USB	–0.3 to +4.0	V
VBATT power supply voltage		VBATT	–0.3 to +4.0	V
Input voltage	Ports for 5 V tolerant*1	V_{in}	–0.3 to +6.5	V
	P03, P05, P07, P40 to P47		–0.3 to AVCC0 + 0.3	
	ANT		–1.0 to +1.4	
	XTAL1_RF, XTAL2_RF		–0.3 to +1.4	
	DCLIN_A, DCLIN_D		–0.3 to +2.2	
	Ports other than above		–0.3 to VCC + 0.3	
Reference power supply voltage		VREFH0	–0.3 to AVCC0 + 0.3	V
Analog power supply voltage		AVCC0	–0.3 to +4.0	V
		VCC_RF	–0.3 to +4.0	V
		AVCC_RF	–0.3 to +4.0	V
Analog input voltage	When AN000 to AN007 are used	V_{AN}	–0.3 to AVCC0 + 0.3	V
	When AN016 to AN020, AN027 are used		–0.3 to VCC + 0.3	
Operating temperature		T_{opr}	–40 to +85	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the MCU may be caused if absolute maximum ratings are exceeded.

To preclude any malfunctions due to noise interference, insert capacitors with high frequency characteristics between the VCC and VSS pins, between the AVCC0 and AVSS0 pins, between the VCC_USB and VSS_USB pins, between the VREFH0 and VREFL0 pins, between the VCC_RF and VSS_RF pins, and between the AVCC_RF and VSS_RF pins. Place capacitors with values of about 2.2 µF in the case of the VCC_RF pin and about 0.1 µF otherwise as close as possible to every power supply pin, and use the shortest and thickest possible traces for the connections.

Connect the VCL pin to a VSS pin via a 4.7 µF capacitor. The capacitor must be placed close to the pin. For details, refer to section 51.16.1, Connecting VCL Capacitor and Bypass Capacitors.

Do not input signals or an I/O pull-up power supply to ports other than 5-V tolerant ports while the device is not powered. The current injection that results from input of such a signal or I/O pull-up may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Even if –0.3 to +6.5 V is input to 5-V tolerant ports, it will not cause problems such as damage to the MCU.

Note 1. Ports 16, 17, 30, 31, and B5 are 5 V tolerant.

Table 51.2 Recommended Operating Voltage Conditions

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltages	VCC*1, *2, *3	When USB is not used	1.8	—	3.6	V
		When USB is used	3.0	—	3.6	
	VSS		—	0	—	
USB power supply voltages	VCC_USB	When USB regulator is not used	—	VCC	—	V
	VSS_USB		—	0	—	
VBATT power supply voltage	VBATT		1.8	—	3.6	V
Analog power supply voltages	AVCC0*1, *2		1.8	—	3.6	V
	AVSS0		—	0	—	
	VREFH0		1.8	—	AVCC0	
	VREFL0		—	0	—	
BLE power supply voltages	VCC_RF*3		1.8	—	3.6	V
	AVCC_RF*3		1.8	—	3.6	
	VSS_RF		—	0	—	

Note 1. P41 and P47: Set AVCC0 to the same voltage as VCC.
If conditions other than those above are applicable, those listed below apply.
While VCC > 2.4 V: AVCC and VCC can be set independently when AVCC0 ≥ 2.4 V
While VCC ≤ 2.4 V: AVCC and VCC can be set independently when AVCC0 ≥ VCC
Note 2. When powering on the VCC and AVCC0 pins, power them on at the same time or the VCC pin first and then the AVCC0 pin.
Note 3. Set VCC_RF and AVCC_RF to the same voltage as VCC.

51.2 DC Characteristics

Table 51.3 DC Characteristics (1)

Conditions: 2.7 V ≤ VCC = VCC_USB = VCC_RF = AVCC_RF ≤ 3.6 V, 2.7 V ≤ AVCC0 ≤ 3.6 V,
VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	RIIC input pin (except for SMBus, 5 V tolerant)		V_{IH}	VCC × 0.7	—	5.8	V	
	Ports 16, 17, port B5 (5 V tolerant)			VCC × 0.8	—	5.8		
	Ports 14, 15, ports 21, 22, 25 to 27, ports 35 to 37, ports B0, B1, B3, B5, B7, ports C0, C2 to C7, ports D3, ports E0 to E4, port J3, Ports 30, 31 (when time capture event input is not selected), RES#			VCC × 0.8	—	VCC + 0.3		
	Ports 03, 05, 07, ports 40 to 47			AVCC0 × 0.8	—	AVCC0 + 0.3		
	Ports 30, 31 (when time capture event input is selected)	When VCC is supplied		VCC × 0.8	—	VCC + 0.3		
		When VBATT is supplied		VBATT × 0.8	—	VBATT + 0.3		
	Ports 03, 05, 07, ports 40 to 47		V_{IL}	–0.3	—	AVCC0 × 0.2		
	RIIC input pin (except for SMBus)			–0.3	—	VCC × 0.3		
	Other than RIIC input pin or ports 30, 31			–0.3	—	VCC × 0.2		
	Ports 30, 31 (when time capture event input is selected)	When VCC is supplied		–0.3	—	VCC × 0.3		
		When VBATT is supplied		–0.3	—	VBATT × 0.3		
	Ports 03, 05, 07, ports 40 to 47		ΔV_T	AVCC0 × 0.1	—	—		
	RIIC input pin (except for SMBus)			VCC × 0.05	—	—		
	Ports 16, 17, Port B5			VCC × 0.05	—	—		
	Other than RIIC input pin			VCC × 0.1	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD		V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL (external clock input)			VCC × 0.8	—	VCC + 0.3		
	RIIC input pin (SMBus)			2.1	—	VCC + 0.3		
	MD		V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL (external clock input)			–0.3	—	VCC × 0.2		
	RIIC input pin (SMBus)			–0.3	—	0.8		

Table 51.4 DC Characteristics (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = VCC_RF = AVCC_RF ≤ 2.7 V, 1.8 V ≤ AVCC0 < 2.7 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Ports 16, 17, port B5 (5 V tolerant)	V_{IH}	VCC × 0.8	—	5.8	V	
	Ports 14, 15, ports 21, 22, 25 to 27, ports 30, 31, 35 to 37, ports B0, B1, B3, B5, B7, ports C0, C2 to C7, ports D3, ports E0 to E4, port J3, RES#		VCC × 0.8	—	VCC + 0.3		
	Ports 03, 05, 07, ports 40 to 47		AVCC0 × 0.8	—	AVCC0 + 0.3		
	Ports 03, 05, 07, ports 40 to 47	V_{IL}	–0.3	—	AVCC0 × 0.2		
	Ports other than above		–0.3	—	VCC × 0.2		
	Ports 03, 05, 07, ports 40 to 47	ΔV_T	AVCC0 × 0.01	—	—		
	Ports other than above		VCC × 0.01	—	—		
Input level voltage (except for Schmitt trigger input pins)	MD	V_{IH}	VCC × 0.9	—	VCC + 0.3	V	
	EXTAL (external clock input)		VCC × 0.8	—	VCC + 0.3		
	MD	V_{IL}	–0.3	—	VCC × 0.1		
	EXTAL (external clock input)		–0.3	—	VCC × 0.2		

Table 51.5 DC Characteristics (3)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input leakage current	RES#, MD, port 35	$\lvert I_{in} \rvert$	—	—	1.0	µA	V_{in} = 0 V, VCC
Three-state leakage current (off-state)	Ports for 5 V tolerant	$\lvert I_{TSI} \rvert$	—	—	1.0	µA	V_{in} = 0 V, 5.8 V
	Ports except for 5 V tolerant		—	—	0.2	µA	V_{in} = 0 V, VCC
Input capacitance	All input pins (except for port 35, USB0_DM, USB0_DP)	C_{in}	—	—	15	pF	V_{in} = 0 mV, f = 1 MHz, T_a = 25°C
	Port 35, USB0_DM, USB0_DP		—	—	30		

Table 51.6 DC Characteristics (4)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input pull-up resistor	All ports (except for port 35)	R_U	10	20	50	kΩ	V_{in} = 0 V

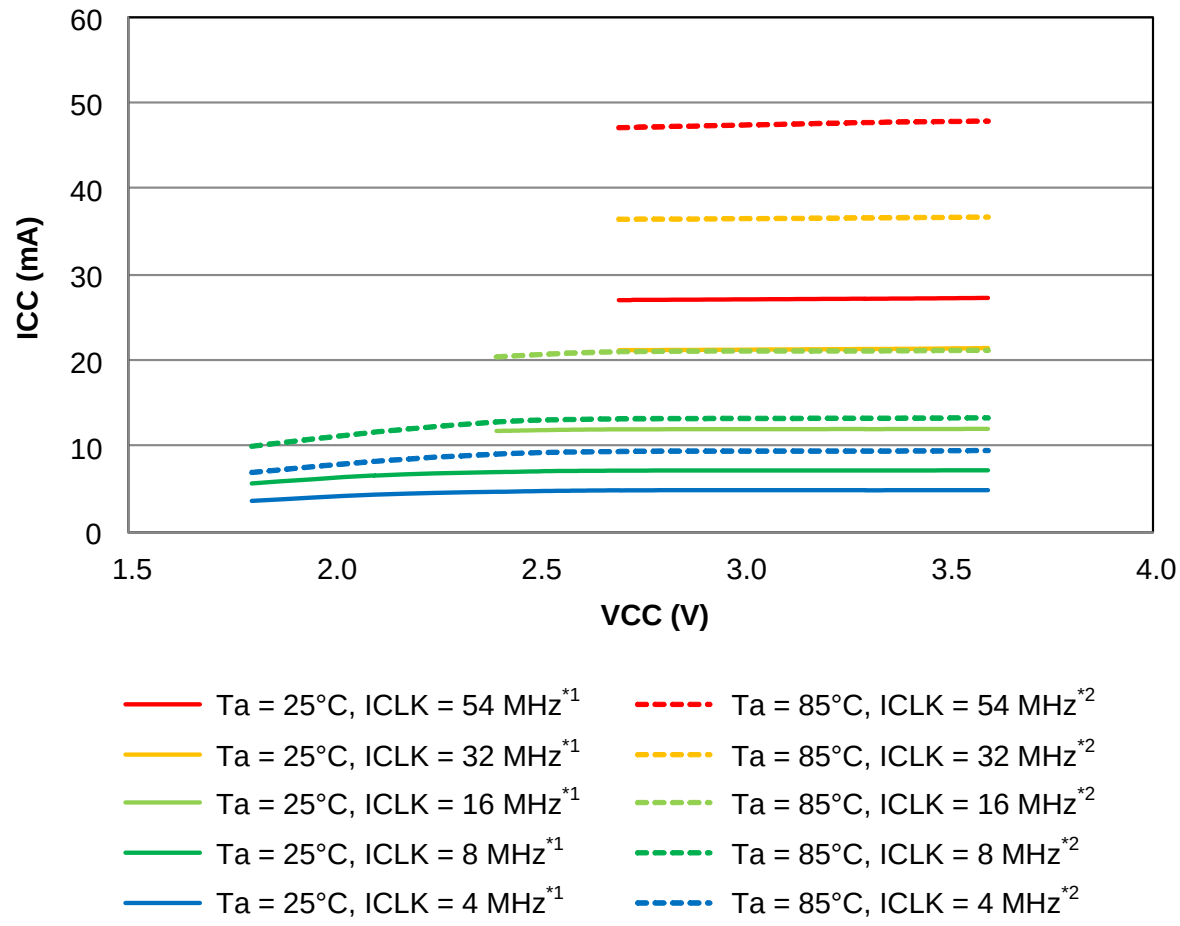
Table 51.7 DC Characteristics (5)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item					Symbol	Typ. *4	Max.	Unit	Test Conditions
Supply current *1	High-speed operating mode	Normal operating mode	No peripheral operation*2	ICLK = 54 MHz	I_{CC}	6.5	—	mA	
				ICLK = 32 MHz		4.1	—		
				ICLK = 16 MHz		2.9	—		
				ICLK = 8 MHz		2.2	—		
				ICLK = 4 MHz		1.9	—		
			All peripheral operation: Normal	ICLK = 54 MHz*11		26.5	—		
				ICLK = 32 MHz*3		21.0	—		
				ICLK = 16 MHz*3		11.8	—		
				ICLK = 8 MHz*3		6.6	—		
				ICLK = 4 MHz*3		4.2	—		
			All peripheral operation: Max.	ICLK = 54 MHz*11		—	53.3		
				ICLK = 32 MHz*3		—	40.8		
			Increase due to operation of the Trusted Secure IP	PCLKB = 32 MHz		—	2		
		Sleep mode	No peripheral operation*2	ICLK = 54 MHz		3.5	—		
				ICLK = 32 MHz		2.4	—		
				ICLK = 16 MHz		1.9	—		
				ICLK = 8 MHz		1.6	—		
				ICLK = 4 MHz		1.5	—		
			All peripheral operation: Normal	ICLK = 54 MHz*11		13.4	—		
				ICLK = 32 MHz*3		12.5	—		
				ICLK = 16 MHz*3		7.3	—		
				ICLK = 8 MHz*3		4.6	—		
				ICLK = 4 MHz*3		3.3	—		
		Deep sleep mode	No peripheral operation*2	ICLK = 54 MHz		2.3	—		
				ICLK = 32 MHz		1.5	—		
				ICLK = 16 MHz		1.3	—		
				ICLK = 8 MHz		1.2	—		
				ICLK = 4 MHz		1.1	—		
			All peripheral operation: Normal	ICLK = 54 MHz*11		10.6	—		
				ICLK = 32 MHz*3		9.9	—		
				ICLK = 16 MHz*3		5.9	—		
				ICLK = 8 MHz*3		3.8	—		
				ICLK = 4 MHz*3		2.7	—		
		Increase during BGO operation*5				2.5	—		
	Middle-speed operating mode	Normal operating mode	No peripheral operation*6	ICLK = 12 MHz	I_{CC}	2.7	—	mA	
				ICLK = 8 MHz		1.8	—		
				ICLK = 4 MHz		1.4	—		
				ICLK = 1 MHz		1.1	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		9.6	—		
				ICLK = 8 MHz		6.2	—		
				ICLK = 4 MHz		3.8	—		
				ICLK = 1 MHz		2.3	—		

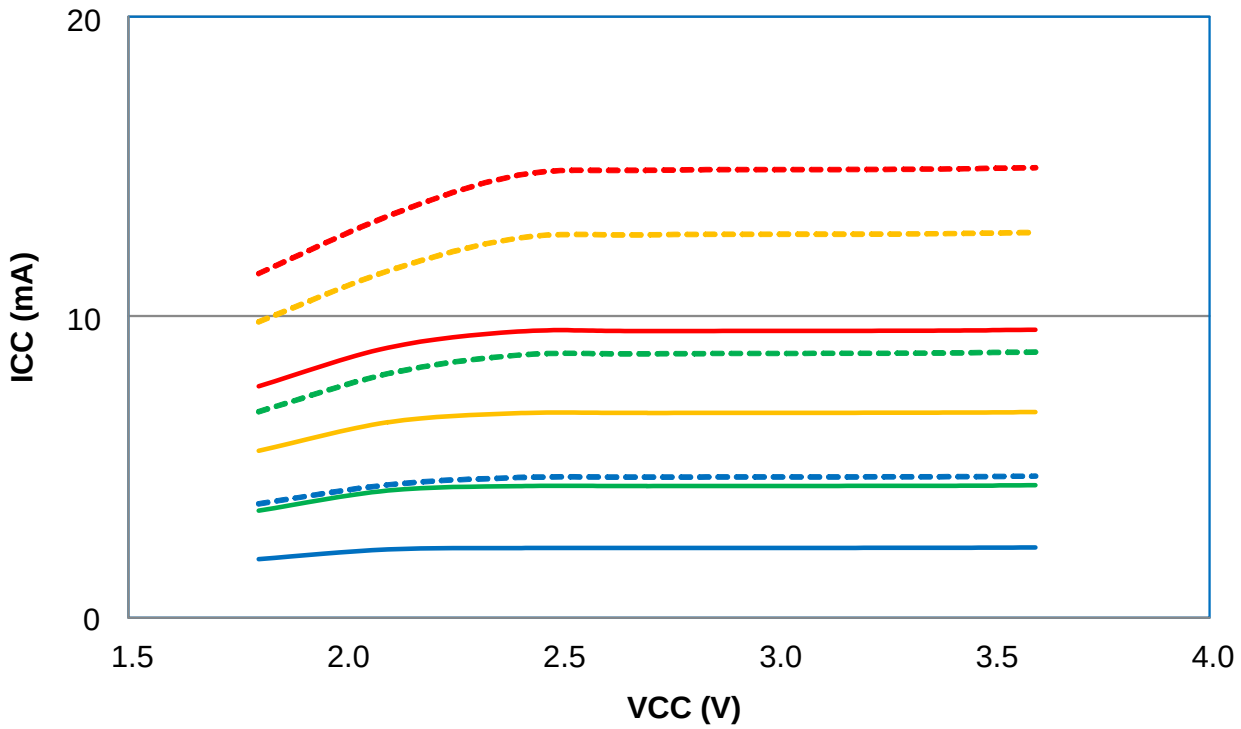
Item					Symbol	Typ. *4	Max.	Unit	Test Conditions
Supply current *1	Middle-speed operating mode	Normal operating mode	All peripheral operation: Max.*7	ICLK = 12 MHz	I_{CC}	—	16.7	mA	
		Sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.9	—		
				ICLK = 8 MHz		1.2	—		
				ICLK = 4 MHz		1.1	—		
				ICLK = 1 MHz		1.0	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		6.1	—		
				ICLK = 8 MHz		4.4	—		
				ICLK = 4 MHz		3.0	—		
				ICLK = 1 MHz		2.0	—		
		Deep sleep mode	No peripheral operation*6	ICLK = 12 MHz		1.6	—		
				ICLK = 8 MHz		1.0	—		
				ICLK = 4 MHz		0.9	—		
				ICLK = 1 MHz		0.8	—		
			All peripheral operation: Normal*7	ICLK = 12 MHz		5.1	—		
				ICLK = 8 MHz		3.7	—		
				ICLK = 4 MHz		2.6	—		
				ICLK = 1 MHz		1.8	—		
		Increase during BGO operation*5				2.5	—		
	Low-speed operating mode	Normal operating mode	No peripheral operation*8	ICLK = 32 kHz	I_{CC}	5.2	—	µA	
			All peripheral operation: Normal *9, *10	ICLK = 32 kHz		22.3	—		
			All peripheral operation: Max.*9, *10	ICLK = 32 kHz		—	74.4		
		Sleep mode	No peripheral operation*8	ICLK = 32 kHz		3.0	—		
			All peripheral operation: Normal*9	ICLK = 32 kHz		13.1	—		
		Deep sleep mode	No peripheral operation*8	ICLK = 32 kHz		2.4	—		
			All peripheral operation: Normal*9	ICLK = 32 kHz		10.5	—		

Note 1. Supply current values do not include the output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.
Note 2. Clock supply to the peripheral functions is stopped. This does not include BGO operation. The clock source is PLL. FCLK, and PCLK are set to divided by 64.
Note 3. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK, and PCLK are the same frequency as that of ICLK.
Note 4. Values when VCC is 3.3 V.
Note 5. This is the increase when data is programmed to or erased from the ROM or E2 DataFlash during program execution.
Note 6. Clock supply to the peripheral functions is stopped. The clock source is PLL when ICLK is 12 MHz and HOCO for other cases. FCLK, and PCLK are set to divided by 64.
Note 7. Clocks are supplied to the peripheral functions. The clock source is PLL when ICLK is 12 MHz and HOCO for other cases. FCLK, and PCLK are the same frequency of that of the ICLK.
Note 8. Clock supply to the peripheral functions is stopped. The clock source is the sub oscillation circuit. FCLK, and PCLK are set to divided by 64.
Note 9. Clocks are supplied to the peripheral functions. The clock source is the sub oscillation circuit. FCLK, and PCLK are the same frequency as that of ICLK.
Note 10. This is the value when the MSTPCRA.MSTPA17 (12-bit A/D converter module stop bit) is in the module stop state.
Note 11. Clocks are supplied to the peripheral functions. This does not include BGO operation. The clock source is PLL. FCLK, and PCLKB are set to divided by 2 and PCLKA and PCLKD are the same frequency as that of ICLK.



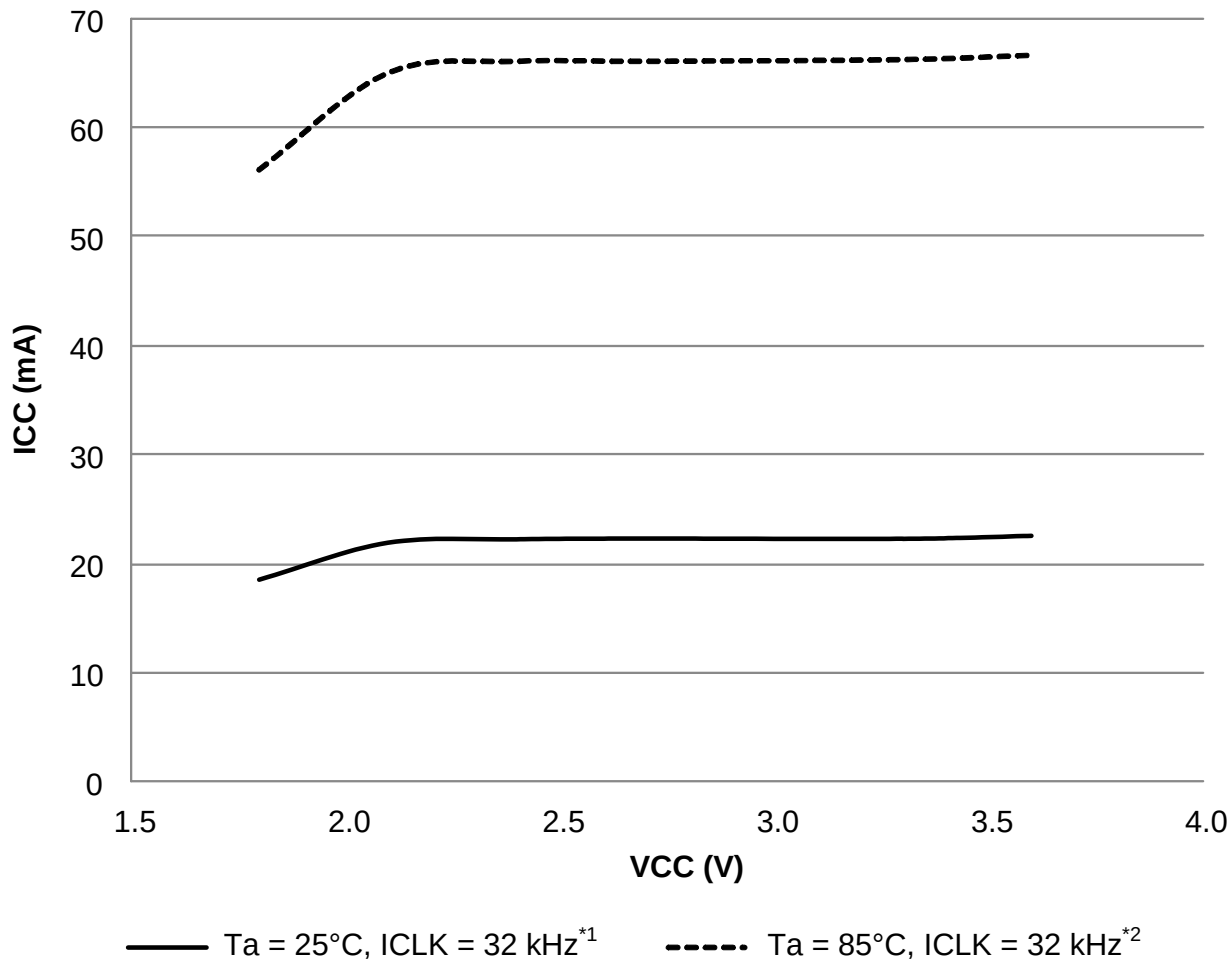
Note 1. All peripheral operations except any BGO operation are operating normally. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 51.1 Voltage Dependency in High-Speed Operating Mode (Reference Data)



Note 1. All peripheral operations except any BGO operation are operating normally. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 51.2 Voltage Dependency in Middle-Speed Operating Mode (Reference Data)



Note 1. All peripheral operations except any BGO operation are operating normally. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. All peripheral operations except any BGO operation are operating at maximum. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

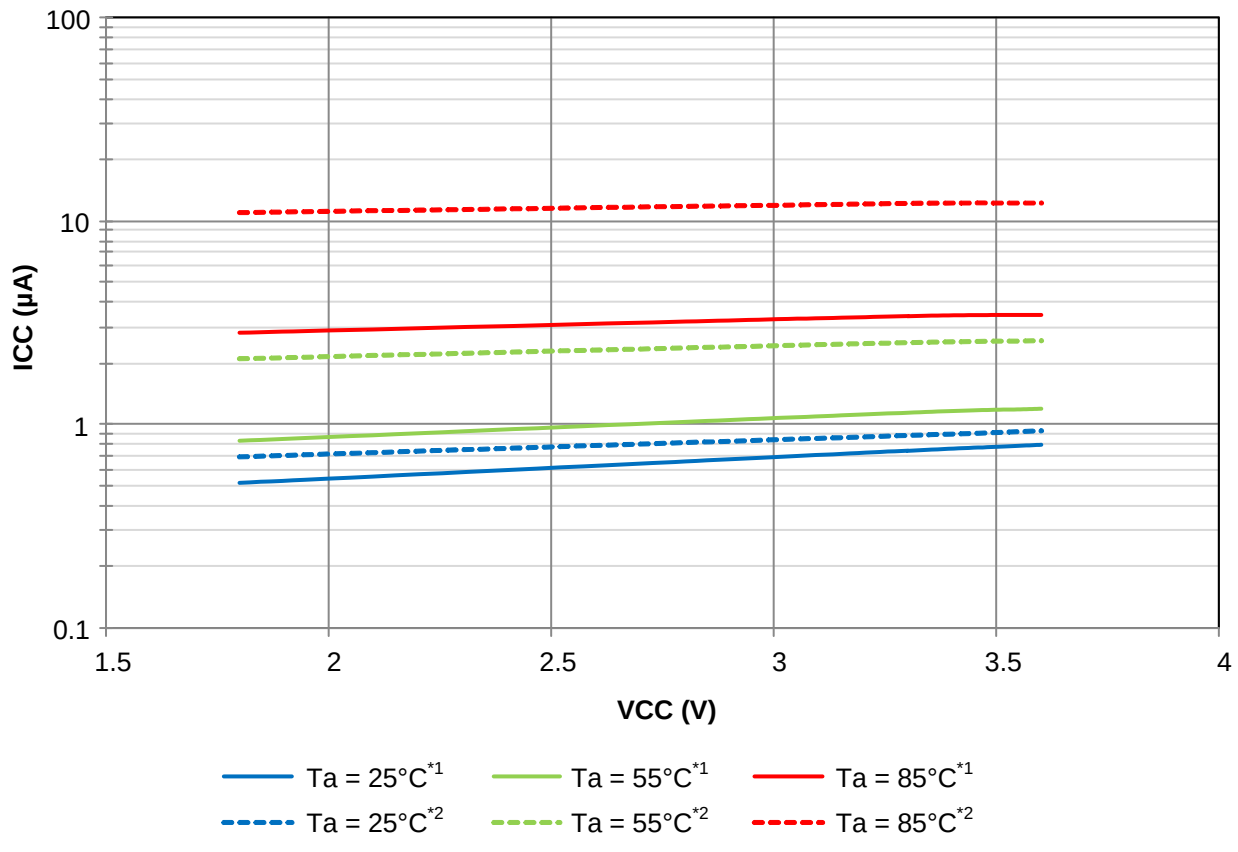
Figure 51.3 Voltage Dependency in Low-Speed Operating Mode (Reference Data)

Table 51.8 DC Characteristics (6)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

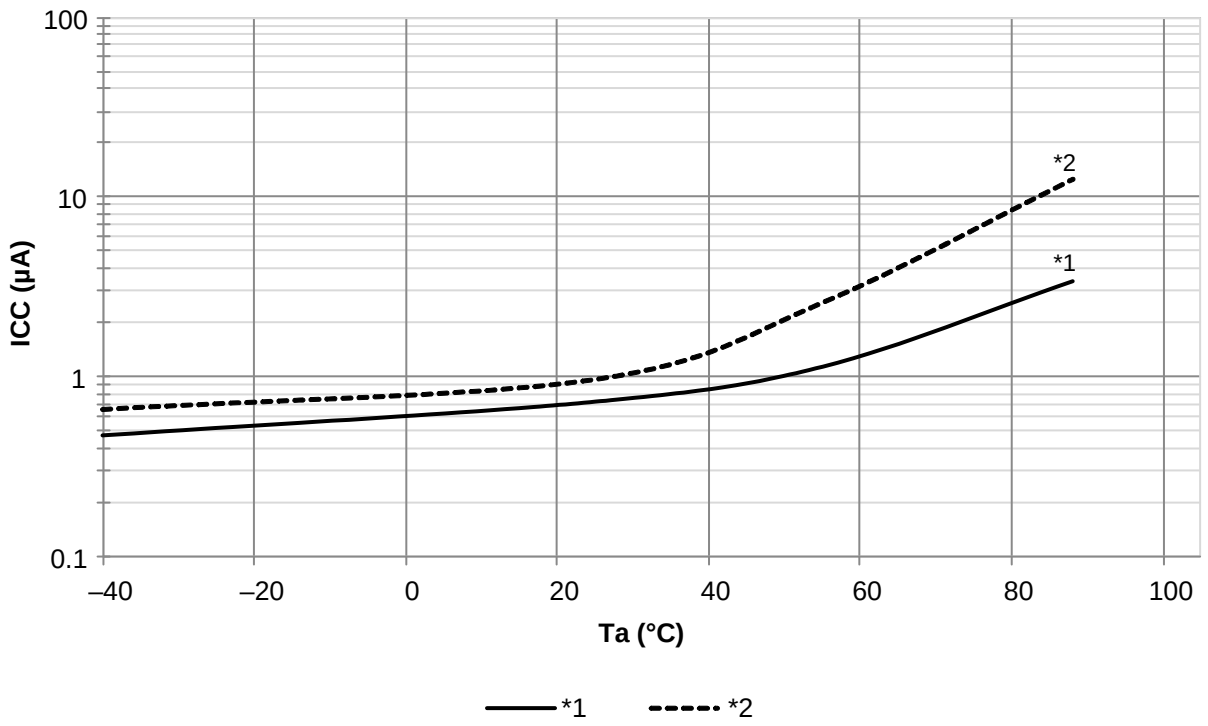
Item			Symbol	Typ.*3	Max.	Unit	Test Conditions
Supply current*1	Software standby mode*2	T_a = 25°C	I_{CC}	0.8	3.7	µA	
		T_a = 55°C		1.2	4.3		
		T_a = 85°C		3.5	18.6		
	Increment for IWDT operation			0.4	—		
	Increment for LPT operation			0.4	—		Use IWDT-Dedicated On-Chip Oscillator for clock source
	Increment for RTC operation*4			0.4	—		RCR3.RTCDV[2:0] set to low drive capacity
				1.2	—		RCR3.RTCDV[2:0] set to normal drive capacity

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOSs in the off state.
Note 2. The IWDT, LVD, and CMPB are stopped.
Note 3. When VCC is 3.3 V.
Note 4. This increment includes the oscillation circuit.



Note 1. Indicates the average of the typical samples through actual measurement during product evaluation.
Note 2. Indicates the average of the upper-limit samples through actual measurement during product evaluation.

Figure 51.4 Voltage Dependency in Software Standby Mode (Reference Data)



Note 1. Average value of the tested middle samples during product evaluation.
Note 2. Average value of the tested upper-limit samples during product evaluation.

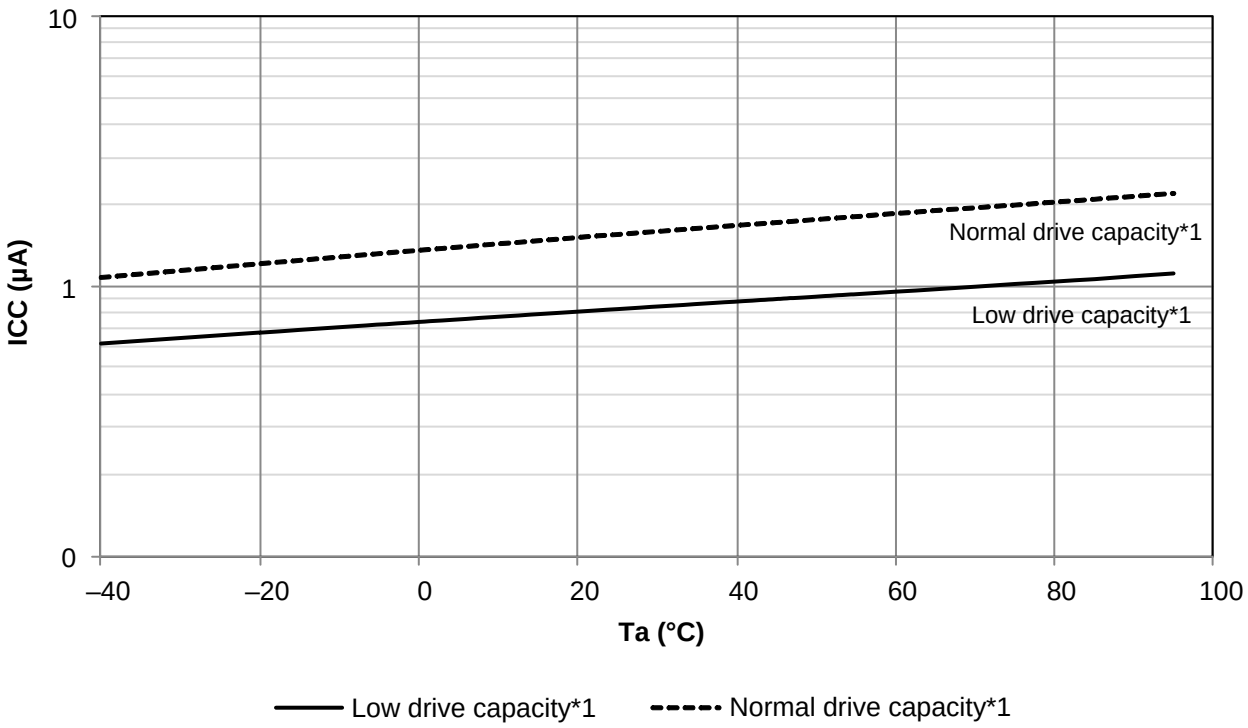
Figure 51.5 Temperature Dependency in Software Standby Mode (Reference Data)

Table 51.9 DC Characteristics (7)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item			Symbol	Typ.	Max.	Unit	Test Conditions
Supply current*1	RTC operation when VCC is off	T_a = 25°C	I_{CC}	0.8	—	µA	VBATT = 2.0 V RCR3.RTCDV[2:0] set to low drive capacity
		T_a = 55°C		0.9	—		
		T_a = 85°C		1.0	—		
		T_a = 25°C		0.9	—		VBATT = 3.3 V RCR3.RTCDV[2:0] set to low drive capacity
		T_a = 55°C		1.0	—		
		T_a = 85°C		1.1	—		
		T_a = 25°C		1.5	—		VBATT = 2.0 V RCR3.RTCDV[2:0] set to normal drive capacity
		T_a = 55°C		1.8	—		
		T_a = 85°C		2.1	—		
		T_a = 25°C		1.6	—		VBATT = 3.3 V RCR3.RTCDV[2:0] set to normal drive capacity
		T_a = 55°C		1.9	—		
		T_a = 85°C		2.2	—		

Note 1. Supply current values do not include output charge/discharge current from all pins. The values apply when internal pull-up MOSs are in the off state.



Note 1. Indicates the average of the typical samples through actual measurement during product evaluation.

Figure 51.6 Temperature Dependency of RTC Operation with VCC Off (Reference Data)

Table 51.10 DC Characteristics (8)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible total power consumption*1	Pd	—	—	350	mW	D-version product

Note 1. Total power dissipated by the entire chip (including output currents)

Table 51.11 DC Characteristics (9)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.*7	Max.	Unit	Test Conditions
Analog power supply current	During A/D conversion (at high-speed conversion)	I_{AVCC}	—	0.7	1.7	mA	
	During A/D conversion (in low-current mode)		—	0.6	1.0		
	During D/A conversion (per channel)*1		—	0.4	0.8		
	Waiting for A/D and D/A conversion (all units)		—	—	0.4	µA	
Reference power supply current	During A/D conversion (at high-speed conversion)	I_{REFH0}	—	25	150	µA	
	Waiting for A/D conversion (all units)		—	—	60	nA	
	During D/A conversion (per channel)	I_{REFH}	—	50	100	µA	
	Waiting for D/A conversion (all units)		—	—	100	nA	
LVD1	—	I_{LVD}	—	0.15	—	µA	
Temperature sensor*6	—	I_{TEMP}	—	75	—	µA	
Comparator B operating current*6	Window mode	I_{CMP}*5	—	12.5	28.6	µA	
	Comparator high-speed mode (per channel)		—	3.2	16.2	µA	
	Comparator low-speed mode (per channel)		—	1.7	4.4	µA	
CTSU operating current	• When sleep mode Base clock frequency: 2MHz Pin capacitance: 50pF	I_{CTSU}	—	150	—	µA	
USB operating current*4	During USB communication operation under the following settings and conditions • Host controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 • Connect peripheral devices via a 1-meter USB cable from the USB port.	I_{USBH}*2	—	4.3 (VCC) 0.9 (VCC_USB)	—	mA	
	During USB communication operation under the following settings and conditions • Function controller operation is set to full-speed mode Bulk OUT transfer (64 bytes) × 1, bulk IN transfer (64 bytes) × 1 • Connect the host device via a 1-meter USB cable from the USB port.	I_{USBF}*2	—	3.6 (VCC) 1.1 (VCC_USB)	—	mA	
	During suspended state under the following setting and conditions • Function controller operation is set to full-speed mode (pull up the USB0_DP pin) • Software standby mode • Connect the host device via a 1-meter USB cable from the USB port.	I_{SUSP}*3	—	0.35 (VCC) 170 (VCC_USB)	—	µA	

Note 1. The value of the D/A converter is the value of the power supply current including the reference current.
Note 2. Current consumed only by the USB module.
Note 3. Includes the current supplied from the pull-up resistor of the USB0_DP pin to the pull-down resistor of the host device, in addition to the current consumed by this MCU during the suspended state.
Note 4. Current consumed by the power supplies (VCC and VCC_USB).
Note 5. Current consumed only by the comparator B module.
Note 6. Current consumed by the power supply (VCC).
Note 7. When VCC = AVCC0 = VCC_USB = 3.3 V.

Table 51.12 DC Characteristics (10)

Conditions: VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF = 3.3 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = +25°C

Item	Symbol	Typ.		Unit	Test Conditions
		Transmit output power			
		0 dBm	4 dBm		
BLE operating current (when the DC-to-DC converter is selected)	Idd_tx	4.3	8.7	mA	Transmit mode, 2Mbps
					Transmit mode, 1Mbps
		4.5	8.7		Transmit mode, 500kbps
					Transmit mode, 125kbps
	Idd_rx	3.0	3.5	mA	Receive mode, 2Mbps Prf = –67dBm
		3.0	3.4		Receive mode, 1Mbps Prf = –67dBm
		3.2	3.5		Receive mode, 500kbps Prf = –72dBm
		3.3	3.5		Receive mode, 125kbps Prf = –79dBm
	Idd_idle	0.5		mA	Idle mode
	Idd_slp	1.5		µA	Deep sleep mode
	Idd_down	0.1		µA	Power down mode
BLE operating current (when the linear regulator is selected)	Idd_tx	10.2	18.1	mA	Transmit mode, 2Mbps
					Transmit mode, 1Mbps
					Transmit mode, 500kbps
					Transmit mode, 125kbps
	Idd_rx	6.9		mA	Receive mode, 2Mbps Prf = –67dBm
		6.9			Receive mode, 1Mbps Prf = –67dBm
		6.9			Receive mode, 500kbps Prf = –72dBm
		7.1			Receive mode, 125kbps Prf = –79dBm
	Idd_idle	0.7		mA	Idle mode
	Idd_slp	1.5		µA	Deep sleep mode
	Idd_down	0.1		µA	Power down mode

Table 51.13 DC Characteristics (11)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	1.8	—	—	V	

Table 51.14 DC Characteristics (12)

Conditions: 0 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power-on VCC rising gradient	At normal startup*1	SrVCC	0.02	—	20	ms/V	
	During fast startup time*2		0.02	—	2		
	Voltage monitoring 0 reset enabled at startup*3, *4		0.02	—	—		

Note 1. When OFS1.(FASTSTUP, LVDAS) bits are 11b.
Note 2. When OFS1.(FASTSTUP, LVDAS) bits are 01b.
Note 3. When OFS1.LVDAS bit is 0.
Note 4. Turn on the power supply voltage according to the normal startup rising gradient because the settings in the OFS1 register are not read in boot mode.

Table 51.15 DC Characteristics (13)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

The ripple voltage must meet the allowable ripple frequency $f_{r\,(VCC)}$ within the range between the VCC upper limit and lower limit. When VCC change exceeds VCC ±10%, the allowable voltage change rising/falling gradient dt/dVCC must be met.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Allowable ripple frequency	$f_{r\,(VCC)}$	—	—	10	kHz	Figure 51.7 $V_{r\,(VCC)}$ ≤ VCC × 0.2
		—	—	1	MHz	Figure 51.7 $V_{r\,(VCC)}$ ≤ VCC × 0.08
		—	—	10	MHz	Figure 51.7 $V_{r\,(VCC)}$ ≤ VCC × 0.06
Allowable voltage change rising/falling gradient	dt/dVCC	1.0	—	—	ms/V	When VCC change exceeds VCC ±10%

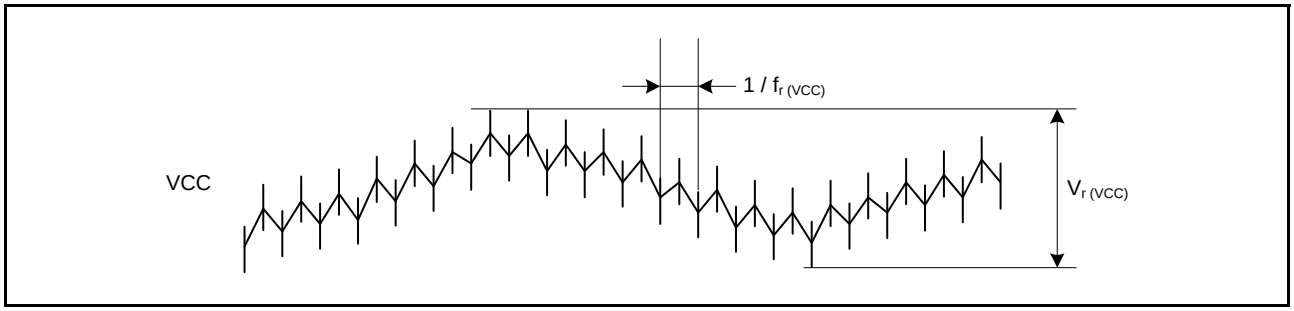


Figure 51.7 Ripple Waveform

Table 51.16 DC Characteristics (14)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Permissible error of VCL pin external capacitance	C_{VCL}	1.4	4.7	7.0	µF	

Note: The recommended capacitance is 4.7 µF. Variations in connected capacitors should be within the above range.

Table 51.17 Permissible Output Currents

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item			Symbol	Max.	Unit
Permissible output low current (average value per pin)	Ports 03, 05, 07, ports 36, 37, ports 40 to 47		I_{OL}	4.0	mA
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current (maximum value per pin)	Ports 03, 05, 07, ports 36, 37, ports 40 to 47			4.0	
	Ports other than above	Normal output mode		4.0	
		High-drive output mode		8.0	
Permissible output low current	Total of ports 03, 05, 07, ports 40 to 47		ΣI_{OL}	40	
	Total of ports 14 to 17, ports 21, 22, 25 to 27, ports 30, 31, 35 to 37, port PJ3			40	
	Total of ports B0, B1, B3, B5, B7, ports C0, C2 to C7			40	
	Total of port D3, ports E0 to E4			40	
	Total of all output pins			80	
Permissible output high current (average value per pin)	Ports 03, 05, 07, ports 36, 37, ports 40 to 47		I_{OH}	–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current (maximum value per pin)	Ports 03, 05, 07, ports 36, 37, ports 40 to 47			–4.0	
	Ports other than above	Normal output mode		–4.0	
		High-drive output mode		–8.0	
Permissible output high current	Total of ports 03, 05, 07, ports 40 to 47		ΣI_{OH}	–40	
	Total of ports 14 to 17, ports 21, 22, 25 to 27, ports 30, 31, 35 to 37, port PJ3			–40	
	Total of ports B0, B1, B3, B5, B7, ports C0, C2 to C7			–40	
	Total of port D3, ports E0 to E4			–40	
	Total of all output pins			–80	

Note: Do not exceed the permissible total supply current.

Table 51.18 Output Values of Voltage (1)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 2.7 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports*1	Normal output mode		V_{OL}	—	0.8	V	I_{OL} = 0.5 mA
		High-drive output mode			—	0.8		I_{OL} = 1.0 mA
Output high	All output ports*1	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	V_{OH}	AVCC0 – 0.5	—	V	I_{OH} = –0.5 mA
			Ports other than above		VCC – 0.5	—		
		High-drive output mode			VCC – 0.5	—		I_{OH} = –1.0 mA

Note 1. This excludes the CLKOUT_RF pin.

Table 51.19 Output Values of Voltage (2)

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Max.	Unit	Test Conditions
Output low	All output ports (except for RIIC) *1	Normal output mode		V_{OL}	—	0.8	V	I_{OL} = 1.0 mA
		High-drive output mode			—	0.8		I_{OL} = 2.0 mA
	RIIC pins	Standard mode (Normal output mode)			—	0.4		I_{OL} = 3.0 mA
		Fast mode (High-drive output mode)			—	0.6		I_{OL} = 6.0 mA
Output high	All output ports*1	Normal output mode	Ports 03, 05, 07, Ports 40 to 47	V_{OH}	AVCC0 – 0.8	—	V	I_{OH} = –1.0 mA
			Ports other than above		VCC – 0.8	—		
		High-drive output mode			VCC – 0.8	—		I_{OH} = –2.0 mA

Note 1. This excludes the CLKOUT_RF pin.

Table 51.20 Output Values of Voltage (3)

Conditions: 3.0V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6V, VSS = AVSS0 = VSS_USB = VSS_RF = 0V, Ta = –40 to +85°C

Item		Symbol	Min.	Max.	Unit	Test Conditions
Output low	CLKOUT_RF	V_{OL}	—	0.3	V	I_{OL} = 0.5 mA
Output high	CLKOUT_RF	V_{OH}	VCC_RF – 0.3	—	V	I_{OH} = –0.5 mA

51.2.1 Normal I/O Pin Output Characteristics (1)

Figure 51.8 to Figure 51.11 show the characteristics when normal output is selected by the drive capacity control register.

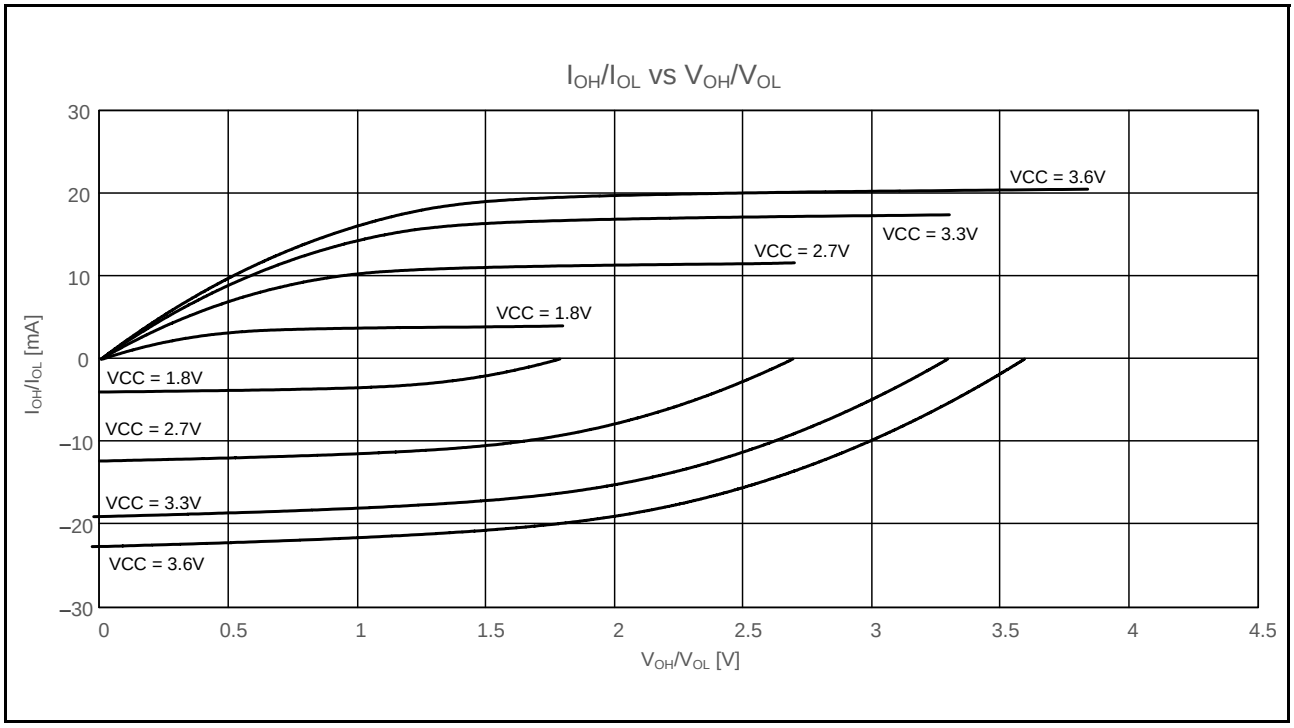


Figure 51.8 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When Normal Output is Selected (Reference Data)

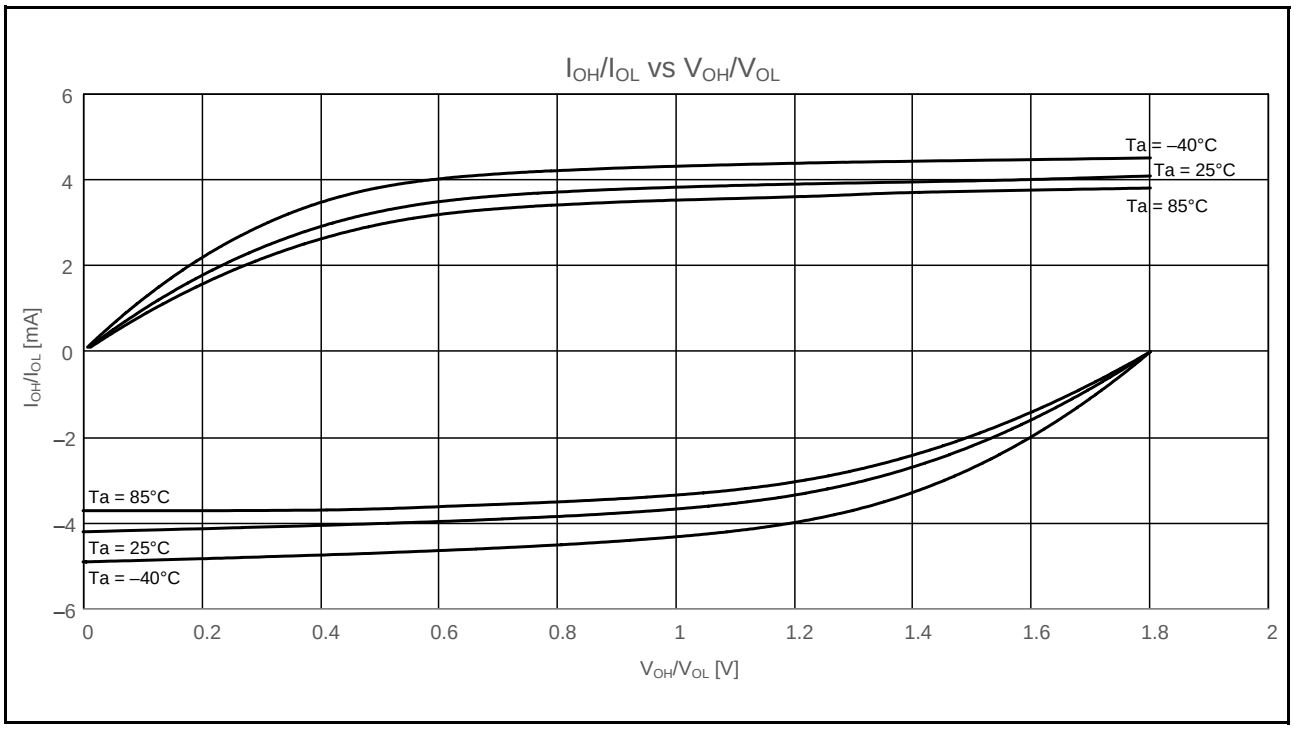


Figure 51.9 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 1.8 V When Normal Output is Selected (Reference Data)

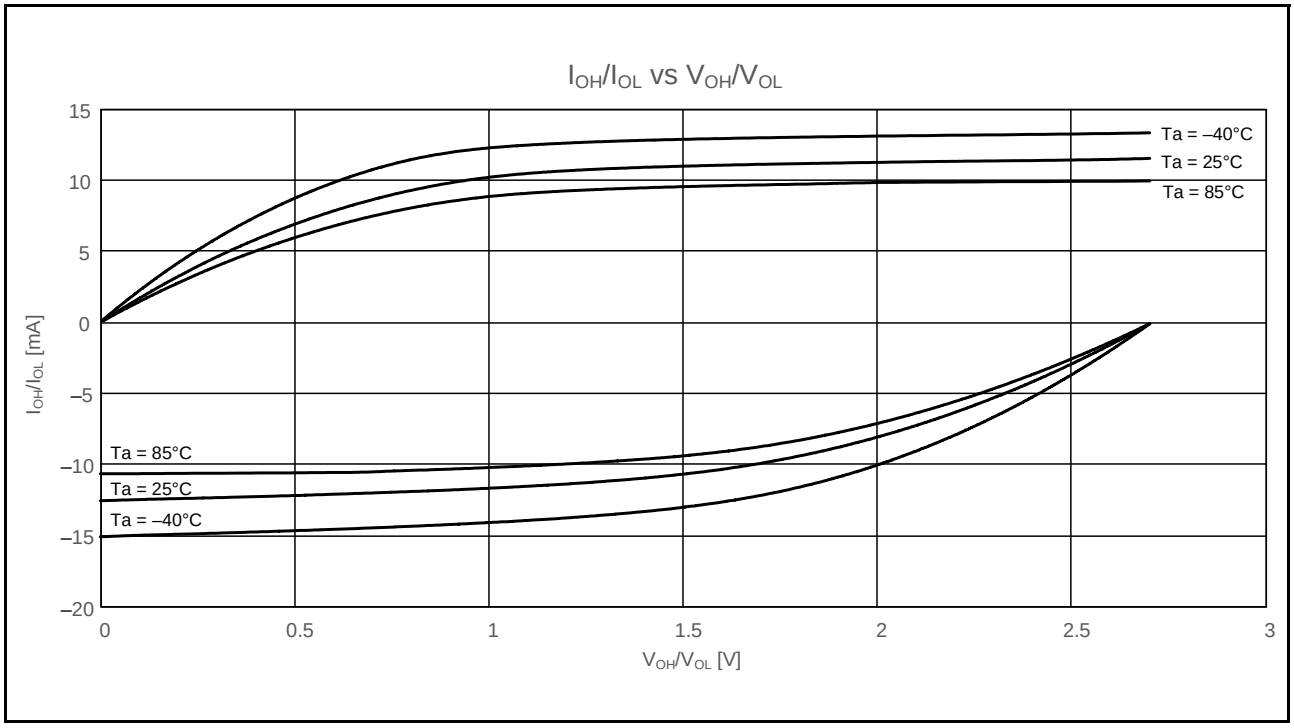


Figure 51.10 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V When Normal Output is Selected (Reference Data)

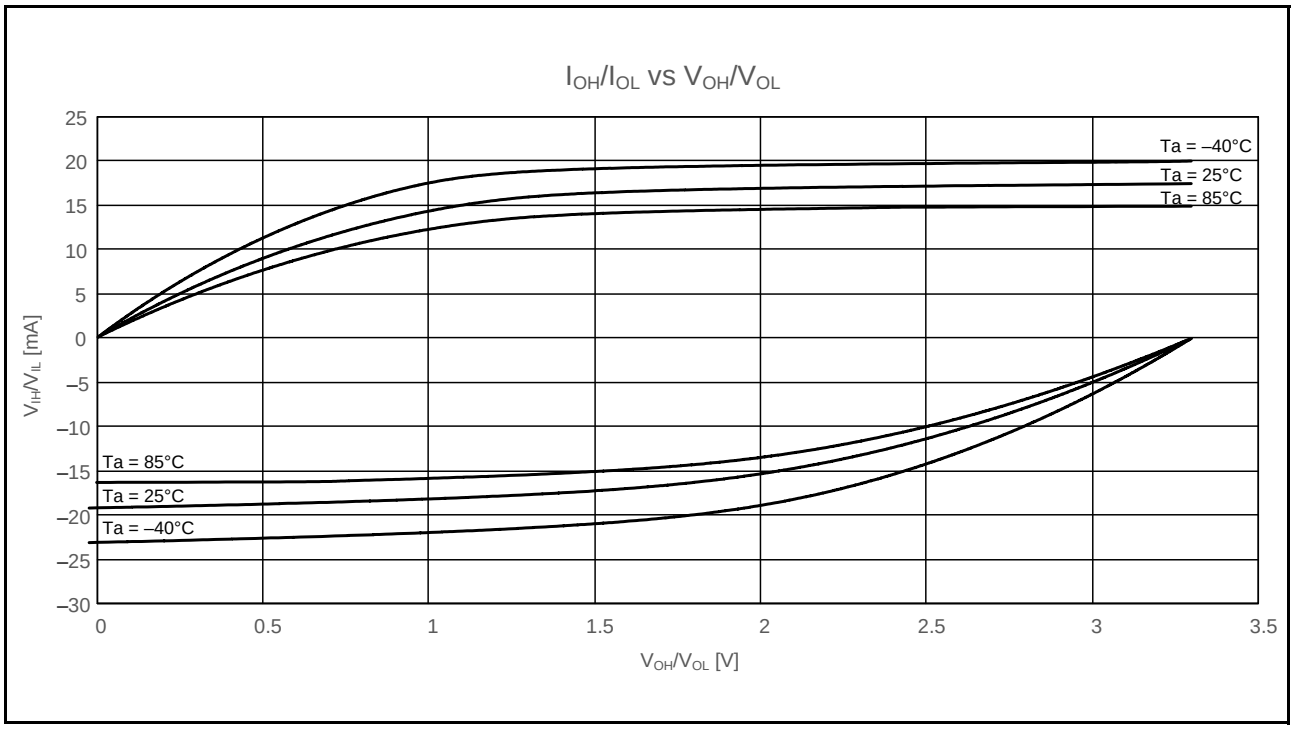


Figure 51.11 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V When Normal Output is Selected (Reference Data)

51.2.2 Normal I/O Pin Output Characteristics (2)

Figure 51.12 to Figure 51.15 show the characteristics when high-drive output is selected by the drive capacity control register.

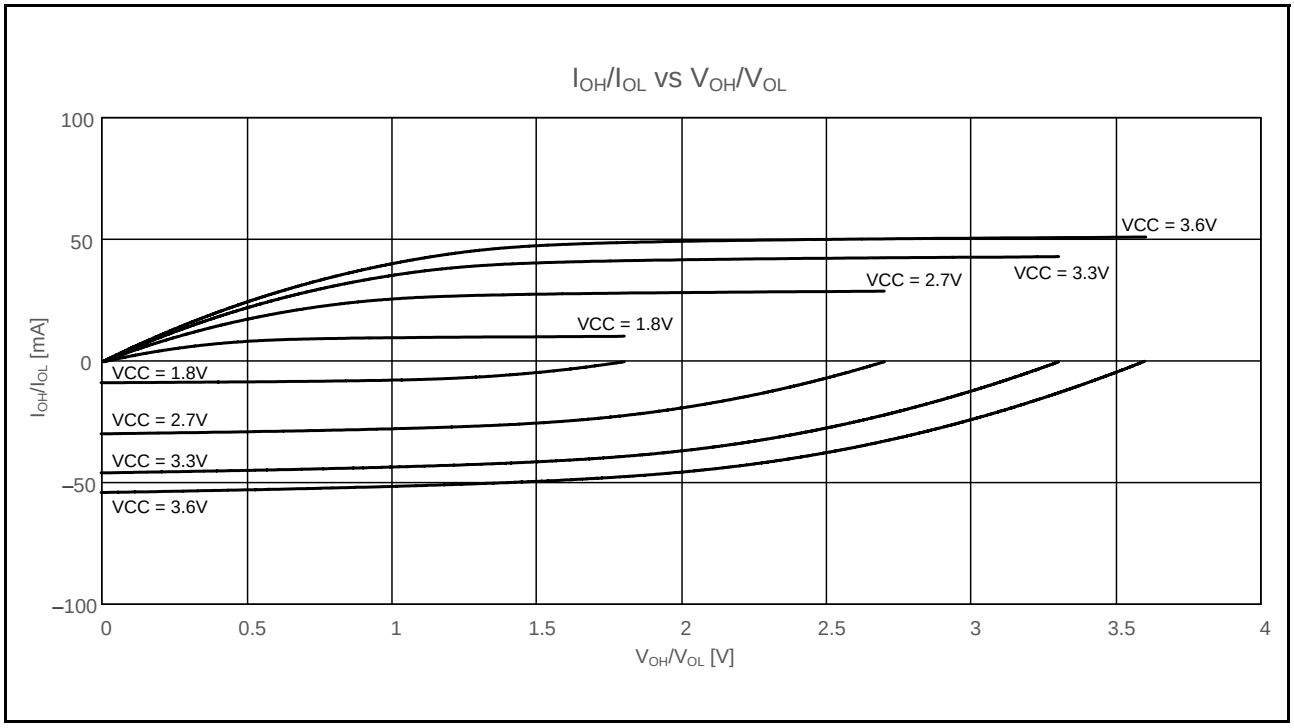


Figure 51.12 V_{OH}/V_{OL} and I_{OH}/I_{OL} Voltage Characteristics at T_a = 25°C When High-Drive Output is Selected (Reference Data)

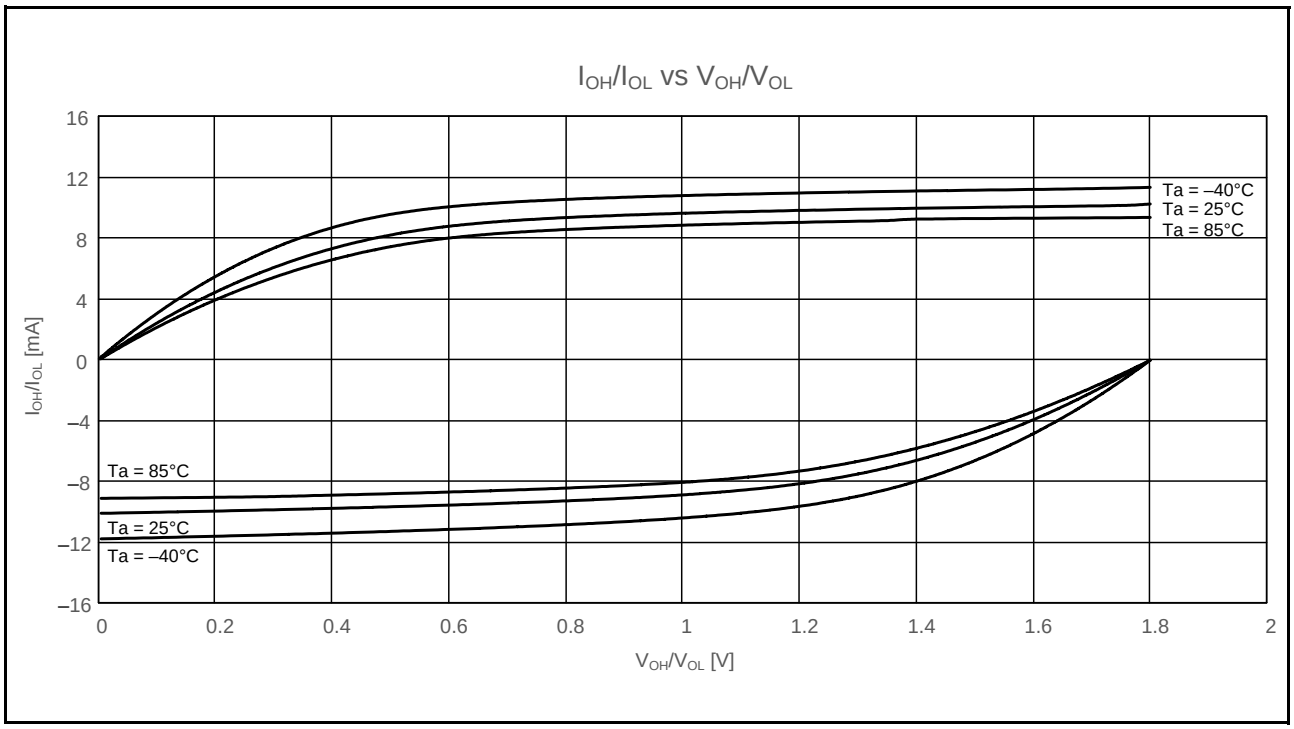


Figure 51.13 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 1.8 V When High-Drive Output is Selected (Reference Data)

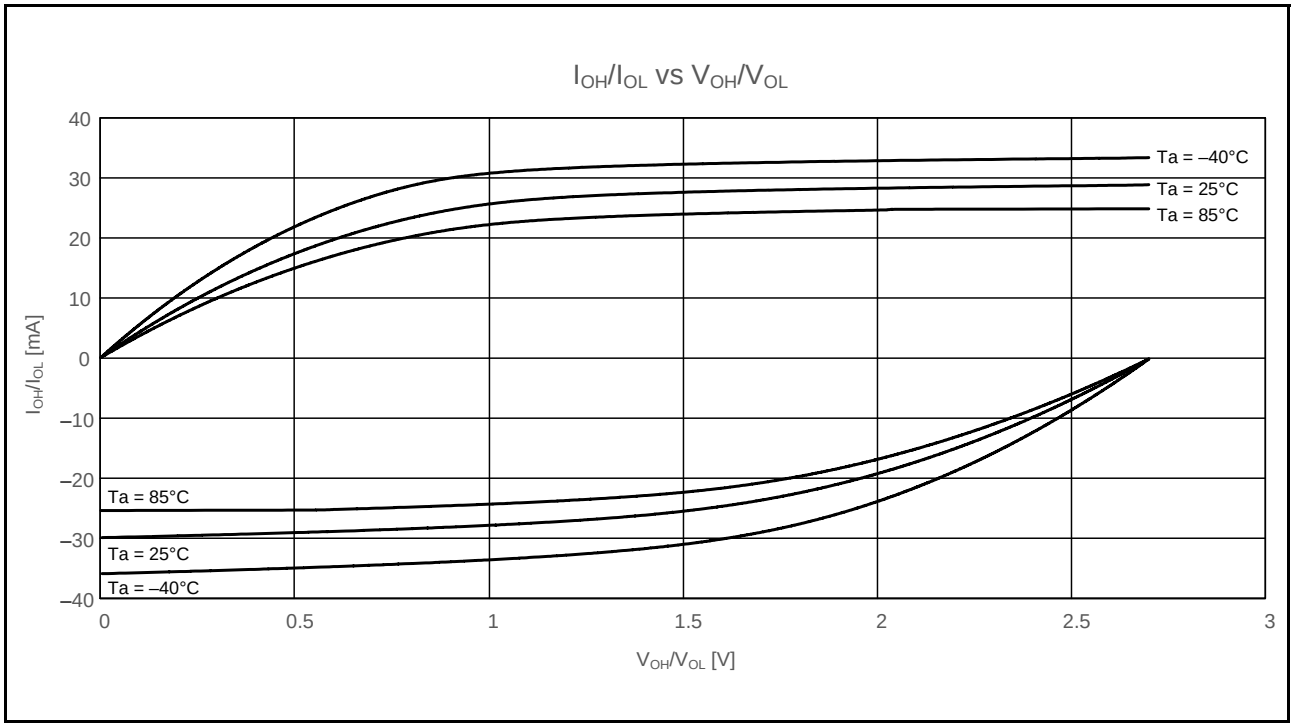


Figure 51.14 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 2.7 V When High-Drive Output is Selected (Reference Data)

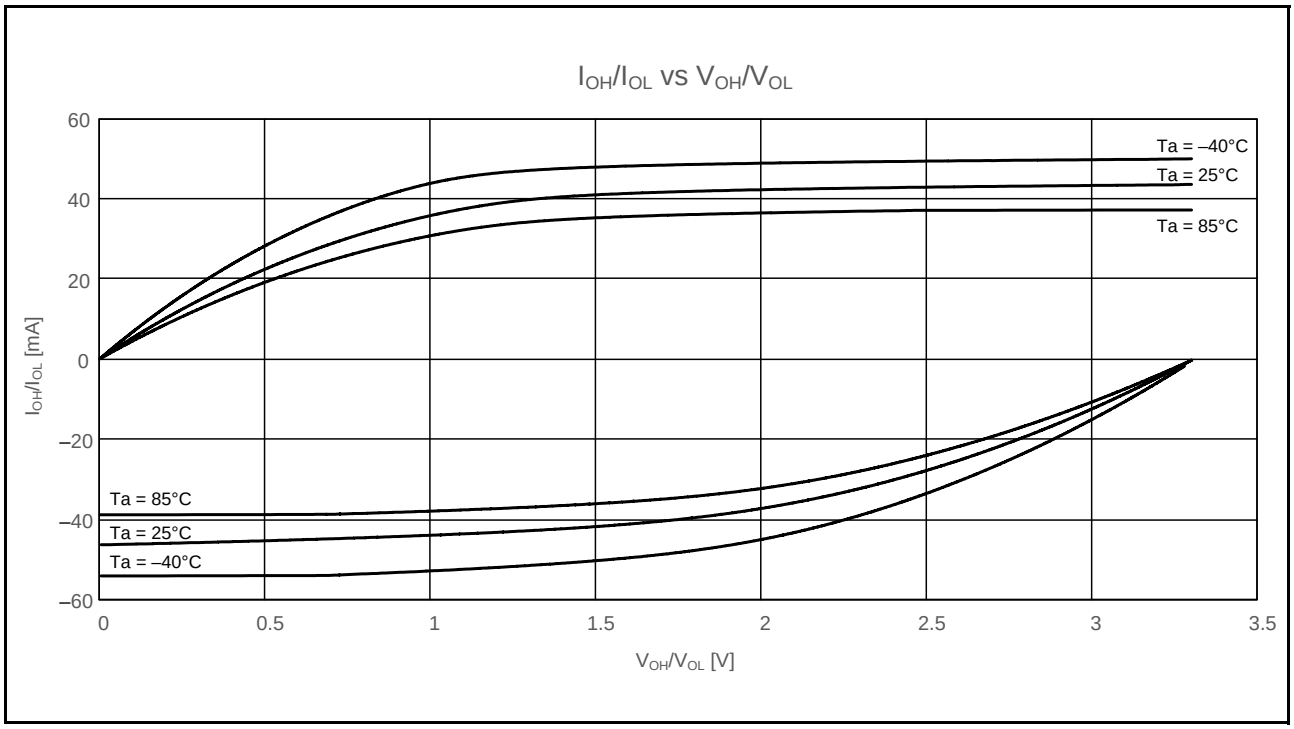


Figure 51.15 V_{OH}/V_{OL} and I_{OH}/I_{OL} Temperature Characteristics at VCC = 3.3 V When High-Drive Output is Selected (Reference Data)

51.2.3 Normal I/O Pin Output Characteristics (3)

Figure 51.16 to Figure 51.18 show the characteristics of the RIIC output pin.

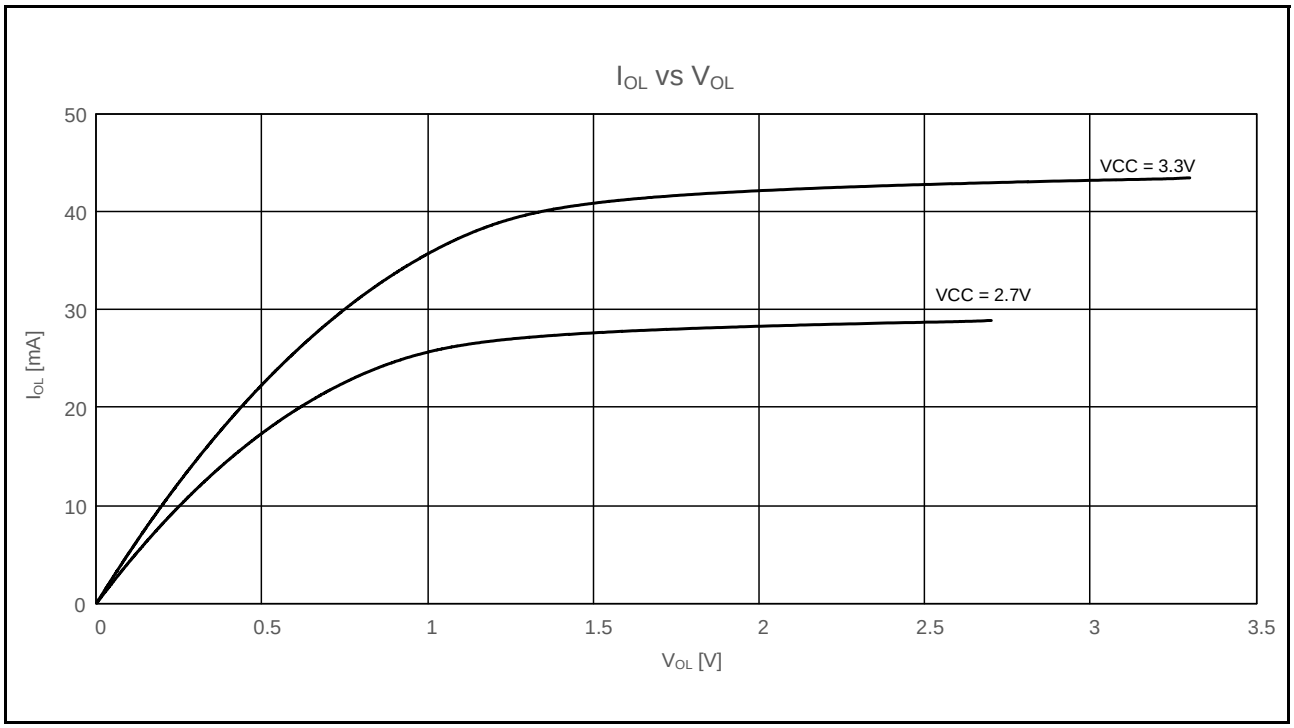


Figure 51.16 V_{OL} and I_{OL} Voltage Characteristics of RIIC Output Pin at T_a = 25°C (Reference Data)

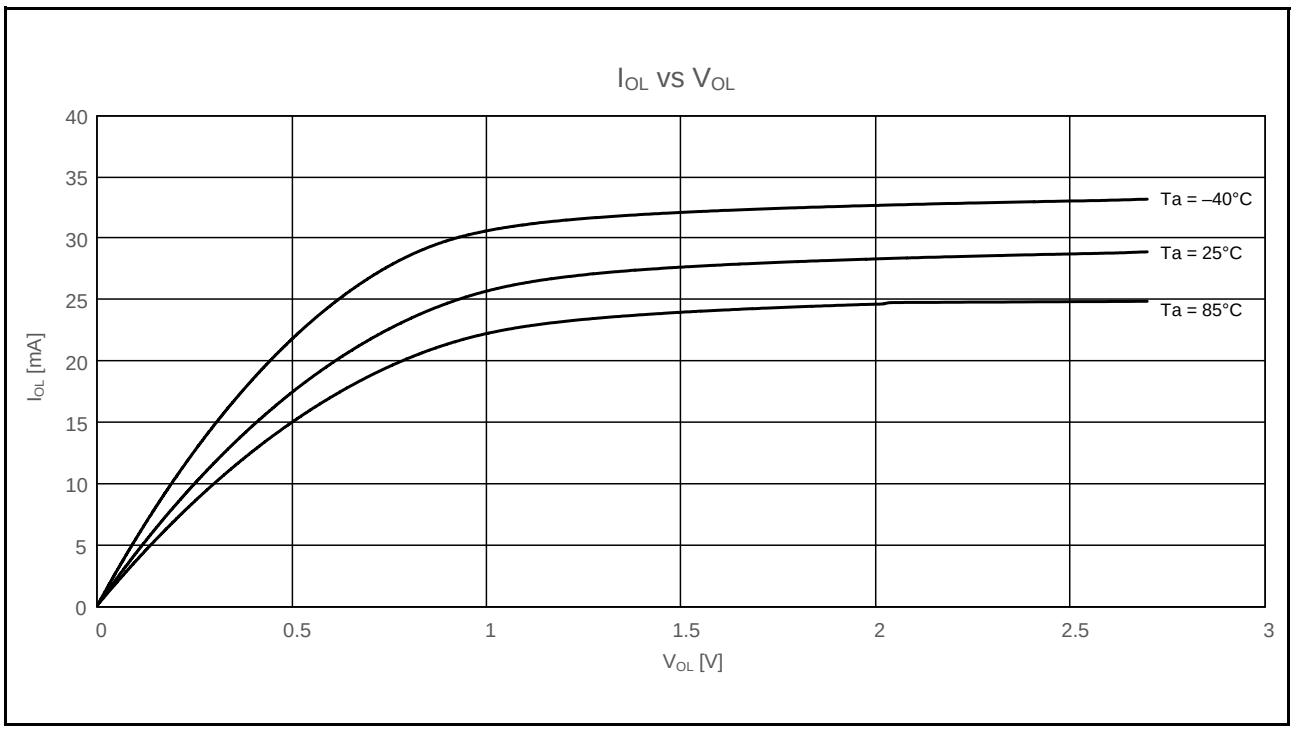


Figure 51.17 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 2.7 V (Reference Data)

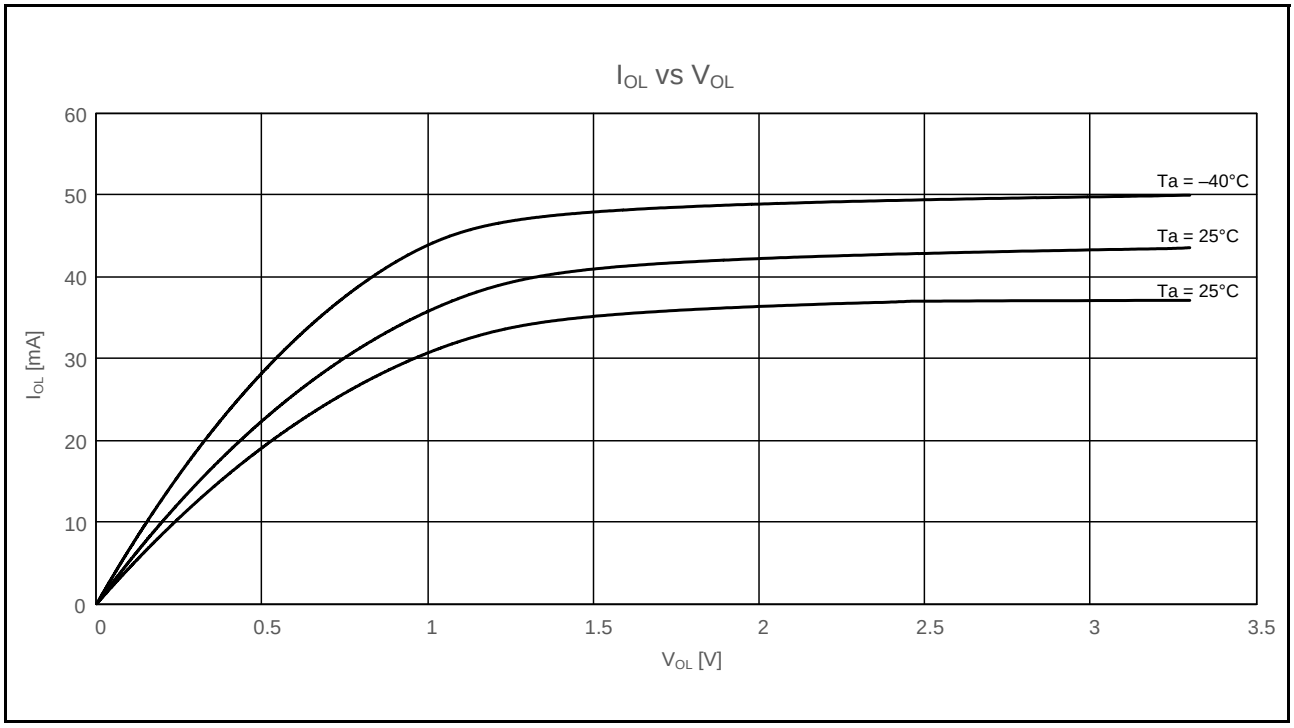


Figure 51.18 V_{OL} and I_{OL} Temperature Characteristics of RIIC Output Pin at VCC = 3.3 V (Reference Data)

51.3 AC Characteristics

51.3.1 Clock Timing

Table 51.21 Operating Frequency Value (High-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item		Symbol	VCC				Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 3.6 V	When USB is in Use*3	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	16	54	54	MHz
	FlashIF clock (FCLK)*1, *2		8	16	32	32	
	Peripheral module clock (PCLKA)		8	16	54	54	
	Peripheral module clock (PCLKB)		8	16	32	32	
	Peripheral module clock (PCLKD)		8	32	54	54	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When FCLK is in use at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be within ±3.5%.
Note 3. The VCC_USB range is 3.0 to 3.6 V when the USB clock is in use.
Note 4. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 51.24, Clock Timing.

Table 51.22 Operating Frequency Value (Middle-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item		Symbol	VCC				Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 3.6 V	When USB is in Use*3	
Maximum operating frequency*4	System clock (ICLK)	f_{max}	8	12	12	12	MHz
	FlashIF clock (FCLK)*1, *2		8	12	12	12	
	Peripheral module clock (PCLKA)		8	12	12	12	
	Peripheral module clock (PCLKB)		8	12	12	12	
	Peripheral module clock (PCLKD)		8	12	12	12	
	USB clock (UCLK)	f_{usb}	—	—	—	48	

Note 1. The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be within ±3.5%.
Note 3. The VCC_USB range is 3.0 to 3.6 V when the USB clock is in use.
Note 4. The maximum operating frequency listed above does not include errors of the external oscillator and internal oscillator. For details on the range for the guaranteed operation, see Table 51.24, Clock Timing.

Table 51.23 Operating Frequency Value (Low-Speed Operating Mode)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item		Symbol	VCC			Unit
			1.8 V ≤ VCC < 2.4 V	2.4 V ≤ VCC < 2.7 V	2.7 V ≤ VCC ≤ 3.6 V	
Maximum operating frequency*3	System clock (ICLK)	f_{max}	32.768			kHz
	FlashIF clock (FCLK)*1		32.768			
	Peripheral module clock (PCLKA)		32.768			
	Peripheral module clock (PCLKB)		32.768			
	Peripheral module clock (PCLKD)*2		32.768			

Note 1. Programming and erasing the flash memory is impossible.
Note 2. The A/D converter cannot be used.
Note 3. The maximum operating frequency listed above does not include errors of the external oscillator. For details on the range for the guaranteed operation, see Table 51.24, Clock Timing.

Table 51.24 Clock Timing

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0= VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
EXTAL external clock input cycle time		t_{Xcyc}	50	—	—	ns	Figure 51.19
EXTAL external clock input high pulse width		t_{XH}	20	—	—	ns	
EXTAL external clock input low pulse width		t_{XL}	20	—	—	ns	
EXTAL external clock rise time		t_{Xr}	—	—	5	ns	
EXTAL external clock fall time		t_{Xf}	—	—	5	ns	
EXTAL external clock input wait time*1		t_{XWT}	0.5	—	—	μs	
Main clock oscillator oscillation frequency*2	2.4 ≤ VCC ≤ 3.6	f_{MAIN}	1	—	20	MHz	
	1.8 ≤ VCC < 2.4		1	—	8		
Main clock oscillation stabilization time (crystal)*2		$t_{MAINOSC}$	—	3	—	ms	Figure 51.20
Main clock oscillation stabilization time (ceramic resonator)*2		$t_{MAINOSC}$	—	50	—	μs	
LOCO clock oscillation frequency		f_{LOCO}	3.44	4.0	4.56	MHz	
LOCO clock oscillation stabilization time		t_{LOCO}	—	—	0.5	μs	Figure 51.21
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	
IWDT-dedicated clock oscillation stabilization time		t_{ILOCO}	—	—	50	μs	Figure 51.22
Bluetooth-dedicated clock oscillation frequency		f_{BLECK}	—	32	—	MHz	
Bluetooth-dedicated low-speed on-chip oscillator oscillation frequency		$f_{BLELOCO}$	—	32.768	—	kHz	
HOCO clock oscillation frequency		f_{HOCO} (32 MHz)	31.36	32	32.64	MHz	T_a = 0 to +85°C
			31.04	32	32.96		T_a = –40 to +85°C
		f_{HOCO} (54 MHz)	52.96	54	55.08	MHz	T_a = 0 to +85°C
			52.38	54	55.62		T_a = –40 to +85°C
HOCO clock oscillation stabilization time		t_{HOCO}	—	—	30	μs	Figure 51.24
PLL input frequency*3		f_{PLLIN}	4	—	12.5	MHz	
PLL circuit oscillation frequency*3		f_{PLL}	24	—	54	MHz	
PLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 51.25
PLL free-running oscillation frequency		f_{PLLFR}	—	8	—	MHz	
USBPLL input frequency*5		f_{PLLIN}	—	4, 6, 8, 12	—	MHz	
USBPLL circuit oscillation frequency*5		f_{PLL}	—	48*6	—	MHz	
USBPLL clock oscillation stabilization time		t_{PLL}	—	—	50	μs	Figure 51.25
Sub-clock oscillator oscillation frequency*7		f_{SUB}	—	32.768	—	kHz	
Sub-clock oscillation stabilization time*4		t_{SUBOSC}	—	0.5	—	s	Figure 51.26

Note 1. Time until the clock can be used after the main clock oscillator stop bit (MOSCCR.MOSTP) is set to 0 (operating).
Note 2. Reference values when an 8-MHz resonator is used.
When specifying the main clock oscillator stabilization time, set the MOSCWTCR register with a stabilization time value that is equal to or greater than the resonator-manufacturer-recommended value.
After the MOSCCR.MOSTP bit is changed to enable the main clock oscillator, confirm that the OSCOVFSR.MOOVF flag has become 1, and then start using the main clock.
Note 3. The VCC range should be 2.4 to 3.6 V when the PLL is used.
Note 4. Reference values when a 32.768-kHz resonator is used.
After the setting of the SOSCCR.SOSTP bit or RCR3.RTCEN bit is changed to operate the sub-clock oscillator, only start using the sub-clock after the sub-clock oscillation stabilization wait time that is equal to or greater than the oscillator-manufacturer-recommended value has elapsed.
Note 5. The VCC range should be 3.0 to 3.6 V when the USBPLL is used.
Note 6. The oscillation frequency can be set to 48 MHz only.
Note 7. Only 32.768 kHz can be used.

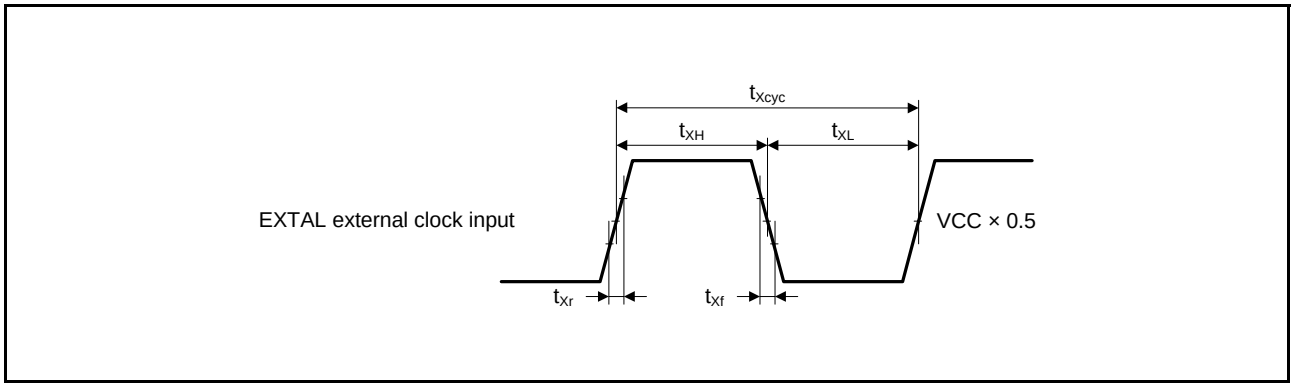


Figure 51.19 EXTAL External Clock Input Timing

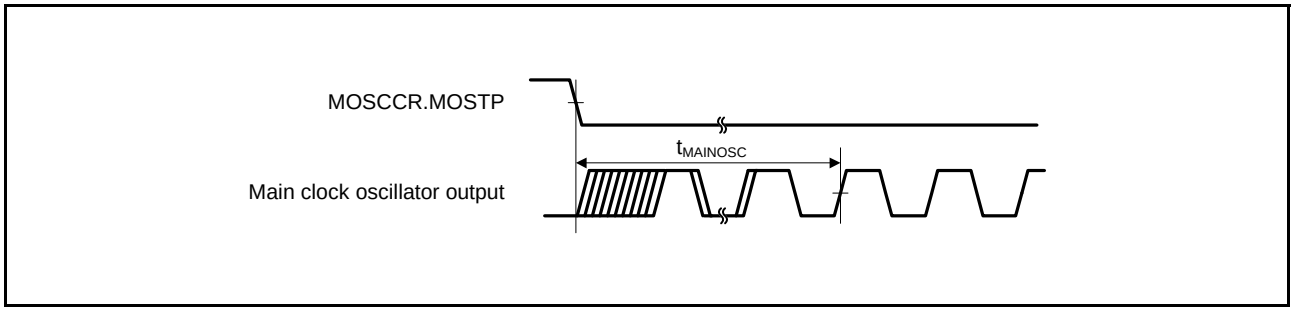


Figure 51.20 Main Clock Oscillation Start Timing

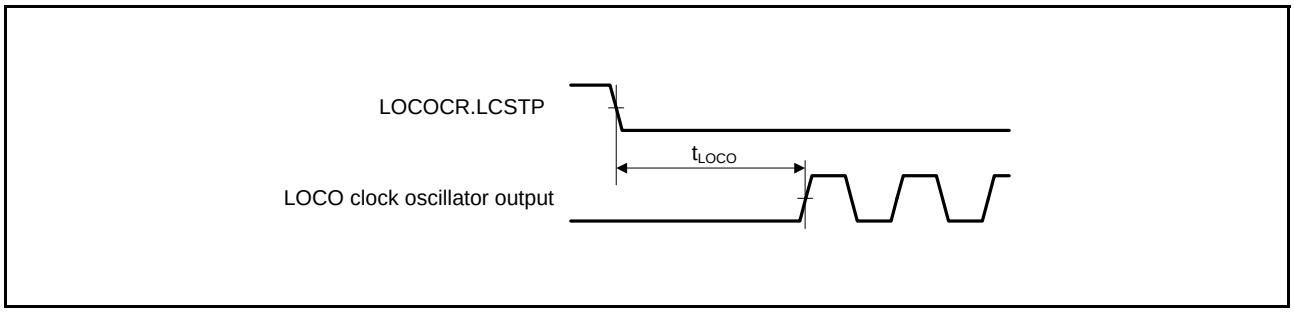


Figure 51.21 LOCO Clock Oscillation Start Timing

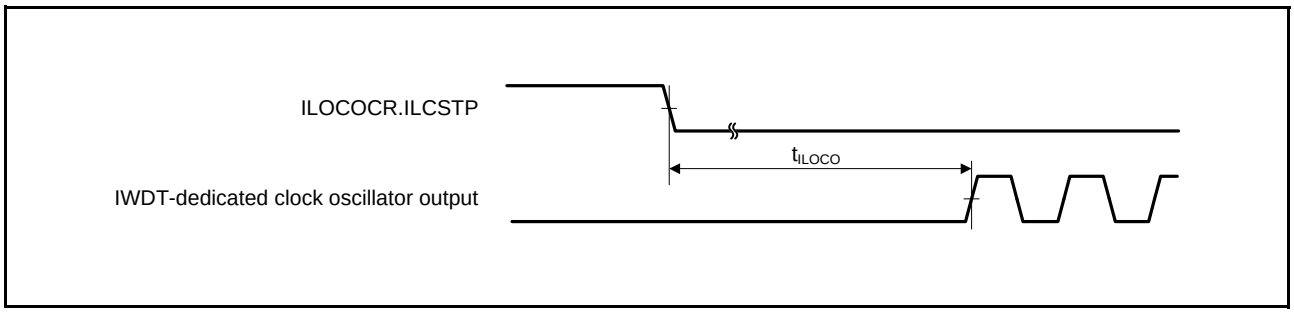


Figure 51.22 IWDT-Dedicated Clock Oscillation Start Timing

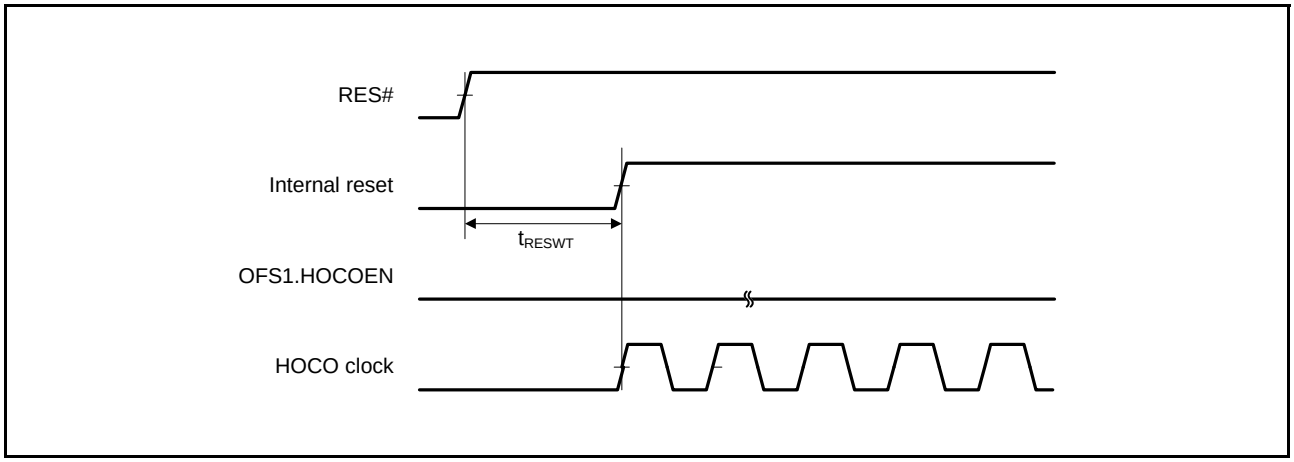


Figure 51.23 HOCO Clock Oscillation Start Timing (After Reset is Canceled by Setting OFS1.HOCOEN Bit to 0)

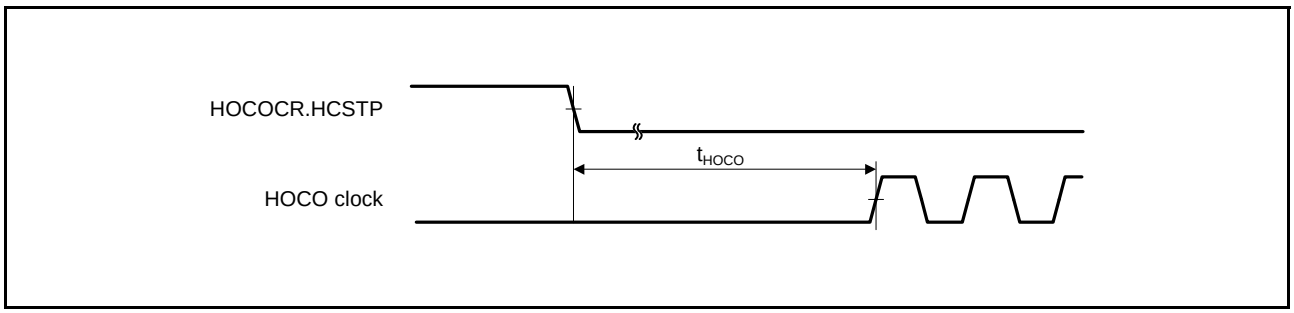


Figure 51.24 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting HOCOCR.HCSTP Bit)

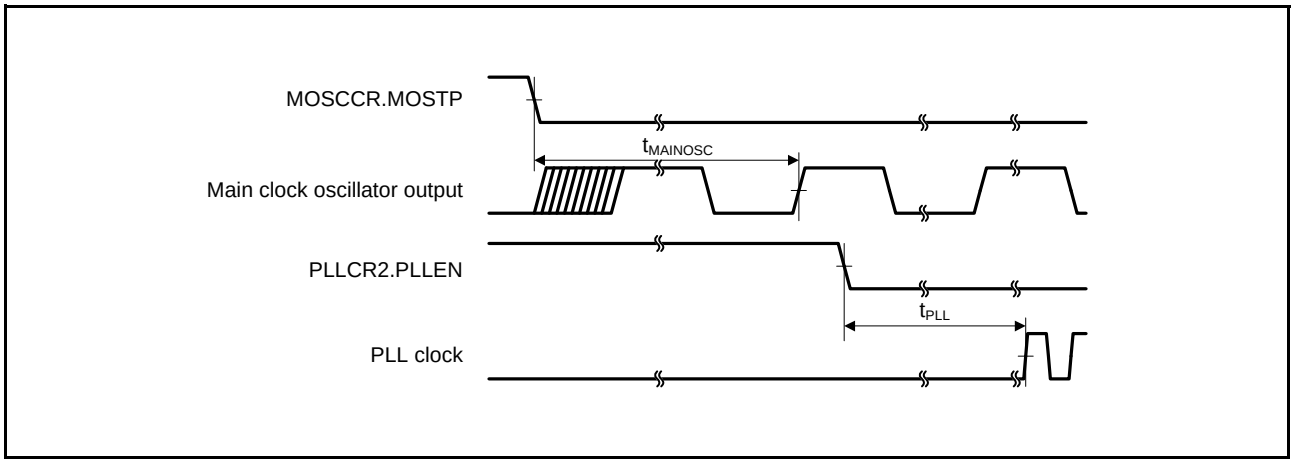


Figure 51.25 PLL Clock Oscillation Start Timing (PLL is Operated after Main Clock Oscillation Has Been Stabled)

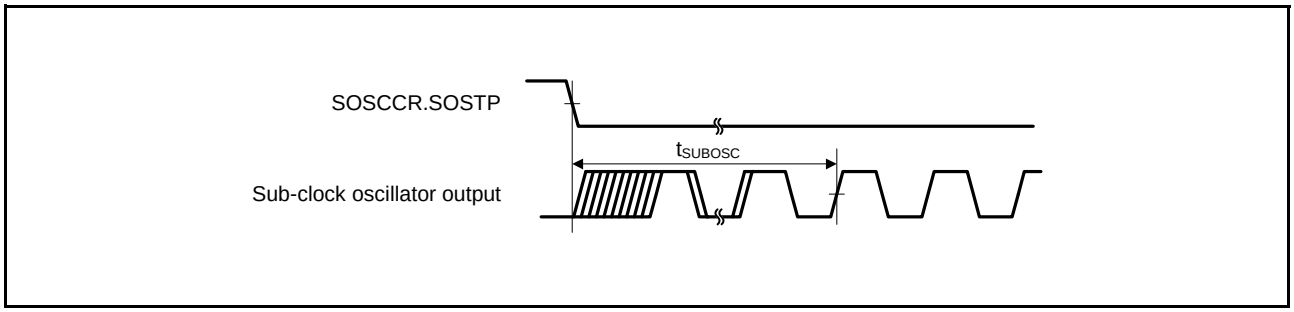


Figure 51.26 Sub-Clock Oscillation Start Timing

51.3.2 Reset Timing

Table 51.25 Reset Timing

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RES# pulse width	At power-on	t_{RESWP}	3	—	—	ms	Figure 51.27
	Other than above	t_{RESW}	30	—	—	µs	Figure 51.28
Wait time after RES# cancellation (at power-on)	At normal startup*1	t_{RESWT}	—	8.5	—	ms	Figure 51.27
	During fast startup time*2	t_{RESWT}	—	560	—	µs	
Wait time after RES# cancellation (during powered-on state)		t_{RESWT}	—	120	—	µs	Figure 51.28
Independent watchdog timer reset period		t_{RESWIW}	—	1	—	IWDT clock cycle	Figure 51.29
Watchdog timer reset period		t_{RESWWW}	—	4	—	PCLKB cycle	
Software reset period		t_{RESWSW}	—	1	—	ICLK cycle	
Wait time after independent watchdog timer reset cancellation*3		t_{RESWT2}	—	300	—	µs	
Wait time after watchdog timer reset cancellation*4		t_{RESWT2}	—	300	—	µs	
Wait time after software reset cancellation		t_{RESWT2}	—	170	—	µs	

Note 1. When OFS1.(LVDAS, FASTSTUP) bits are 11b.
Note 2. When OFS1.(LVDAS, FASTSTUP) bits are a value other than 11b.
Note 3. When IWDTCR.CKS[3:0] bits are 0000b.
Note 4. When WDTCR.CKS[3:0] bits are 0001b.

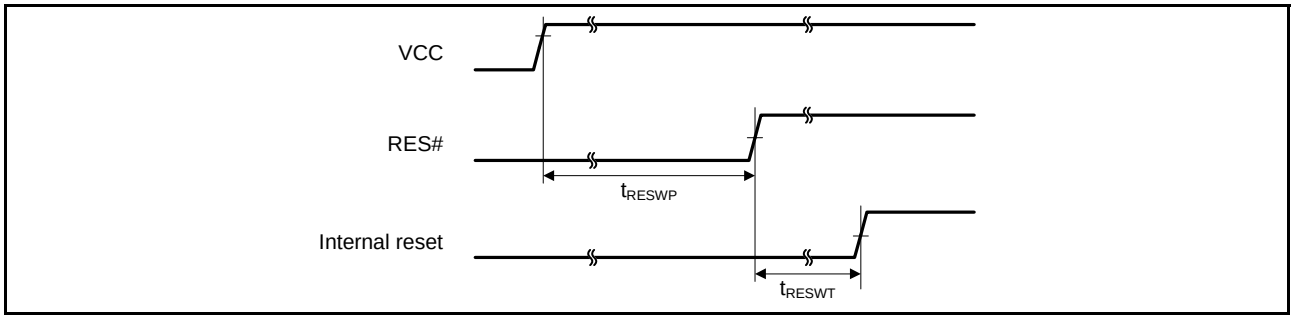


Figure 51.27 Reset Input Timing at Power-On

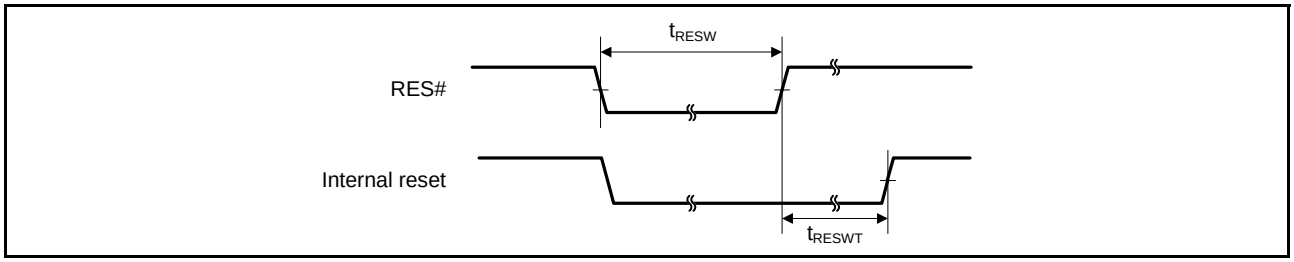


Figure 51.28 Reset Input Timing (1)

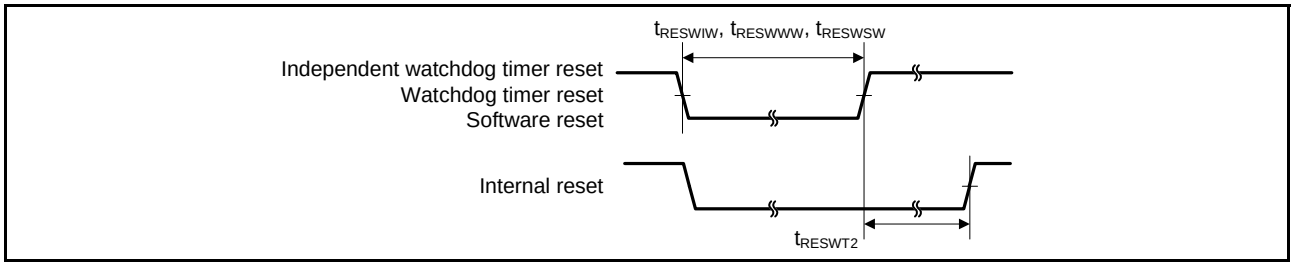


Figure 51.29 Reset Input Timing (2)

51.3.3 Timing of Recovery from Low Power Consumption Modes

Table 51.26 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	High-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 51.30
		External clock input to main clock oscillator	Main clock oscillator operating*3	t_{SBYEX}	—	35	50	µs	
		Sub-clock oscillator operating		t_{SBYSC}	—	650	800	µs	
		HOCO clock oscillator operating		t_{SBYHO}	—	40	55	µs	
		LOCO clock oscillator operating		t_{SBYLO}	—	40	55	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. When multiple oscillators are operating, the recovery time varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
Note 2. When the frequency of the crystal is 20 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 3. When the frequency of the external clock is 20 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.

Table 51.27 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item				Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Middle-speed mode	Crystal connected to main clock oscillator	Main clock oscillator operating*2	t_{SBYMC}	—	2	3	ms	Figure 51.30
			Main clock oscillator and PLL circuit operating*3	t_{SBYPC}	—	2	3	ms	
		External clock input to main clock oscillator	Main clock oscillator operating*4	t_{SBYEX}	—	3	4	µs	
			Main clock oscillator and PLL circuit operating*5	t_{SBYPE}	—	65	85	µs	
		Sub-clock oscillator operating		t_{SBYSC}	—	600	750	µs	
		HOCO clock oscillator operating*6		t_{SBYHO}	—	40	50	µs	
		LOCO clock oscillator operating		t_{SBYLO}	—	5	7	µs	

Note 1. The recovery time varies depending on the state of each oscillator when the WAIT instruction is executed. When multiple oscillators are operating, the recovery time varies depending on the operating state of the oscillators that are not selected as the system clock source. The above table applies when only the corresponding clock is operating.
Note 2. When the frequency of the crystal is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 3. When the frequency of PLL is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 04h.
Note 4. When the frequency of the external clock is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
Note 5. When the frequency of PLL is 12 MHz.
When the main clock oscillator wait control register (MOSCWTCR) is set to 00h.
Note 6. This is the case when HOCO is selected as the system clock and its frequency division is set to be 8 MHz.

Table 51.28 Timing of Recovery from Low Power Consumption Modes (3)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item			Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from software standby mode*1	Low-speed mode	Sub-clock oscillator operating	t_{SBYSC}	—	600	750	µs	Figure 51.30

Note 1. The sub-clock continues oscillating in software standby mode during low-speed mode.

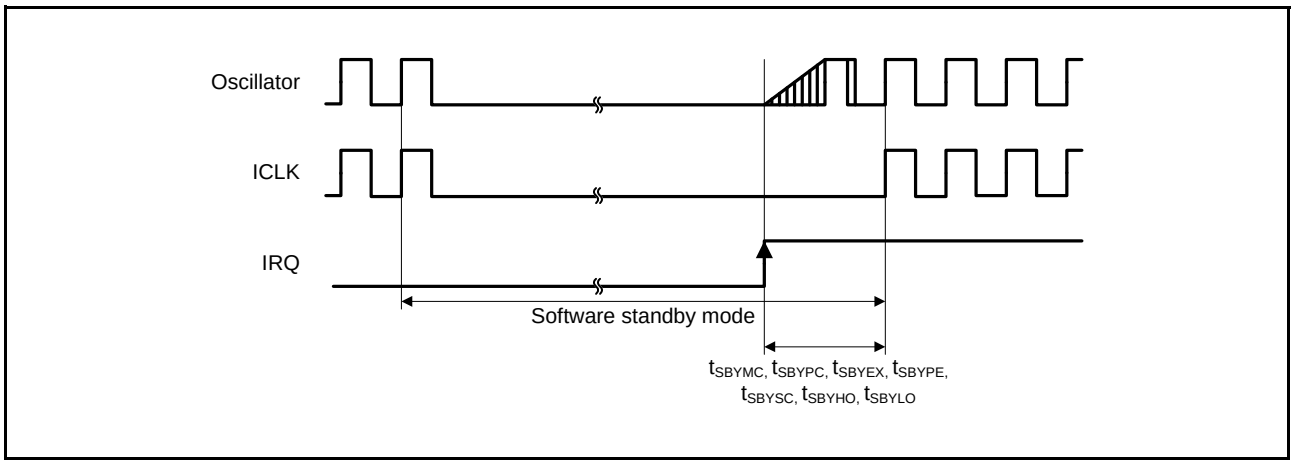


Figure 51.30 Software Standby Mode Recovery Timing

Table 51.29 Timing of Recovery from Low Power Consumption Modes (4)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Recovery time from deep sleep mode*1	High-speed mode*2	t_{DSLP}	—	2	3.5	µs	Figure 51.31
	Middle-speed mode*3	t_{DSLP}	—	3	4	µs	
	Low-speed mode*4	t_{DSLP}	—	400	500	µs	

Note 1. Oscillators continue oscillating in deep sleep mode.
Note 2. When the frequency of the system clock is 32 MHz.
Note 3. When the frequency of the system clock is 12 MHz.
Note 4. When the frequency of the system clock is 32 kHz.

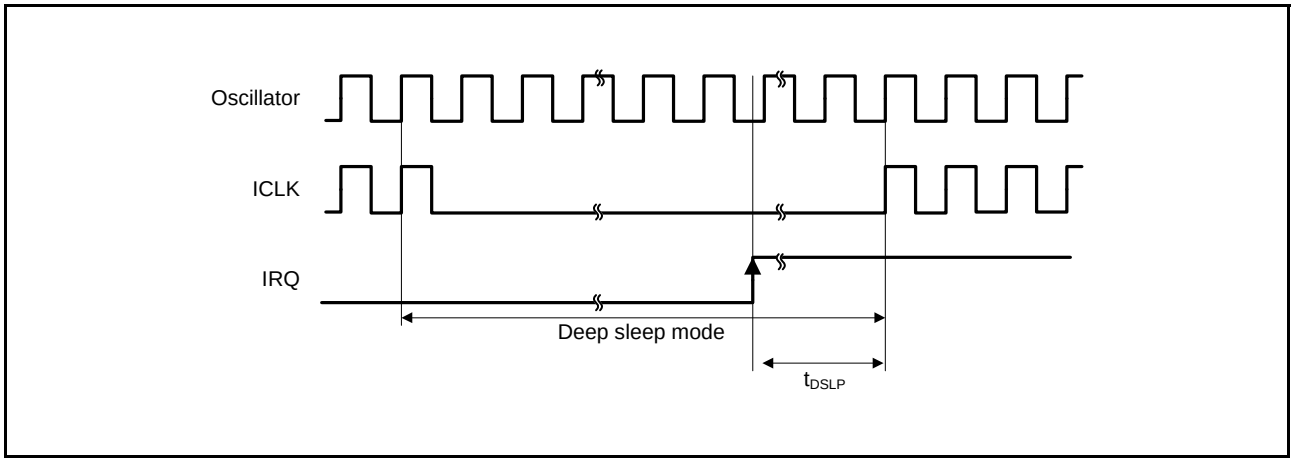


Figure 51.31 Deep Sleep Mode Recovery Timing

Table 51.30 Operating Mode Transition Time

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Mode before Transition	Mode after Transition	ICLK Frequency	Transition Time			Unit
			Min.	Typ.	Max.	
High-speed operating mode	Middle-speed operating modes	8 MHz	—	10	—	µs
Middle-speed operating modes	High-speed operating mode	8 MHz	—	37.5	—	µs
Low-speed operating mode	Middle-speed operating mode, high-speed operating mode	32.768 kHz	—	215	—	µs
Middle-speed operating mode, high-speed operating mode	Low-speed operating mode	32.768 kHz	—	185	—	µs

Note: Values when the frequencies of PCLKA, PCLKB, PCLKD, and FCLK, are not divided.

51.3.4 Control Signal Timing

Table 51.31 Control Signal Timing

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
NMI pulse width	t_{NMIW}	200	—	—	ns	NMI digital filter is disabled (NMIFLTE.NFLTEN = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		NMI digital filter is enabled (NMIFLTE.NFLTEN = 1)	t_{NMICK} × 3 ≤ 200 ns
		t_{NMICK} × 3.5*2	—	—			t_{NMICK} × 3 > 200 ns
IRQ pulse width	t_{IRQW}	200	—	—	ns	IRQ digital filter is disabled (IRQFLTE0.FLTENi = 0)	t_{Pcyc} × 2 ≤ 200 ns
		t_{Pcyc} × 2*1	—	—			t_{Pcyc} × 2 > 200 ns
		200	—	—		IRQ digital filter is enabled (IRQFLTE0.FLTENi = 1)	t_{IRQCK} × 3 ≤ 200 ns
		t_{IRQCK} × 3.5*3	—	—			t_{IRQCK} × 3 > 200 ns

Note: 200 ns minimum in software standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 7).

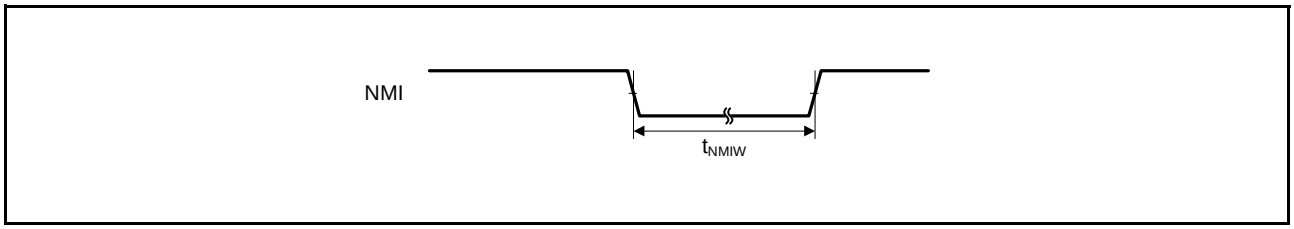


Figure 51.32 NMI Interrupt Input Timing

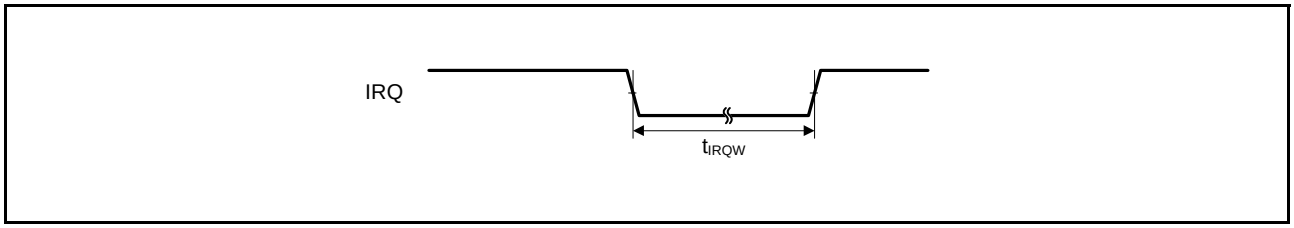


Figure 51.33 IRQ Interrupt Input Timing

51.3.5 Timing of On-Chip Peripheral Modules

51.3.5.1 Timing of I/O Ports

Table 51.32 Timing of I/O Ports

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

Item		Symbol	Min.	Max.	Unit *1	Test Conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	—	t_{Pcyc}	Figure 51.34

Note 1. t_{Pcyc}: PCLK cycle

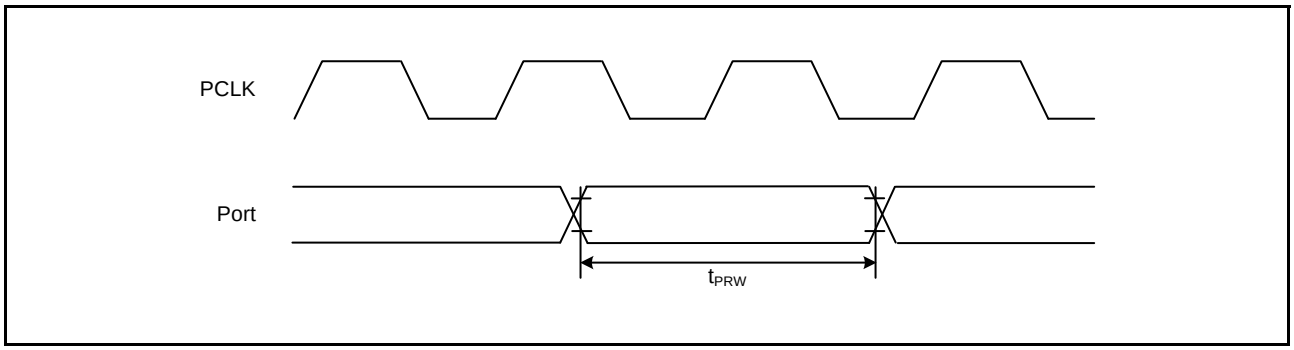


Figure 51.34 I/O Port Input Timing

51.3.5.2 Timing of MTU/TPU

Table 51.33 Timing of MTU/TPU

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
MTU/TPU	Input capture input pulse width	Single-edge setting	t_{TICW}	1.5	—	t_{Pcyc}	Figure 51.35
		Both-edge setting		2.5	—		
	Timer clock pulse width	Single-edge setting	t_{TCKWH}, t_{TCKWL}	1.5	—	t_{Pcyc}	Figure 51.36
		Both-edge setting		2.5	—		
		Phase counting mode		2.5	—		

Note 1. t_{Pcyc}: PCLK cycle

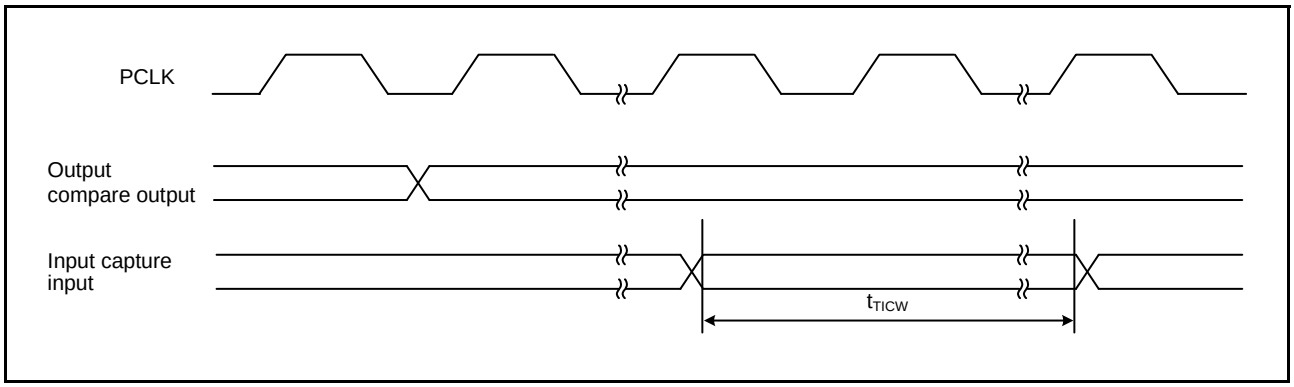


Figure 51.35 MTU Input/Output Timing

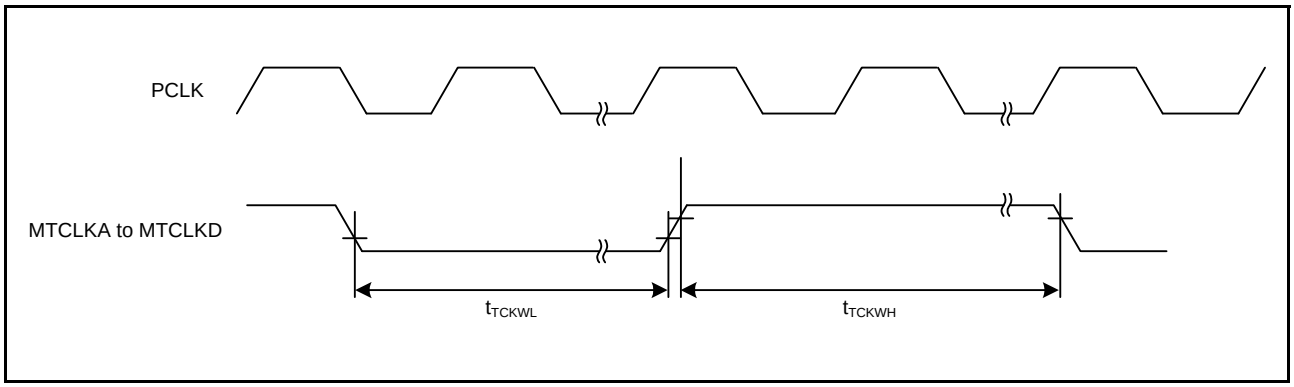


Figure 51.36 MTU Clock Input Timing

51.3.5.3 Timing of POE

Table 51.34 Timing of POE

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

Item		Symbol	Min.	Max.	Unit *1	Test Conditions
POE	POE# input pulse width	t_{POEW}	1.5	—	t_{Pcyc}	Figure 51.37

Note 1. t_{Pcyc}: PCLK cycle

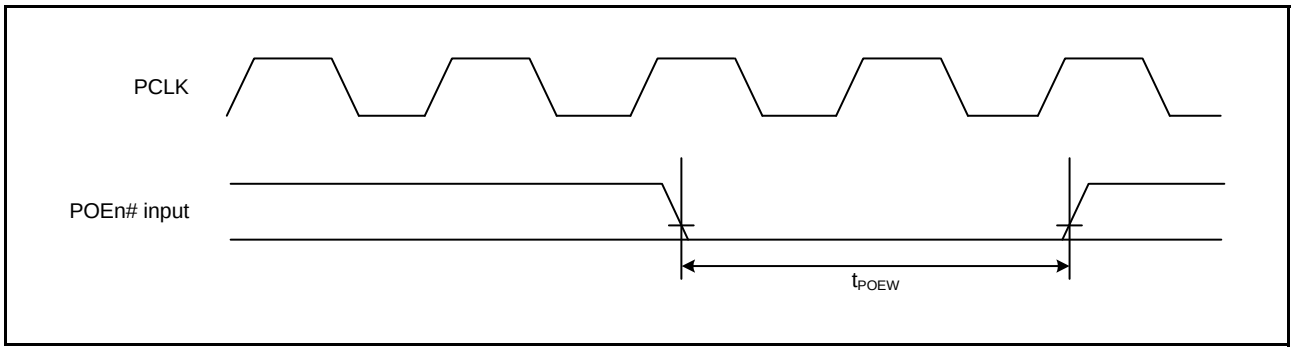


Figure 51.37 POE# Input Timing

51.3.5.4 Timing of TMR

Table 51.35 Timing of TMR

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
TMR	Timer clock pulse width	Single-edge setting	t_{TMCWH}, t_{TMCWL}	1.5	—	t_{Pcyc}	Figure 51.38
		Both-edge setting		2.5	—		

Note 1. t_{Pcyc}: PCLK cycle

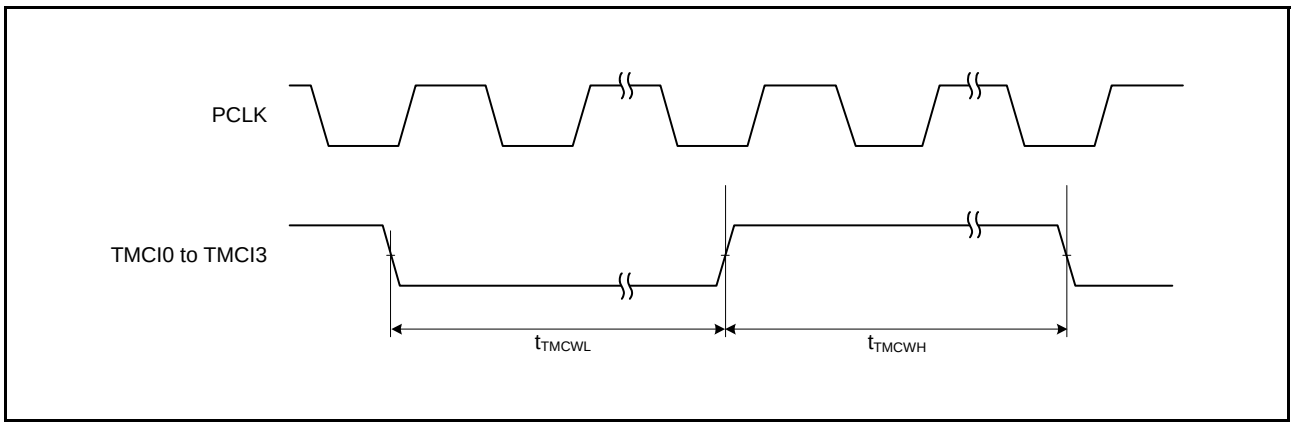


Figure 51.38 TMR Clock Input Timing

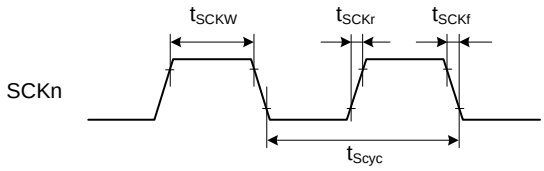
51.3.5.5 Timing of SCI

Table 51.36 Timing of SCI

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

Item				Symbol	Min.	Max.	Unit *1	Test Conditions
SCI	Input clock cycle time		Asynchronous	t_{Scyc}	4	—	t_{Pcyc}	Figure 51.39
			Clock synchronous		6	—		
	Input clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time			t_{SCKr}	—	20	ns	
	Input clock fall time			t_{SCKf}	—	20	ns	
	Output clock cycle time		Asynchronous	t_{Scyc}	16	—	t_{Pcyc}	Figure 51.40
			Clock synchronous		4	—		
	Output clock pulse width			t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time			t_{SCKr}	—	20	ns	
	Output clock fall time			t_{SCKf}	—	20	ns	
	Transmit data delay time (master)	Clock synchronous		t_{TXD}	—	40	ns	
	Transmit data delay time (slave)	Clock synchronous	2.7 V or above		—	65	ns	
			1.8 V or above		—	100	ns	
	Receive data setup time (master)	Clock synchronous	2.7 V or above	t_{RXS}	65	—	ns	
			1.8 V or above		90	—	ns	
	Receive data setup time (slave)	Clock synchronous			40	—	ns	
	Receive data hold time	Clock synchronous		t_{RXH}	40	—	ns	

Note 1. t_{Pcyc}: PCLK cycle



n = 1, 5, 8, 12

Figure 51.39 SCK Clock Input Timing

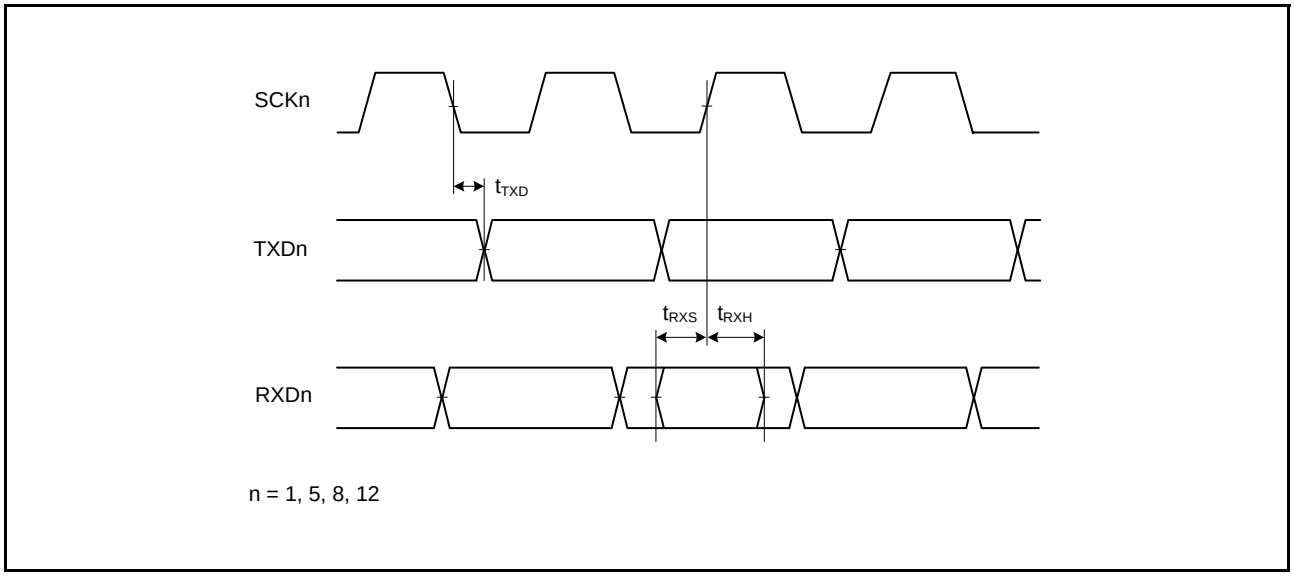


Figure 51.40 SCI Input/Output Timing: Clock Synchronous Mode

Table 51.37 Timing of Simple I²C

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, fPCLKB ≤ 32 MHz, T_a = –40 to +85°C

Item		Symbol	Min.*1	Max.	Unit	Test Conditions
Simple I²C (Standard mode)	SSDA rise time	t_{Sr}	—	1000	ns	Figure 51.41
	SSDA fall time	t_{Sf}	—	300	ns	
	SSDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data setup time	t_{SDAS}	250	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b	—	400	pF	
Simple I²C (Fast mode)	SSDA rise time	t_{Sr}	—	300	ns	Figure 51.41
	SSDA fall time	t_{Sf}	—	300	ns	
	SSDA spike pulse removal time	t_{SP}	0	4 × t_{Pcyc}	ns	
	Data setup time	t_{SDAS}	100	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SSCL, SSDA capacitive load	C_b	—	400	pF	

Note: t_{Pcyc}: PCLK cycle
Note 1. C_b is the total capacitance of the bus lines.

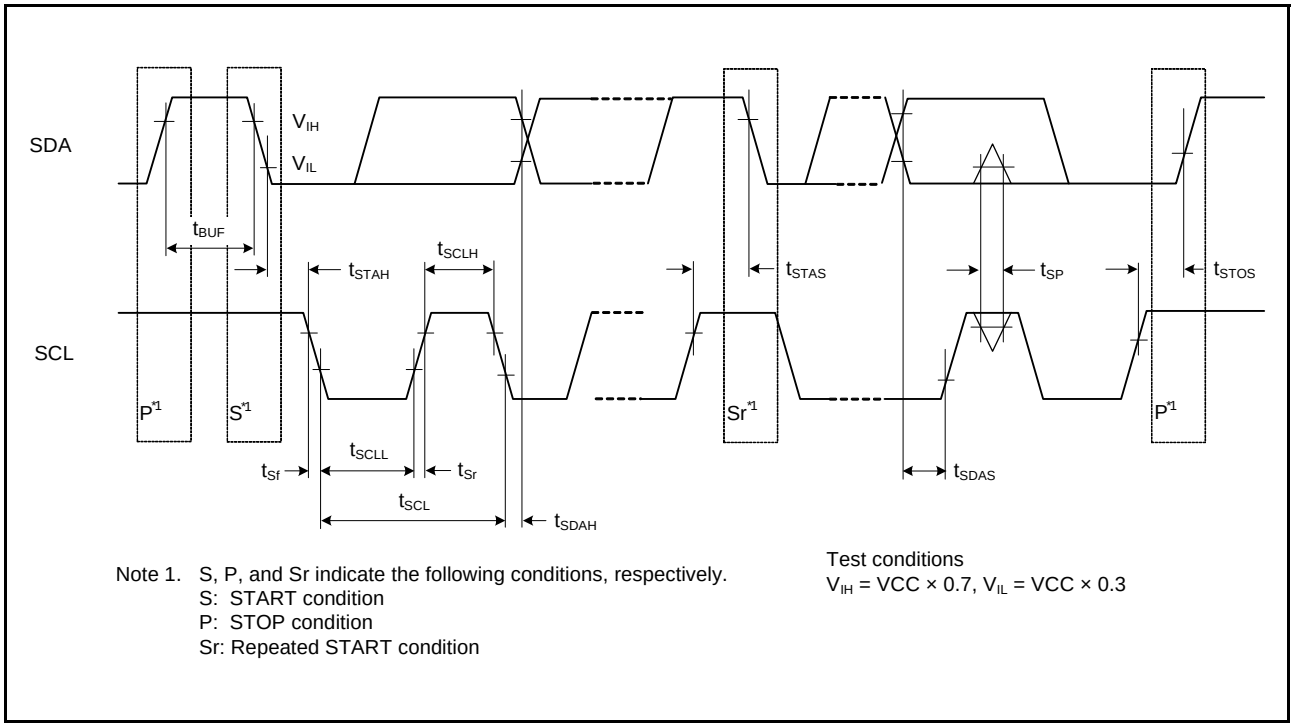


Figure 51.41 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

Table 51.38 Timing of Simple SPI

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

Item			Symbol	Min.	Max.	Unit*1	Test Conditions
Simple SPI	SCK clock cycle output (master)		t_{SPcyc}	4	65536	t_{Pcyc}	Figure 51.42
	SCK clock cycle input (slave)			6	65536	t_{Pcyc}	
	SCK clock high pulse width		t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width		t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise/fall time		t_{SPCKr}, t_{SPCKf}	—	20	ns	
	Data input setup time (master)	2.7 V or above	t_{SU}	65	—	ns	Figure 51.43, Figure 51.44
		1.8 V or above		95	—		
	Data input setup time (slave)			40	—		
	Data input hold time		t_H	40	—	ns	
	SSL input setup time		t_{LEAD}	3	—	t_{SPcyc}	
	SSL input hold time		t_{LAG}	3	—	t_{SPcyc}	
	Data output delay time (master)		t_{OD}	—	40	ns	
	Data output delay time (slave)	2.7 V or above		—	65		
		1.8 V or above		—	100		
	Data output hold time (master)	2.7 V or above	t_{OH}	–10	—	ns	
		1.8 V or above		–20	—		
	Data output hold time (slave)			–10	—		
	Data rise/fall time		t_{Dr}, t_{Df}	—	20	ns	
	SSL input rise/fall time		t_{SSLr}, t_{SSLf}	—	20	ns	
	Slave access time		t_{SA}	—	6	t_{Pcyc}	Figure 51.45, Figure 51.46
	Slave output release time		t_{REL}	—	6	t_{Pcyc}	

Note 1. t_{Pcyc}: PCLK cycle

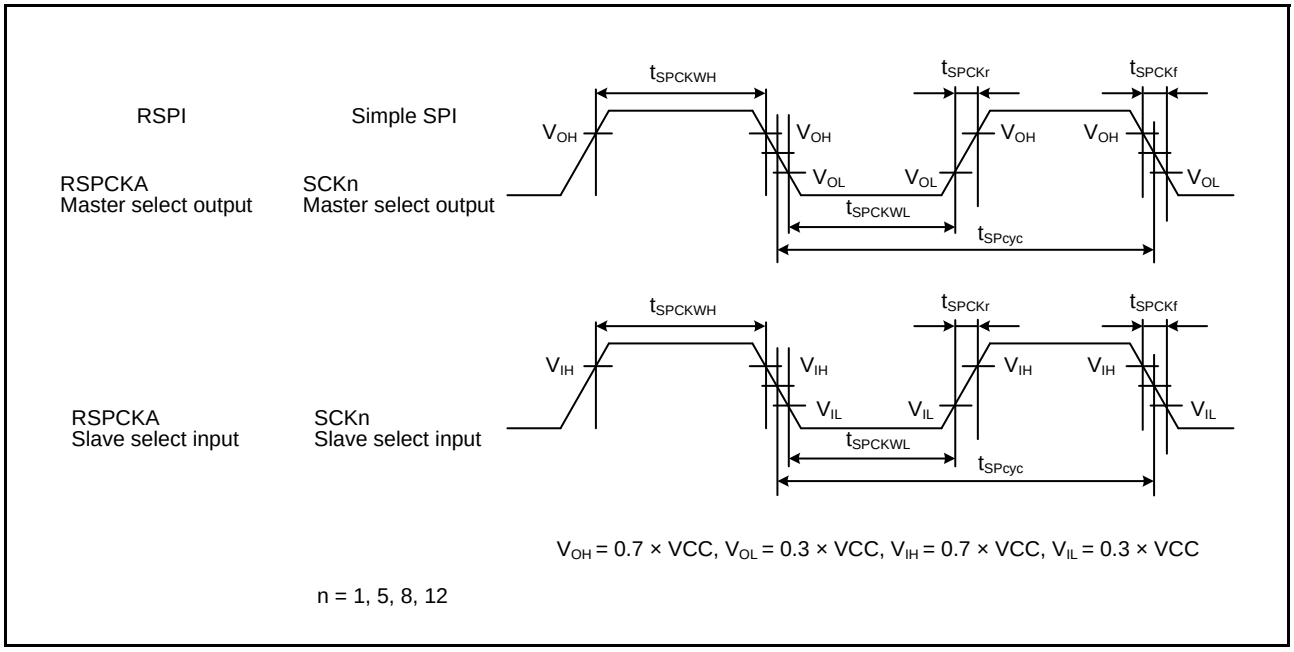


Figure 51.42 RSPI Clock Timing and Simple SPI Clock Timing

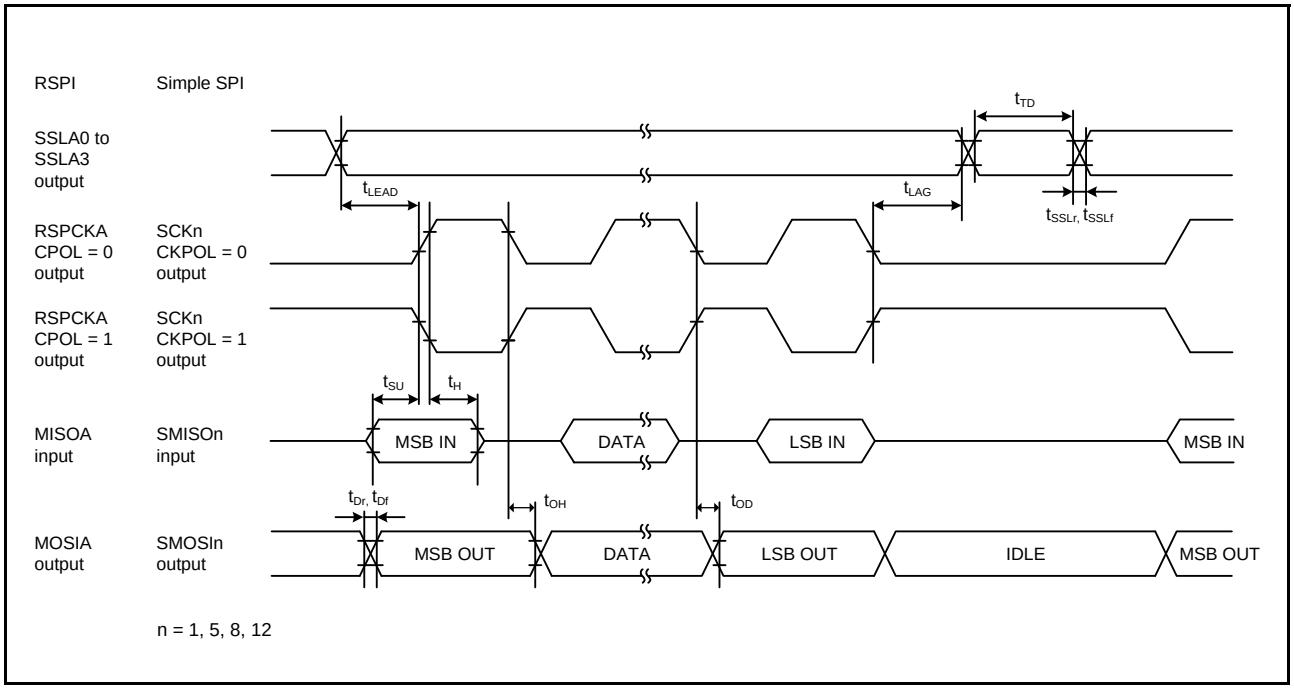


Figure 51.43 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)

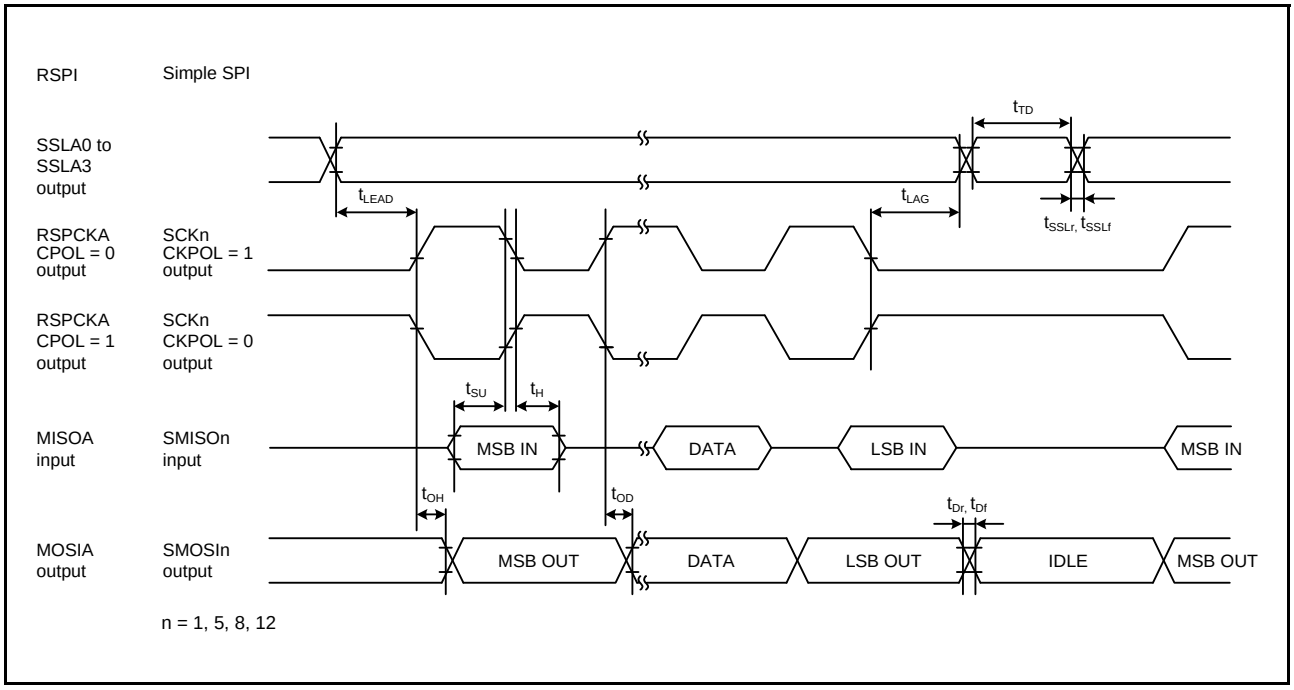


Figure 51.44 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

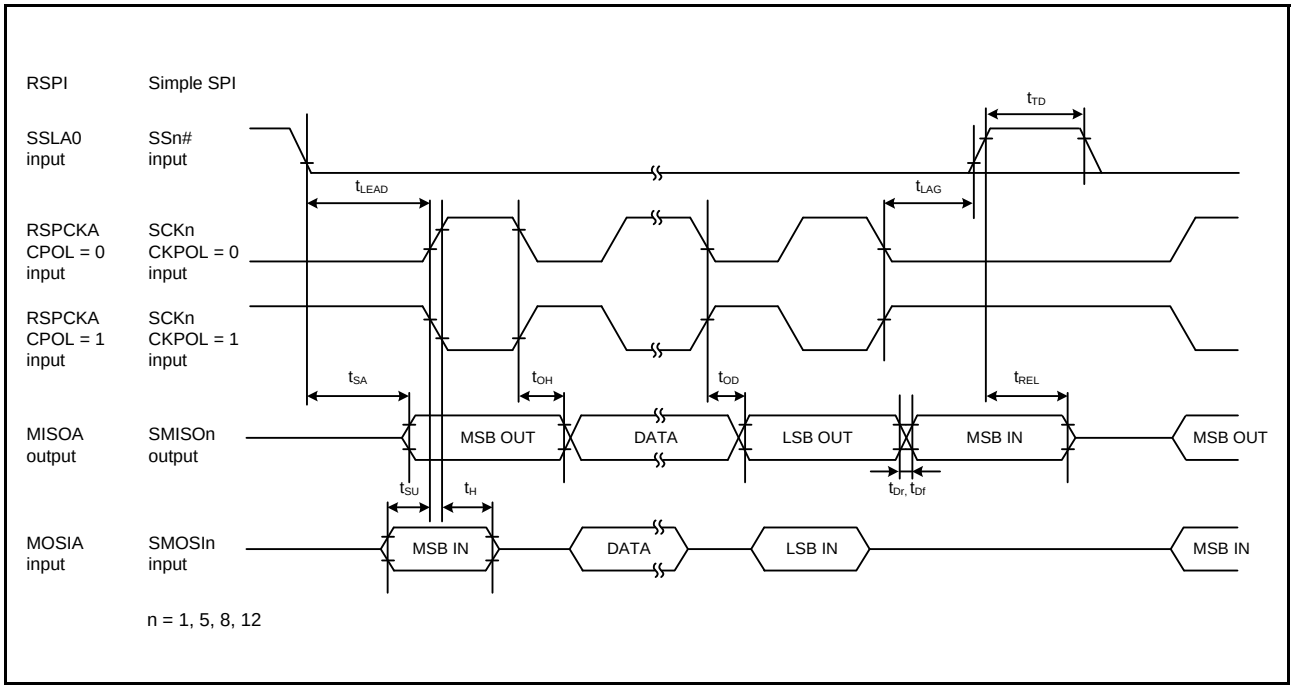


Figure 51.45 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

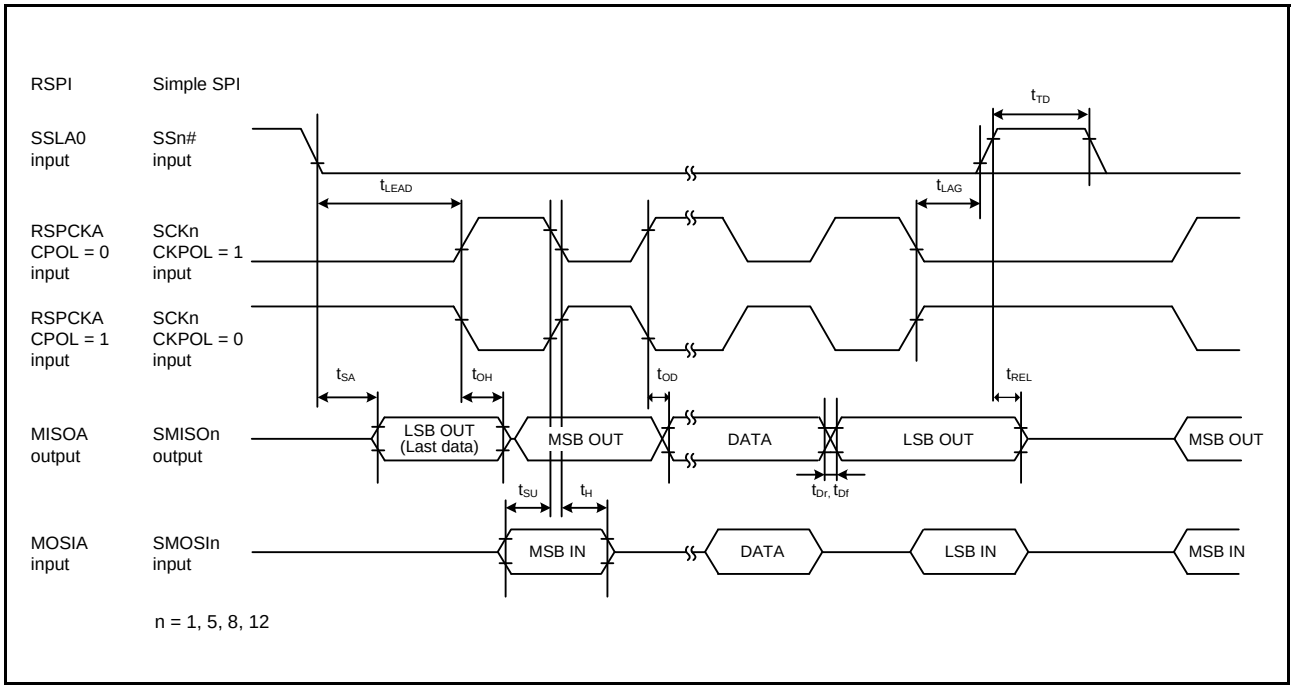


Figure 51.46 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)

51.3.5.6 Timing of RIIC

Table 51.39 Timing of RIIC

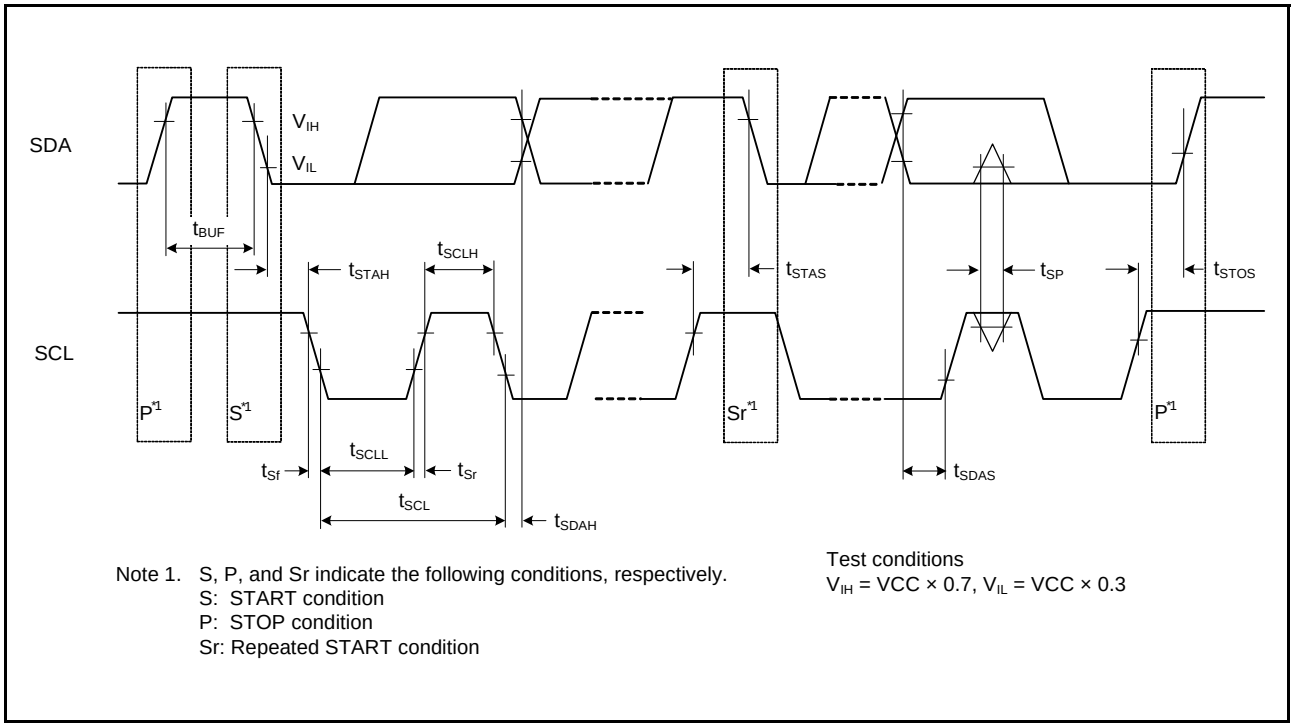
Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, fPCLKB ≤ 32 MHz, T_a = –40 to +85°C

Item		Symbol	Min.*1, *2	Max.	Unit	Test Conditions
RIIC (Standard mode, SMBus)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	—	ns	Figure 51.47
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	1000	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	1000	—	ns	
	STOP condition setup time	t_{STOS}	1000	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	
RIIC (Fast mode)	SCL cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	—	ns	Figure 51.47
	SCL high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	—	ns	
	SCL, SDA rise time	t_{Sr}	—	300	ns	
	SCL, SDA fall time	t_{Sf}	—	300	ns	
	SCL, SDA spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA bus free time	t_{BUF}	3 (6) × t_{IICcyc} + 300	—	ns	
	START condition hold time	t_{STAH}	t_{IICcyc} + 300	—	ns	
	Repeated START condition setup time	t_{STAS}	300	—	ns	
	STOP condition setup time	t_{STOS}	300	—	ns	
	Data setup time	t_{SDAS}	t_{IICcyc} + 50	—	ns	
	Data hold time	t_{SDAH}	0	—	ns	
	SCL, SDA capacitive load	C_b	—	400	pF	

Note: t_{IICcyc}: RIIC internal reference clock (IICφ) cycle

Note 1. The value in parentheses is used when the ICMR3.NF[1:0] bits are set to 11b while a digital filter is enabled with the ICFER.NFE bit = 1.

Note 2. C_b is the total capacitance of the bus lines.



Note 1. S, P, and Sr indicate the following conditions, respectively.
S: START condition
P: STOP condition
Sr: Repeated START condition

Figure 51.47 RIIC Bus Interface Input/Output Timing and Simple I²C Bus Interface Input/Output Timing

51.3.5.7 Timing of RSPI

Table 51.40 Timing of RSPI

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C, C = 30 pF, when high-drive output is selected by the drive capacity control register

Item				Symbol	Min.	Max.	Unit	Test Conditions
RSPI	RSPCK clock cycle	Master		t_{SPcyc}	2	4096	t_{Pcyc}*1	Figure 51.48
		Slave			8	4096		
	RSPCK clock high pulse width	Master		t_{SPCKWH}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock low pulse width	Master		t_{SPCKWL}	$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2 - 3$	—	ns	
		Slave			$(t_{SPcyc} - t_{SPCKr} - t_{SPCKf})/2$	—		
	RSPCK clock rise/fall time	Output	2.7 V or above	t_{SPCKr}, t_{SPCKf}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	µs	
	Data input setup time	Master	2.7 V or above	t_{SU}	10	—	ns	Figure 51.49 to Figure 51.52
			1.8 V or above		30	—		
		Slave			$25 - t_{Pcyc}$	—		
	Data input hold time	Master	RSPCK set to a division ratio other than PCLKB divided by 2	t_H	t_{Pcyc}	—	ns	
			RSPCK set to PCLKB divided by 2	t_{HF}	0	—		
		Slave		t_H	$20 + 2 \times t_{Pcyc}$	—		
	SSL setup time	Master		t_{LEAD}	$–30 + N^{*2} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	SSL hold time	Master		t_{LAG}	$–30 + N^{*3} \times t_{SPcyc}$	—	ns	
		Slave			2	—	t_{Pcyc}	
	Data output delay time	Master	2.7 V or above	t_{OD}	—	14	ns	
			1.8 V or above		—	30		
		Slave	2.7 V or above		—	$3 \times t_{Pcyc} + 65$		
			1.8 V or above		—	$3 \times t_{Pcyc} + 105$		
	Data output hold time	Master		t_{OH}	0	—	ns	
		Slave			0	—		
	Successive transmission delay time	Master		t_{TD}	$t_{SPcyc} + 2 \times t_{Pcyc}$	$8 \times t_{SPcyc} + 2 \times t_{Pcyc}$	ns	
		Slave			$4 \times t_{Pcyc}$	—		
	MOSI and MISO rise/fall time	Output	2.7 V or above	t_{Dr}, t_{Df}	—	10	ns	
			1.8 V or above		—	15		
		Input			—	1	µs	
	SSL rise/fall time	Output	2.7 V or above	t_{SSLr}, t_{SSLf}	—	10	ns	
			1.8 V or above		—	15	ns	
		Input			—	1	µs	
	Slave access time		2.7 V or above	t_{SA}	—	6	t_{Pcyc}	Figure 51.51, Figure 51.52
			1.8 V or above		—	7		
	Slave output release time		2.7 V or above	t_{REL}	—	5	t_{Pcyc}	
			1.8 V or above		—	6		

Note 1. t_{Pcyc}: PCLK cycle
Note 2. N: An integer from 1 to 8 that can be set by the RSPI clock delay register (SPCKD)
Note 3. N: An integer from 1 to 8 that can be set by the RSPI slave select negation delay register (SSLND)

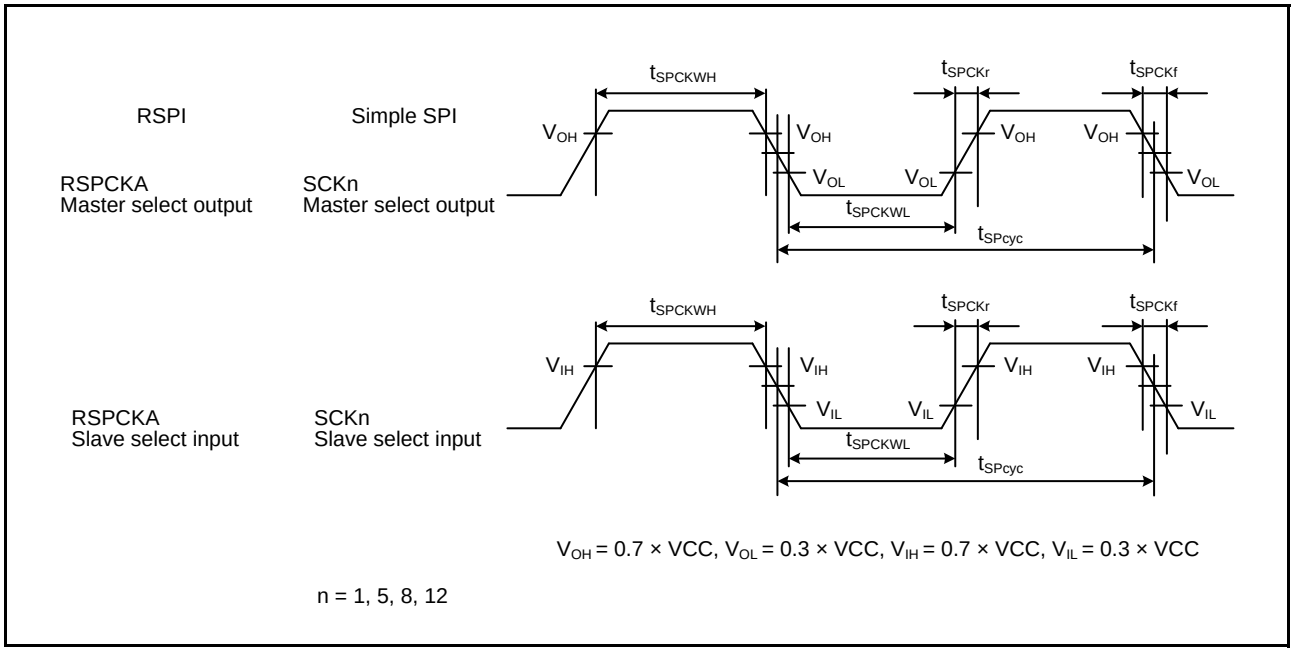


Figure 51.48 RSPI Clock Timing and Simple SPI Clock Timing

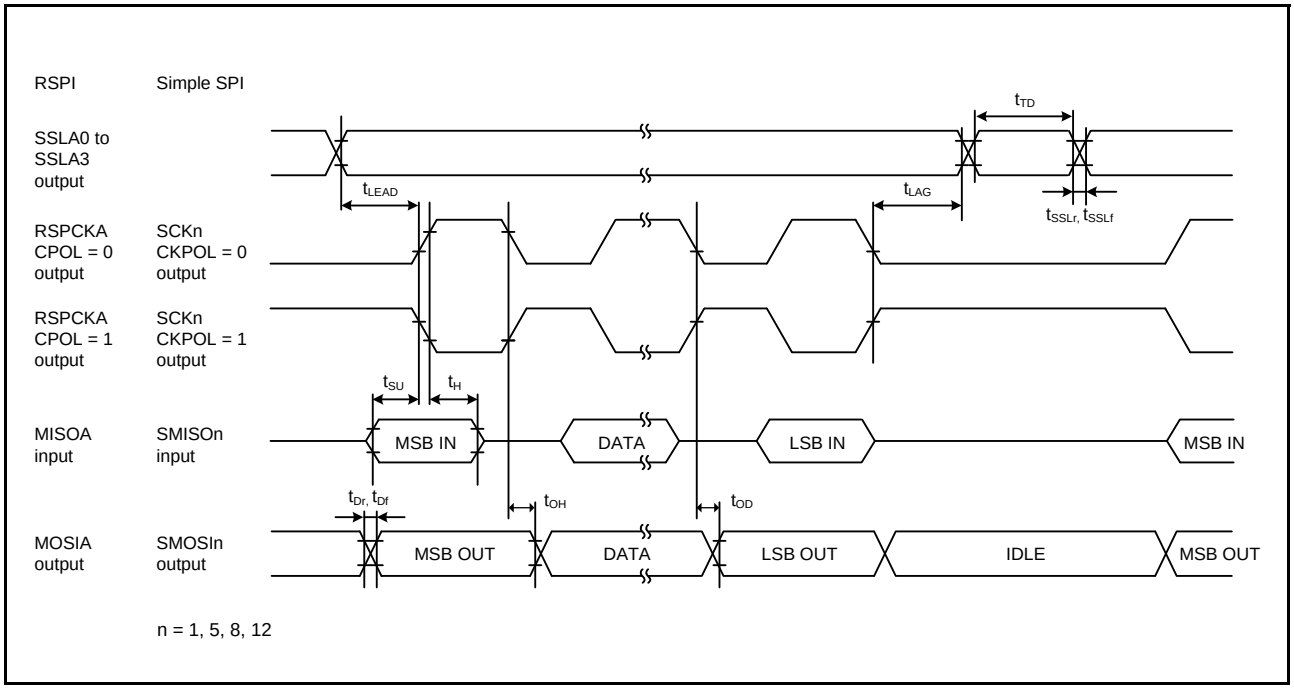


Figure 51.49 RSPI Timing (Master, CPHA = 0) and Simple SPI Clock Timing (Master, CKPH = 1)

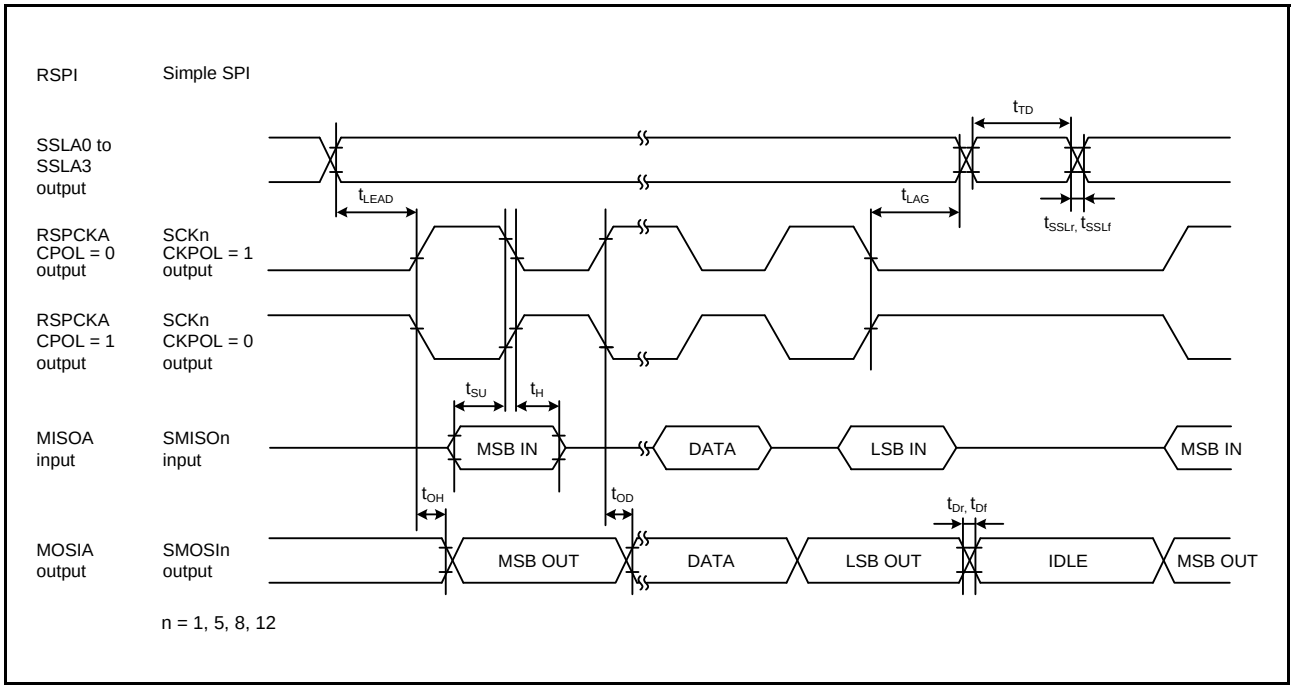


Figure 51.50 RSPI Timing (Master, CPHA = 1) and Simple SPI Clock Timing (Master, CKPH = 0)

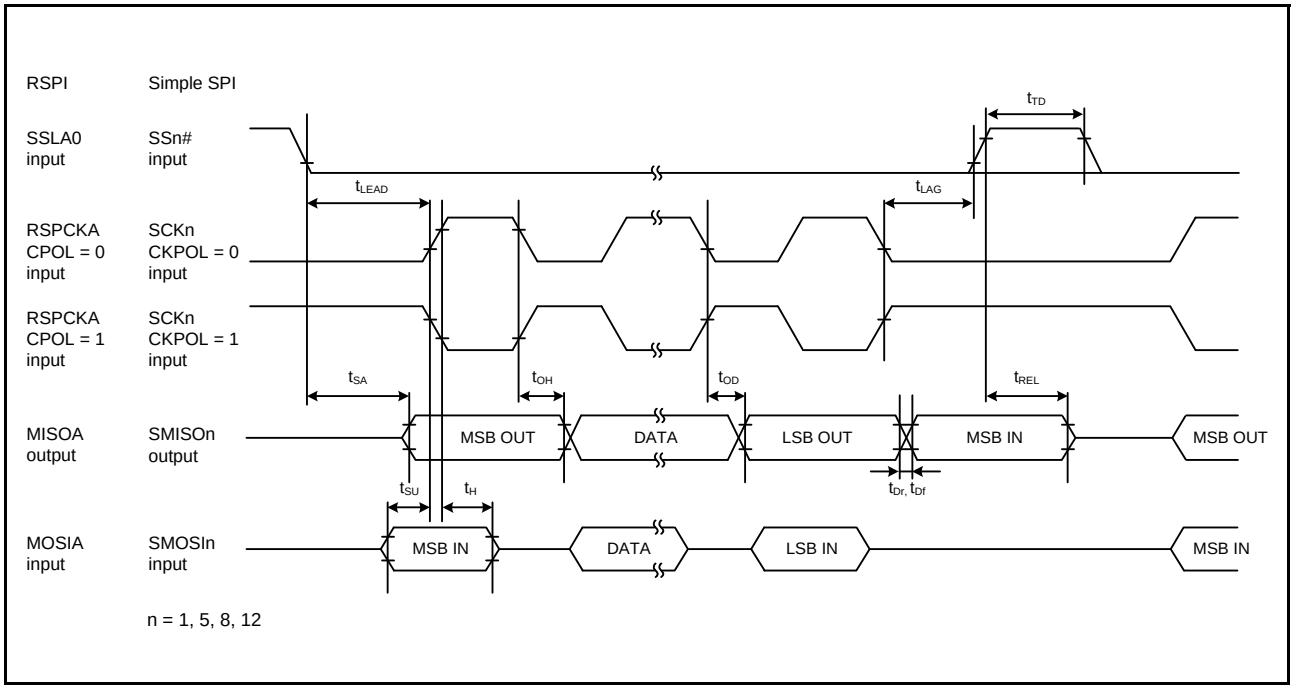


Figure 51.51 RSPI Timing (Slave, CPHA = 0) and Simple SPI Clock Timing (Slave, CKPH = 1)

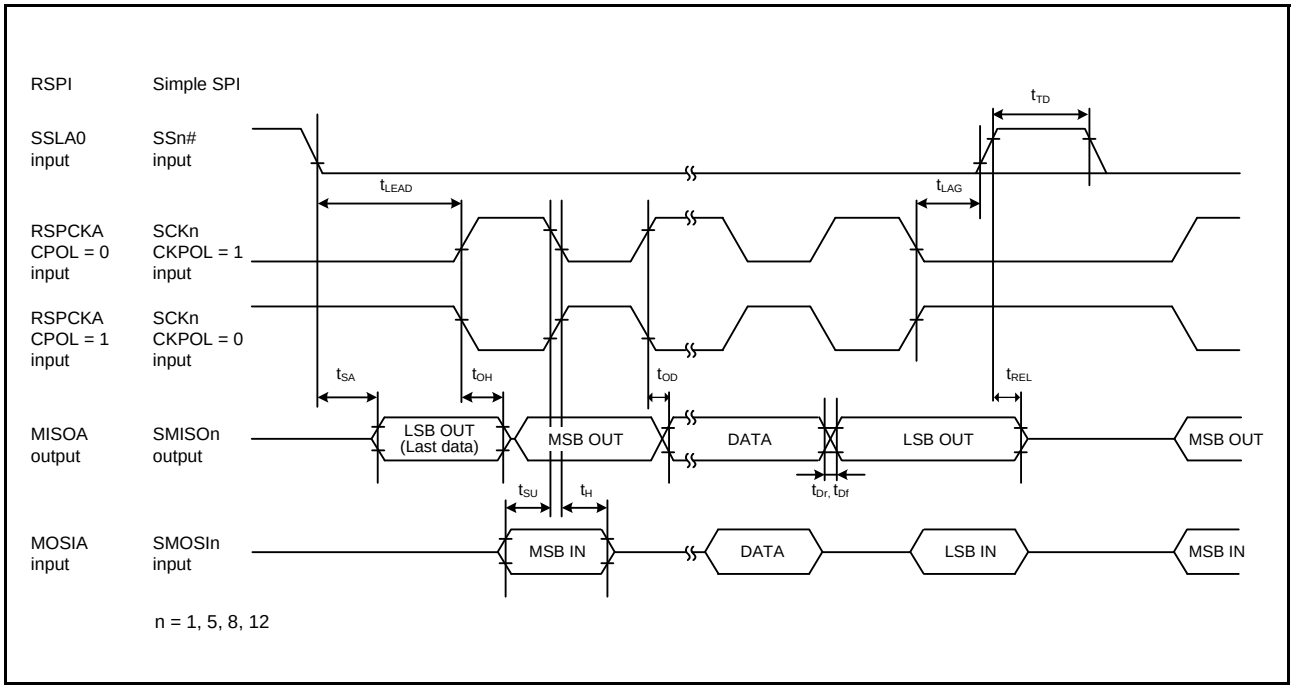


Figure 51.52 RSPI Timing (Slave, CPHA = 1) and Simple SPI Clock Timing (Slave, CKPH = 0)

51.3.5.8 Timing of SSI

Table 51.41 Timing of SSI

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, fPCLKB ≤ 32 MHz, T_a = –40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions
SSI	AUDIO_MCLK input frequency	2.7 V or above	t_{AUDIO}	1	25	MHz	
		1.8 V or above		1	4		
	Output clock cycle		t_O	250	—	ns	Figure 51.53
	Input clock cycle		t_I	250	—	ns	
	Clock high level		t_{HC}	0.4	0.6	to, ti	
	Clock low level		t_{LC}	0.4	0.6	to, ti	
	Clock rise time		t_{RC}	—	20	ns	
	Data delay time	2.7 V or above	t_{DTR}	—	65	ns	Figure 51.54 Figure 51.55
		1.8 V or above		—	105		
	Setup time	2.7 V or above	t_{SR}	65	—	ns	
		1.8 V or above		90	—		
	Hold time		t_{HTR}	40	—	ns	
	WS changing edge SSIDATA output delay		t_{DTRW}	—	105	ns	Figure 51.56

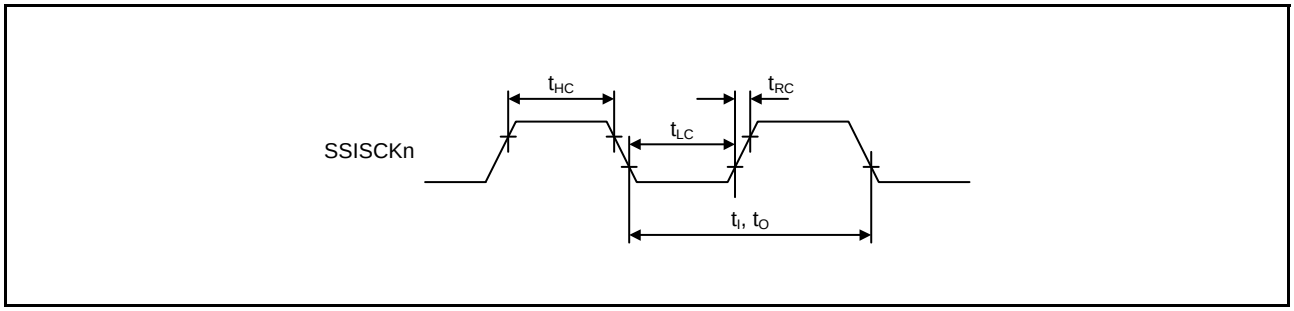


Figure 51.53 SSI Clock Input/Output Timing

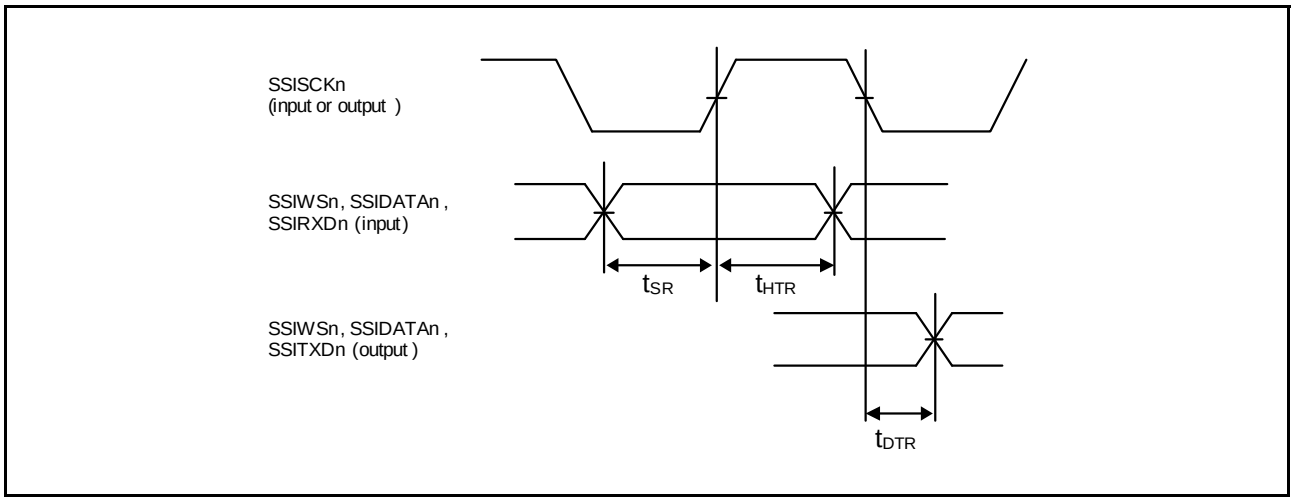


Figure 51.54 SSI Transmission/Reception Timing (SSICR.SCKP = 0)

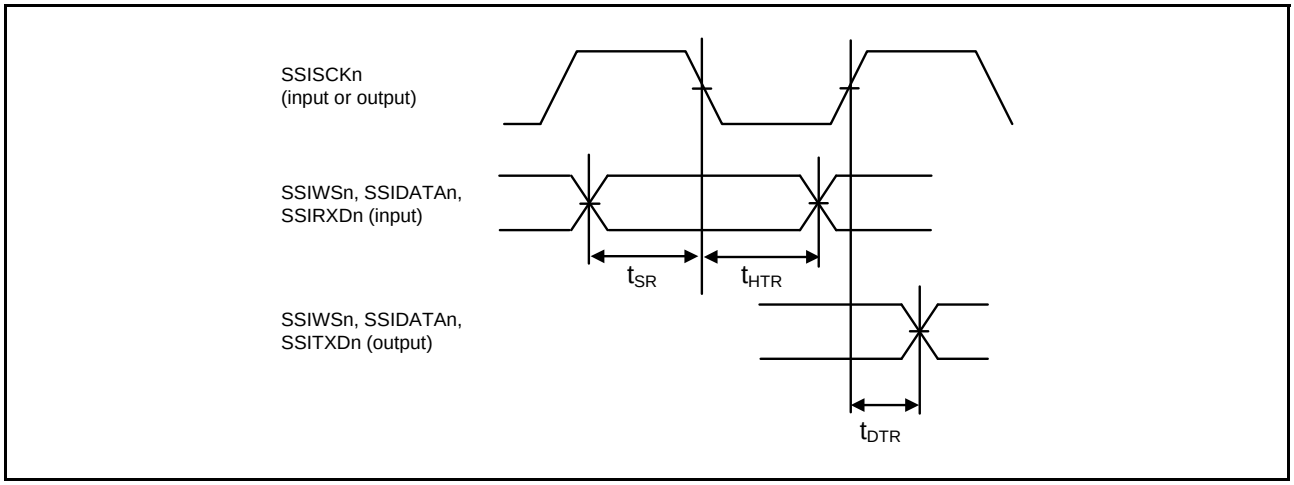
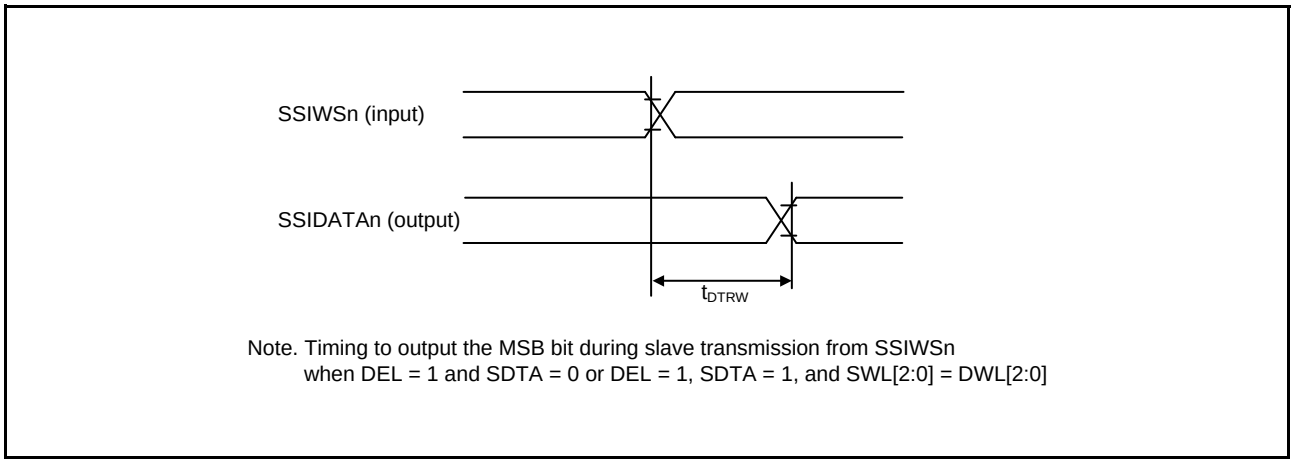


Figure 51.55 SSI Transmission/Reception Timing (SSICR.SCKP = 1)



Note. Timing to output the MSB bit during slave transmission from SSIWSn
when DEL = 1 and SDTA = 0 or DEL = 1, SDTA = 1, and SWL[2:0] = DWL[2:0]

Figure 51.56 SSIDATA Output Delay After SSIWSn Changing Edge

51.3.5.9 Timing of SDHI

Table 51.42 Timing of SDHI

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, fPCLKB ≤ 32 MHz, T_a = –40 to +85°C,
when high-drive output is selected by the drive capacity control register

Item		Symbol	Min.	Max.	Unit	Test Conditions
SDHI	SDHI_CLK pin output cycle time	$t_{PP(SD)}$	62.5	—	ns	Figure 51.57
	SDHI_CLK pin output high pulse width	$t_{WH(SD)}$	18.25	—	ns	
	SDHI_CLK pin output low pulse width	$t_{WL(SD)}$	18.25	—	ns	
	SDHI_CLK pin output rise time	$t_{TLH(SD)}$	—	10	ns	
	SDHI_CLK pin output fall time	$t_{THL(SD)}$	—	10	ns	
	Output data delay time (data transfer mode) for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ODLY(SD)}$	–18.25	18.25	ns	
	Input data setup time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{ISU(SD)}$	9.25	—	ns	
	Input data hold time for SDHI_CMD and SDHI_D0 to SDHI_D3 pins	$t_{IH(SD)}$	8.3	—	ns	

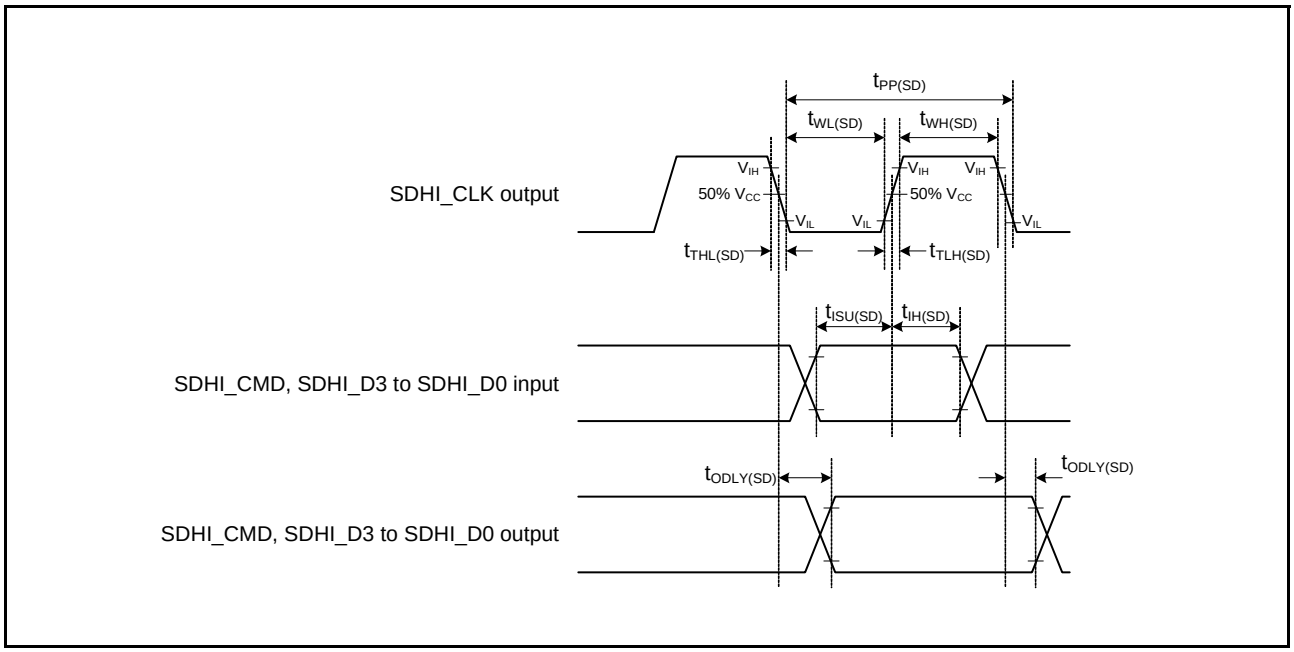


Figure 51.57 SD Host Interface Input/Output Signal Timing

51.3.5.10 Timing of A/D Converter Trigger

Table 51.43 Timing of A/D Converter Trigger

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

Item		Symbol	Min.	Max.	Unit *1	Test Conditions
A/D converter	Trigger input pulse width	t_{TRGW}	1.5	—	t_{Pcyc}	Figure 51.58

Note 1. t_{Pcyc}: PCLK cycle

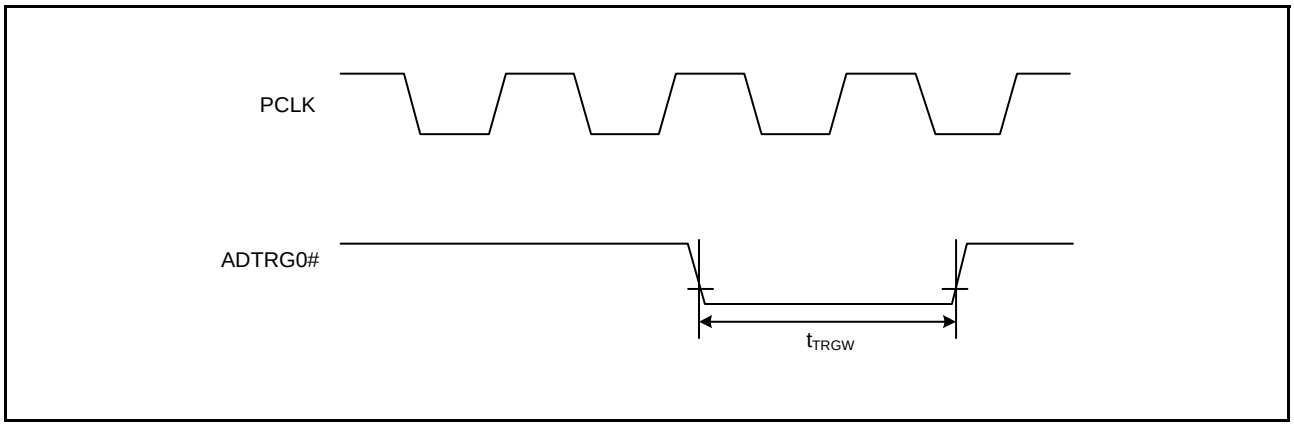


Figure 51.58 A/D Converter External Trigger Input Timing

51.3.5.11 Timing of CAC

Table 51.44 Timing of CAC

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
CAC	CACREF input pulse width	$t_{Pcyc} \le t_{cac}$ *2	t_{CACREF}	4.5 t_{cac} + 3 t_{Pcyc}	—	ns	
		$t_{Pcyc} > t_{cac}$ *2		5 t_{cac} + 6.5 t_{Pcyc}			

Note 1. t_{Pcyc}: PCLK cycle
Note 2. t_{cac}: CAC count clock source cycle

51.3.5.12 Timing of CLKOUT

Table 51.45 Timing of CLKOUT

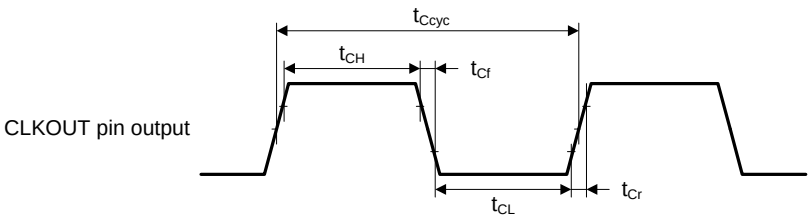
Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item			Symbol	Min.	Max.	Unit *1	Test Conditions
CLKOUT	CLKOUT pin output cycle*3	VCC = 2.7 V or above	t_{Ccyc}	62.5	—	ns	Figure 51.59
		VCC = 1.8 V or above		125			
	CLKOUT pin high pulse width*2	VCC = 2.7 V or above	t_{CH}	15	—	ns	
		VCC = 1.8 V or above		30			
	CLKOUT pin low pulse width*2	VCC = 2.7 V or above	t_{CL}	15	—	ns	
		VCC = 1.8 V or above		30			
	CLKOUT pin output rise time	VCC = 2.7 V or above	t_{Cr}	—	12	ns	
		VCC = 1.8 V or above			25		
	CLKOUT pin output fall time	VCC = 2.7 V or above	t_{Cf}	—	12	ns	
		VCC = 1.8 V or above			25		

Note 1. t_{Pcyc}: PCLK cycle

Note 2. When the LOCO is selected as the clock output source (the CKOCR.CKOSEL[2:0] bits are 000b), set the clock output division ratio selection to divided by 2 (the CKOCR.CKODIV[2:0] bits are 001b).

Note 3. When the EXTAL external clock input or an oscillator is used with divided by 1 (the CKOCR.CKOSEL[2:0] bits are 010b and the CKOCR.CKODIV[2:0] bits are 000b) to output from CLKOUT, the above should be satisfied with an input duty cycle of 45 to 55%.



Test conditions: V_{OH} = VCC × 0.7, V_{OL} = VCC × 0.3, I_{OH} = -1.0 mA, I_{OL} = 1.0 mA, C = 30 pF

Figure 51.59 CLKOUT Output Timing

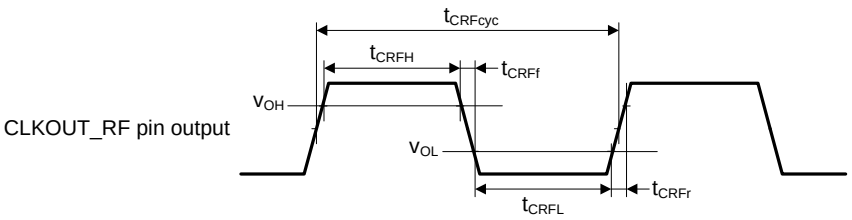
51.3.5.13 Timing of CLKOUT_RF

Table 51.46 Timing of CLKOUT_RF

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Max.	Unit *1	Test Conditions
CLKOUT_RF *2	CLKOUT_RF pin output cycle	t_{CRFcyc}	250	—	ns	Figure 51.60
	CLKOUT_RF pin high pulse width	t_{CRFH}	100	—	ns	
	CLKOUT_RF pin low pulse width	t_{CRFL}	100	—	ns	
	CLKOUT_RF pin output rise time	t_{CRFr}	—	5	ns	
	CLKOUT_RF pin output fall time	t_{CRFf}	—	5	ns	

Note 1. t_{Pcyc}: PCLK cycle
Note 2. The voltage for VCC_RF when CLKOUT_RF pin is to be used is between 3.0 V and 3.6 V.



Test conditions: V_{OH} = VCC_RF × 0.8 , V_{OL} = VCC_RF × 0.2
Note. The voltage for VCC_RF pin when CLKOUT_RF is to be used is between 3.0 V and 3.6 V.

Figure 51.60 CLKOUT_RF Output Timing

51.4 USB Characteristics

Table 51.47 USB Characteristics (USB0_DP and USB0_DM Pin Characteristics)

Conditions: 3.0 V ≤ VCC = VCC_USB = AVCC = VCC_RF = AVCC_RF < 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item			Symbol	Min.	Max.	Unit	Test Conditions	
Input characteristics	Input high level voltage		V_{IH}	2.0	—	V		
	Input low level voltage		V_{IL}	—	0.8	V		
	Differential input sensitivity		V_{DI}	0.2	—	V	| USB0_DP – USB0_DM |	
	Differential common mode range		V_{CM}	0.8	2.5	V		
Output characteristics	Output high level voltage		V_{OH}	2.8	VCC_USB	V	I_{OH} = –200 µA	
	Output low level voltage		V_{OL}	0.0	0.3	V	I_{OL} = 2 mA	
	Cross-over voltage		V_{CRS}	1.3	2.0	V		Figure 51.61, Figure 51.62
	Rise time	FS	t_r	4	20	ns		
		LS		75	300			
	Fall time	FS	t_f	4	20	ns		
		LS		75	300			
	Rise/fall time ratio	FS	t_r/t_f	90	111.11	%	t_r/t_f	
		LS		80	125			
	Output resistance		Z_{DRV}	28	44	Ω	(Adjusting the resistance by external elements is not necessary.)	
VBUS characteristics	VBUS input voltage		V_{IH}	VCC × 0.8	—	V		
			V_{IL}	—	VCC × 0.2	V		
Pull-up, pull-down	Pull-down resistor		R_{PD}	14.25	24.80	kΩ		
	Pull-up resistor		R_{PUI}	0.9	1.575	kΩ	During idle state	
			R_{PUA}	1.425	3.09	kΩ	During reception	
Battery Charging Specification Ver 1.2	D+ sink current		I_{DP_SINK}	25	175	µA		
	D- sink current		I_{DM_SINK}	25	175	µA		
	DCD source current		I_{DP_SRC}	7	13	µA		
	Data detection voltage		V_{DAT_REF}	0.25	0.4	V		
	D+ source current		V_{DP_SRC}	0.5	0.7	V	Output current = 250 µA	
	D- source current		V_{DM_SRC}	0.5	0.7	V	Output current = 250 µA	

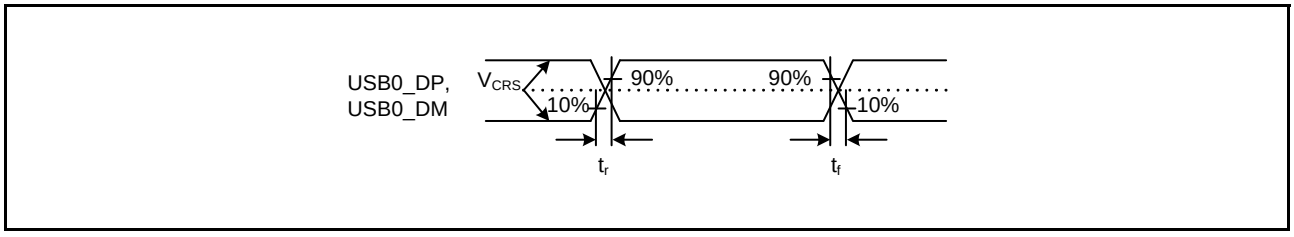


Figure 51.61 USB0_DP and USB0_DM Output Timing

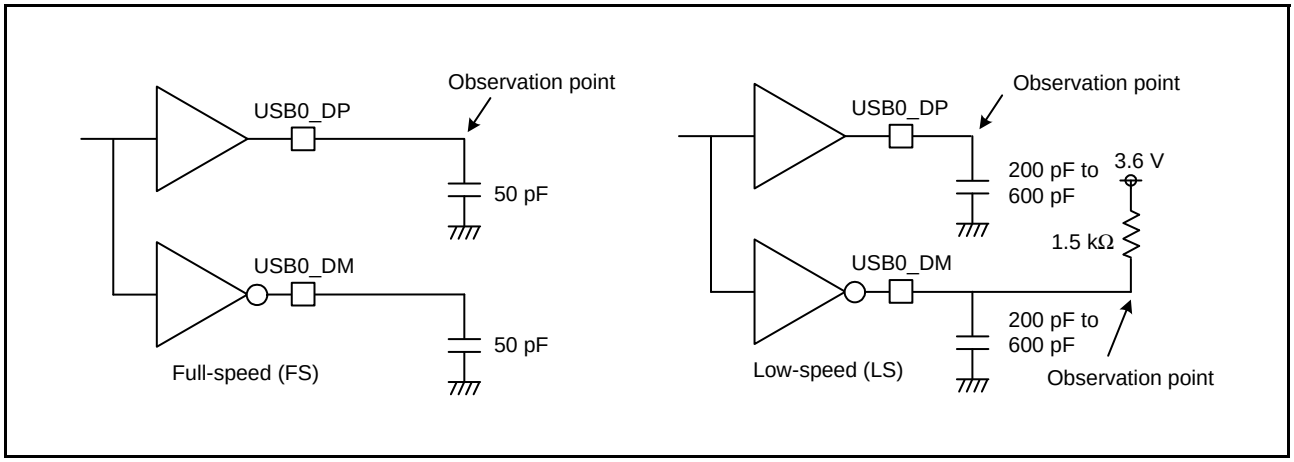


Figure 51.62 Test Circuit

51.5 A/D Conversion Characteristics

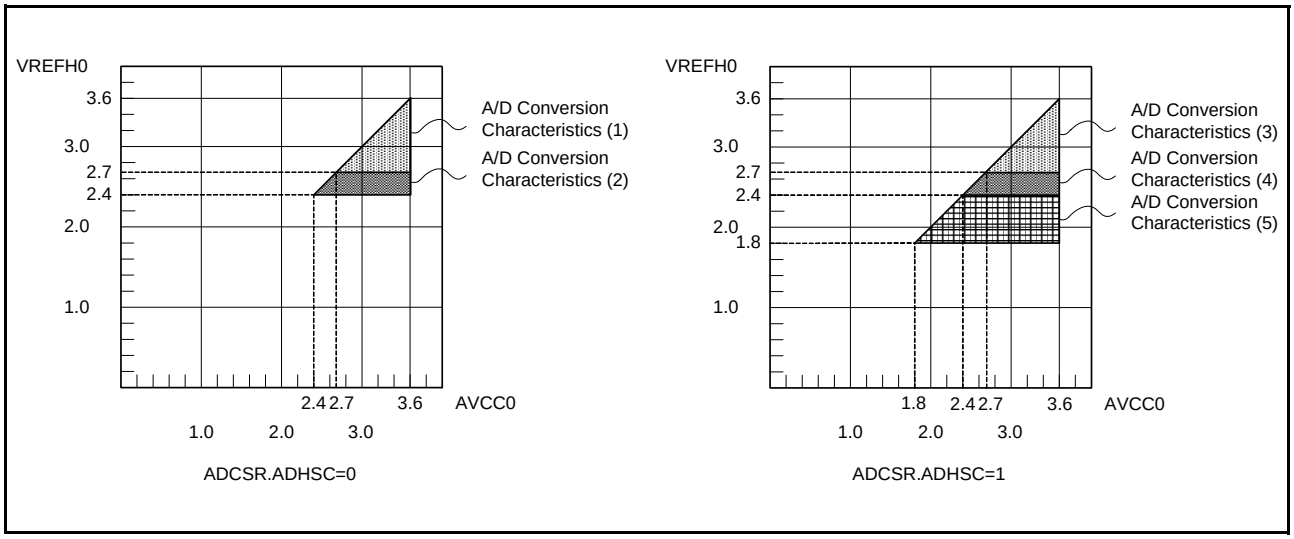


Figure 51.63 VREFH0 Voltage Range vs. AVCC0

Table 51.48 A/D Conversion Characteristics (1)

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0, reference voltage = VREFH0 selected, VSS = AVSS0 = VREFL0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	54	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 54 MHz)	Permissible signal source impedance (Max.) = 0.3 kΩ	0.83	—	—	µs	High-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 0Dh
		1.33	—	—		Normal-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 51.64
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 51.64
Analog input voltage range	Ain	0	—	VREFH0	V	
Offset error		—	±0.5	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Full-scale error		—	±0.75	±4.5	LSB	High-precision channel
				±6.0	LSB	Other than above
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 51.49 A/D Conversion Characteristics (2)

Conditions: 2.4 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, 2.4 V ≤ VREFH0 ≤ AVCC0,
reference voltage = VREFH0 selected, VSS = AVSS0 = VREFL0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	32	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 32 MHz)	Permissible signal source impedance (Max.) = 1.3 kΩ	1.41	—	—	µs	High-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 0Dh
		2.25	—	—		Normal-precision channel The ADCSR.ADHSC bit is 0 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 51.64
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 51.64
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.0	±4.5	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 51.50 A/D Conversion Characteristics (3)

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, 2.7 V ≤ VREFH0 ≤ AVCC0,
reference voltage = VREFH0 selected, VSS = AVSS0 = VREFL0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	27	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 27 MHz)	Permissible signal source impedance (Max.) = 1.1 kΩ	2	—	—	µs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn.SST[7:0] bits are 0Dh
		3	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn.SST[7:0] bits are 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 51.64
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 51.64
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 51.51 A/D Conversion Characteristics (4)

Conditions: 2.4 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, 2.4 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = VSS_USB = 0 V, reference voltage = VREFH0 selected, T_a = –40 to +85°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	16	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 16 MHz)	Permissible signal source impedance (Max.) = 2.2 kΩ	3.38	—	—	µs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 0Dh
		5.06	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 51.64
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 51.64
Offset error		—	±0.5	±4.5	LSB	
Full-scale error		—	±0.75	±4.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±1.25	±5.0	LSB	High-precision channel
				±8.0	LSB	Other than above
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.0	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 51.52 A/D Conversion Characteristics (5)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, 1.8 V ≤ VREFH0 ≤ AVCC0,
VSS = AVSS0 = VSS_USB = 0 V, reference voltage = VREFH0 selected, T_a = –40 to +85°C

Item		Min.	Typ.	Max.	Unit	Test Conditions
Frequency		1	—	8	MHz	
Resolution		—	—	12	Bit	
Conversion time*1 (Operation at PCLKD = 8 MHz)	Permissible signal source impedance (Max.) = 5 kΩ	6.75	—	—	µs	High-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 0Dh
		10.13	—	—		Normal-precision channel The ADCSR.ADHSC bit is 1 The ADSSTRn register is 28h
Analog input capacitance	Cs	—	—	15	pF	Pin capacitance included Figure 51.64
Analog input resistance	Rs	—	—	2.5	kΩ	Figure 51.64
Offset error		—	±1	±7.5	LSB	
Full-scale error		—	±1.5	±7.5	LSB	
Quantization error		—	±0.5	—	LSB	
Absolute accuracy		—	±3.0	±8.0	LSB	
DNL differential non-linearity error		—	±1.0	—	LSB	
INL integral non-linearity error		—	±1.25	±3.0	LSB	

Note: The characteristics apply when no pin functions other than A/D converter input are used. Absolute accuracy includes quantization errors. Offset error, full-scale error, DNL differential non-linearity error, and INL integral non-linearity error do not include quantization errors.

Note 1. The conversion time is the sum of the sampling time and the comparison time. As the test conditions, the number of sampling states is indicated.

Table 51.53 A/D Converter Channel Classification

Classification	Channel	Conditions	Remarks
High-precision channel	AN000 to AN007	AVCC0 = 1.8 to 3.6 V	Pins AN000 to AN007 cannot be used as digital outputs when the A/D converter is in use.
Normal-precision channel	AN016 to AN020, AN027		
Internal reference voltage input channel	Internal reference voltage	AVCC0 = 2.0 to 3.6 V	
Temperature sensor input channel	Temperature sensor output	AVCC0 = 2.0 to 3.6 V	

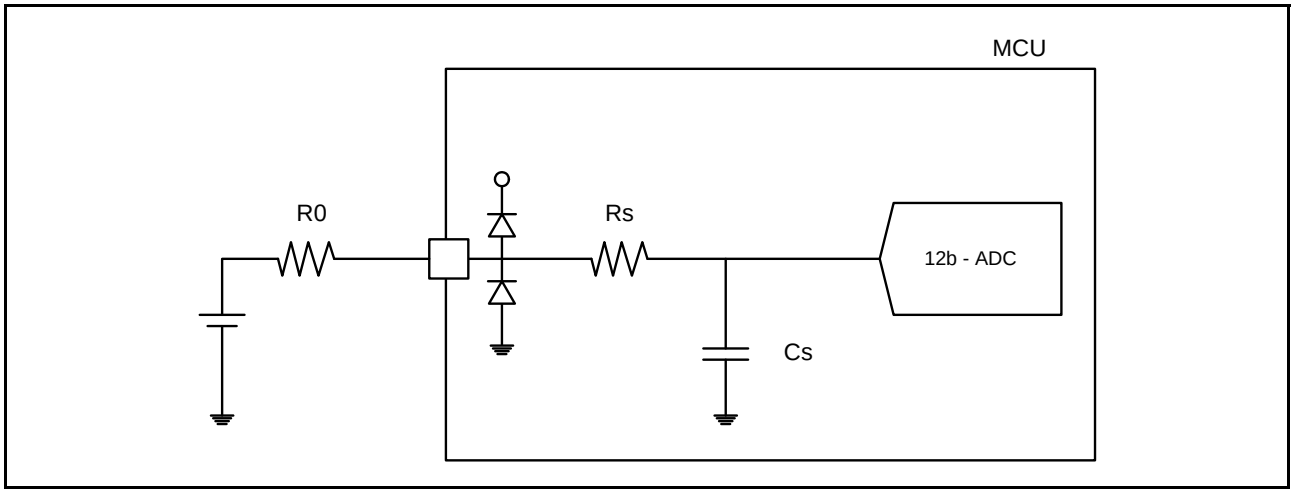


Figure 51.64 Equivalent Circuit

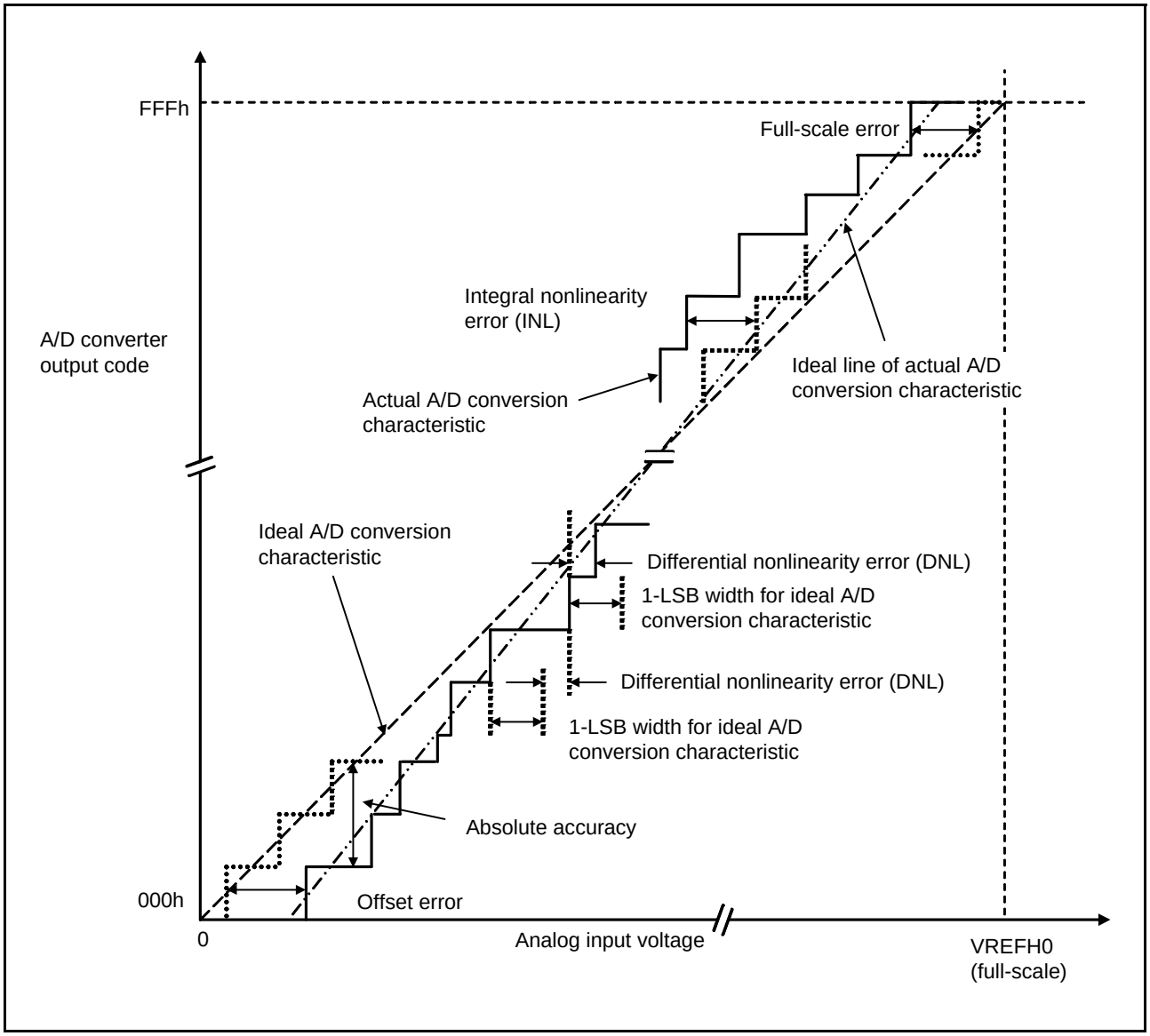


Figure 51.65 Illustration of A/D Converter Characteristic Terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of analog input voltage (1-LSB width), that can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and if reference voltage (VREFH0 = 3.072 V), then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, 1.5 mV, ... are used as analog input voltages.

If analog input voltage is 6 mV, absolute accuracy = ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, although an output code, 008h, can be expected from the theoretical A/D conversion characteristics.

Integral non-linearity error (INL)

The integral non-linearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential non-linearity error (DNL)

The differential non-linearity error is the difference between 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Offset error

An offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

A full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

51.6 D/A Conversion Characteristics

Table 51.54 D/A Conversion Characteristics (1)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C, Reference voltage = AVCC0 or AVSS0 selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Resistive load	30	—	—	kΩ	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	AVCC0 - 0.47	V	
DNL differential non-linearity error	—	±0.5	±2.0	LSB	
INL integral non-linearity error	—	±2.0	±8.0	LSB	
Offset error	—	—	±30	mV	
Full-scale error	—	—	±30	mV	
Output resistance	—	5	—	Ω	
Conversion time	—	—	30	µs	

Table 51.55 D/A Conversion Characteristics (2)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C, Reference voltage = internal reference voltage selected

Item	Min.	Typ.	Max.	Unit	Test Conditions
Resolution	—	—	12	Bit	
Internal reference voltage (Vbgr)	1.36	1.43	1.50	V	
Resistive load	30	—	—	kΩ	
Capacitive load	—	—	50	pF	
Output voltage range	0.35	—	Vbgr	V	
DNL differential non-linearity error	—	±2.0	±16.0	LSB	
INL integral non-linearity error	—	±8.0	±16.0	LSB	
Offset error	—	—	30	mV	
Output resistance	—	5	—	Ω	
Conversion time	—	—	30	µs	

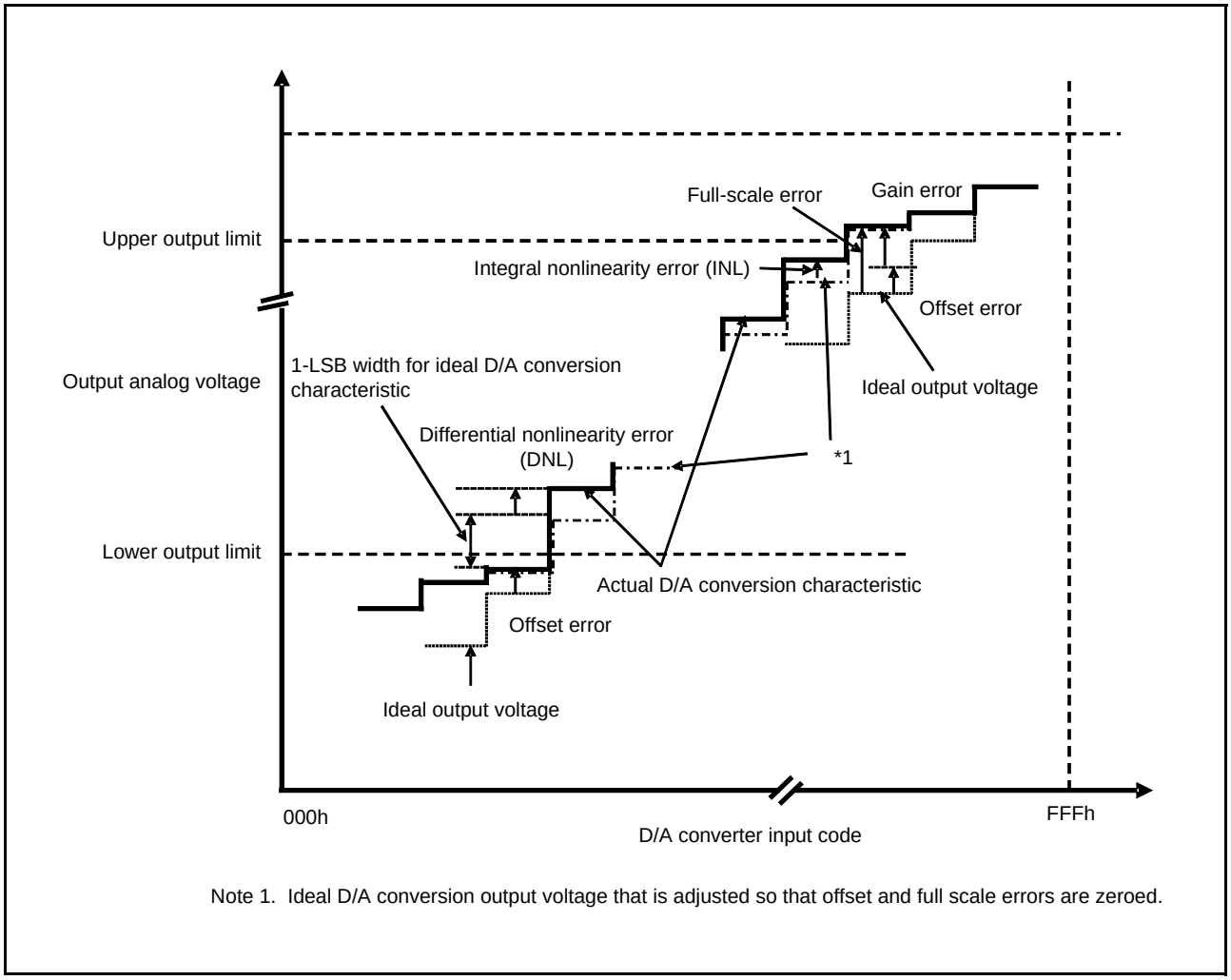


Figure 51.66 Illustration of D/A Converter Characteristic Terms

Integral non-linearity error (INL)

The integral non-linearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential non-linearity error (DNL)

The differential non-linearity error is the difference between 1-LSB width based on the ideal D/A conversion characteristics and the width of the actually output code.

Offset error

An offset error is the difference between a transition point of the ideal first output code and the actual first output code.

Full-scale error

A full-scale error is the difference between a transition point of the ideal last output code and the actual last output code.

51.7 Temperature Sensor Characteristics

Table 51.56 Temperature Sensor Characteristics

Conditions: 2.0 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Relative accuracy	—	—	±1.5	—	°C	2.4 V or above
		—	±2.0	—		Below 2.4 V
Temperature slope	—	—	–3.65	—	mV/°C	
Output voltage (25°C)	—	—	1.05	—	V	VCC = 3.3 V
Temperature sensor start time	t_{START}	—	—	5	µs	
Sampling time	—	5	—	—	µs	

51.8 Comparator Characteristics

Table 51.57 Comparator Characteristics

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V,
T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
CVREFB2, CVREFB3 input reference voltage		VREF	0	—	VCC - 1.4	V	
CMPB2, CMPB3 input voltage		VI	–0.3	—	VCC + 0.3	V	
Offset	Comparator high-speed mode	—	—	—	50	mV	
	Comparator high-speed mode Window function enabled	—	—	—	60	mV	
	Comparator low-speed mode	—	—	—	40	mV	
Comparator output delay time	Comparator high-speed mode	Td	—	—	1.2	µs	VCC = 3 V, input slew rate ≥ 50 mV/µs
	Comparator high-speed mode Window function enabled	Tdw	—	—	2.0	µs	
	Comparator low-speed mode	Td	—	—	5.0	µs	
High-side reference voltage (comparator high-speed mode, window function enabled)		VRFH	—	0.76 VCC	—	V	
Low-side reference voltage (comparator high-speed mode, window function enabled)		VRFL	—	0.24 VCC	—	V	
Operation stabilization wait time		Tcmp	100	—	—	µs	

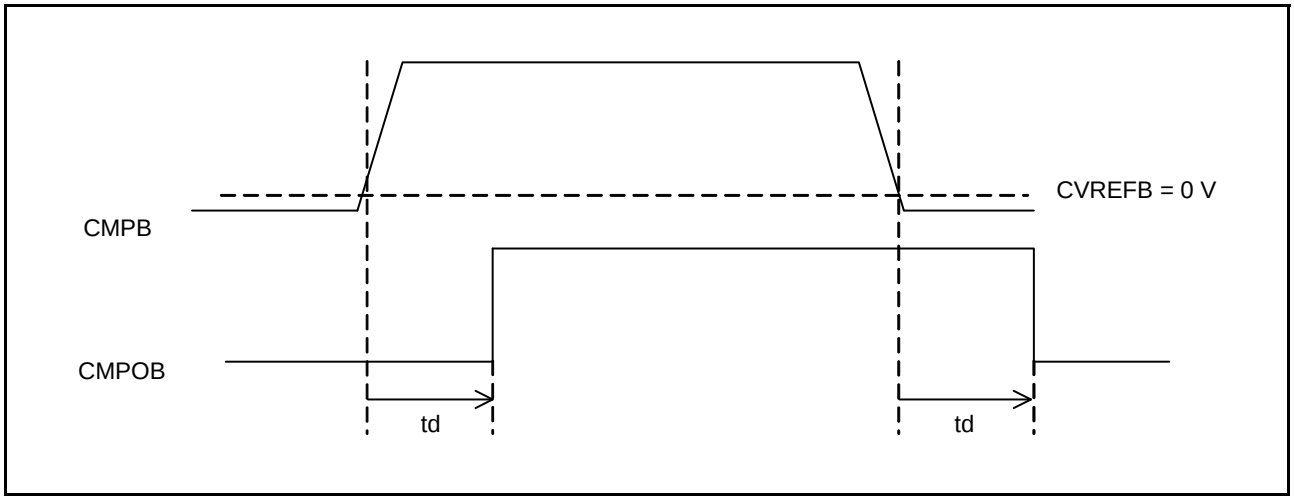


Figure 51.67 Comparator Output Delay Time in Comparator High-Speed Mode and Low-Speed Mode

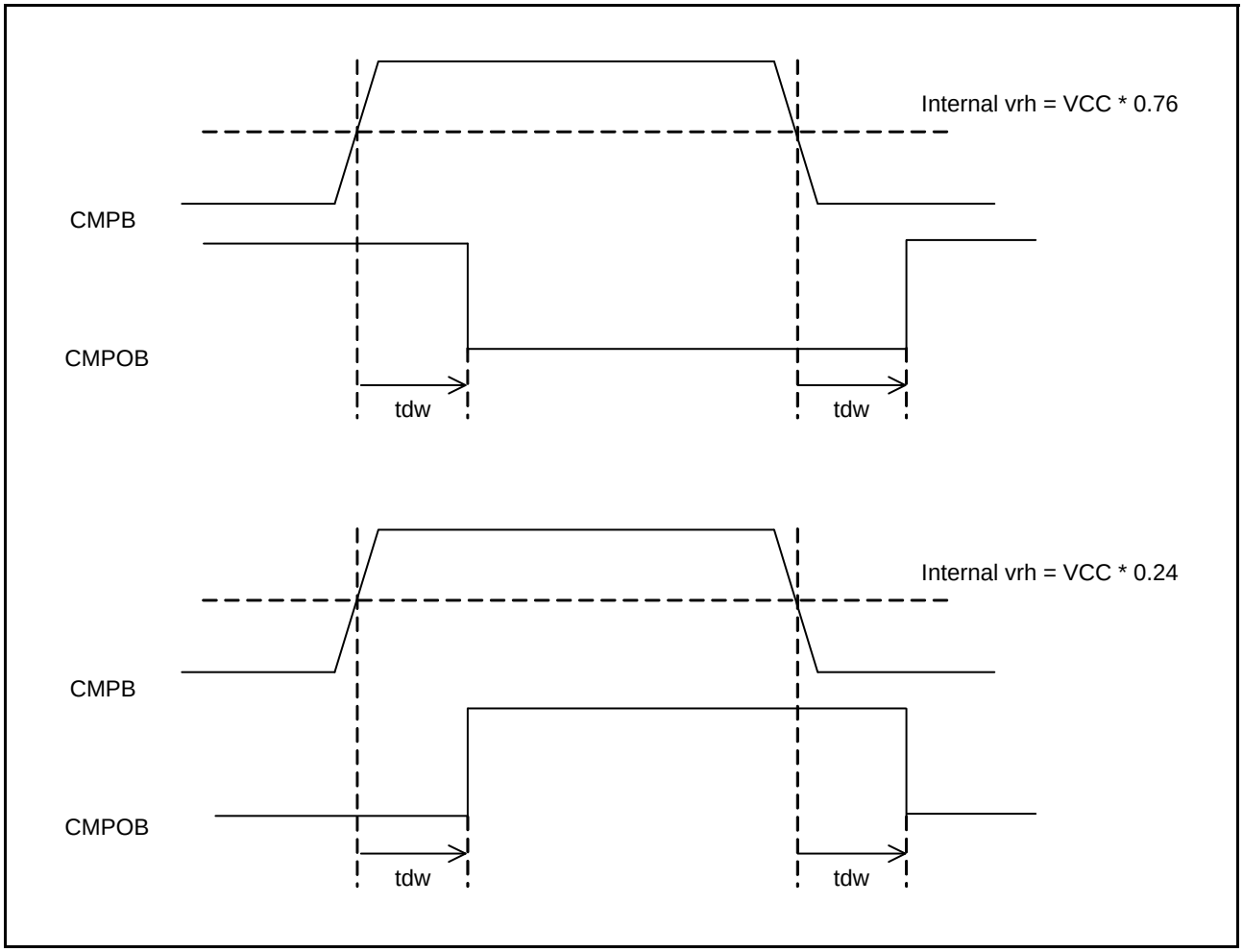


Figure 51.68 Comparator Output Delay Time in High-Speed Mode with Window Function Enabled

51.9 CTSU Characteristics

Table 51.58 CTSU Characteristics

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	
TS pin capacitive load	C_{base}	—	—	50	pF	
Permissible output high current	ΣI_{OH}	—	—	–24	mA	When the mutual capacitance method is applied

51.10 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit

Table 51.59 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (1)

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage detection level	Power-on reset (POR)	V_{POR}	1.35	1.50	1.65	V	Figure 51.69, Figure 51.70
	Voltage detection circuit (LVD0)*1	V_{det0_1}	2.70	2.82	3.00	V	Figure 51.71 At falling edge VCC
		V_{det0_2}	2.37	2.51	2.67		
		V_{det0_3}	1.80	1.90	1.99		
	Voltage detection circuit (LVD1)*2	V_{det1_4}	2.99	3.10	3.29	V	Figure 51.72 At falling edge VCC
		V_{det1_5}	2.89	3.00	3.19		
		V_{det1_6}	2.79	2.90	3.09		
		V_{det1_7}	2.68	2.79	2.98		
		V_{det1_8}	2.57	2.68	2.87		
		V_{det1_9}	2.47	2.58	2.67		
		V_{det1_A}	2.37	2.48	2.57		
		V_{det1_B}	2.10	2.20	2.30		
		V_{det1_C}	1.86	1.96	2.06		
		V_{det1_D}	1.80	1.86	1.96		

Note: These characteristics apply when noise is not superimposed on the power supply.
Note 1. n in the symbol Vdet0_n denotes the value of the OFS1.VDSEL[1:0] bits.
Note 2. n in the symbol Vdet1_n denotes the value of the LVDLVLR.LVD1LVL[3:0] bits.

Table 51.60 Characteristics of Power-On Reset Circuit and Voltage Detection Circuit (2)

Conditions: 1.8 V ≤ VCC0 = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Wait time after power-on reset cancellation	At normal startup*1	t_{POR}	—	9.1	—	ms	Figure 51.70
	During fast startup time*2	t_{POR}	—	1.6	—		
Wait time after voltage monitoring 0 reset cancellation	Power-on voltage monitoring 0 reset disabled*1	t_{LVD0}	—	568	—	µs	Figure 51.71
	Power-on voltage monitoring 0 reset enabled*2		—	100	—		
Wait time after voltage monitoring 1 reset cancellation		t_{LVD1}	—	100	—	µs	Figure 51.72
Response delay time		t_{det}	—	—	350	µs	Figure 51.69
Minimum VCC down time*3		t_{VOFF}	350	—	—	µs	Figure 51.69, VCC = 1.0 V or above
Power-on reset enable time		$t_{W(POR)}$	1	—	—	ms	Figure 51.70, VCC = below 1.0 V
LVD operation stabilization time (after LVD is enabled)		$Td_{(E-A)}$	—	—	300	µs	Figure 51.72
Hysteresis width (power-on rest (POR))		V_{PORH}	—	110	—	mV	
Hysteresis width (voltage detection circuit: LVD1)		V_{LVH}	—	70	—	mV	When Vdet1_4 is selected
			—	60	—		When Vdet1_5 to Vdet1_9 is selected
			—	50	—		When Vdet1_A or Vdet1_B is selected
			—	40	—		When Vdet1_C or Vdet1_D is selected

Note: These characteristics apply when noise is not superimposed on the power supply.
Note 1. When OFS1.(LVDAS, FASTSTUP) = 11b.
Note 2. When OFS1.(LVDAS, FASTSTUP) ≠ 11b.
Note 3. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det0}, and V_{det1} for the POR/LVD.

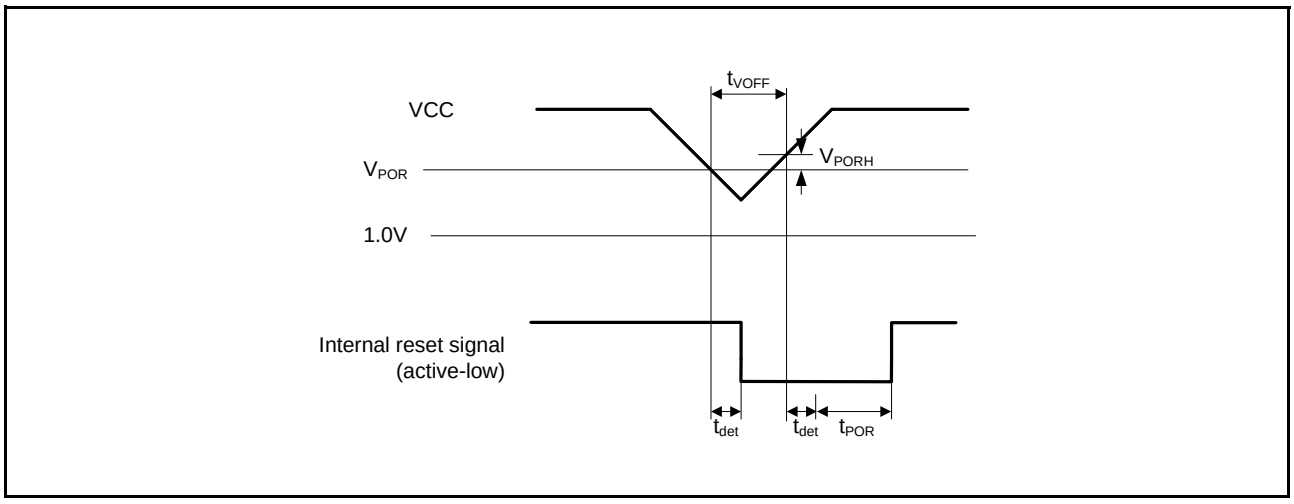
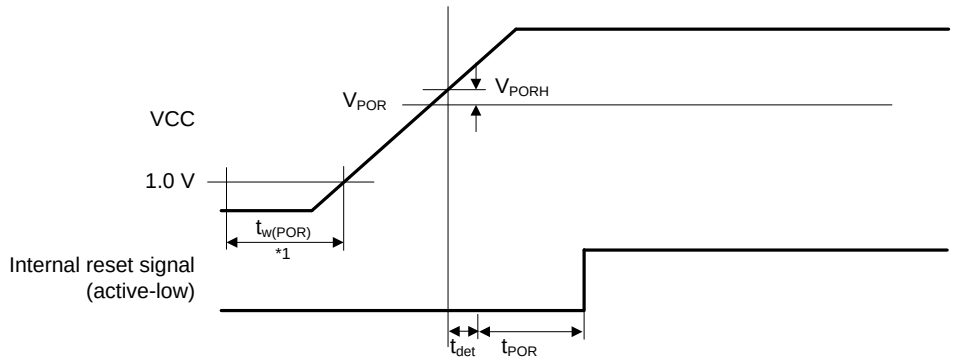


Figure 51.69 Voltage Detection Reset Timing



Note 1. $t_{w(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When turning the VCC on, maintain a voltage below 1.0V for at least 1.0ms.

Figure 51.70 Power-On Reset Timing

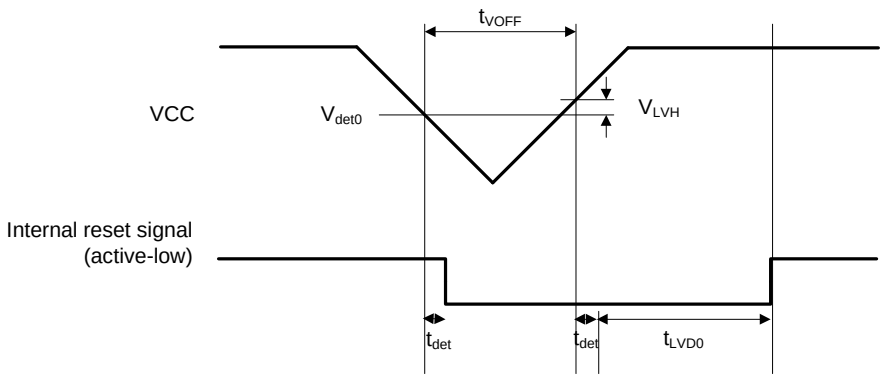


Figure 51.71 Voltage Detection Circuit Timing (Vdet0)

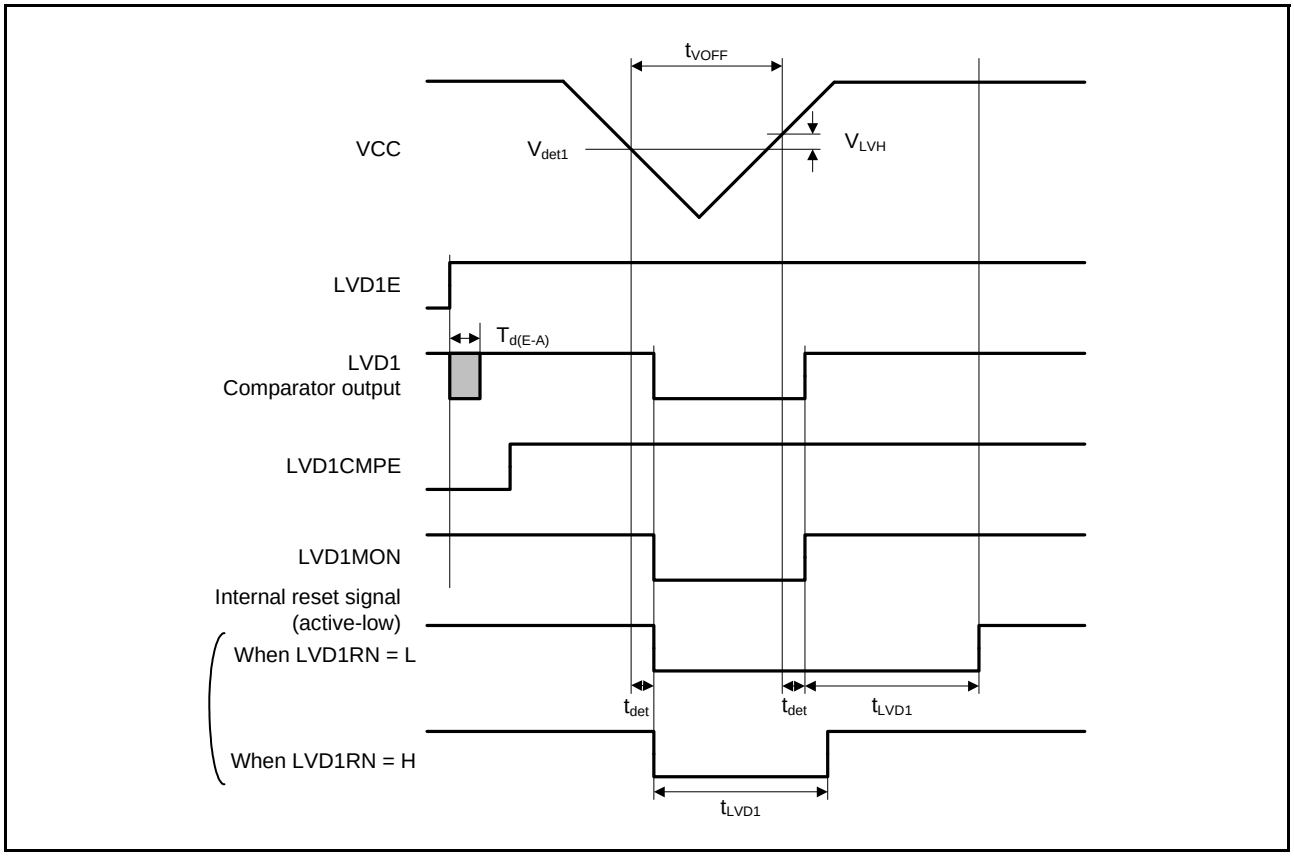


Figure 51.72 Voltage Detection Circuit Timing (V_{det1})

51.11 Oscillation Stop Detection Timing

Table 51.61 Oscillation Stop Detection Timing

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V,
VSS = AVSS0 = VREFL0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Detection time	t_{dr}	—	—	1	ms	Figure 51.73

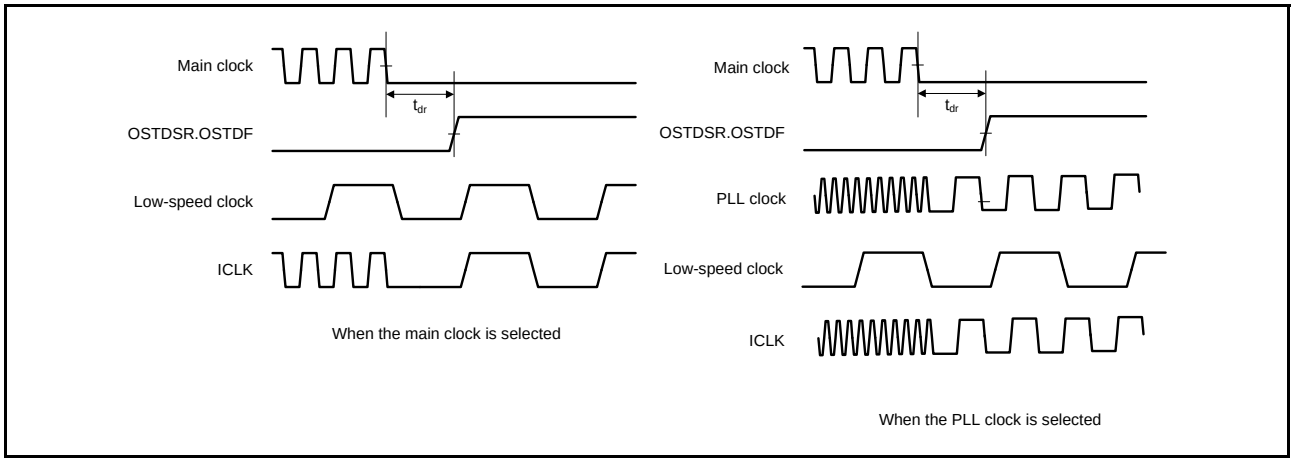


Figure 51.73 Oscillation Stop Detection Timing

51.12 Battery Backup Function Characteristics

Table 51.62 Battery Backup Function Characteristics

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, 1.8 V ≤ VBATT ≤ 3.6 V,
VSS = AVSS0 = VREFL0 = VSS_USB = VSS_RF = 0 V, T_a = –40 to +85°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Voltage level for switching to battery backup (falling)		$V_{DETBATT}$	1.99	2.09	2.19	V	Figure 51.74
Hysteresis width		V_{VBATTH}	—	100	—	mV	
VCC-off period for starting power supply switching		$t_{VOFFBATT}$	—	—	350	µs	
Allowable voltage change rising/falling gradient		dt/dVCC	1.0	—	—	ms/V	Figure 51.7
Level for detection of voltage drop on the VBATT pin (falling)	VBTLVDLVL[1:0] = 10b	$V_{DETBATLVD}$	2.11	2.20	2.29	V	Figure 51.74
	VBTLVDLVL[1:0] = 11b		1.87	2.00	2.13	V	
Hysteresis width for detection of voltage drop on the VBATT pin		$V_{BATLVDH}$	—	50	—	mV	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

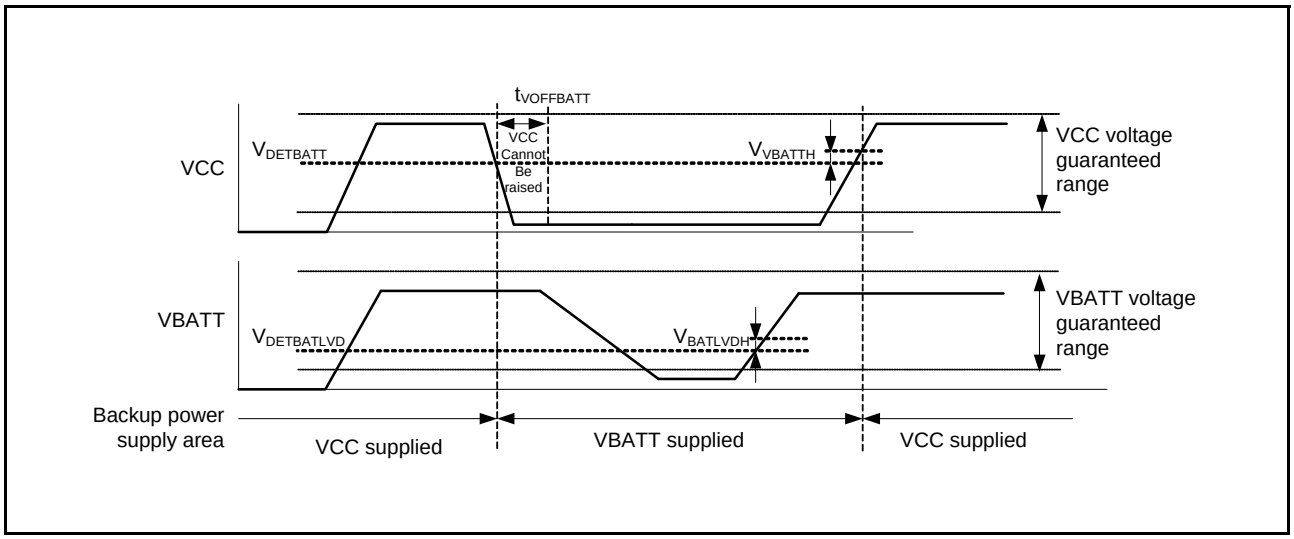


Figure 51.74 Battery Backup Function Characteristics

51.13 ROM (Flash Memory for Code Storage) Characteristics

Table 51.63 ROM (Flash Memory for Code Storage) Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogramming/erasure cycle*1		N_{PEC}	1000	—	—	Times	
Data hold time	After 1000 times of N_{PEC}	t_{DRP}	20*2, *3	—	—	Year	T_a = +85°C

Note 1. Definition of reprogram/erase cycle: The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 1000), erasing can be performed n times for each block. For instance, when 4-byte programming is performed 256 times for different addresses in a 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when using the flash memory programmer and the self-programming library provided from Renesas Electronics.
Note 3. This result is obtained from reliability testing.

Table 51.64 ROM (Flash Memory for Code Storage) Characteristics (2) High-Speed Operating Mode

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	112	967	—	52.3	491	µs
Erasure time	2-Kbyte	t_{E2K}	—	8.75	278	—	5.50	215	ms
	512-Kbyte (when block erase command is used)	t_{E512K}	—	928	19218	—	72.0	1679	ms
	512-Kbyte (when all-block erase command is used)	t_{EA512K}	—	923	19013	—	66.7	1469	ms
Blank check time	8-byte	t_{BC8}	—	—	55.0	—	—	16.1	µs
	2-Kbyte	t_{BC2K}	—	—	1840	—	—	136	ms
Erase operation forced stop time		t_{SED}	—	—	18.0	—	—	10.7	µs
Start-up area switching setting time		t_{SAS}	—	12.3	566.5	—	6.2	434	ms
Access window time		t_{AWS}	—	12.3	566.5	—	6.2	434	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	µs
ROM mode transition wait time 2		t_{MS}	5.0	—	—	5.0	—	—	µs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be within ±3.5%.

Table 51.65 ROM (Flash Memory for Code Storage) Characteristics (3) Middle-Speed Operating Mode

Conditions: 1.8 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB= VSS_RF = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	8-byte	t_{P8}	—	152	1367	—	97.9	936	µs
Erasure time	2-Kbyte	t_{E2K}	—	8.8	279.7	—	5.9	221	ms
	512-Kbyte (when block erase command is used)	t_{E512K}	—	928	19221	—	191	4108	ms
	512-Kbyte (when all-block erase command is used)	t_{EA512K}	—	923	19015	—	185	3901	ms
Blank check time	8-byte	t_{BC8}	—	—	85.0	—	—	50.88	µs
	2-Kbyte	t_{BC2K}	—	—	1870	—	—	402	µs
Erase operation forced stop time		t_{SED}	—	—	28.0	—	—	21.3	µs
Start-up area switching setting time		t_{SAS}	—	13.0	573.3	—	7.7	451	ms
Access window time		t_{AWS}	—	13.0	573.3	—	7.7	451	ms
ROM mode transition wait time 1		t_{DIS}	2.0	—	—	2.0	—	—	µs
ROM mode transition wait time 2		t_{MS}	3.0	—	—	3.0	—	—	µs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be within ±3.5%.

51.14 E2 DataFlash Characteristics (Flash Memory for Data Storage)

Table 51.66 E2 DataFlash Characteristics (1)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reprogramming/erasure cycle*1		N_{DPEC}	100000	1000000	—	Times	
Data hold time	After 10000 times of N_{DPEC}	t_{DDRP}	20*2, *3	—	—	Year	T_a = +85°C
	After 100000 times of N_{DPEC}		5*2, *3	—	—	Year	
	After 1000000 times of N_{DPEC}		—	1*2, *3	—	Year	T_a = +25°C

Note 1. The reprogram/erase cycle is the number of erasing for each block. When the reprogram/erase cycle is n times (n = 100000), erasing can be performed n times for each block. For instance, when 1-byte programming is performed 1000 times for different addresses in a 1-Kbyte block and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address for several times as one erasing is not enabled (overwriting is prohibited).
Note 2. Characteristic when the flash memory programmer is used and the self-programming library is provided from Renesas Electronics.
Note 3. These results are obtained from reliability testing.

Table 51.67 E2 DataFlash Characteristics (2): high-speed operating mode

Conditions: 2.7 V ≤ VCC = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	t_{DP1}	—	95.0	797	—	40.8	376	µs
Erasure time	1 Kbyte	t_{DE1K}	—	19.5	498	—	6.2	230	ms
	8 Kbyte	t_{DE8K}	—	119.8	2556	—	12.9	368	ms
Blank check time	1 byte	t_{DBC1}	—	—	55.00	—	—	16.1	µs
	1 Kbyte	t_{DBC1K}	—	—	0.72	—	—	0.50	ms
Erase operation forced stop time		t_{DSED}	—	—	16.0	—	—	10.7	µs
DataFlash STOP recovery time		t_{DSTOP}	5.0	—	—	5.0	—	—	µs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be within ±3.5%.

Table 51.68 E2 DataFlash Characteristics (3): middle-speed operating mode

Conditions: 1.8 V ≤ VCC0 = VCC_USB = AVCC0 = VCC_RF = AVCC_RF ≤ 3.6 V, VSS = AVSS0 = VSS_USB = VSS_RF = 0 V
Temperature range for the programming/erasure operation: T_a = –40 to +85°C

Item		Symbol	FCLK = 1 MHz			FCLK = 8 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	t_{DP1}	—	135	1197	—	86.5	823	µs
Erasure time	1 Kbyte	t_{DE1K}	—	19.6	501	—	8.0	265	ms
	8 Kbyte	t_{DE8K}	—	120	2558	—	27.7	669	ms
Blank check time	1 byte	t_{DBC1}	—	—	85.0	—	—	50.9	µs
	1 Kbyte	t_{DBC1K}	—	—	0.72	—	—	1.45	ms
Erase operation forced stop time		t_{DSED}	—	—	28.0	—	—	21.3	µs
DataFlash STOP recovery time		t_{DSTOP}	0.72	—	—	0.72	—	—	µs

Note: The time until each operation of the flash memory is started after instructions are executed by software is not included.
Note: The lower-limit frequency of FCLK is 1 MHz during programming or erasing of the flash memory. When using FCLK at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note: The frequency accuracy of FCLK must be within ±3.5%.

51.15 BLE Characteristics

51.15.1 Transmission Characteristics

Table 51.69 Transmission Characteristics

Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Range of frequency		RF_{CF}	2402	—	2480	MHz	
Data rate		RF_{DATA_2M}	—	2	—	Mbps	
		RF_{DATA_1M}	—	1	—	Mbps	
		RF_{DATA_500k}	—	500	—	kbps	
		RF_{DATA_125k}	—	125	—	kbps	
Maximum transmitted output power		RF_{POWER}	—	0	2	dBm	0 dBm output mode
			—	4	6	dBm	4 dBm output mode
Output frequency error	85-pin BGA, 56-pin QFN	RF_{TXFERR}	–10	—	10	ppm	*1
	83-pin LGA	$RF_{MTXFERR}$	–50	—	50	ppm	T_a: –40 to +85°C

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. This does not take frequency errors due to manufacturing irregularities, drift with temperature, or deterioration of the crystal over time into account.

51.15.2 Reception Characteristics (2 Mbps)

Table 51.70 Reception Characteristics

Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Input frequency	RF_{RXFIN_2M}	2402	—	2480	MHz		
Maximum input level	RF_{LEVL_2M}	–10	4	—	dBm	*1	
Receiver sensitivity	RF_{STY_2M}	—	–92	—	dBm	*1	
Secondary emission strength	RF_{RXSP_2M}	—	–72	–57	dBm	30 MHz to 1 GHz	
		—	–54	–47	dBm	1 GHz to 12 GHz	
Co-channel rejection ratio	RF_{CCR_2M}	—	–8	—	dB	Prf = –67 dBm*1	
Adjacent channel rejection ratio	RF_{ADCR_2M}	—	2	—	dB	Prf = –67 dBm*1	±2 MHz
		—	35	—	dB		±4 MHz
		—	39	—	dB		±6 MHz
Blocking	RF_{BLK_2M}	—	–1	—	dBm	Prf = –67 dBm*1	30 MHz to 2000 MHz
		—	–25	—	dBm		2000 MHz to 2399 MHz
		—	–21	—	dBm		2484 MHz to 3000 MHz
		—	–10	—	dBm		> 3000 MHz
Allowable frequency deviation*2	RF_{RXFER_2M}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_2M}	—	±4	—	dB	–70 dBm ≤ Prf ≤ –10 dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. PER ≤ 30.8%, and a 37-byte payload
Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

51.15.3 Reception Characteristics (1 Mbps)

Table 51.71 Reception Characteristics

Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Input frequency	RF_{RXFIN_1M}	2402	—	2480	MHz		
Maximum input level	RF_{LEVL_1M}	–10	4	—	dBm	*1	
Receiver sensitivity	RF_{STY_1M}	—	–95	—	dBm	*1	
Secondary emission strength	RF_{RXSP_1M}	—	–72	–57	dBm	30MHz to 1GHz	
		—	–54	–47	dBm	1GHz to 12GHz	
Co-channel rejection ratio	RF_{CCR_1M}	—	–7	—	dB	Prf = –67dBm*1	
Adjacent channel rejection ratio	RF_{ADCR_1M}	—	–1	—	dB	Prf = –67dBm*1	±1MHz
		—	34	—	dB		±2MHz
		—	35	—	dB		±3MHz
Blocking	RF_{BLK_1M}	—	0	—	dBm	Prf = –67dBm*1	30MHz to 2000MHz
		—	–24	—	dBm		2000MHz to 2399MHz
		—	–20	—	dBm		2484MHz to 3000MHz
		—	–4	—	dBm		> 3000MHz
Allowable frequency deviation*2	RF_{RXFER_1M}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_1M}	—	±4	—	dB	–70dBm ≤ Prf ≤ –10dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. PER ≤ 30.8%, and a 37-byte payload
Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

51.15.4 Reception Characteristics (500 kbps)

Table 51.72 Reception Characteristics

Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Input frequency	RF_{RXFIN_500k}	2402	—	2480	MHz		
Maximum input level	RF_{LEVL_500k}	–10	4	—	dBm	*1	
Receiver sensitivity	RF_{STY_500k}	—	–100	—	dBm	*1	
Secondary emission strength	RF_{RXSP_500k}	—	–72	–57	dBm	30MHz to 1GHz	
		—	–54	–47	dBm	1GHz to 12GHz	
Co-channel rejection ratio	RF_{CCR_500k}	—	–4	—	dB	Prf = –72dBm*1	
Adjacent channel rejection ratio	RF_{ADCR_500k}	—	6	—	dB	Prf = –72dBm*1	±1MHz
		—	36	—	dB		±2MHz
		—	42	—	dB		±3MHz
Blocking	RF_{BLK_500k}	—	0	—	dBm	Prf = –72dBm*1	30MHz to 2000MHz
		—	–23	—	dBm		2000MHz to 2399MHz
		—	–20	—	dBm		2484MHz to 3000MHz
		—	–7	—	dBm		> 3000MHz
Allowable frequency deviation*2	RF_{RXFER_500k}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_500k}	—	±4	—	dB	–70dBm ≤ Prf ≤ –10dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. PER ≤ 30.8%, and a 37-byte payload
Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

51.15.5 Reception Characteristics (125 kbps)

Table 51.73 Reception Characteristics

Conditions: VCC = VCC_RF = AVCC_RF = 3.3 V, VSS = VSS_RF = 0 V, T_a = +25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Input frequency	RF_{RXFIN_125k}	2402	—	2480	MHz		
Maximum input level	RF_{LEVL_125k}	–10	4	—	dBm	*1	
Receiver sensitivity	RF_{STY_125k}	—	–105	—	dBm	*1	
Secondary emission strength	RF_{RXSP_125k}	—	–72	–57	dBm	30 MHz to 1 GHz	
		—	–54	–47	dBm	1 GHz to 12 GHz	
Co-channel rejection ratio	RF_{CCR_125k}	—	–2	—	dB	Prf = –79 dBm*1	
Adjacent channel rejection ratio	RF_{ADCR_125k}	—	12	—	dB	Prf = –79 dBm*1	±1 MHz
		—	39	—	dB		±2 MHz
		—	45	—	dB		±3 MHz
Blocking	RF_{BLK_125k}	—	0	—	dBm	Prf = –79 dBm*1	30 MHz to 2000 MHz
		—	–23	—	dBm		2000 MHz to 2399 MHz
		—	–20	—	dBm		2484 MHz to 3000 MHz
		—	–1	—	dBm		> 3000MHz
Allowable frequency deviation*2	RF_{RXFER_125k}	–120	—	120	ppm	*1	
RSSI accuracy	RF_{RSSIS_125k}	—	±4	—	dB	–70 dBm ≤ Prf ≤ –10 dBm	

Note: The characteristics are based on pins and functions other than those for the BLE interface not being in use.
Note 1. PER ≤ 30.8%, and a 37-byte payload
Note 2. Allowable range of difference between the center frequency for the RF input signals and the carrier frequency generated within the chip

51.16 Usage Notes

51.16.1 Connecting VCL Capacitor and Bypass Capacitors

This MCU integrates an internal voltage-down circuit, which is used for lowering the power supply voltage in the internal MCU automatically to the optimum level. A 4.7-µF capacitor needs to be connected between this internal voltage-down power supply (VCL pin) and the VSS pin. Place an external capacitor close to the pins. Do not apply the power supply voltage to the VCL pin.

Insert a multilayer ceramic capacitor as a bypass capacitor between each pair of the power supply pins. Implement a bypass capacitor as closer to the MCU power supply pins as possible. We recommend capacitors with a value of 2.2 µF for that connected to the VCC_RF pin and 0.1 µF for the others. For the capacitors related to crystal oscillation, see section 9, Clock Generation Circuit. For the capacitors related to analog modules, also see section 44, 12-Bit A/D Converter (S12ADE).

For notes on designing the printed circuit board, see the descriptions of the application note, the Hardware Design Guide (R01AN1411EJ). The latest version can be downloaded from the Renesas Electronics website.

Appendix 1. Port States in Each Processing Mode

Table 1.1 Port States in Each Processing Mode

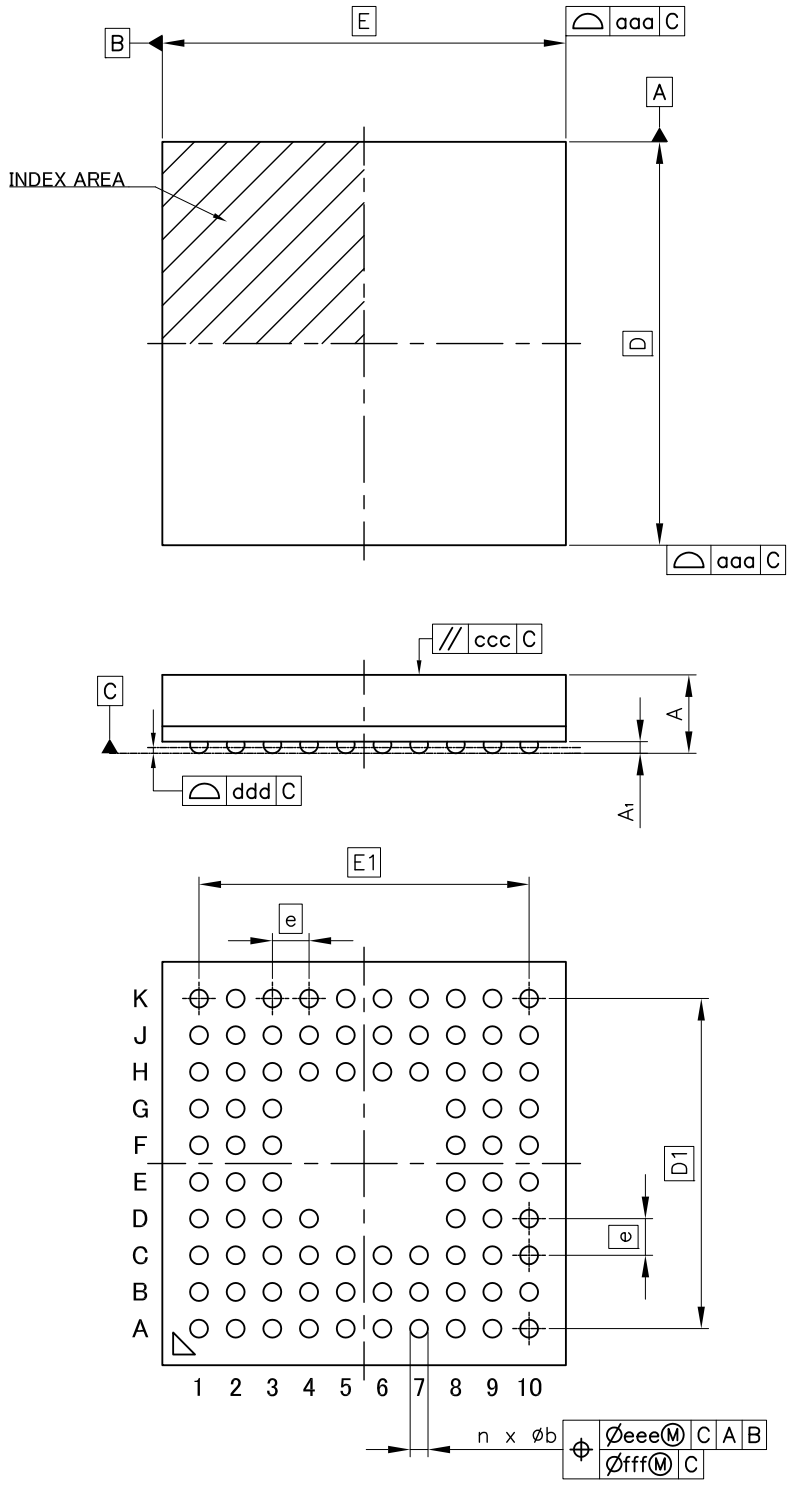
Port Name (Pin Name)	Operating Mode According to Registers Setting		Reset	Software Standby Mode	
				OPE = 1	OPE = 0
P03 (DA0)	All	DA0 output (DAOE0 = 1)	Hi-Z	DA output retained	
		Other than the above (DAOE0 = 0)		Keep-O	
P05 (DA1)	All	DA1 output (DAOE1 = 1)	Hi-Z	DA output retained	
		Other than the above (DAOE1 = 0)		Keep-O	
P07	All		Hi-Z	Keep-O	
P14 (USB0_OVRCURA/ IRQ4)	All		Hi-Z	Keep-O*1, *2	
P15 (IRQ5)	All		Hi-Z	Keep-O*1	
P16 (USB0_VBUS/ USB0_OVRCURB/ IRQ6/RTCOUT)	All		Hi-Z	[RTCOUT output] RTCOUT output [Other than the above] Keep-O*1, *2	
P17 (CMPOB2/IRQ7)	All		Hi-Z	[CMPOB2 output] CMPOB2 output [Other than the above] Keep-O*1	
P21	All		Hi-Z	Keep-O	
P22 (USB0_OVRCURB)	All		Hi-Z	Keep-O*2	
P25 to P27	All		Hi-Z	Keep-O	
P30 (CMPOB3/IRQ0)	All		Hi-Z	[CMPOB3 output] CMPOB3 output [Other than the above] Keep-O*1	
P31 (IRQ1)	All		Hi-Z	Keep-O*1	
P35 (NMI)	All		Hi-Z	Keep-O*1	
P36, P37	All		Hi-Z	Keep-O	
P40 to P47	All		Hi-Z	Keep-O	
PB0	All		Hi-Z	Keep-O	
PB1 (IRQ4)	All		Hi-Z	Keep-O*1	
PB3	All		Hi-Z	Keep-O	
PB5 (USB0_VBUS)	All		Hi-Z	Keep-O*2	
PB7	All		Hi-Z	Keep-O	
PC0, PC2 to PC7	All		Hi-Z	Keep-O	
PD3	All		Hi-Z	Keep-O	
PE0, PE1	All		Hi-Z	Keep-O	
PE2 (IRQ7)	All		Hi-Z	Keep-O*1	
PE3, PE4 (CLKOUT, CLKOUT)	All		Hi-Z	[CLKOUT output] CLKOUT output [Other than the above] Keep-O	
PJ3	All		Hi-Z	Keep-O	

Keep-O: Output pins retain their previous values, and input pins become high-impedance.
Hi-Z: High-impedance
Note 1. Input is enabled if the pin is specified as the software standby mode canceling source while it is used as an external interrupt pin.
Note 2. Input is enabled if the pin is used a USB pin (USB0_VBUS/USB0_OVRCURA/USB0_OVRCURB).

Appendix 2. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

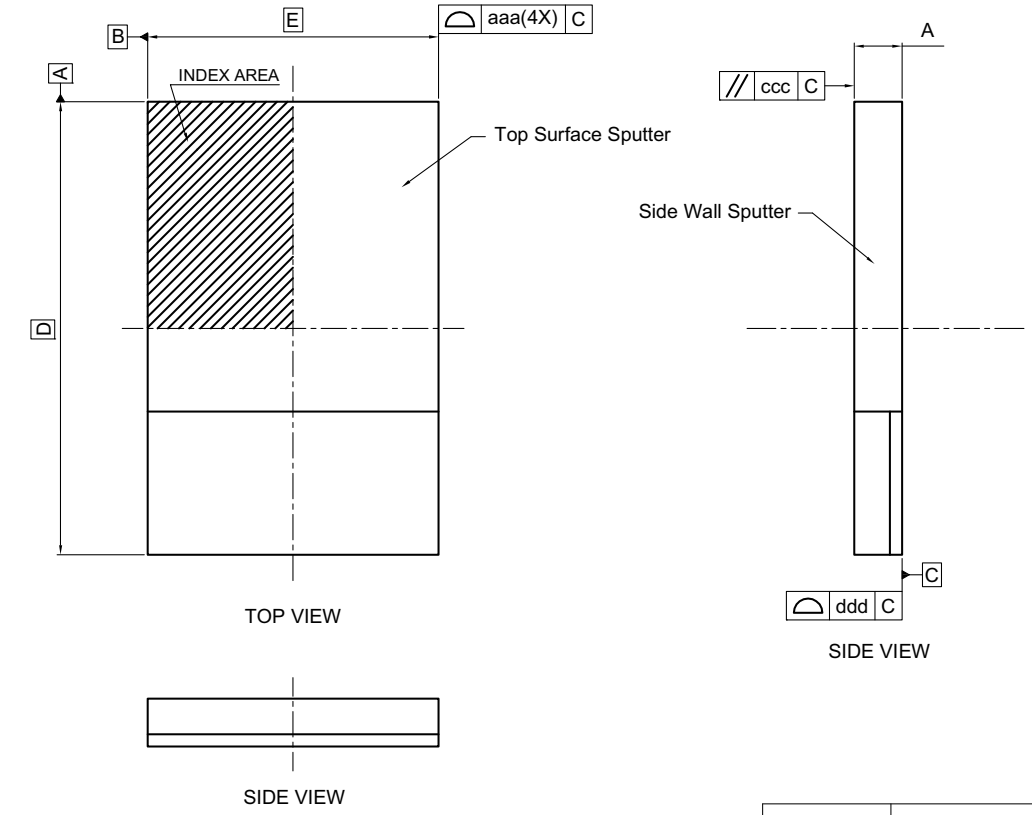
JEITA Package Code	RENESAS Code	MASS(Typ.)[g]
P-TFBGA85-5.5×5.5-0.50	PTBG0085KB-A	0.07

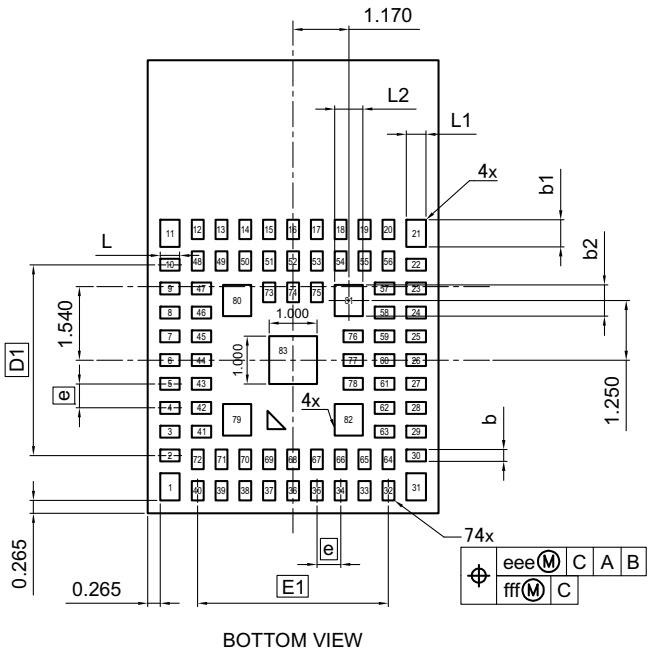


Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	5.500	—
E	—	5.500	—
D1	—	4.500	—
E1	—	4.500	—
A	—	—	1.200
A_1	0.110	—	0.210
b	0.200	—	0.300
e	—	0.500	—
aaa	—	—	0.100
ccc	—	—	0.100
ddd	—	—	0.080
eee	—	—	0.150
fff	—	—	0.080
n	—	85	—

Figure A 85-Pin BGA (PTBG0085KB-A)

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-TFLGA83-6.1x9.5-0.50	PTLG0083KA-A	0.12

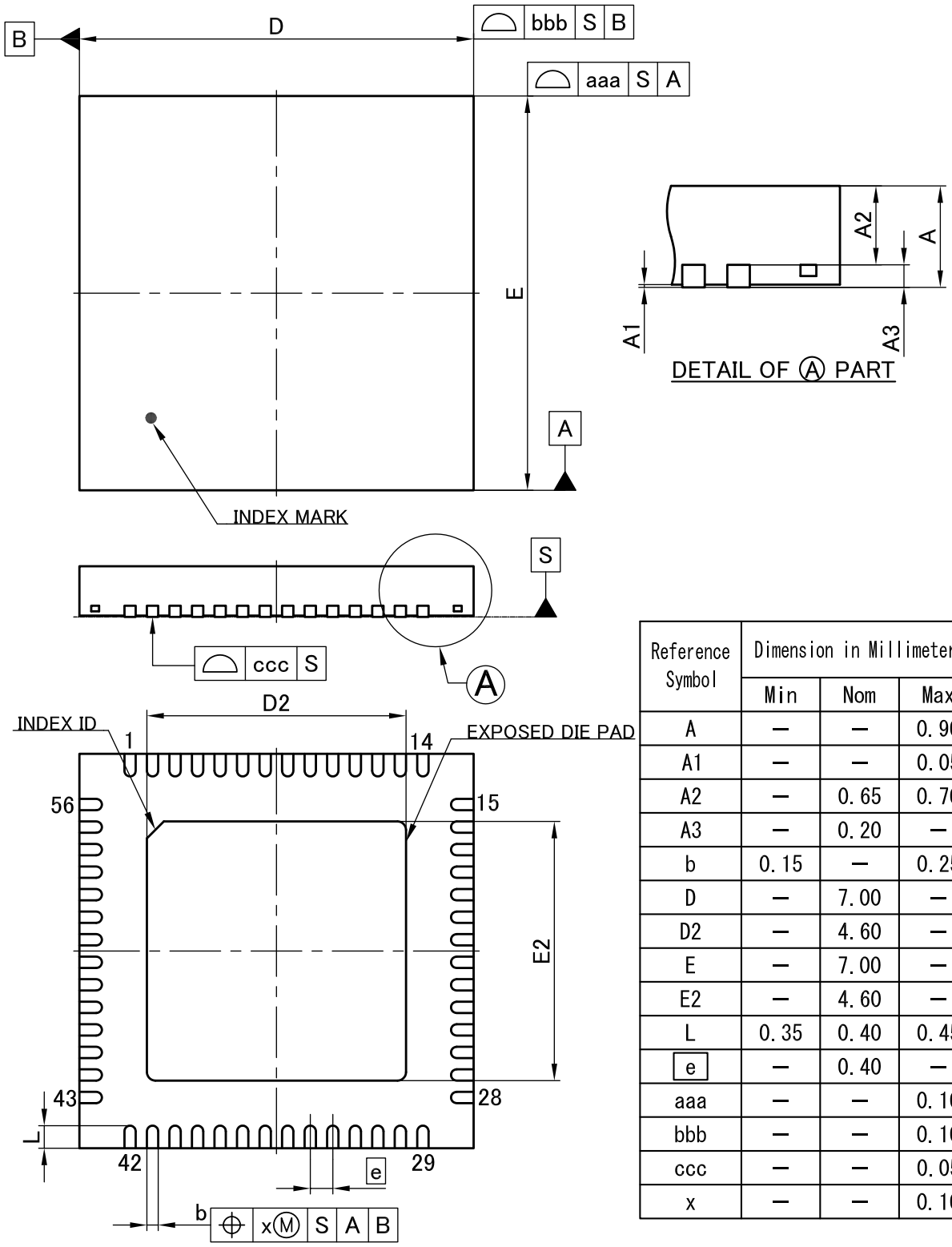




Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	9.500	—
E	—	6.100	—
D1	—	4.000	—
E1	—	4.000	—
A	—	—	1.009
b	—	0.250	—
b1	—	0.570	—
b2	—	0.660	—
L	—	0.410	—
L1	—	0.410	—
L2	—	0.590	—
e	—	0.500	—
aaa	—	—	0.150
ccc	—	—	0.200
ddd	—	—	0.120
eee	—	—	0.150
fff	—	—	0.080

Figure B 83-Pin LGA (PTLG0083KA-A)

JEITA Package Code	RENESAS Code	MASS(Typ.) [g]
P-HVQFN56-7×7-0.40	PVQN0056LA-A	0.13



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	0.90
A1	—	—	0.05
A2	—	0.65	0.70
A3	—	0.20	—
b	0.15	—	0.25
D	—	7.00	—
D2	—	4.60	—
E	—	7.00	—
E2	—	4.60	—
L	0.35	0.40	0.45
e	—	0.40	—
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.05
x	—	—	0.10

Figure C 56-Pin QFN (PVQN0056LA-A)

REVISION HISTORY	RX23W Group User's Manual: Hardware

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

Rev.	Date	Description		Classification
		Page	Summary	
1.00	Jul 31, 2019	—	First edition, issued	
1.10	Nov 30, 2020	Features		
		51	83-pin LGA specifications, added	
		1. Overview		
		All	83-pin LGA specifications, added	
		9. Clock Generation Circuit		
		173, 174	Table 9.1 Specifications of Clock Generation Circuit, changed	
		176	Figure 9.2 Block Diagram of Clock Generation Circuit (83-Pin LGA), added	
		206	9.5 Dedicated Clock Oscillator for Bluetooth, changed	
		206	9.5.1 Connecting the Oscillator, added	
		206	Figure 9.11 Example of the Connection of a 32-MHz Crystal Resonator, changed	
		207	Figure 9.12 Example of Connection of the Bluetooth-dedicated clock output pin, added	
		212	9.9.2 Note on Rewriting the SCKCR3 Register, added	TN-RX*-A0224B/E
		19. Data Transfer Controller (DTCa)		
		394	19.2.8 DTC Vector Base Register (DTCVBR), changed	
		20. Event Link Controller (ELC)		
		421	Table 20.3 Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signals (1/2), changed	
		424	20.2.5 Event Link Option Setting Register C (ELOPC), changed	
		431	Table 20.5 Operations of Peripheral Modules When Event Signal is Input, changed	
		432	20.3.4 Operation of CTSU When Event Signal is Input, added	
		22. Multi-Function Pin Controller (MPC)		
		All	83-pin LGA specifications, added	
		28. Realtime Clock (RTCe)		
		789, 790	28.2.18 RTC Control Register 2 (RCR2), changed	
		793, 794	28.2.21 Time Capture Control Register n (RTCCRn) (n = 0, 1), changed	
		801	Figure 28.3 Clock and Count Mode Setting Procedure, changed	
		802	Figure 28.4 Setting the Time, changed	
		802	Figure 28.5 30-Second Adjustment, changed	
		808	28.3.9 Time Capture Function, title changed	
		813	28.6.5 Notes on Writing to and Reading from Registers, title changed	
		814	Figure 28.14 Initialization Procedure, changed	
		29. Low-Power Timer (LPT)		
		815	Table 29.1 LPT Specifications, changed	
		815	Figure 29.1 LPT Block Diagram, changed	
		816, 817	29.2.1 Low-Power Timer Control Register 1 (LPTCR1), changed	
		818	29.2.3 Low-Power Timer Control Register 3 (LPTCR3), changed	
		819	29.2.4 Low-Power Timer Period Setting Register (LPTPRD), changed	
		820	Table 29.2 Example of Low-Power Timer Period Settings for IWDTCLK, changed	
		821	Table 29.3 Example of Low-Power Timer Period Settings for Sub-Clock, changed	
		822	29.2.5 Low-Power Timer Compare Register 0 (LPCMR0), changed	
		823	29.2.6 Low-Power Timer Standby Wakeup Enable Register (LPWUCR), changed	
		824, 825	29.3.1 Periodic Counting Operation, changed	
		827	29.4 Wakeup from Software Standby Mode by an Interrupt through the Event Link Controller (ELC), changed	

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		Page	Summary	
1.10	Nov 30, 2020	32. USB 2.0 Host/Function Module (USBc)		
		861, 862	32.1 Overview, changed	
		861	Table 32.1 USB Specifications, changed	
		865	32.2.2 System Configuration Status Register 0 (SYSSTS0), changed	
		866	32.2.3 Device State Control Register 0 (DVSTCTR0), changed	
		869, 870	32.2.4 CFIFO Port Register (CFIFO), D0FIFO Port Register (D0FIFO), D1FIFO Port Register (D1FIFO), changed	
		871, 872	32.2.5 CFIFO Port Select Register (CFIFOSEL), D0FIFO Port Select Register (D0FIFOSEL), D1FIFO Port Select Register (D1FIFOSEL) • D0FIFOSEL, D1FIFOSEL, changed	
		875, 876	32.2.6 CFIFO Port Control Register (CFIFOCTR), D0FIFO Port Control Register (D0FIFOCTR), D1FIFO Port Control Register (D1FIFOCTR), changed	
		877	32.2.7 Interrupt Enable Register 0 (INTENB0), changed	
		878	32.2.8 Interrupt Enable Register 1 (INTENB1), changed	
		879	32.2.9 BRDY Interrupt Enable Register (BRDYENB), changed	
		880	32.2.10 NRDY Interrupt Enable Register (NRDYENB), changed	
		881	32.2.11 BEMP Interrupt Enable Register (BEMPENB), changed	
		886 to 888	32.2.14 Interrupt Status Register 1 (INTSTS1), changed	
		889	32.2.15 BRDY Interrupt Status Register (BRDYSTS), changed	
		890	32.2.16 NRDY Interrupt Status Register (NRDYSTS), changed	
		891	32.2.17 BEMP Interrupt Status Register (BEMPSTS), changed	
		901	32.2.26 Pipe Window Select Register (PIPESEL), changed	
		902, 903	32.2.27 Pipe Configuration Register (PIPECFG), changed	
		904	32.2.28 Pipe Maximum Packet Size Register (PIPEMAXP), changed	
		905	32.2.29 Pipe Cycle Control Register (PIPEPERI), changed	
		915	32.2.32 Pipe n Transaction Counter Register (PIPEnTRN) (n = 1 to 5), changed	
		916	32.2.33 Device Address n Configuration Register (DEVADDn) (n = 0 to 5), changed	
		917	32.2.34 USB Module Control Register (USBMC), changed	
		920	32.3.1.2 Controller Function Selection, changed	
		920	32.3.1.3 Controlling USB Data Bus Resistors, changed	
		921 to 926	32.3.1.4 Example of USB External Connection Circuit, changed	
		923	Figure 32.3 Functional Connection of USB Connector in Self-Powered State, changed	
		924	Figure 32.4 Functional Connection Sample of USB Connector with Battery Charging Specification Rev.1.2 Supported, changed	
		926	Figure 32.6 Functional Connection Sample of USB Connector in Bus Powered State, changed	
		927	Table 32.12 Interrupt Sources, changed	
		—	Figure 32.7 Functional Connection Sample of USB Connector in Bus Powered State (2), deleted	
		928	Figure 32.7 Circuits Related to Interrupts in USB, changed	
		930	32.3.3.1 BRDY Interrupt (2) When the SOFCFG.BRDYM Bit = 0 and the PIPECFG.BFRE Bit = 1, changed	
		941	Table 32.15 Pipe Settings, changed	
		942	32.3.4.2 Transfer , changed	
		942	32.3.4.3 Endpoint Number, changed	
		943	32.3.4.4 Maximum Packet Size Setting, changed	
		943	32.3.4.5 Transaction Counter (For Pipes 1 to 5 in Reading Direction), title changed	
		945	32.3.4.9 Auto Response Mode, changed	
		946, 947	32.3.5.1 FIFO Buffer Memory, changed	
		947	32.3.5.2 FIFO Buffer Clearing, changed	
		949	32.3.5.4 DMA Transfers (D0FIFO and D1FIFO Ports) (1) Overview of DMA Transfers, changed	

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		Page	Summary	
1.10	Nov 30, 2020	952	32.3.7 Bulk Transfers (Pipes 1 to 5), changed	
		952	32.3.8 Interrupt Transfers (Pipes 6 to 9), title changed	
		953	32.3.9 Isochronous Transfers (Pipes 1 and 2), title changed	
		962	32.3.11.2 Transfer Schedule, changed	
		963	32.4.1 Setting the Module-Stop Function, changed	
		33. Serial Communications Interface (SCIg, SCIh)		
		971	Table 33.2 SCIh Specifications (2/2), changed	
		985, 986	33.2.8 Serial Control Register (SCR) (1) Non-Smart Card Interface Mode (SCMR.SMIF = 0), changed	
		994, 995	33.2.10 Smart Card Mode Register (SCMR), changed	
		1028	33.3.2 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode, Note 1, changed	
		1031, 1032	33.3.6 SCI Initialization (Asynchronous Mode), changed	
		1031	Figure 33.8 Sample SCI Initialization Flowchart (Asynchronous Mode), changed	
		1037 to 1040	33.3.8 Serial Data Reception (Asynchronous Mode), changed	
		1038	Table 33.28 Status Flags in the SSR Register and Receive Data Handling, changed	
		1047	33.5.2 CTS and RTS Functions, changed	
		1048	33.5.3 SCI Initialization (Clock Synchronous Mode), changed	
		1048	Figure 33.24 Example of SCI Initialization Flowchart (Clock Synchronous Mode), changed	
		1053 to 1055	33.5.5 Serial Data Reception (Clock Synchronous Mode), changed	
		1055	Figure 33.31 Example Flowchart of Serial Reception in Clock Synchronous Mode, changed	
		1056	Figure 33.32 Example Flowchart of Simultaneous Serial Transmission and Reception in Clock Synchronous Mode, changed	
		1060	33.6.3 Block Transfer Mode, changed	
		1061	Figure 33.38 Example of SCI Initialization Flowchart (Smart Card Interface Mode), changed	
		1063 to 1065	33.6.6 Serial Data Transmission (Except in Block Transfer Mode), changed	
		1066, 1067	33.6.7 Serial Data Reception (Except in Block Transfer Mode), changed	
		1074	Figure 33.51 Example of the Flowchart of SCI Initialization (for Simple I^2C Mode), changed	
		1076	Figure 33.54 Example of the Procedure for Master Transmission Operations in Simple I^2C Mode (with Transmission Interrupts and Reception Interrupts in Use), changed	
		1083	33.8.5 SCI Initialization (Simple SPI Mode), changed	
		1100	Figure 33.75 Block Diagram of Digital Noise Filter, title changed	
		1101	33.12.2 Interrupts in Asynchronous Mode, Clock Synchronous Mode, and Simple SPI Mode, changed	
		1113	Figure 33.82 Example of Flowchart for Receive Error Handling (during Reception of the Start Frame), changed	
		35. I^2C-bus Interface (RIICa)		
		1121 to 1123	35.1 Overview, changed	
		1121	Table 35.1 RIIC Specifications (1/2), changed	
		1122	Table 35.1 RIIC Specifications (2/2), changed	
		1122	Figure 35.1 RIIC Block Diagram, changed	
		1123	Figure 35.2 I/O Pin Connection to the External Circuit (I^2C-bus Configuration Example), changed	
		1124, 1125	35.2.1 I^2C-bus Control Register 1 (ICCR1), changed	
		1126 to 1129	35.2.2 I^2C-bus Control Register 2 (ICCR2), changed	
		1130	35.2.3 I^2C-bus Mode Register 1 (ICMR1), changed	
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