UBM1-GL

Hardware Design

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About the Document

Revision History

Version	Date	Author	Description
1.0	2024-02-04	Gustavo Suarez	Initial

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1 Introduction

This document defines UBM1-GL module and describes its air and hardware interfaces which connect to your applications.

This document helps you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of UBM1-GL. To facilitate application designs, it also includes some reference designs. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

FCC Certification Requirements.
According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.
And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based timeaveraging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.

2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

3. A label with the following statements must be attached to the host end product: This device contains FCC ID: 2AECKUBM1GL

4. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

Operating Band	Peak gain	Manufacturer	Impedance	Antenna type
LTE Band 2	1.59 dBi	Shanghai Saintenna Electronic Technology Co., Ltd.	50Ω	External Antenna
LTE Band 4	2.00 dBi			
LTE Band 5	2.53 dBi			
LTE Band 12	3.95 dBi			
LTE Band 13	4.45 dBi			
LTE Band 18(815-824)	3.19 dBi			
LTE Band 18(824-830)	2.53 dBi			
LTE Band 19	2.29 dBi			
LTE Band 25	1.59 dBi			
LTE Band 26(814-824)	3.19 dBi			

LTE Band 26(824-849)	2.53 dBi			
LTE Band 66	2.00 dBi			
LTE Band 85	3.95 dBi			

5. This module must not transmit simultaneously with any other antenna or transmitter

6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.
For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093
If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.
For this device, OEM integrators must be provided with labeling instructions of finished products.
Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:
A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).
For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: 2AECKUBM1GL" or "Contains FCC ID: 2AECKUBM1GL" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.
The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.
The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.
To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B

unintentional radiator requirements.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

IC Statement

IRSS-GEN

"This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Déclaration sur l'exposition aux rayonnements RF

L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

The host product shall be properly labeled to identify the modules within the host product.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word "Contains" or similar wording expressing the same meaning, as follows:

"Contains IC: 28560-UBM1GL" or "where: 28560-UBM1GL is the module's certification number".

Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.

L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:

"Contient IC: 28560-UBM1GL " ou "où: 28560-UBM1GL est le numéro de certification du module".

KDB 996369 D03 OEM Manual rule sections:

2.2 List of applicable FCC rules

This module has been tested for compliance to FCC Part 15.247

2.3 Summarize the specific operational use conditions

The module is tested for standalone mobile RF exposure use condition. Any other usage conditions such as co-location with other transmitter(s) or being used in a portable condition will need a separate reassessment through a class 2 permissive change application or new certification.

2.4 Limited module procedures

Not applicable.

2.5 Trace antenna designs

Not applicable.

2.6 RF exposure considerations

This equipment complies with FCC mobile radiation exposure limits set forth for an controlled environment. This equipment should be installed and operated with a minimum distance of 20cm between the radiator & your body. If the module is installed in a portable host, a separate SAR evaluation is required to confirm compliance with relevant FCC portable RF exposure rules.

2.7 Antennas

Please refer to page 7 of the manual

2.8 Label and compliance information

The host system using this module, should have label in a visible area indicated the following texts: “Contains FCC ID: 2AECKUBM1GL, Contains IC: 28560-UBM1GL”

2.9 Information on test modes and additional testing requirements5

Top band can increase the utility of our modular transmitters by providing instructions that simulates or characterizes a connection by enabling a transmitter.

2.10 Additional testing, Part 15 Subpart B disclaimer

The module without unintentional-radiator digital circuity, so the module does not require an evaluation by FCC Part 15 Subpart B. The host should be evaluated by the FCC Subpart B.

2.11 Note EMI Considerations

Please follow the guidance provided for host manufacturers in KDB publications 996369 D02 and D04.

2.12 How to make changes

Only Grantees are permitted to make permissive changes.

IMPORTANT NOTE: In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

2 Product Overview

2.1. General Description

UBM1-GL is an embedded IoT LTE Cat M1 wireless communication modules. It provides data connectivity on LTE HD-FDD networks. It also provides GNSS functions to meet your specific application demands.

The module is based on an architecture in which WWAN and GNSS Rx chains share certain hardware blocks. However, the module does not support concurrent operation of WWAN and GNSS. The solution adopted in the module is a form of coarse time-division multiplexing (TDM) between WWAN and GNSS Rx chains. Given the relaxed latency requirements of most LPWA applications, time-division sharing of resources can be made largely transparent to applications. For more details, see ***document [1]***.

UBM1-GL is an industrial-grade module for industrial and commercial applications only.

Table 2: Frequency Bands of UBM1-GL Modules

Supported Bands	LTE Bands Power Class	GNSS
Cat M1 Only: LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/B25/B26/B27/B28/B66/B85	Power Class 5 (21 dBm)	GPS, GLONASS, BDS, Galileo, QZSS

With such a compact size as 23.6 mm × 19.9 mm × 2.2 mm, the module can meet different requirements for M2M applications such as smart metering, tracking system, security and wireless POS.

UBM1-GL is a SMD type modules that can be embedded into applications through the 102 LGA pins. It supports internet service protocols like TCP, UDP and PPP. Based on extended AT commands developed by Ubicquia, you can use these internet service protocols easily.

2.2. Key Features

Table 3: Key Features of UBM1-GL Module

Features	Details
Power Supply	● Supply voltage [1]: 2.6–4.8 V ● Typical supply voltage: 3.3 V
Transmitting Power [2]	**LTE HD-FDD bands:** ● Class 5 (21 dBm +1.7/-3 dB)
LTE Features [3]	● Supports 3GPP Rel-14 ● Supports LTE Cat M1 ● Supports 1.4 MHz RF bandwidth for LTE Cat M1 ● Max. transmission data rates: Cat M1: 588 kbps (DL)/1119 kbps (UL)
Internet Protocol Features	● Supports PPP/TCP/UDP/SSL/TLS/FTP(S)/HTTP(S)/NITZ/PING/MQTT/ LwM2M/CoAP/IPv6 protocols ● Supports PAP and CHAP for PPP connections
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interface	Supports 1.8 V USIM/SIM card only
PCM Interface	Supports one digital audio interface: PCM interface for VoLTE
USB Interface	● Compliant with USB 2.0 specification (slave only) ● Supports operations at high-speed, full-speed and low-speed modes ● Used for AT command communication, data transmission, GNSS NMEA sentences output, software debugging and firmware upgrade ● Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–6.5, Android 4.x–13.x
UART	**Main UART:** ● Used for data transmission and AT command communication ● 115200 bps by default ● The default frame format is 8N1 (8 data bits, no parity, 1 stop bit) ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for software debugging and log output

[1] For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. To ensure full functionality mode, the minimum power supply voltage should be higher than 2.8 V.
[2] See ***Table 2*** or ***Chapter 6.5*** for the LTE bands power class level of each module model.
[3] See ***Table 2*** or ***Chapter 6.5*** for the LTE and GSM features of each model.

	● Supports 115200 bps **GNSS UART:** ● Used for GNSS data and NMEA sentences output ● 115200 bps baud rate by default
GNSS Features	● GPS, GLONASS, BDS, Galileo and QZSS ● 1 Hz data update rate by default
AT Commands	● *3GPP TS 27.007* and *3GPP TS 27.005* AT commands ● Enhanced AT commands
Network Indication	One NET_STATUS pin for network connectivity status indication
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● GNSS antenna interface (ANT_GNSS)
Physical Characteristics	● Dimensions: (23.6 ±0.2) mm × (19.9 ±0.2) mm × (2.2 ±0.2) mm ● Weight: approx. 2.15 g
Temperature Range	● Operating temperature range: -35 to +75 °C [4] ● Extended temperature range: -40 to +85 °C [5] ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	USB interface, DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

[4] Within the operating temperature range, the module meets 3GPP specifications.
[5] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice*, SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

2.3. Functional Diagram

The following figures show the block diagram of UBM1-GL and the major functional parts.

- Power management
- Baseband
- Radio frequency
- Peripheral interfaces

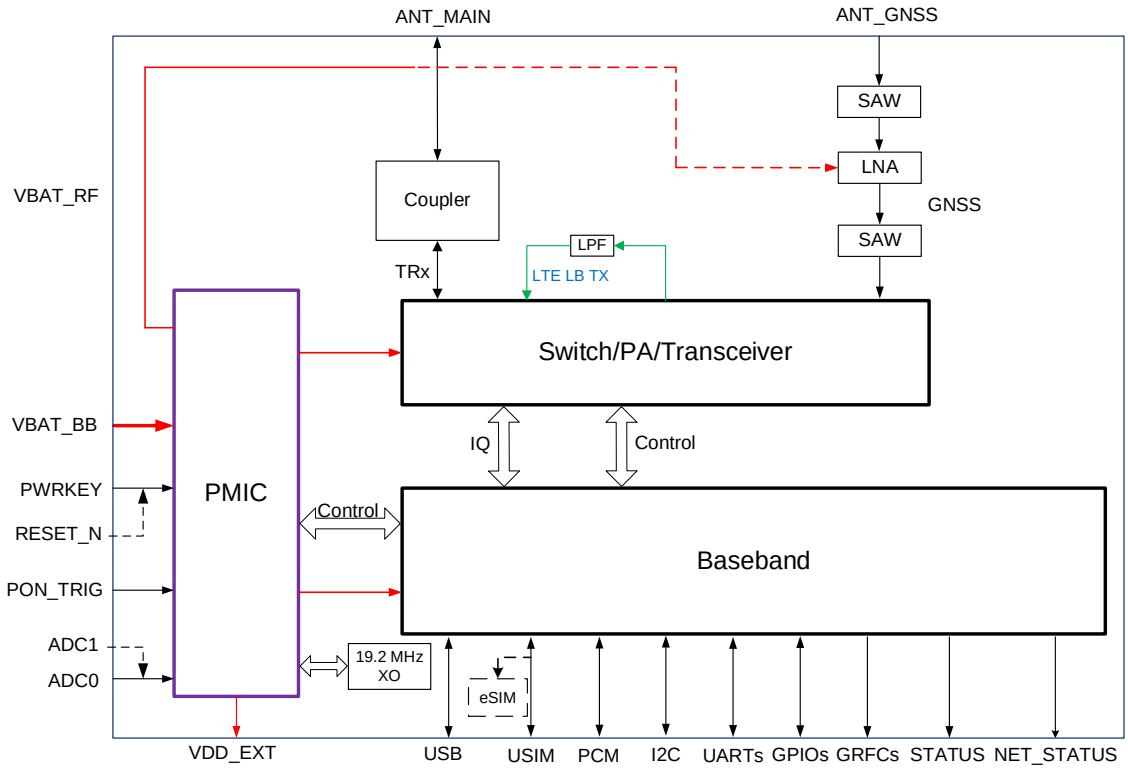


Figure 1: Functional Diagram of UBM1-GL

NOTE

1. eSIM* function is optional. If eSIM is selected, then any external (U)SIM card cannot be used simultaneously.
2. The output voltage of PWRKEY is 1.5 V because of the voltage drop inside the chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, never pull down PWRKEY to GND permanently.
3. RESET_N connects directly to PWRKEY inside the module.
4. Do not use ADC0 and ADC1 simultaneously, as ADC1 connects directly to ADC0 inside the module. UBM1-GL supports the use of only one ADC interface at a time: either ADC0 or ADC1.

2.4. EVB Kit

To help you develop applications with the module, Ubicquia supplies an evaluation board (UMTS&LTE EVB) with accessories to develop or test the module. For more details, see ***document [2]***.

3 Application Interfaces

UBM1-GL is designed with 102 LGA pins for connection to various cellular application platforms. The subsequent chapters describe the interfaces listed below in detail:

- Power supply
- PON_TRIG Interface
- (U)SIM interface
- USB interface
- UART
- PCM and I2C interfaces
- Status indication interfaces
- MAIN_RI
- USB_BOOT
- ADC interfaces
- GPIO interfaces
- GRFC interfaces

3.1. Pin Assignment

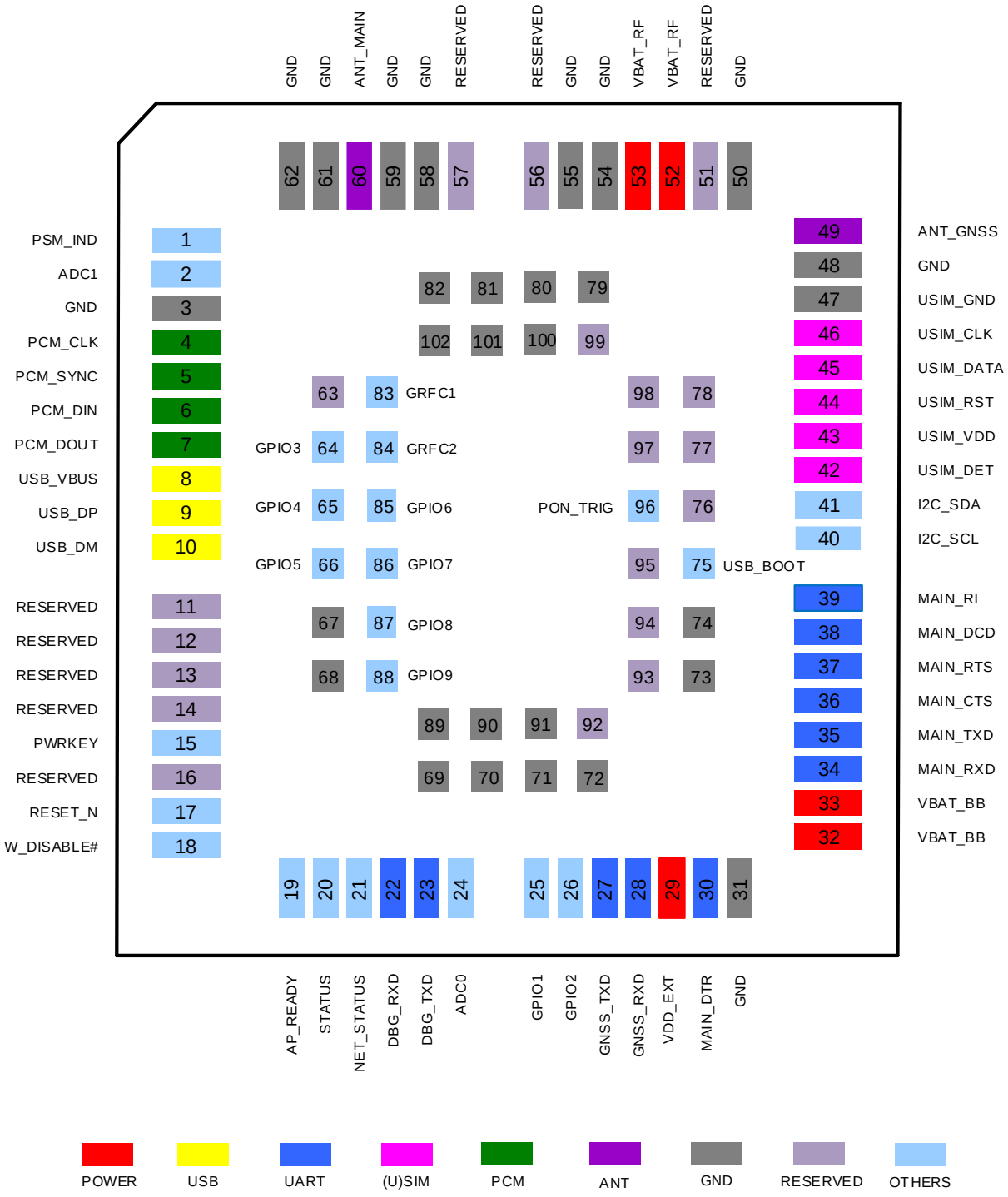


Figure 2: Pin Assignment (Top View)

NOTE

1. Do not use ADC0 and ADC1 simultaneously, as ADC1 connects directly to ADC0 inside the module. UBM1-GL supports the use of only one ADC interface at a time: either ADC0 or ADC1.
2. The output voltage of PWRKEY is 1.5 V because of the voltage drop inside the chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, never pull down PWRKEY to GND permanently.
3. RESET_N connects directly to PWRKEY inside the module.
4. GNSS_TXD (pin 27) and GRFC2 (pin 84) are BOOT_CONFIG pins. Never pull them up before startup, otherwise the module cannot power on normally.
5. GPIO1 (pin 25) supports fast shutdown function. This function is disabled by default. See ***Chapter 3.6.3*** for more details.
6. PCM and I2C interfaces are used for VoLTE.
7. Keep all RESERVED and unused pins unconnected.
8. Connect GND pins to the ground in the design.

3.2. Pin Description

Table 4: Definition of I/O Parameters

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rate current.

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	Vmax = 4.8 V Vmin = 2.6 V Vnom = 3.3 V	
VBAT_RF	52, 53	PI	Power supply for the module's RF part		
VDD_EXT	29	PO	Provides 1.8 V for external circuits	Vnom = 1.8 V $I_O$max = 50 mA	If unused, keep this pin open.
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102				
Turn-on/Turn-off the Module					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turn on/off the module	Vnom = 1.5 V V_{IL}max = 0.45 V	Never pull down PWRKEY to GND permanently. The output voltage is 1.5 V because of the voltage drop inside the chipset.
Reset the Module					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET_N	17	DI	Reset the module	Vnom = 1.5 V V_{IL}max = 0.45 V	Multiplexed from PWRKEY (connects directly to PWRKEY inside the module). If unused, keep it open.
Status Indication Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PSM_IND [6]	1	DO	Indicate the module's power saving mode	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep these pins open.

[6] When PSM is enabled, the function of PSM_IND pin will be activated after the module is rebooted. When PSM_IND is in high voltage level, the module is in full functionality mode. When it is in low voltage level, the module is in PSM.

STATUS	20	DO	Indicate the module's operation status		
NET_STATUS	21	DO	Indicate the module's network activity status		
PON_TRIG Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PON_TRIG	96	DI	Wake up the module from PSM		1.8 V power domain. Rising-edge triggered. Pulled-down by default. If unused, keep this pin open.
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	AI	USB connection detect	Vmax = 5.25 V Vmin = 4.0 V Vnom = 5.0 V	Typical 5.0 V
USB_DP	9	AIO	USB differential data (+)		Compliant with USB 2.0 standard specification. Require differential impedance of 90 Ω.
USB_DM	10	AIO	USB differential data (-)		
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_DET	42	DI	(U)SIM card hot-plug detect	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
USIM_VDD	43	PO	(U)SIM card power supply	Vmax = 1.9 V Vmin = 1.7 V	Only 1.8 V (U)SIM card is supported.
USIM_RST	44	DO	(U)SIM card reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
USIM_DATA	45	DIO	(U)SIM card data	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V V_{OL}max = 0.45 V	1.8 V power domain.

				V_{OH}min = 1.35 V	
USIM_CLK	46	DO	(U)SIM card clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain.
USIM_GND	47		Specified ground for (U)SIM card		
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_DTR	30	DI	Main UART data terminal ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep these pins open.
MAIN_RXD	34	DI	Main UART receive		
MAIN_TXD	35	DO	Main UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
MAIN_CTS	36	DO	Clear to send signal from the module		Connect to the MCU's CTS. 1.8 V power domain. If unused, keep the pin open.
MAIN_RTS	37	DI	Request to send signal to the module	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	Connect to the MCU's RTS. 1.8 V power domain. If unused, keep the pin open.
MAIN_DCD	38	DO	Main UART data carrier detect	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep these pins open.
MAIN_RI	39	DO	Main UART ring indication		
Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	22	DI	Debug UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep these pins open.
DBG_TXD	23	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
GNSS UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

GNSS_TXD	27	DO	GNSS UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain. If unused, keep this pin open.
GNSS_RXD	28	DI	GNSS UART receive	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
PCM Interface [7]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_CLK	4	DO	PCM clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep these pins open.
PCM_SYNC	5	DO	PCM data frame sync		
PCM_DIN	6	DI	PCM data input	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	
PCM_DOUT	7	DO	PCM data output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	
I2C Interface [7]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	40	OD	I2C serial clock (for external codec)		External pull-up resistor is required. 1.8 V only. If unused, keep these pins open.
I2C_SDA	41	OD	I2C serial data (for external codec)		
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	60	AIO	Main antenna interface		50 Ω impedance
ANT_GNSS	49	AI	GNSS antenna interface		50 Ω impedance. If unused, keep this pin open.

[7] PCM and I2C interfaces are used for VoLTE.

GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1 [8]	25	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
GPIO2	26				
GPIO3	64				
GPIO4 错误!未定义书签。	65				
GPIO5	66				
GPIO6	85				
GPIO7	86				
GPIO8	87				
GPIO9	88				
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	24	AI	General-purpose ADC interface	Voltage range: 0.1–1.8 V	Do not use ADC0 and ADC1 simultaneously, as ADC1 connects directly to ADC0 inside the module. If unused, keep these pins open.
ADC1	2	AI			
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
W_DISABLE#	18	DI	Airplane mode control	V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.2 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. When it is in low voltage level, the module can enter airplane mode. If unused, keep this pin open.
AP_READY	19	DI	Application processor ready	V_{IL}min = -0.3 V V_{IL}max = 0.6 V	1.8 V power domain. If unused, keep this pin

[8] This pin is GPIO by default, which can be multiplexed into fast shutdown interface (see ***Chapter 3.6.3*** for details).

				V_{IH}min = 1.2 V V_{IH}max = 2.0 V	open.
USB_BOOT	75	DI	Force the module into emergency download mode		1.8 V power domain.
GRFC Interfaces [9]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	83	DO	Generic RF controller	V_{OL}max = 0.45 V V_{OH}min = 1.35 V	1.8 V power domain. If unused, keep this pin open.
GRFC2	84				BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain. If unused, keep this pin open.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	11–14, 16, 51, 56-57, 63, 76–78, 92–95, 97–99				Keep these pins open.

3.3. Operating Modes

Table 6: Operating Modes

Mode	Details	
Full Functionality Mode	Connected	The module connects to network. Its power consumption varies with the network setting and data transfer rate.
	Idle	The module remains registered on network, and is ready to send and receive data. In this mode, the software is active.
Extended Idle Mode DRX (e-I-DRX)	The module and the network may negotiate over non-access stratum signaling the use of e-I-DRX for reducing power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module into airplane mode where the RF function is invalid.	
Minimum Functionality Mode	**AT+CFUN=0** can set the module into a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Sleep Mode	The module remains the ability to receive paging message, SMS and TCP/UDP data from the network normally. In this mode, the power consumption reduces to a low level.	
Power OFF Mode	The module's power supply is shut down by its power management unit. In this mode, the software is inactive, the serial interfaces are inaccessible, while the operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	
Power Saving Mode (PSM)	PSM is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. The power consumption reduces to a minimized level.	

NOTE

During e-I-DRX, it is recommended to use UART for data communication, as the use of USB interface increases power consumption.

3.4. Power Saving

3.4.1. Airplane Mode

When the module enters airplane mode, the RF function does not work, and all AT commands correlative with RF function are inaccessible. This mode can be set via the following methods.

Hardware:

W_DISABLE# is pulled up by default. Driving it low makes the module enter airplane mode.

Software:

AT+CFUN=<fun> provides choice of the functionality level via setting **<fun>** to 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1**: Full functionality mode (by default).
- **AT+CFUN=4**: Airplane mode. RF function is disabled.

NOTE

1. Airplane mode control via W_DISABLE# is disabled in firmware by default. It can be enabled by **AT+QCFG="airplanecontrol"**. For details of the command, see ***document [4]***.
2. The execution of **AT+CFUN** (see ***document [3]***) will not affect GNSS function.

3.4.2. Power Saving Mode (PSM)

The module minimizes its power consumption through entering PSM. PSM mode is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. Therefore, the module in PSM cannot immediately respond to your requests.

When the module wants to use the PSM, it shall request an Active Time value during every Attach and TAU procedures. If the network supports PSM and accepts that the module uses PSM, the network confirms usage of PSM by allocating an Active Time value to the module. If the module wants to change the Active Time value, e.g., the module requests the value it wants in the TAU procedure.

If PSM is supported by the network, then it can be enabled via **AT+CPSMS**. See ***document [3]*** for details about the AT command.

Any of the following methods can wake up the module from PSM:

- Wake up the module from PSM through a rising edge on PON_TRIG. (Recommended)
- Wake up the module by driving PWRKEY low.
- When the TAU timer expires, the module wakes up from PSM automatically.

3.4.3. Extended Idle Mode DRX (e-I-DRX)

The module (UE) and the network may negotiate over non-access stratum signalling the use of e-I-DRX for reducing its power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.

Applications that want to use e-I-DRX need to consider specific handling of mobile terminating services or data transfers, and in particular they need to consider the delay tolerance of mobile terminated data.

In order to negotiate the use of e-I-DRX, the UE requests e-I-DRX parameters during attach procedure and RAU/TAU procedure. The EPC may reject or accept the UE request for enabling e-I-DRX. In case the EPC accepts e-I-DRX, the EPC based on operator policies and, if available, the e-I-DRX cycle length value in the subscription data from the HSS, may also provide different values of the e-I-DRX parameters than what were requested by the UE. If the EPC accepts the use of e-I-DRX, the UE applies e-I-DRX based on the received e-I-DRX parameters. If the UE does not receive e-I-DRX parameters in the relevant accept message because the EPC rejected its request or because the request was received by EPC not supporting e-I-DRX, the UE shall apply its regular discontinuous reception.

If e-I-DRX is supported by the network, then it can be enabled by **AT+CEDRXS=1**. See ***document [3]*** for details about the AT command.

3.4.4. Sleep Mode

The module reduces its current consumption to a low level during sleep mode. The following sub-chapters describe the power saving procedure of the module.

3.4.4.1. UART Application

If the MCU communicates with the module via UART, the following preconditions enable the module to enter sleep mode.

- Execute **AT+QSCLK=1** (see ***document [3]***) to enable sleep mode.
- Drive MAIN_DTR high.

The following figure shows the connection between the module and the MCU.

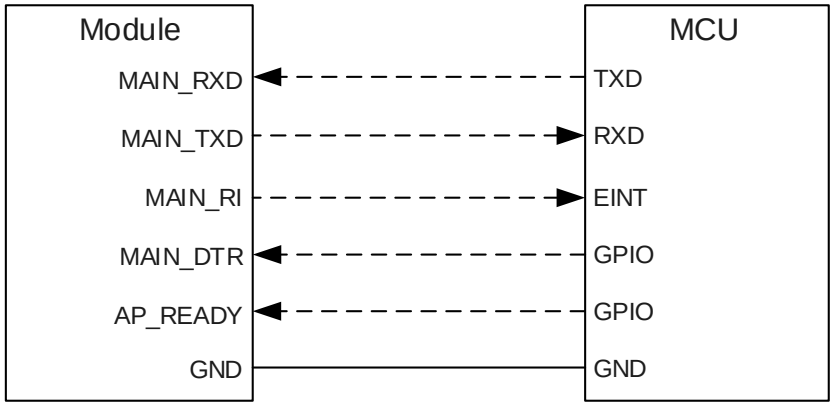


Figure 3: Sleep Mode Application via UART

- When the module has a URC to report, MAIN_RI will wake up the MCU. See ***Chapter 3.15*** for details about MAIN_RI behavior.
- Driving MAIN_DTR low will wake up the module.
- AP_READY detects the sleep state of the MCU (can be configured into high-level or low-level detection). See **AT+QCFG="apready"** in ***document [4]*** for details.

3.5. Power Supply

3.5.1. Power Supply Pins

UBM1-GL provides the following four VBAT pins for connection with an external power supply. There are two separate voltage domains for VBAT.

- Two VBAT_RF pins for the module's RF part.
- Two VBAT_BB pins for the module's baseband part.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	IO	Description	Min.	Typ.	Max.	Unit
VBAT_RF	52, 53	PI	Power supply for the module's RF part	2.6	3.3	4.8	V
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	2.6	3.3	4.8	V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102						

3.5.2. Voltage Stability Requirements

The power supply range of UBM1-GL is 2.6–4.8 V. For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. To ensure full functionality mode, the minimum power supply voltage should be higher than 2.8 V. Make sure that the input voltage never drops below 2.6 V.

To decrease voltage-drop, bypass capacitors of about 100 µF with low ESR should be used, and multi-layer ceramic chip capacitor (MLCC) arrays should also be reserved due to their low ESR. Use seven ceramic capacitors (220 nF, 47 nF, 150 pF, 100 pF, 68 pF, 33 pF, 10 pF) to compose the MLCC array for VBAT_BB, three ceramic capacitors (100 nF, 33 pF, 10 pF) to compose the MLCC array for VBAT_RF, and place these capacitors close to VBAT pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be not less than 0.6 mm. The longer the VBAT trace is, the wider it should be.

To get a stable power source, it is suggested to use two TVS components with low leakage current and suitable reverse stand-off voltage, and it is recommended to place them as close as possible to the VBAT pins.

In addition, route VBAT_BB and VBAT_RF traces in inner-layer of the PCB, and place a ferrite bead as close to VBAT_BB as possible. Follow the criteria below for ferrite bead selection:

- Current rating ≥ 600 mA and low DC resistance to avoid voltage drop during instantaneous high power consumption.
- ≥ 800 Ω impedance @ 700–960 MHz.

The following figure shows the star structure of the power supply.

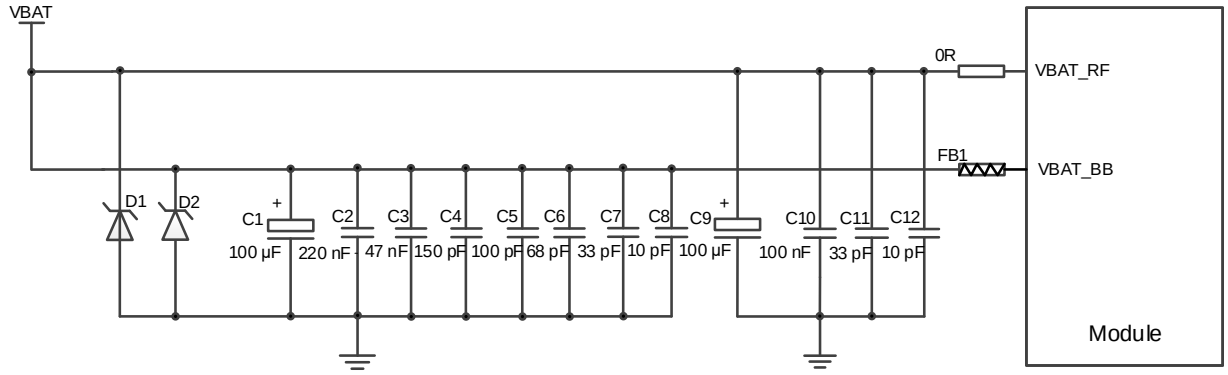


Figure 4: Star Structure of the Power Supply

It is recommended to select a DC-DC converter chip or LDO chip with ultra-low leakage current and current output not less than 1.0 A for the power supply design.

3.5.3. Power Supply Voltage Monitoring

AT+CBC monitors the VBAT_BB voltage value. For more details, see ***document [3]***.

3.6. Turn On and Turn Off

3.6.1. Turn On with PWRKEY

Table 8: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	Never pull down PWRKEY to GND permanently. The output voltage is 1.5 V because of the voltage drop inside the chipset.

The module can be turned on by driving PWRKEY low for 500–1000 ms. It is recommended to use an open drain/collector driver to control the PWRKEY.

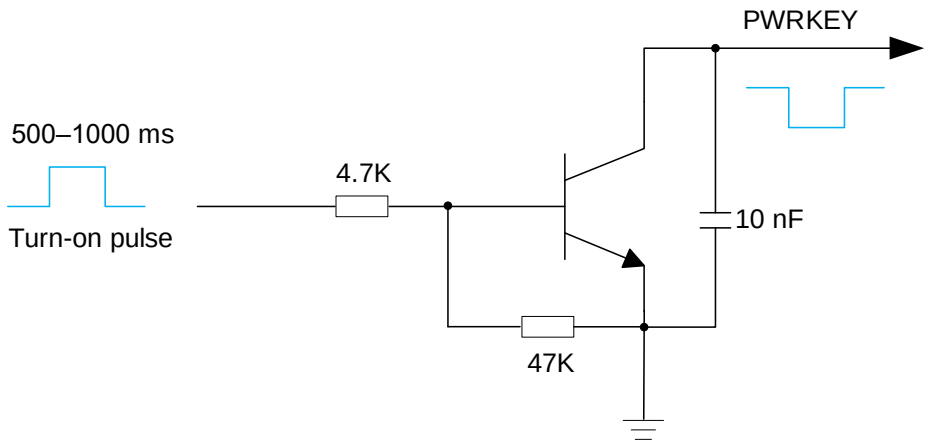


Figure 5: Turn On the Module with a Driver Circuit

Another way to control the PWRKEY is using a push button. As electrostatic strike may be generated from the finger touching when the button is pressed, a TVS component is indispensable to be placed near the button for ESD protection. A reference circuit is illustrated in the following figure.

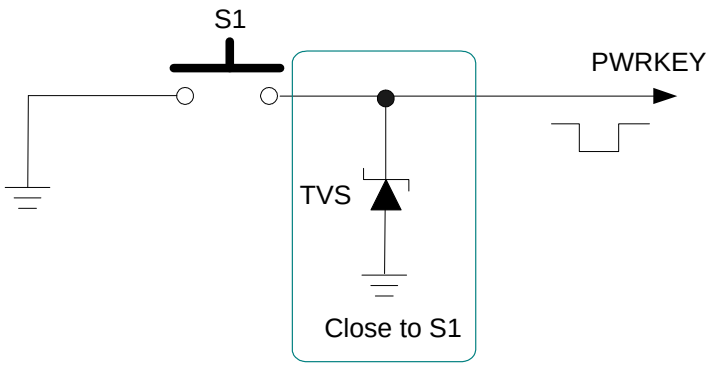


Figure 6: Turn On the Module with a Push Button

The power-up timing is illustrated in the following figure.

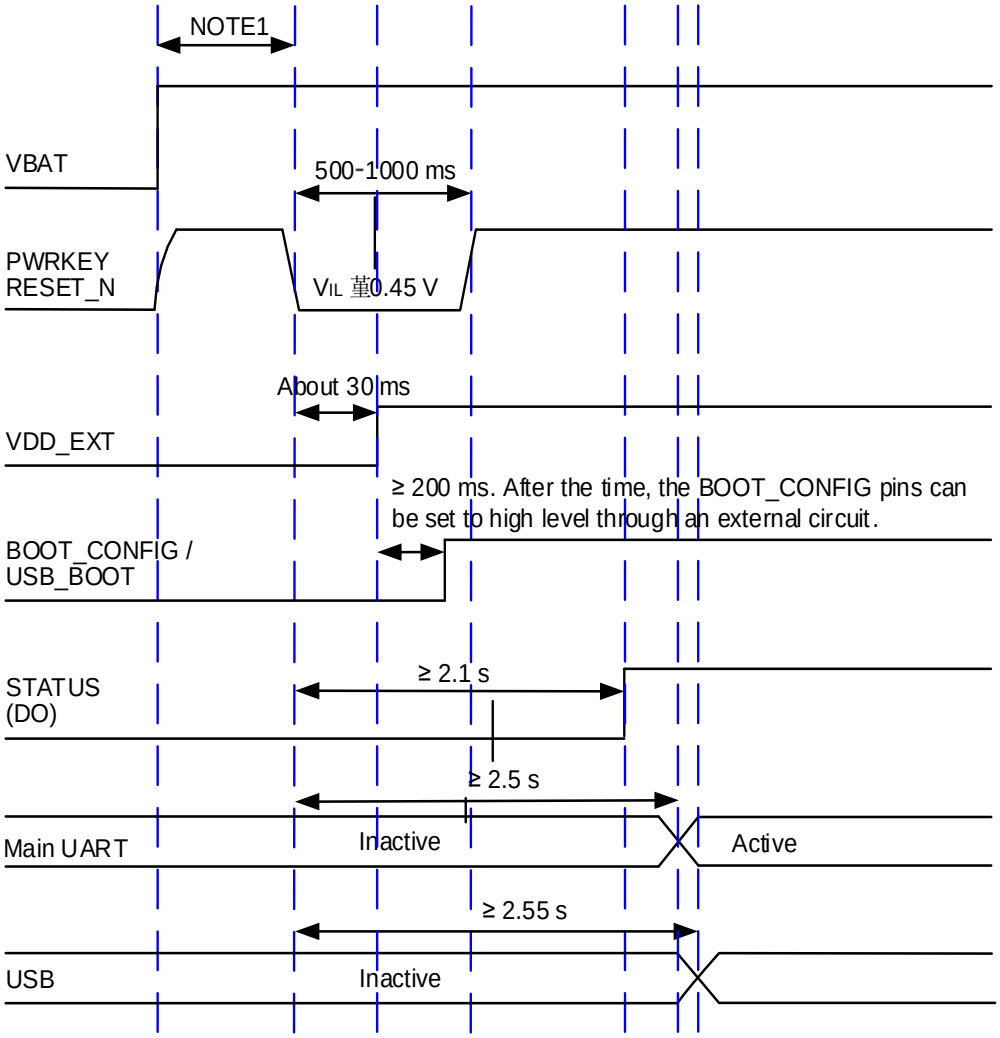


Figure 7: Power-up Timing

NOTE

1. Ensure that VBAT is stable before pulling down PWRKEY and keep the interval not less than 30 ms.
2. The output voltage of PWRKEY is 1.5 V because of the voltage drop inside the chipset. Due to platform limitations, the chipset has integrated the reset function into PWRKEY. Therefore, never pull down PWRKEY to GND permanently.

3.6.2. Turn Off

Either of the following methods can be used to turn off the module:

- with PWRKEY
- with **AT+QPOWD**

3.6.2.1. Turn Off with PWRKEY

Driving PWRKEY low for 650–1500 ms and then releasing it, the module will execute power-down procedure.

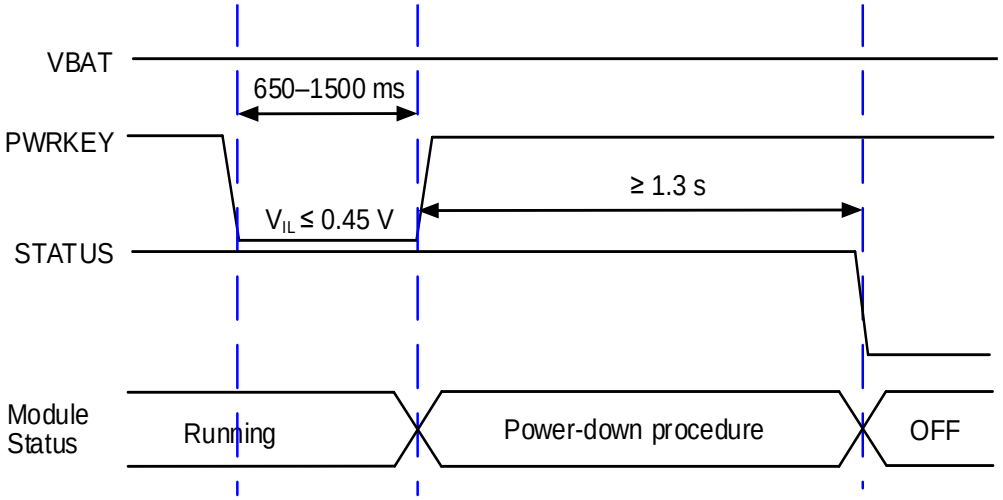


Figure 8: Power-down Timing

3.6.2.2. Turn Off with AT Command

It is also a safe way to execute **AT+QPOWD** to turn off the module, which is similar to turning off the module with PWRKEY. See ***document [3]*** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module is working. Only after the module is shut down with PWRKEY, fast shutdown function or AT command can the power supply be cut off.

2. While turning off the module with AT command, keep PWRKEY at high level after the execution of turn-off command, otherwise the module will be turned on again after it turns off.
3. It is recommended to judge whether the module has been shut down based on the state of STATUS.

3.6.3. Fast Shutdown

The module supports fast shutdown function through GPIO1 (pin 25). When the pin detects a falling edge, the module powers off within 100 ms without damaging the file system, but the writing data may be lost. Fast shutdown is disabled by default.

For more details, see **AT+QCFG="fast/poweroff"** in ***document [4]***.

Table 9: Pin Definition of Fast Shutdown Interface

Pin Name	Pin No.	I/O	Description	Comment
GPIO1 [10]	25	DI	When the pin detects a falling edge, the module powers off	Falling-edge triggered. Pulled-up by default. 1.8 V power domain.

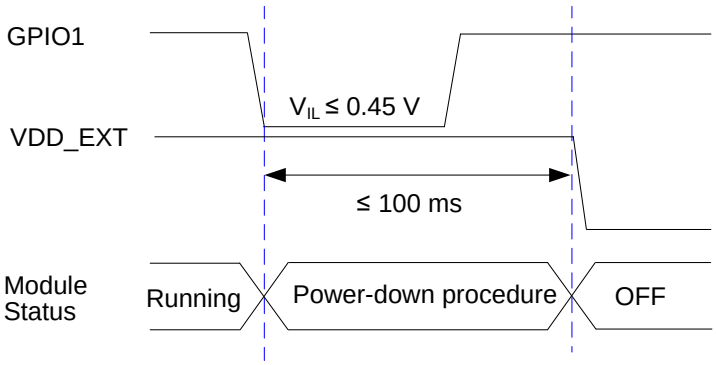


Figure 9: Fast Shutdown Timing

[10] Pin 25 is a general-purpose IO by default. It can be multiplexed into fast shutdown interface with **AT+QCFG="fast/poweroff"**.

3.7. Reset

RESET_N works to reset the module. Due to platform limitations, the chipset has integrated the reset function into PWRKEY, and RESET_N connects directly to PWRKEY inside the module.

Table 10: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Reset the module	Multiplexed from PWRKEY.

The module can be reset by driving RESET_N low for 2–3.8 s.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or a button can be used to control RESET_N.

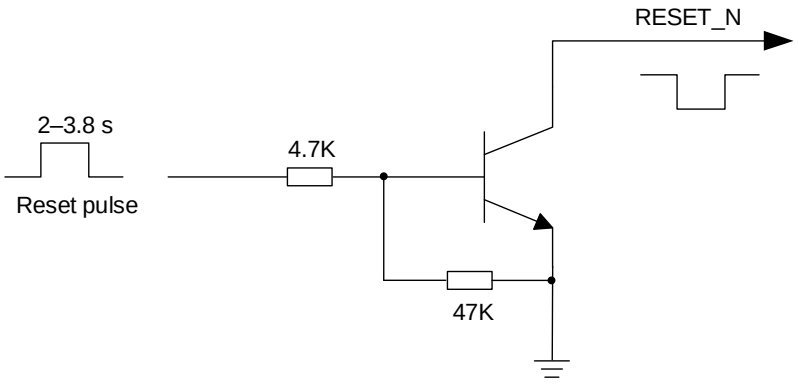


Figure 10: Reference Design of RESET_N with a Driver Circuit

Another way to control the RESET_N is to use a push button.

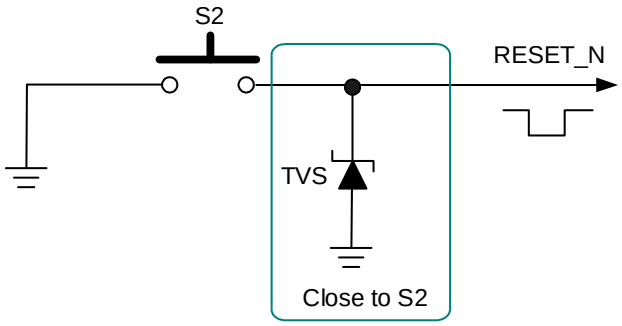


Figure 11: Reference Design of RESET_N with a Push Button

The reset timing is illustrated in the following figure.

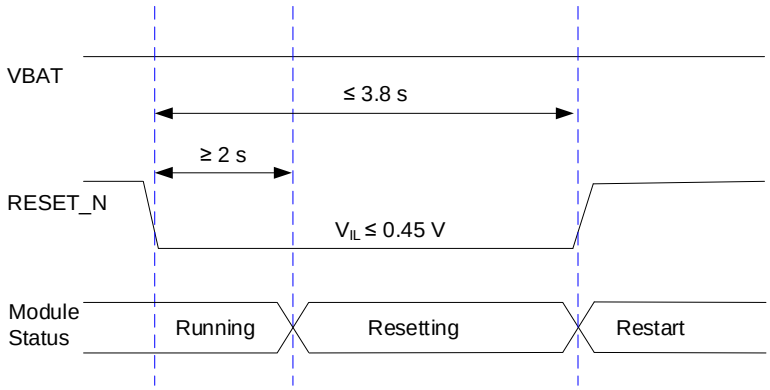


Figure 12: Reset Timing

NOTE

Ensure that there is no large capacitance on RESET_N.

3.8. PON_TRIG Interface

The module provides one PON_TRIG pin which is used to wake up the module from PSM. When the pin detects a rising edge and keeps at high level for at least 30 ms, the module wakes up from PSM.

Table 11: Pin Definition of PON_TRIG Interface

Pin Name	Pin No.	I/O	Description	Comment
PON_TRIG	96	DI	Wake up the module from PSM	Rising-edge triggered. Pulled-down by default. 1.8 V power domain. If unused, keep this pin open.

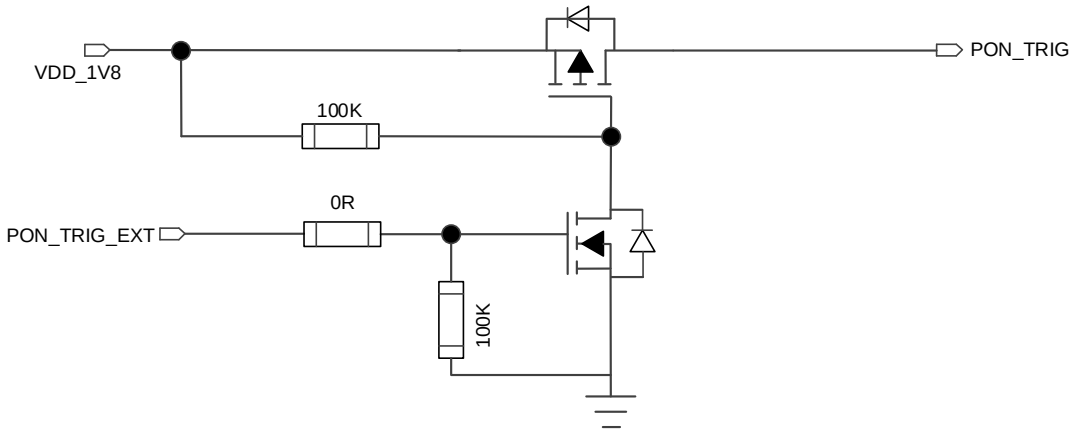


Figure 13: Reference Design of PON_TRIG

NOTE

VDD_1V8 is provided by an external LDO.

3.9. (U)SIM Interface

The module supports 1.8 V (U)SIM card only. The (U)SIM interface circuit meets ETSI and IMT-2000 requirements.

Table 12: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_DET	42	DI	(U)SIM card hot-plug detect	1.8 V power domain. If unused, keep this pin open.
USIM_VDD	43	PO	(U)SIM card power supply	Only 1.8 V (U)SIM card is supported.
USIM_RST	44	DO	(U)SIM card reset	1.8 V power domain.
USIM_DATA	45	DIO	(U)SIM card data	
USIM_CLK	46	DO	(U)SIM card clock	
USIM_GND	47		Specified ground for (U)SIM card	

The module supports (U)SIM card hot-plug via the USIM_DET pin, and both high-level and low-level

detections are supported. The function is disabled by default, and see **AT+QSIMDET** in ***document [3]*** for more details.

The following figure shows a reference design of (U)SIM interface with an 8-pin (U)SIM card connector.

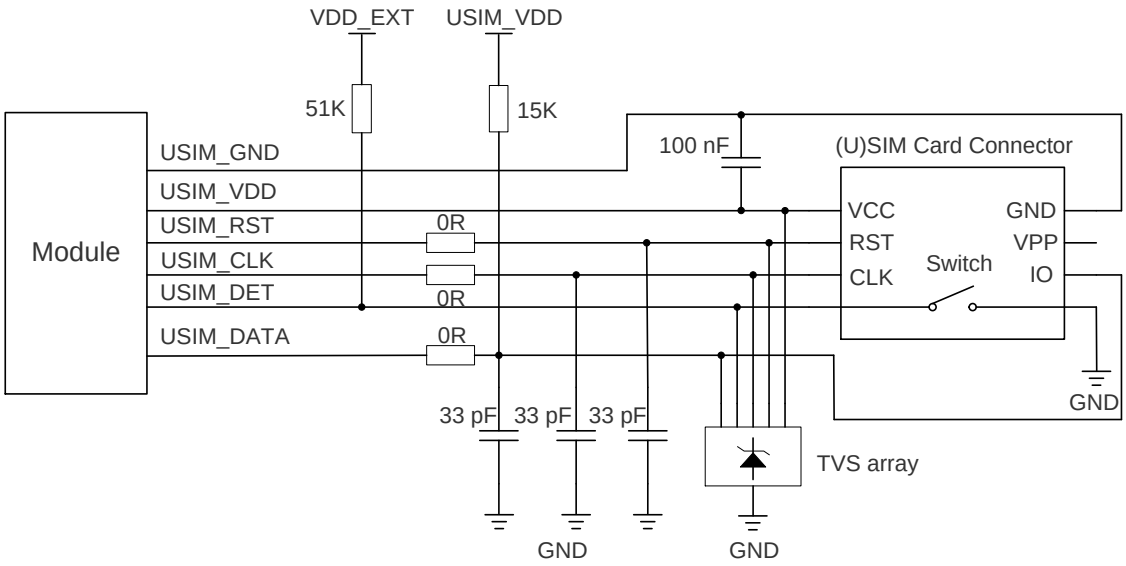


Figure 14: Reference Design of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

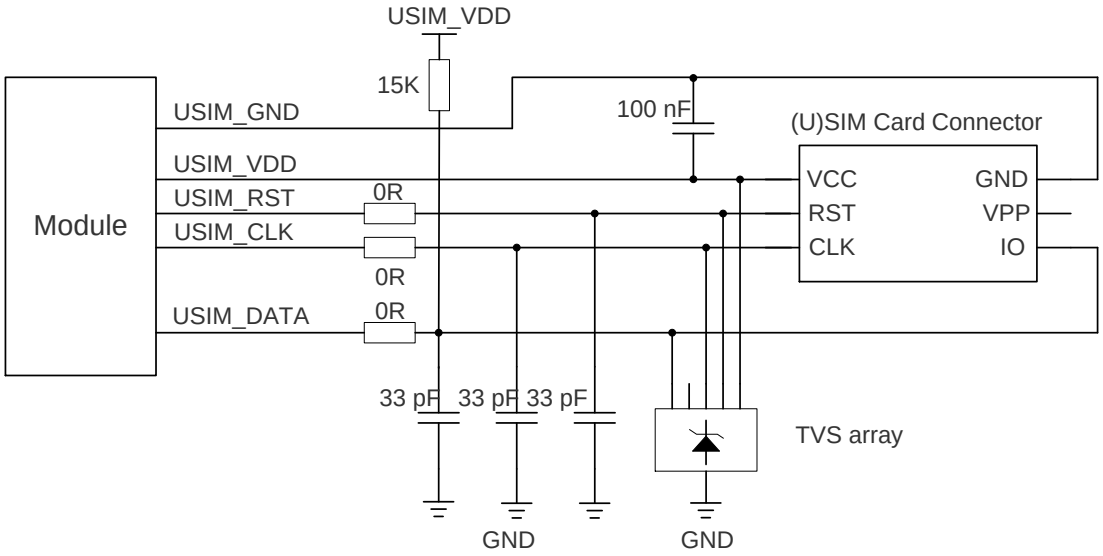


Figure 15: Reference Design of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design:

- Keep the placement of (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and power supply traces.
- Assure the ground trace between the module and the (U)SIM card connector short and wide. Keep the trace width of ground and USIM_VDD not less than 0.5 mm to maintain the same electric potential. Make sure the bypass capacitor between USIM_VDD and USIM_GND is less than 1 μF, and place it as close to (U)SIM card connector as possible. If the system ground plane is complete, USIM_GND can be connected to the system ground directly.
- To avoid crosstalk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground. USIM_RST should also be surrounded with ground.
- To offer good ESD protection, it is recommended to add a TVS array with parasitic capacitance not exceeding 15 pF. To facilitate debugging, it is recommended to reserve series resistors for the (U)SIM signals of the module. The 33 pF capacitors are used for RF filtering interference. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

3.10. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports operation at low-speed (1.5 Mbps), full-speed (12 Mbps) and high-speed (480 Mbps) modes.

The USB interface is used for AT command communication, data transmission[11], GNSS NMEA sentences output, software debugging and firmware upgrade. The following table shows the pin definition of USB interface.

Table 13: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Typical 5.0 V
USB_DP	9	AIO	USB differential data (+)	Require differential impedance of 90 Ω.
USB_DM	10	AIO	USB differential data (-)	
GND	3		Ground	

[11] It is not recommended to use USB for data communication, as this will increase the power consumption.

For more details about USB 2.0 specification, visit https://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade and software debugging in application designs. The following figure shows a reference design of USB interface.

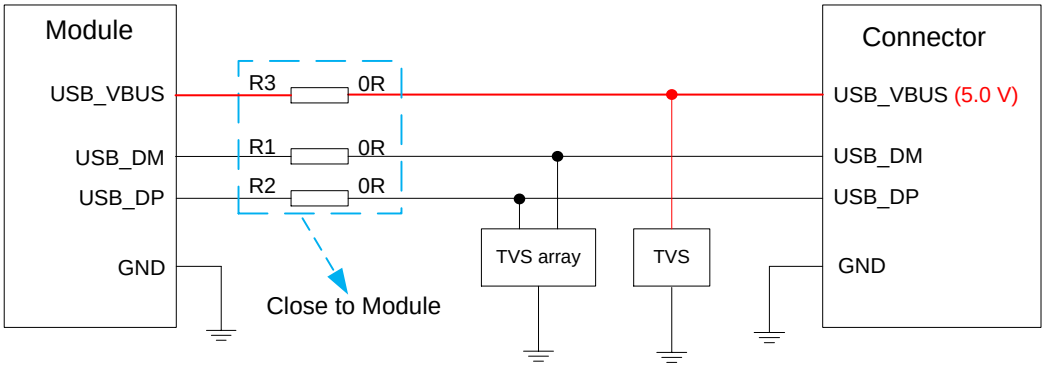


Figure 16: Reference Design of USB Interface

To ensure the integrity of USB data trace signal, resistors should be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

To meet USB 2.0 specification, comply with the following principles while designing the USB interface.

- It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection components might cause influences on USB data traces, so pay attention to the selection of the components. Typically, the stray capacitance should be less than 2 pF.
- Keep TVS components as close to the USB connector as possible.

NOTE

The USB interface supports slave mode only.

3.11. UART

The module provides three UART: the main UART, debug UART and the GNSS UART. Their features are outlined below:

- The main UART supports 9600, 19200, 38400, 57600, 115200, 230400, 460800 and 921600, 2000000, 2900000, 3000000, 3200000, 3686400, 4000000 bps baud rates, and the default baud rate is 115200 bps. It is used for data transmission and AT command communication, and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).
- The debug UART supports a fixed baud rate of 115200 bps, and is used for software debugging and log output.
- The GNSS UART supports 115200 bps baud rate by default, and is used for GNSS data and NMEA sentences output.

Table 14: Pin Definition of Main UART

Pin Name	Pin No.	I/O	Description	Comment
MAIN_DTR	30	DI	Main UART data terminal ready	1.8 V power domain. If unused, keep these pins open.
MAIN_RXD	34	DI	Main UART receive	
MAIN_TXD	35	DO	Main UART transmit	
MAIN_CTS	36	DO	Clear to send signal from the module	Connect to the MCU's CTS. 1.8 V power domain. If unused, keep the pin open.
MAIN_RTS	37	DI	Request to send signal to the module	Connect to the MCU’s RTS. 1.8 V power domain. If unused, keep the pin open.
MAIN_DCD	38	DO	Main UART data carrier detect	1.8 V power domain. If unused, keep these pins open.
MAIN_RI	39	DO	Main UART ring indication	

NOTE

AT+IPR can be used to set the baud rate of the main UART, and **AT+IFC** can be used to enable/disable the hardware flow control (the function is disabled by default). See ***document [3]*** for more details about these AT commands.

Table 15: Pin Definition of Debug UART

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	22	DI	Debug UART receive	1.8 V power domain. If unused, keep these pins open.
DBG_TXD	23	DO	Debug UART transmit	

Table 16: Pin Definition of GNSS UART

Pin Name	Pin No.	I/O	Description	Comment
GNSS_TXD	27	DO	GNSS UART transmit	BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain. If unused, keep this pin open.
GNSS_RXD	28	DI	GNSS UART receive	1.8 V power domain. If unused, keep this pin open.

NOTE

GNSS_TXD is a BOOT_CONFIG pin. Never pull it up before startup, otherwise the module cannot power up normally.

The module provides 1.8 V UART. A voltage-level translator should be used if your application is equipped with a 3.3 V UART. The voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended.

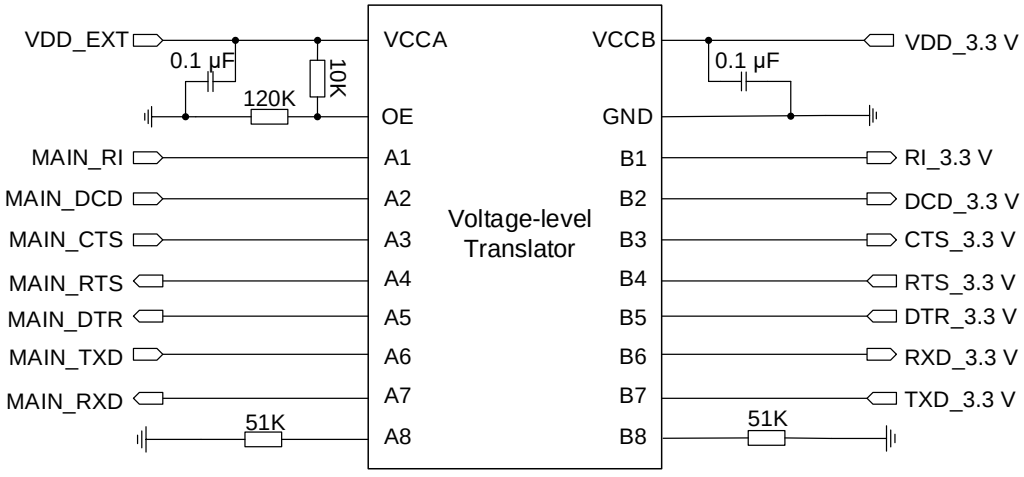


Figure 17: Main UART Reference Design (IC Solution)

Visit http://www.ti.com/ for more information.

Another example with transistor translation circuit is shown as below. For the design of circuits shown in dotted lines, refer to the solid lines, but pay attention to the direction of connection.

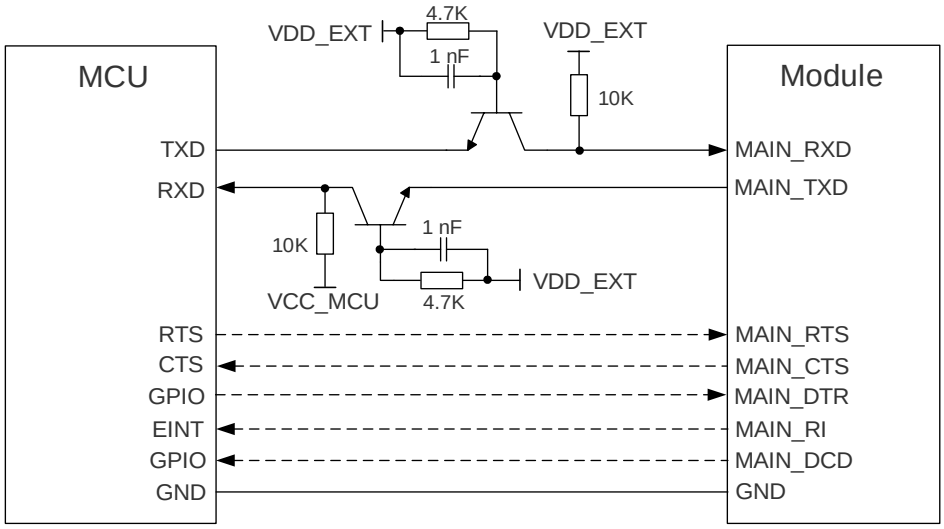


Figure 18: Main UART Reference Design (Transistor Solution)

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.
3. The level shifting circuit of debug UART and GNSS UART is similar to main UART.

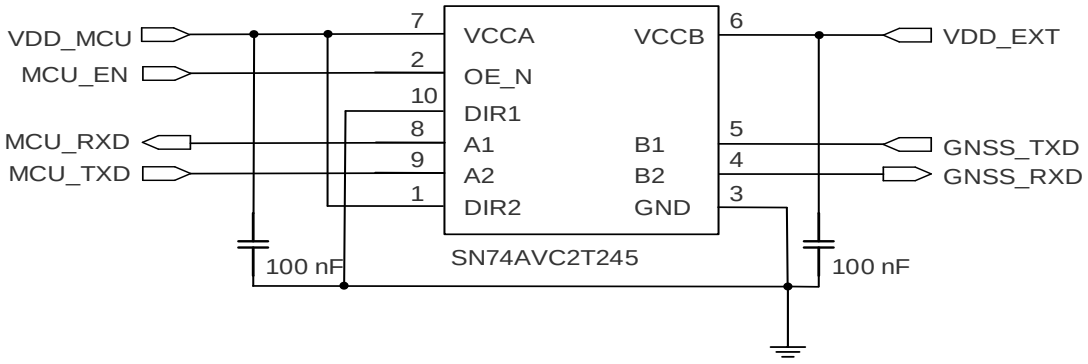


Figure 19: GNSS UART Reference Design (IC Solution Without Internal Pull-up)

NOTE

GNSS_TXD is a BOOT_CONFIG pin (pin 27), therefore the IC solution with pull-up circuit or transistor/MOSFET circuit is not applicable. It is recommended to adopt an IC solution without internal pull-up.

3.12. PCM and I2C Interfaces

The module provides one Pulse Code Modulation (PCM) digital interface and one inter-integrated circuit (I2C) interface which are used for VoLTE.

The following table shows the pin definition of the two interfaces which can be applied to audio codec design.

Table 17: Pin Definition of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_CLK	4	DO	PCM clock	1.8 V power domain. If unused, keep these pins open.
PCM_SYNC	5	DO	PCM data frame sync	
PCM_DIN	6	DI	PCM data input	
PCM_DOUT	7	DO	PCM data output	
I2C_SCL	40	OD	I2C serial clock (for external codec)	External pull-up resistors are required. 1.8 V only. If unused, keep these pins open.
I2C_SDA	41	OD	I2C serial data (for external codec)	

The following figure shows a reference design of PCM and I2C interfaces with an external codec IC.

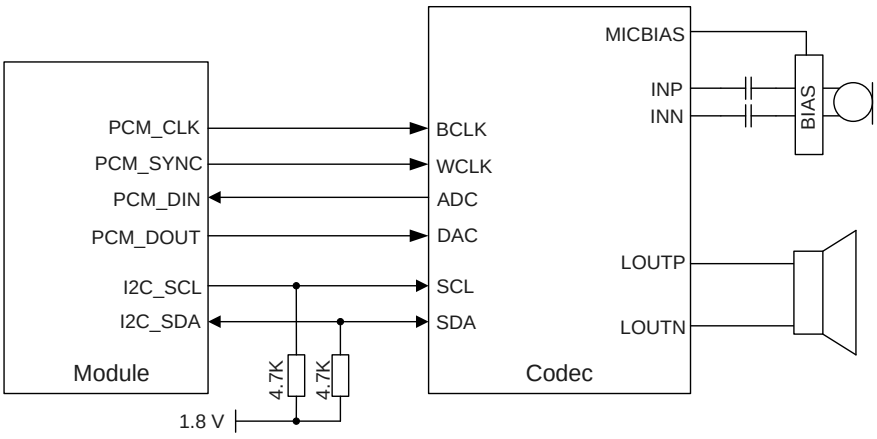


Figure 20: Reference Design of PCM and I2C Application with Audio Codec

3.13. Network Status Indication

The module provides one network status indication pin (NET_STATUS). The pin is used to drive a network status indication LED. The following tables describe the pin definition and logic level changes of NET_STATUS in different network activity status.

Table 18: Pin Definition of NET_STATUS

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	21	DO	Indicates the module's network activity status	1.8 V power domain. If unused, keep this pin open.

Table 19: Operating State of NET_STATUS

Pin Name	Logic Level Changes	Network Status
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing
	Always high	Voice calling

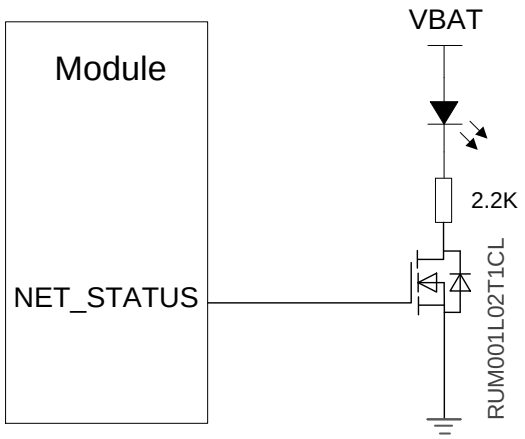


Figure 21: Reference Design of the Network Status Indicator

3.14. STATUS

The STATUS pin indicates the operation status of the module. It outputs high level when the module powers up.

Table 20: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicates the module's operation status	1.8 V power domain. If unused, keep this pin open.

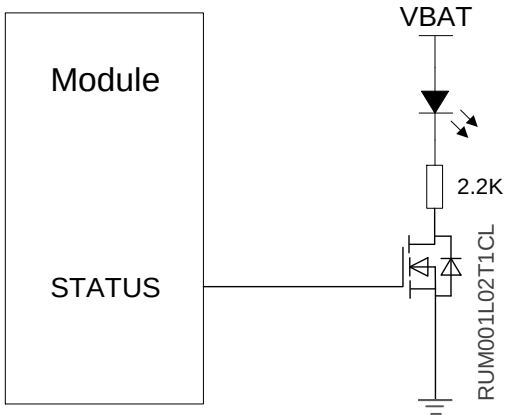


Figure 22: Reference Design of STATUS

3.15. MAIN_RI

AT+QCFG="risignaltype","physical" can configure MAIN_RI behavior. No matter on which port the URC is presented, the URC will trigger the behavior of MAIN_RI.

Table 21: Default Behaviours of MAIN_RI

State	Response
Idle	MAIN_RI keeps in high level.
URC	MAIN_RI outputs 120 ms low pulse when a new URC returns.

The default MAIN_RI pin behaviors can be configured flexibly by **AT+QCFG="urc/ri/ring"**. For more details about **AT+QCFG**, see ***document [4]***.g

NOTE

A URC can be output from the UART through configuration via **AT+QURCCFG**. For details about the AT command, see ***document [3]***.

3.16. USB_BOOT

UBM1-GL provides a USB_BOOT pin. During development or factory production, USB_BOOT can force the module to boot from USB interface for firmware upgrade.

Table 22: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module into emergency download mode.	1.8 V power domain. Active high. If unused, keep it open.

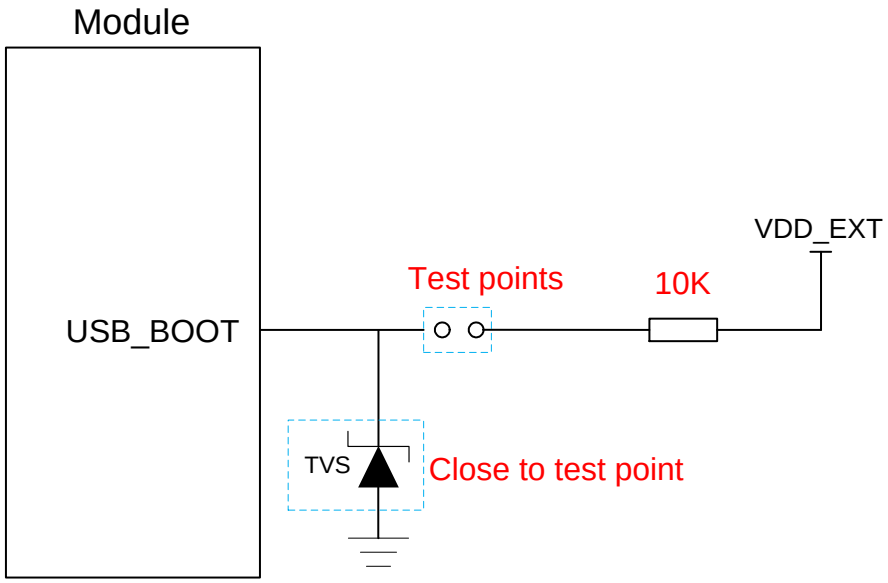


Figure 23: Reference Design of USB_BOOT Interface

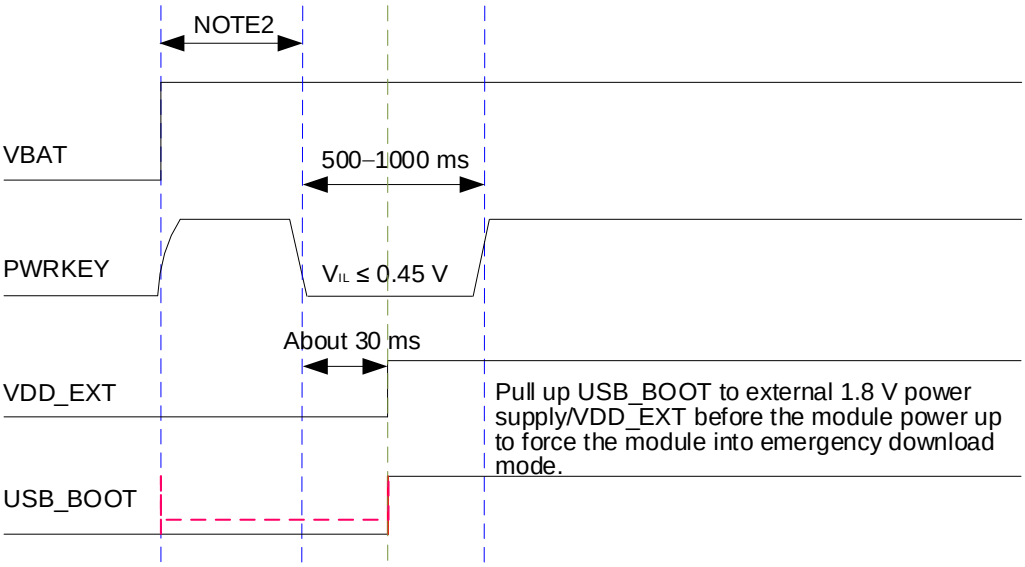


Figure 24: Timing for Turning on the Module with USB_BOOT

NOTE

1. It is recommended to reserve the above circuit design during application design.
2. Ensure that VBAT is stable before pulling down PWRKEY. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY is not less than 30 ms.
3. When using MCU to control the module entering emergency download mode, follow the above timing. Connecting the test points as shown in ***Figure 23*** can manually force the module to enter download mode.

3.17. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces but only one ADC interface can be used at a time since ADC1 connects directly to ADC0 inside the module.

AT+QADC=0 can be used to read the voltage value on the ADC being used. For more details about the AT command, see ***document [3]***.

To improve the accuracy of ADC voltage values, the traces of ADC should be surrounded with ground.

Table 23: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose ADC interface	Do not use ADC0 and ADC1 simultaneously.
ADC1	2	AI		

Table 24: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
Voltage Range	0.1	-	1.8	V
Resolution (LSB)	-	64.879	-	μV
Analog Bandwidth	-	500	-	kHz
Sample Clock	-	4.8	-	MHz
Input Resistance	10	-	-	MΩ

NOTE

1. It is prohibited to supply any voltage to ADC pin when VBAT is removed.
2. It is recommended to use resistor divider circuit for ADC application, and the divider resistor accuracy should be not less than 1 %.
3. Do not use ADC0 and ADC1 simultaneously, as ADC1 connects directly to ADC0 inside the module.

3.18. GPIO Interfaces

The module provides nine general-purpose input and output (GPIO) interfaces. **AT+QCFG="gpio"** can configure the status of GPIO pins. For more details about the AT command, see ***document [4]***.

Table 25: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GPIO1 [12]	25	DIO	General-purpose input/output	1.8 V power domain. If unused, keep these pins open.
GPIO2	26			
GPIO3	64			
GPIO4 [19]	65			
GPIO5	66			
GPIO6	85			
GPIO7	86			
GPIO8	87			
GPIO9	88			

[12] Pin 25 is a general-purpose IO by default. It can be multiplexed into fast shutdown interface with **AT+QCFG="fast/poweroff"**.

3.19. GRFC Interfaces

The module provides two generic RF control interfaces for the control of external antenna tuners.

Table 26: Pin Definition of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comments
GRFC1	83	DO	Generic RF controller	1.8 V power domain. If unused, keep this pin open.
GRFC2	84			BOOT_CONFIG. Do not pull it up before startup. 1.8 V power domain.

Table 27: Truth Table of GRFC Interfaces

GRFC1 Level	GRFC2 Level	Frequency Range (MHz)	Band
Low	Low	880–2180	B1, B2, B3, B4, B8, B25, B66
Low	High	791–894	B5, B18, B19, B20, B26, B27
High	Low	698–803	B12, B13, B28, B85
High	High	617–698	B71

NOTE

1. GRFC2 (pin 84) is a BOOT_CONFIG pin. Never pull it up before startup, otherwise the module cannot power on normally.

4 GNSS

4.1. General Description

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, Galileo and QZSS.

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, UBM1-GL GNSS engine is switched off. It has to be switched on via AT command. The module does not support concurrent operation of WWAN and GNSS. For more details about GNSS engine technology and configurations, see ***document [1]***.

4.2. GNSS Performance

Table 28: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Acquisition	Autonomous	-146	dBm
	Reacquisition	Autonomous	-157	dBm
	Tracking	Autonomous	-157	dBm
TTFF	Cold start @ open sky	Autonomous	31.01	s
		XTRA enabled	10.4	s
	Warm start @ open sky	Autonomous	30.58	s
		XTRA enabled	1.53	s
	Hot start @ open sky	Autonomous	1.6	s

		XTRA enabled	1.5	s
Accuracy	CEP-50	Autonomous @ open sky	2.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in application designs.

- Maximize the distance between GNSS antenna and main antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be away from the antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50 Ω characteristic impedance for ANT_GNSS trace.

See ***Chapter 5*** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

The module includes a main antenna interface and a GNSS antenna interface. The impedance of antenna ports is 50 Ω.

5.1. Main Antenna Interface

5.1.1. Pin Definition

Table 29: Pin Definition of Main Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance

5.1.2. Operating Frequency

Table 30: Operating Frequency of UBM1-GL Module

3GPP Band	Transmit	Receive	Unit
LTE HD-FDD B1	1920–1980	2110–2170	MHz
LTE HD-FDD B2	1850–1910	1930–1990	MHz
LTE HD-FDD B3	1710–1785	1805–1880	MHz
LTE HD-FDD B4	1710–1755	2110–2155	MHz
LTE HD-FDD B5	824–849	869–894	MHz
LTE HD-FDD B8	880–915	925–960	MHz
LTE HD-FDD B12	699–716	729–746	MHz

LTE HD-FDD B13	777–787	746–756	MHz
LTE HD-FDD B18	815–830	860–875	MHz
LTE HD-FDD B19	830–845	875–890	MHz
LTE HD-FDD B20	832–862	791–821	MHz
LTE HD-FDD B25	1850–1915	1930–1995	MHz
LTE HD-FDD B26	814–849	859–894	MHz
LTE HD-FDD B27	807–824	852–869	MHz
LTE HD-FDD B28	703–748	758–803	MHz
LTE HD-FDD B66	1710–1780	2110–2180	MHz
LTE HD-FDD B85	698–716	728–746	MHz

5.1.3. Reference Design

A reference design of main antenna interface is shown as below. It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (R1/C1/C2) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

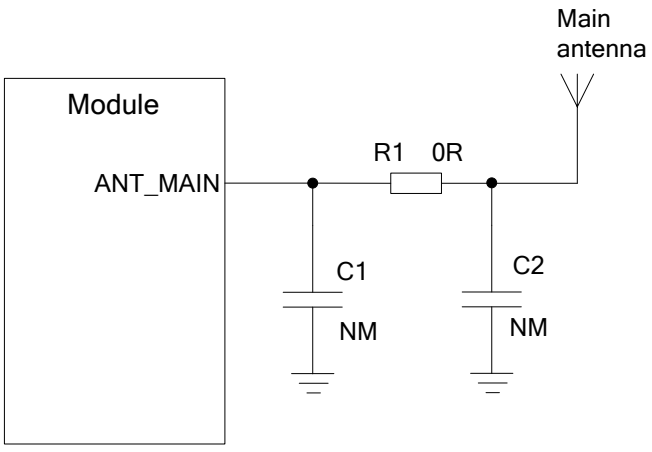


Figure 25: Reference Design of Main Antenna Interface

5.2. GNSS Antenna Interface

5.2.1. Pin Definition

Table 31: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50 Ω impedance. If unused, keep this pin open.

5.2.2. GNSS Operating Frequency

Table 32: GNSS Operating Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BDS	1561.098 ±2.046	MHz
QZSS	1575.42 ±1.023	MHz

5.2.3. Reference Design

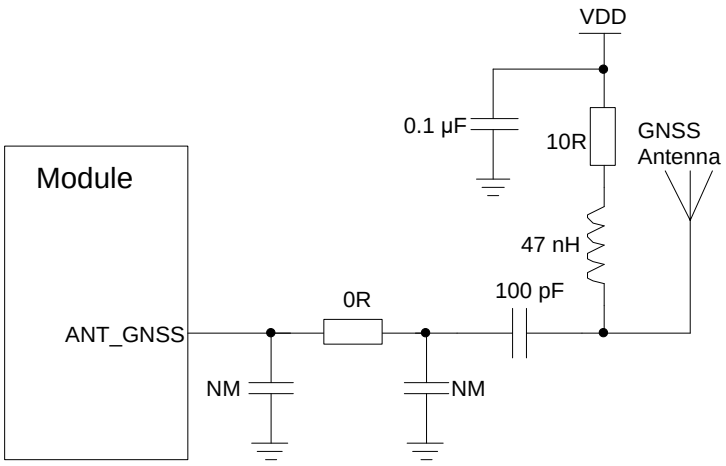


Figure 26: Reference Design of GNSS Antenna Interface

NOTE

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

5.3. RF Routing Guidelines

For your PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

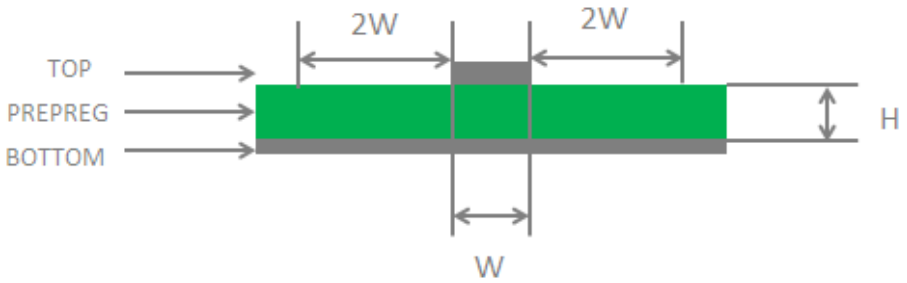


Figure 27: Microstrip Design on a 2-layer PCB

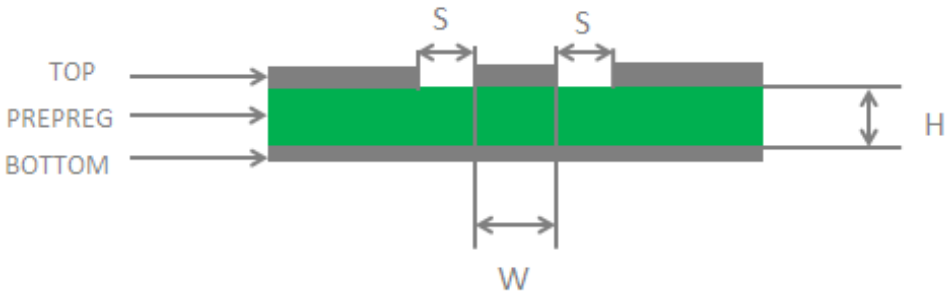


Figure 28: Coplanar Waveguide Design on a 2-layer PCB

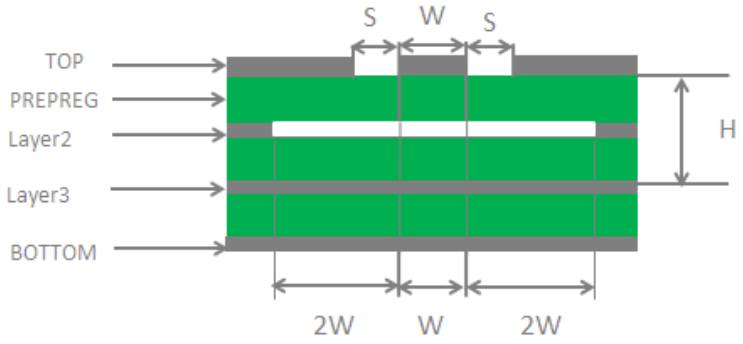


Figure 29: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

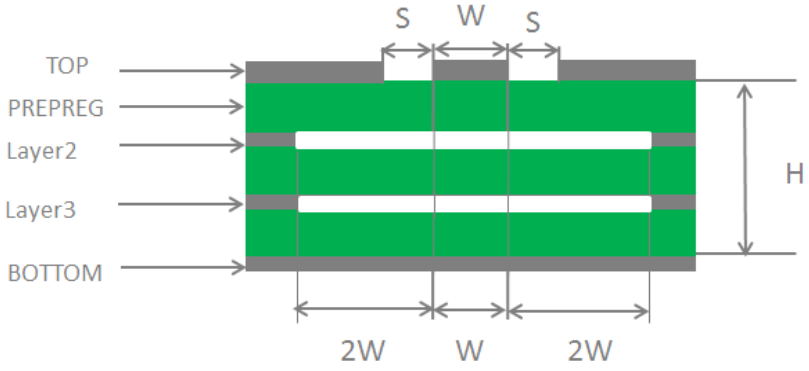


Figure 30: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.

- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [5]***.

5.4. Antenna Installation

5.4.1. Requirements for Antenna Design

Table 33: Requirements for Antenna Design

Antenna Type	Requirements
GNSS [13]	Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: ≤ 2 (Typ.) Passive antenna gain: > 0 dBi Active antenna noise figure: < 1.5 dB Active antenna gain: > 0 dBi Active antenna embedded LNA gain: < 17 dB
LTE	VSWR: ≤ 2 Efficiency: > 30 % Max. Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: ● **< 1 dB:** LB (<1 GHz) ● **< 1.5 dB:** MB (1–2.3 GHz)

[13] It is recommended to use a passive GNSS antenna when LTE HD-FDD B13 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.4.2. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connectors provided by Hirose.

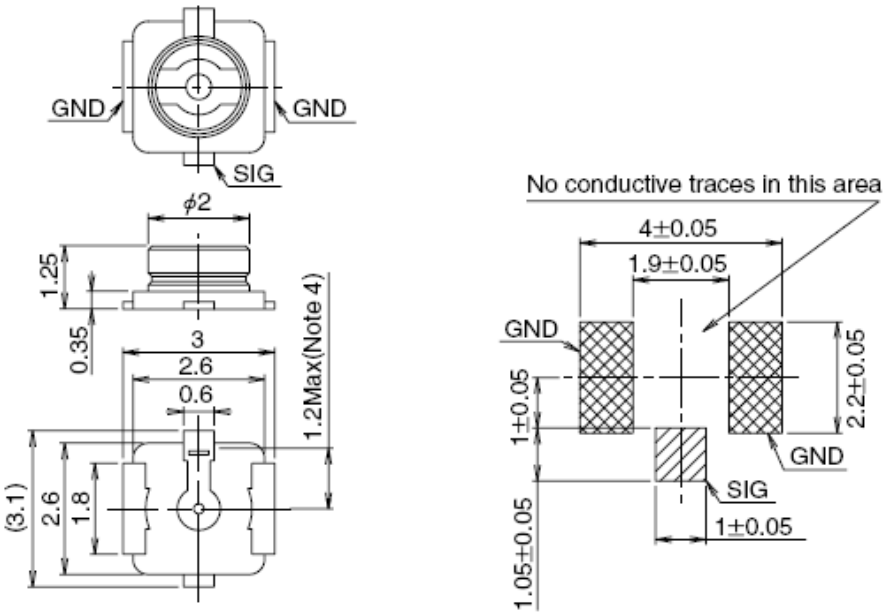


Figure 31: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

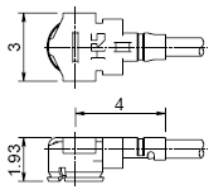
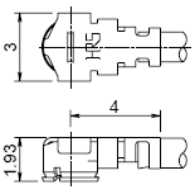
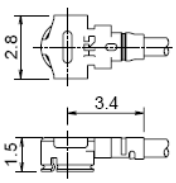
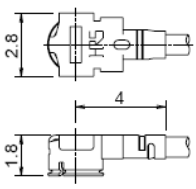
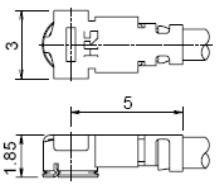
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 32: Specifications of Mated Plugs

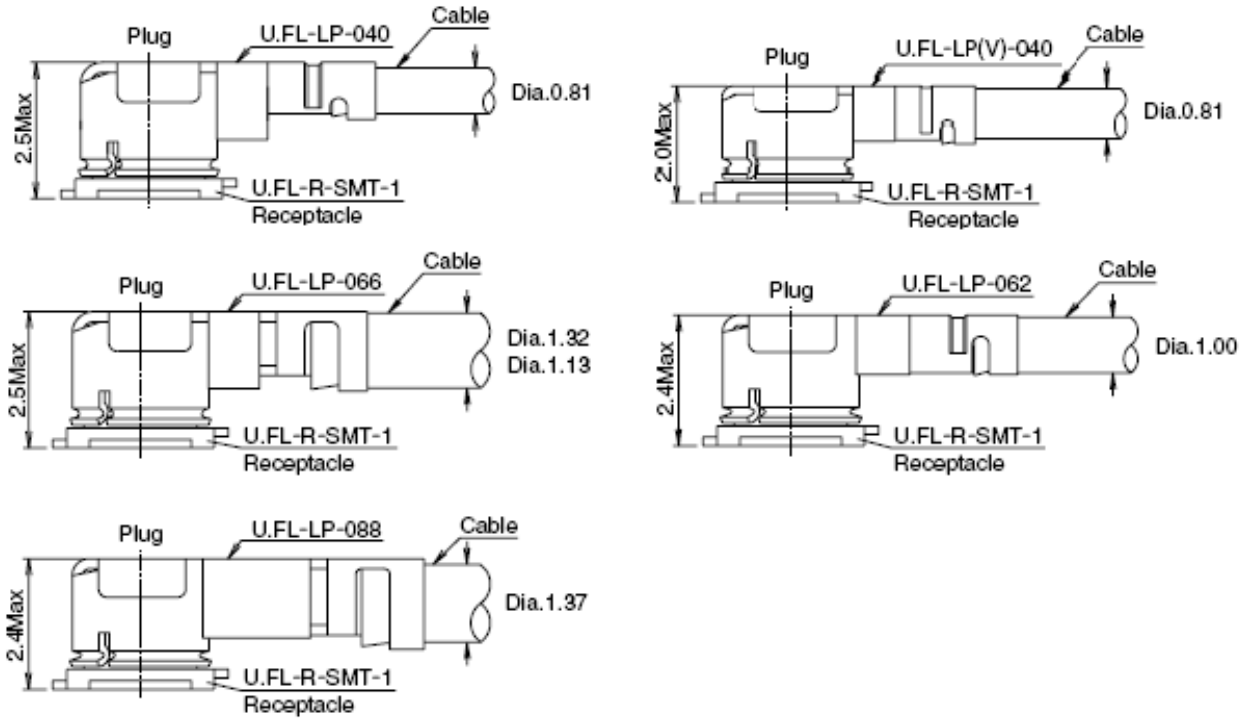


Figure 33: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 34: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_BB	-0.5	6.0	V
VBAT_RF	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Voltage at Digital Pins	-0.3	2.09	V

6.2. Power Supply Ratings

Table 35: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB/ VBAT_RF	The actual input voltages must be kept between the minimum	2.6 [14]	3.3	4.8	V

[14] For every VBAT transition/re-insertion from 0 V, the minimum power supply voltage should be higher than 2.7 V. After the module starts up normally, the minimum safety voltage is 2.6 V. To ensure full functionality mode, the minimum power supply voltage should be higher than 2.8 V.

		and the maximum values.				
I_{VBAT}	Peak power consumption	In LTE Cat M1 transmission modes	-	0.8	1.0	A
USB_VBUS	USB connection detection		4.0	5.0	5.25	V

6.3. Operating and Storage Temperatures

Table 36: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [15]	-35	+25	+75	ºC
Extended Temperature Range [16]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

6.4. Power Consumption

6.4.1. Power Consumption

Table 37: UBM1-GL Power Consumption (3.3 V Power Supply, Room Temperature)

Description	Conditions	Average	Unit
Leakage	Power-off @ USB and UART disconnected	14	μA

[15] Within the operating temperature range, the module meets 3GPP specifications.

[16] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice*, SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

PSM [17]	Power Saving Mode	4	μA
Rock Bottom	**AT+CFUN=0** @ Sleep mode	0.53	mA
Sleep Mode (USB disconnected)	LTE Cat M1 DRX = 1.28 s	1.7	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	0.577	mA
Idle Mode (USB disconnected)	LTE Cat M1 DRX = 1.28 s	20	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	19.57	mA
LTE Cat M1 data transfer (GNSS OFF)	B1 @ 20.66 dBm	200.47	mA
	B2 @ 20.81 dBm	202.12	mA
	B3 @ 21.24 dBm	199.57	mA
	B4 @ 20.82 dBm	197.79	mA
	B5 @ 21.12 dBm	219.9	mA
	B8 @ 21.03 dBm	209.96	mA
	B12 @ 20.67 dBm	202.55	mA
	B13 @ 20.92 dBm	225.42	mA
	B18 @ 21.02 dBm	214.87	mA
	B19 @ 20.95 dBm	216.17	mA
	B20 @ 20.96 dBm	214.52	mA
	B25 @ 21.02 dBm	203.86	mA
	B26 @ 21.06 dBm	218.97	mA
	B27 @ 20.8 dBm	212.89	mA
	B28A @ 20.89 dBm	210.15	mA

[17] The module's power consumption in PSM is much lower than that in power-off mode due to the following two designs:

- More internal power supplies are powers off in PSM.
- The internal clock frequency is reduced in PSM.

The module's USB and UART are disconnected and GSM network (if available) does not support PSM.

	B28B @ 21 dBm	217.13	mA
	B66 @ 21.03 dBm	198.63	mA
	B85 @ 21 dBm	203.36	mA

6.4.2. GNSS Power Consumption

Table 38: GNSS Power Consumption (3.3 V Power Supply, Room Temperature)

Description	Conditions	Typ.	Unit
Acquisition (**AT+CFUN=0**)	Cold start @ Instrument	76.74	mA
	Hot start @ Instrument	74.04	mA
	Warm start @ Instrument	76.19	mA
	Lost state @ Instrument	76.05	mA
Tracking (**AT+CFUN=0**)	Instrument Environment @ Passive Antenna	23.14	mA
	Open Sky @ Real network, Passive Antenna	26.352	mA
	Open Sky @ Real network, Active Antenna	27.463	mA

6.5. Tx Power

Table 39: Conducted Tx Power

Frequency Bands	Max. Tx Power	Min. Tx Power
LTE HD-FDD B1/B2/B3/B4/B5/B8/B12/B13/B18/ B19/B20/B25/B26/B27/B28/B66/B71/B85	21 dBm +1.7/-3 dB	< -39 dBm

6.6. Rx Sensitivity

Table 40: Conducted Rx Sensitivity

Mode	Band	Primary	Diversity	Receiving Sensitivity (dBm)	
				Cat M1/3GPP	Cat NB2
LTE	LTE HD-FDD B1	Supported	-	-108/-102.3	-
	LTE HD-FDD B2			-108.4/-100.3	
	LTE HD-FDD B3			-108.4/-99.3	
	LTE HD-FDD B4			-108/-102.3	
	LTE HD-FDD B5			-107.6/-100.8	
	LTE HD-FDD B8			-108/-99.8	
	LTE HD-FDD B12			-108.6/-99.3	
	LTE HD-FDD B13			-107/-99.3	
	LTE HD-FDD B18			-108/-102.3	
	LTE HD-FDD B19			-108/-102.3	
	LTE HD-FDD B20			-108/-99.8	
	LTE HD-FDD B25			-108.2/-100.3	
	LTE HD-FDD B26			-108.2/-100.3	
	LTE HD-FDD B27			-108.4/-100.8	
	LTE HD-FDD B28			-106.8/-100.8	
	LTE HD-FDD B66			-107.8/-101.8	
	LTE HD-FDD B71			-	
	LTE HD-FDD B85			-108.4/-99.3	

6.7. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, it is imperative to adopt proper ESD countermeasures and handling methods. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 41: Electrostatic Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±6	±8	kV
Main/GNSS Antenna Interfaces	±5	±6	kV

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

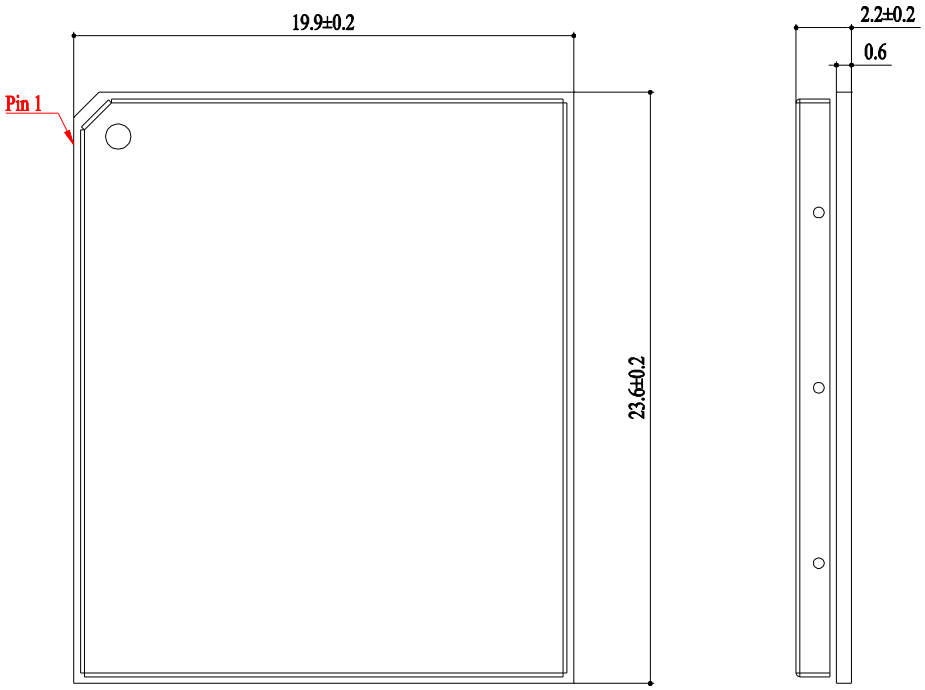


Figure 34: Module Top and Side Dimensions

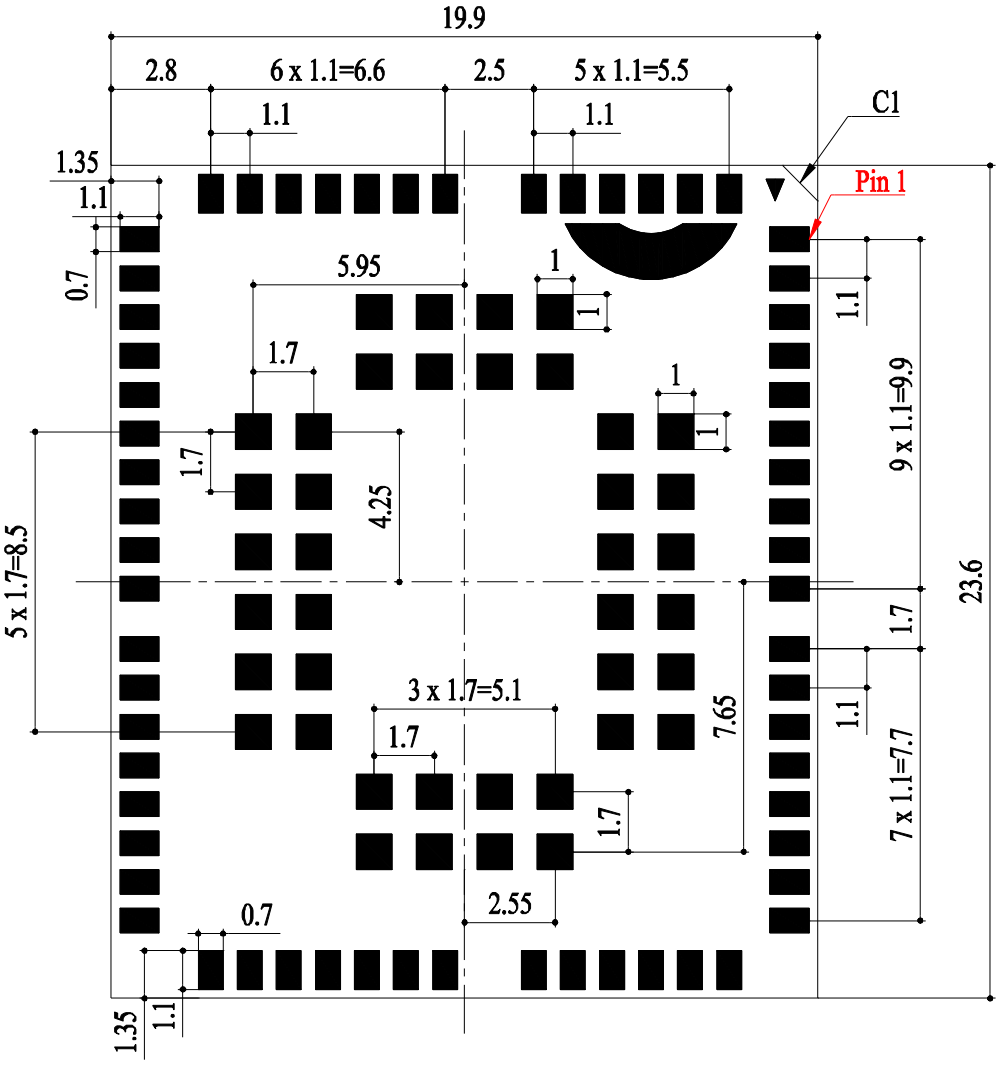


Figure 35: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

7.2. Recommended Footprint

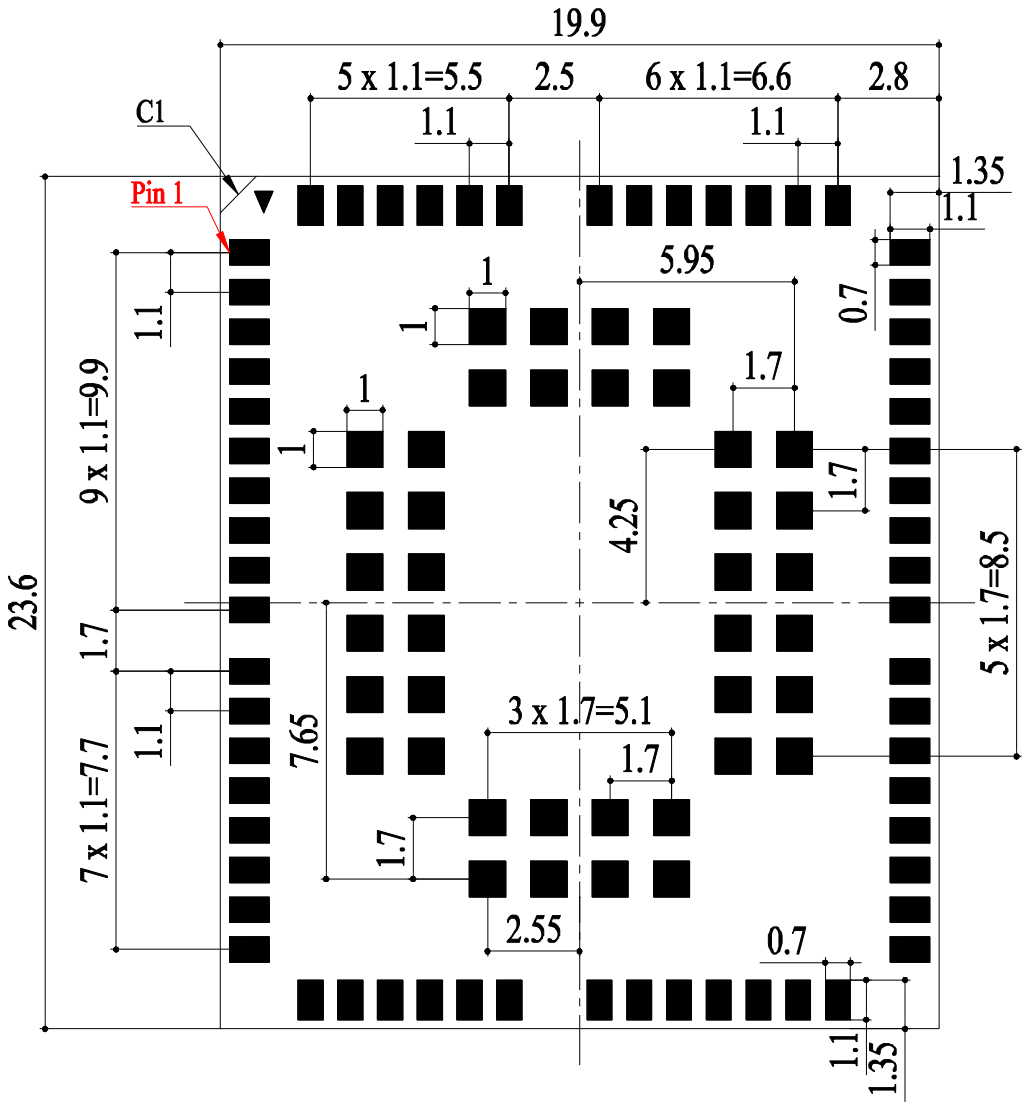


Figure 36: Recommended Footprint (Top View)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

Figure 37: Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Ubicquia.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [18] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[18] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [6]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

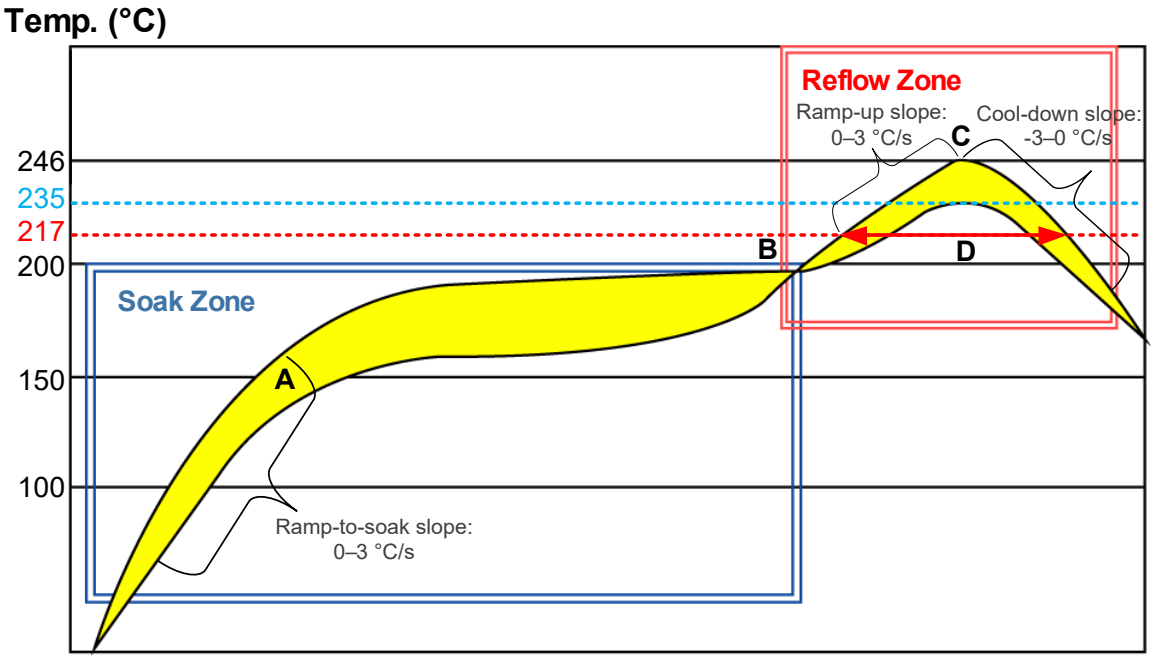


Figure 38: Recommended Reflow Soldering Thermal Profile

Table 42: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217°C)	40–70 s
Max Temperature	235–246 °C
Cool-down Slope	-3–0 °C/s
Reflow Cycle	
Max Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Due to the complexity of the SMT process, please contact Ubicquia Technical Supports in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [6]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1.Carrier Tape

Dimension details are as follow:

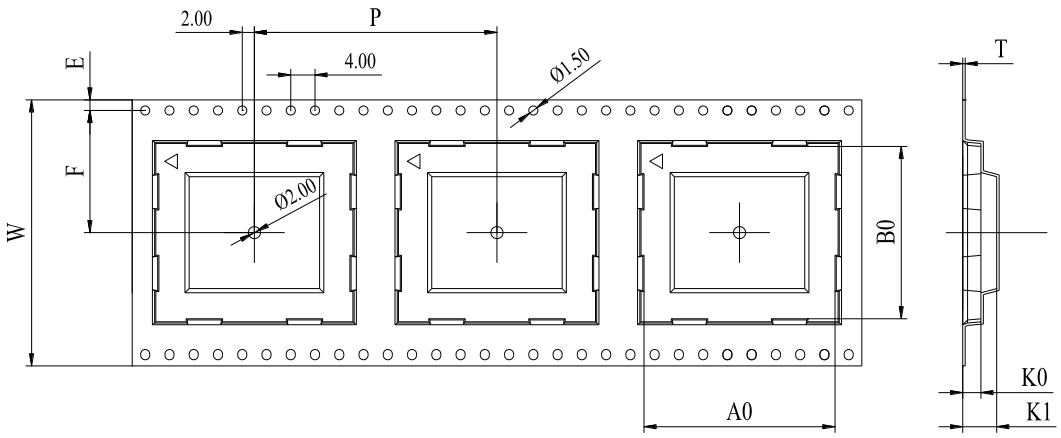


Figure 39: Carrier Tape Dimension Drawing

Table 43: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	20.2	24	3.15	6.65	20.2	1.75

8.3.2. Plastic Reel

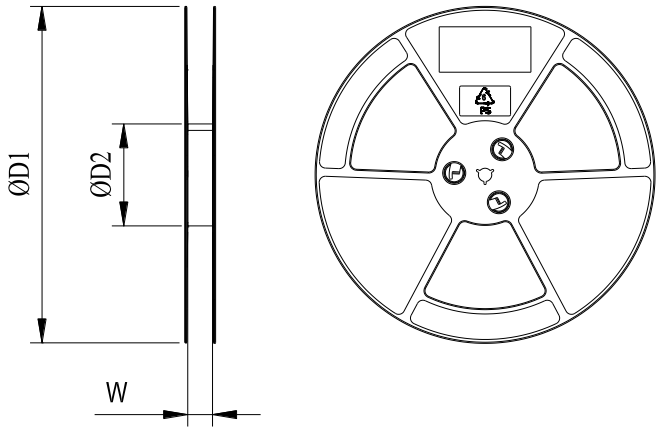


Figure 40: Plastic Reel Dimension Drawing

Table 44: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

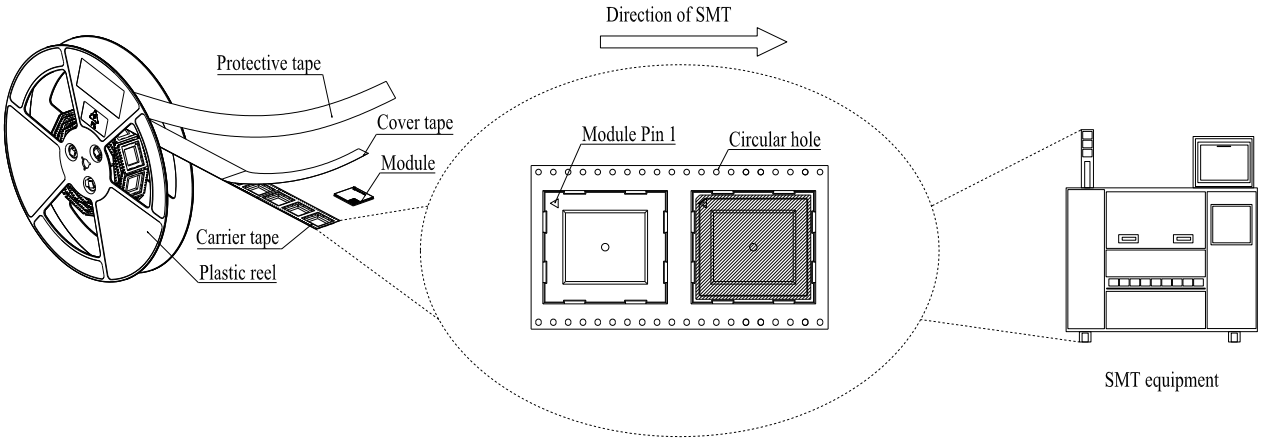
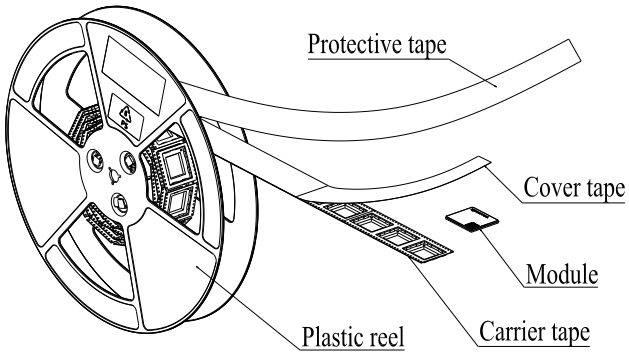


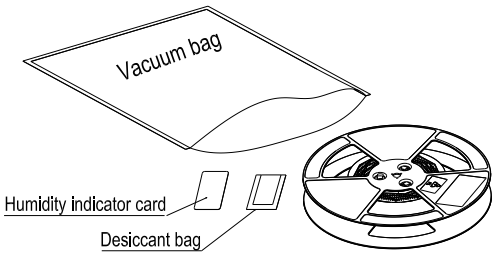
Figure 41: Mounting Direction

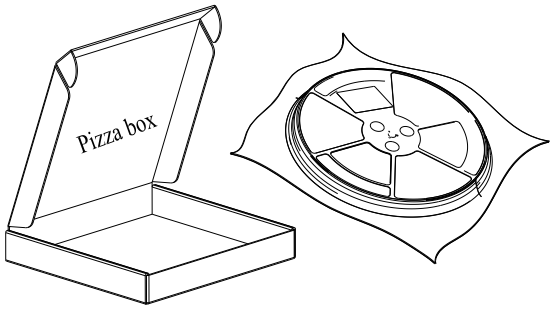
8.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 1000 modules.

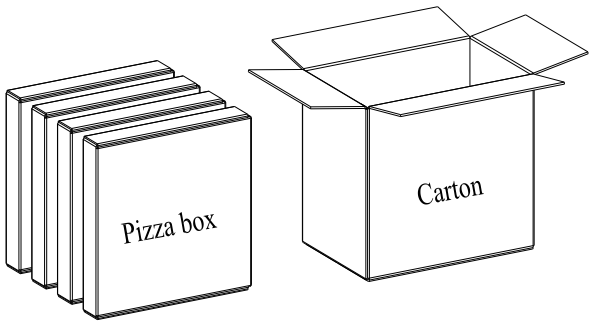


Figure 42: Packaging Process

Table 45: Packaging Specifications

MOQ for MP	Minimum Package: 250	Minimum Package × 4 = 1000
250	Size: 370 mm × 350 mm × 56 mm Net Weight: 0.61 kg Gross Weight: 1.35 kg	Size: 380 mm × 250 mm × 365 mm Net Weight: 2.45 kg Gross Weight: 6.28 kg

9 Appendix A References

Table 46: Related Documents

Document Name
[1] Ubicquia_UBM1-GL_Series_GNSS_Application_Note
[2] Ubicquia_UMTS&LTE_EVB_User_Guide
[3] Ubicquia_UBM1-GL_Series_AT_Commands_Manual
[4] Ubicquia_UBM1-GL_Series_QCFG_AT_Commands_Manual
[5] Ubicquia_RF_Layout_Application_Note
[6] Ubicquia_Module_SMT_Application_Note

Table 47: Terms and Abbreviations

Abbreviation	Description
ASM	Antenna Switch Modules
bps	Bits per second
CHAP	Challenge Handshake Authentication Protocol
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DTR	Data Terminal Ready
e-I-DRX	Extended Idle Mode Discontinuous Reception
EPC	Evolved Packet Core
ESD	Electrostatic Discharge

FDD	Frequency Division Duplex
GMSK	Gaussian Minimum Shift Keying
HSS	Home Subscriber Server
I2C	Inter-Integrated Circuit
I/O	Input/Output
LED	Light Emitting Diode
LDO	Low-dropout Regulator
LNA	Low Noise Amplifier
LPF	Low-Pass Filter
LTE	Long Term Evolution
MO	Mobile Originated
MOQ	Minimum Order Quantity
MT	Mobile Terminated
PA	Power Amplifier
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PMIC	Power Management IC
PPP	Point-to-Point Protocol
PSM	Power Saving Mode
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SAW	Surface Acoustic Wave
SMS	Short Message Service

TX	Transmit
UL	Uplink
UE	User Equipment
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-Level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
$V_I$max	Absolute Maximum Input Voltage
$V_I$min	Absolute Minimum Input Voltage
V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WWAN	Wireless Wide Area Network