

BT Qualification
QDID: 52727

FCC ID: 2AE2I-ACI810700S

ACI810700S-BLE-MD module specification

With 128KBytes In-system programmable flash memory

Version :V1.6

Revision History

Date	Revision Content	Revised By	Version
2015/12/26	Initial released	David Liao	V1.0
2016/01/18	Revise function Block	David Liao	V1.1
2016/01/24	Revise General Description, Feature Addition BTLE Certification QDID Addition packing information .Trav/Vacuum bag	David Liao	V1.2
2016/03/02	Addition FCC module with shielding case information	David Liao	V1.3
2016/04/06	Revise TX Power Range, addition FCC ID	David Liao	V1.4
2016/04/14	Addition FCC STATEMENT	David Liao	V1.5
2016/05/18	change the specified output power to 0 dBm follow FCC	David Liao	V1.6

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General Description

A8107 SiP (System-in-Package) is a high performance and low cost 2.4GHz FSK/GFSK SiP wireless transceiver. With in SiP fraction-N synthesizer, it can support the application of data rate from 5Kbps to 2Mbps and frequency hopping system and it is designed for Bluetooth Low Energy (Bluetooth 4.0 Single mode). It is a Bluetooth smart SiP. This SiP integrates high speed pipeline 8051 MCU, 128K Bytes In-system programmable flash memory, 8KB SRAM, various powerful functions and excellent performance of a leading 2.4GHz FSK/GFSK RF transceiver. It can be operated with wide voltage from 2.0V ~ 3.6V. There are 2 types of A8107 SiP. One is A8107F7000 which needs external crystal (16MHz and 32.768KHz), another is A8107F7001 which doesn't need any crystal. A8107 SiP has 128K bytes flash that supports AES128 engine and CCM, And support **transparent & Command mode or iBeacon ,MESH, custom mode** ,Also support **Upgrades Over the Air without Additional Flash** ;For details about register setting, please refer to another document A8107 Datasheet

Application

- Consumer electronics
- Mobile phone accessories
- Sports & Fitness equipment
- HID applications
- Home Automation and Lighting Control
- Alarm and Security
- Electronic Shelf Labeling
- Proximity Tags
- Medical and Healthcare
- Remote Controls
- Wireless Sensor Networks



Feature

- Bluetooth v4.2 Compliant Protocol Stack for Single-Mode BLE Module
- A8107F7000 SIP Chip package size (LGA8x8, 40 pins).
- Single-chip BLE SoC, Integrated BLE radio & High performance pipeline complicated 8051
- Complete BLE protocol stack and application profiles, Ability to be **BLE Central or Peripheral mode**
- **BLE iBeacon ,MESH, custom profile**, Also support **BLE +2.4G proprietary dual mode**.
- Operation clock: 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of crystal oscillator.
- 128KB Flash memory with copy protection, 8KB SARM
- UART, I²C, SPI serial communication
- Three 16/8-bit counter/timers
- Four Channel PWM
- Watchdog timer
- Sleep timer
- In-Circuit Debugger
- In-System programming/ In-Application programming
- 24 GPIO
- RX current consumption with MCU in operation mode: 17mA
- TX current consumption with MCU in operation mode (15mA @ 0dBm,).
- Deep sleep current (0.8 uA)
- Low sleep current (3 uA)
- Frequency band: 2400 – 2483MHz.
- FSK and GFSK modulation
- High sensitivity:
 - ◆ -96dBm at 500Kbps data rate
 - ◆ -92dBm at 1Mbps data rate
 - ◆ -90dBm at 2Mbps data rate
- Programmable data rate 5K ~ 2Mbps.
- Fast settling time synthesizer for frequency hopping system.
- Built-in thermal sensor for monitoring relative temperature.
- Built-in one channel 8-bits ADC for external analog voltage (0V ~ 1.2V).
- Built-in eight channels 12-bits ADC for general purpose analog input (0V ~ 1.8 V).
- Built-in Low Battery Detector.
- Support 16MHz crystal
- Easy to use.
 - ◆ Change frequency channel by ONE register setting.
 - ◆ 8-bits Digital RSSI for clear channel indication.
 - ◆ Auto RSSI measurement.
 - ◆ Auto WOR (wake up when receive RX packet).
 - ◆ Auto WOT (wake up to transmit TX packet).
 - ◆ Auto Calibrations.
 - ◆ Auto IF function.
 - ◆ Auto Frequency Compensation.
 - ◆ Auto CRC Check.
 - ◆ Separated 64 bytes RX and TX FIFO.
 - ◆ **Over the Air Secure Firmware Upgrade**

FCC Certification only refers to the version with integrated antenna and the shielding

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Electrical Specification

Item	Specification	Remark
Standard	Bluetooth	BTLE V4.2
Data Encryption	AES128 engine and CCM	
Antenna Type	Without Antenna & integrated Print circuit board antenna	
Supply voltage	2.0V~3.6V	
Current consumption (MCU only, RF in sleep mode)	0.8uA @Deep Sleep mode 3.0uA @Sleep(WOR/TWOR off) 5.0uA @Sleep (WOR /TWOR wake) 2.5mA @Normal	typical
Current Consumption (RF with MCU in normal mode)	3mA @Stand-by mode 12.5mA @PLL mode 17mA @Rx mode 15mA @Tx mode	typical
Frequency	2402 – 2480 MHz	ISM band
Transmit output power	0 dBm @ room temperature	Typical <u>Annotation 1</u>
Rx sensitivity	-92 dBm (typical) @ 1Mbps mode	BER \leq 1E-3
Modulation	GFSK	
Interface	7 pin 1.27mm header X 1 9 pin 1.27mm header X 1 10 pin 1.27mm header X 1	
Dimension		
ACI810700S-BLE-MD	14.5mm(L) x 12.5mm(W) mm ² without Antenna	
ACI810700S-BLE-MD+ANT	21.3mm(L) x 12.5mm(W) mm ² with integrated PCB Antenna	
ACI810700S-BLE-MD+Shielding	21.3mm(L) x 12.5mm(W) mm ² with integrated Shielding case Shielding case height:2.75mm and PCB thickness is 0.8mm	
Operating temperature	-40 ~ 85 °C	

Absolute Maximum Ratings

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD)	GND	-0.3 ~ 3.6	V
Digital IO pins range	GND	-0.3 ~ VDD+0.3	V
Voltage on the analog pins range	GND	-0.3 ~ 2.1	V
Input RF level		14	dBm
Storage Temperature range		-55 ~ 125	°C
ESD Rating	HBM	\pm 5K	V
	MM	\pm 200	V

*Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.

*Device is Moisture Sensitivity Level III (MSL 3).

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Electrical Specification in detail

(Ta=25°C, REGI = 3.3V, internal regulator voltage = 1.8V, unless otherwise noted)

Parameter	Description	Min.	Type	Max.	Unit
General					
Operating Temperature		-40		85	°C
Supply Voltage (VDD)	Regulator supply input	2.0		3.6	V
Current Consumption (MCU in stop mode and RF in sleep mode)	PM1 with Sleep timer		5		uA
	PM2 with Sleep timer		5		uA
	PM3 with Sleep timer		3		uA
	PM3 without Sleep timer		0.9		uA
Current Consumption (MCU in normal mode) MCU Clock @ 16MHz	Standby Mode	3			mA
	PLL Mode		12.5		mA
	RX Mode (AGC Off)		16.5		mA
	RX Mode (AGC On)		17		mA
	TX Mode (@0dBm output)		15		mA
	TX Mode (@6dBm output)		20		mA
Synthesizer block					
Crystal settling time	PM2 to Standby A8107F7000SQ8A(External Xtal,49US) A8107F7001SQ8A(Internal Xtal of SiP)		0.6/0.9		ms
Crystal frequency			16		MHz
Crystal tolerance			±2		ppm
Crystal Load Capacitance			1		pF
Crystal ESR				80	ohm
PLL settling time	Standby to PLL		75		μs
Transmitter					
Carrier Frequency		2400		2483.5	MHz
Maximum Output Power		-10	0		dBm
RF Power Control Range			20		dB
Out Band Spurious Emission	30MHz~1GHz 1GHz~12.75GHz 1.8GHz~ 1.9GHz 5.15GHz~ 5.3GHz			-36 -30 -47 -47	dBm
Frequency deviation	500Kbps 1M 2M		186K 250K 500K		Hz
Data rate		4K		2M	bps
TX settling time	Standby to TX		120		μs
Receiver					
Receiver sensitivity @ BER = 0.1%	Data rate 2M (F _{IF} = 2MHz) Data rate 1M (F _{IF} = 1MHz) Data rate 500K (F _{IF} = 1MHz)		-90 -92 -96		dBm
IF Filter bandwidth			1200/2400		KHz
IF center frequency			1000/2000		KHz
Interference	Co-Channel (C/I ₀) 1 st Adjacent Channel (C/I ₁) 2 nd Adjacent Channel (C/I ₂) 3 rd Adjacent Channel (C/I ₃) Image (C/I _{IM})		11 2 -18 -28 -12		dB
Maximum Operating Input Power	@RF input (BER=0.1%)			0	dBm
RX Spurious Emission	30MHz~1GHz 1GHz~12.75GHz			-52 -47	dBm
RSSI Range with AGC turn on	@RF input	-100		-10	dBm
RX settling time	Standby to RX		130		μs

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12Bit SAR ADC

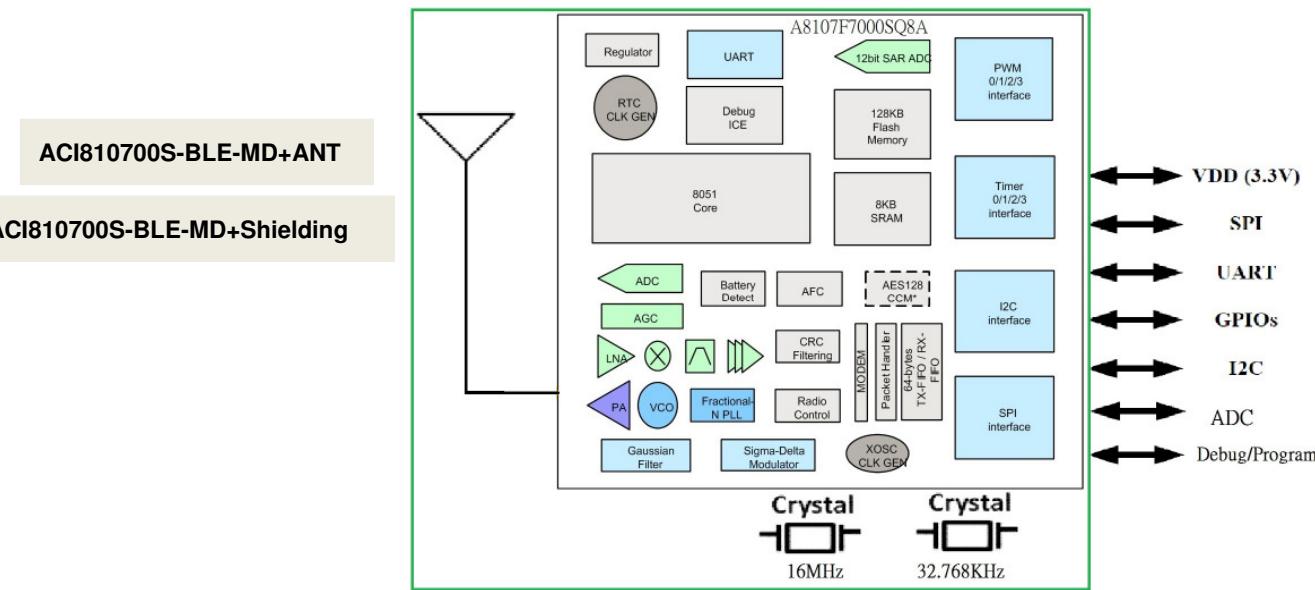
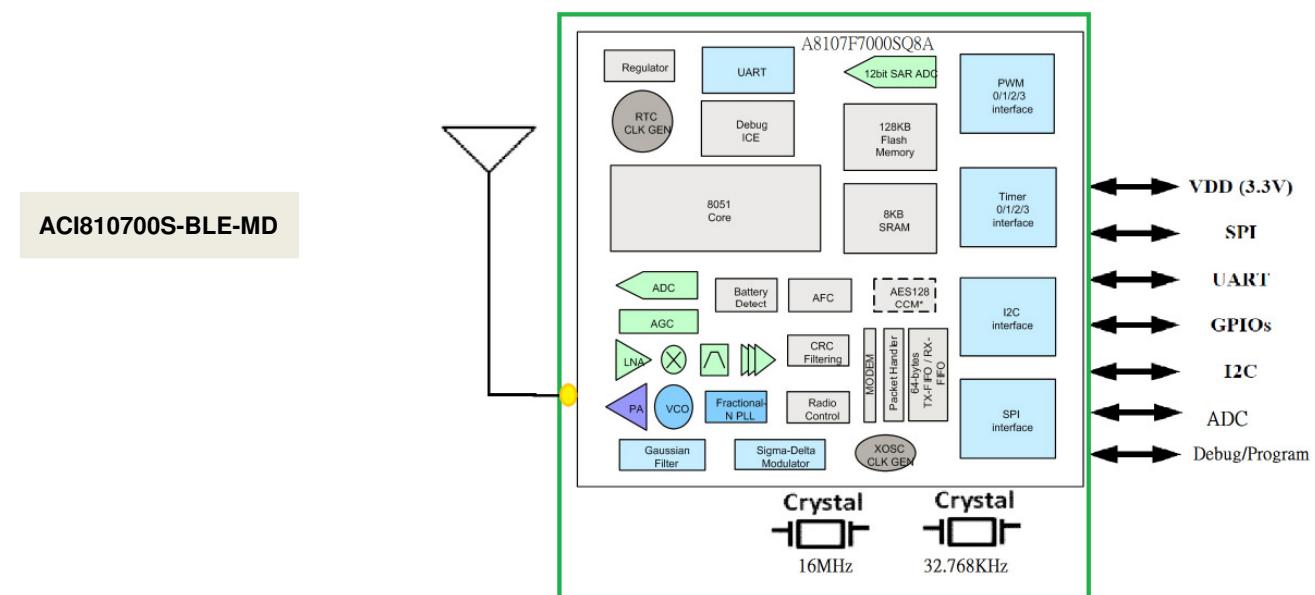
Input voltage range	0	1.8	V
External reference voltage		1.8	V
Input capacitor		25	pF
Bandwidth		200	KHz
EOB, effective number of bits		10	bit
INL		+/- 2	LSB
DNL		+/-1	LSB
Conversion time	128	8	μs
Current consumption		0.4	mA

Regulator

Regulator settling time	A8107 Chip Pin 19 connected to 1nF	200		μs
Band-gap reference voltage		1.21		V
Regulator output voltage		1.8		V

Digital IO DC characteristics

High Level Input Voltage (V _{IH})	0.8*VDD	VDD	V
Low Level Input Voltage (V _{IL})	0	0.2*VDD	V
High Level Output Voltage (V _{OH})	VDD-0.4	VDD	V
Low Level Output Voltage (V _{OL})	0	0.4	V

SiP Module Block Diagram

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Interface Descriptions

J1

Pin No.	Symbol	Function Description	Remark
1	P0_0	SPI_SCLK	
2	P0_1	SPI_MOSI	
3	P0_2	SPI_MISO	
4	GND	Ground	
5	REGI	RF Module supply voltage supply input	2.0 ~ 3.6V
6	P0_3	SPI_SSEL	
7	P0_4	GPIO/ ICE mode	

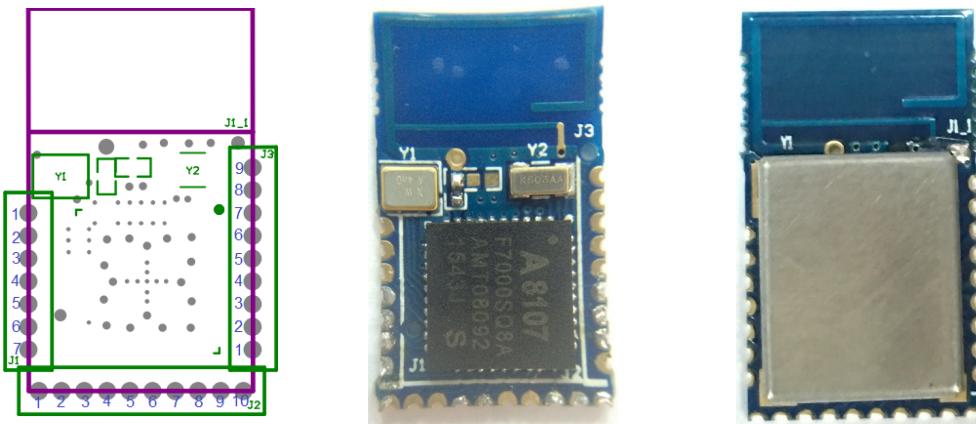
J2

Pin No.	Symbol	Function Description	Remark
1	P0_5	I2C_SCL	
2	P0_6	I2C_SDA	
3	P0_7	INT2 /GPIO1	
4	P1_0	Timer2_T2	
5	P1_1	Timer2_T2EX	
6	P1_2	INT3 /GPIO2	
7	P1_3	INT4/ CKO	
8	P1_4	TTAG_TTDIO / PWM2	
9	P1_5	TTAG_TTCR / PWM3	
10	P1_6	PWM0/ADC4	

J3

Pin No.	Symbol	Function Description	Remark
1	P1_7	PWM1/ADC5	
2	P3_0	UART0_RX/ADC6	
3	P3_1	UART0_TX/ADC7	
4	P3_2	INT0/ADC0	
5	P3_3	INT1/ADC1	
6	P3_4	Timer0_T0/ADC2	
7	P3_5	Timer1_T1/ADC3	
8	NC		
9	RESETN	RESETN	

Outline TOP View



ACI810700S-BLE-MD+ANT

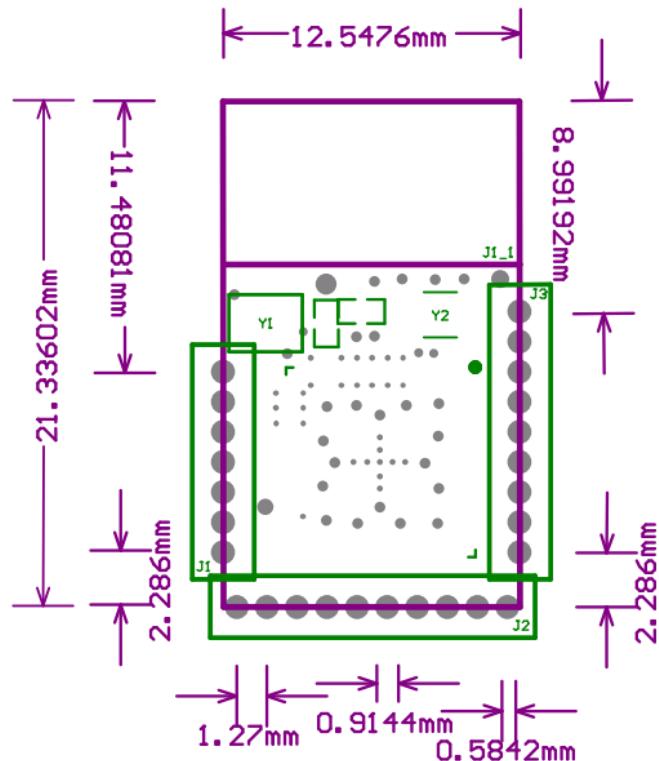
ACI810700S-BLE-MD+Shielding

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Dimension information

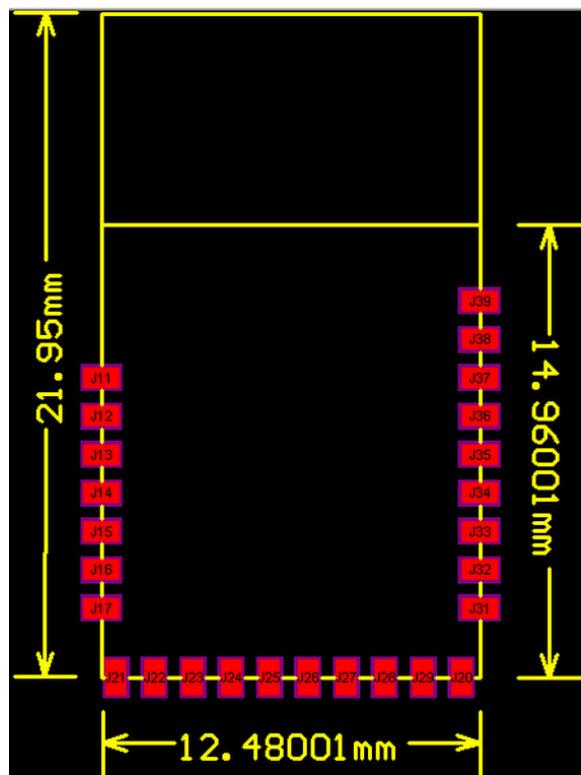
SiP Module Outline Dimensions(Top View)



ACI810700S-BLE-MD+ANT

ACI810700S-BLE-MD+Shielding

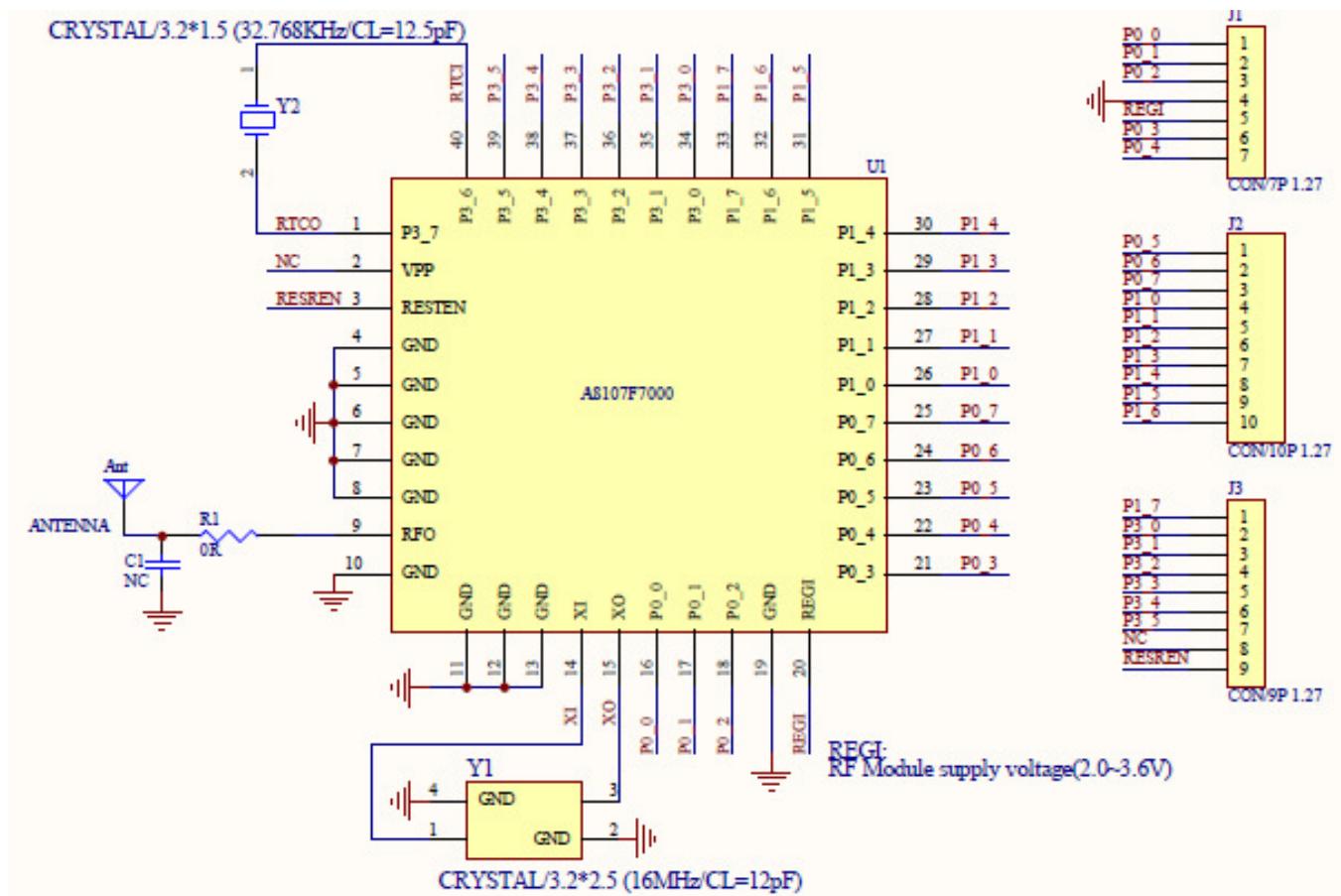
Footprint



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Schematic



Bill of Material

Item	Component	Description	Size	Value	Tol.	Manufacturer	Manufacturer Number
1	U1	128KB Flash Transceiver	LGA 8x8 40pins	A8107F7000		AMICCOM	
2	Y1	Crystal	3.2 x2.5mm	16MHz, CL =12pF	±20ppm	1. AURUM 2. TST	<u>Annotation1</u>
3	Y2	Crystal	3.2 x1.5mm	32.768KHz CL = 12.5pF	±20ppm		<u>Annotation2</u>

Annotation1:

1. A8107 has built-in crystal loading. User can set VCOSC[5:0] to meet crystal loading requirement.
2. Recommend VCOSC = 20, if crystal load = 12pf ,Recommend VCOSC = 13, if crystal load = 9pf

Annotation2:

1. A8107F7000 has built-in crystal loading capacitor for 32.768KHz crystal, but only for Cload =12.5pF.

BTLE QDID Profile Certification Numbers

Bluetooth(R) SIG Qualifications

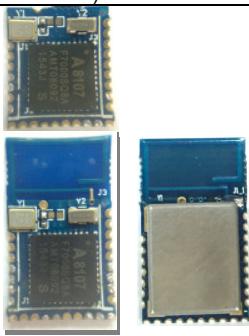
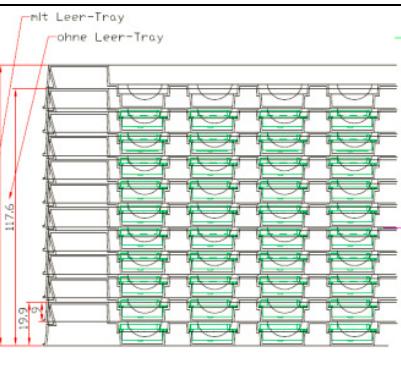
QDID	Product Type	Design Name	Design Description
52727	Controller Subsystem	A8105 controller subsystem-4.0	A8105 / A8107 (RF compatible w. A8105) is a high speed 51 family SOC w. single mode Bluetooth low energy (BLE) RF transceiver
45008	Host Subsystem	AMC_BLE Host	A host subsystem for Bluetooth 4.0 LE
49896	Profile Subsystem	AMC_BLE Profile SPL01	A profile subsystem for Bluetooth 4.0 LE
51582	Profile Subsystem	AMC_BLE Profile SPL02	A profile subsystem for Bluetooth 4.0 LE (expansion)
62785	Profile Subsystem	AMC_BLE Profile SPL03	A profile subsystem for Bluetooth 4.1 LE

Note: Profile subsystem QDID is needed only if SIG standard profile is used.

All subsystem by AMICCOM.

Order & Shipping Packing Information

Item	Module Part No.	dimension	N.W	MOQ	Tray	Vacuum Bag	Carton	Remark
1	ACI810700S-BLE-MD	14.5 x 12.5 mm	mg	1000PCS	100 pcs	1000pcs/10Tray	5000pcs/5 Bag	Without Antenna
2	ACI810700S-BLE-MD+ANT	21.3 x 12.5 mm	mg	1000PCS	100 pcs	1000pcs/10Tray	5000pcs/5 Bag	Integrated PCB Antenna
3	ACI810700S-BLE-MD+Shielding	21.3 x 12.5 mm	mg	1000PCS	100 pcs	1000pcs/10Tray	5000pcs/5 Bag	Integrated Shielding Case

Module	Tray	Stacked trays(Vacuum Bag)	Packing carton
14.5 x 12.5 mm 21.3 x 12.5 mm(PCB Antenna)	290 x 205 x 11(H)mm	290 x 205 x 50(H)mm	380 x 270 x 270(H)mm
			

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焊接信息:**濕度敏感組件**

以往SIP對濕氣的吸收相當敏感。因此建議上件之前，SIP或SIP模組先進行125°C烘烤8小時之後再進行上件。一般上件情況如下列：

- (a.) 透過錫爐將**SIP**焊接至PCB上。
- (b.) 透過熱風槍將**SIP**焊接至PCB上。
- (c.) 透過錫爐將**SIP模組**焊接至其他主機板上。
- (d.) 透過熱風槍將**SIP模組**焊接至其他主機板上。

A8107 SIP 有通過 JEDEC 規範 MSL-3 的測試，經過烘烤後 SIP 或 SIP 模組在工廠環境下($\leq 30^{\circ}\text{C}/60\%\text{RH}$)可暴露 168 小時。在此時間內使用可以不需要烘烤。

回流焊

A8107 SIP 允許通過最多 3 次回流焊。

MSL Label**注意****使用時須遵守的注意事項****靜電敏感元件****濕度敏感元件****警告!!!****此袋內裝濕度敏感之電子元件**

1. 此袋在密封狀態下，可在溫度 $<40^{\circ}\text{C}$ 及相對溼度 $<90\%$ 下儲存12個月
2. 包裝袋被打開後，元件將被迴焊製程所採用時必須符合：
 - a. 在168小時內且工廠環境為 $\leq 30^{\circ}\text{C}/60\%\text{RH}$ 完成。
 - b. 保存在 $<10\%\text{RH}$ 環境下。
3. 元件在下述情況下必須再進行烘烤：
 - a. 濕度指示卡在 $23^{\circ}\text{C}/-5^{\circ}\text{C}$ 時， $>20\%$ 的點已變色。
 - b. 未符合2a或2b的規範。
4. 如需要烘烤，元件得於 $125^{\circ}\text{C}/-5^{\circ}\text{C}$ 下烘烤12小時。
5. 使用元件時須特別小心，否則可能會造成腳平面度/彎腳的異常。

備註:等級及溫度被定義於IPC/JEDEC J-STD-020**包裝袋密封日期: _____**

(如果空白,請參照旁邊的條碼貼紙)



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IPC/JEDEC J-STD-020D.1

CLASSIFICATION/RECLASSIFICATION

Refer to 4.2 for guidance on reclassification of previously qualified/classified SMDs.

Engineering studies have shown that thin, small volume SMD packages reach higher body temperatures during reflow soldering to boards that have been profiled for larger packages. Therefore, technical and/or business issues normally require thin, small volume SMD packages (reference Tables 4-1 and 4-2) to be classified at higher reflow temperatures. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 1: Previously classified SMDs should only be reclassified by the manufacturer. Users should refer to the "Moisture Sensitivity" label on the bag to determine at which reflow temperature the SMD packages were classified.

Note 2: Unless labeled otherwise, level 1 SMD packages are considered to be classified at 220 °C.

Note 3: If supplier and user agree, components can be classified at temperatures other than those in Tables 4-1 and 4-2.

4.1 Compatibility with Pb-Free Assembly Rework Pb-free area array components (classified per Table 4.2) should be capable of assembly rework at 260 °C within 8 hours of removal from dry storage or bake, per J-STD-033. Components that do not meet this assembly rework requirement or that the supplier does not support 260 °C rework **shall** be so specified by the component manufacturer. To verify this capability for components classified at a temperature below 260 °C, a sample of the size per 5.1.2 **shall** be soaked per level 6 conditions (see Table 5-1) using a time on label (TOL) of 8 hours, and subjected to a single reflow cycle with T_p of not less than 260 °C. All devices in the sample **shall** pass electrical test and have a damage response (per 6.1 and 6.2) not greater than that observed for the same package at its rated MSL level. Rework compatibility verification is not required for area array components rated at 260 °C or peripheral leaded metal lead frame packages that do not require full body hot air rework.

Table 4-1 SnPb Eutectic Process - Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 4-2 Pb-Free Process - Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350 - 2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (T_p) can exceed the values specified in Tables 4-1 or 4-2. The use of a higher T_p does not change the classification temperature (T_c).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Note 4: Moisture sensitivity levels of components intended for use in a Pb-free assembly process **shall** be evaluated using the Pb-free classification temperatures and profiles defined in Tables 4.2 and 5-2, whether or not Pb-free.

Note 5: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

4.1 Compatibility with Pb-Free Assembly Rework Pb-free area array components (classified per Table 4.2) should be capable of assembly rework at 260 °C within 8 hours of removal from dry storage or bake, per J-STD-033. Components that do not meet this assembly rework requirement or that the supplier does not support 260 °C rework **shall** be so specified by the component manufacturer. To verify this capability for components classified at a temperature below 260 °C, a sample of the size per 5.1.2 **shall** be soaked per level 6 conditions (see Table 5-1) using a time on label (TOL) of 8 hours, and subjected to a single reflow cycle with T_p of not less than 260 °C. All devices in the sample **shall** pass electrical test and have a damage response (per 6.1 and 6.2) not greater than that observed for the same package at its rated MSL level. Rework compatibility verification is not required for area array components rated at 260 °C or peripheral leaded metal lead frame packages that do not require full body hot air rework.

4.2 Reclassification SMD packages previously classified to a moisture sensitivity level and classification temperature (T_c) may be reclassified if the damage response (e.g., delamination/cracking) at the more severe condition for items listed in 6.1 and 6.2 is less than, or equal to, the damage response at the original classification condition. If no major changes have been made to a previously qualified SMD package, this method may be used for reclassification to an improved level (i.e., longer floor life) at the same reflow temperature. The reclassification level cannot be improved by more than 1 level without additional reliability testing. Reclassification to level 1 requires additional reliability testing. If no major changes have been made to a previously qualified SMD package, this method may be used for reclassification at a higher reflow temperature providing the moisture level remains the same or degrades to a more sensitive level. No SMD packages classified as moisture sensitive by any previous version of J-STD-020, JESD22-A112 (rescinded), or IPC-SM-786 (rescinded) may be reclassified as nonmoisture sensitive (level 1) without additional reliability stress testing (e.g., JESD22-A113 and JESD-47 or the semiconductor manufacturer's in-house procedures). To minimize testing, the results from a given SMD package may be generically accepted to cover all other devices which are manufactured in the same package, using the same packaging materials (e.g., die attach, mold compound and/or die coating, etc.), with the die using the same wafer fabrication technology, and with die pad dimensions not greater than those qualified.

The following attributes could affect the moisture sensitivity of a device and may require reclassification:

- Die attach material/process.
- Number of pins.
- Encapsulation (mold compound or glob top) material/process.
- Die pad area and shape.
- Body size.
- Passivation/die coating.
- Leadframe, substrate, and/or heat spreader design/material/finish.
- Die size/thickness.
- Wafer fabrication technology/process.
- Interconnect.
- Lead lock taping size/location as well as material.

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PROCEDURE

The recommended procedure is to start testing at the lowest moisture sensitivity level the evaluation package is reasonably expected to pass (based on knowledge of other similar evaluation packages). In the case of equipment malfunction, operator error, or electrical power loss, engineering judgment **shall** be used to ensure that the minimum intent/requirements of this specification are met.

5.1 Sample Requirements

5.1.1 Reclassification (qualified package without additional reliability testing) For a qualified SMD package being reclassified without additional reliability testing, select a minimum sample of 22 units for each moisture sensitivity level to be tested. A minimum of 2 nonconsecutive assembly lots must be included in the sample with each lot having approximately the same representation. Sample units **shall** have completed all manufacturing processing required prior to shipment. Sample groups may be run concurrently on 1 or more moisture sensitivity levels.

5.1.2 Classification/Reclassification and Rework Select a minimum sample of 11 units for each moisture sensitivity level to be tested. A minimum of 2 nonconsecutive assembly lots must be included in the sample with each lot having approximately the same representation. Sample units **shall** have completed all manufacturing processes required prior to shipment. Sample groups may be run concurrently on 1 or more moisture sensitivity levels. Testing must be continued until a passing level is found. SMD packages should not be reclassified by the user unless approved by the supplier.

5.2 Initial Electrical Test Test appropriate electrical parameters (e.g., data sheet values, in-house specifications, etc.). Replace any components, while maintaining the sample requirements of 5.1.2, which fail to meet tested parameters.

5.3 Initial Inspection Perform an external visual (at 40X) and acoustic microscope examination on all components to establish a baseline for the cracking/delamination criteria in 6.2.1.

Note: This standard does not consider or establish any accept/reject criteria for delamination at initial/time zero inspection.

5.4 Bake Bake the sample for 24 hours minimum at 125 +5/-0 °C. This step is intended to remove moisture from the package so that it will be "dry."

Note: This time/temperature may be modified if desorption data on the particular device under test shows that a different condition is required to obtain a "dry" package when starting in the wet condition for 85 °C/85% RH (see 8.3).

5.5 Moisture Soak Place devices in a clean, dry, shallow container so that the package bodies do not touch or overlap each other. Submit each sample to the appropriate soak requirements shown in Table 5-1. At all times parts should be handled using proper ESD procedures in accordance with JESD-625

JEDEC MSL-3 Moisture Sensitivity Levels

LEVEL	FLOOR LIFE		SOAK REQUIREMENTS				
			STANDARD		ACCELERATED EQUIVALENT ¹		
	TIME	CONDITION	TIME (hours)	CONDITION	TIME (hours)	TIME (hours)	CONDITION
1	Unlimited	≤30 °C/85% RH	168 +5/-0	85 °C/85% RH	NA	NA	NA
2	1 year	≤30 °C/60% RH	168 +5/-0	85 °C/60% RH	NA	NA	NA
2a	4 weeks	≤30 °C/60% RH	696 +5/-0	30 °C/60% RH	120 +1/-0	168 +1/-0	60 °C/60% RH
3	168 hours	≤30 °C/60% RH	192 +5/-0	30 °C/60% RH	40 +1/-0	52 +1/-0	60 °C/60% RH
4	72 hours	≤30 °C/60% RH	96 +2/-0	30 °C/60% RH	20 +0.5/-0	24 +0.5/-0	60 °C/60% RH
5	48 hours	≤30 °C/60% RH	72 +2/-0	30 °C/60% RH	15 +0.5/-0	20 +0.5/-0	60 °C/60% RH
5a	24 hours	≤30 °C/60% RH	48 +2/-0	30 °C/60% RH	10 +0.5/-0	13 +0.5/-0	60 °C/60% RH
6	Time on Label(TOL)	≤30 °C/60% RH	TOL	30 °C/60% RH	NA	NA	NA

Note 1: CAUTION - To use the "accelerated equivalent" soak conditions, correlation of damage response (including electrical, after soak and reflow), should be established with the "standard" soak conditions. Alternatively, if the known activation energy for moisture diffusion of the package materials is in the range of 0.40 - 0.48 eV or 0.30 - 0.39 eV, the "accelerated equivalent" may be used. Accelerated soak times may vary due to material properties (e.g., mold compound, encapsulant, etc.). JEDEC document JESD22-A120 provides a method for determining the diffusion coefficient.

Note 2: The standard soak time includes a default value of 24 hours for semiconductor manufacturer's exposure time (MET) between bake and bag and includes the maximum time allowed out of the bag at the distributor's facility.

If the actual MET is less than 24 hours the soak time may be reduced. For soak conditions of 30 °C/60% RH, the soak time is reduced by 1 hour for each hour the MET is less than 24 hours. For soak conditions of 60 °C/60% RH, the soak time is reduced by 1 hour for each 5 hours the MET is less than 24 hours.

If the actual MET is greater than 24 hours the soak time must be increased. If soak conditions are 30 °C/60% RH, the soak time is increased 1 hour for each hour that the actual MET exceeds 24 hours. If soak conditions are 60 °C/60% RH, the soak time is increased 1 hour for each 5 hours that the actual MET exceeds 24 hours.

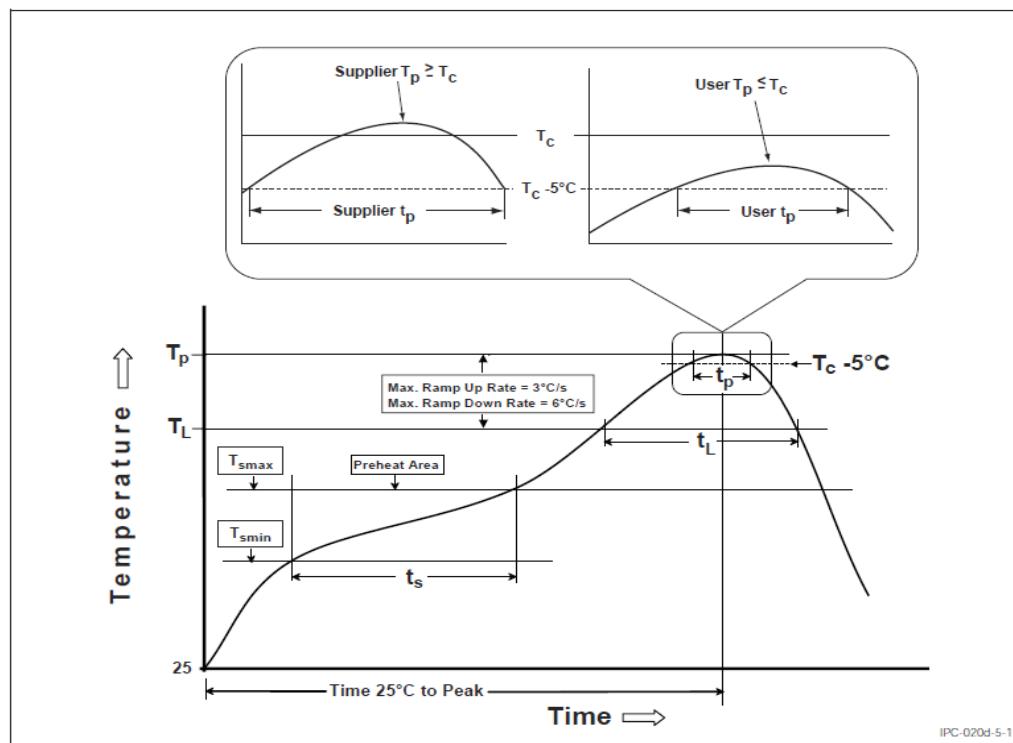
Note 3: Supplier may extend the soak times at their own risk.

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Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <260 °C; Number of Times : **2 times****Classification Reflow Profiles**

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min (T_{smin})	100 °C	150 °C
Temperature Max (T_{smax})	150 °C	200 °C
Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds	60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time (t_L) maintained above T_L	60-150 seconds	60-150 seconds
Peak package body temperature (T_p)	For users T_p must not exceed the Classification temp in Table 4-1. For suppliers T_p must equal or exceed the Classification temp in Table 4-1.	For users T_p must not exceed the Classification temp in Table 4-2. For suppliers T_p must equal or exceed the Classification temp in Table 4-2.
Time (t_p)* within 5 °C of the specified classification temperature (T_c), see Figure 5-1.	20* seconds	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g., live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e., dead-bug), T_p shall be within ± 2 °C of the live-bug T_p and still meet the T_c requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 5-2.

For example, if T_c is 260 °C and time t_p is 30 seconds, this means the following for the supplier and the user.

For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds. For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.

Note 3: All components in the test load shall meet the classification profile requirements.

Note 4: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

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FEDERAL COMMUNICATIONS COMMISSION STATEMENT

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try correcting the interference by one or more of the following measures:

- Reorient the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

You are cautioned that changes or modifications not expressly approved by the party responsible for compliance could void your authority to operate the equipment.

Important FCC notice:

In accordance with FCC Part 15C, this module is listed as a Modular Transmitter device.

The antenna of this transmitter must not be co-located or operating in conjunction with any other antenna or transmitters within a host device, except in accordance with FCC multitransmitter product approval procedures.

FCC Label Instructions

The outside of final products that contains this module device must display a label referring to the enclosed module. This exterior label can use wording such as the following: **“Contains Transmitter Module FCC ID: 2AE2I-ACI810700S”** or **“Contains FCC ID: 2AE2I-ACI810700S”** Any similar wording that expresses the same meaning may be used

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