AI7931LD
User's Guide

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2022/04/29	Initial Version	Ivan	A
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Lists of Tables and Figures

1.Introduction

1.1.General Description

AI7931LD is a highly integrated IoT module that features an ARM® Cortex-M33 application processor, a low power 1x1 802.11a/b/g/n/ax dual-band Wi-Fi subsystem, a Bluetooth v5.0 subsystem and a Power Management Unit (PMU). The Wi-Fi subsystem and a Bluetooth v5.0 subsystem offer feature-rich wireless connectivity at high standards, and deliver reliable, cost-effective throughput from an extended distance. The AI7931LD is designed to support standard based features in the areas of security, quality of service and international regulations, giving end users the greatest performance any time and in any circumstance.

The AI7931LD is based on ARM® Cortex-M33 with floating point microcontroller (MCU) including SRAM/ROM memory. The module also supports rich peripheral interfaces, including SDIO, SPI master, I2C, I2S_IN, IR input, UART, AUXADC, PWM, and GPIOs.

These features are used to download and debug a project on EK-AI7931LD.

The front view of the EK-AI7931LD including AI7931LD module is shown in Figure 1.

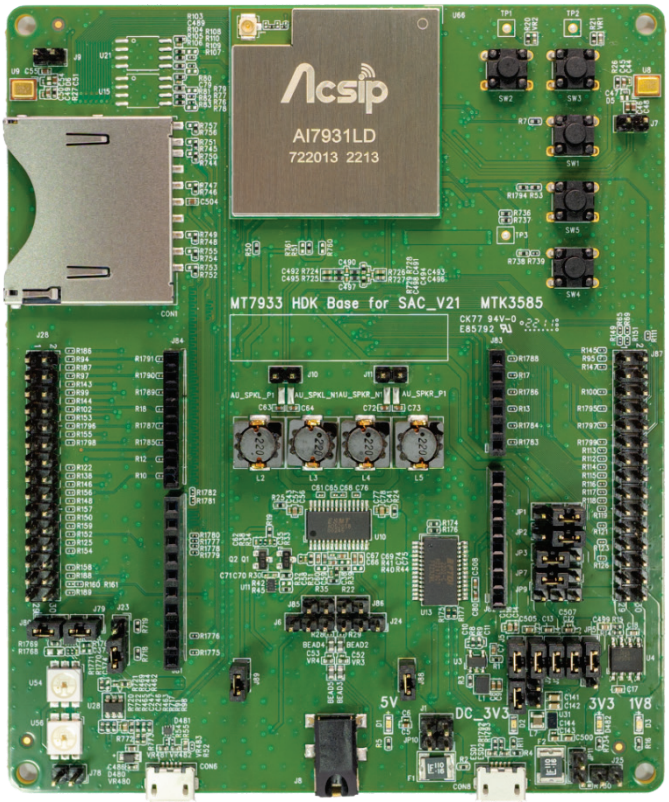


Figure 1. Front view of EK-AI7931LD

2. Get started with the HDK

Before commencing the application development, you need to configure the development platform.

2.1. Configuring the EK-AI7931LD

The top view of the EK-AI7931LD is shown in Figure 2

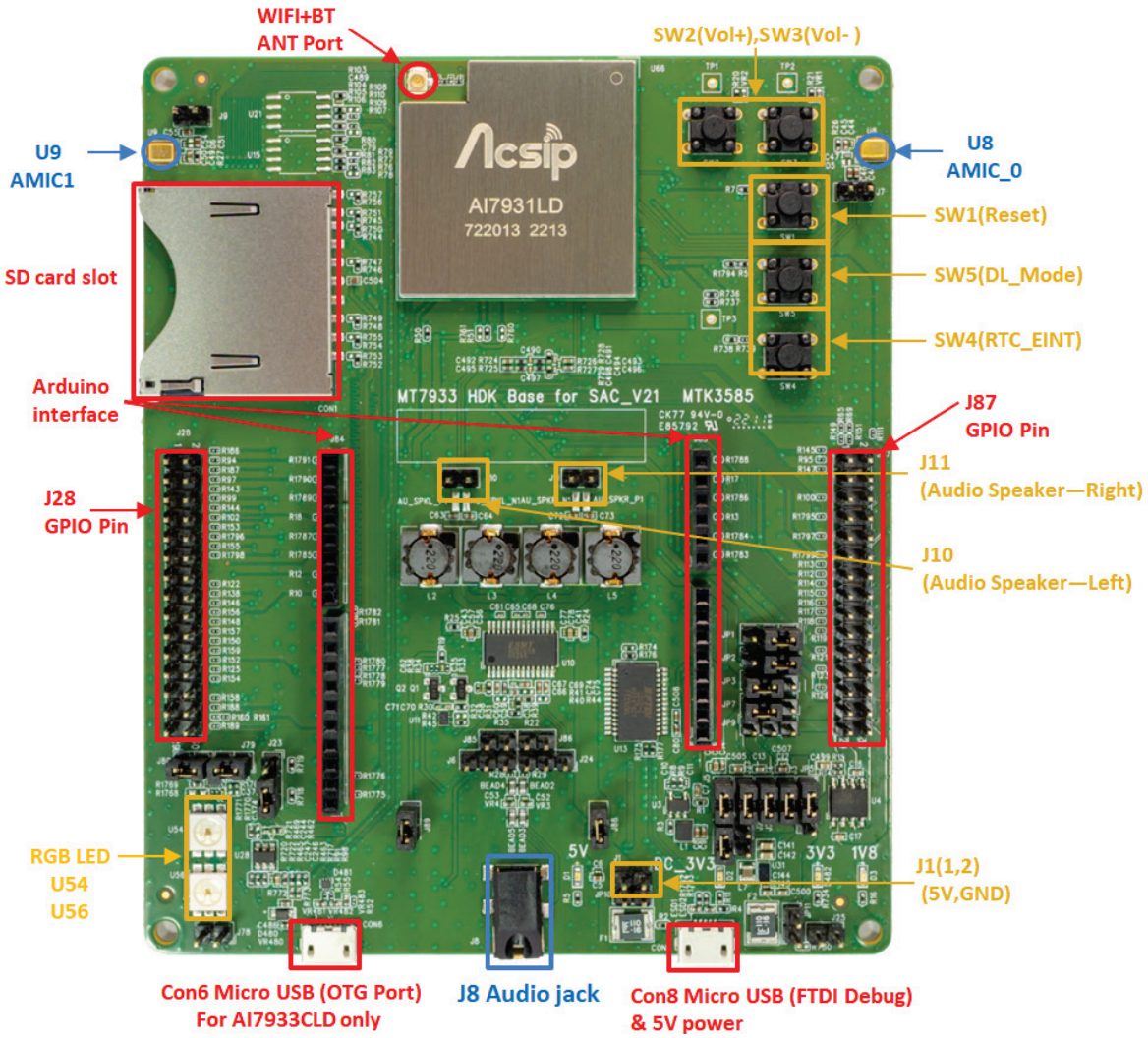


Figure 2. Jumpers and connectors on the EK-AI7931LD

The description of pins (Figure 2) and their functionality is provided below:

1) CON8 transfer USB interface to UART interface, can debug through UART, transmit, and receive a signal form PC.

2) CON8 is a USB 5V power for EK-AI7931LD, or you can use external 5V power at J1.

3) Press SW1 to reset the system For SW2~SW5 more detail, please see “section 4.4”.

4) For Wi-Fi and BT function AI7931LD module reserve a Wi-Fi + BT IPEX connector. Please connect external antenna to transmit and receive RF signals.

5) U8 and U9 are on-board AMICs which can catch voice command.

6) U54/U56 are RGB LEDs and these RGB LED will be controlled by SPIM interface.

7) J28 and J87 support multifunction GPIO interface, for more detail please refer to “section 4.7”.

8) J10 and J11 are audio speaker pin header which can connect 8ohm/2W speaker to achieve voice assistant function.

2.2.Installing the FTDI drivers on Microsoft Windows

To configure the EK-AI7931LD:

1) Connect the EK-AI7931LD CON8 to the computer using a micro-USB cable.

2) Check your PC is x86 or x64 system. And download and install FTDI Windows serial port driver from Here. (The red block showed the download file at below figure)

Currently Supported D2XX Drivers:

		Processor Architecture					
Operating System	Release Date	x86 (32-bit)	x64 (64-bit)	ARM	MIPS	SH4	Comments
Windows*	2017-08-30	2.12.28	2.12.28	-	-	-	WHQL Certified. Includes VCP and D2XX. Available as a setup executable Please read the Release Notes and Installation Guides.
Windows RT	2014-07-04	1.0.2	-	1.0.2	-	-	A guide to support the driver (AN_271) is available here
Linux	2018-06-22	1.4.8	1.4.8	1.4.8 ARMv5 soft-float 1.4.8 ARMv5 soft-float uClibc 1.4.8 ARMv6 hard-float *** 1.4.8 ARMv7 hard-float *** 1.4.8 ARMv8 hard-float ***	1.4.8 MIPS32 soft-float 1.4.8 MIPS32 hard-float 1.4.8 MIPS openwrt-uclibc		If unsure which ARM version to use, compare the output of `readelf` and `file` commands on a system binary with the content of release/build/libftd2xx.txt in each package. ReadMe NEW! Video Install Guide

3) If your OS is Windows7 or 10, please open Windows Control Panel then click System and enter Device Manager.

4) In Device Manager, navigate to Ports (COM & LPT) (see Figure 3).

5) A new COM device should appear under Ports (COM & LPT) in Device Manager, as shown in Figure 3. Note the COMx port number of the serial communication port, this information is needed to send command and receive logs from the COM port.

Due to the com port numbers (COMx) are different at different PC. As red block in Figure 3. showed, means “CM33 UART”.

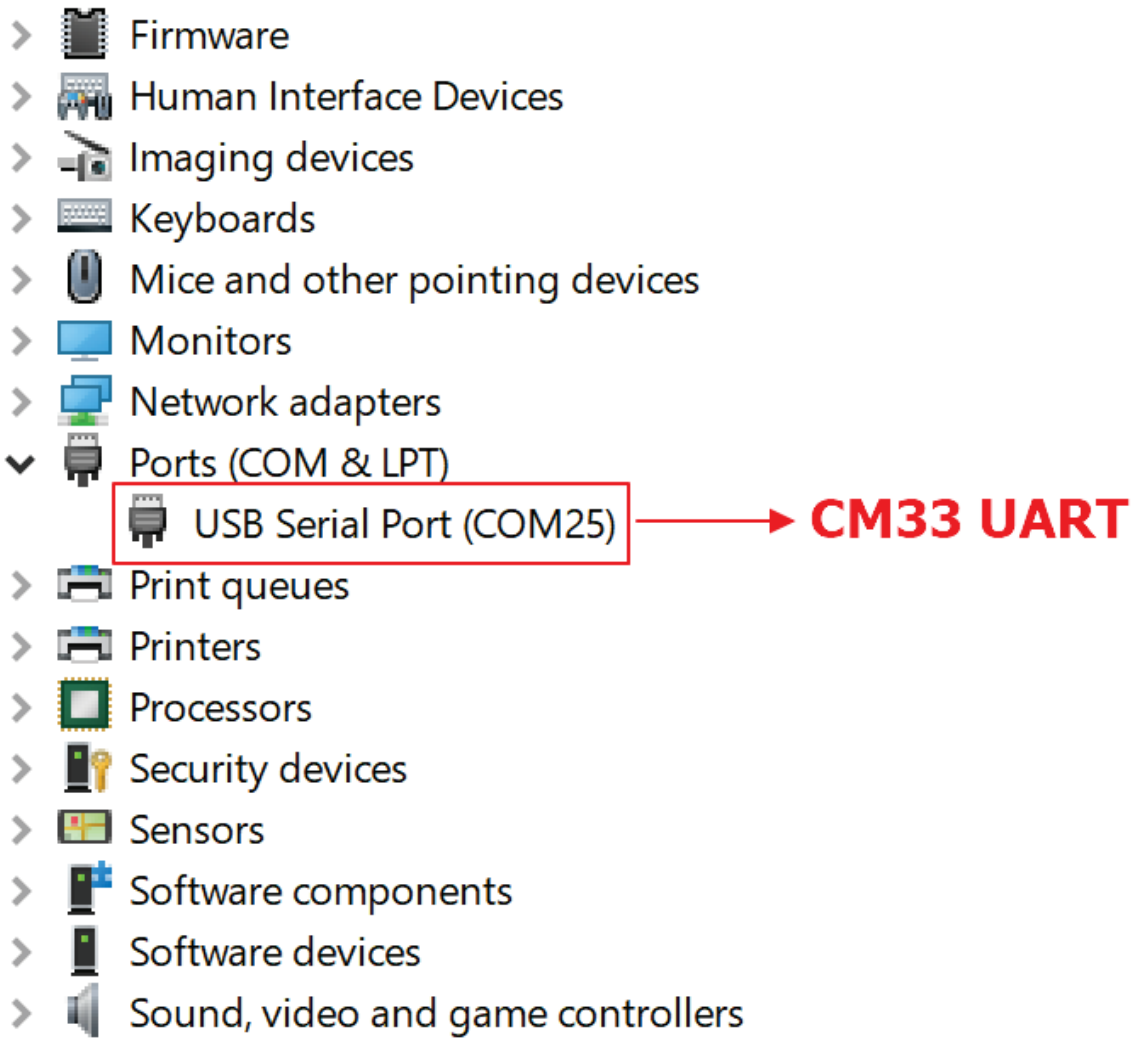


Figure 3. COM port associated with the EK-AI7931LD

3.Hardware Features

This section provides the main supported features of the EK-AI7931LD The detailed description of the features is provided in the upcoming sections

3.1.Features Description

3.1.1. Technology and Package

- AI7931LD LGA-104 module, 32mm X 32mm X 2.7mm (Typ.)

3.1.2. Power Management and Clock Source

- Integrates high efficiency power management unit with single 3.3V power supply input.
- Integrates 26MHz crystal clock with low power operation in idle mode.
- Integrates 32KHz crystal oscillator for low power sleep mode.

3.1.3. Platform

- ARM® Cortex-M33 MCU with FPU with up to 300MHz clock speed
- Embedded 1MB SRAM and 4MB PSRAM
- Embedded 16MB serial flash with eXecute In Place (XIP) and on-the-fly AES
- Supports Hardware crypto engines including AES, DES/3DES, SHA, ECC, TRNG for network security
- Supports up to 22 General Purpose IOs, which are multiplexed with SDIO, SPI Master, UART, I2C, I2S_IN, AUXADC, PWM and GPIO interfaces
- Supports 12 DMA channels.

3.1.4. Wi-Fi

- IEEE 802.11 1T1R a/b/g/n/ax 5GHz and 2.4GHz
- Supports 1x1 20MHz bandwidth, MCS0~8(256-QAM) in 2.4G/5GHz band
- Support uplink MU-OFDMA TX and downlink MU-OFDMA RX
- Support LDPC Tx (Low-density parity check)
- Support STBC Rx
- Wi-Fi security WFA WPA/WPA2/WPA3 personal, WPS2.0
- QOS supports of WFA WMM, WMM PS
- Support 11ax TWT low power
- Support CSI (Channel Signal Information)
- Support antenna diversity

3.1.5. Bluetooth

- BT5.0 2M_PHY / Long Range / Advertising Extension / SAM / CS#2 / High Duty Cycle Non-Connectable ADV
- BT4.2 Link Layer Privacy / LE Secure Connection / LE Data Packet Length Extension / Link Layer Extended Scanner Filter Policies
- BT4.1 Link Layer Topology / Secure Connection
- BT4.0
- Up to 8 BLE link
- Packet loss concealment
- Channel quality driven data rate adaptation
- Channel assessment and WB RSSI for AFH
- Supports Bluetooth/Wi-Fi coexistence

3.1.6. Miscellaneous

- Embedded eFuse to store specific device information and RF calibration data.
- Advanced TDD mode Wi-Fi/Bluetooth coexistence scheme.

4.Hardware Feature Configuration

4.1.Microcontroller

The AI7931LD features an ARM® Cortex-M33 processor, which is the most energy efficient ARM® processor currently available. It supports the clock rates up to 200MHz when core power is 0.7V and 300MHz when core power is 0.8V. The MCU executes the Thump-2 instruction set for optimal performance and code size, including hardware division, single cycle multiplication and bit-field manipulation. The AI7931LD includes a Memory Protection Unit (MPU) in Cortex-M33 MCU to detect unexpected memory access and provides other memory protection features. The AI7931LD also includes FPU in Cortex-M33 MCU.

4.2.Power supply

EK-AI7931LD supports two types of power supply.

1) Power up with a micro-USB connector.

An on-board switching regulator provides voltage of 3.3V for the EK-AI7931LD, if the power is supplied from an on-board micro-USB connector CON8 (Figure 2). This supply can be isolated from the switching regulator using the jumpers.

Note: that the jumpers J2, J3, J4, J5, J27 pin1 and pin2. JP1, JP2, JP5 pin1 and pin2 are required to be set on. More details on the jumpers can be found in Table 1.

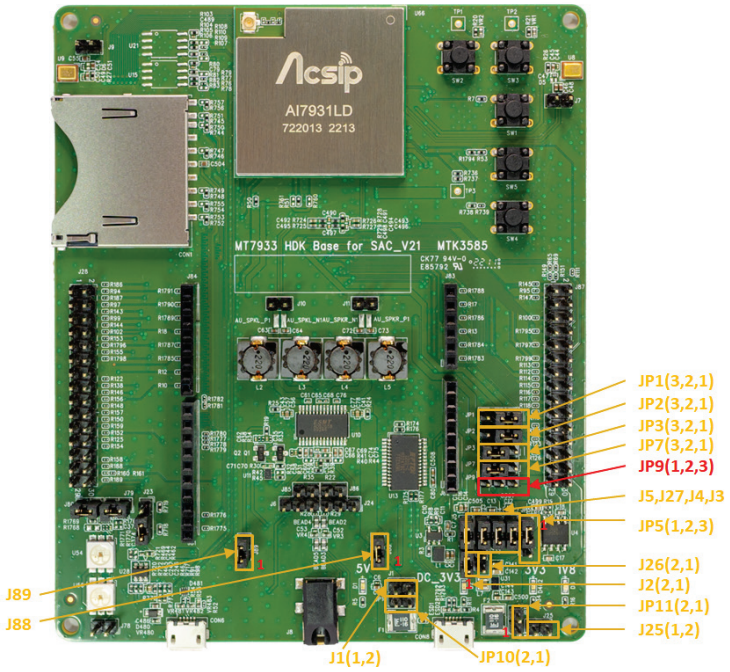


Figure 4. Default power jumper plot

Table 1 Jumper settings for system power input through USB connection

Jumper	Usage	Comments
J1	External 5V power supply	Use external power source to supply 5V voltage to EK-AI7931LD PCB. Pin 1 is 5V source. Pin2 is GND.
J2	DC-5V transfer to DC-3V3 current source	
J3	Current measurement (3V3)	Measures the current flow in AI7931LD module.
J4	3V3 for EEPROM power	EEPROM has no parts.
J5	3V3 for external components	
J25	AVDD33_VRTC battery power supply	Use AA or AAA battery for RTC 3V3 power. Pin1 is positive endpoint, Pin2 is GND.
J26	Current measurement in RTC mode	RTC mode For AI7933CLD only.
J27	3V3 for SD_CARD power	
JP1	Switch VCCIO_L to 3V3 power domain or 1V8 power domain	Select pin 1 & 2, means VCCIO_L use 3V3 power domain Select pin 2 & 3, means VCCIO_L use 1V8 power domain
JP2	Switch VCCIO to 3V3 power domain or1V8 power domain	Select pin 1 & 2, means VCCIO use 3V3 power domain Select pin 2 & 3, means VCCIO use 1V8 power domain Caution: The flash of AI7931LD default using3V3 power domain, if you want to change VCCIO to 1V8 power domain please rework flash to 1V8 power domain flash (eq. W25Q128JWPIQ)
JP3	Switch 1V8 VCCIO from internal PHYLDOor external LDO	Select pin 2 & 3, means 1V8 VCCIO from internal PHYLDO Select pin 1 & 2, means 1V8 VCCIO from external Buck component
JP5	Switch RTC 3V3 from DC-3V3 or AVDD33_VRTC	Select pin 1 & 2, means RTC_3V3 use DC-3V3 Select pin 2 & 3, means RTC_3V3 use AVDD33_VRTC
JP7	Switch SD Card to 3V3 power domain or 1V8 power domain	Select pin 1 & 2, means SD_CARD power use 1V8 power domain Select pin 2 & 3, means SD_CARD power use 3V3 power domain
JP9	Switch EEPROM(NC) to 3V3 power domain or 1V8 power domain	Select pin 1 & 2, means EEPROM power use 3V3 power domain Select pin 2 & 3, means EEPROM power use 1V8 power domain
J88	5V for (U10) Audio AMP power	Pin 1 is EXUSB_5V
J89	5V for (U10) Audio AMP using	Pin 1 is EXUSB_5V

2) Power up using an AA or AAA battery.

Connect an external AA or AAA battery to battery pin header (J25) to supply power to the system, as shown in Figure 5. Please note that remove jumper J2 and plug in jumper J26. Jumper JP5 can be removed.

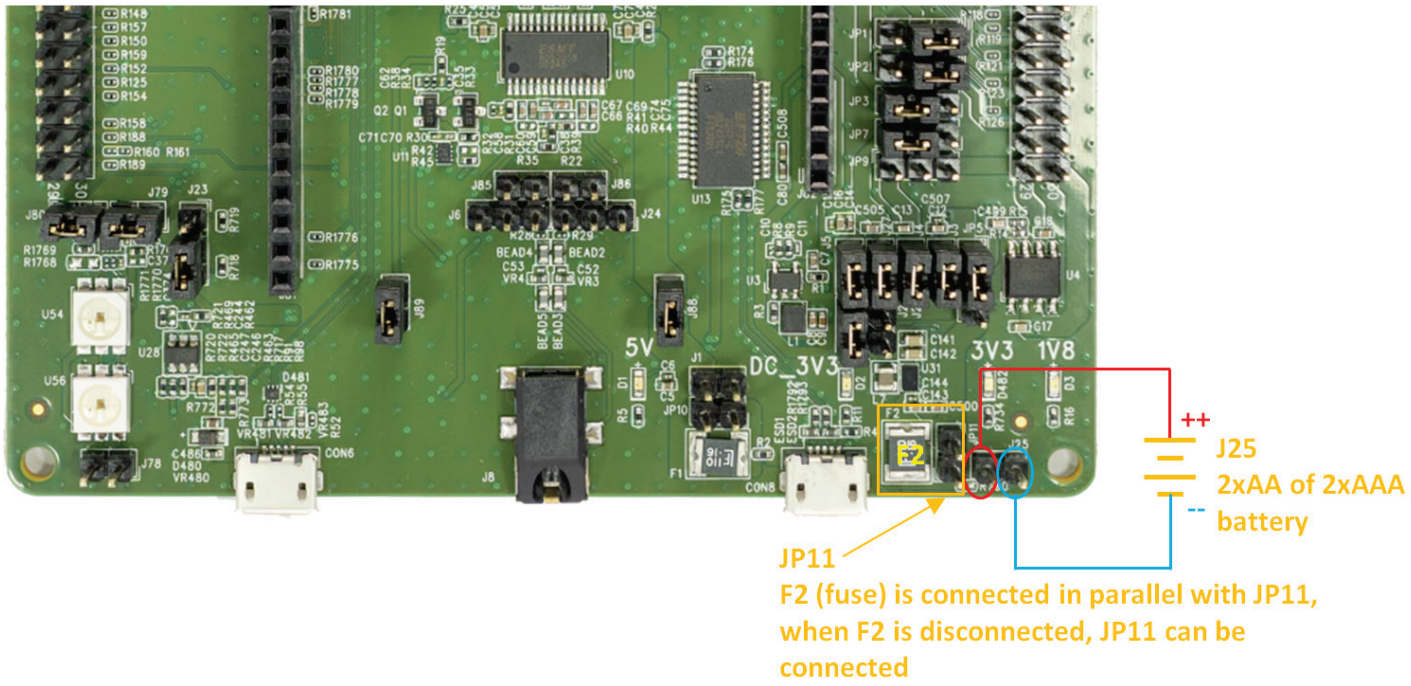


Figure 5. Power up the HDK using an AA or AAA Battery (J25)

4.3. Audio

The EK-AI7931LD has on-board audio connector associated with different functionalities of the board. The detail of audio related function can refer to Table 2.

Table 2 Audio related function

item	Detail
J8	3.5mm audio jack for external active speaker.
J6	Audio-Left_P switch , Pin(3,2,1) Pin define (Amp_L_in_P , Module_audio_out_L, Audio jack_L_in) Select pin 2 & 1, The audio is output by audio jack. Select pin 3 & 2, The audio is output by speaker (J10)
J24	Audio-Right_P switch, Pin(3,2,1) Pin define (Audio jack_R_in , Module_audio_out_R ,Amp_R_in_P) Select pin 3 & 2, The audio is output by audio jack. Select pin 2 & 1, The audio is output by speaker (J11)
J85	Audio-Left_N , Pin(1,2) Pin define (Audio_L_N,GND)
J86	Audio-Right_N, Pin(1,2) Pin define (GND, Audio_R_N)
J10	Audio header for left speaker
J11	Audio header for right speaker
U8	AMIC for left channel (the microphone hole is set at back side of EK-AI7931LD)
U9	AMIC for right channel (the microphone hole is set at back side of EK-AI7931LD)
SW2	Audio volume up button
SW3	Audio volume down button

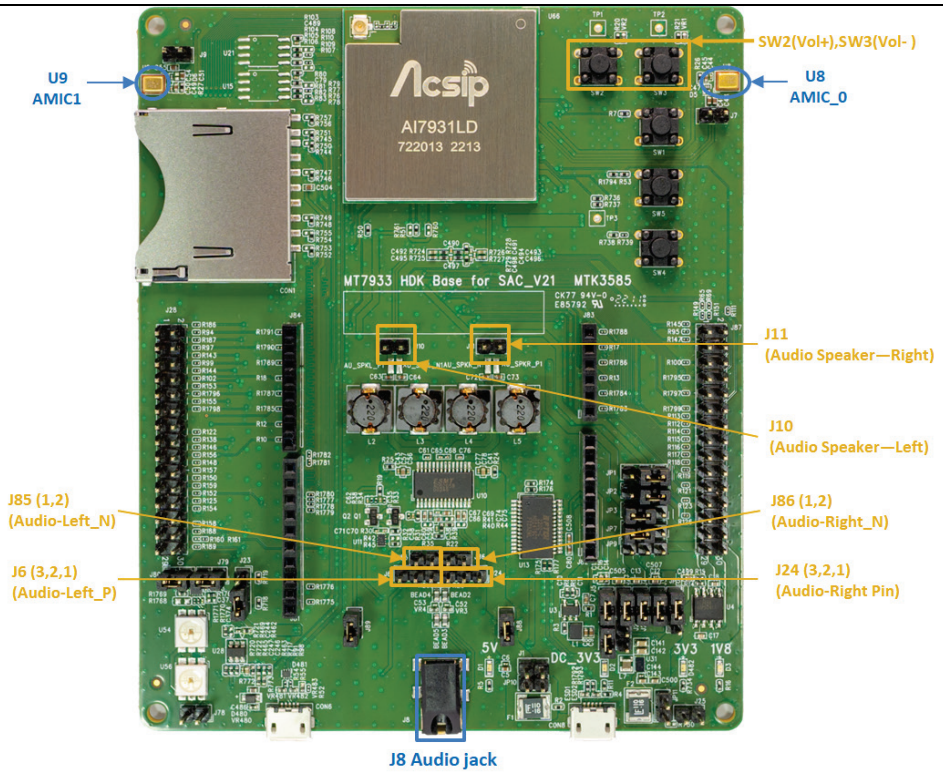


Figure 6. Audio related function

4.4.Buttons

The EK-AI7931LD is equipped with buttons with the following functionality.

The push buttons are shown in Figure 2 The detail of buttons can refer to Table 3.

Table 3 Buttons

Button	Name	Detail
SW1	SYSRST	Press SW1 to restart the EK-AI7931LD
SW2	Vol+	Audio volume up button
SW3	Vol-	Audio volume down button
SW4	RTC_EINT	For AI7933CLD only
SW5	Force DL mode	Press SW5 to trigger strapping mode (download mode…)

4.5. RGB LED

As Figure7. showed, the EK-AI7931LD has on-board RGB LEDs (U54/U56) which be controlled by SPIM interface. Please note that ensure jumper J79 and J80 are connected before using RGB LED function If you want to cascade more RGB LED, you can connect to J78

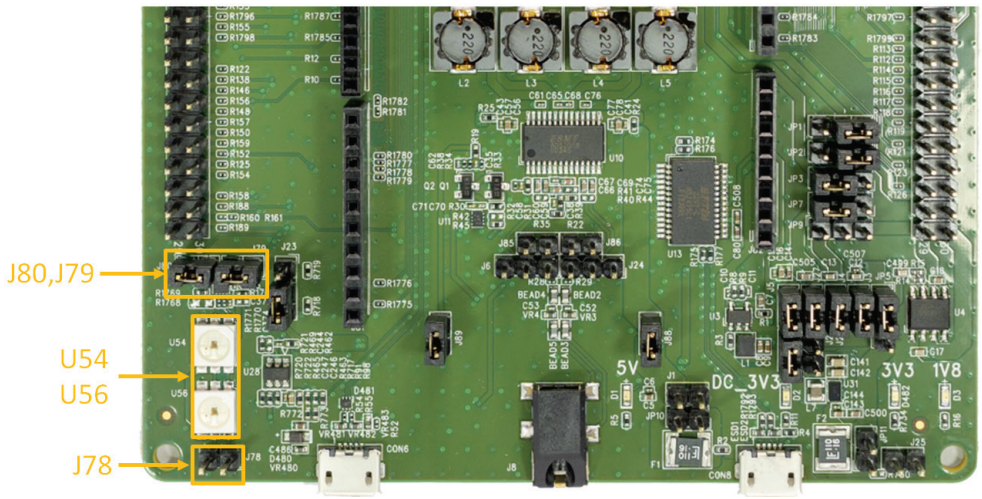


Figure 7. RGB LED

4.6. SD Card

The EK-AI7931LD reserve a SD card slot to provide user to save data into a SD card. And note that there are some registers which placed need to be reworked before using SD card. Please refer to figure.8 and switch R756 to R757; switch R745 to R751; switch R744 to R750; switch R746 to R747; switch R748 to R749; switch R754 to R755; switch R752 to R753.

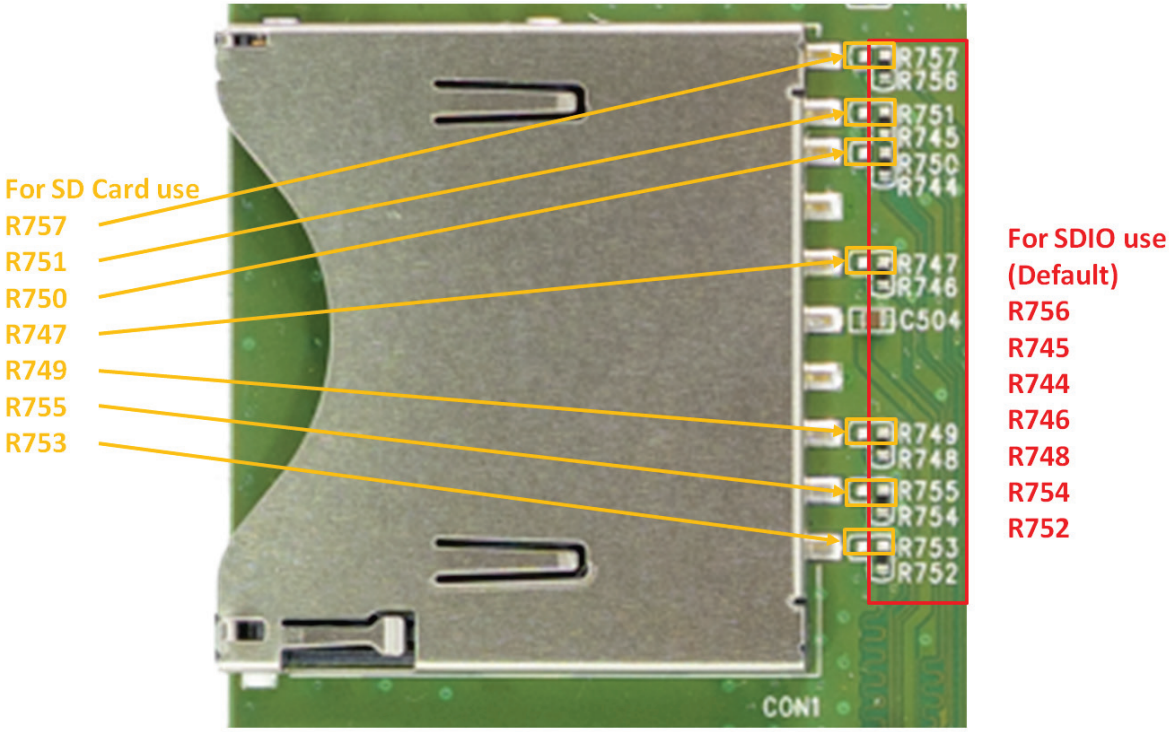
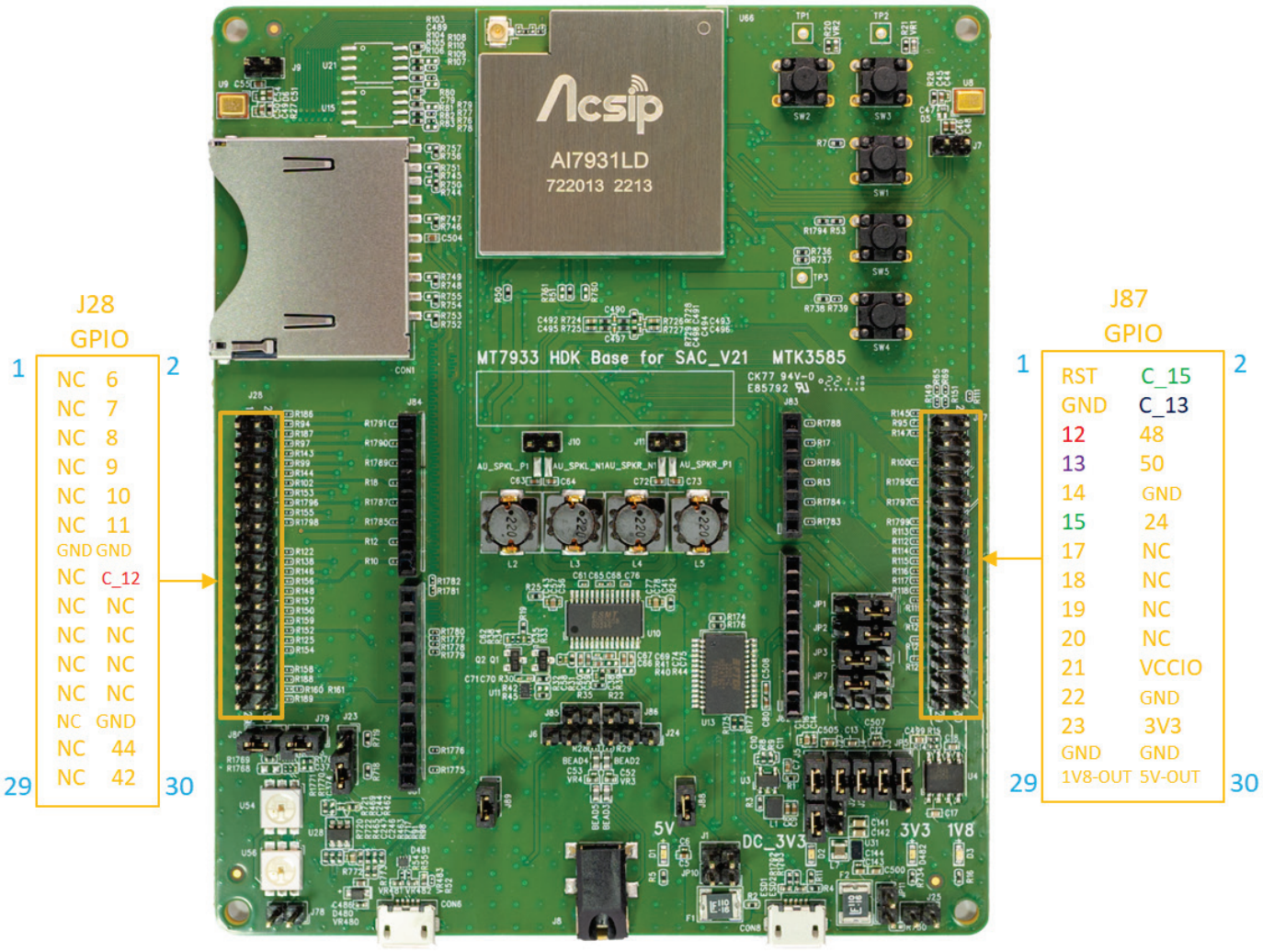


Figure 8. SD card slot rework

4.7.Extension connectors

The EK-AI7931LD provides similar pin-out extension connectors for various sensor and device connectivity, as shown in Figure.9 and described in Table 4.

The board has 22 GPIOs multiplexed with other interfaces. Depending on the use case, user can configure each I/O functionality.



Note: GPIO-12 & GPIO-C_12 are the same circuit.

GPIO-13 & GPIO-C_13 are the same circuit.

GPIO-15 & GPIO-C_15 are the same circuit.

Figure 9. GPIO pin-out extension connectors

Table 4 GPIO pin-out extension connector

Signal Name	Connector Pin Number	Signal Name	Connector Pin Number
GPIO_0	Reserve for flash	GPIO_14	J87 - 9
GPIO_1	Reserve for flash	GPIO_15	J87 - 11
GPIO_2	Reserve for flash	GPIO_17	J87 - 13
GPIO_3	Reserve for flash	GPIO_18	J87 - 15
GPIO_4	Reserve for flash	GPIO_19	J87 - 17 Reserve for Arduino:I2C1_SDA
GPIO_5	Reserve for flash	GPIO_20	J87 - 19 Reserve for Arduino:I2C1_SCL
GPIO_6	J28 - 2 Reserve for Arduino:SPI0_CSK	GPIO_21	J87 - 21
GPIO_7	J28 - 4 Reserve for Arduino:SPI0_CSN	GPIO_22	J87 - 23
GPIO_8	J28 - 6 Reserve for Arduino:SPI0_MISO	GPIO_23	J87 - 25
GPIO_9	J28 - 8 Reserve for Arduino:SPI0_MOSI	GPIO_24	J87 - 12
GPIO_10	J28 - 10	GPIO_42	J28 - 30 Reserve for Arduino:UART1_RX
GPIO_11	J28 - 12	GPIO_44	J28 - 28 Reserve for Arduino:UART1_TX
GPIO_12	J87 - 5	GPIO_48	J87 - 6 Reserve for CM33 UART
GPIO_13	J87 - 7	GPIO_50	J87 - 8 Reserve for CM33 UART

Table 5 GPIO pin multi-function definition

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
PAD_SYSRST_B	NA	PAD_SYSRST_B			PU	Chip hardware fundamental reset pin
SDIO_CLK	0000	GPIO[6]	I/O	I	PD	GPIO 6
	0001 *	SDIO_CLK	I			SDIO Clock
	0010	MSDC0_CLK	O			MSDC Clock
	0011	SPIM0_SCK	O			SPI0 (Master) Clock
	0100	CM33_GPIO_EINT0	I			CM33 EINT0
	0101	DEBUG_0	O			Debug signal
	0110	ANT_SEL0	O			Antenna Select 0
	0111	BGF_EINT_10_B	I			
SDIO_CMD	0000	GPIO[7]	I/O	I	PU	GPIO 7
	0001 *	SDIO_CMD	I/O			SDIO Command
	0010	MSDC0_CMD	I/O			
	0011	SPIM0_CS_N	O			SPI0 (Master) Chip Select
	0100	CM33_GPIO_EINT1	I			CM33 EINT1
	0101	DEBUG_1	O			Debug signal
	0110	ANT_SEL1	O			Antenna Select 1
	0111	PINMUX_EXT_INT_N_IN	I			
SDIO_DAT0	0000	GPIO[8]	I/O	I	PU	GPIO 8
	0001 *	SDIO_DAT0	O			SDIO Data[0]
	0010	MSDC0_DAT0	I/O			MSDC0 data0
	0011	SPIM0_MISO	I			SPI0 (Master) Input
	0100	UART0_RTS	O			
	0101	DEBUG_2	O			Debug signal
	0110	ANT_SEL2	O			Antenna Select 2
	0111	CM33_GPIO_EINT0	I			CM33 EINT0
SDIO_DAT1	0000	GPIO[9]	I/O	I	PU	GPIO 9
	0001 *	SDIO_DAT1	I/O			SDIO Data[1]
	0010	MSDC0_DAT1	I/O			MSDC0 data1
	0011	SPIM0_MOSI	O			SPI0 (Master) Output
	0100	UART0_CTS	I			UART0 Control
	0101	DEBUG_3	O			Debug signal
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT1	I			CM33 EINT1

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
SDIO_DAT2	0000	GPIO[10]	I/O	I	PU	GPIO 10
	0001 *	SDIO_DAT2	I/O			SDIO Data[2]
	0010	MSDC0_DAT2	I/O			MSDC0 data2
	0011	I2SIN_DAT0	I			
	0100	UART0_RX	I			UART0 RX
	0101	DEBUG_4	O			Debug signal
	0110	I2C0_SCL	I/O			
	0111	CM33_GPIO_EINT2	I			CM33 EINT2
SDIO_DAT3	0000	GPIO[11]	I/O	I	PU	GPIO 11
	0001 *	SDIO_DAT3	I/O			SDIO Data[3]
	0010	MSDC0_DAT3	I/O			
	0011	I2SO_DAT0	O			I2SO Data
	0100	UART0_TX	O			UART0 TX
	0101	DEBUG_5	O			Debug signal
	0110	I2C0_SDA	I			I2C0 Data
	0111	CM33_GPIO_EINT3	I			CM33 EINT3
GPIO_B_0	0000	GPIO[12]	I/O	O	PU	GPIO 12
	0001 *	CONN_BGF_UART0_TXD	O			
	0010	MSDC0_RST	O			MSDC0 reset
	0011	CONN_BT_TXD	O			
	0100	WIFI_TXD	O			
	0101	DEBUG_6	O			Debug signal
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT4	I			CM33 EINT4
GPIO_B_1	0000	GPIO[13]	I/O	I	PU	GPIO 13
	0001 *	USB_IDDIG	I			USB OTG ID pin
	0010	SPIM1_SCK	O			SPIM1 (Master) Clock
	0011	I2SO_BCK	O			I2SO BCK
	0100	UART1_RX	I			UART1 RX
	0101	DEBUG_7	O			
	0110	ANT_SEL4	O			Antenna Select 4
	0111	CM33_GPIO_EINT5	I			CM33 EINT5
GPIO_B_2	0000	GPIO[14]	I/O	O	PD	GPIO 14
	0001 *	USB_DRV_VBUS	O			USB OTG host mode
	0010	SPIM1_MOSI	O			SPI1 (Master) Output
	0011	I2SO_LRCK	O			I2SO LRCK
	0100					
	0101	DEBUG_8	O			Debug signal
	0110	ANT_SEL5	O			Antenna Select 5
	0111	CM33_GPIO_EINT6	I			CM33 EINT6
GPIO_B_3	0000	GPIO[15]	I/O	I	PD	GPIO 15
	0001 *	USB_OC	I			USB Host mode over-
	0010	SPIM1_MISO	I			SPI1 (Master) Input
	0011	I2SO_MCK	O			I2STX MCLK
	0100	I2SIN_MCK	O			I2SRX MCK
	0101	DEBUG_9	O			Debug signal
	0110	ANT_SEL6	O			Antenna Select 6
	0111	CM33_GPIO_EINT7	I			CM33 EINT7

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_B_5 (AUXADC)	0000	GPIO[17]	I/O	I	PU	GPIO 17
	0001 *	CONN_BGF_UART0_RXD	I			
	0010	UART0_RX	I			UART0 RX
	0011	TDMIN_MCLK	I			
	0100	DMIC_CLK0	O			DMIC CLK0
	0101	DEBUG_11	O			Debug signal
	0110	ANT_SEL8	O			Antenna Select 8
	0111	CM33_GPIO_EINT9	I			CM33 EINT9
GPIO_B_6 (AUXADC)	0000	GPIO[18]	I/O	O	PU	GPIO 18
	0001 *	CONN_BT_TXD	O			
	0010	UART0_TX	O			UART0 TX
	0011	TDMIN_BCK	I			
	0100	DMIC_DAT0	I			DMIC DAT0
	0101	UART1_RX	I			UART1 Control
	0110	IR_IN	I			
	0111	CM33_GPIO_EINT10	I			CM33 EINT10
GPIO_B_7 (AUXADC)	0000	GPIO[19]	I/O	O	PD	GPIO 19
	0001 *	WIFI_TXD	O			
	0010	UART0_RTS	O			UART0 Control
	0011	I2C1_SDA	I			I2C1 Data
	0100	I2SIN_LRCK	O			I2SRX LRCK
	0101	UART1_TX	O			UART1 TX
	0110	PTA_EXT_IF_FREQ	I			
	0111	CM33_GPIO_EINT11	I			CM33 EINT11
GPIO_B_8 (AUXADC)	0000	GPIO[20]	I/O	I	PD	GPIO 20
	0001 *	CONN_WF_MCU_AICE_TCKC	I			
	0010	UART0_CTS	I			UART0 Control
	0011	I2C1_SCL	I			I2C1 clock
	0100	I2SIN_BCK	O			I2SRX BCK
	0101	DEBUG_12	O			Debug signal
	0110	PTA_EXT_IF_FACT	I			
	0111	CM33_GPIO_EINT12	I			CM33 EINT12
GPIO_B_9 (AUXADC)	0000	GPIO[21]	I/O	I	PU	GPIO 21
	0001 *	CONN_WF_MCU_AICE_TMSC	I/O			
	0010	PTA_EXT_IF_PRI	I/O			
	0011	TDMIN_LRCK	I/O			
	0100	DMIC_DAT1	I			DMIC DAT1
	0101	DEBUG_13	O			Debug signal
	0110	ANT_SEL9	O			Antenna Select 9
	0111	CM33_GPIO_EINT13	I			CM33 EINT13
GPIO_B_10 (AUXADC)	0000	GPIO[22]	I/O	I	PD	GPIO 22
	0001 *	CONN_BGF_MCU_AICE_TCKC	I			
	0010	PTA_EXT_IF_WLAN_ACT	O			
	0011	TDMIN_DI	I			
	0100	DMIC_DAT2	I			DMIC Data2
	0101	DEBUG_14	O			Debug signal
	0110	ANT_SEL10	O			Antenna Select 10
	0111	CM33_GPIO_EINT14	I			CM33 EINT14
GPIO_B_11 (AUXADC)	0000	GPIO[23]	I/O	I	PU	GPIO 23
	0001 *	CONN_BGF_MCU_AICE_TMSC	I/O			
	0010	DSP_URXD0	I			
	0011	I2C0_SDA	I/O			I2C0 Data
	0100	DMIC_DAT3	I			DMIC Data3
	0101	DEBUG_15	O			Debug signal
	0110	ANT_SEL11	O			Antenna Select 11
	0111	CM33_GPIO_EINT15				CM33 EINT15

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
GPIO_B_12 (AUXADC)	0000	GPIO[24]	I/O	O	PU	GPIO 24
	0001 *	ADSP_JTAG_TDO	O			DSP JTAG
	0010	DSP_UTXD0	O			
	0011	I2C0_SCL	I/O			I2C0 clock
	0100	DMIC_CLK1	O			DMIC CLK1
	0101	CM33_UART_TX	O			CM33 UART TX
	0110	ANT_SEL12	O			Antenna Select 12
	0111	CM33_GPIO_EINT16	I			CM33 EINT16
GPIO_T_1	0000	GPIO[42]	I/O	I	PD	GPIO 42
	0001	CM33_RSVD1	I			
	0010 *	DBSYS_SWCLK_TCLK	I			CM33 JTAG, CM33_SWD
	0011	UART1_RX	I			UART1 RX
	0100	UART0_RX	I			UART0 RX
	0101	DSP_URXD0	I			
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT1	I			CM33 EINT1
GPIO_T_3	0000	GPIO[44]	I/O	I	PD	GPIO 44
	0001	CM33_RSDV3	I/O			
	0010 *	DBSYS_SWDIO_TMS	I			CM33 JTAG, CM33_SWD
	0011	UART1_TX	O			UART1 TX
	0100	UART0_TX	O			UART0 TX
	0101	DSP_UTXD0	O			
	0110	ANT_SEL5	O			Antenna Select 5
	0111	CM33_GPIO_EINT18	I			CM33 EINT18
GPIO_T_7	0000	GPIO[48]	I/O	I	PU	GPIO 48
	0001 *	CM33_UART_RX	I			
	0010	CM33_TRACE_D2	O			
	0011	KEYPAD_KPROW_1	I/O			
	0100	DSP_URXD0	I			
	0101	PWM_3	O			PWM 3
	0110	ANT_SEL9	O			Antenna Select 9
	0111	AUDIO_DEBUG_IN_0	I			
GPIO_T_9	0000	GPIO[50]	I/O	O	PU	GPIO 50
	0001 *	CM33_UART_TX	O			
	0010	CM33_TRACE_D0	O			
	0011	KEYPAD_KPCOL_0	I			
	0100	DSP_UTXD0	O			
	0101	PWM_5	O			PWM 5
	0110	ANT_SEL11	O			Antenna Select 11
	0111	AUDIO_DEBUG_IN_2	I			

Federal Communication Commission Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

IMPORTANT NOTE:

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Country Code selection feature to be disabled for products marketed to the US/CANA

Integration instructions for host product manufacturers

Applicable FCC rules to module

FCC Part 15.247

FCC Part 15.407

Summarize the specific operational use conditions

The module is must be installed in mobile device.

This device is intended only for OEM integrators under the following conditions:

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

IMPORTANT NOTE: In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization. The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as show in this manual.

Limited module procedures

Not applicable

Trace antenna designs

Not applicable

RF exposure considerations

20 cm separation distance and co-located issue shall be met as mentioned in "Summarize the specific operational use conditions".

Product manufacturer shall provide below text in end-product manual

"This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body."

Antennas

Brand Name	Model Name	Antenna Type	Antenna Gain	Antenna Connector
SINBON	IAHA202205004	PCB Dipole	4.99 dBi	RF Mini Plug
SINBON	IAHA202205005	FPC Dipole	4.36 dBI	RF Mini Plug

Label and Compliance Information

Product manufacturers need to provide a physical or e-label stating
"Contains FCC ID: 2ADWC-AI7931LD" with finished product

Information on Test Modes and Additional Testing Requirements

Test tool: termite-3.3 shall be used to set the module to transmit continuously.

Additional Testing, Part 15 Subpart B Disclaimer

The module is only FCC authorized for the specific rule parts listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.