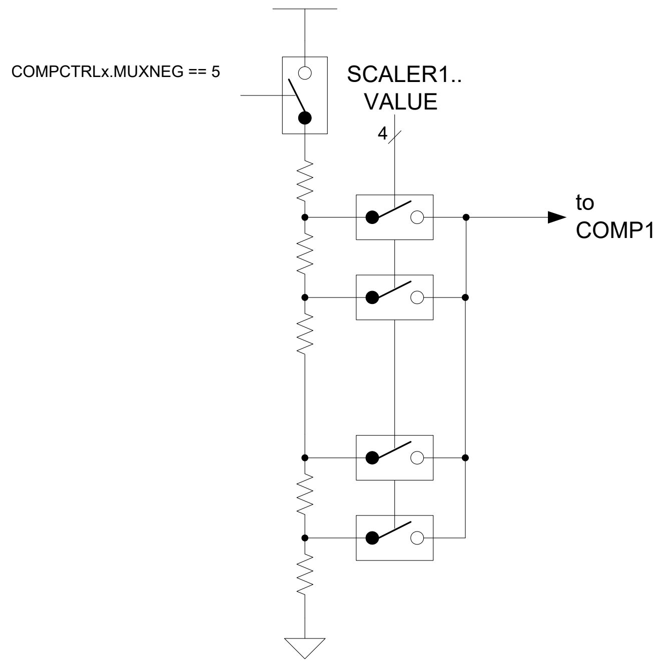
39.5.5 VDD Scaler

The VDD scaler generates a reference voltage that is a fraction of the device's supply voltage with 64 levels. The programmable VDD scaler (PLVD Scaler) is available for AC_CMP1 only. AC_CMP0 uses a fixed VDD/2 reference. The scaler of a comparator is enabled when the Negative Input Mux bit field or the Positive Input Mux in the respective Comparator Control register (COMPCTRLx.MUXNEG) is set to `0x5` and the comparator is enabled. The voltage of each channel is selected by the Value bit field in the SCALER1 registers (SCALER1.VALUE) using the VDD resistor ladder.

Figure 39-5. PLVD Scaler



39.5.6 Filtering

The output of the comparators can be filtered digitally to reduce noise. The filtering is determined by the Filter Length bits in the Comparator Control x register (COMPCTRLx.FLEN), and is independent for each comparator. Filtering is selectable from none, 3-bit majority (N=3) or 5-bit majority (N=5) functions. Any change in the comparator output is considered valid only if N/2+1 out of the last N samples agree. The filter sampling rate is the GCLK_AC frequency.

Note that filtering creates an additional delay of N-1 sampling cycles from when a comparison is started until the comparator output is validated. For Continuous mode, the first valid output will occur when the required number of filter samples is taken. Subsequent outputs will be generated every cycle based on the current sample plus the previous N-1 samples, as shown in Figure 39-6. For Single-shot mode, the comparison completes after the Nth filter sample, as shown in Figure 39-7.

Figure 39-6. Continuous Mode Filtering

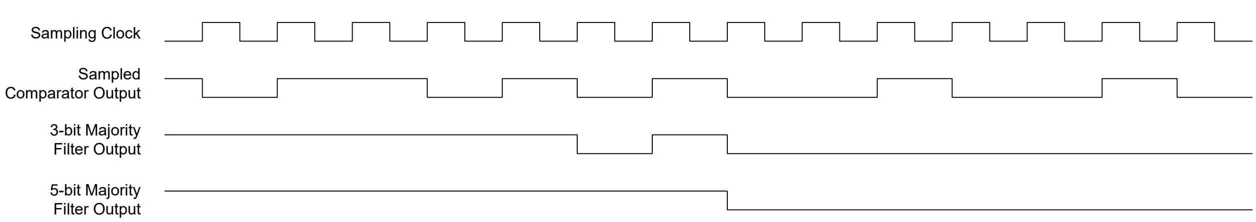
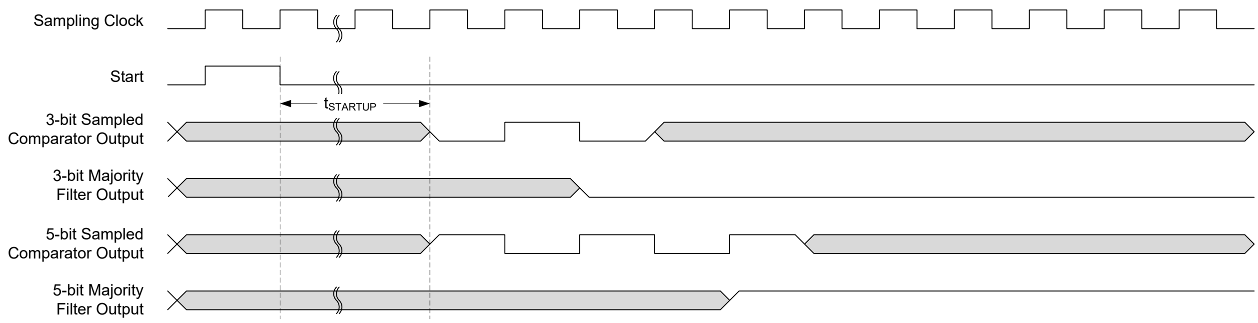


Figure 39-7. Single-Shot Filtering



During Sleep modes, filtering is supported only for single-shot measurements. Filtering must be disabled if continuous measurements will be done during Sleep modes, or the resulting interrupt/event may be generated incorrectly.

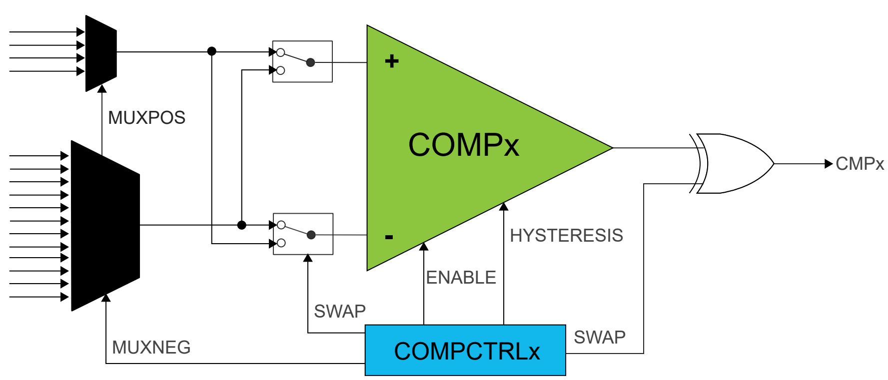
39.5.7 Comparator Output

The output of each comparator can be routed to an I/O pin by setting the Output bit group in the Comparator Control x register (COMPCTRLx.OUT). To get the analog comparator output on the I/O line, CFGCON1.CMP0_OE/CFGCON1.CMP1_OE also needs to be set or enabled. This allows the comparator to be used by external circuitry. Either the raw, non-synchronized output of the comparator or the GCLK_AC-synchronized version, including filtering, can be used as the I/O signal source. The output appears on the corresponding AC_CMPx pin. The AC_CMP1 can be output on an alternate pin by configuring the CFGCON0.ACCMP1_ALTEN configuration.

39.5.8 Offset Compensation

The Swap bit in the Comparator Control registers (COMPCTRLx.SWAP) controls switching of the input signals to a comparator's positive and negative terminals. When the comparator terminals are swapped, the output signal from the comparator is also inverted, as shown in Figure 39-8. This allows the user to measure or compensate for the comparator input offset voltage. As part of the input selection, COMPCTRLx.SWAP can be changed only while the comparator is disabled.

Figure 39-8. Input Swapping for Offset Compensation



39.5.9 DMA Operation

Not applicable.

39.5.10 Interrupts

The AC has the following interrupt sources:

- Comparator (COMP0, COMP1): Indicates a change in comparator status
- Window (WIN0): Indicates a change in the window status

Comparator interrupts are generated based on the conditions selected by the Interrupt Selection bit group in the Comparator Control registers (COMPCTRLx.INTSEL). Window interrupts are generated based on the conditions selected by the Window Interrupt Selection bit group in the Window Control register (WINCTRL.WINTSEL[1:0]).

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the interrupt condition occurs. Each interrupt can be individually enabled by writing a one to the corresponding bit in the Interrupt Enable Set (INTENSET) register and disabled by writing a one to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled or the AC is Reset. See *INTFLAG* register from Related Links for details on how to clear interrupt flags. All interrupt requests from the peripheral are OR'ed together on the system level to generate one combined interrupt request to the NVIC. The user must read the INTFLAG register to determine which interrupt condition is present. See *Nested Vector Interrupt Controller (NVIC)* from Related Links.

Note: Interrupts must be globally enabled for interrupt requests to be generated.

Related Links
Nested Vector Interrupt Controller (NVIC)
INTFLAG
Interrupt Flag Status and Clear

39.5.11 Events

The AC can generate the following output events:

- Comparator (COMP0, COMP1): Generated as a copy of the comparator status
- Window (WIN0): Generated as a copy of the window inside/outside status

Writing a one to an Event Output bit in the Event Control Register (EVCTRL.xxEO) enables the corresponding output event. Writing a zero to this bit disables the corresponding output event. See *Event System (EVSYS)* from Related Links for details on how to configure the Event System.

The AC can take the following action on an input event:

- Start comparison (START0, START1): Start a comparison

Writing a one to an Event Input bit into the Event Control register (EVCTRL.COMPEIx) enables the corresponding action on an input event. Writing a zero to this bit disables the corresponding action on an input event. Note that if several events are connected to the AC, the enabled action will be taken on any of the incoming events. See *Event System (EVSYS)* from Related Links for details on how to configure the Event System.

When EVCTRL.COMPEIx is one, the event will start a comparison on COMPx after the start-up time delay. In normal mode, each comparator responds to its corresponding input event independently. For a pair of comparators in window mode, either comparator event will trigger a comparison on both comparators simultaneously.

Related Links
Event System (EVSYS)

39.5.12 Sleep Mode Operation

The Run in Standby bits in the Comparator x Control registers (COMPCTRLx.RUNSTDBY) control the behavior of the AC during standby sleep mode. Each RUNSTDBY bit controls one comparator. When the bit is zero, the comparator is disabled during sleep, but maintains its current configuration. When the bit is one, the comparator continues to operate during sleep. Note that when RUNSTDBY is zero, the analog blocks are powered off for the lowest power consumption. This necessitates a start-up time delay when the system returns from sleep.

For Window Mode operation, both comparators in a pair must have the same RUNSTDBY configuration.

When RUNSTDBY is one, any enabled AC interrupt source can wake up the CPU. The AC can also be used during sleep modes where the clock used by the AC is disabled, provided that the AC is still powered (not in shutdown). In this case, the behavior is slightly different and depends on the measurement mode, as listed in Table 39-2.

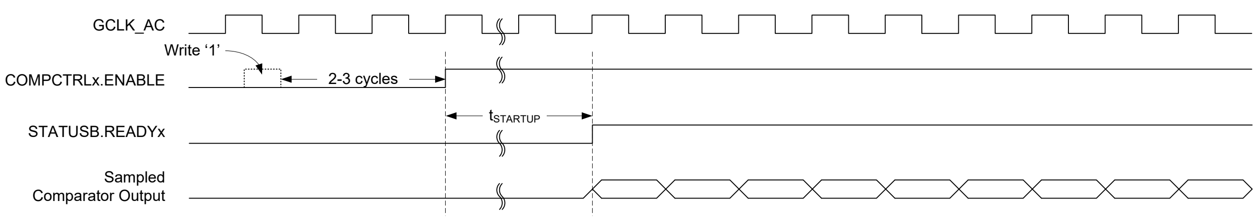
Table 39-2. Sleep Mode Operation

COMPCTRLx.MODE	RUNSTDBY=0	RUNSTDBY=1
0 (Continuous)	COMPx disabled	GCLK_AC stopped, COMPx enabled
1 (Single-shot)	COMPx disabled	GCLK_AC stopped, COMPx enabled only when triggered by an input event

39.5.12.1 Continuous Measurement during Sleep

When a comparator is enabled in continuous measurement mode and GCLK_AC is disabled during sleep, the comparator will remain continuously enabled and will function asynchronously. The current state of the comparator is asynchronously monitored for changes. If an edge matching the interrupt condition is found, GCLK_AC is started to register the interrupt condition and generate events. If the interrupt is enabled in the Interrupt Enable registers (INTENCLR/SET), the AC can wake up the device; otherwise GCLK_AC is disabled until the next edge detection. Filtering is not possible with this configuration.

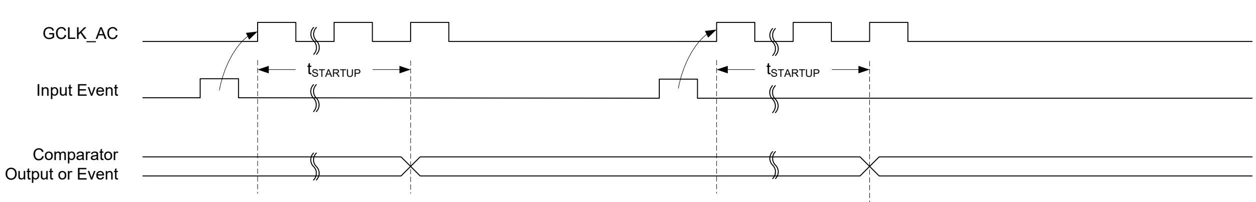
Figure 39-9. Continuous Mode SleepWalking



39.5.12.2 Single-Shot Measurement during Sleep

For low-power operation, event-triggered measurements can be performed during sleep modes. When the event occurs, the CRU will start GCLK_AC. The comparator is enabled and, after the start-up time has passed, a comparison is done, with filtering if desired, and the appropriate peripheral events and interrupts are also generated as shown in the following figure. The comparator and GCLK_AC are, then, disabled again automatically unless configured to wake the system from sleep. Filtering is allowed with this configuration.

Figure 39-10. Single-Shot SleepWalking



39.5.13 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset bit in Control register (CTRLA.SWRST)
- Enable bit in Control register (CTRLA.ENABLE)
- Enable bit in Comparator Control register (COMPCTRLn.ENABLE)

The following registers are synchronized when written:

- Window Control register (WINCTRL)

Required write synchronization is denoted by the "Write-Synchronized" property in the register description.

39.6 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0							ENABLE	SWRST
0x01	CTRLB	7:0							START1	START0
0x02	EVCTRL	7:0				WINEO0			COMPEO1	COMPEO0
		15:8			INVEI1	INVEI0			COMPEI1	COMPEI0
0x04	INTENCLR	7:0				WIN0			COMP1	COMP0
0x05	INTENSET	7:0				WIN0			COMP1	COMP0
0x06	INTFLAG	7:0				WIN0			COMP1	COMP0
0x07	STATUSA	7:0			WSTATE0[1:0]				STATE1	STATE0
0x08	STATUSB	7:0							READY1	READY0
0x09	DBGCTRL	7:0								DBGRUN
0x0A	WINCTRL	7:0						WINTSEL0[1:0]		WEN0
0x0B ... 0x0C	Reserved									
0x0D	SCALER1	7:0					VALUE[3:0]			
0x0E ... 0x0F	Reserved									
0x10	COMPCTRL0	7:0		RUNSTDBY		INTSEL[1:0]		SINGLE	ENABLE	
		15:8	SWAP	MUXPOS[2:0]				MUXNEG[2:0]		
		23:16								
		31:24			OUT[1:0]			FLEN[2:0]		
0x14	COMPCTRL1	7:0		RUNSTDBY		INTSEL[1:0]		SINGLE	ENABLE	
		15:8	SWAP	MUXPOS[2:0]				MUXNEG[2:0]		
		23:16								
		31:24			OUT[1:0]			FLEN[2:0]		
0x18 ... 0x1F	Reserved									
0x20	SYNCBUSY	7:0				COMPCTRL1	COMPCTRL0	WINCTRL	ENABLE	SWRST
		15:8								
		23:16								
		31:24								

39.7 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write-protection is denoted by the “PAC Write-Protection” property in each individual register description. See *Register Access Protection* from Related Links.

Some registers are synchronized when read and/or written. Synchronization is denoted by the “Write-Synchronized” or the “Read-Synchronized” property in each individual register description. See *Synchronization* from Related Links.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

Related Links

Register Access Protection
Synchronization

39.7.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
							ENABLE	SWRST
Access							R/W	W
Reset							0	0

Bit 1 – ENABLE Enable

Due to synchronization, there is delay from updating the register until the peripheral is enabled/disabled. The value written to CTRL.ENABLE will read back immediately and the corresponding bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE is cleared when the peripheral is enabled/disabled.

Value	Description
0	The AC is disabled.
1	The AC is enabled. Each comparator must also be enabled individually by the Enable bit in the Comparator Control register (COMPCTRLn.ENABLE).

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.
Writing a '1' to this bit resets all registers in the AC to their initial state, and the AC will be disabled.
Writing a '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.
Due to synchronization, there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

39.7.2 Control B

Name: CTRLB
Offset: 0x01
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
							START1	START0
Access							R/W	R/W
Reset							0	0

Bits 0, 1 – STARTx Comparator x Start Comparison
Writing a '0' to this field has no effect.
Writing a '1' to STARTx starts a single-shot comparison on COMPx if both the Single-Shot and Enable bits in the Comparator x Control Register are '1' (COMPCTRLx.SINGLE and COMPCTRLx.ENABLE). If comparator x is not implemented, or if it is not enabled in single-shot mode, Writing a '1' has no effect.
This bit always reads as zero.

39.7.3 Event Control

Name: EVCTRL
Offset: 0x02
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
			INVEI1	INVEI0			COMPEI1	COMPEI0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	7	6	5	4	3	2	1	0
				WINEO0			COMPEO1	COMPEO0
Access				R/W			R/W	R/W
Reset				0			0	0

Bits 12, 13 – INVEIx Inverted Event Input Enable x

Value	Description
0	Incoming event is not inverted for comparator x.
1	Incoming event is inverted for comparator x.

Bits 8, 9 – COMPEIx Comparator x Event Input

Note that several actions can be enabled for incoming events. If several events are connected to the peripheral, the enabled action will be taken for any of the incoming events. There is no way to tell which of the incoming events caused the action.

These bits indicate whether a comparison will start or not on any incoming event.

Value	Description
0	Comparison will not start on any incoming event.
1	Comparison will start on any incoming event.

Bit 4 – WINEO0 Window 0 Event Output Enable

These bits indicate whether the window 0 function can generate a peripheral event or not.

Value	Description
0	Window 0 Event is disabled.
1	Window 0 Event is enabled.

Bits 0, 1 – COMPEOx Comparator x Event Output Enable

These bits indicate whether the comparator x output can generate a peripheral event or not.

Value	Description
0	COMPx event generation is disabled.
1	COMPx event generation is enabled.

39.7.4 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
				WIN0			COMP1	COMP0
Access				R/W			R/W	R/W
Reset				0			0	0

Bit 4 – WIN0 Window 0 Interrupt Enable
Reading this bit returns the state of the Window 0 interrupt enable.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit disables the Window 0 interrupt.

Value	Description
0	The Window 0 interrupt is disabled.
1	The Window 0 interrupt is enabled.

Bits 0, 1 – COMPx Comparator x Interrupt Enable
Reading this bit returns the state of the Comparator x interrupt enable.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit disables the Comparator x interrupt.

Value	Description
0	The Comparator x interrupt is disabled.
1	The Comparator x interrupt is enabled.

39.7.5 Interrupt Enable Set

Name: INTENSET
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
				WIN0			COMP1	COMP0
Access				R/W			R/W	R/W
Reset				0			0	0

Bit 4 – WIN0 Window 0 Interrupt Enable
Reading this bit returns the state of the Window 0 interrupt enable.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit enables the Window 0 interrupt.

Value	Description
0	The Window 0 interrupt is disabled.
1	The Window 0 interrupt is enabled.

Bits 0, 1 – COMPx Comparator x Interrupt Enable
Reading this bit returns the state of the Comparator x interrupt enable.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Ready interrupt bit and enable the Ready interrupt.

Value	Description
0	The Comparator x interrupt is disabled.
1	The Comparator x interrupt is enabled.

39.7.6 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x06
Reset: 0x00
Property: –

Bit	7	6	5	4	3	2	1	0
				WIN0			COMP1	COMP0
Access				R/W			R/W	R/W
Reset				0			0	0

Bit 4 – WIN0 Window 0

This flag is set according to the Window 0 Interrupt Selection bit group in the WINCTRL register (WINCTRL.WINTSELx) and will generate an interrupt if INTENCLR/SET.WINx is also one.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Window 0 interrupt flag.

Bits 0, 1 – COMPx Comparator x

Reading this bit returns the status of the Comparator x interrupt flag. If comparator x is not implemented, COMPx always reads as zero.
This flag is set according to the Interrupt Selection bit group in the Comparator x Control register (COMPCTRLx.INTSEL) and will generate an interrupt if INTENCLR/SET.COMPx is also one.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Comparator x interrupt flag.

39.7.7 Status A

Name: STATUSA
Offset: 0x07
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
			WSTATE0[1:0]				STATE1	STATE0
Access			R	R			R	R
Reset			0	0			0	0

Bits 5:4 – WSTATE0[1:0] Window 0 Current State
These bits show the current state of the signal if the window 0 mode is enabled.

Value	Name	Description
0x0	ABOVE	Signal is above window
0x1	INSIDE	Signal is inside window
0x2	BELOW	Signal is below window
0x3		Reserved

Bits 0, 1 – STATEx Comparator x Current State
This bit shows the current state of the output signal from COMPx. STATEx is valid only when STATUSB.READYx is one.

39.7.8 Status B

Name: STATUSB
Offset: 0x08
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
							READY1	READY0
Access							R	R
Reset							0	0

Bits 0, 1 – READYx Comparator x Ready
This bit is cleared when the comparator x output is not ready.
This bit is set when the comparator x output is ready.

39.7.9 Debug Control

Name: DBGCTRL
Offset: 0x09
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN Debug Run
This bit is not reset by a software reset.
This bits controls the functionality when the CPU is halted by an external debugger.

Value	Description
0	The AC is halted when the CPU is halted by an external debugger. Any on-going comparison will complete.
1	The AC continues normal operation when the CPU is halted by an external debugger.

39.7.10 Window Control

Name: WINCTRL
Offset: 0x0A
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
						WINTSEL0[1:0]		WEN0
Access						R/W	R/W	R/W
Reset						0	0	0

Bits 2:1 – WINTSEL0[1:0] Window 0 Interrupt Selection
These bits configure the interrupt mode for the comparator window 0 mode.

Value	Name	Description
0x0	ABOVE	Interrupt on signal above window
0x1	INSIDE	Interrupt on signal inside window
0x2	BELOW	Interrupt on signal below window
0x3	OUTSIDE	Interrupt on signal outside window

Bit 0 – WEN0 Window 0 Mode Enable

Value	Description
0	Window mode is disabled for comparators 0 and 1.
1	Window mode is enabled for comparators 0 and 1.

39.7.11 Scaler 1

Name: SCALER1
Offset: 0x0D
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
					VALUE[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – VALUE[3:0] Scaler Value

These bits define the scaling factor for channel 1 of the VDD voltage scaler. The output voltage, V_{SCALE}, is:

$$V_{\text{SCALE}} = V_{DD} \times \left(\frac{R\_Bottom}{R\_Total}\right)$$

Where, R_Total = 900.
Refer to the following table for R_Bottom for different VALUE[3:0]
For example, V_{SCALE} for VALUE[3:0] = 0x02 at VDD = 3.3V

$$V_{\text{SCALE}} = 3.3 \times \left(\frac{598.5}{900}\right) = 2.1945V$$

Table 39-3. Scaler Value

Value[3:0]	R_Bottom
0x0	Reserved
0x1	Reserved
0x2	598.5
0x3	634.5
0x4	306
0x5	324
0x6	328.5
0x7	360
0x8	387
0x9	400.5
0xA	432
0xB	450
0xC	468
0xD	490.5
0xE	481.5
0xF	External Reference on LVDIN pin

39.7.12 Comparator Control n

Name: COMPCTRL
Offset: 0x10 + n*0x04 [n=0..1]
Reset: 0x00000000
Property: PAC Write-Protection

Note: 32 pins variants only have COMP1.

Bit	31	30	29	28	27	26	25	24
			OUT[1:0]			FLEN[2:0]		
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	SWAP	MUXPOS[2:0]				MUXNEG[2:0]		
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
		RUNSTDBY		INTSEL[1:0]		SINGLE	ENABLE	
Access		R/W		R/W	R/W	R/W	R/W	
Reset		0		0	0	0	0	

Bits 29:28 – OUT[1:0] Output

These bits configure the output selection for comparator n. COMPCTRLn.OUT can be written only while COMPCTRLn.ENABLE is zero.
Note: For internal use of the comparison results by the CCL, this must be 0x1 or 0x2.

These bits are not synchronized.

Value	Name	Description
0x0	OFF	The output of COMPn is not routed to the COMPn I/O port
0x1	ASYNC	The asynchronous output of COMPn is routed to the COMPn I/O port
0x2	SYNC	The synchronous output (including filtering) of COMPn is routed to the COMPn I/O port
0x3	N/A	Reserved

Bits 26:24 – FLEN[2:0] Filter Length

These bits configure the filtering for comparator n. COMPCTRLn.FLEN can only be written while COMPCTRLn.ENABLE is zero.
These bits are not synchronized.

Value	Name	Description
0x0	OFF	No filtering
0x1	MAJ3	3-bit majority function (2 of 3)
0x2	MAJ5	5-bit majority function (3 of 5)
0x3-0x7	N/A	Reserved

Bit 15 – SWAP Swap Inputs and Invert

This bit swaps the positive and negative inputs to COMPn and inverts the output. This function can be used for offset cancellation. COMPCTRLn.SWAP can be written only while COMPCTRLn.ENABLE is zero.
These bits are not synchronized.

Value	Description
0	The output of MUXPOS connects to the positive input, and the output of MUXNEG connects to the negative input.
1	The output of MUXNEG connects to the positive input, and the output of MUXPOS connects to the negative input.

Bits 14:12 – MUXPOS[2:0] Positive Input Mux Selection

These bits select which input will be connected to the positive input of comparator n.
COMPCTRLn.MUXPOS can be written only while COMPCTRLn.ENABLE is zero.
These bits are not synchronized.

Value	Name	Description
0x0	PIN0	I/O pin 0
0x1	PIN1	I/O pin 1
0x2	PIN2	I/O pin 2
0x3	PIN3	I/O pin 3
0x4	VSCALE	VDD scaler
0x5-0x7	-	Reserved

Bits 10:8 – MUXNEG[2:0] Negative Input Mux Selection

These bits select which input will be connected to the negative input of comparator n.
COMPCTRLn.MUXNEG can only be written while COMPCTRLn.ENABLE is zero.
These bits are not synchronized.

Value	Name	Description
0x0	PIN0	I/O pin 0
0x1	PIN1	I/O pin 1
0x2	PIN2	I/O pin 2
0x3	PIN3	I/O pin 3
0x4	GND	Ground
0x5	VSCALE	VDD scaler
0x6	BANDGAP	Internal bandgap voltage

Bit 6 – RUNSTDBY Run in Standby

This bit controls the behavior of the comparator during standby sleep mode.
This bit is not synchronized

Value	Description
0	The comparator is disabled during sleep.
1	The comparator continues to operate during sleep.

Bits 4:3 – INTSEL[1:0] Interrupt Selection

These bits select the condition for comparator n to generate an interrupt or event.
COMPCTRLn.INTSEL can be written only while COMPCTRLn.ENABLE is zero.
These bits are not synchronized.

Value	Name	Description
0x0	TOGGLE	Interrupt on comparator output toggle
0x1	RISING	Interrupt on comparator output rising
0x2	FALLING	Interrupt on comparator output falling
0x3	EOC	Interrupt on end of comparison (single-shot mode only)

Bit 2 – SINGLE Single-Shot Mode

This bit determines the operation of comparator n. COMPCTRLn.SINGLE can be written only while COMPCTRLn.ENABLE is zero.
These bits are not synchronized.

Value	Description
0	Comparator n operates in continuous measurement mode.
1	Comparator n operates in single-shot mode.

Bit 1 – ENABLE Enable

Writing a zero to this bit disables comparator n.
Writing a one to this bit enables comparator n.
Due to synchronization, there is a delay from updating the register until the comparator is enabled/ disabled. The value written to COMPCTRLn.ENABLE will read back immediately after being written. SYNCBUSY.COMPCTRLn is set. SYNCBUSY.COMPCTRLn is cleared when the peripheral is enabled/ disabled.
Writing a one to COMPCTRLn.ENABLE will prevent further changes to the other bits in COMPCTRLn. These bits remain protected until COMPCTRLn.ENABLE is written to zero and the write is synchronized.

39.7.13 Synchronization Busy

Name: SYNCBUSY
Offset: 0x20
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
				COMPCTRL1	COMPCTRL0	WINCTRL	ENABLE	SWRST
Access				R	R	R	R	R
Reset				0	0	0	0	0

Bits 3, 4 – COMPCTRLx COMPCTRLx Synchronization Busy

This bit is cleared when the synchronization of the COMPCTRLx register between the clock domains is complete.
This bit is set when the synchronization of the COMPCTRLx register between clock domains is started.

Bit 2 – WINCTRL WINCTRL Synchronization Busy

This bit is cleared when the synchronization of the WINCTRL register between the clock domains is complete.
This bit is set when the synchronization of the WINCTRL register between clock domains is started.

Bit 1 – ENABLE Enable Synchronization Busy

This bit is cleared when the synchronization of the CTRLA.ENABLE bit between the clock domains is complete.
This bit is set when the synchronization of the CTRLA.ENABLE bit between clock domains is started.

Bit 0 – SWRST Software Reset Synchronization Busy

This bit is cleared when the synchronization of the CTRLA.SWRST bit between the clock domains is complete.
This bit is set when the synchronization of the CTRLA.SWRST bit between clock domains is started.

40. Timer/Counter (TC)

40.1 Overview

There are up to four TC peripheral instances. Up to four TCs (TC[3:0]) are in PD1, whereas TC4, present in all device configurations, is always located in power domain PD0.

Each TC consists of a counter, a prescaler, compare/capture channels and control logic. The counter can be set to count events or clock pulses. The counter, together with the compare/capture channels, can be configured to time stamp input events or IO pin edges, allowing for capturing of frequency and/or pulse width.

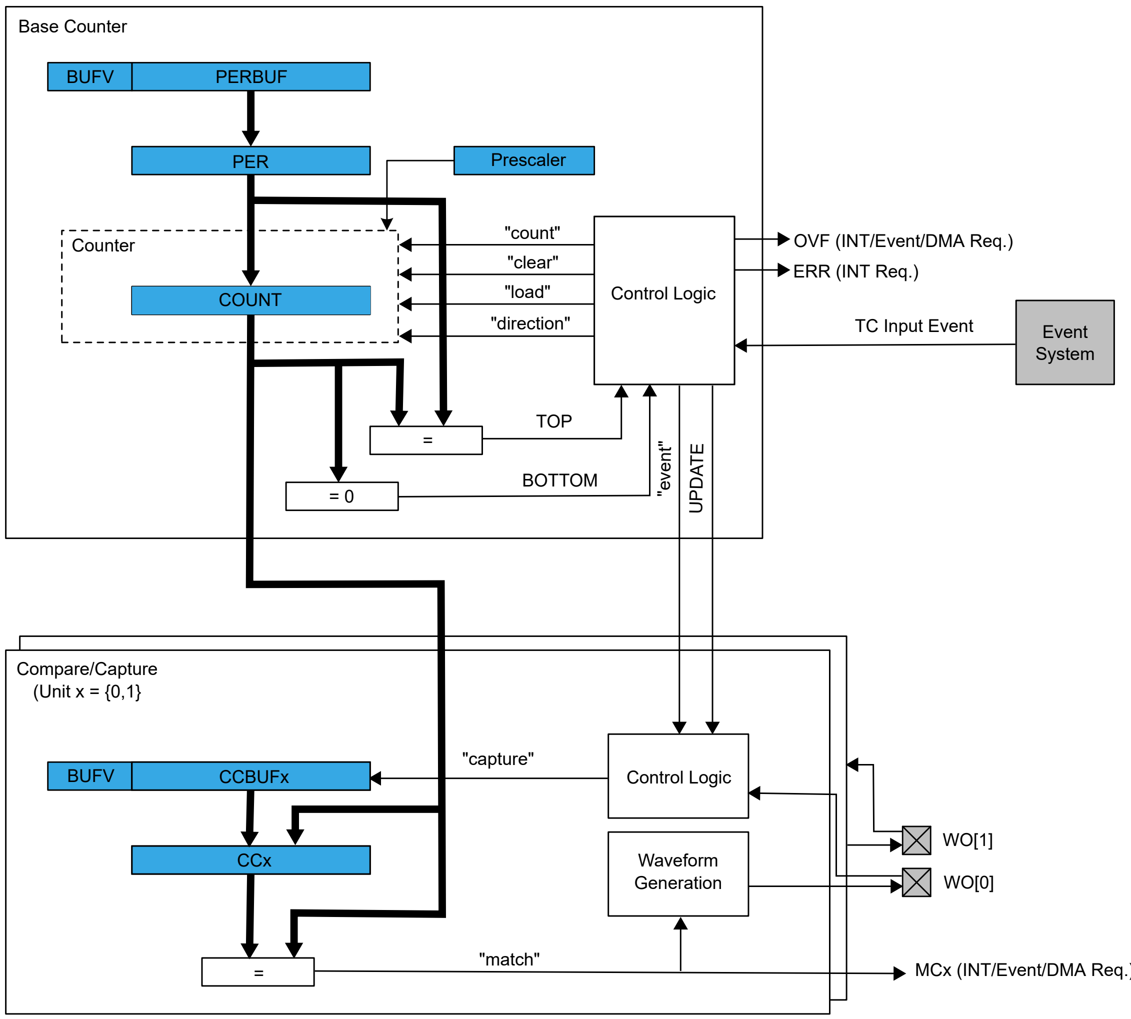
A TC can also perform waveform generation, such as frequency generation and pulse-width modulation.

40.2 Features

- Selectable Configuration
  - 8-, 16- or 32-bit TC operation, with compare/capture channels
- 2 Compare/Capture Channels (CC) with:
  - Double buffered timer period setting (in 8-bit mode only)
  - Double buffered compare channel
- Waveform Generation
  - Frequency generation
  - Single-slope pulse-width modulation
- Input Capture
  - Event / IO pin edge capture
  - Frequency capture
  - Pulse-width capture
  - Time-stamp capture
  - Minimum and maximum capture
- One Input Event
- Interrupts/Output Events ON:
  - Counter overflow/underflow
  - Compare match or capture
- Internal Prescaler
- DMA Support

40.3 Block Diagram

Figure 40-1. Timer/Counter Block Diagram



40.4 Signal Description

Table 40-1. Signal Description for TC

Signal Name	Type	Description
WO[1:0]	Digital output	Waveform output
	Digital input	Capture input

See *I/O Ports and Peripheral Pin Select (PPS)* from Related Links for details on the pin mapping for this peripheral. One signal can be mapped on several pins.

Related Links

I/O Ports and Peripheral Pin Select (PPS)

40.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

40.5.1 I/O Lines

In order to use the I/O lines of this peripheral, the I/O pins must be configured using the I/O Peripheral Pin Select (PPS).

40.5.2 Power Management

This peripheral can continue to operate in any Sleep mode where its source clock is running. The interrupts can wake up the device from Sleep modes. Events connected to the event system can trigger other operations in the system without exiting Sleep modes.

40.5.3 Clocks

The TC bus clocks (PB1_CLK) can be enabled and disabled in the PMD Registers. For more details and default status of this clock, see *Peripheral Module Disable Register (PMD)* from Related Links.

The generic clocks (GCLK_TCx) are asynchronous to the user interface clock (PB1_CLK). Due to this asynchronicity, accessing certain registers will require synchronization between the clock domains.

Note: Two instances of the TC may share a peripheral clock channel. In this case, they cannot be set to different clock frequencies. See *System and Peripheral Clock Generation (CLKGEN)* from Related Links to identify shared peripheral clocks.

Related Links
System and Peripheral Clock Generation (CLKGEN)
Peripheral Module Disable Register (PMD)

40.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral, the DMAC must be configured first (see *Direct Memory Access Controller (DMAC)* from Related Links).

Related Links
Direct Memory Access Controller (DMAC)

40.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. In order to use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. See *Nested Vector Interrupt Controller (NVIC)* from Related Links.

Related Links
Nested Vector Interrupt Controller (NVIC)

40.5.6 Events

The events of this peripheral are connected to the Event System.

Related Links
Event System (EVSYS)

40.5.7 Debug Operation

When the CPU is halted in Debug mode, this peripheral will halt normal operation. This peripheral can be forced to continue operation during debugging. For more details, see *DBGCTRL* from Related Links.

Related Links

DBGCTRL

Debug Control

40.5.8 Register Access Protection

Registers with write access can be optionally write-protected by the Peripheral Access Controller (PAC), except for the following:

- Interrupt Flag Status and Clear register (INTFLAG)
- Status register (STATUS)
- Period and Period Buffer registers (PER, PERBUF)
- Compare/Capture Value registers and Compare/Capture Value Buffer registers (CCx, CCBUFx)

Note: Optional write protection is indicated by the "PAC Write Protection" property in the register description.

Write protection does not apply for accesses through an external debugger.

40.5.9 Analog Connections

Not applicable.

40.6 Functional Description

40.6.1 Principle of Operation

The following definitions are used throughout the documentation:

Table 40-2. Timer/Counter Definitions

Name	Description
TOP	The counter reaches TOP when it becomes equal to the highest value in the count sequence. The TOP value can be the same as Period (PER) or the Compare Channel 0 (CC0) register value depending on the waveform generator mode in Waveform Output Operations. See *Waveform Output Operations* from Related Links.
ZERO	The counter is ZERO when it contains all zeros.
MAX	The counter reaches MAX when it contains all ones.
UPDATE	The timer/counter signals an update when it reaches ZERO or TOP, depending on the direction settings.
Timer	The timer/counter clock control is handled by an internal source.
Counter	The clock control is handled externally (e.g., counting external events).
CC	For compare operations, the CC are referred to as “compare channels.” For capture operations, the CC are referred to as “capture channels.”

Each TC instance has up to two compare/capture channels (CC0 and CC1).

The counter in the TC can either count events from the Event System or clock ticks of the GCLK_TCx clock, which may be divided by the prescaler.

The counter value is passed to the CCx where it can be either compared to user-defined values or captured.

For optimized timing, the CCx and CCBUFx registers share a common resource. When writing into CCBUFx, lock the access to the corresponding CCx register (SYNCBUSY.CCX = 1) until the CCBUFx register value is not loaded into the CCx register (BUFVx == 1). Each buffer register has a buffer valid (BUFV) flag that indicates when the buffer contains a new value.

The Counter register (COUNT) and the Compare and Capture registers with buffers (CCx and CCBUFx) can be configured as 8-, 16- or 32-bit registers, with corresponding MAX values. Mode settings (CTRLA.MODE) determine the maximum range of the Counter register.

In 8-bit mode, a Period Value (PER) register and its Period Buffer Value (PERBUF) register are also available. The counter range and the operating frequency determine the maximum time resolution achievable with the TC peripheral.

The TC can be set to count up or down. Under normal operation, the counter value is continuously compared to the TOP or ZERO value to determine whether the counter has reached that value. On a comparison match, the TC can request DMA transactions, or generate interrupts or events for the Event System.

In a compare operation, the counter value is continuously compared to the values in the CCx registers. In the case of a match, the TC can request DMA transactions, or generate interrupts or events for the Event System. In waveform generator mode, these comparisons are used to set the waveform period or pulse width.

Capture operation can be enabled to perform input signal period and pulse width measurements, or to capture selectable edges from an IO pin or internal event from Event System.

Related Links

Waveform Output Operations

40.6.2 Basic Operation

40.6.2.1 Initialization

The following registers are enable-protected, meaning that they can only be written when the TC is disabled (CTRLA.ENABLE=0):

- Control A register (CTRLA), except the Enable (ENABLE) and Software Reset (SWRST) bits
- Drive Control register (DRVCTRL)
- Wave register (WAVE)
- Event Control register (EVCTRL)

Writing to enable-protected bits and setting the CTRLA.ENABLE bit can be performed in a single 32-bit access of the CTRLA register. Writing to enable-protected bits and clearing the CTRLA.ENABLE bit cannot be performed in a single 32-bit access.

Before enabling the TC, the peripheral must be configured by the following steps:

1. Enable the TC bus clock if not already enabled by default (PB1_CLK).
2. Select 8-, 16- or 32-bit counter mode via the TC Mode bit group in the Control A register (CTRLA.MODE). The default mode is 16-bit.
3. Select one wave generation operation in the Waveform Generation Operation bit group in the WAVE register (WAVE.WAVEGEN).
4. If desired, the GCLK_TCx clock can be prescaled via the Prescaler bit group in the Control A register (CTRLA.PRESCALER).
   – If the prescaler is used, select a prescaler synchronization operation via the Prescaler and Counter Synchronization bit group in the Control A register (CTRLA.PRESYNC).
5. If desired, select one-shot operation by writing a ‘1’ to the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT).
6. If desired, configure the counting direction ‘down’ (starting from the TOP value) by writing a ‘1’ to the Counter Direction bit in the Control B register (CTRLBSET.DIR).
7. For capture operation, enable the individual channels to capture in the Capture Channel x Enable bit group in the Control A register (CTRLA.CAPTEN).

8. If desired, enable inversion of the waveform output or IO pin input signal for individual channels via the Invert Enable bit group in the Drive Control register (DRVCTRL.INVEN).

40.6.2.2 Enabling, Disabling, and Resetting

The TC is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The TC is disabled by writing a zero to CTRLA.ENABLE.

The TC is reset by writing a '1' to the Software Reset bit in the Control A register (CTRLA.SWRST). All registers in the TC, except DBGCTRL, will be reset to their initial state. See *CTRLA* from Related Links.

The TC must be disabled before the TC is reset in order to avoid undefined behavior.

Related Links

CTRLA

Control A

40.6.2.3 Prescaler Selection

The GCLK_TCx is fed into the internal prescaler.

The prescaler consists of a counter that counts up to the selected prescaler value, whereupon the output of the prescaler toggles.

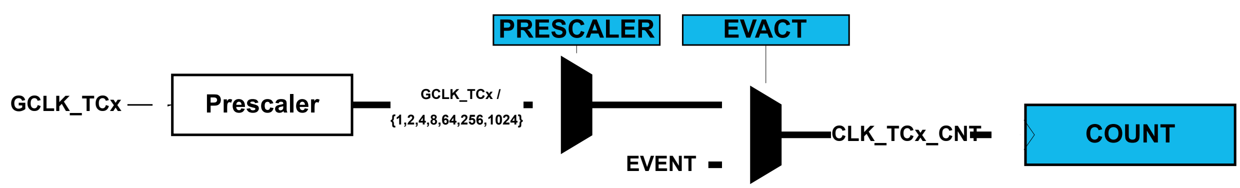
If the prescaler value is higher than one, the Counter Update condition can be optionally executed on the next GCLK_TCx clock pulse or the next prescaled clock pulse. For further details, refer to Prescaler (CTRLA.PRESCALER) and Counter Synchronization (CTRLA.PRESYNC) description.

Prescaler outputs from 1 to 1/1024 are available. For a complete list of available prescaler outputs, see the register description for the Prescaler bit group in the Control A register (CTRLA.PRESCALER).

Note: When counting events, the prescaler is bypassed.

The joint stream of prescaler ticks and event action ticks is called CLK_TCx_CNT.

Figure 40-2. Prescaler



40.6.2.4 Counter Mode

The counter mode is selected by the Mode bit group in the Control A register (CTRLA.MODE).
By default, the counter is enabled in the 16-bit counter resolution. Three counter resolutions are available:

- COUNT8: The 8-bit TC has its own Period Value and Period Buffer Value registers (PER and PERBUF).
- COUNT16: 16-bit is the default counter mode. There is no dedicated period register in this mode.
- COUNT32: 32-bit mode is achieved by pairing two 16-bit TC peripherals. TC(2n) is paired with TC(n+1).
  When paired, the TC peripherals are configured using the registers of the even-numbered TC (TC0 or TC2, respectively).
  The TC bus clocks (PB1_CLK) for both host and client TCs need to be enabled.
  The odd-numbered partner (TC1 or TC3, respectively) will act as a client, and the Client bit in the Status register (STATUS.SLAVE) will be set. The register values of a client will not reflect the registers of the 32-bit counter. Writing to any of the client registers will not affect the 32-bit counter. Normal access to the client COUNT and CCx registers is not allowed.

40.6.2.5 Counter Operations

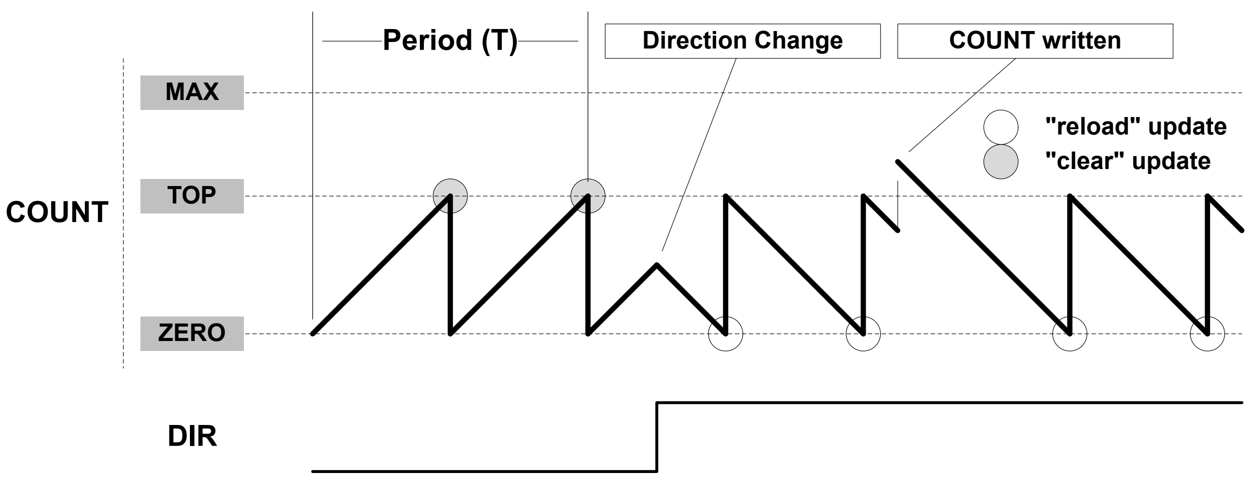
Depending on the mode of operation, the counter is cleared, reloaded, incremented, or decremented at each TC clock input (CLK_TCx_CNT). A counter clear or reload marks the end of the current counter cycle and the start of a new one.

The counting direction is set by the Direction bit in the Control B register (CTRLB.DIR). If this bit is zero the counter is counting up, and counting down if CTRLB.DIR=1. The counter will count up or down for each tick (clock or event) until it reaches TOP or ZERO. When it is counting up and TOP is reached, the counter will be set to zero at the next tick (overflow) and the Overflow Interrupt Flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF) will be set. When it is counting down, the counter is reloaded with the TOP value when ZERO is reached (underflow), and INTFLAG.OVF is set.

INTFLAG.OVF can be used to trigger an interrupt, a DMA request, or an event. An overflow/underflow occurrence (i.e., a compare match with TOP/ZERO) will stop counting if the One-Shot bit in the Control B register is set (CTRLBSET.ONESHOT).

It is possible to change the counter value (by writing directly in the COUNT register) even when the counter is running. When starting the TC, the COUNT value will be either ZERO or TOP (depending on the counting direction set by CTRLBSET.DIR or CTRLBCLR.DIR), unless a different value has been written to it, or the TC has been stopped at a value other than ZERO. The write access has higher priority than count, clear, or reload. The direction of the counter can also be changed when the counter is running. See also the following figure.

Figure 40-3. Counter Operation



Due to asynchronous clock domains, the internal counter settings are written when the synchronization is complete. Normal operation must be used when using the counter as timer base for the capture channels.

40.6.2.5.1 Stop Command and Event Action

A Stop command can be issued from software by using Command bits in the Control B Set register (CTRLBSET.CMD = 0x2, STOP). When a Stop is detected while the counter is running, the counter will not retain its current value. All waveforms are cleared and the Stop bit in the Status register is set (STATUS.STOP).

40.6.2.5.2 Re-Trigger Command and Event Action

A re-trigger command can be issued from software by writing the Command bits in the Control B Set register (CTRLBSET.CMD = 0x1, RETRIGGER), or from event when a re-trigger event action is configured in the Event Control register (EVCTRL.EVACT = 0x1, RETRIGGER).

When the command is detected during counting operation, the counter will be reloaded or cleared, depending on the counting direction (CTRLBSET.DIR or CTRLBCLR.DIR). When the re-trigger command is detected while the counter is stopped, the counter will resume counting from the current value in the COUNT register.

Note: When a re-trigger event action is configured in the Event Action bits in the Event Control register (EVCTRL.EVACT=0x1, RETRIGGER), enabling the counter will not start the counter. The counter will start on the next incoming event and restart on corresponding following event.

40.6.2.5.3 Count Event Action

The TC can count events. When an event is received, the counter increases or decreases the value, depending on direction settings (CTRLBSET.DIR or CTRLBCLR.DIR). The count event action can be selected by the Event Action bit group in the Event Control register (EVCTRL.EVACT=0x2, COUNT).

Note: If this operation mode is selected, PWM generation is not supported.

40.6.2.5.4 Start Event Action

The TC can start counting operation on an event when previously stopped. In this configuration, the event has no effect if the counter is already counting. When the peripheral is enabled, the counter operation starts when the event is received or when a re-trigger software command is applied.

The Start TC on Event action can be selected by the Event Action bit group in the Event Control register (EVCTRL.EVACT=0x3, START).

40.6.2.6 Compare Operations

By default, the Compare/Capture channel is configured for compare operations.

When using the TC and the Compare/Capture Value registers (CCx) for compare operations, the counter value is continuously compared to the values in the CCx registers. This can be used for timer or for waveform operation.

The Channel x Compare Buffer (CCBUFx) registers provide double buffer capability. The double buffering synchronizes the update of the CCx register with the buffer value at the UPDATE condition or a forced update command (CTRLBSET.CMD=UPDATE). See *Double Buffering* from Related Links. The synchronization prevents the occurrence of odd-length, non-symmetrical pulses and ensures glitch-free output.

Related Links
Double Buffering

40.6.2.6.1 Waveform Output Operations

The compare channels can be used for waveform generation on output port pins. To make the waveform available on the connected pin, the following requirements must be fulfilled:

1. Choose a Waveform Generation mode in the Waveform Generation Operation bit in Waveform register (WAVE.WAVEGEN).
2. Optionally invert the waveform output WO[x] by writing the corresponding Output Waveform x Invert Enable bit in the Driver Control register (DRVCTRL.INVENx).
3. Configure the pins with the I/O Peripheral Pin Select (PPS). See *I/O Ports and Peripheral Pin Select (PPS)* from Related Links.
   Note: Event must not be used when the compare channel is set in waveform output operating mode.

The counter value is continuously compared with each CCx value. On a comparison match, the Match or Capture Channel x bit in the Interrupt Flag Status and Clear register (INTFLAG.MCx) will be set on the next zero-to-one transition of CLK_TC_CNT (see Normal Frequency Operation). An interrupt/and or event can be generated on comparison match if enabled. The same condition generates a DMA request.

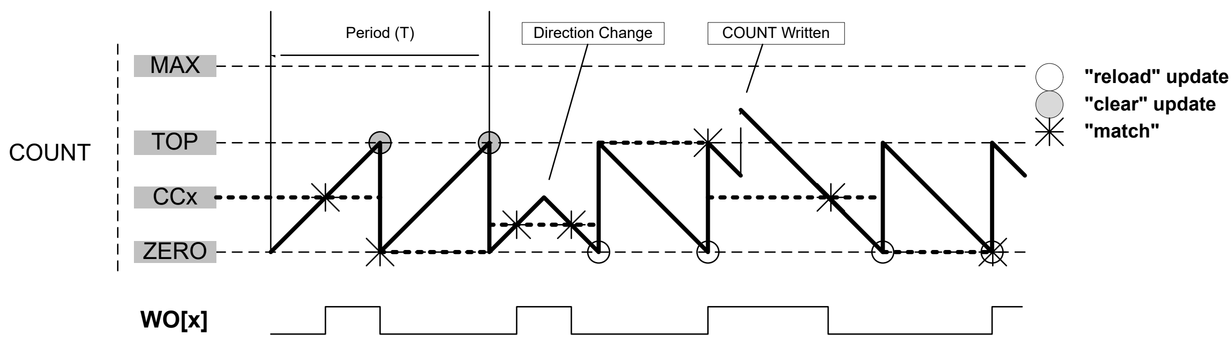
There are four waveform configurations for the Waveform Generation Operation bit group in the Waveform register (WAVE.WAVEGEN). This will influence how the waveform is generated and impose restrictions on the top value. The configurations are:

- Normal frequency (NFRQ)
- Match frequency (MFRQ)
- Normal pulse-width modulation (NPWM)
- Match pulse-width modulation (MPWM)

When using NPWM or NFRQ configuration, the TOP will be determined by the counter resolution. In 8-bit Counter mode, the Period register (PER) is used as TOP, and the TOP can be changed by writing to the PER register. In 16- and 32-bit Counter mode, TOP is fixed to the maximum (MAX) value of the counter.

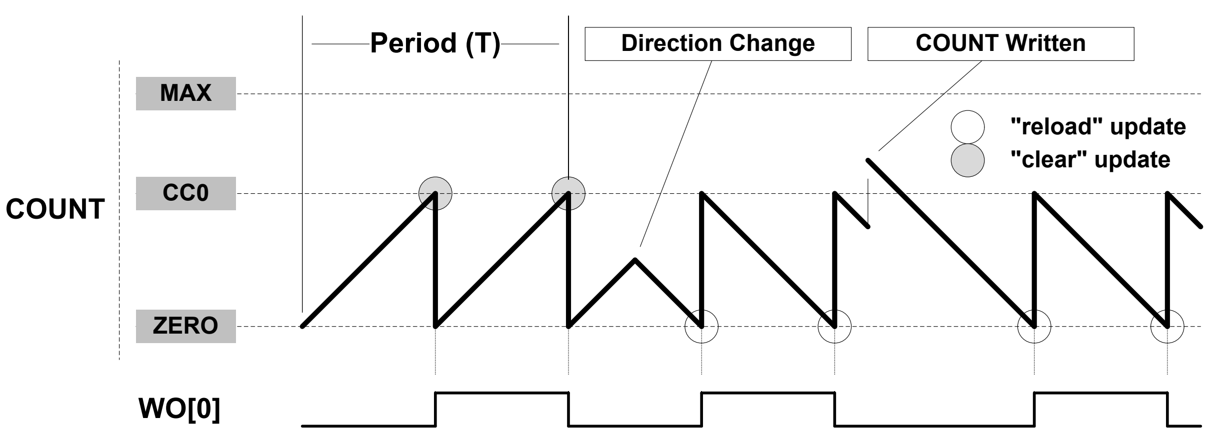
Normal Frequency Generation (NFRQ)
For Normal Frequency Generation, the period time (T) is controlled by the period register (PER) for 8-bit Counter mode and MAX for 16- and 32-bit mode. The waveform generation output (WO[x]) is toggled on each compare match between COUNT and CCx, and the corresponding Match or Capture Channel x Interrupt Flag (INTFLAG.MCx) will be set.

Figure 40-4. Normal Frequency Operation



Match Frequency Generation (MFRQ)
For Match Frequency Generation, the period time (T) is controlled by the CC0 register instead of PER or MAX. WO[0] toggles on each Update condition.

Figure 40-5. Match Frequency Operation



Normal Pulse-Width Modulation Operation (NPWM)
NPWM uses single-slope PWM generation.

For single-slope PWM generation, the period time (T) is controlled by the TOP value, and CCx controls the duty cycle of the generated waveform output. When up-counting, the WO[x] is set at start or compare match between the COUNT and TOP values, and cleared on compare match between COUNT and CCx register values. When down-counting, the WO[x] is cleared at start or compare match between the COUNT and ZERO values, and set on compare match between COUNT and CCx register values.

The following equation calculates the exact resolution for a single-slope PWM (R_{PWM_SS}) waveform:

$$R_{\mathrm{PWM\_SS}} = \frac{\log(\mathrm{TOP}+1)}{\log(2)}$$

The PWM frequency (f_{PWM_SS}) depends on TOP value and the peripheral clock frequency (f_{GCLK_TC}), and can be calculated by the following equation:

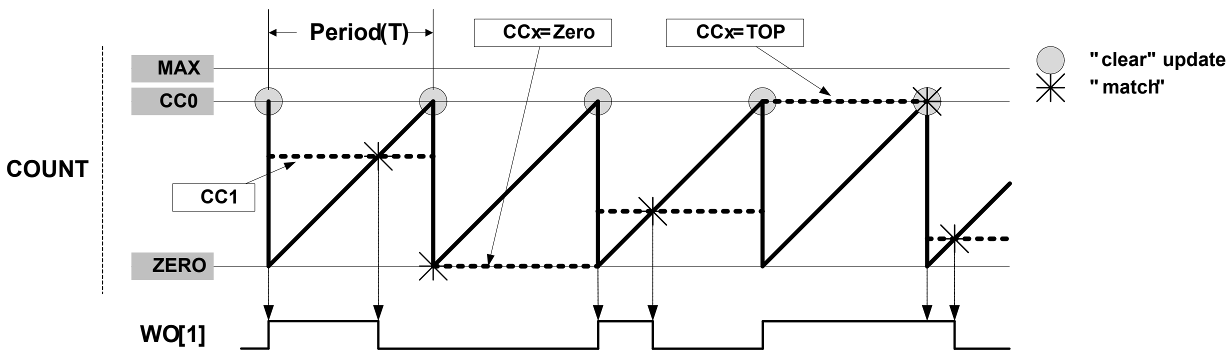
$$f_{\mathrm{PWM\_SS}} = \frac{f_{\mathrm{GCLK\_TC}}}{\mathrm{N}(\mathrm{TOP}+1)}$$

Where N represents the prescaler divider used (1, 2, 4, 8, 16, 64, 256, 1024).

Match Pulse-Width Modulation Operation (MPWM)

In MPWM, the output of WO[1] is depending on CC1 as shown in the figure below. On every overflow/underflow, a one-TC-clock-cycle negative pulse is put out on WO[0] (not shown in the figure).

Figure 40-6. Match PWM Operation



The following table shows the Update Counter and Overflow Event/Interrupt Generation conditions in different operation modes.

Table 40-3. Counter Update and Overflow Event/interrupt Conditions in TC

Name	Operation	TOP	Update	Output Waveform		OVFIF/Event	
				On Match	On Update	Up	Down
NFRQ	Normal Frequency	PER	TOP/ ZERO	Toggle	Stable	TOP	ZERO
MFRQ	Match Frequency	CC0	TOP/ ZERO	Toggle	Stable	TOP	ZERO
NPWM	Single-slope PWM	PER	TOP/ ZERO	See description above.		TOP	ZERO
MPWM	Single-slope PWM	CC0	TOP/ ZERO	Toggle	Toggle	TOP	ZERO

Related Links

I/O Ports and Peripheral Pin Select (PPS)

40.6.2.7 Double Buffering

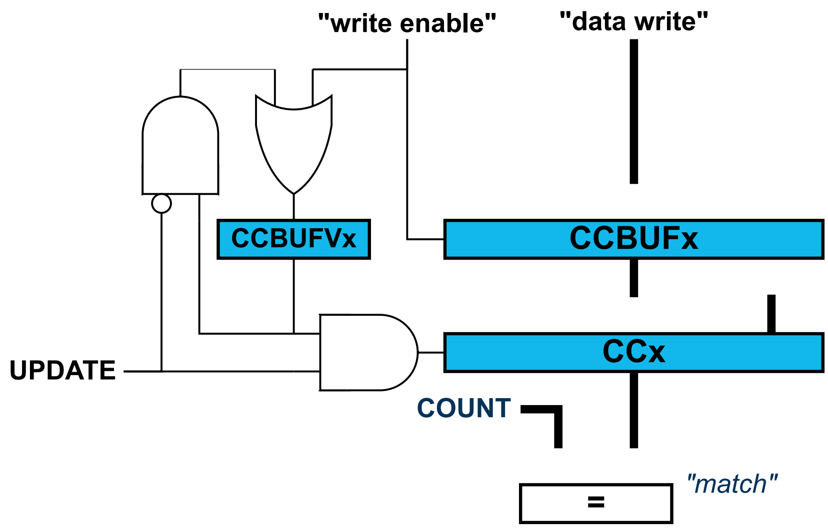
The Compare Channels (CCx) registers, and the Period (PER) register in 8-bit mode are double buffered. Each buffer register has a buffer valid bit (CCBUFVx or PERBUFV) in the STATUS register, which indicates that the buffer register contains a new valid value that can be copied into the corresponding register. As long as the respective buffer valid status flag (PERBUFV or CCBUFVx) are set to '1', related syncbusy bits are set (SYNCBUSY.PER or SYNCBUSY.CCx), a write to the respective

PER/PERBUF or CCx/CCBUFx registers will generate a PAC error, and access to the respective PER or CCx register is invalid.

When the buffer valid flag bit in the STATUS register is '1' and the Lock Update bit in the CTRLB register is set to '0', (writing CTRLBCLR.LUPD to '1'), double buffering is enabled: the data from buffer registers will be copied into the corresponding register under hardware UPDATE conditions, then the buffer valid flags bit in the STATUS register are automatically cleared by hardware.
Note: The software update command (CTRLBSET.CMD=0x3) is acting independently of the LUPD value.

A compare register is double buffered as in the following figure.

Figure 40-7. Compare Channel Double Buffering



Both the registers (PER/CCx) and corresponding buffer registers (PERBUF/CCBUFx) are available in the I/O register map, and the double buffering feature is not mandatory. The double buffering is disabled by writing a '1' to CTRLBSET.LUPD.

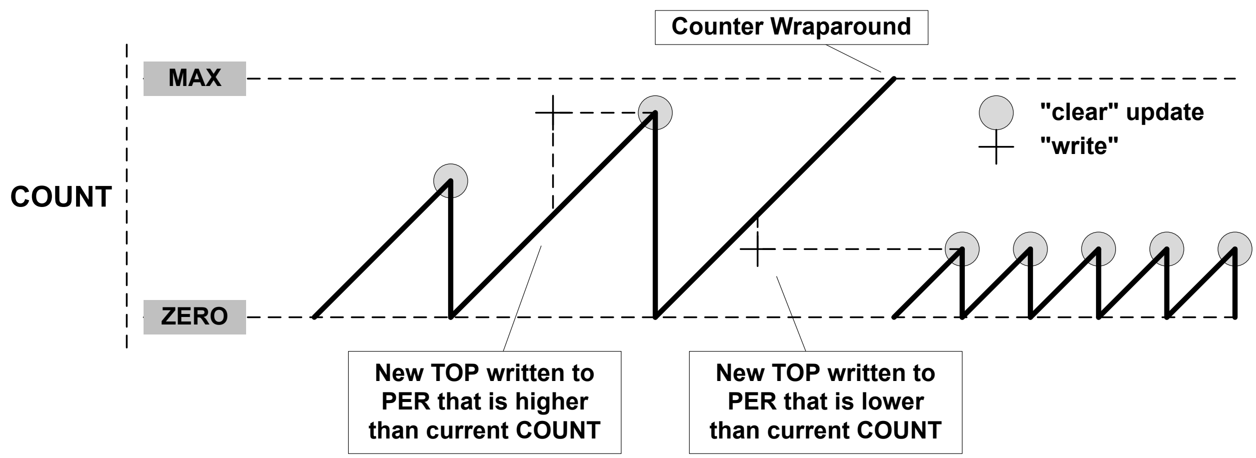
Note: In NFRQ, MFRQ or PWM, down-counting counter mode (CTRLBSET.DIR=1), when double buffering is enabled (CTRLBCLR.LUPD=1), PERBUF register is continuously copied into the PER independently of update conditions.

Changing the Period

The counter period can be changed by writing a new TOP value to the Period register (PER or CC0, depending on the waveform generation mode), which is available in 8-bit mode. Any period update on registers (PER or CCx) is effective after the synchronization delay.

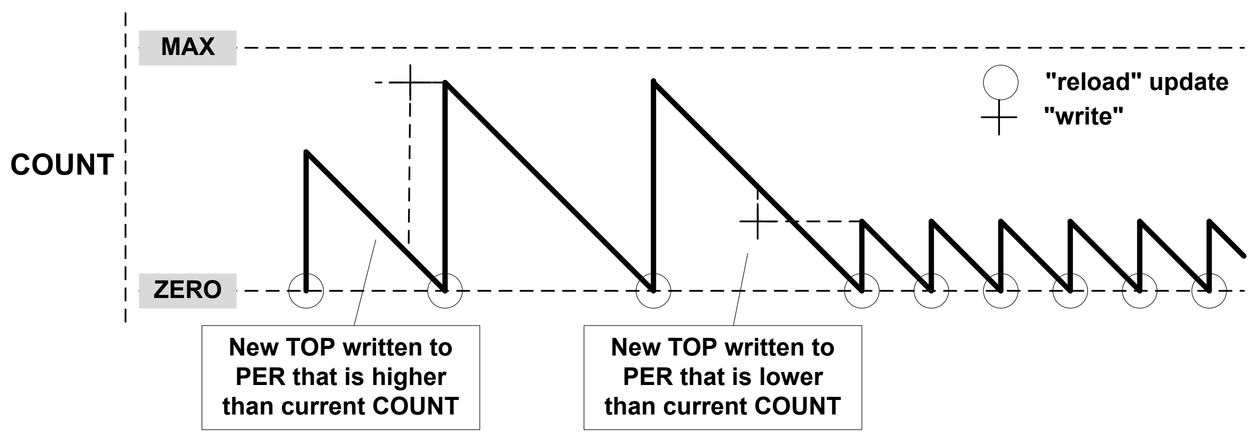
A counter wraparound can occur in any operation mode when up-counting without buffering (see the following figure).

Figure 40-8. Unbuffered Single-Slope Up-Counting Operation



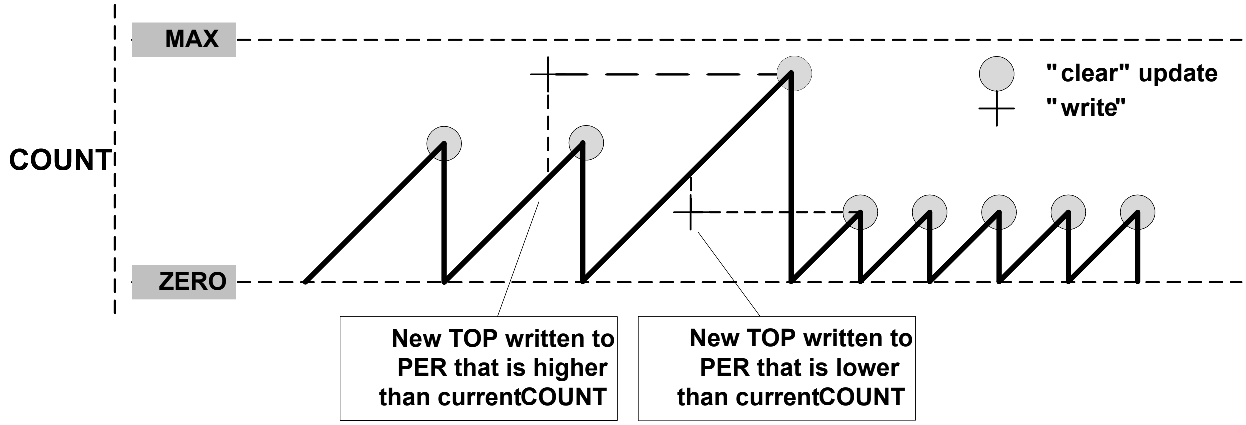
COUNT and TOP are continuously compared, so when a new TOP value that is lower than current COUNT is written to TOP, COUNT will wrap before a compare match.

Figure 40-9. Unbuffered Single-Slope Down-Counting Operation



When double buffering is used, the buffer can be written at any time and the counter will still maintain correct operation. The period register is always updated on the update condition, as shown in the following figure. This prevents wraparound and the generation of odd waveforms.

Figure 40-10. Changing the Period Using Buffering



40.6.2.8 Capture Operations

To enable and use capture operations, the corresponding Capture Channel x Enable bit in the Control A register (CTRLA.CAPTENx) must be written to '1'.

A capture trigger can be provided by input event line TC_EV or by asynchronous IO pin WO[x] for each capture channel or by a TC event. To enable the capture from input event line, Event Input Enable bit in the Event Control register (EVCTRL.TCEI) must be written to '1'. To enable the capture from the IO pin, the Capture On Pin x Enable bit in CTRLA register (CTRLA.COPENx) must be written to '1'.

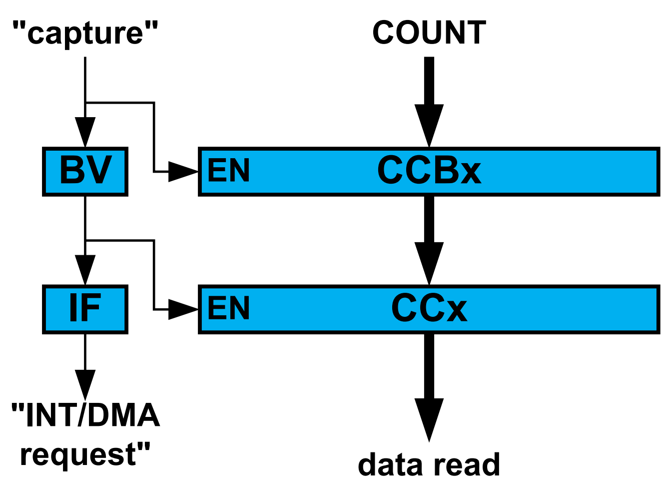
Notes:

1. The RETRIGGER, COUNT and START event actions are available only on an event from the Event System.
2. Event system channels must be configured to operate in asynchronous mode of operation when used for capture operations.

By default, a capture operation is done when a rising edge is detected on the input signal. Capture on falling edge is available, its activation is depending on the input source:

- When the channel is used with a IO pin, write a '1' to the corresponding Invert Enable bit in the Drive Control register (DRVCTRL.INVENx).
- When the channel is counting events from the Event System, write a '1' to the TC Event Input Invert Enable bit in Event Control register (EVCTRL.TCINV).

Figure 40-11. Capture Double Buffering



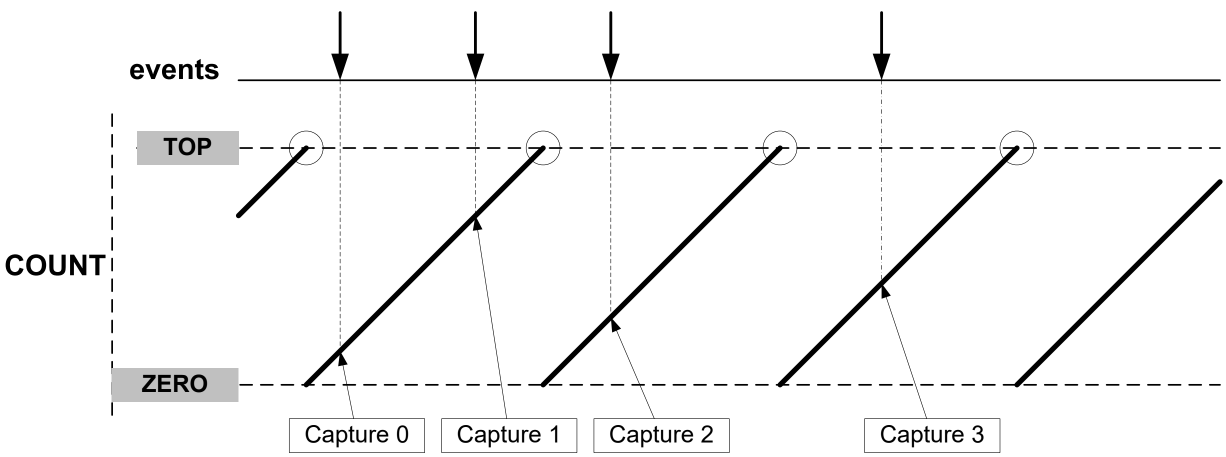
For input capture, the buffer register and the corresponding CCx act like a FIFO. When CCx is empty or read, any content in CCBUFx is transferred to CCx. The buffer valid flag is passed to set the CCx interrupt flag (IF) and generate the optional interrupt, event or DMA request. The CCBUFx register value can't be read, all captured data must be read from CCx register.

Note:
When up-counting (CTRLBSET.DIR=0), counter values lower than 1 cannot be captured. To capture the full range including value 0, the TC must be in down-counting mode (CTRLBSET.DIR=0).

40.6.2.8.1 Event Capture Action

The compare/capture channels can be used as input capture channels to capture events from the Event System and give them a timestamp. The following figure shows four capture events for one capture channel.

Figure 40-12. Input Capture Timing



The TC can detect capture overflow of the input capture channels. When a new capture event is detected while the Capture Interrupt flag (INTFLAG.MCx) is still set, the new timestamp will not be stored and INTFLAG.ERR will be set. The user needs to clear INTFLAG.MCx at the beginning of the interrupt routine and poll the bit until INTFLAG.MCx is cleared before exiting the ISR.

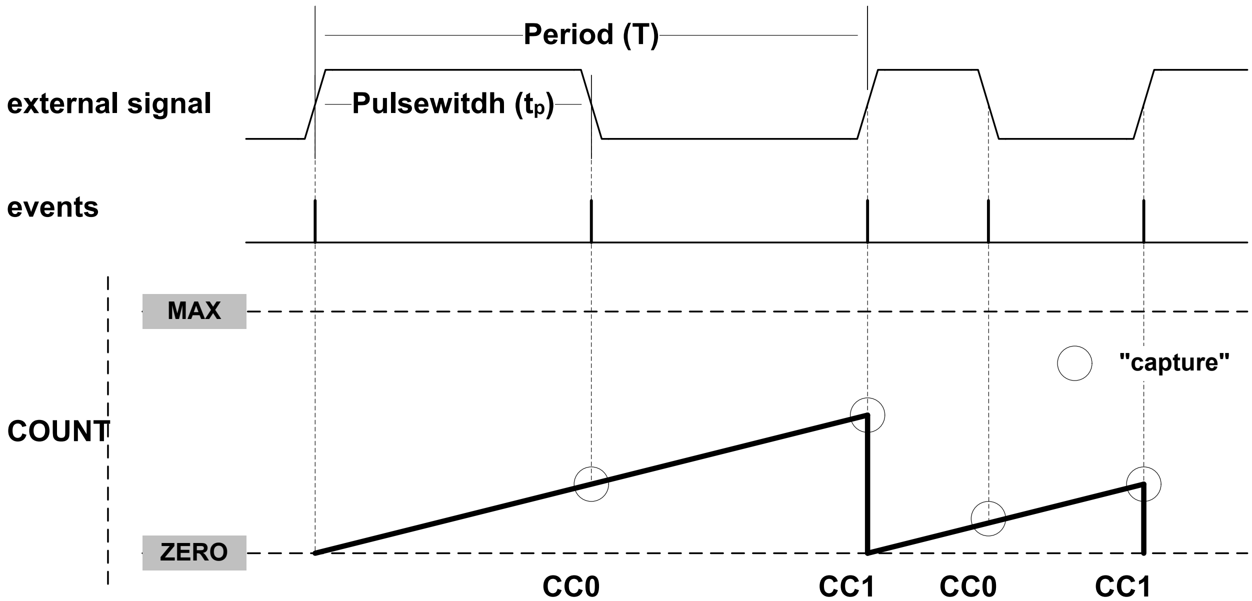
40.6.2.8.2 Period and Pulse-Width (PPW) Capture Action

The TC can perform two input captures and restart the counter on one of the edges. This enables the TC to measure the pulse width and period and to characterize the frequency, *f*, and duty cycle of an input signal:

$$f = \frac{1}{T}$$

$$\text{dutyCycle} = \frac{t_p}{T}$$

Figure 40-13. PWP Capture



Selecting PWP in the Event Action bit group in the Event Control register (EVCTRL.EVACT) enables the TC to perform one capture action on the rising edge and the other one on the falling edge. The period, *T*, will be captured into CC1 and the pulse width, t_p, in CC0. EVCTRL.EVACT=PPW (Period and Pulse-Width) offers identical functionality, but will capture *T* into CC0 and t_p into CC1.

The TC Event Input Invert Enable bit in the Event Control register (EVCTRL.TCINV) is used to select whether the wraparound must occur on the rising edge or the falling edge. If EVCTRL.TCINV=`1`, the wraparound will happen on the falling edge. If the pin capture is enabled, this can also be achieved by modifying the value of the DRVCTRL.INVENx bit.

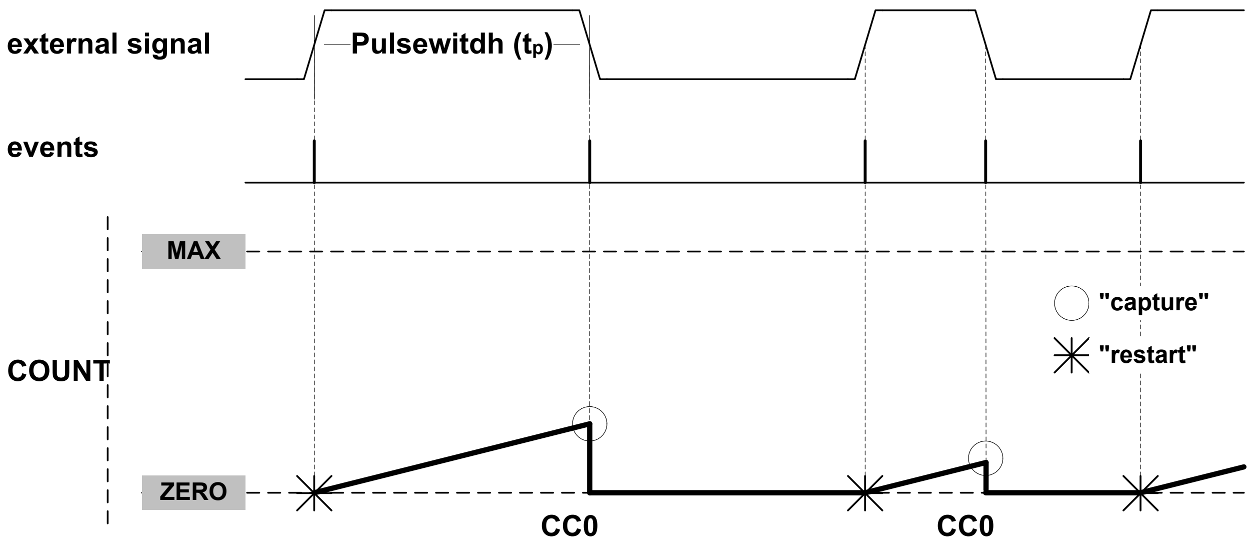
The TC can detect capture overflow of the input capture channels: When a new capture event is detected while the Capture Interrupt flag (INTFLAG.MCx) is still set, the new timestamp will not be stored and INTFLAG.ERR will be set. The user needs to clear INTFLAG.MCx at the beginning of the interrupt routine and poll the bit until INTFLAG.MCx is cleared before exiting the ISR.

Note: The corresponding capture is working only if the channel is enabled in capture mode (CTRLA.CAPTENx=`1`). If not, the capture action is ignored and the channel is enabled in the Compare mode of the operation. Consequently, both channels must be enabled to fully characterize the input.

40.6.2.8.3 Pulse-Width Capture Action

The TC performs the input capture on the falling edge of the input signal. When the edge is detected, the counter value is cleared and the TC stops counting. When a rising edge is detected on the input signal, the counter restarts the counting operation. To enable the operation on opposite edges, the input signal to capture must be inverted (refer to DRVCTRL.INVEN or EVCTRL.TCEINV).

Figure 40-14. Pulse-Width Capture on Channel 0



The TC can detect capture overflow of the input capture channels: When a new capture event is detected while the Capture Interrupt flag (INTFLAG.MCx) is still set, the new timestamp will not be stored and INTFLAG.ERR will be set. The user needs to clear INTFLAG.MCx at the beginning of the interrupt routine and poll the bit until INTFLAG.MCx is cleared before exiting the ISR.

40.6.3 Additional Features

40.6.3.1 One-Shot Operation

When one-shot is enabled, the counter automatically stops on the next Counter Overflow or Underflow condition. When the counter is stopped, the Stop bit in the Status register (STATUS.STOP) is automatically set and the waveform outputs are set to zero.

One-shot operation is enabled by writing a '1' to the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT), and disabled by writing a '1' to CTRLBCLR.ONESHOT. When enabled, the TC will count until an overflow or underflow occurs and stops counting operation. The one-shot operation can be restarted by a re-trigger software command, a re-trigger event, or a start event. When the counter restarts its operation, STATUS.STOP is automatically cleared.

40.6.3.2 Timestamp Capture

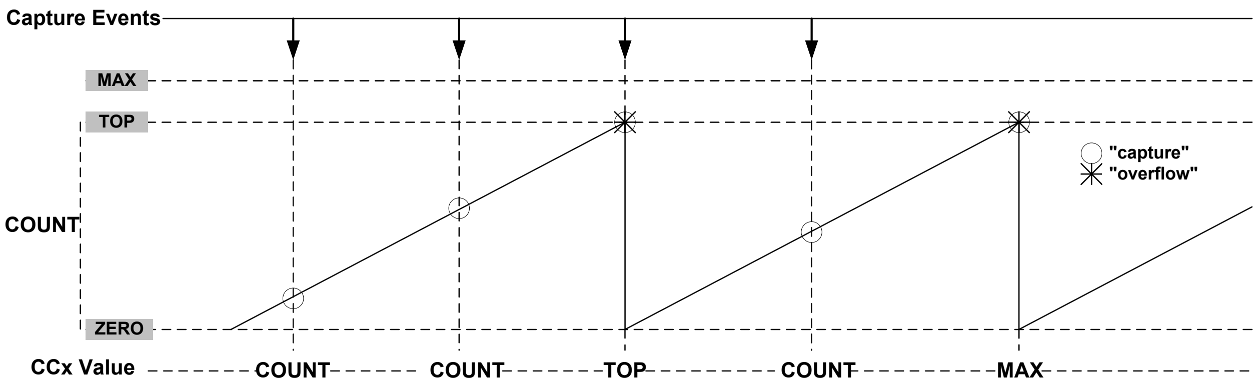
This feature is enabled when the Capture Time Stamp (STAMP) Event Action in Event Control register (EVCTRL.EVACT) is selected. The counter TOP value must be smaller than MAX.

When a capture event is detected, the COUNT value is copied into the corresponding Channel x Compare/Capture Value (CCx) register. If there is an overflow, the MAX value is copied into the corresponding CCx register.

When a valid captured value is present in the capture channel register, the corresponding Capture Channel x Interrupt Flag (INTFLAG.MCx) is set.

The timer/counter can detect capture overflow of the input capture channels. When a new capture event is detected while the Capture Channel interrupt flag (INTFLAG.MCx) is still set, the new timestamp will not be stored and INTFLAG.ERR will be set. The user needs to clear INTFLAG.MCx at the beginning of the interrupt routine and poll the bit until INTFLAG.MCx is cleared before exiting the ISR.

Figure 40-15. Time-Stamp



40.6.3.3 Minimum Capture

The minimum capture is enabled by writing the CAPTMIN mode in the Channel n Capture Mode bits in the Control A register (CTRLA.CAPTMODEn = CAPTMIN).

CCx Content:

In CAPTMIN operations, CCx keeps the Minimum captured values. Before enabling this mode of capture, the user must initialize the corresponding CCx register value to a value different from zero. If the CCx register initial value is zero, no captures will be performed using the corresponding channel.

MCx Behaviour:

In CAPTMIN operation, capture is performed only when on capture event time. The counter value is lower than the last captured value. The MCx interrupt flag is set only when on capture event time. The counter value is higher or equal to the value captured on the previous event. Therefore, the interrupt flag is set when a new absolute local Minimum value is detected.

40.6.3.4 Maximum Capture

The maximum capture is enabled by writing the CAPTMAX mode in the Channel n Capture Mode bits in the Control A register (CTRLA.CAPTMODEn = CAPTMAX).

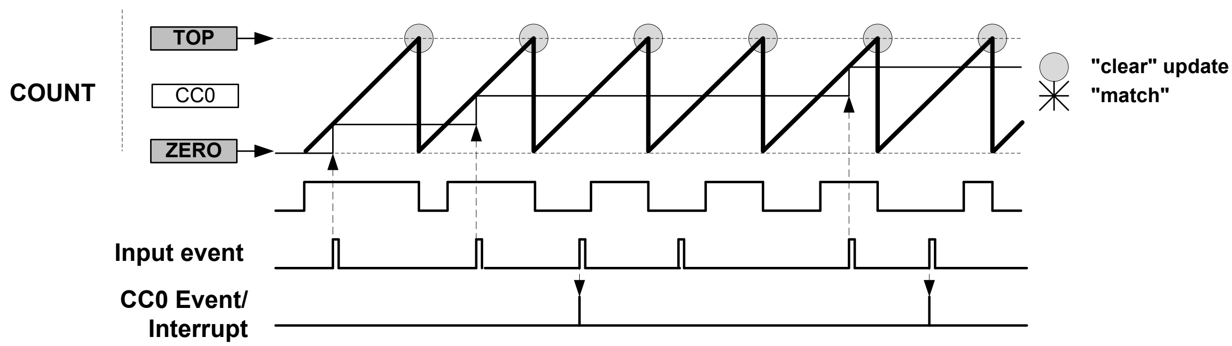
CCx Content:

In CAPTMAX operations, CCx keeps the Maximum captured values. Before enabling this mode of capture, the user must initialize the corresponding CCx register value to a value different from TOP. If the CCx register initial value is TOP, no captures will be performed using the corresponding channel.

MCx Behaviour:

In CAPTMAX operation, capture is performed only when on capture event time. The counter value is higher than the last captured value. The MCx interrupt flag is set only when on capture event time. The counter value is lower or equal to the value captured on the previous event. Therefore, the interrupt flag is set when a new absolute local Maximum value is detected.

Figure 40-16. Maximum Capture Operation with CC0 Initialized with ZERO Value



40.6.4 DMA Operation

The TC can generate the following DMA requests:

- Overflow (OVF): the request is set when an update condition (overflow, underflow or re-trigger) is detected, the request is cleared by hardware on DMA acknowledge.
- Match or Capture Channel x (MCx): for a compare channel, the request is set on each compare match detection, the request is cleared by hardware on DMA acknowledge. For a capture channel, the request is set when valid data is present in the CCx register, and cleared when CCx register is read.

40.6.5 Interrupts

The TC has the following interrupt sources:

- Overflow/Underflow (OVF)
- Match or Capture Channel x (MCx)
- Capture Overflow Error (ERR)

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear register (INTFLAG) is set when the interrupt condition occurs.

Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set register (INTENSET), and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear register (INTENCLR). The status of enabled interrupts can be read from either INTENSET or INTENCLR.

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until either the interrupt flag is cleared, the interrupt is disabled, or the TC is reset. See *INTFLAG* from Related Links for more details on how to clear the interrupt flags.

The TC has one common interrupt request line for all the interrupt sources. The user must read the INTFLAG register to determine which interrupt condition is present.

Note that interrupts must be globally enabled for interrupt requests to be generated. See *Nested Vector Interrupt Controller (NVIC)* from Related Links.

Related Links

Nested Vector Interrupt Controller (NVIC)
INTFLAG
Interrupt Flag Status and Clear

40.6.6 Events

The TC can generate the following output events:

- Overflow/Underflow (OVF)
- Match or Capture Channel x (MCX0-1)

Writing a '1' to an Event Output bit in the Event Control register (EVCTRL.MCEOx) enables the corresponding output event. The output event is disabled by writing EVCTRL.MCEOx=0.

One of the following event actions can be selected by the Event Action bit group in the Event Control register (EVCTRL.EVACT):

- Disable event action (OFF)
- Start TC (START)
- Re-trigger TC (RETRIGGER)
- Count on event (COUNT)
- Capture time stamp (STAMP)
- Capture Period (PPW and PWP)
- Capture Pulse Width (PW)

Writing a '1' to the TC Event Input bit in the Event Control register (EVCTRL.TCEI) enables input events (EVU0-2) to the TC. Writing a '0' to this bit disables input events to the TC. The TC requires only asynchronous event inputs. See *Event System (EVSYS)* from Related Links for additional information on configuring the asynchronous events.

Related Links

Event System (EVSYS)

40.6.7 Sleep Mode Operation

The TC can be configured to operate in any sleep mode. To be able to run in standby, the RUNSTDBY bit in the Control A register (CTRLA.RUNSTDBY) must be '1'. This peripheral can wake up the device from any sleep mode using interrupts or perform actions through the Event System.

If the On Demand bit in the Control A register (CTRLA.ONDEMAND) is written to '1', the module stops requesting its peripheral clock when the STOP bit in STATUS register (STATUS.STOP) is set to '1'. When a re-trigger or start condition is detected, the TC requests the clock before the operation starts.

40.6.8 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset and Enable bits in Control A register (CTRLA.SWRST and CTRLA.ENABLE)
- Capture Channel Buffer Valid bit in STATUS register (STATUS.CCBUFVx)

The following registers are synchronized when written:

- Control B Clear and Control B Set registers (CTRLBCLR and CTRLBSET)
- Count Value register (COUNT)
- Period Value and Period Buffer Value registers (PER and PERBUF)
- Channel x Compare/Capture Value and Channel x Compare/Capture Buffer Value registers (CCx and CCBUFx)

The following registers are synchronized when read:

- Count Value register (COUNT): synchronization is done on demand through READSYNC command (CTRLBSET.CMD)

- Control B Clear and Control B Set registers (CTRLBCLR and CTRLBSET)
- Channel x Compare/Capture Value (CCx)

Required write synchronization is denoted by the "Write-Synchronized" property in the register description.

Required read synchronization is denoted by the "Read-Synchronized" property in the register description.

40.7 Register Description

Registers can be 8, 16 or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write protection is denoted by the “PAC Write-Protection” property in each individual register description.

Some registers are synchronized when read and/or written. Synchronization is denoted by the “Write-Synchronized” or the “Read-Synchronized” property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable protection is denoted by the “Enable-Protected” property in each individual register description.

Note: All registers in this table have corresponding CLR, SET and INV registers at its virtual address, plus an offset of 0x4, 0x8 and 0xC, respectively. See *CLR, SET, and INV Registers* from Related Links.

Related Links

CLR, SET and INV Registers

40.7.1 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
		15:8	DMAOS				ALOCK	PRESCALER[2:0]		
		23:16			COPEN1	COPEN0			CAPTEN1	CAPTEN0
		31:24				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
0x04	CTRLBCLR	7:0	CMD[2:0]					ONESHOT	LUPD	DIR
0x05	CTRLBSET	7:0	CMD[2:0]					ONESHOT	LUPD	DIR
0x06	EVCTRL	7:0			TCEI	TCINV		EVACT[2:0]		
		15:8			MCEO1	MCEO0				OVFEO
0x08	INTENCLR	7:0			MC1	MC0			ERR	OVF
0x09	INTENSET	7:0			MC1	MC0			ERR	OVF
0x0A	INTFLAG	7:0			MC1	MC0			ERR	OVF
0x0B	STATUS	7:0			CCBUFV1	CCBUFV0	PERBUFV		SLAVE	STOP
0x0C	WAVE	7:0							WAVEGEN[1:0]	
0x0D	DRVCTRL	7:0							INVEN1	INVEN0
0x0E	Reserved									
0x0F	DBGCTRL	7:0								DBGRUN
0x10	SYNCBUSY	7:0	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
0x11 ... 0x13	Reserved									
0x14	COUNT	7:0	COUNT[7:0]							
0x15 ... 0x1A	Reserved									
0x1B	PER	7:0	PER[7:0]							
0x1C	CC0	7:0	CC[7:0]							
0x1D	CC1	7:0	CC[7:0]							
0x1E ... 0x2E	Reserved									
0x2F	PERBUF	7:0	PERBUF[7:0]							
0x30	CCBUF0	7:0	CCBUF[7:0]							
0x31	CCBUF1	7:0	CCBUF[7:0]							

40.7.2 Register Description - 8-bit Mode

40.7.2.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Enable-Protected

Bit	31	30	29	28	27	26	25	24
				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
Access				R/W	R/W		R/W	R/W
Reset				0	0		0	0

Bit	23	22	21	20	19	18	17	16
			COPEN1	COPEN0			CAPTEN1	CAPTEN0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	15	14	13	12	11	10	9	8
	DMAOS				ALOCK	PRESCALER[2:0]		
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
Reset	0	0	0	0	0	0	0	0

Bits 28:27 – CAPTMODE1[1:0] Capture mode Channel 1
These bits select the channel 1 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 25:24 – CAPTMODE0[1:0] Capture mode Channel 0
These bits select the channel 0 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 20, 21 – COPENx Capture On Pin x Enable [x=1..0]
Bit x of COPEN[1:0] selects the trigger source for capture operation, either events or I/O pin input. This bit is not synchronized.

Value	Description
0	Event from Event System is selected as trigger source for capture operation on channel x.
1	I/O pin is selected as trigger source for capture operation on channel x.

Bits 16, 17 – CAPTENx Capture Channel x Enable [x=1..0]
Bit x of CAPTEN[1:0] selects whether channel x is a capture or a compare channel.

These bits are not synchronized.

Value	Description
0	CAPTEN disables capture on channel x.
1	CAPTEN enables capture on channel x.

Bit 15 – DMAOS DMA One-Shot Trigger Mode

This bit enables the DMA One-shot Trigger Mode.
Writing a '1' to this bit will generate a DMA trigger on TC cycle following a TC_CTRLBSET_CMD_DMAOS command.
Writing a '0' to this bit will generate DMA triggers on each TC cycle.
This bit is not synchronized.

Bit 11 – ALOCK Auto Lock

When this bit is set, Lock bit update (LUPD) is set to '1' on each overflow/underflow or re-trigger event.
This bit is not synchronized.

Value	Description
0	The LUPD bit is not affected on overflow/underflow, and re-trigger event.
1	The LUPD bit is set on each overflow/underflow or re-trigger event.

Bits 10:8 – PRESCALER[2:0] Prescaler

These bits select the counter prescaler factor.
These bits are not synchronized.

Value	Name	Description
0x0	DIV1	Prescaler: GCLK_TC
0x1	DIV2	Prescaler: GCLK_TC/2
0x2	DIV4	Prescaler: GCLK_TC/4
0x3	DIV8	Prescaler: GCLK_TC/8
0x4	DIV16	Prescaler: GCLK_TC/16
0x5	DIV64	Prescaler: GCLK_TC/64
0x6	DIV256	Prescaler: GCLK_TC/256
0x7	DIV1024	Prescaler: GCLK_TC/1024

Bit 7 – ONDEMAND Clock On Demand

This bit selects the clock requirements when the TC is stopped.
In standby mode, if the Run in Standby bit (CTRLA.RUNSTDBY) is '0', ONDEMAND is forced to '0'.
This bit is not synchronized.

Value	Description
0	The On Demand is disabled. If On Demand is disabled, the TC will continue to request the clock when its operation is stopped (STATUS.STOP=1).
1	The On Demand is enabled. When On Demand is enabled, the stopped TC will not request the clock. The clock is requested when a software re-trigger command is applied or when an event with start/re-trigger action is detected.

Bit 6 – RUNSTDBY Run in Standby

This bit is used to keep the TC running in standby mode.
This bit is not synchronized.

Value	Description
0	The TC is halted in standby.
1	The TC continues to run in standby.

Bits 5:4 – PRESCSYNC[1:0] Prescaler and Counter Synchronization

These bits select whether the counter must wrap around on the next GCLK_TCx clock or the next prescaled GCLK_TCx clock. It also makes it possible to reset the prescaler.

These bits are not synchronized.

Value	Name	Description
0x0	GCLK	Reload or reset the counter on next generic clock
0x1	PRESC	Reload or reset the counter on next prescaler clock
0x2	RESYNC	Reload or reset the counter on next generic clock. Reset the prescaler counter
0x3	-	Reserved

Bits 3:2 – MODE[1:0] Timer Counter Mode

These bits select the counter mode.

These bits are not synchronized.

Value	Name	Description
0x0	COUNT16	Counter in 16-bit mode
0x1	COUNT8	Counter in 8-bit mode
0x2	COUNT32	Counter in 32-bit mode
0x3	-	Reserved

Bit 1 – ENABLE Enable

Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately, and the ENABLE Synchronization Busy bit in the SYNCBUSY register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

This bit is not enable-protected.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the TC, except DBGCTRL, to their initial state, and the TC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence; all other writes in the same write-operation will be discarded.

This bit is not enable-protected.

40.7.2.2 Control B Clear

Name: CTRLBCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

This register allows the user to clear bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set register (CTRLBSET).

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]					ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command

These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command is executed, the CMD bit group is read back as zero.
Writing '0x0' to these bits has no effect.
Writing a '1' to any of these bits clears the pending command.

Bit 2 – ONESHOT One-Shot on Counter

This bit controls one-shot operation of the TC.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit disables one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update

This bit controls the update operation of the TC buffered registers.
When CTRLB.LUPD is set, no update of the registers with the value of its buffered register is performed on the hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before a hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.
This bit has no effect when the input capture operation is enabled.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the LUPD bit.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction

This bit is used to change the direction of the counter.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

40.7.2.3 Control B Set

Name: CTRLBSET
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection, Read-synchronized, Write-Synchronized

This register allows the user to set bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Clear register (CTRLBCLR).

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]					ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command

These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command has been executed, the CMD bit group will be read back as zero.
Writing 0x0 to these bits has no effect.
Writing a value different from 0x0 to these bits will issue a command for execution.

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Force a start, restart or retrigger
0x2	STOP	Force a stop
0x3	UPDATE	Force update of double buffered registers
0x4	READSYNC	Force a read synchronization of COUNT

Bit 2 – ONESHOT One-Shot on Counter

This bit controls one-shot operation of the TC.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will enable one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update

This bit controls the update operation of the TC buffered registers.
When CTRLB.LUPD is set, no update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the LUPD bit.
This bit has no effect when input capture operation is enabled.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction

This bit is used to change the direction of the counter.
Writing a '0' to this bit has no effect

Writing a '1' to this bit will set the bit and make the counter count down.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

40.7.2.4 Event Control

Name: EVCTRL
Offset: 0x06
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
			MCEO1	MCEO0				OVFEO
Access			R/W	R/W				R/W
Reset			0	0				0

Bit	7	6	5	4	3	2	1	0
			TCEI	TCINV		EVACT[2:0]		
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bits 12, 13 – MCEOx Match or Capture Channel x Event Output Enable [x = 1..0]
These bits enable the generation of an event for every match or capture on channel x.

Value	Description
0	Match/Capture event on channel x is disabled and will not be generated.
1	Match/Capture event on channel x is enabled and will be generated for every compare/capture.

Bit 8 – OVFEO Overflow/Underflow Event Output Enable
This bit enables the Overflow/Underflow event. When enabled, an event will be generated when the counter overflows/underflows.

Value	Description
0	Overflow/Underflow event is disabled and will not be generated.
1	Overflow/Underflow event is enabled and will be generated for every counter overflow/underflow.

Bit 5 – TCEI TC Event Enable
This bit is used to enable asynchronous input events to the TC.

Value	Description
0	Incoming events are disabled.
1	Incoming events are enabled.

Bit 4 – TCINV TC Inverted Event Input Polarity
This bit inverts the asynchronous input event source.

Value	Description
0	Input event source is not inverted.
1	Input event source is inverted.

Bits 2:0 – EVACT[2:0] Event Action
These bits define the event action the TC will perform on an event.

Value	Name	Description
0x0	OFF	Event action disabled
0x1	RETRIGGER	Start, restart or retrigger TC on event
0x2	COUNT	Count on event
0x3	START	Start TC on event
0x4	STAMP	Time stamp capture
0x5	PPW	Period captured in CC0, pulse width in CC1

Value	Name	Description
0x6	PWP	Period captured in CC1, pulse width in CC0
0x7	PW	Pulse width capture

40.7.2.5 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable [x = 1..0]
Writing a '0' to these bits has no effect.
Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Disable
Writing a '0' to these bits has no effect.
Writing a '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Disable
Writing a '0' to these bits has no effect.
Writing a '1' to this bit will clear the Overflow Interrupt Enable bit, which disables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

40.7.2.6 Interrupt Enable Set

Name: INTENSET
Offset: 0x09
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable [x = 1..0]
Writing a '0' to these bits has no effect.
Writing a '1' to MCx will set the corresponding Match or Capture Channel x Interrupt Enable bit, which enables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Enable
Writing a '0' to these bits has no effect.
Writing a '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Enable
Writing a '0' to these bits has no effect.
Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

40.7.2.7 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x0A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x [x = 1..0]
This flag is set on a comparison match, or when the corresponding CCx register contains a valid capture value. This flag is set on the next CLK_TC_CNT cycle, and will generate an interrupt request if the corresponding Match or Capture Channel x Interrupt Enable bit in the Interrupt Enable Set register (INTENSET.MCx) is '1'.
Writing a '0' to these bits has no effect.
Writing a '1' to one of these bits will clear the corresponding Match or Capture Channel x interrupt flag
In capture operation, this flag is automatically cleared when CCx register is read.

Bit 1 – ERR Error Interrupt Flag
This flag is set when a new capture occurs on a channel while the corresponding Match or Capture Channel x interrupt flag is set, in which case there is no place to store the new capture.
Writing a '0' to these bits has no effect.
Writing a '1' to this bit clears the Error interrupt flag.

Bit 0 – OVF Overflow Interrupt Flag
This flag is set on the next CLK_TC_CNT cycle after an overflow condition occurs, and will generate an interrupt request if INTENCLR.OVF or INTENSET.OVF is '1'.
Writing a '0' to these bits has no effect.
Writing a '1' to this bit clears the Overflow interrupt flag.

40.7.2.8 Status

Name: STATUS
Offset: 0x0B
Reset: 0x01
Property: Read-Synchronized

Bit	7	6	5	4	3	2	1	0
			CCBUFV1	CCBUFV0	PERBUFV		SLAVE	STOP
Access			R/W	R/W	R/W		R	R
Reset			0	0	0		0	1

Bits 4, 5 – CCBUFVx Channel x Compare or Capture Buffer Valid [x = 1..0]
For a compare channel x, the bit x is set when a new value is written to the corresponding CCBUFx register.
The bit x is cleared by writing a '1' to it when CTRLB.LUPD is set, or it is cleared automatically by hardware on UPDATE condition.
For a capture channel x, the bit x is set when a valid capture value is stored in the CCBUFx register.
The bit x is cleared automatically when the CCx register is read.

Bit 3 – PERBUFV Period Buffer Valid
This bit is set when a new value is written to the PERBUF register. The bit is cleared by writing '1' to the corresponding location when CTRLB.LUPD is set, or automatically cleared by hardware on UPDATE condition. This bit is available only in 8-bit mode and will always read zero in 16- and 32-bit modes.

Bit 1 – SLAVE Client Status Flag
This bit is only available in 32-bit mode on the Client TC (i.e., TC1, TC3, TC5 and/or TC7). The bit is set when the associated Host TC (TC0, TC2, TC4 and/or TC6, respectively) is set to run in 32-bit mode.

Bit 0 – STOP Stop Status Flag
This bit is set when the TC is disabled, on a Stop command, or on an overflow/underflow condition when the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT) is '1'.

Value	Description
0	Counter is running.
1	Counter is stopped.

40.7.2.9 Waveform Generation Control

Name: WAVE
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
							WAVEGEN[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 1:0 – WAVEGEN[1:0] Waveform Generation Mode
These bits select the waveform generation operation. They affect the top value, as shown in Waveform Output Operations. They also control whether frequency or PWM waveform generation must be used. The waveform generation operations are explained in Waveform Output Operations. See *Waveform Output Operations* from Related Links.
These bits are not synchronized.

Value	Name	Operation	Top Value	Output Waveform on Match	Output Waveform on Wraparound
0x0	NFRQ	Normal frequency	PER[1] / Max	Toggle	No action
0x1	MFRQ	Match frequency	CC0	Toggle	No action
0x2	NPWM	Normal PWM	PER[1] / Max	Set	Clear
0x3	MPWM	Match PWM	CC0	Set	Clear

1. This depends on the TC mode: In 8-bit mode, the top value is the Period Value register (PER). In 16- and 32-bit mode, it is the respective MAX value.

Related Links
Waveform Output Operations

40.7.2.10 Driver Control

Name: DRVCTRL
Offset: 0x0D
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
							INVEN1	INVEN0
Access							R/W	R/W
Reset							0	0

Bits 0, 1 – INVENx Output Waveform x Invert Enable [x=1..0]
Bit x of INVEN[1:0] selects inversion of the output or capture trigger input of channel x.

Value	Description
0	Disable inversion of the WO[x] output and IO input pin.
1	Enable inversion of the WO[x] output and IO input pin.

40.7.2.11 Debug Control

Name: DBGCTRL
Offset: 0x0F
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN Run in Debug Mode
This bit is not affected by a software Reset, and must not be changed by software while the TC is enabled.

Value	Description
0	The TC is halted when the device is halted in debug mode.
1	The TC continues normal operation when the device is halted in debug mode.

40.7.2.12 Synchronization Busy

Name: SYNCBUSY
Offset: 0x10
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 6, 7 – CCx Compare/Capture Channel x Synchronization Busy [x=0..1]
For details on CC channels number, refer to each TC feature list.
This bit is set when the synchronization of CCx between clock domains is started.
This bit is also set when the CCBUFx is written, and cleared on update condition. The bit is automatically cleared when the STATUS.CCBUFx bit is cleared.

Bit 5 – PER PER Synchronization Busy
This bit is cleared when the synchronization of PER between the clock domains is complete.
This bit is set when the synchronization of PER between clock domains is started.
This bit is also set when the PER is written, and cleared on update condition. The bit is automatically cleared when the STATUS.PERBUF bit is cleared.

Bit 4 – COUNT COUNT Synchronization Busy
This bit is cleared when the synchronization of COUNT between the clock domains is complete.
This bit is set when the synchronization of COUNT between clock domains is started.

Bit 3 – STATUS STATUS Synchronization Busy
This bit is cleared when the synchronization of STATUS between the clock domains is complete.
This bit is set when a '1' is written to the Capture Channel Buffer Valid status flags (STATUS.CCBUFVx) and the synchronization of STATUS between clock domains is started.

Bit 2 – CTRLB CTRLB Synchronization Busy
This bit is cleared when the synchronization of CTRLB between the clock domains is complete.
This bit is set when the synchronization of CTRLB between clock domains is started.

Bit 1 – ENABLE ENABLE Synchronization Busy
This bit is cleared when the synchronization of ENABLE bit between the clock domains is complete.
This bit is set when the synchronization of ENABLE bit between clock domains is started.

Bit 0 – SWRST SWRST Synchronization Busy
This bit is cleared when the synchronization of SWRST bit between the clock domains is complete.
This bit is set when the synchronization of SWRST bit between clock domains is started.
Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

40.7.2.13 Counter Value, 8-bit Mode

Name: COUNT
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Note: Prior to any read access, this register must be synchronized by user by writing the according TC Command value to the Control B Set register (CTRLBSET.CMD=READSYNC).

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – COUNT[7:0] Counter Value
These bits contain the current counter value.

40.7.2.14 Period Value, 8-bit Mode

Name: PER
Offset: 0x1B
Reset: 0xFF
Property: Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	PER[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 7:0 – PER[7:0] Period Value
These bits hold the value of the Period Buffer register PERBUF. The value is copied to PER register on UPDATE condition.

40.7.2.15 Channel x Compare/Capture Value, 8-bit Mode

Name: CCx
Offset: 0x1C + x*0x01 [x=0..1]
Reset: 0x00
Property: Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	CC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – CC[7:0] Channel x Compare/Capture Value
These bits contain the compare/capture value in 8-bit TC mode. In Match frequency (MFRQ) or Match PWM (MPWM) waveform operation (WAVE.WAVEGEN), the CC0 register is used as a period register.

40.7.2.16 Period Buffer Value, 8-bit Mode

Name: PERBUF
Offset: 0x2F
Reset: 0xFF
Property: Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	PERBUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	1

Bits 7:0 – PERBUF[7:0] Period Buffer Value
These bits hold the value of the period buffer register. The value is copied to PER register on UPDATE condition.

40.7.2.17 Channel x Compare Buffer Value, 8-bit Mode

Name: CCBUFx
Offset: 0x30 + x*0x01 [x=0..1]
Reset: 0x00
Property: Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	CCBUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – CCBUF[7:0] Channel x Compare Buffer Value
These bits hold the value of the Channel x Compare Buffer Value. When the buffer valid flag is '1' and double buffering is enabled (CTRLBCLR.LUPD=1), the data from buffer registers will be copied into the corresponding CCx register under UPDATE condition (CTRLBSET.CMD=0x3), including the software update command.

40.7.3 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
		15:8	DMAOS				ALOCK	PRESCALER[2:0]		
		23:16			COPEN1	COPEN0			CAPTEN1	CAPTEN0
		31:24				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
0x04	CTRLBCLR	7:0	CMD[2:0]					ONESHOT	LUPD	DIR
0x05	CTRLBSET	7:0	CMD[2:0]					ONESHOT	LUPD	DIR
0x06	EVCTRL	7:0			TCEI	TCINV		EVACT[2:0]		
		15:8			MCEO1	MCEO0				OVFEO
0x08	INTENCLR	7:0			MC1	MC0			ERR	OVF
0x09	INTENSET	7:0			MC1	MC0			ERR	OVF
0x0A	INTFLAG	7:0			MC1	MC0			ERR	OVF
0x0B	STATUS	7:0			CCBUFV1	CCBUFV0	PERBUFV		SLAVE	STOP
0x0C	WAVE	7:0							WAVEGEN[1:0]	
0x0D	DRVCTRL	7:0							INVEN1	INVEN0
0x0E	Reserved									
0x0F	DBGCTRL	7:0								DBGRUN
0x10	SYNCBUSY	7:0	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
0x11 ... 0x13	Reserved									
0x14	COUNT	7:0	COUNT[7:0]							
		15:8	COUNT[15:8]							
0x16 ... 0x1B	Reserved									
0x1C	CC0	7:0	CC[7:0]							
		15:8	CC[15:8]							
0x1E	CC1	7:0	CC[7:0]							
		15:8	CC[15:8]							
0x20 ... 0x2F	Reserved									
0x30	CCBUF0	7:0	CCBUF[7:0]							
		15:8	CCBUF[15:8]							
0x32	CCBUF1	7:0	CCBUF[7:0]							
		15:8	CCBUF[15:8]							

40.7.4 Register Description - 16-bit Mode

40.7.4.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Enable-Protected

Bit	31	30	29	28	27	26	25	24
				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
Access				R/W	R/W		R/W	R/W
Reset				0	0		0	0

Bit	23	22	21	20	19	18	17	16
			COPEN1	COPEN0			CAPTEN1	CAPTEN0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	15	14	13	12	11	10	9	8
	DMAOS				ALOCK	PRESCALER[2:0]		
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
Reset	0	0	0	0	0	0	0	0

Bits 28:27 – CAPTMODE1[1:0] Capture mode Channel 1
These bits select the channel 1 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 25:24 – CAPTMODE0[1:0] Capture mode Channel 0
These bits select the channel 0 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 20, 21 – COPENx Capture On Pin x Enable [x=1..0]
Bit x of COPEN[1:0] selects the trigger source for capture operation, either events or I/O pin input.
This bit is not synchronized.

Value	Description
0	Event from Event System is selected as trigger source for capture operation on channel x.
1	I/O pin is selected as trigger source for capture operation on channel x.

Bits 16, 17 – CAPTENx Capture Channel x Enable [x=1..0]
Bit x of CAPTEN[1:0] selects whether channel x is a capture or a compare channel.

These bits are not synchronized.

Value	Description
0	CAPTEN disables capture on channel x.
1	CAPTEN enables capture on channel x.

Bit 15 – DMAOS DMA One-Shot Trigger Mode

This bit enables the DMA One-shot Trigger Mode.
Writing a '1' to this bit will generate a DMA trigger on TC cycle following a TC_CTRLBSET_CMD_DMAOS command.
Writing a '0' to this bit will generate DMA triggers on each TC cycle.
This bit is not synchronized.

Bit 11 – ALOCK Auto Lock

When this bit is set, Lock bit update (LUPD) is set to '1' on each overflow/underflow or re-trigger event.
This bit is not synchronized.

Value	Description
0	The LUPD bit is not affected on overflow/underflow, and re-trigger event.
1	The LUPD bit is set on each overflow/underflow or re-trigger event.

Bits 10:8 – PRESCALER[2:0] Prescaler

These bits select the counter prescaler factor.
These bits are not synchronized.

Value	Name	Description
0x0	DIV1	Prescaler: GCLK_TC
0x1	DIV2	Prescaler: GCLK_TC/2
0x2	DIV4	Prescaler: GCLK_TC/4
0x3	DIV8	Prescaler: GCLK_TC/8
0x4	DIV16	Prescaler: GCLK_TC/16
0x5	DIV64	Prescaler: GCLK_TC/64
0x6	DIV256	Prescaler: GCLK_TC/256
0x7	DIV1024	Prescaler: GCLK_TC/1024

Bit 7 – ONDEMAND Clock On Demand

This bit selects the clock requirements when the TC is stopped.
In standby mode, if the Run in Standby bit (CTRLA.RUNSTDBY) is '0', ONDEMAND is forced to '0'.
This bit is not synchronized.

Value	Description
0	The On Demand is disabled. If On Demand is disabled, the TC will continue to request the clock when its operation is stopped (STATUS.STOP=1).
1	The On Demand is enabled. When On Demand is enabled, the stopped TC will not request the clock. The clock is requested when a software re-trigger command is applied or when an event with start/re-trigger action is detected.

Bit 6 – RUNSTDBY Run in Standby

This bit is used to keep the TC running in standby mode.
This bit is not synchronized.

Value	Description
0	The TC is halted in standby.
1	The TC continues to run in standby.

Bits 5:4 – PRESCSYNC[1:0] Prescaler and Counter Synchronization

These bits select whether the counter must wrap around on the next GCLK_TCx clock or the next prescaled GCLK_TCx clock. It also makes it possible to reset the prescaler.
These bits are not synchronized.

Value	Name	Description
0x0	GCLK	Reload or reset the counter on next generic clock
0x1	PRESC	Reload or reset the counter on next prescaler clock
0x2	RESYNC	Reload or reset the counter on next generic clock. Reset the prescaler counter
0x3	-	Reserved

Bits 3:2 – MODE[1:0] Timer Counter Mode

These bits select the counter mode.
These bits are not synchronized.

Value	Name	Description
0x0	COUNT16	Counter in 16-bit mode
0x1	COUNT8	Counter in 8-bit mode
0x2	COUNT32	Counter in 32-bit mode
0x3	-	Reserved

Bit 1 – ENABLE Enable

Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately, and the ENABLE Synchronization Busy bit in the SYNCBUSY register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.
This bit is not enable-protected.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.
Writing a '1' to this bit resets all registers in the TC, except DBGCTRL, to their initial state, and the TC will be disabled.
Writing a '1' to CTRLA.SWRST will always take precedence; all other writes in the same write-operation will be discarded.
This bit is not enable-protected.

40.7.4.2 Control B Clear

Name: CTRLBCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

This register allows the user to clear bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set register (CTRLBSET).

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]					ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command

These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TCx clock cycle. When a command has been executed, the CMD bit group will be read back as '0'.
Writing '0x0' to these bits has no effect.
Writing a '1' to any of these bits will clear the pending command.

Bit 2 – ONESHOT One-Shot on Counter

This bit controls one-shot operation of the TC.
Writing a '0' to this bit has no effect
Writing a '1' to this bit will disable one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update

This bit controls the update operation of the TC buffered registers.
When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.
This bit has no effect when input capture operation is enabled.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the LUPD bit.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction

This bit is used to change the direction of the counter.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clears the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

40.7.4.3 Control B Set

Name: CTRLBSET
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

This register allows the user to set bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Clear register (CTRLBCLR).

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]					ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command
These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command has been executed, the CMD bit group will be read back as '0'.
Writing 0x0 to these bits has no effect.
Writing a value different from 0x0 from the following table will issue a command for execution.

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Force a start, restart or retrigger
0x2	STOP	Force a stop
0x3	UPDATE	Force update of double buffered registers
0x4	READSYNC	Force a read synchronization of COUNT

Bit 2 – ONESHOT One-Shot on Counter
This bit controls one-shot operation of the TC.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will enable one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update
This bit controls the update operation of the TC buffered registers.
When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the LUPD bit.
This bit has no effect when input capture operation is enabled.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction
This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect
Writing a '1' to this bit will set the bit and make the counter count down.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

40.7.4.4 Event Control

Name: EVCTRL
Offset: 0x06
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
			MCEO1	MCEO0				OVFEO
Access			R/W	R/W				R/W
Reset			0	0				0

Bit	7	6	5	4	3	2	1	0
			TCEI	TCINV		EVACT[2:0]		
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bits 12, 13 – MCEOx Match or Capture Channel x Event Output Enable [x = 1..0]
These bits enable the generation of an event for every match or capture on channel x.

Value	Description
0	Match/Capture event on channel x is disabled and will not be generated.
1	Match/Capture event on channel x is enabled and will be generated for every compare/capture.

Bit 8 – OVFEO Overflow/Underflow Event Output Enable
This bit enables the Overflow/Underflow event. When enabled, an event will be generated when the counter overflows/underflows.

Value	Description
0	Overflow/Underflow event is disabled and will not be generated.
1	Overflow/Underflow event is enabled and will be generated for every counter overflow/underflow.

Bit 5 – TCEI TC Event Enable
This bit is used to enable asynchronous input events to the TC.

Value	Description
0	Incoming events are disabled.
1	Incoming events are enabled.

Bit 4 – TCINV TC Inverted Event Input Polarity
This bit inverts the asynchronous input event source.

Value	Description
0	Input event source is not inverted.
1	Input event source is inverted.

Bits 2:0 – EVACT[2:0] Event Action
These bits define the event action the TC will perform on an event.

Value	Name	Description
0x0	OFF	Event action disabled
0x1	RETRIGGER	Start, restart or retrigger TC on event
0x2	COUNT	Count on event
0x3	START	Start TC on event
0x4	STAMP	Time stamp capture
0x5	PPW	Period captured in CC0, pulse width in CC1

Value	Name	Description
0x6	PWP	Period captured in CC1, pulse width in CC0
0x7	PW	Pulse width capture

40.7.4.5 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable
Writing a '0' to these bits has no effect.
Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Disable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Disable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Overflow Interrupt Enable bit, which disables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

40.7.4.6 Interrupt Enable Set

Name: INTENSET
Offset: 0x09
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable
Writing a '0' to these bits has no effect.
Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Enable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Enable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

40.7.4.7 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x0A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x

This flag is set on a comparison match, or when the corresponding CCx register contains a valid capture value. This flag is set on the next CLK_TC_CNT cycle, and will generate an interrupt request if the corresponding Match or Capture Channel x Interrupt Enable bit in the Interrupt Enable Set register (INTENSET.MCx) is '1'.
Writing a '0' to one of these bits has no effect.
Writing a '1' to one of these bits will clear the corresponding Match or Capture Channel x interrupt flag
In capture operation, this flag is automatically cleared when CCx register is read.

Bit 1 – ERR Error Interrupt Flag

This flag is set when a new capture occurs on a channel while the corresponding Match or Capture Channel x interrupt flag is set, in which case there is nowhere to store the new capture.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Error interrupt flag.

Bit 0 – OVF Overflow Interrupt Flag

This flag is set on the next CLK_TC_CNT cycle after an overflow condition occurs, and will generate an interrupt request if INTENCLR.OVF or INTENSET.OVF is '1'.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Overflow interrupt flag.

40.7.4.8 Status

Name: STATUS
Offset: 0x0B
Reset: 0x01
Property: Read-Synchronized, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
			CCBUFV1	CCBUFV0	PERBUFV		SLAVE	STOP
Access			R/W	R/W	R/W		R	R
Reset			0	0	0		0	1

Bits 4, 5 – CCBUFVx Channel x Compare or Capture Buffer Valid
For a compare channel x, the bit x is set when a new value is written to the corresponding CCBUFx register.
The bit x is cleared by writing a '1' to it when CTRLB.LUPD is set, or it is cleared automatically by hardware on UPDATE condition.
For a capture channel x, the bit x is set when a valid capture value is stored in the CCBUFx register.
The bit x is cleared automatically when the CCx register is read.

Bit 3 – PERBUFV Period Buffer Valid
This bit is set when a new value is written to the PERBUF register. The bit is cleared by writing '1' to the corresponding location when CTRLB.LUPD is set, or automatically cleared by hardware on UPDATE condition. This bit is available only in 8-bit mode and will always read zero in 16- and 32-bit modes.

Bit 1 – SLAVE Client Status Flag
This bit is only available in 32-bit mode on the client TC (i.e., TC1 and/or TC3). The bit is set when the associated host TC (TC0 and TC2, respectively) is set to run in 32-bit mode.

Bit 0 – STOP Stop Status Flag
This bit is set when the TC is disabled, on a Stop command, or on an overflow/underflow condition when the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT) is '1'.

Value	Description
0	Counter is running.
1	Counter is stopped.

40.7.4.9 Waveform Generation Control

Name: WAVE
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
							WAVEGEN[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 1:0 – WAVEGEN[1:0] Waveform Generation Mode

These bits select the waveform generation operation. They affect the top value, as shown in Waveform Output Operations. They also control whether frequency or PWM waveform generation must be used. The waveform generation operations are explained in Waveform Output Operations. See *Waveform Output Operations* from Related Links.

These bits are not synchronized.

Value	Name	Operation	Top Value	Output Waveform on Match	Output Waveform on Wraparound
0x0	NFRQ	Normal frequency	PER[1] / Max	Toggle	No action
0x1	MFRQ	Match frequency	CC0	Toggle	No action
0x2	NPWM	Normal PWM	PER[1] / Max	Set	Clear
0x3	MPWM	Match PWM	CC0	Set	Clear

1. This depends on the TC mode: In 8-bit mode, the top value is the Period Value register (PER). In 16- and 32-bit mode, it is the respective MAX value.

Related Links

Waveform Output Operations

40.7.4.10 Driver Control

Name: DRVCTRL
Offset: 0x0D
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
							INVEN1	INVEN0
Access							R/W	R/W
Reset							0	0

Bits 0, 1 – INVENx Output Waveform x Invert Enable
INVENx bit selects inversion of the output or capture trigger input of channel x.

Value	Description
0	Disable inversion of the WO[x] output and IO input pin.
1	Enable inversion of the WO[x] output and IO input pin.

40.7.4.11 Debug Control

Name: DBGCTRL
Offset: 0x0F
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN Run in Debug Mode

This bit is not affected by a software Reset, and must not be changed by software while the TC is enabled.

Value	Description
0	The TC is halted when the device is halted in debug mode.
1	The TC continues normal operation when the device is halted in debug mode.

40.7.4.12 Synchronization Busy

Name: SYNCBUSY
Offset: 0x10
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 6, 7 – CCx Compare/Capture Channel x Synchronization Busy [x=0..1]
For details on CC channels number, refer to each TC feature list.
This bit is set when the synchronization of CCx between clock domains is started.
This bit is also set when the CCBUFx is written, and cleared on update condition. The bit is automatically cleared when the STATUS.CCBUFx bit is cleared.

Bit 5 – PER PER Synchronization Busy
This bit is cleared when the synchronization of PER between the clock domains is complete.
This bit is set when the synchronization of PER between clock domains is started.
This bit is also set when the PER is written, and cleared on update condition. The bit is automatically cleared when the STATUS.PERBUF bit is cleared.

Bit 4 – COUNT COUNT Synchronization Busy
This bit is cleared when the synchronization of COUNT between the clock domains is complete.
This bit is set when the synchronization of COUNT between clock domains is started.

Bit 3 – STATUS STATUS Synchronization Busy
This bit is cleared when the synchronization of STATUS between the clock domains is complete.
This bit is set when a '1' is written to the Capture Channel Buffer Valid status flags (STATUS.CCBUFVx) and the synchronization of STATUS between clock domains is started.

Bit 2 – CTRLB CTRLB Synchronization Busy
This bit is cleared when the synchronization of CTRLB between the clock domains is complete.
This bit is set when the synchronization of CTRLB between clock domains is started.

Bit 1 – ENABLE ENABLE Synchronization Busy
This bit is cleared when the synchronization of ENABLE bit between the clock domains is complete.
This bit is set when the synchronization of ENABLE bit between clock domains is started.

Bit 0 – SWRST SWRST Synchronization Busy
This bit is cleared when the synchronization of SWRST bit between the clock domains is complete.
This bit is set when the synchronization of SWRST bit between clock domains is started.
Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

40.7.4.13 Counter Value, 16-bit Mode

Name: COUNT
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Note: Prior to any read access, this register must be synchronized by user by writing the according TC Command value to the Control B Set register (CTRLBSET.CMD=READSYNC).

Bit	15	14	13	12	11	10	9	8
	COUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – COUNT[15:0] Counter Value
These bits contain the current counter value.

40.7.4.14 Channel x Compare/Capture Value, 16-bit Mode

Name: CCx
Offset: 0x1C + x*0x02 [x=0..1]
Reset: 0x0000
Property: Write-Synchronized

Bit	15	14	13	12	11	10	9	8
	CC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CC[15:0] Channel x Compare/Capture Value
These bits contain the compare/capture value in 16-bit TC mode. In Match frequency (MFRQ) or Match PWM (MPWM) waveform operation (WAVE.WAVEGEN), the CC0 register is used as a period register.

40.7.4.15 Channel x Compare Buffer Value, 16-bit Mode

Name: CCBUFx
Offset: 0x30 + x*0x02 [x=0..1]
Reset: 0x0000
Property: Write-Synchronized

Bit	15	14	13	12	11	10	9	8
	CCBUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CCBUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – CCBUF[15:0] Channel x Compare Buffer Value

These bits hold the value of the Channel x Compare Buffer Value. When the buffer valid flag is '1' and double buffering is enabled (CTRLBCLR.LUPD=1), the data from buffer registers will be copied into the corresponding CCx register under UPDATE condition (CTRLBSET.CMD=0x3), including the software update command.

40.7.5 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
		15:8	DMAOS				ALOCK	PRESCALER[2:0]		
		23:16			COPEN1	COPEN0			CAPTEN1	CAPTEN0
		31:24				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
0x04	CTRLBCLR	7:0	CMD[2:0]					ONESHOT	LUPD	DIR
0x05	CTRLBSET	7:0	CMD[2:0]					ONESHOT	LUPD	DIR
0x06	EVCTRL	7:0			TCEI	TCINV		EVACT[2:0]		
		15:8			MCEO1	MCEO0				OVFEO
0x08	INTENCLR	7:0			MC1	MC0			ERR	OVF
0x09	INTENSET	7:0			MC1	MC0			ERR	OVF
0x0A	INTFLAG	7:0			MC1	MC0			ERR	OVF
0x0B	STATUS	7:0			CCBUFV1	CCBUFV0	PERBUFV		SLAVE	STOP
0x0C	WAVE	7:0							WAVEGEN[1:0]	
0x0D	DRVCTRL	7:0							INVEN1	INVEN0
0x0E	Reserved									
0x0F	DBGCTRL	7:0								DBGRUN
0x10	SYNCBUSY	7:0	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
0x11 ... 0x13	Reserved									
0x14	COUNT	7:0	COUNT[7:0]							
		15:8	COUNT[15:8]							
		23:16	COUNT[23:16]							
		31:24	COUNT[31:24]							
0x18 ... 0x1B	Reserved									
0x1C	CC0	7:0	CC[7:0]							
		15:8	CC[15:8]							
		23:16	CC[23:16]							
		31:24	CC[31:24]							
0x20	CC1	7:0	CC[7:0]							
		15:8	CC[15:8]							
		23:16	CC[23:16]							
		31:24	CC[31:24]							
0x24 ... 0x2F	Reserved									
0x30	CCBUF0	7:0	CCBUF[7:0]							
		15:8	CCBUF[15:8]							
		23:16	CCBUF[23:16]							
		31:24	CCBUF[31:24]							
0x34	CCBUF1	7:0	CCBUF[7:0]							
		15:8	CCBUF[15:8]							
		23:16	CCBUF[23:16]							
		31:24	CCBUF[31:24]							

40.7.6 Register Description - 32-bit Mode

40.7.6.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Enable-Protected

Bit	31	30	29	28	27	26	25	24
				CAPTMODE1[1:0]			CAPTMODE0[1:0]	
Access				R/W	R/W		R/W	R/W
Reset				0	0		0	0

Bit	23	22	21	20	19	18	17	16
			COPEN1	COPEN0			CAPTEN1	CAPTEN0
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bit	15	14	13	12	11	10	9	8
	DMAOS				ALOCK	PRESCALER[2:0]		
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY	PRESCSYNC[1:0]		MODE[1:0]		ENABLE	SWRST
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
Reset	0	0	0	0	0	0	0	0

Bits 28:27 – CAPTMODE1[1:0] Capture mode Channel 1
These bits select the channel 1 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 25:24 – CAPTMODE0[1:0] Capture mode Channel 0
These bits select the channel 0 capture mode.

Value	Name	Description
0x0	DEFAULT	Default capture
0x1	CAPTMIN	Minimum capture
0x2	CAPTMAX	Maximum capture
0x3		Reserved

Bits 20, 21 – COPENx Capture On Pin x Enable [x=1..0]
Bit x of COPEN[1:0] selects the trigger source for capture operation, either events or I/O pin input.
This bit is not synchronized.

Value	Description
0	Event from Event System is selected as trigger source for capture operation on channel x.
1	I/O pin is selected as trigger source for capture operation on channel x.

Bits 16, 17 – CAPTENx Capture Channel x Enable [x=1..0]
Bit x of CAPTEN[1:0] selects whether channel x is a capture or a compare channel.

These bits are not synchronized.

Value	Description
0	CAPTEN disables capture on channel x.
1	CAPTEN enables capture on channel x.

Bit 15 – DMAOS DMA One-Shot Trigger Mode

This bit enables the DMA One-shot Trigger Mode.
Writing a '1' to this bit will generate a DMA trigger on TC cycle following a TC_CTRLBSET_CMD_DMAOS command.
Writing a '0' to this bit will generate DMA triggers on each TC cycle.
This bit is not synchronized.

Bit 11 – ALOCK Auto Lock

When this bit is set, Lock bit update (LUPD) is set to '1' on each overflow/underflow or re-trigger event.
This bit is not synchronized.

Value	Description
0	The LUPD bit is not affected on overflow/underflow, and re-trigger event.
1	The LUPD bit is set on each overflow/underflow or re-trigger event.

Bits 10:8 – PRESCALER[2:0] Prescaler

These bits select the counter prescaler factor.
These bits are not synchronized.

Value	Name	Description
0x0	DIV1	Prescaler: GCLK_TC
0x1	DIV2	Prescaler: GCLK_TC/2
0x2	DIV4	Prescaler: GCLK_TC/4
0x3	DIV8	Prescaler: GCLK_TC/8
0x4	DIV16	Prescaler: GCLK_TC/16
0x5	DIV64	Prescaler: GCLK_TC/64
0x6	DIV256	Prescaler: GCLK_TC/256
0x7	DIV1024	Prescaler: GCLK_TC/1024

Bit 7 – ONDEMAND Clock On Demand

This bit selects the clock requirements when the TC is stopped.
In standby mode, if the Run in Standby bit (CTRLA.RUNSTDBY) is '0', ONDEMAND is forced to '0'.
This bit is not synchronized.

Value	Description
0	The On Demand is disabled. If On Demand is disabled, the TC will continue to request the clock when its operation is stopped (STATUS.STOP=1).
1	The On Demand is enabled. When On Demand is enabled, the stopped TC will not request the clock. The clock is requested when a software re-trigger command is applied or when an event with start/re-trigger action is detected.

Bit 6 – RUNSTDBY Run in Standby

This bit is used to keep the TC running in standby mode.
This bit is not synchronized.

Value	Description
0	The TC is halted in standby.
1	The TC continues to run in standby.

Bits 5:4 – PRESCSYNC[1:0] Prescaler and Counter Synchronization

These bits select whether the counter must wrap around on the next GCLK_TCx clock or the next prescaled GCLK_TCx clock. It also makes it possible to reset the prescaler.
These bits are not synchronized.

Value	Name	Description
0x0	GCLK	Reload or reset the counter on next generic clock
0x1	PRESC	Reload or reset the counter on next prescaler clock
0x2	RESYNC	Reload or reset the counter on next generic clock. Reset the prescaler counter
0x3	-	Reserved

Bits 3:2 – MODE[1:0] Timer Counter Mode

These bits select the counter mode.
These bits are not synchronized.

Value	Name	Description
0x0	COUNT16	Counter in 16-bit mode
0x1	COUNT8	Counter in 8-bit mode
0x2	COUNT32	Counter in 32-bit mode
0x3	-	Reserved

Bit 1 – ENABLE Enable

Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRLA.ENABLE will read back immediately, and the ENABLE Synchronization Busy bit in the SYNCBUSY register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.
This bit is not enable-protected.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.
Writing a '1' to this bit resets all registers in the TC, except DBGCTRL, to their initial state, and the TC will be disabled.
Writing a '1' to CTRLA.SWRST will always take precedence; all other writes in the same write-operation will be discarded.
This bit is not enable-protected.

40.7.6.2 Control B Clear

Name: CTRLBCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

This register allows the user to clear bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set register (CTRLBSET).

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]					ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command
These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TCx clock cycle. When a command has been executed, the CMD bit group will be read back as '0'.
Writing '0x0' to these bits has no effect.
Writing a '1' to any of these bits will clear the pending command.

Bit 2 – ONESHOT One-Shot on Counter
This bit controls one-shot operation of the TC.
Writing a '0' to this bit has no effect
Writing a '1' to this bit will disable one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update
This bit controls the update operation of the TC buffered registers.
When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.
This bit has no effect when input capture operation is enabled.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the LUPD bit.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction
This bit is used to change the direction of the counter.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clears the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

40.7.6.3 Control B Set

Name: CTRLBSET
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection, Read-Synchronized, Write-Synchronized

This register allows the user to set bits in the CTRLB register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Clear register (CTRLBCLR).

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]					ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W			R/W	R/W	R/W
Reset	0	0	0			0	0	0

Bits 7:5 – CMD[2:0] Command

These bits are used for software control of the TC. The commands are executed on the next prescaled GCLK_TC clock cycle. When a command has been executed, the CMD bit group will be read back as '0'.
Writing 0x0 to these bits has no effect.
Writing a value different from 0x0 from the following table will issue a command for execution.

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Force a start, restart or retrigger
0x2	STOP	Force a stop
0x3	UPDATE	Force update of double buffered registers
0x4	READSYNC	Force a read synchronization of COUNT

Bit 2 – ONESHOT One-Shot on Counter

This bit controls one-shot operation of the TC.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will enable one-shot operation.

Value	Description
0	The TC will wrap around and continue counting on an overflow/underflow condition.
1	The TC will wrap around and stop on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update

This bit controls the update operation of the TC buffered registers.
When CTRLB.LUPD is set, no any update of the registers with value of its buffered register is performed on hardware UPDATE condition. Locking the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the LUPD bit.
This bit has no effect when input capture operation is enabled.

Value	Description
0	The CCBUFx and PERBUF buffer registers value are copied into CCx and PER registers on hardware update condition.
1	The CCBUFx and PERBUF buffer registers value are not copied into CCx and PER registers on hardware update condition.

Bit 0 – DIR Counter Direction

This bit is used to change the direction of the counter.

Writing a '0' to this bit has no effect
Writing a '1' to this bit will set the bit and make the counter count down.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

40.7.6.4 Event Control

Name: EVCTRL
Offset: 0x06
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected

Bit	15	14	13	12	11	10	9	8
			MCEO1	MCEO0				OVFEO
Access			R/W	R/W				R/W
Reset			0	0				0

Bit	7	6	5	4	3	2	1	0
			TCEI	TCINV		EVACT[2:0]		
Access			R/W	R/W		R/W	R/W	R/W
Reset			0	0		0	0	0

Bits 12, 13 – MCEOx Match or Capture Channel x Event Output Enable [x = 1..0]
These bits enable the generation of an event for every match or capture on channel x.

Value	Description
0	Match/Capture event on channel x is disabled and will not be generated.
1	Match/Capture event on channel x is enabled and will be generated for every compare/capture.

Bit 8 – OVFEO Overflow/Underflow Event Output Enable
This bit enables the Overflow/Underflow event. When enabled, an event will be generated when the counter overflows/underflows.

Value	Description
0	Overflow/Underflow event is disabled and will not be generated.
1	Overflow/Underflow event is enabled and will be generated for every counter overflow/underflow.

Bit 5 – TCEI TC Event Enable
This bit is used to enable asynchronous input events to the TC.

Value	Description
0	Incoming events are disabled.
1	Incoming events are enabled.

Bit 4 – TCINV TC Inverted Event Input Polarity
This bit inverts the asynchronous input event source.

Value	Description
0	Input event source is not inverted.
1	Input event source is inverted.

Bits 2:0 – EVACT[2:0] Event Action
These bits define the event action the TC will perform on an event.

Value	Name	Description
0x0	OFF	Event action disabled
0x1	RETRIGGER	Start, restart or retrigger TC on event
0x2	COUNT	Count on event
0x3	START	Start TC on event
0x4	STAMP	Time stamp capture
0x5	PPW	Period captured in CC0, pulse width in CC1

Value	Name	Description
0x6	PWP	Period captured in CC1, pulse width in CC0
0x7	PW	Pulse width capture

40.7.6.5 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable
Writing a '0' to these bits has no effect.
Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Disable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Error Interrupt Enable bit, which disables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Disable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Overflow Interrupt Enable bit, which disables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

40.7.6.6 Interrupt Enable Set

Name: INTENSET
Offset: 0x09
Reset: 0x00
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear register (INTENCLR).

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x Interrupt Enable
Writing a '0' to these bits has no effect.
Writing a '1' to MCx will clear the corresponding Match or Capture Channel x Interrupt Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 1 – ERR Error Interrupt Enable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Error Interrupt Enable bit, which enables the Error interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Enable
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Overflow Interrupt Enable bit, which enables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

40.7.6.7 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x0A
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
			MC1	MC0			ERR	OVF
Access			R/W	R/W			R/W	R/W
Reset			0	0			0	0

Bits 4, 5 – MCx Match or Capture Channel x
This flag is set on a comparison match, or when the corresponding CCx register contains a valid capture value. This flag is set on the next CLK_TC_CNT cycle, and will generate an interrupt request if the corresponding Match or Capture Channel x Interrupt Enable bit in the Interrupt Enable Set register (INTENSET.MCx) is '1'.
Writing a '0' to one of these bits has no effect.
Writing a '1' to one of these bits will clear the corresponding Match or Capture Channel x interrupt flag
In capture operation, this flag is automatically cleared when CCx register is read.

Bit 1 – ERR Error Interrupt Flag
This flag is set when a new capture occurs on a channel while the corresponding Match or Capture Channel x interrupt flag is set, in which case there is nowhere to store the new capture.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Error interrupt flag.

Bit 0 – OVF Overflow Interrupt Flag
This flag is set on the next CLK_TC_CNT cycle after an overflow condition occurs, and will generate an interrupt request if INTENCLR.OVF or INTENSET.OVF is '1'.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Overflow interrupt flag.

40.7.6.8 Status

Name: STATUS
Offset: 0x0B
Reset: 0x01
Property: Read-Synchronized, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
			CCBUFV1	CCBUFV0	PERBUFV		SLAVE	STOP
Access			R/W	R/W	R/W		R	R
Reset			0	0	0		0	1

Bits 4, 5 – CCBUFVx Channel x Compare or Capture Buffer Valid

For a compare channel x, the bit x is set when a new value is written to the corresponding CCBUFx register.
The bit x is cleared by writing a '1' to it when CTRLB.LUPD is set, or it is cleared automatically by hardware on UPDATE condition.
For a capture channel x, the bit x is set when a valid capture value is stored in the CCBUFx register.
The bit x is cleared automatically when the CCx register is read.

Bit 3 – PERBUFV Period Buffer Valid

This bit is set when a new value is written to the PERBUF register. The bit is cleared by writing '1' to the corresponding location when CTRLB.LUPD is set, or automatically cleared by hardware on UPDATE condition. This bit is available only in 8-bit mode and will always read zero in 16- and 32-bit modes.

Bit 1 – SLAVE Client Status Flag

This bit is only available in 32-bit mode on the client TC (i.e., TC1 and/or TC3). The bit is set when the associated host TC (TC0 and TC2, respectively) is set to run in 32-bit mode.

Bit 0 – STOP Stop Status Flag

This bit is set when the TC is disabled, on a Stop command, or on an overflow/underflow condition when the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT) is '1'.

Value	Description
0	Counter is running.
1	Counter is stopped.

40.7.6.9 Waveform Generation Control

Name: WAVE
Offset: 0x0C
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
							WAVEGEN[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 1:0 – WAVEGEN[1:0] Waveform Generation Mode

These bits select the waveform generation operation. They affect the top value, as shown in Waveform Output Operations. They also control whether frequency or PWM waveform generation must be used. The waveform generation operations are explained in Waveform Output Operations. See *Waveform Output Operations* from Related Links.
These bits are not synchronized.

Value	Name	Operation	Top Value	Output Waveform on Match	Output Waveform on Wraparound
0x0	NFRQ	Normal frequency	PER[1] / Max	Toggle	No action
0x1	MFRQ	Match frequency	CC0	Toggle	No action
0x2	NPWM	Normal PWM	PER[1] / Max	Set	Clear
0x3	MPWM	Match PWM	CC0	Set	Clear

1. This depends on the TC mode: In 8-bit mode, the top value is the Period Value register (PER). In 16- and 32-bit mode, it is the respective MAX value.

Related Links
Waveform Output Operations

40.7.6.10 Driver Control

Name: DRVCTRL
Offset: 0x0D
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
							INVEN1	INVEN0
Access							R/W	R/W
Reset							0	0

Bits 0, 1 – INVENx Output Waveform x Invert Enable
INVENx bit selects inversion of the output or capture trigger input of channel x.

Value	Description
0	Disable inversion of the WO[x] output and IO input pin.
1	Enable inversion of the WO[x] output and IO input pin.

40.7.6.11 Debug Control

Name: DBGCTRL
Offset: 0x0F
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								DBGRUN
Access								R/W
Reset								0

Bit 0 – DBGRUN Run in Debug Mode

This bit is not affected by a software Reset, and must not be changed by software while the TC is enabled.

Value	Description
0	The TC is halted when the device is halted in debug mode.
1	The TC continues normal operation when the device is halted in debug mode.

40.7.6.12 Synchronization Busy

Name: SYNCBUSY
Offset: 0x10
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	CC1	CC0	PER	COUNT	STATUS	CTRLB	ENABLE	SWRST
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 6, 7 – CCx Compare/Capture Channel x Synchronization Busy [x=0..1]
For details on CC channels number, refer to each TC feature list.
This bit is set when the synchronization of CCx between clock domains is started.
This bit is also set when the CCBUFx is written, and cleared on update condition. The bit is automatically cleared when the STATUS.CCBUFx bit is cleared.

Bit 5 – PER PER Synchronization Busy
This bit is cleared when the synchronization of PER between the clock domains is complete.
This bit is set when the synchronization of PER between clock domains is started.
This bit is also set when the PER is written, and cleared on update condition. The bit is automatically cleared when the STATUS.PERBUF bit is cleared.

Bit 4 – COUNT COUNT Synchronization Busy
This bit is cleared when the synchronization of COUNT between the clock domains is complete.
This bit is set when the synchronization of COUNT between clock domains is started.

Bit 3 – STATUS STATUS Synchronization Busy
This bit is cleared when the synchronization of STATUS between the clock domains is complete.
This bit is set when a '1' is written to the Capture Channel Buffer Valid status flags (STATUS.CCBUFVx) and the synchronization of STATUS between clock domains is started.

Bit 2 – CTRLB CTRLB Synchronization Busy
This bit is cleared when the synchronization of CTRLB between the clock domains is complete.
This bit is set when the synchronization of CTRLB between clock domains is started.

Bit 1 – ENABLE ENABLE Synchronization Busy
This bit is cleared when the synchronization of ENABLE bit between the clock domains is complete.
This bit is set when the synchronization of ENABLE bit between clock domains is started.

Bit 0 – SWRST SWRST Synchronization Busy
This bit is cleared when the synchronization of SWRST bit between the clock domains is complete.
This bit is set when the synchronization of SWRST bit between clock domains is started.
Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST cleared by hardware.

40.7.6.13 Counter Value, 32-bit Mode

Name: COUNT
Offset: 0x14
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Note: Prior to any read access, this register must be synchronized by user by writing the according TC Command value to the Control B Set register (CTRLBSET.CMD=READSYNC).

Bit	31	30	29	28	27	26	25	24
	COUNT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	COUNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	COUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – COUNT[31:0] Counter Value
These bits contain the current counter value.

40.7.6.14 Channel x Compare/Capture Value, 32-bit Mode

Name: CCx
Offset: 0x1C + x*0x04 [x=0..1]
Reset: 0x00000000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
	CC[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	23	22	21	20	19	18	17	16
	CC[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8
	CC[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
	CC[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CC[31:0] Channel x Compare/Capture Value

These bits contain the compare/capture value in 32-bit TC mode. In Match frequency (MFRQ) or Match PWM (MPWM) waveform operation (WAVE.WAVEGEN), the CC0 register is used as a period register.

40.7.6.15 Channel x Compare Buffer Value, 32-bit Mode

Name: CCBUFx
Offset: 0x30 + x*0x04 [x=0..1]
Reset: 0x00000000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
	CCBUF[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	CCBUF[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CCBUF[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CCBUF[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – CCBUF[31:0] Channel x Compare Buffer Value
These bits hold the value of the Channel x Compare Buffer Value. When the buffer valid flag is '1' and double buffering is enabled (CTRLBCLR.LUPD=1), the data from buffer registers will be copied into the corresponding CCx register under UPDATE condition (CTRLBSET.CMD=0x3), including the software update command.

41. Timer/Counter for Control Applications (TCC)

41.1 Overview

The device provides three instances of the Timer/Counter for Control Applications (TCC).

Each TCC instance consists of a counter, a prescaler, compare/capture channels and control logic. The counter can be set to count events or clock pulses. The counter together with the compare/capture channels can be configured to timestamp input events, allowing capture of frequency and pulse-width. It can also perform waveform generation, such as frequency generation and pulse-width modulation.

Waveform extensions are featured for motor control, ballast, LED, H-bridge, power converters and other types of power control applications. They allow for low-side and high-side output with optional dead-time insertion. Waveform extensions can also generate a synchronized bit pattern across the waveform output pins. The fault options enable fault protection for safe and deterministic handling, disabling and/or shut-down of external drivers.

Note: The TCC configurations, such as channel numbers and features, may be reduced for some of the TCC instances.

Table 41-1. TCC Specific Configuration

					Extensions					
TCC No.	Counter Size (SIZE)	Host Link (Host_Client_MODE) (0 = NA, 1 = Host, 2 = Client)	Channels (CC_NUM)	Pins WO_NUM (OW_NUM)	Fault 1=YES	Dithering 1=YES	OutMatrix 1=YES (OTMX)	Dead Time Insertion 1=YES (DTI)	Swap 1=YES (SWAP)	Pattern Generation 1=YES (PG)
0	24	1	6	6	1	1	1	1	1	1
1	24	2	6	6	1	1	1	1	1	1
2	16	0	2	2	1	0	1	0	0	0

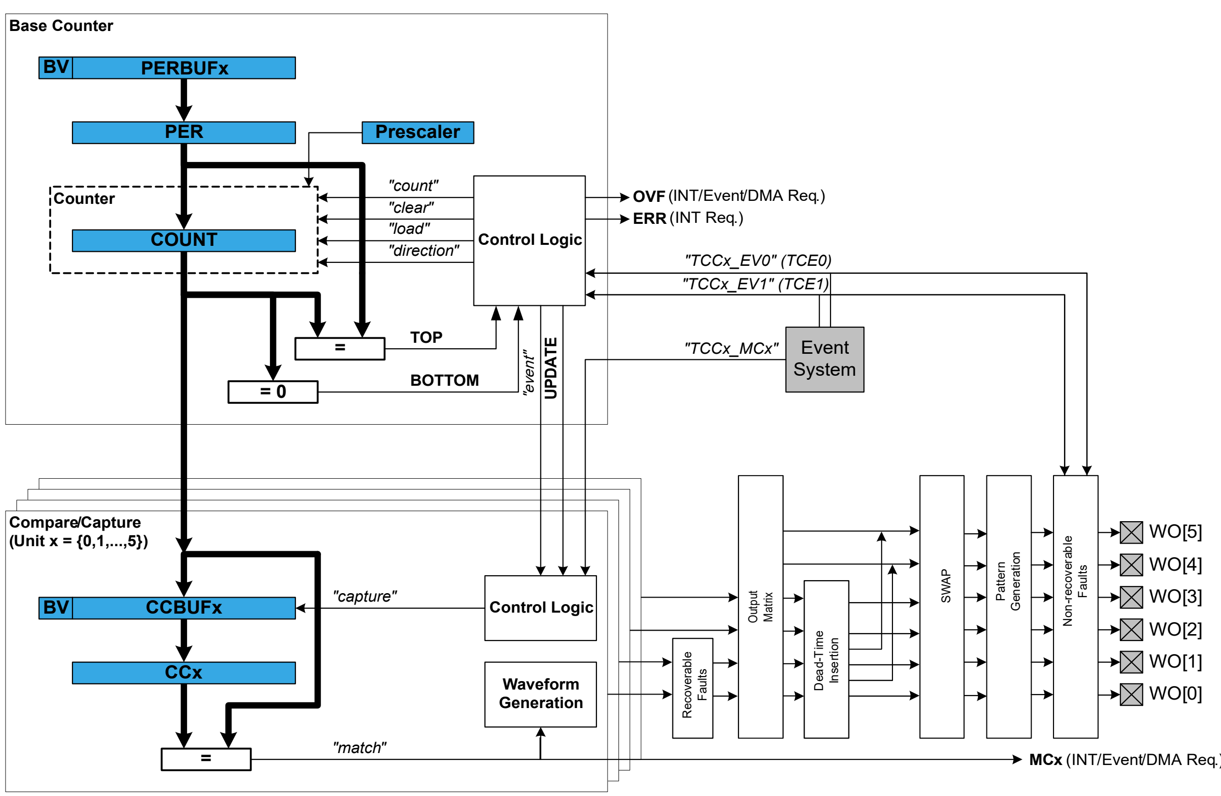
41.2 Features

- Up to six Compare/Capture Channels (CC) with:
  - Double buffered period setting
  - Double buffered compare or capture channel
  - Circular buffer on period and compare channel registers
- Waveform Generation:
  - Frequency generation
  - Single-slope pulse-width modulation (PWM)
  - Dual-slope PWM with half-cycle reload capability
- Input Capture:
  - Event capture
  - Frequency capture
  - Pulse-width capture
- Waveform Extensions:
  - Configurable distribution of compare channels outputs across port pins
  - Low-side and high-side output with programmable dead-time insertion
  - Waveform swap option with double buffer support
  - Pattern generation with double buffer support

- Dithering support
- Fault Protection for Safe Disabling of Drivers:
  - Two recoverable fault sources
  - Two non-recoverable fault sources
  - Debugger can be a source of non-recoverable fault
- Input Events:
  - Two input events (EVx) for counter
  - One input event (MCx) for each channel
- Output Events:
  - Three output events (Count, re-trigger and overflow) are available for counter
  - One compare match/input capture event output for each channel
- Interrupts:
  - Overflow and re-trigger interrupt
  - Compare match/input capture interrupt
  - Interrupt on fault detection

41.3 Block Diagram

Figure 41-1. Timer/Counter for Control Applications - Block Diagram



41.4 Signal Description

Table 41-2. Signal Description

Pin Name	Type	Description
TCCx/WO[0]	Digital output	Compare channel 0 waveform output
TCCx/WO[1]	Digital output	Compare channel 1 waveform output
...	...	...
TCCx/WO[WO_NUM-1]	Digital output	Compare channel n waveform output

See *I/O Ports and Peripheral Pin Select (PPS)* from Related Links for details on the pin mapping for this peripheral. One signal can be mapped on several pins.

Related Links
I/O Ports and Peripheral Pin Select (PPS)

41.5 Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

41.5.1 I/O Lines

In order to use the I/O lines of this peripheral, the I/O pins must be configured using the I/O Peripheral Pin Select (PPS).

41.5.2 Power Management

This peripheral can continue to operate in any Sleep mode where its source clock is running. The interrupts can wake up the device from Sleep modes. Events connected to the event system can trigger other operations in the system without exiting Sleep modes.

41.5.3 Clocks

A generic clock (GCLK_TCCx) is required to clock the TCC. This clock must be configured and enabled in the generic clock controller before using the TCC. Note that TCC1 and TCC2 share a single peripheral clock generator.

The generic clocks (GCLK_TCCx) are asynchronous to the bus clock (PB1_CLK). Due to this asynchronicity, writing certain registers will require synchronization between the clock domains.

41.5.4 DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral, the DMAC must be configured first (see *Direct Memory Access Controller (DMAC)* from Related Links).

Related Links
Direct Memory Access Controller (DMAC)

41.5.5 Interrupts

The interrupt request line is connected to the Interrupt Controller. In order to use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. See *Nested Vector Interrupt Controller (NVIC)* from Related Links.

Related Links
Nested Vector Interrupt Controller (NVIC)

41.5.6 Events

The events of this peripheral are connected to the Event System.

Related Links
Event System (EVSYS)

41.5.7 Debug Operation

When the CPU is halted in Debug mode, this peripheral will halt normal operation. This peripheral can be forced to continue operation during debugging - refer to the Debug Control (DBGCTRL) register for details.

Related Links
DBGCTRL
Debug control

41.5.8 Register Access Protection

Registers with write access can be optionally write-protected by the Peripheral Access Controller (PAC), except for the following:

- Interrupt Flag register (INTFLAG)
- Status register (STATUS)
- Period and Period Buffer registers (PER, PERBUF)
- Compare/Capture and Compare/Capture Buffer registers (CCx, CCBUFx)
- Control Waveform register (WAVE)
- Pattern Generation Value and Pattern Generation Value Buffer registers (PATT, PATTBUF)

Note: Optional write protection is indicated by the "PAC Write Protection" property in the register description.

Write protection does not apply for accesses through an external debugger.

41.5.9 Analog Connections

Not applicable.

41.6 Functional Description

41.6.1 Principle of Operation

The following definitions are used throughout the documentation:

Table 41-3. Timer/Counter for Control Applications – Definitions

Name	Description
TOP	The counter reaches TOP when it becomes equal to the highest value in the count sequence. The TOP value can be the same as Period (PER) or the Compare Channel 0 (CC0) register value depending on the Waveform Generator mode in Waveform Output Operations. See *Waveform Output Generation Operations* from Related Links.
ZERO	The counter reaches ZERO when it contains all zeros.
MAX	The counter reaches maximum when it contains all ones.
UPDATE	The timer/counter signals an update when it reaches ZERO or TOP, depending on the direction settings.
Timer	The timer/counter clock control is handled by an internal source.
Counter	The clock control is handled externally (e.g., counting external events).
CC	For compare operations, the CC are referred to as "compare channels." For capture operations, the CC are referred to as "capture channels."

Each TCC instance has up to six compare/capture channels (CCx).

The Counter register (COUNT), Period registers with Buffer (PER and PERBUF), and Compare and Capture registers with buffers (CCx and CCBUFx) are 16- or 24-bit registers, depending on each TCC instance. Each Buffer register has a Buffer Valid (BUFV) flag that indicates when the buffer contains a new value.

Under normal operation, the counter value is continuously compared to the TOP or ZERO value to determine whether the counter has reached TOP or ZERO. In either case, the TCC can generate interrupt requests or generate events for the Event System. In Waveform Generator mode, these comparisons are used to set the waveform period or pulse width.

A prescaled generic clock (GCLK_TCCx) and events from the event system can be used to control the counter. The event system is also used as a source to the input capture.

The Recoverable Fault Unit enables event-controlled waveforms by acting directly on the generated waveforms of the TCC compare channels output. These events can restart, halt the timer/counter period, shorten the output pulse active time, or disable waveform output as long as the fault condition is present. This can typically be used for current sensing regulation, and zero-crossing and demagnetization re-triggering.

The MCE0 and MCE1 asynchronous event sources are shared with the recoverable fault unit. Only asynchronous events are used internally when fault unit extension is enabled. See *Event System (EVSYS)* from Related Links for further details on how to configure asynchronous events routing.

Recoverable fault sources can be filtered and/or windowed to avoid false triggering, for example from I/O pin glitches, by using digital filtering, input blanking and qualification options. See *Recoverable Faults* from Related Links.

In order to support applications with different types of motor control, ballast, LED, H-bridge, power converter and other types of power switching applications, the following independent units are implemented in some of the TCC instances as optional and successive units:

- Recoverable faults and non-recoverable faults
- Output matrix
- Dead-time insertion
- Swap
- Pattern generation

See *Timer/Counter for Control Applications - Block Diagram* in the *Block Diagram* from Related Links.

The output matrix (OTMX) can distribute and route out the TCC waveform outputs across the port pins in different configurations, each optimized for different application types. The Dead-Time Insertion (DTI) unit splits the four lower OTMX outputs into two non-overlapping signals: the non-inverted Low Side (LS) and inverted High Side (HS) of the waveform output with optional dead-time insertion between LS and HS switching. The SWAP unit can swap the LS and HS pin outputs and can be used for fast decay motor control.

The pattern generation unit can be used to generate synchronized waveforms with constant logic level on TCC UPDATE conditions. This is useful for easy stepper motor and full bridge control.

The non-recoverable fault module enables event-controlled fault protection by acting directly on the generated waveforms of the timer/counter compare channel outputs. When a non-recoverable fault condition is detected, the output waveforms are forced to a preconfigured value that is safe for the application. This is typically used for instant and predictable shut-down and disabling high current or voltage drives.

The count event sources (TCE0 and TCE1) are shared with the non-recoverable fault extension. The events can be optionally filtered. If the filter options are not used, the non-recoverable faults provide an immediate asynchronous action on waveform output, even for cases where the clock is not present. See *Event System (EVSYS)* from Related Links for further details on how to configure asynchronous events routing.

Related Links
Event System (EVSYS)
Waveform Output Operations
Block Diagram
Recoverable Faults

41.6.2 Basic Operation

41.6.2.1 Initialization

The following registers are enable-protected, meaning that they can only be written when the TCC is disabled (CTRLA.ENABLE=0):

- Control A (CTRLA) register, except Run Standby (RUNSTDBY), Enable (ENABLE) and Software Reset (SWRST) bits
- Recoverable Fault n Control registers (FCTRLA and FCTRLB)
- Waveform Extension Control register (WEXCTRL)
- Drive Control register (DRVCTRL)
- Event Control register (EVCTRL)

Enable-protected bits in the CTRLA register can be written at the same time as CTRLA.ENABLE is written to '1', but not at the same time as CTRLA.ENABLE is written to '0'. Enable-protection is denoted by the "Enable-Protected" property in the register description.

Before the TCC is enabled, it must be configured as outlined by the following steps:

1. Enable the TCC bus clock if not already enabled by default (PB1_CLK).
2. If Capture mode is required, enable the channel in Capture mode by writing a '1' to the Capture Enable bit in the Control A register (CTRLA.CPTEN).

Optionally, the following configurations can be set before enabling TCC:

1. Select PRESCALER setting in the Control A register (CTRLA.PRESCALER).
2. Select Prescaler Synchronization setting in Control A register (CTRLA.PRESCSYNC).
3. If down-counting operation is desired, write the Counter Direction bit in the Control B Set register (CTRLBSET.DIR) to '1'.
4. Select the Waveform Generation operation in the WAVE register (WAVE.WAVEGEN).
5. Select the Waveform Output Polarity in the WAVE register (WAVE.POL).
6. The waveform output can be inverted for the individual channels using the Waveform Output Invert Enable bit group in the Driver register (DRVCTRL.INVEN).

41.6.2.2 Enabling, Disabling, and Resetting

The TCC is enabled by writing a '1' to the Enable bit in the Control A register (CTRLA.ENABLE). The TCC is disabled by writing a zero to CTRLA.ENABLE.

The TCC is reset by writing '1' to the Software Reset bit in the Control A register (CTRLA.SWRST). All registers in the TCC, except DBGCTRL, will be reset to their initial state, and the TCC will be disabled.

The TCC must be disabled before the TCC is reset to avoid undefined behavior.

41.6.2.3 Prescaler Selection

The GCLK_TCCx clock is fed into the internal prescaler.

The prescaler consists of a counter that counts up to the selected prescaler value, whereupon the output of the prescaler toggles.

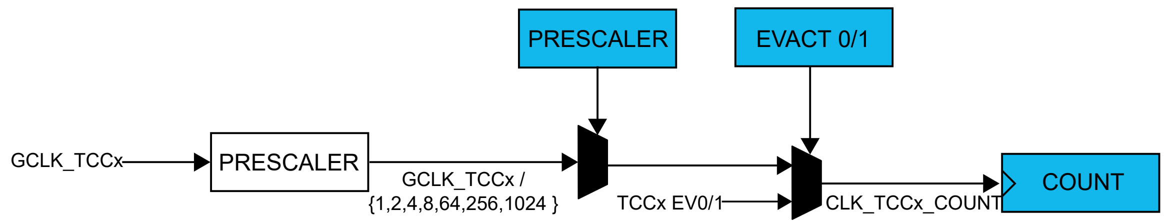
If the prescaler value is higher than one, the Counter Update condition can be optionally executed on the next GCLK_TCCx clock pulse or the next prescaled clock pulse. For further details, refer to the Prescaler (CTRLA.PRESCALER) and Counter Synchronization (CTRLA.PRESYNC) descriptions.

Prescaler outputs from 1 to 1/1024 are available. For a complete list of available prescaler outputs, see the register description for the Prescaler bit group in the Control A register (CTRLA.PRESCALER).

Note: When counting events, the prescaler is bypassed.

The joint stream of prescaler ticks and event action ticks is called CLK_TCCx_COUNT.

Figure 41-2. Prescaler



41.6.2.4 Counter Operation

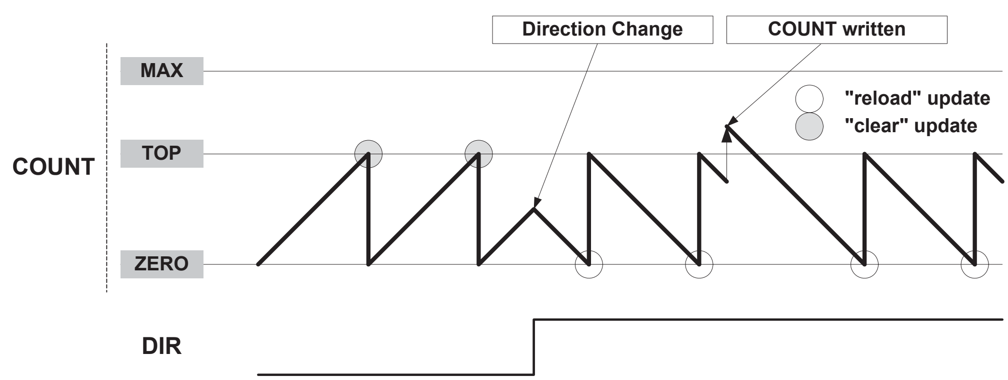
Depending on the mode of operation, the counter is cleared, reloaded, incremented, or decremented at each TCC clock input (CLK_TCCx_COUNT). A counter clear or reload mark the end of current counter cycle and the start of a new one.

The counting direction is set by the Direction bit in the Control B register (CTRLB.DIR). If the bit is zero, it's counting up and one if counting down.

The counter will count up or down for each tick (clock or event) until it reaches TOP or ZERO. When it's counting up and TOP is reached, the counter will be set to zero at the next tick (overflow) and the Overflow Interrupt Flag in the Interrupt Flag Status and Clear register (INTFLAG.OVF) will be set. When down-counting, the counter is reloaded with the TOP value when ZERO is reached (underflow), and INTFLAG.OVF is set.

INTFLAG.OVF can be used to trigger an interrupt, or an event. An overflow/underflow occurrence (i.e. a compare match with TOP/ZERO) will stop counting if the One-Shot bit in the Control B register is set (CTRLBSET.ONESHOT). The One-Shot feature is explained in the Additional Features section.

Figure 41-3. Counter Operation



It is possible to change the counter value (by writing directly in the COUNT register) even when the counter is running. The COUNT value will always be ZERO or TOP, depending on direction set by CTRLBSET.DIR or CTRLBCLR.DIR, when starting the TCC, unless a different value has been written to it, or the TCC has been stopped at a value other than ZERO. The write access has higher priority than count, clear, or reload. The direction of the counter can also be changed during normal operation. See also Figure 41-3.

Stop Command

A stop command can be issued from software by using TCC Command bits in Control B Set register (CTRLBSET.CMD=0x2, STOP).

When a stop is detected while the counter is running, the counter will maintain its current value. If the waveform generation (WG) is used, all waveforms are set to a state defined in Non-Recoverable State x Output Enable bit and Non- Recoverable State x Output Value bit in the Driver Control register (DRVCTRL.NREx and DRVCTRL.NRVx), and the Stop bit in the Status register is set (STATUS.STOP).

Pause Event Action

A pause command can be issued when the stop event action is configured in the Input Event Action 1 bits in Event Control register (EVCTRL.EVACT1=0x3, STOP).

When a pause is detected, the counter can stop immediatly maintaining its current value and all waveforms keep their current state, as long as a start event action is detected: Input Event Action 0 bits in Event Control register (EVCTRL.EVACT0=0x3, START).

Re-Trigger Command and Event Action

A re-trigger command can be issued from software by using TCC Command bits in Control B Set register (CTRLBSET.CMD=0x1, RETRIGGER), or from event when the re-trigger event action is configured in the Input Event 0/1 Action bits in Event Control register (EVCTRL.EVACTn=0x1, RETRIGGER).

When the command is detected during counting operation, the counter will be reloaded or cleared, depending on the counting direction (CTRLBSET.DIR or CTRLBCLR.DIR). The Re-Trigger bit in the Interrupt Flag Status and Clear register will be set (INTFLAG.TRG). It is also possible to generate an event by writing a '1' to the Re-Trigger Event Output Enable bit in the Event Control register (EVCTRL.TRGEO). If the re-trigger command is detected when the counter is stopped, the counter will resume counting operation from the value in COUNT.

Note:
When a re-trigger event action is configured in the Event Action bits in the Event Control register (EVCTRL.EVACTn=0x1, RETRIGGER), enabling the counter will not start the counter. The counter will start on the next incoming event and restart on corresponding following event.

Start Event Action

The start action can be selected in the Event Control register (EVCTRL.EVACT0=0x3, START) and can start the counting operation when previously stopped. The event has no effect if the counter is already counting. When the module is enabled, the counter operation starts when the event is received or when a re-trigger software command is applied.

Note:
When a start event action is configured in the Event Action bits in the Event Control register (EVCTRL.EVACT0=0x3, START), enabling the counter will not start the counter. The counter will start on the next incoming event, but it will not restart on subsequent events.

Count Event Action

The TCC can count events. When an event is received, the counter increases or decreases the value, depending on direction settings (CTRLBSET.DIR or CTRLBCLR.DIR).

The count event action is selected by the Event Action 0 bit group in the Event Control register (EVCTRL.EVACT0=0x5, COUNT).

Direction Event Action

The direction event action can be selected in the Event Control register (EVCTRL.EVACT1=0x2, DIR). When this event is used, the asynchronous event path specified in the event system must be configured or selected. The direction event action can be used to control the direction of the counter operation, depending on external events level. When received, the event level overrides the Direction settings (CTRLBSET.DIR or CTRLBCLR.DIR) and the direction bit value is updated accordingly.

Increment Event Action

The increment event action can be selected in the Event Control register (EVCTRL.EVACT0=0x4, INC) and can change the Counter state when an event is received. When the TCE0 event (TCCx_EV0) is received, the counter increments, whatever the direction setting (CTRLBSET.DIR or CTRLBCLR.DIR) is.

Decrement Event Action

The decrement event action can be selected in the Event Control register (EVCTRL.EVACT1=0x4, DEC) and can change the Counter state when an event is received. When the TCE1 (TCCx_EV1) event is received, the counter decrements, whatever the direction setting (CTRLBSET.DIR or CTRLBCLR.DIR) is.

Non-recoverable Fault Event Action

Non-recoverable fault actions can be selected in the Event Control register (EVCTRL.EVACTn=0x7, FAULT). When received, the counter will be stopped and the output of the compare channels is overridden according to the Driver Control register settings (DRVCTRL.NREx and DRVCTRL.NRVx). TCE0 and TCE1 must be configured as asynchronous events.

Event Action Off

If the event action is disabled (EVCTRL.EVACTn=0x0, OFF), enabling the counter will also start the counter.

Related Links
One-Shot Operation

41.6.2.5 Compare Operations

By default, the Compare/Capture channel is configured for compare operations. To perform capture operations, it must be re-configured.

When using the TCC with the Compare/Capture Value registers (CCx) for compare operations, the counter value is continuously compared to the values in the CCx registers. This can be used for timer or for waveform operation.

The Channel x Compare/Capture Buffer Value (CCBUFx) registers provide double buffer capability. The double buffering synchronizes the update of the CCx register with the buffer value at the UPDATE condition or a force update command (CTRLBSET.CMD=0x3, UPDATE). See *Double Buffering* from Related Links. The synchronization prevents the occurrence of odd-length, non-symmetrical pulses and ensures glitch-free output.

Related Links
Double Buffering

41.6.2.5.1 Waveform Output Generation Operations

The compare channels can be used for waveform generation on output port pins. To make the waveform available on the connected pin, the following requirements must be fulfilled:

1. Choose a Waveform Generation mode in the Waveform Generation Operation bit in the Waveform register (WAVE.WAVEGEN).
2. Optionally, invert the waveform output WO[x] by writing the corresponding Waveform Output x Inversion bit in the Driver Control register (DRVCTRL.INVENx).

3. Configure the pins with the I/O Pin Controller. See *I/O Ports and Peripheral Pin Select (PPS)* from Related Links.
   Note: The event must not be used when the compare channel is set in Waveform Output Operating mode.

The counter value is continuously compared with each CCx value. On a comparison match, the Match or Capture Channel x bit in the Interrupt Flag Status and Clear register (INTFLAG.MCx) will be set on the next zero-to-one transition of CLK_TCC_COUNT (see Normal Frequency Operation). An interrupt and/or event can be generated on the same condition if Match/Capture occurs, i.e., INTENSET.MCx and/or EVCTRL.MCEOx is '1'. Both the interrupt and event can be generated simultaneously. The user needs to clear INTFLAG.MCx at the beginning of the interrupt routine and poll the bit until INTFLAG.MCx is cleared before exiting the ISR.

There are seven waveform configurations for the Waveform Generation Operation bit group in the Waveform register (WAVE.WAVEGEN). This will influence how the waveform is generated and impose restrictions on the top value. The configurations are:

- Normal Frequency (NFRQ)
- Match Frequency (MFRQ)
- Normal Pulse-Width Modulation (NPWM)
- Dual-slope, interrupt/event at TOP (DSTOP)
- Dual-slope, interrupt/event at ZERO (DSBOTTOM)
- Dual-slope, interrupt/event at Top and ZERO (DSBOTH)
- Dual-slope, critical interrupt/event at ZERO (DSCRITICAL)

When using MFRQ configuration, the TOP value is defined by the CC0 register value. For the other waveform operations, the TOP value is defined by the Period (PER) register value.

For dual-slope waveform operations, the update time occurs when the counter reaches ZERO. For the other Waveforms Generation modes, the update time occurs on counter wraparound, on overflow, underflow or re-trigger.

The table below shows the update counter and overflow event/interrupt generation conditions in different operation modes.

Table 41-4. Counter Update and Overflow Event/interrupt Conditions

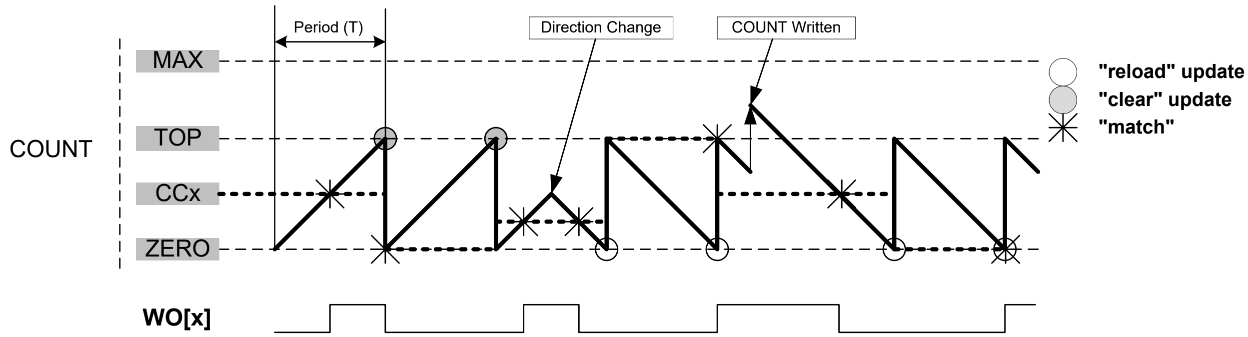
Name	Operation	TOP	Update	Output Waveform		OVFIF/Event	
				On Match	On Update	Up	Down
NFRQ	Normal Frequency	PER	TOP/ ZERO	Toggle	Stable	TOP	ZERO
MFRQ	Match Frequency	CC0	TOP/ ZERO	Toggle	Stable	TOP	ZERO
NPWM	Single-slope PWM	PER	TOP/ ZERO	See section 'Output Polarity' below		TOP	ZERO
DSCRITICAL	Dual-slope PWM	PER	ZERO			—	ZERO
DSBOTTOM	Dual-slope PWM	PER	ZERO			—	ZERO
DSBOTH	Dual-slope PWM	PER	TOP[(1)] & ZERO			TOP	ZERO
DSTOP	Dual-slope PWM	PER	ZERO			TOP	—

1. The UPDATE condition on TOP only will occur when the circular buffer is enabled for the channel.

41.6.2.5.2 Normal Frequency (NFRQ)

For Normal Frequency generation, the period time (T) is controlled by the period register (PER). The waveform generation output (WO[x]) is toggled on each compare match between COUNT and CCx, and the corresponding Match or Capture Channel x Interrupt Flag (EVCTRL.MCEOx) will be set.

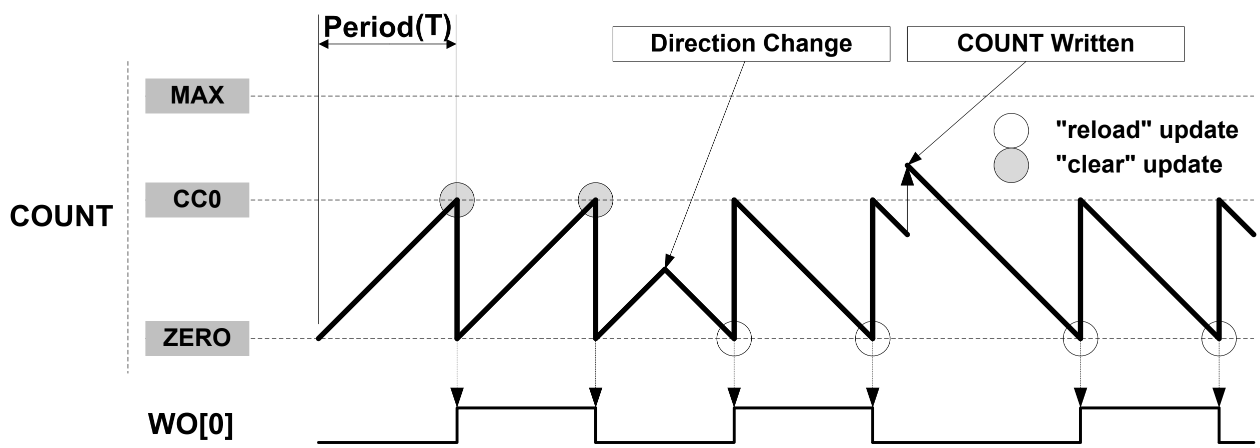
Figure 41-4. Normal Frequency Operation



41.6.2.5.3 Match Frequency (MFRQ)

For Match Frequency generation, the period time (T) is controlled by CC0 register instead of PER. WO[0] toggles on each update condition.

Figure 41-5. Match Frequency Operation



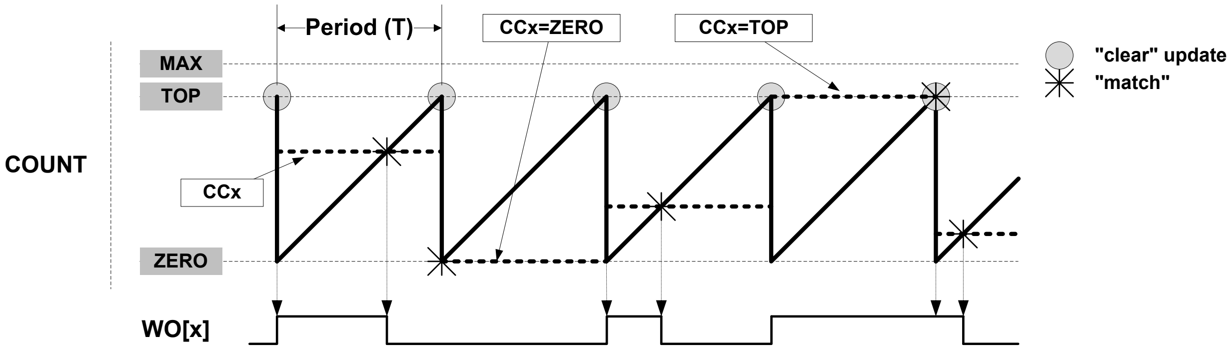
41.6.2.5.4 Normal Pulse-Width Modulation (NPWM)

NPWM uses single-slope PWM generation.

41.6.2.5.5 Single-Slope PWM Operation

For single-slope PWM generation, the period time (T) is controlled by Top value, and CCx controls the duty cycle of the generated waveform output. When up-counting, the WO[x] is set at start or compare match between the COUNT and TOP values, and cleared on compare match between COUNT and CCx register values. When down-counting, the WO[x] is cleared at start or compare match between the COUNT and ZERO values, and set on compare match between COUNT and CCx register values.

Figure 41-6. Single-Slope PWM Operation



The following equation calculates the exact resolution for a single-slope PWM (R_{PWM_SS}) waveform:

$$R_{PWM\_SS} = \frac{\log(TOP+1)}{\log(2)}$$

The PWM frequency depends on the Period register value (PER) and the peripheral clock frequency (f_{GCLK_TCCx}), and can be calculated by the following equation:

$$f_{PWM\_SS} = \frac{f_{GCLK\_TCCx}}{N(TOP+1)}$$

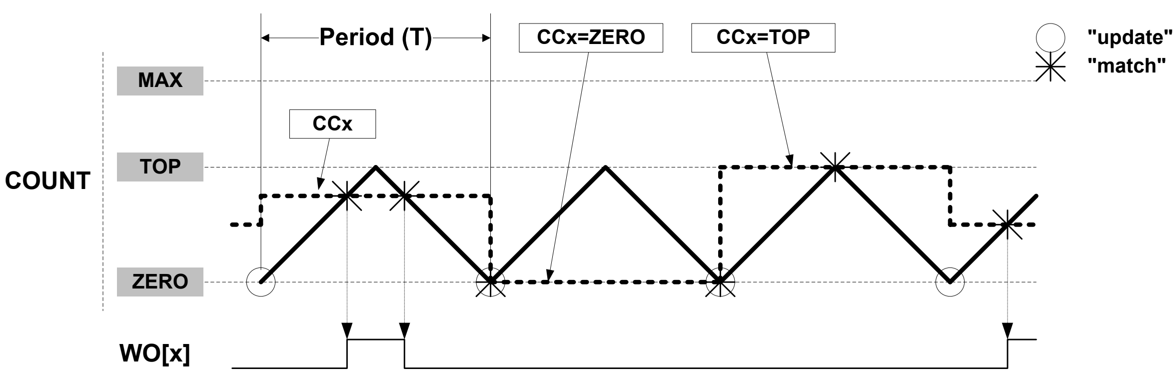
Where N represents the prescaler divider used (1, 2, 4, 8, 16, 64, 256, 1024).

41.6.2.5.6 Dual-Slope PWM Generation

For dual-slope PWM generation, the period setting (TOP) is controlled by PER, while CCx control the duty cycle of the generated waveform output. The figure below shows how the counter repeatedly counts from ZERO to PER and then from PER to ZERO. The waveform generator output is set on compare match when up-counting, and cleared on compare match when down-counting. An interrupt and/or event is generated on TOP (when counting upwards) and/or ZERO (when counting up or down).

In DSBOTH operation, the circular buffer must be enabled to enable the update condition on TOP.

Figure 41-7. Dual-Slope Pulse Width Modulation



Using dual-slope PWM results in a lower maximum operation frequency compared to single-slope PWM generation. The period (TOP) defines the PWM resolution. The minimum resolution is 1 bit (TOP=0x00000001).

The following equation calculates the exact resolution for dual-slope PWM (R_{PWM_DS}):

$$R_{PWM\_DS} = \frac{\log(PER+1)}{\log(2)}.$$

The PWM frequency f_{PWM_DS} depends on the period setting (TOP) and the peripheral clock frequency f_{GCLK_TCCx}, and can be calculated by the following equation:

$$f_{PWM\_DS} = \frac{f_{GCLK\_TCCx}}{2N \cdot PER}$$

N represents the prescaler divider used. The waveform generated will have a maximum frequency of half of the TCC clock frequency (f_{GCLK_TCCx}) when TOP is set to 0x00000001 and no prescaling is used.

The pulse width (P_{PWM_DS}) depends on the compare channel (CCx) register value and the peripheral clock frequency (f_{GCLK_TCCx}), and can be calculated by the following equation:

$$P_{PWM\_DS} = \frac{2N \cdot (TOP - CCx)}{f_{GCLK\_TCCx}}$$

N represents the prescaler divider used.

Note: In DSTOP, DSBOTTOM and DSBOTH operation, when TOP is lower than MAX/2, the CCx MSB bit defines the ramp on which the CCx Match interrupt or event is generated. (Rising if CCx[MSB] = 0, falling if CCx[MSB] = 1.)

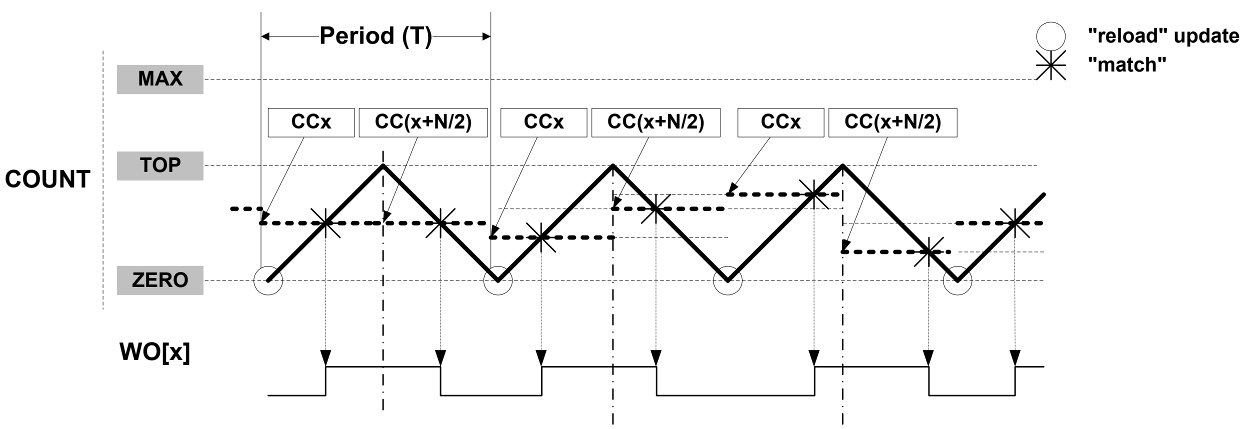
Related Links

Circular Buffer

41.6.2.5.7 Dual-Slope Critical PWM Generation

Critical mode generation allows generation of non-aligned centered pulses. In this mode, the period time is controlled by PER while CCx control the generated waveform output edge during up-counting and CC(x+CC_NUM/2) control the generated waveform output edge during down-counting.

Figure 41-8. Dual-Slope Critical Pulse Width Modulation (N=CC_NUM)



41.6.2.5.8 Output Polarity

The polarity (WAVE.POLx) is available in all waveform output generation. In single-slope and dual-slope PWM operation, it is possible to invert the pulse edge alignment individually on start or end of a PWM cycle for each compare channels. The table below shows the waveform output set/clear conditions, depending on the settings of timer/counter, direction, and polarity.

Table 41-5. Waveform Generation Set/Clear Conditions

Waveform Generation Operation	DIR	POLx	Waveform Generation Output Update	
			Set	Clear
Single-Slope PWM	0	0	Timer/counter matches TOP	Timer/counter matches CCx
		1	Timer/counter matches CC	Timer/counter matches TOP
	1	0	Timer/counter matches CC	Timer/counter matches ZERO
		1	Timer/counter matches ZERO	Timer/counter matches CC
Dual-Slope PWM	x	0	Timer/counter matches CC when counting up	Timer/counter matches CC when counting down
		1	Timer/counter matches CC when counting down	Timer/counter matches CC when counting up

In Normal and Match Frequency, the WAVE.POLx value represents the initial state of the waveform output.

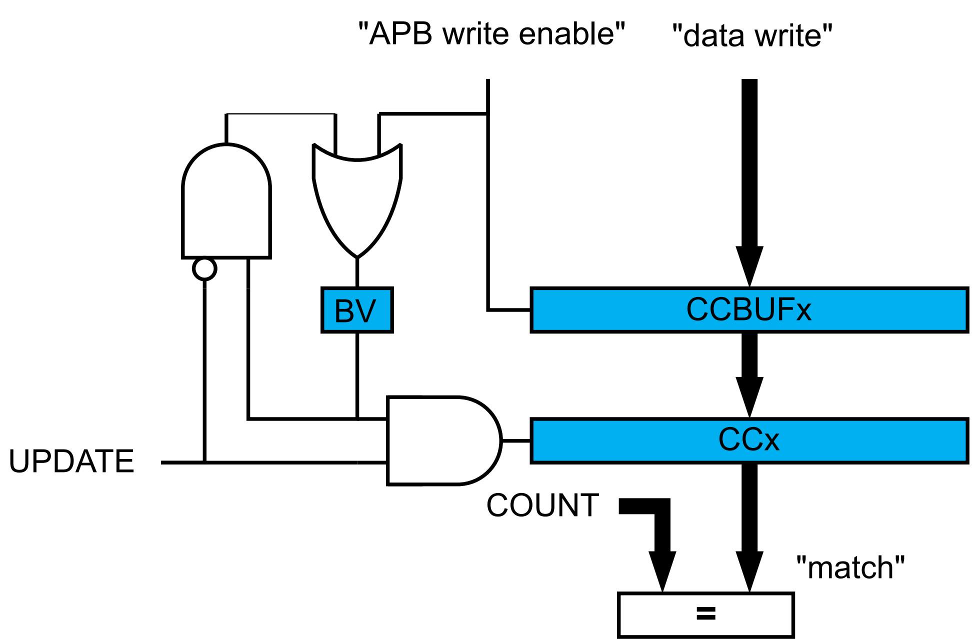
41.6.2.6 Double Buffering

The Pattern (PATT), Period (PER) and Compare Channels (CCx) registers are all double buffered. Each buffer register has a buffer valid (PATTBUFV, PERBUFV and CCBUFVx) bit in the STATUS register that indicates that the Buffer register contains a valid value that can be copied into the corresponding register. As long as the respective Buffer Valid Status flags (PATTBUFV, PERBUFV or CCBUFVx) are set to '1', the related SYNCBUSY bits are set (SYNCBUSY.PATT, SYNCBUSY.PER or SYNCBUSY.CCx), a write to the respective PATT/PATTBUF, PER/PERBUF or CCx/CCBUFx registers will generate a PAC error, and read access to the respective PATT, PER or CCx register is invalid.

When the Buffer Valid Flag bit in the STATUS register is '1' and the Lock Update bit in the CTRLB register is set to '0' (writing CTRLBCLR.LUPD to '1'), double buffering is enabled: the data from the buffer registers will be copied into the corresponding register under the hardware UPDATE conditions, then the Buffer Valid flags bit in the STATUS register is automatically cleared by the hardware.
Note: The software update command (CTRLBSET.CMD=0x3) acts independently of the LUPD value.

A compare register is double buffered as in the following figure.

Figure 41-9. Compare Channel Double Buffering



Both the registers (PATT/PER/CCx) and corresponding Buffer registers (PATTBUFPERBUF/CCBUFx) are available in the I/O register map, and the double buffering feature is not mandatory. The double buffering is disabled by writing a '1' to CTRLSET.LUPD.

Note: In NFRQ, MFRQ or PWM Down-Counting Counter mode (CTRLBSET.DIR=1), when double buffering is enabled (CTRLBCLR.LUPD=1), the PERBUF register is continuously copied into the PER independently of the update conditions.

Changing the Period

The counter period can be changed by writing a new Top value to the Period register (PER or CC0, depending on the Waveform Generation mode). Any period update on the registers (PER or CCx) is effective after the synchronization delay, whatever double buffering enabling is.

Figure 41-10. Unbuffered Single-Slope Up-Counting Operation

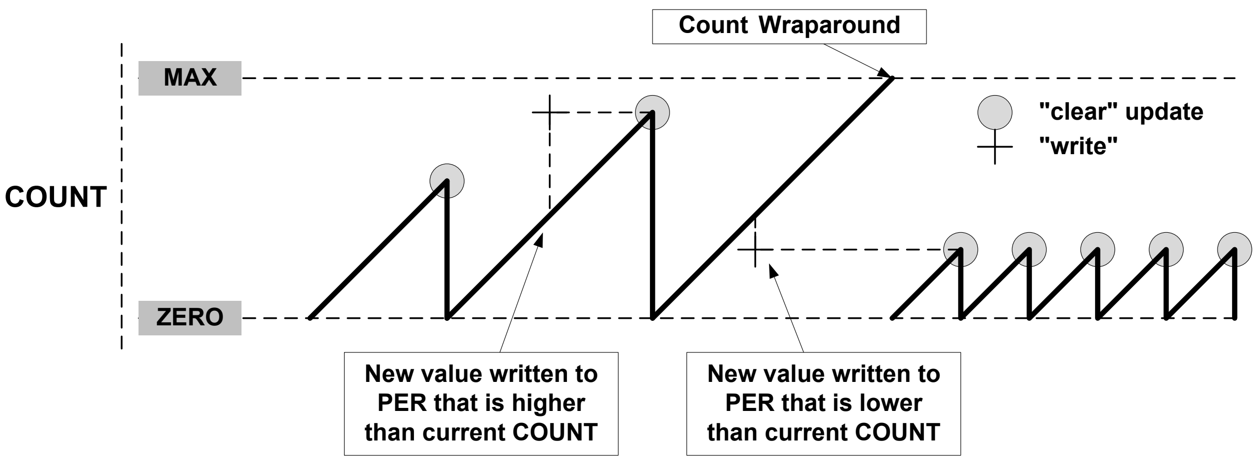
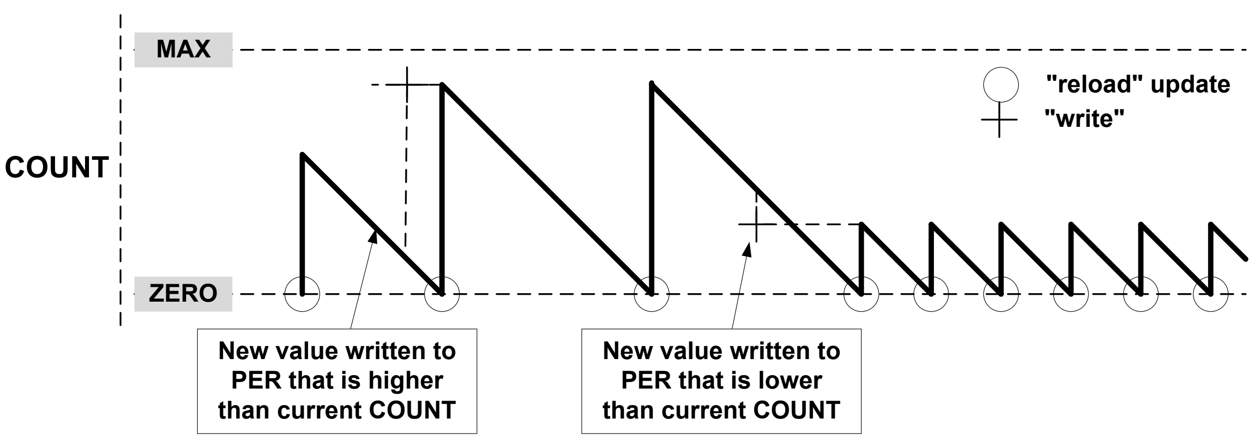
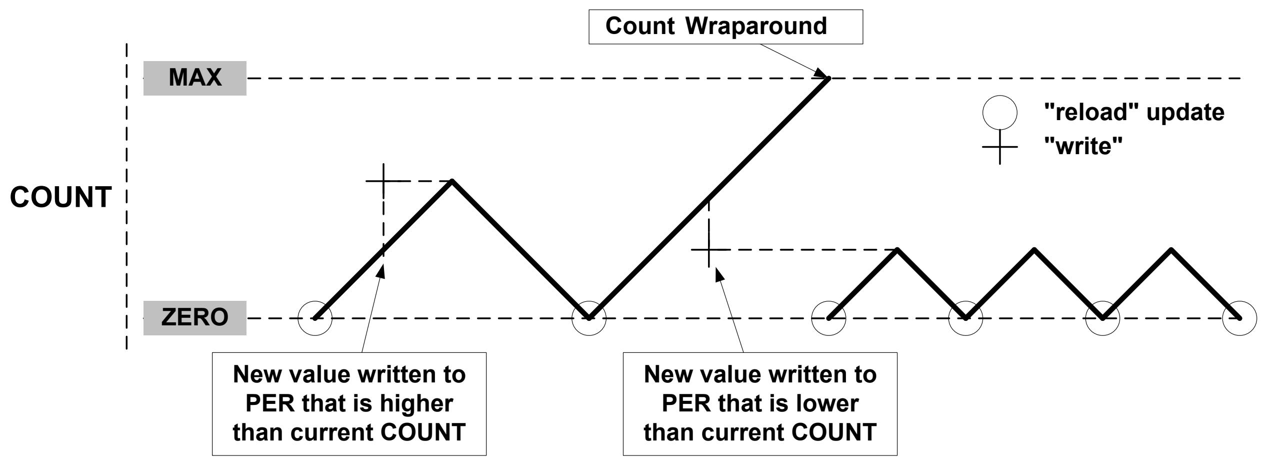


Figure 41-11. Unbuffered Single-Slope Down-Counting Operation



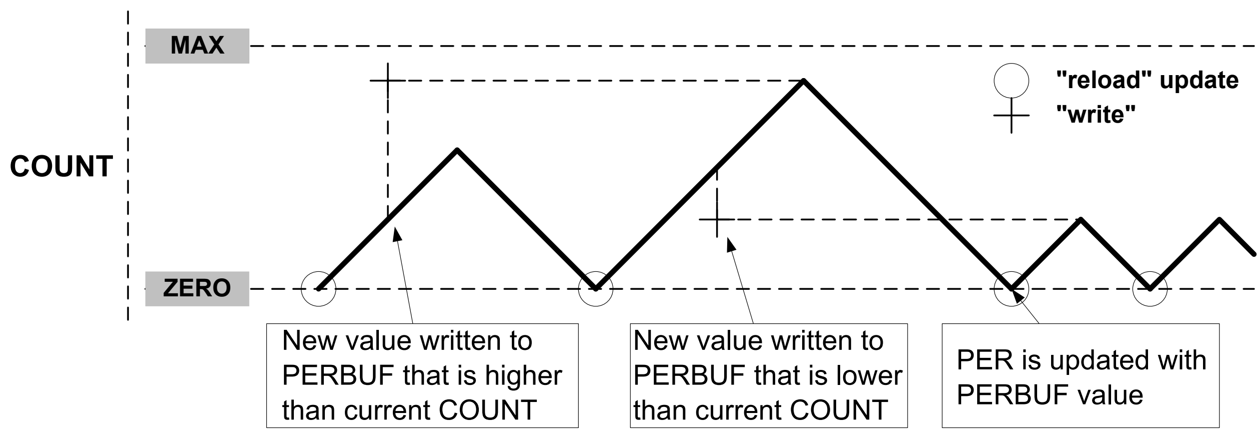
A counter wraparound can occur in any operation mode when up-counting without buffering (see Figure 41-10). COUNT and TOP are continuously compared, so when a new value that is lower than the current COUNT is written to TOP, COUNT will wrap before a compare match.

Figure 41-12. Unbuffered Dual-Slope Operation



When double buffering is used, the buffer can be written at any time and the counter will still maintain correct operation. The period register is always updated on the update condition, as shown in Figure 41-13. This prevents wraparound and the generation of odd waveforms.

Figure 41-13. Changing the Period Using Buffering



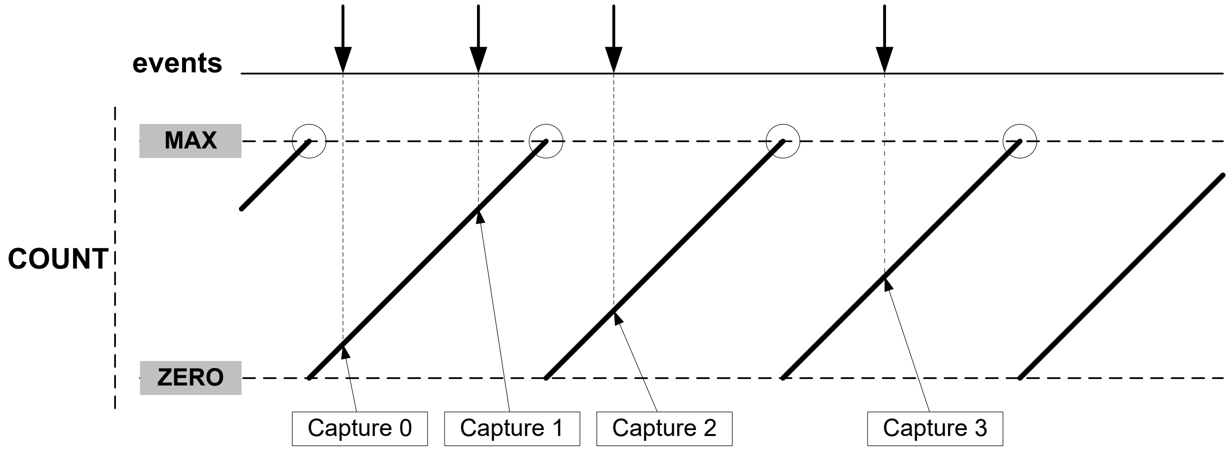
41.6.2.7 Capture Operations

To enable and use capture operations, the Match or Capture Channel x Event Input Enable bit in the Event Control register (EVCTRL.MCEIx) must be written to '1'. The capture channels to be used must also be enabled in the Capture Channel x Enable bit in the Control A register (CTRLA.CPTENx) before capturing can be performed.

Event Capture Action

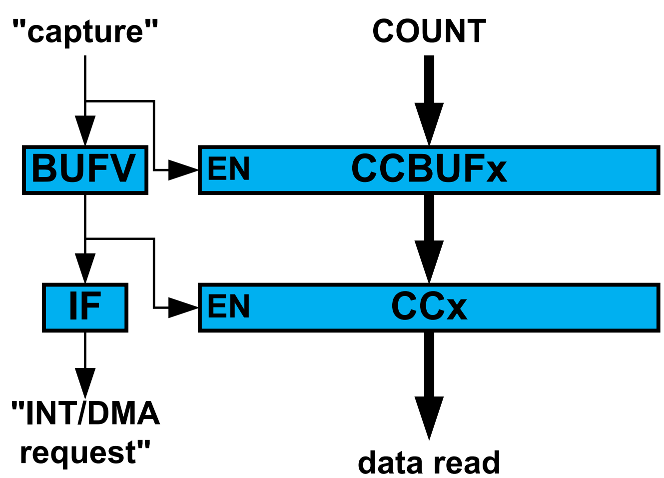
The compare/capture channels can be used as input capture channels to capture events from the Event System and give them a timestamp. The following figure shows four capture events for one capture channel. Event system channels must be configured to operate in asynchronous mode when used for capture operations.

Figure 41-14. Input Capture Timing



For input capture, the Buffer register and the corresponding CCx act like a FIFO. When CCx is empty or read, any content in CCBUFx is transferred to CCx. The Buffer Valid flag is passed to set the CCx Interrupt flag (IF) and generate the optional interrupt, event or DMA request. The CCBUFx register value cannot be read; all captured data must be read from the CCx register.

Figure 41-15. Capture Double Buffering



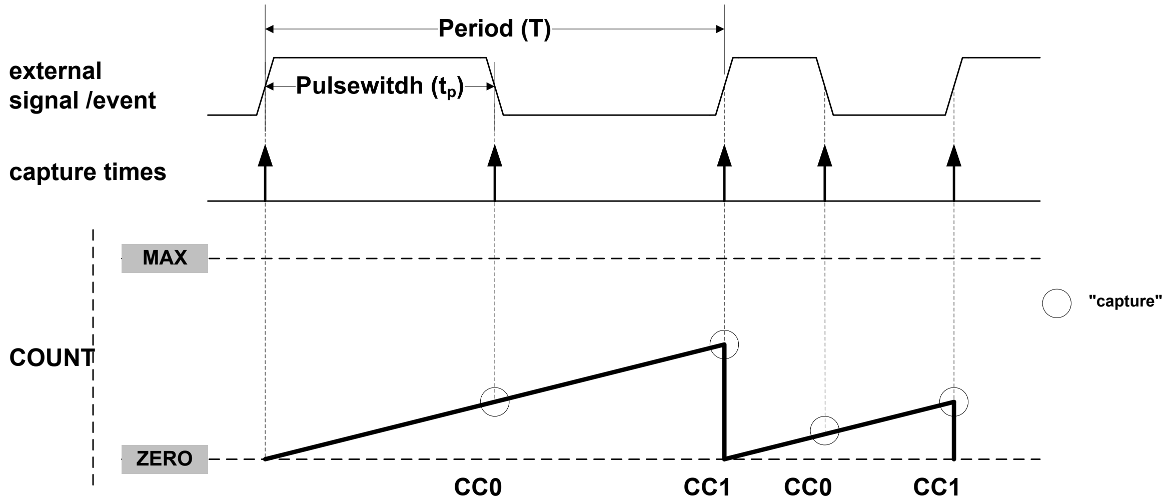
The TCC can detect capture overflow of the input capture channels. When a new capture event is detected while the Capture Buffer Valid flag (STATUS.CCBUFV) is still set, the new timestamp will not be stored and INTFLAG.ERR will be set.

Period and Pulse-Width (PPW) Capture Action

The TCC can perform two input captures and restart the counter on one of the edges. This enables the TCC to measure the pulse-width and period and to characterize the frequency f and *dutyCycle* of an input signal, as shown below:

$$f = \frac{1}{T} \quad , \quad dutyCycle = \frac{t_p}{T}$$

Figure 41-16. PWP Capture



Selecting PWP or PPW in the Timer/Counter Event Input 1 Action bit group in the Event Control register (EVCTRL.EVACT1) enables the TCC to perform one capture action on the rising edge and the other one on the falling edge. When using PPW event action, period T will be captured into CC0 and the pulse-width t_p into CC1. The PWP (Pulse-width and Period) event action offers the same functionality but T will be captured into CC1 and t_p into CC0.

The Timer/Counter Event x Invert Enable bit in Event Control register (EVCTRL.TCEINVx) is used for event source x to select whether the wraparound must occur on the rising edge or the falling edge. If EVCTRL.TCEINVx=`1`, the wraparound will happen on the falling edge.

The corresponding capture is done only if the channel is enabled in Capture mode (CTRLA.CPTENx=`1`). If not, the capture action will be ignored and the channel will be enabled in the Compare mode of the operation. When only one of these channels is required, the other channel can be used for other purposes.

The TCC can detect capture overflow of the input capture channels. When a new capture event is detected while the INTFLAG.MCx is still set, the new timestamp will not be stored and INTFLAG.ERR will be set. The user needs to clear INTFLAG.MCx at the beginning of the interrupt routine and poll the bit until INTFLAG.MCx is cleared before exiting the ISR.

Note: When up-counting (CTRLBSET.DIR=`0`), counter values lower than 1 cannot be captured in the Capture Minimum mode (FCTRLn.CAPTURE=CAPTMIN). To capture the full range including value 0, the TCC must be configured in Down-counting mode (CTRLBSET.DIR=`0`).

Note: In dual-slope PWM operation and when TOP is lower than MAX/2, the CCx MSB captures the CTRLB.DIR state to identify the ramp where the capture was done. For rising ramps, CCx[MSB] is zero; for falling ramps, CCx[MSB]=`1`.

41.6.3 Additional Features

41.6.3.1 One-Shot Operation

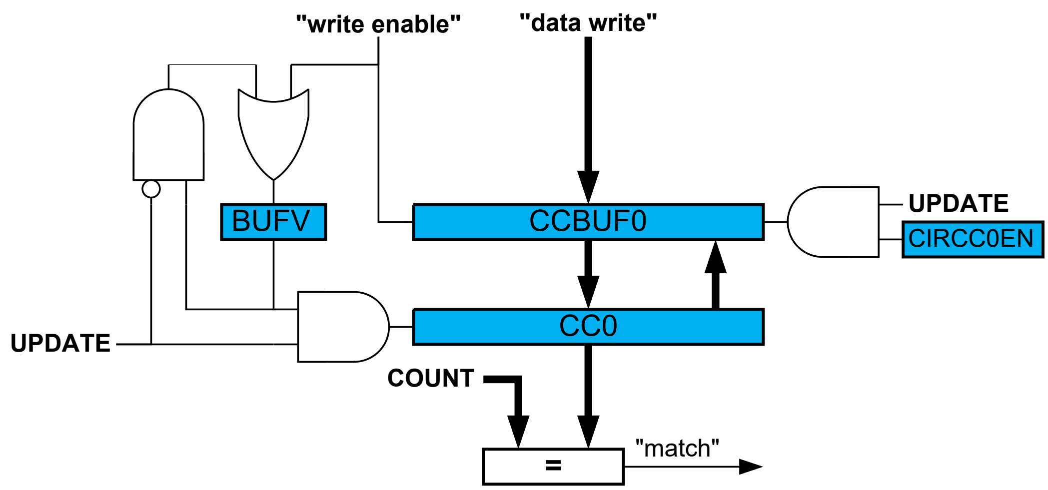
When one-shot is enabled, the counter automatically stops on the next Counter Overflow or Underflow condition. When the counter is stopped, the Stop bit in the Status register (STATUS.STOP) is set and the waveform outputs are set to the value defined by DRVCTRL.NREx and DRVCTRL.NRVx.

One-shot operation can be enabled by writing a '1' to the One-Shot bit in the Control B Set register (CTRLBSET.ONESHOT) and disabled by writing a '1' to CTRLBCLR.ONESHOT. When enabled, the TCC will count until an overflow or underflow occurs and stop counting. The one-shot operation can be restarted by a re-trigger software command, a re-trigger event or a start event. When the counter restarts its operation, STATUS.STOP is automatically cleared.

41.6.3.2 Circular Buffer

The Period register (PER) and the Compare Channels register (CC0 toCC5) support circular buffer operation. When circular buffer operation is enabled, the PER or CCx values are copied into the corresponding buffer registers at each update condition. Circular buffering is dedicated to RAMP2, RAMP2A, and DSBOTH operations.

Figure 41-17. Circular Buffer on Channel 0



41.6.3.3 Dithering Operation

The TCC supports dithering on Pulse-width or Period on a 16, 32 or 64 PWM cycles frame.

Dithering consists in adding some extra clocks cycles in a frame of several PWM cycles, and can improve the accuracy of the *average* output pulse width and period. The extra clock cycles are added on some of the compare match signals, one at a time, through a "blue noise" process that minimizes the flickering on the resulting dither patterns.

Dithering is enabled by writing the corresponding configuration in the Enhanced Resolution bits in CTRLA register (CTRLA.RESOLUTION):

- DITH4 enable dithering every 16 PWM frames
- DITH5 enable dithering every 32 PWM frames
- DITH6 enable dithering every 64 PWM frames

The DITHERCY bits of COUNT, PER and CCx define the number of extra cycles to add into the frame (DITHERCY bits from the respective COUNT, PER or CCx registers). The remaining bits of COUNT, PER, CCx define the compare value itself.

The pseudo code, giving the extra cycles insertion regarding the cycle is:

```
int extra_cycle(resolution, dithercy, cycle){
  int MASK;
  int value
  switch (resolution){
    DITH4: MASK = 0x0f;
    DITH5: MASK = 0x1f;
    DITH6: MASK = 0x3f;
  }
  value = cycle * dithercy;
  if (((MASK & value) + dithercy) > MASK)
    return 1;
 return 0;
}
```

Dithering on Period

Writing DITHERCY in PER will lead to an average PWM period configured by the following formulas.

DITH4 mode:

$$PwmPeriod = \left(\frac{\text{DITHERCY}}{16} + \text{PER}\right)\left(\frac{1}{f_{\text{GCLK\_TCC}x}}\right)$$

Note: If DITH4 mode is enabled, the last 4 significant bits from PER/CCx or COUNT register correspond to the DITHERCY value, rest of the bits corresponds to PER/CCx or COUNT value.

DITH5 mode:

$$PwmPeriod = \left(\frac{\text{DITHERCY}}{32} + \text{PER}\right)\left(\frac{1}{f_{\text{GCLK\_TCC}x}}\right)$$

DITH6 mode:

$$PwmPeriod = \left(\frac{\text{DITHERCY}}{64} + \text{PER}\right)\left(\frac{1}{f_{\text{GCLK\_TCC}x}}\right)$$

Dithering on Pulse-Width

Writing DITHERCY in CCx will lead to an average PWM pulse width configured by the following formula.

DITH4 mode:

$$PwmPulseWidth = \left(\frac{\text{DITHERCY}}{16} + \text{CCx}\right)\left(\frac{1}{f_{\text{GCLK\_TCC}x}}\right)$$

DITH5 mode:

$$PwmPulseWidth = \left(\frac{\text{DITHERCY}}{32} + \text{CCx}\right)\left(\frac{1}{f_{\text{GCLK\_TCC}x}}\right)$$

DITH6 mode:

$$PwmPulseWidth = \left(\frac{\text{DITHERCY}}{64} + \text{CCx}\right)\left(\frac{1}{f_{\text{GCLK\_TCC}x}}\right)$$

Note: The PWM period will remain static in this case.

41.6.3.4 Ramp Operations

Three ramp operation modes are supported. All of them require the timer/counter running in single-slope PWM generation. The Ramp mode is selected by writing to the Ramp Mode bits in the Waveform Control register (WAVE.RAMP).

RAMP1 Operation

This is the default PWM operation.

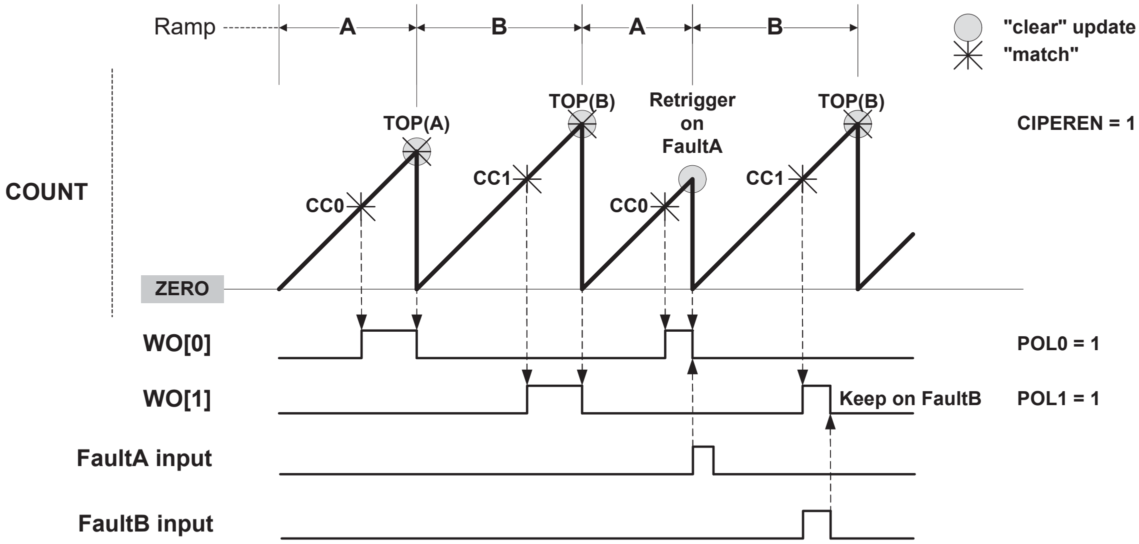
RAMP2 Operation

These operation modes are dedicated for power factor correction (PFC), Half-Bridge and Push-Pull SMPS topologies, where two consecutive timer/counter cycles are interleaved (see the following figure). In cycle A, odd channel output is disabled, and in cycle B, even channel output is disabled. The ramp index changes after each update, but can be software modified using the Ramp index command bits in the Control B Set register (CTRLBSET.IDXCMD).

Standard RAMP2 (RAMP2) Operation

Ramp A and B periods are controlled by the PER register value. The PER value can be different on each ramp by the Circular Period buffer option in the Wave register (WAVE.CIPEREN=1). This mode uses a two-channel TCC to generate two output signals, or one output signal with another CC channel enabled in Capture mode.

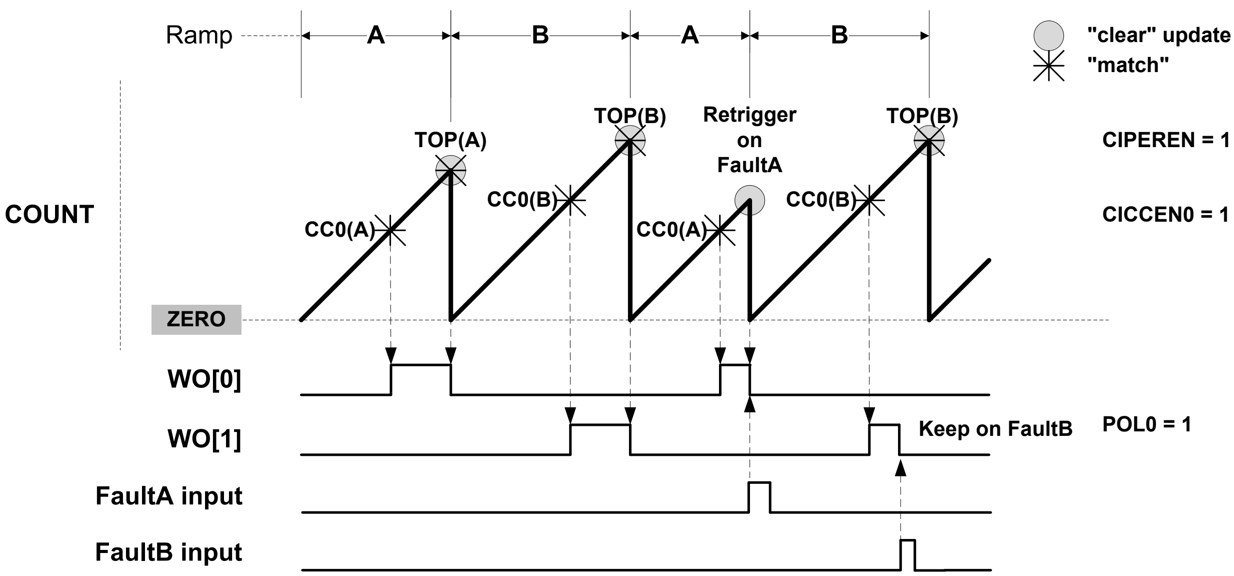
Figure 41-18. RAMP2 Standard Operation



Alternate RAMP2 (RAMP2A) Operation

Alternate RAMP2 operation is similar to RAMP2, but CC0 controls both WO[0] and WO[1] waveforms when the corresponding circular buffer option is enabled (CIPEREN=1). The waveform polarity is the same on both outputs. Channel 1 can be used in capture mode.

Figure 41-19. RAMP2 Alternate Operation



Critical RAMP2 (RAMP2C) Operation

Critical RAMP2 operation provides a way to cover RAMP2 operation requirements without the update constraint associated with the use of circular buffers. In this mode, CC0 is controlling the period of ramp A and PER is controlling the period of ramp B. When using more than two channels, WO[0] output is controlled by CC2 (HIGH) and CC0 (LOW). On TCC with 2 channels, a pulse on WO[0] will last the entire period of ramp A, if WAVE.POL0=0.

Figure 41-20. RAMP2 Critical Operation With More Than 2 Channels

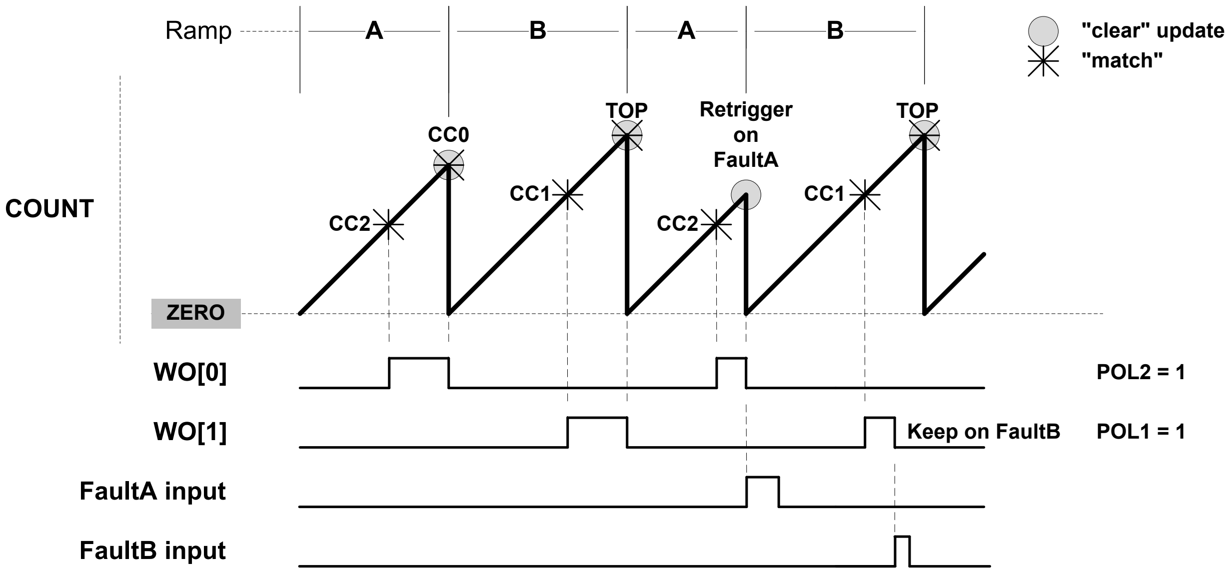
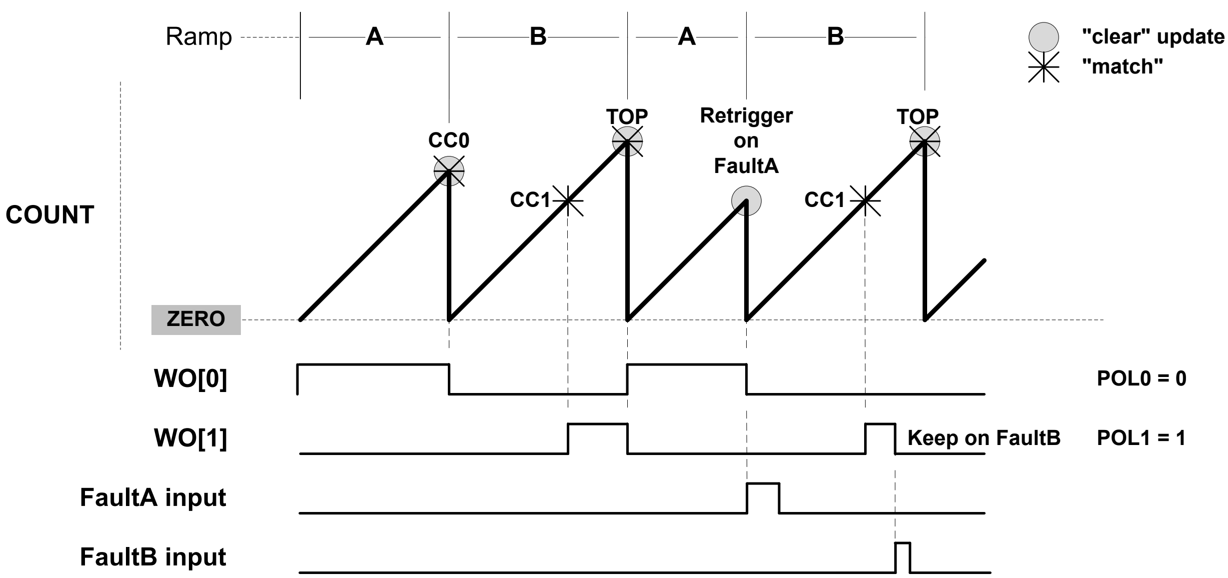


Figure 41-21. RAMP2 Critical Operation With 2 Channels



41.6.3.5 Recoverable Faults

Recoverable faults can restart or halt the timer/counter. Two faults, called Fault A and Fault B, can trigger recoverable fault actions on the compare channels CC0 and CC1 of the TCC. The compare channels' outputs can be clamped to inactive state either as long as the fault condition is present, or from the first valid fault condition detection on until the end of the timer/counter cycle.

Fault Inputs

The first two channel input events (TCCxMC0 and TCCxMC1) can be used as Fault A and Fault B inputs, respectively. Event system channels connected to these fault inputs must be configured as asynchronous. The TCC must work in a PWM mode.

Fault Filtering

There are three filters available for each input Fault A and Fault B. They are configured by the corresponding Recoverable Fault n Configuration registers (FCTRLA and FCTRLB). The three filters can either be used independently or in any combination.

Input Filtering

By default, the event detection is asynchronous. When the event occurs, the fault system will immediately and asynchronously perform the selected fault action on the compare channel output, also in device power modes where the clock is not available. To avoid false fault detection on external events (e.g. due to a glitch on an I/O port) a digital filter can be enabled and configured by the Fault B Filter Value bits in the Fault n Configuration registers (FCTRLn.FILTERVAL). If the event width is less than FILTERVAL (in clock cycles), the event will be discarded. A valid event will be delayed by FILTERVAL clock cycles.

Fault Blanking

This ignores any fault input for a certain time just after a selected waveform output edge. This can be used to prevent false fault triggering due to signal bouncing, as shown in the figure below. Blanking can be enabled by writing an edge triggering configuration to the Fault n Blanking Mode bits in the Recoverable Fault n Configuration register (FCTRLn.BLANK). The desired duration of the blanking must be written to the Fault n Blanking Time bits (FCTRLn.BLANKVAL).

The blanking time $t_b$is calculated by

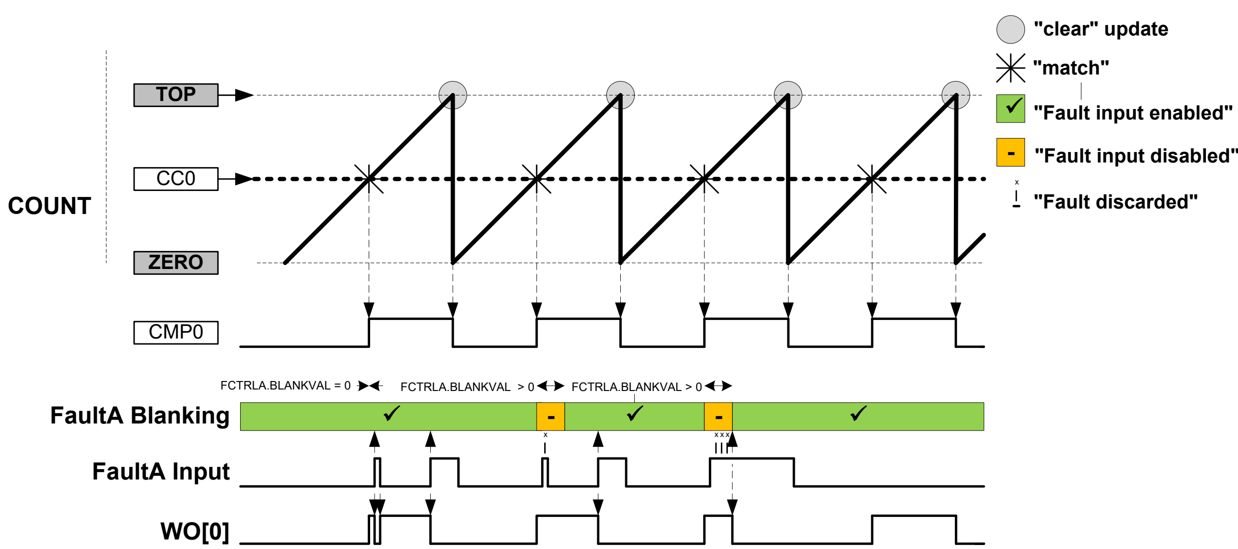
$$t_b = \frac{1 + \mathrm{BLANKVAL}}{f_{\mathrm{GCLK\_TCCx\_PRESC}}}$$

Here, $f_{\mathrm{GCLK\_TCCx\_PRESC}}$ is the frequency of the prescaled peripheral clock frequency $f_{\mathrm{GCLK\_TCCx}}$.

The prescaler is enabled by writing '1' to the Fault n Blanking Prescaler bit (FCTRLn.BLANKPRESC). When disabled, $f_{\mathrm{GCLK\_TCCx\_PRESC}}=f_{\mathrm{GCLK\_TCCx}}$. When enabled, $f_{\mathrm{GCLK\_TCCx\_PRESC}}=f_{\mathrm{GCLK\_TCCx}}/64$.

The maximum blanking time (FCTRLn.BLANKVAL= 255) at $f_{\mathrm{GCLK\_TCCx}}$=96MHz is 2.67µs (no prescaler) or 170µs (prescaling). For $f_{\mathrm{GCLK\_TCCx}}$=1MHz, the maximum blanking time is either 170µs (no prescaling) or 10.9ms (prescaling enabled).

Figure 41-22. Fault Blanking in RAMP1 Operation with Inverted Polarity



Fault Qualification

This is enabled by writing a '1' to the Fault n Qualification bit in the Recoverable Fault n Configuration register (FCTRLn.QUAL). When the recoverable fault qualification is enabled (FCTRLn.QUAL=1), the fault input is disabled all the time the corresponding channel output has an inactive level, as shown in the figures below.

Figure 41-23. Fault Qualification in RAMP1 Operation

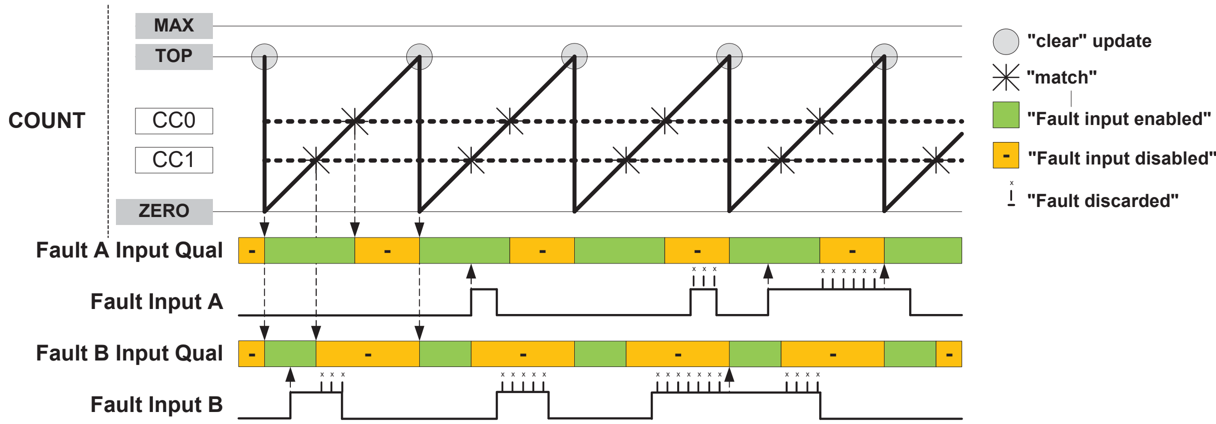
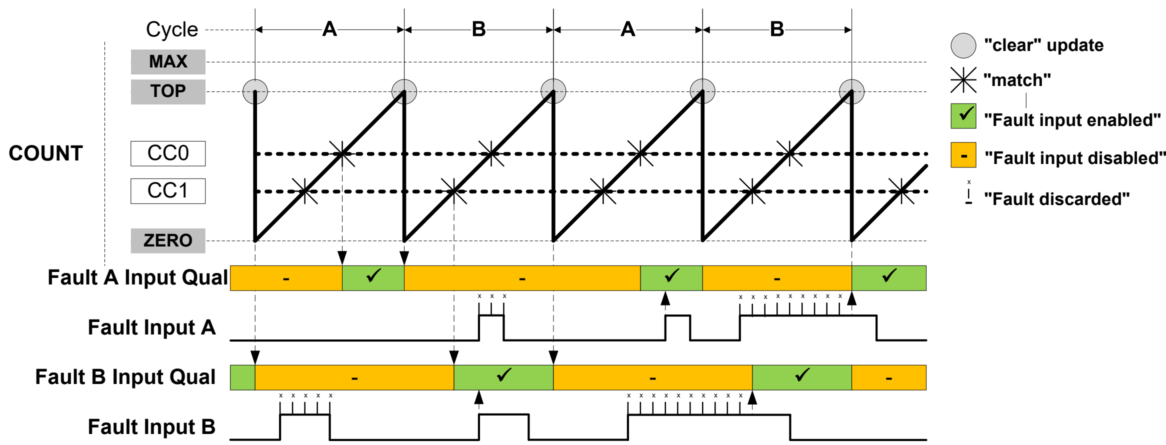


Figure 41-24. Fault Qualification in RAMP2 Operation with Inverted Polarity

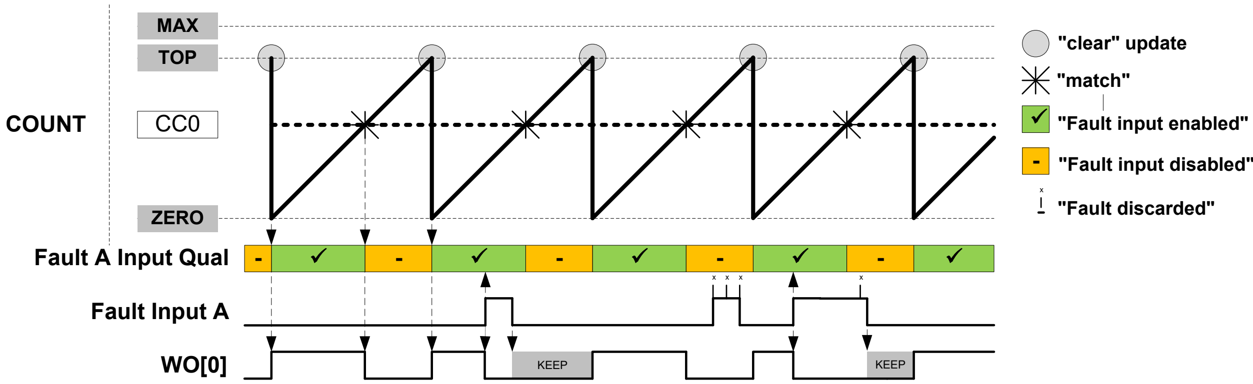


Fault Actions

Different fault actions can be configured individually for Fault A and Fault B. Most fault actions are not mutually exclusive; hence two or more actions can be enabled at the same time to achieve a result that is a combination of fault actions.

Keep Action — This is enabled by writing the Fault n Keeper bit in the Recoverable Fault n Configuration register (FCTRLn.KEEP) to '1'. When enabled, the corresponding channel output will be clamped to zero as long as the fault condition is present. The clamp will be released on the start of the first cycle after the fault condition is no longer present, see next Figure.

Figure 41-25. Waveform Generation with Fault Qualification and Keep Action



Restart Action

This is enabled by writing the Fault n Restart bit in Recoverable Fault n Configuration register (FCTRLn.RESTART) to '1'. When enabled, the timer/counter will be restarted as soon as the corresponding fault condition is present. The ongoing cycle is stopped and the timer/counter starts a new cycle, see Figure 41-26. In Ramp 1 mode, when the new cycle starts, the compare outputs will be clamped to inactive level as long as the fault condition is present.

Note: For RAMP2 operation, when a new timer/counter cycle starts the cycle index will change automatically, see Figure 41-27. Fault A and Fault B are qualified only during the cycle A and cycle B respectively: Fault A is disabled during cycle B, and Fault B is disabled during cycle A.

Figure 41-26. Waveform Generation in RAMP1 mode with Restart Action

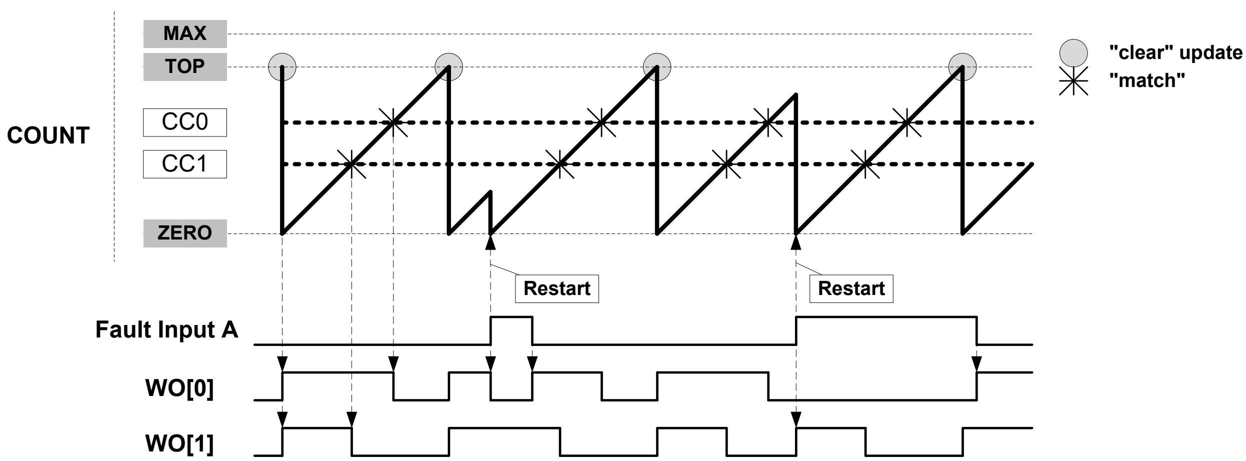
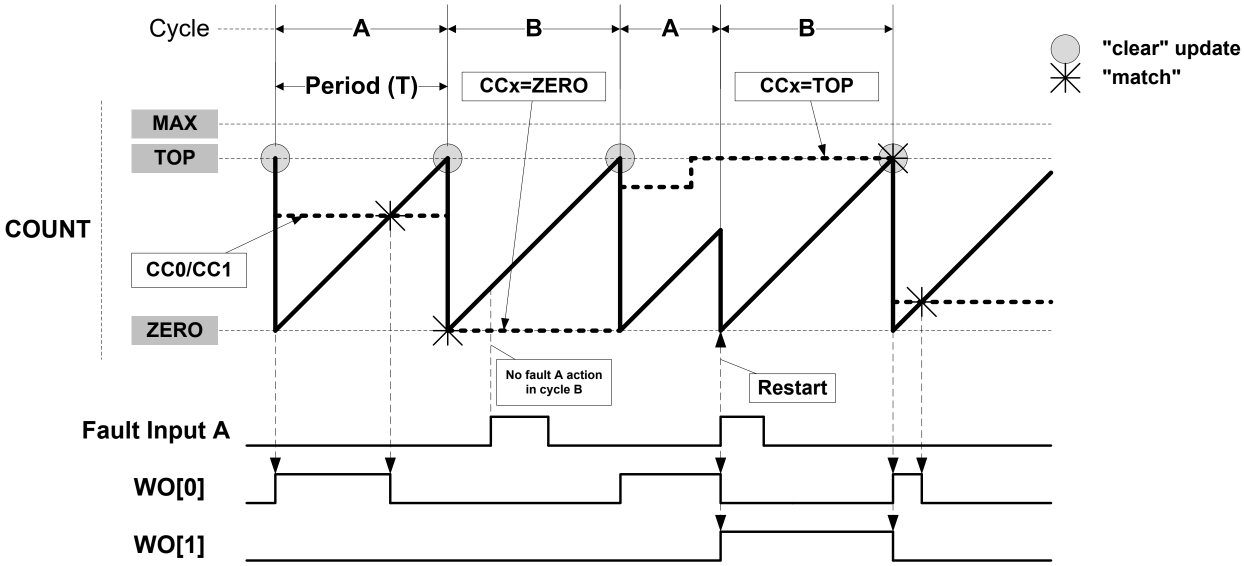


Figure 41-27. Waveform Generation in RAMP2 mode with Restart Action



Capture Action

Several capture actions can be selected by writing the Fault n Capture Action bits in the Fault n Control register (FCTRLn.CAPTURE). When one of the capture operations is selected, the counter value is captured when the fault occurs. These capture operations are available:

- CAPT - the equivalent to a standard capture operation.
- CAPTMIN - gets the minimum time stamped value: on each new local minimum captured value, an event or interrupt is issued.
- CAPTMAX - gets the maximum time stamped value: on each new local maximum captured value, an event or interrupt (IT) is issued, see Figure 41-28.
- LOCMIN - notifies by event or interrupt when a local minimum captured value is detected.
- LOCMAX - notifies by event or interrupt when a local maximum captured value is detected.
- DERIV0 - notifies by event or interrupt when a local extreme captured value is detected, see Figure 41-29.

CCx Content:

In CAPTMIN and CAPTMAX operations, CCx keeps the respective extremum captured values, see Figure 41-28. In LOCMIN, LOCMAX or DERIV0 operation, CCx follows the counter value at fault time, see Figure 41-29.

Before enabling CAPTMIN or CAPTMAX mode of capture, the user must initialize the corresponding CCx register value to a value different from zero (for CAPTMIN) top (for CAPTMAX). If the CCx register initial value is zero (for CAPTMIN) top (for CAPTMAX), no captures will be performed using the corresponding channel.

MCx Behaviour:

In LOCMIN and LOCMAX operation, capture is performed on each capture event. The MCx interrupt flag is set only when the captured value is above or equal (for LOCMIN) or below or equal (for LOCMAX) to the previous captured value. So interrupt flag is set when a new relative local Minimum (for CAPTMIN) or Maximum (for CAPTMAX) value has been detected. DERIV0 is equivalent to an OR function of (LOCMIN, LOCMAX).

In CAPT operation, capture is performed on each capture event. The MCx interrupt flag is set on each new capture.

In CAPTMIN and CAPTMAX operation, capture is performed only when on capture event time, the counter value is lower (for CAPTMIN) or higher (for CAPMAX) than the last captured value. The MCx interrupt flag is set only when on capture event time, the counter value is higher or equal (for CAPTMIN) or lower or equal (for CAPTMAX) to the value captured on the previous event. So interrupt flag is set when a new absolute local Minimum (for CAPTMIN) or Maximum (for CAPTMAX) value has been detected.

Interrupt Generation

In CAPT mode, an interrupt is generated on each filtered Fault n and each dedicated CCx channel capture counter value. In other modes, an interrupt is only generated on an extreme captured value.

Figure 41-28. Capture Action “CAPTMAX”

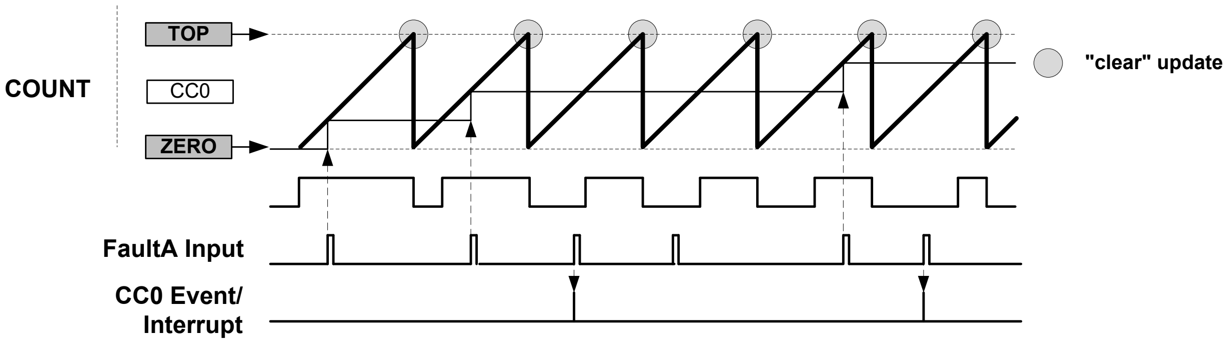
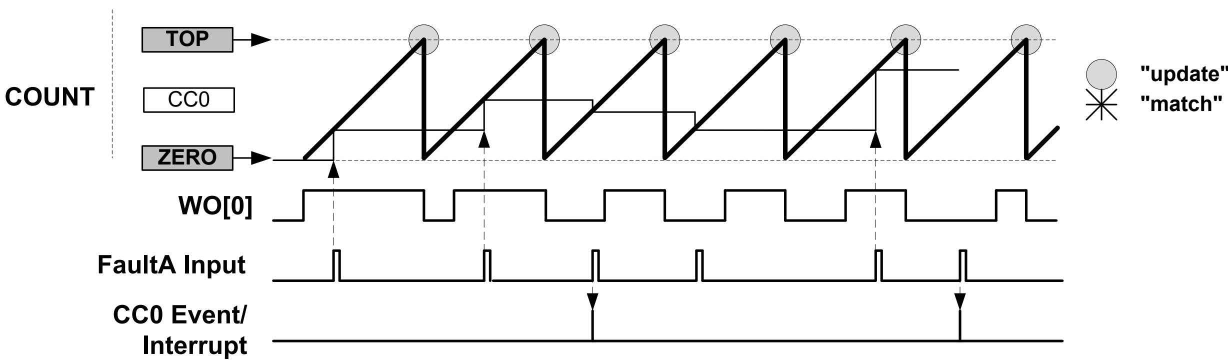


Figure 41-29. Capture Action “DERIV0”



Hardware Halt Action

This is configured by writing 0x1 to the Fault n Halt mode bits in the Recoverable Fault n Configuration register (FCTRLn.HALT). When enabled, the timer/counter is halted and the cycle is extended as long as the corresponding fault is present.

The next figure ('Waveform Generation with Halt and Restart Actions') shows an example where both restart action and hardware halt action are enabled for Fault A. The compare channel 0 output is clamped to inactive level as long as the timer/counter is halted. The timer/counter resumes the counting operation as soon as the fault condition is no longer present. As the restart action is enabled in this example, the timer/counter is restarted after the fault condition is no longer present.

The figure after that ('Waveform Generation with Fault Qualification, Halt, and Restart Actions') shows a similar example, but with additionally enabled fault qualification. Here, counting is resumed after the fault condition is no longer present.

Note that in RAMP2 and RAMP2A operations, when a new timer/counter cycle starts, the cycle index will automatically change.

Figure 41-30. Waveform Generation with Halt and Restart Actions

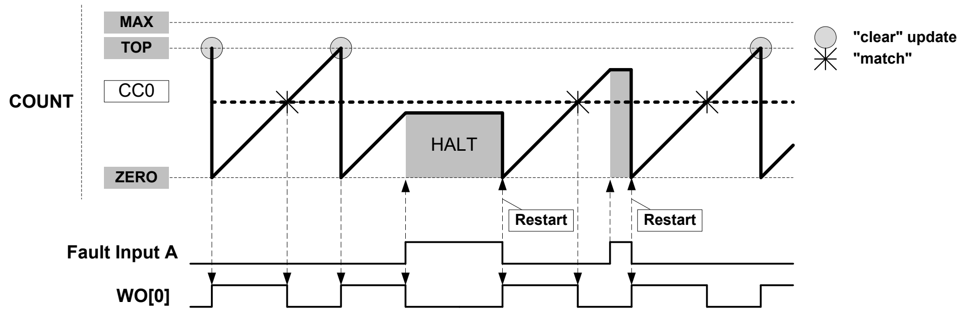
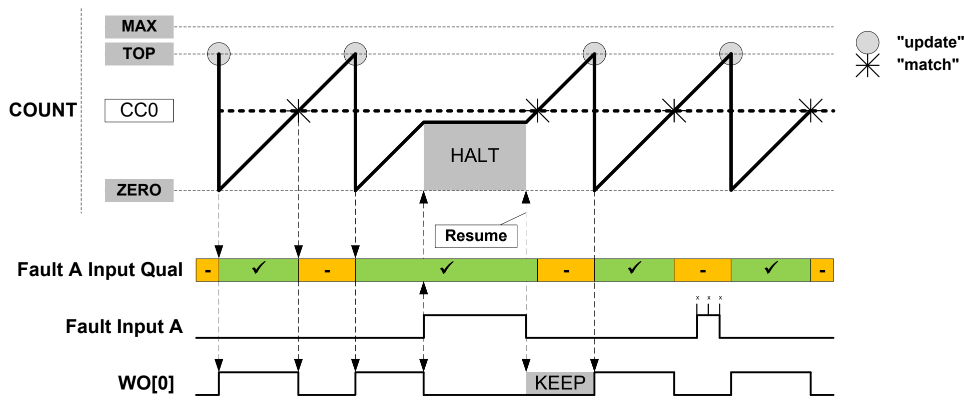


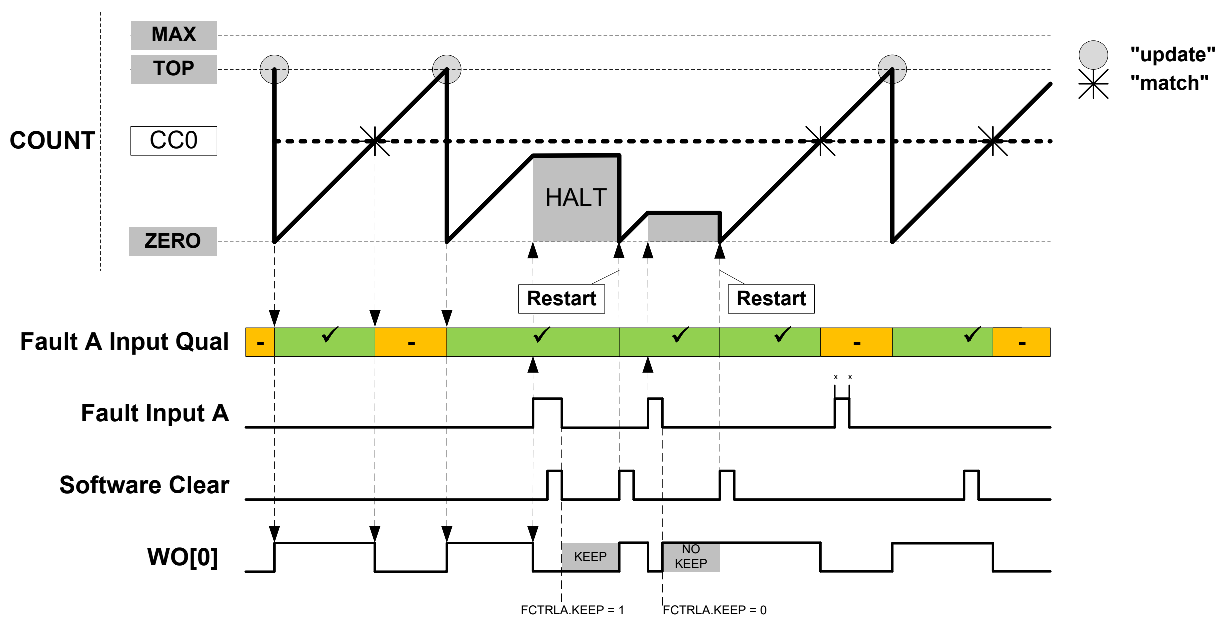
Figure 41-31. Waveform Generation with Fault Qualification, Halt, and Restart Actions



Software Halt Action

This is configured by writing 0x2 to the Fault n Halt mode bits in the Recoverable Fault n configuration register (FCTRLn.HALT). Software halt action is similar to hardware halt action, but in order to restart the timer/counter, the corresponding fault condition must not be present anymore, and the corresponding FAULT n bit in the STATUS register must be cleared by software.

Figure 41-32. Waveform Generation with Software Halt, Fault Qualification, Keep and Restart Actions



41.6.3.6 Non-Recoverable Faults

The non-recoverable fault action will force all the compare outputs to a pre-defined level programmed into the Driver Control register (DRVCTRL.NRE and DRVCTRL.NRV). The non-recoverable fault input (EV0 and EV1) actions are enabled in Event Control register (EVCTRL.EVACT0 and EVCTRL.EVACT1).

To avoid false fault detection on external events (e.g. a glitch on an I/O port) a digital filter can be enabled using Non-Recoverable Fault Input x Filter Value bits in the Driver Control register (DRVCTRL.FILTERVALn). Therefore, the event detection is synchronous, and event action is delayed by the selected digital filter value clock cycles.

When the Fault Detection on Debug Break Detection bit in Debug Control register (DGBCTRL.FDDBD) is written to '1', a non-recoverable Debug Faults State and an interrupt (DFS) is generated when the system goes in debug operation.

In RAMP2, RAMP2A, or DSBOTH operation, when the Lock Update bit in the Control B register is set by writing CTRLBSET.LUPD=1 and the ramp index or counter direction changes, a non-recoverable Update Fault State and the respective interrupt (UFS) are generated.

41.6.3.7 Timestamp Capture

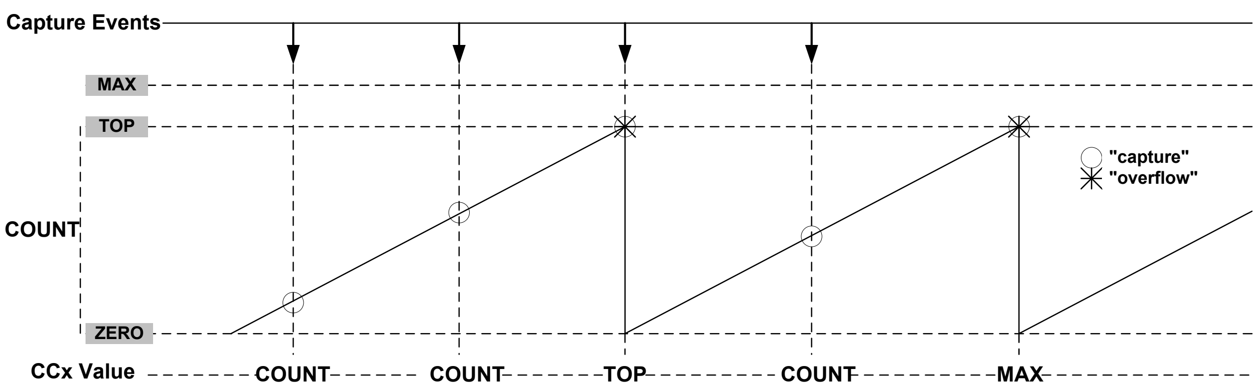
This feature is enabled when the Capture Time Stamp (STAMP) Event Action in Event Control register (EVCTRL.EVACT) is selected. The counter TOP value must be smaller than MAX.

When a capture event is detected, the COUNT value is copied into the corresponding Channel x Compare/Capture Value (CCx) register. If an overflow occurs, the MAX value is copied into the corresponding CCx register.

When a valid captured value is present in the capture channel register, the corresponding Capture Channel x Interrupt Flag (INTFLAG.MCx) is set.

The timer/counter can detect capture overflow of the input capture channels. When a new capture event is detected while the Capture Channel interrupt flag (INTFLAG.MCx) is still set, the new timestamp will not be stored and INTFLAG.ERR will be set. The user needs to clear INTFLAG.MCx at the beginning of the interrupt routine and poll the bit until INTFLAG.MCx is cleared before exiting the ISR.

Figure 41-33. Time-Stamp



41.6.3.8 Waveform Extension

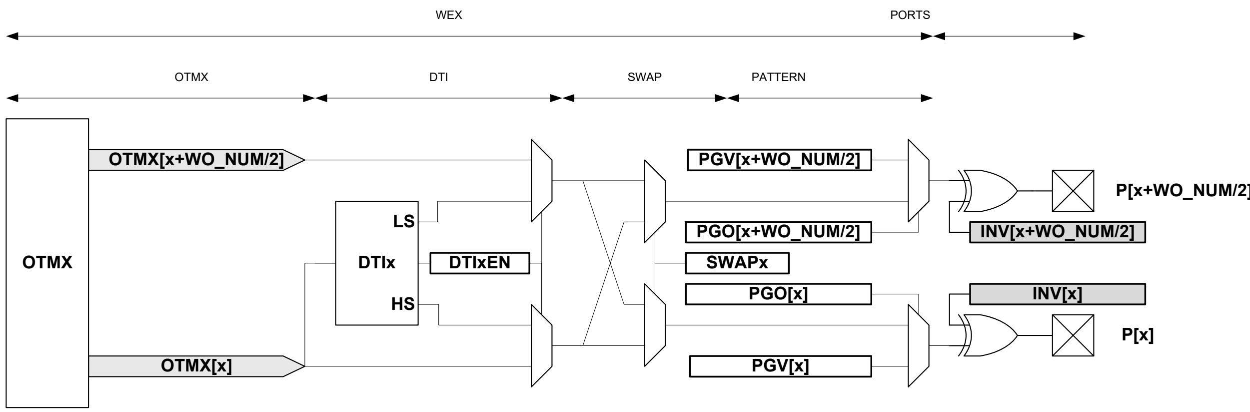
Figure 41-34 shows a schematic diagram of actions of the four optional units that follow the recoverable fault stage on a port pin pair: Output Matrix (OTMX), Dead-Time Insertion (DTI), SWAP and Pattern Generation. The DTI and SWAP units can be seen as a four port pair slices:

- Slice 0 DTI0 / SWAP0 acting on port pins (WO[0], WO[WO_NUM/2 +0])
- Slice 1 DTI1 / SWAP1 acting on port pins (WO[1], WO[WO_NUM/2 +1])

And generally:

- Slice n DTIx / SWAPx acting on port pins (WO[x], WO[WO_NUM/2 +x])

Figure 41-34. Waveform Extension Stage Details



The **output matrix (OTMX)** unit distributes compare channels, according to the selectable configurations in the following table.

Table 41-6. Output Matrix Channel Pin Routing Configuration

Value	OTMX[7]	OTMX[6]	OTMX[5]	OTMX[4]	OTMX[3]	OTMX[2]	OTMX[1]	OTMX[0]
0x0	CC1	CC0	CC5	CC4	CC3	CC2	CC1	CC0
0x1	CC1	CC0	CC2	CC1	CC0	CC2	CC1	CC0
0x2	CC0	CC0	CC0	CC0	CC0	CC0	CC0	CC0
0x3	CC1	CC1	CC1	CC1	CC1	CC1	CC1	CC0

- Configuration 0x0 is the default configuration. The channel location is the default one and channels are distributed on outputs modulo the number of channels. Channel 0 is routed to the Output matrix output OTMX[0], and Channel 1 to OTMX[1]. If there are more outputs than channels, then channel 0 is duplicated to the Output matrix output OTMX[CC_NUM], channel 1 to OTMX[CC_NUM+1] and so on.
- Configuration 0x1 distributes the channels on output modulo half the number of channels. This assigns twice the number of output locations to the lower channels than the default configuration. This can be used, for example, to control the four transistors of a full bridge using only two compare channels.
  Using pattern generation, some of these four outputs can be overwritten by a constant level, enabling flexible drive of a full bridge in all quadrant configurations.
- Configuration 0x2 distributes compare channel 0 (CC0) to all port pins. With pattern generation, this configuration can control a stepper motor.
- Configuration 0x3 distributes the compare channel CC0 to the first output, and the channel CC1 to all other outputs. Together with pattern generation and the fault extension, this configuration can control up to seven LED strings, with a boost stage.

The table below is an example showing four compare channels on four outputs.

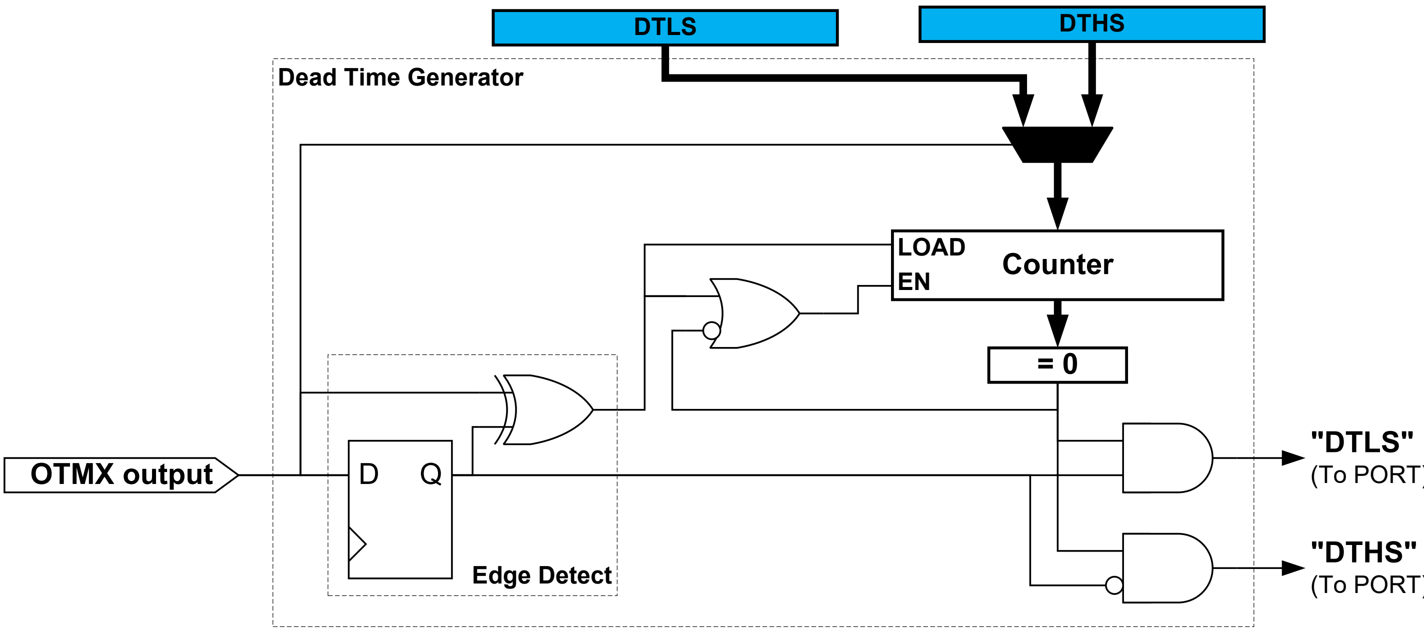
Table 41-7. Four Compare Channels on Four Outputs

Value	OTMX[3]	OTMX[2]	OTMX[1]	OTMX[0]
0x0	CC3	CC2	CC1	CC0
0x1	CC1	CC0	CC1	CC0
0x2	CC0	CC0	CC0	CC0
0x3	CC1	CC1	CC1	CC0

The dead-time insertion (DTI) unit generates OFF time with the non-inverted low side (LS) and inverted high side (HS) of the wave generator output forced at low level. This OFF time is called dead time. Dead-time insertion ensures that the LS and HS will never switch simultaneously.

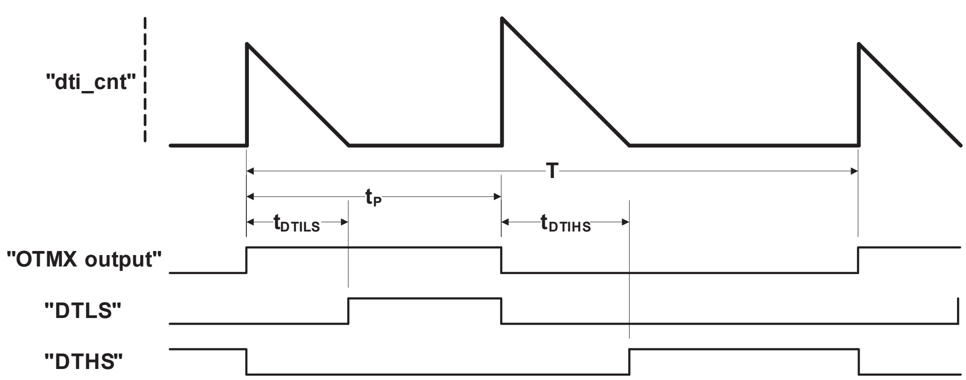
The DTI stage consists of four equal dead-time insertion generators; one for each of the first four compare channels. Figure 41-35 shows the block diagram of one DTI generator. The four channels have a common register which controls the dead time, which is independent of high side and low side setting.

Figure 41-35. Dead-Time Generator Block Diagram



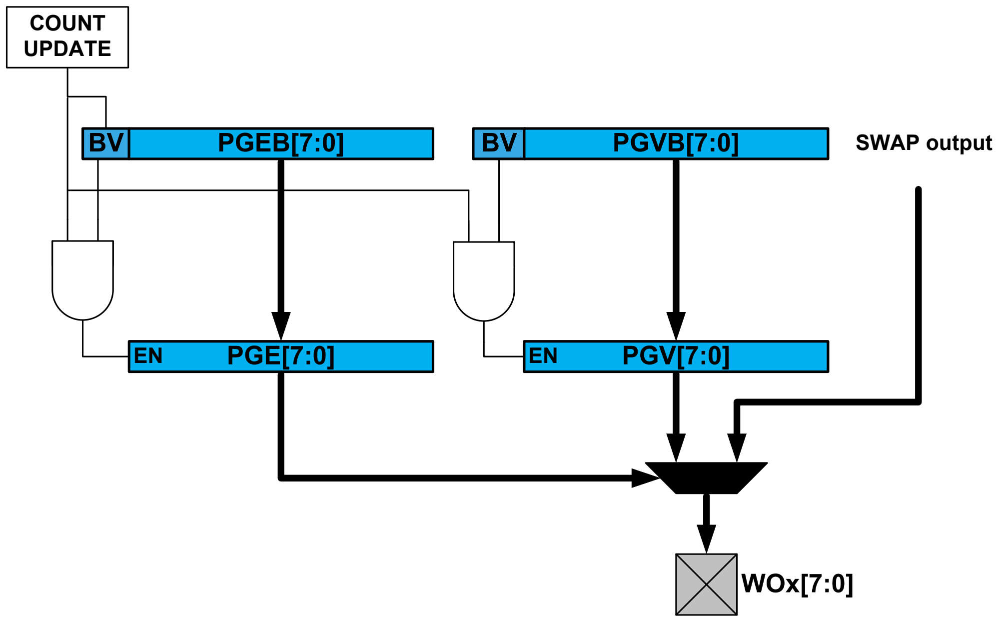
As shown in Figure 41-36, the 8-bit dead-time counter is decremented by one for each peripheral clock cycle until it reaches zero. A non-zero counter value will force both the low side and high side outputs into their OFF state. When the output matrix (OTMX) output changes, the dead-time counter is reloaded according to the edge of the input. When the output changes from low to high (positive edge) it initiates a counter reload of the DTLS register. When the output changes from high to low (negative edge) it reloads the DTHS register.

Figure 41-36. Dead-Time Generator Timing Diagram



The pattern generator unit produces a synchronized bit pattern across the port pins it is connected to. The pattern generation features are primarily intended for handling the commutation sequence in brushless DC motors (BLDC), stepper motors, and full bridge control. See also Figure 41-37.

Figure 41-37. Pattern Generator Block Diagram



As with other double-buffered timer/counter registers, the register update is synchronized to the UPDATE condition set by the timer/counter waveform generation operation. If synchronization is not required by the application, the software can simply access directly the PATT.PGE, PATT.PGV bits registers.

41.6.4 Host/Client Operation

Two TCC instances sharing the same GCLK_TCC clock, can be linked to provide more synchronized CC channels. The operation is enabled by setting the Host Synchronization bit in Control A register (CTRLA.MSYNC) in the Client instance. When the bit is set, the Client TCC instance will synchronize the CC channels to the Host counter.

Related Links

CTRLA

Control A

41.6.5 DMA, Interrupts, and Events

Table 41-8. Module Requests for TCC

Condition	Interrupt request	Event output	Event input	DMA request	DMA request is cleared
Overflow / Underflow	Yes	Yes		Yes[(1)]	On DMA acknowledge
Channel Compare Match or Capture	Yes	Yes	Yes[(2)]	Yes[(3)]	For circular buffering: on DMA acknowledge For capture channel: when CCx register is read
Retrigger	Yes	Yes			
Count	Yes	Yes			
Capture Overflow Error	Yes				
Debug Fault State	Yes				
Recoverable Faults	Yes				

...........continued					
Condition	Interrupt request	Event output	Event input	DMA request	DMA request is cleared
Non-Recoverable Faults	Yes				
TCCx Event 0 input			Yes[4]		
TCCx Event 1 input			Yes[5]		

Notes:
1. DMA request set on Overflow, Underflow or Re-trigger conditions.
2. Can perform capture or generate recoverable fault on an event input.
3. In Capture or Circular modes.
4. On event input, either action can be executed:
   – re-trigger counter
   – control counter direction
   – stop the counter
   – decrement the counter
   – perform period and pulse width capture
   – generate non-recoverable fault
5. On event input, either action can be executed:
   – re-trigger counter
   – increment or decrement counter depending on direction
   – start the counter
   – increment or decrement counter based on direction
   – increment counter regardless of direction
   – generate non-recoverable fault

41.6.5.1 DMA Operation

The TCC can generate the following DMA requests:

Counter overflow (OVF)	If the One-shot Trigger mode in the control A register (CTRLA.DMAOS) is written to '0', the TCC generates a DMA request on each cycle when an update condition (Overflow, Underflow or Re-trigger) is detected. When an update condition (Overflow, Underflow or Re-trigger) is detected while CTRLA.DMAOS=1, the TCC generates a DMA trigger on the cycle following the DMA One-Shot Command written to the Control B register (CTRLBSET.CMD=DMAOS). In both cases, the request is cleared by hardware on DMA acknowledge.
Channel Match (MCx)	A DMA request is set only on a compare match if CTRLA.DMAOS=0. The request is cleared by hardware on DMA acknowledge. When CTRLA.DMAOS=1, the DMA requests are not generated.
Channel Capture (MCx)	For a capture channel, the request is set when valid data is present in the CCx register, and cleared once the CCx register is read. In this operation mode, the CTRLA.DMAOS bit value is ignored.

DMA Operation with Circular Buffer

When circular buffer operation is enabled, the Buffer registers must be written in a correct order and synchronized to the update times of the timer. The DMA triggers of the TCC provide a way to ensure a safe and correct update of circular buffers.
Note: Circular buffer are intended to be used with RAMP2, RAMP2A and DSBOTH operation only.

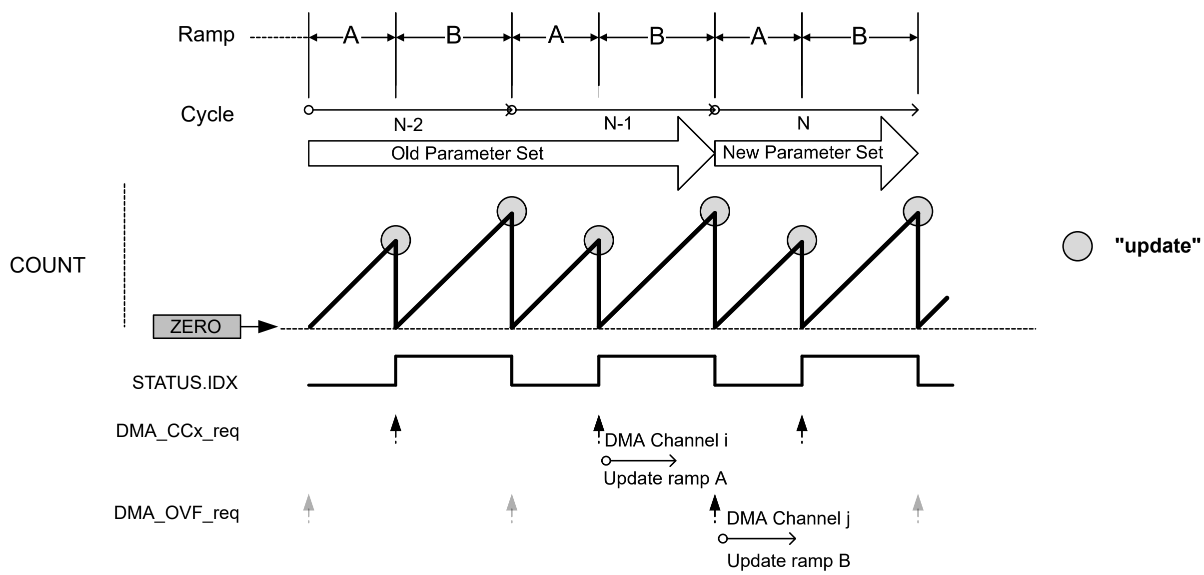
DMA Operation with Circular Buffer in RAMP2 and RAMP2A Mode

When a CCx channel is selected as a circular buffer, the related DMA request is not set on a compare match detection, but on start of ramp B.

If at least one circular buffer is enabled, the DMA overflow request is conditioned to the start of ramp A with an effective DMA transfer on previous ramp B (DMA acknowledge).

The update of all circular buffer values for ramp A can be done through a DMA channel triggered on a MC trigger. The update of all circular buffer values for ramp B, can be done through a second DMA channel triggered by the overflow DMA request.

Figure 41-38. DMA Triggers in RAMP and RAMP2 Operation Mode and Circular Buffer Enabled

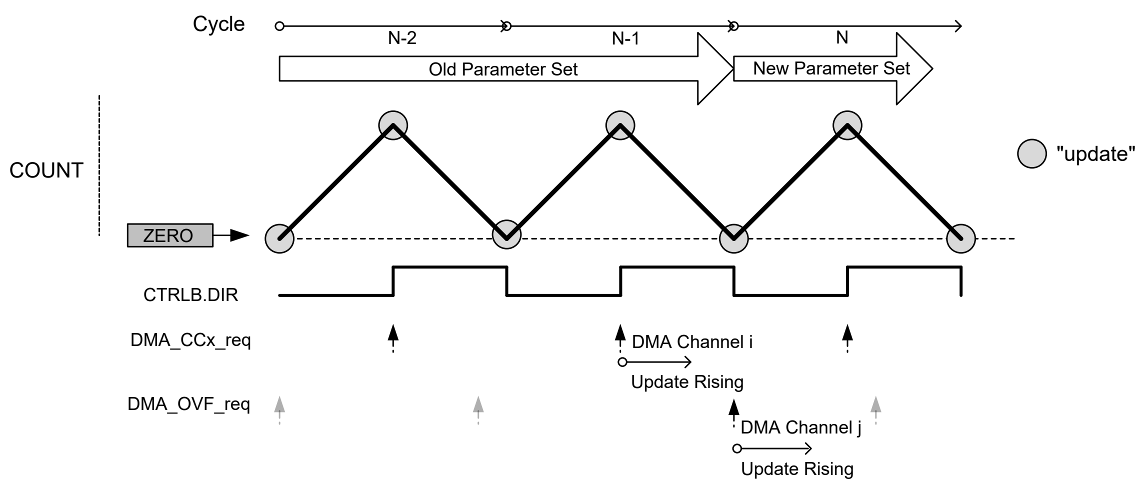


DMA Operation with Circular Buffer in DSBOTH Mode
When a CC channel is selected as a circular buffer, the related DMA request is not set on a compare match detection, but on start of down-counting phase.

If at least one circular buffer is enabled, the DMA overflow request is conditioned to the start of up-counting phase with an effective DMA transfer on previous down-counting phase (DMA acknowledge).

When up-counting, all circular buffer values can be updated through a DMA channel triggered by MC trigger. When down-counting, all circular buffer values can be updated through a second DMA channel, triggered by the OVF DMA request.

Figure 41-39. DMA Triggers in DSBOTH Operation Mode and Circular Buffer Enabled



41.6.5.2 Interrupts

The TCC has the following interrupt sources:

- Overflow/Underflow (OVF)
- Retrigger (TRG)
- Count (CNT) – Refer also to the description of EVCTRL.CNTSEL
- Capture Overflow Error (ERR)
- Non-Recoverable Update Fault (UFS)
- Debug Fault State (DFS)
- Recoverable Faults (FAULTn)
- Non-recoverable Faults (FAULTx)
- Compare Match or Capture Channels (MCx)

These interrupts are asynchronous wake-up sources.

Each interrupt source has an Interrupt flag associated with it. The Interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the Interrupt condition occurs. Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set (INTENSET) register, and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register. The status of enabled interrupts can be read from either INTENSET or INTENCLR.

An interrupt request is generated when the Interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the Interrupt flag is cleared, the interrupt is disabled or the TCC is reset. See *INTFLAG* from Related Links for details on how to clear Interrupt flags. The TCC has one common interrupt request line for all the interrupt sources. The user must read the INTFLAG register to determine which Interrupt condition is present.

Interrupts must be globally enabled for interrupt requests to be generated. See *Nested Vector Interrupt Controller (NVIC)* from Related Links.

Related Links

Nested Vector Interrupt Controller (NVIC)

INTFLAG

Interrupt Flag Status and Clear

41.6.5.3 Events

The TCC can generate the following output events:

- Overflow/Underflow (OVF)
- Trigger (TRG)
- Counter (CNT) (For further details, refer to the EVCTRL.CNTSEL description.)
- Compare Match or Capture on compare/capture channels: MCx

Writing a '1' ('0') to an Event Output bit in the Event Control Register (EVCTRL.xxEO) enables (disables) the corresponding output event. See *Event System (EVSYS)* from Related Links.

The TCC can take the following actions on a channel input event (MCx):

- Capture event
- Generate a recoverable or non-recoverable fault

The TCC can take the following actions on counter Event 1 (TCCx EV1):

- Counter re-trigger
- Counter direction control
- Stop the counter
- Decrement the counter on event
- Period and pulse width capture
- Non-recoverable fault

The TCC can take the following actions on counter Event 0 (TCCx EV0):

- Counter re-trigger
- Count on event (increment or decrement, depending on counter direction)
- Counter start – Start counting on the event rising edge. Further events will not restart the counter; the counter will keep counting using prescaled GCLK_TCCx, until it reaches TOP or ZERO, depending on the direction.
- Counter increment on event. This will increment the counter, irrespective of the counter direction.
- Count during active state of an asynchronous event (increment or decrement, depending on counter direction). In this case, the counter will be incremented or decremented on each cycle of the prescaled clock, as long as the event is active.
- Non-recoverable fault

The counter Event Actions are available in the Event Control registers (EVCTRL.EVACT0 and EVCTRL.EVACT1). See *EVCTRL* from Related Links.

Writing a '1' ('0') to an Event Input bit in the Event Control register (EVCTRL.MCEIx or EVCTRL.TCEIx) enables (disables) the corresponding action on input event.

Note: When several events are connected to the TCC, the enabled action will apply for each of the incoming events. See *Event System (EVSYS)* from Related Links for details on how to configure the Event System.

Related Links

Event System (EVSYS)

EVCTRL

Event Control

41.6.6 Sleep Mode Operation

The TCC can be configured to operate in any Sleep mode. To be able to run in standby the RUNSTDBY bit in the Control A register (CTRLA.RUNSTDBY) must be '1'. The MODULE can in any Sleep mode wake-up the device using interrupts or perform actions through the Event System.

41.6.7 Synchronization

Due to asynchronicity between the main clock domain and the peripheral clock domains, some registers need to be synchronized when written or read.

The following bits are synchronized when written:

- Software Reset and Enable bits in Control A register (CTRLA.SWRST and CTRLA.ENABLE)

The following registers are synchronized when written:

- Control B Clear and Control B Set registers (CTRLBCLR and CTRLBSET)
- Status register (STATUS)
- Pattern and Pattern Buffer registers (PATT and PATTBUF)
- Waveform register (WAVE)
- Count Value register (COUNT)
- Period Value and Period Buffer Value registers (PER and PERBUF)
- Compare/Capture Channel x and Channel x Compare/Capture Buffer Value registers (CCx and CCBUFx)

The following registers are synchronized when read:

- Control B Clear and Control B Set registers (CTRLBCLR and CTRLBSET)
- Count Value register (COUNT): synchronization is done on demand through READSYNC command (CTRLBSET.CMD)
- Pattern and Pattern Buffer registers (PATT and PATTBUF)
- Waveform register (WAVE)
- Period Value and Period Buffer Value registers (PER and PERBUF)
- Compare/Capture Channel x and Channel x Compare/Capture Buffer Value registers (CCx and CCBUFx)

Required write synchronization is denoted by the "Write-Synchronized" property in the register description.

Required read synchronization is denoted by the "Read-Synchronized" property in the register description.

41.7 Register Summary

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x00	CTRLA	7:0		RESOLUTION[1:0]					ENABLE	SWRST
		15:8	MSYNC	ALOCK	PRESCYNC[1:0]		RUNSTDBY	PRESCALER[2:0]		
		23:16	DMAOS							
		31:24					CPTEN3	CPTEN2	CPTEN1	CPTEN0
0x04	CTRLBCLR	7:0	CMD[2:0]			IDXCMD[1:0]		ONESHOT	LUPD	DIR
0x05	CTRLBSET	7:0	CMD[2:0]			IDXCMD[1:0]		ONESHOT	LUPD	DIR
0x06 ... 0x07	Reserved									
0x08	SYNCBUSY	7:0	PER	WAVE	PATT	COUNT	STATUS	CTRLB	ENABLE	SWRST
		15:8			CC5	CC4	CC3	CC2	CC1	CC0
		23:16								
		31:24								
0x0C	FCTRLA	7:0	RESTART	BLANK[1:0]		QUAL	KEEP		SRC[1:0]	
		15:8	BLANKPRESC	CAPTURE[2:0]			CHSEL[1:0]		HALT[1:0]	
		23:16	BLANKVAL[7:0]							
		31:24					FILTERVAL[3:0]			
0x10	FCTRLB	7:0	RESTART	BLANK[1:0]		QUAL	KEEP		SRC[1:0]	
		15:8	BLANKPRESC	CAPTURE[2:0]			CHSEL[1:0]		HALT[1:0]	
		23:16	BLANKVAL[7:0]							
		31:24					FILTERVAL[3:0]			
0x14	WEXCTRL	7:0							OTMX[1:0]	
		15:8					DTIEN3	DTIEN2	DTIEN1	DTIEN0
		23:16	DTLS[7:0]							
		31:24	DTHS[7:0]							
0x18	DRVCTRL	7:0	NRE7	NRE6	NRE5	NRE4	NRE3	NRE2	NRE1	NRE0
		15:8	NRV7	NRV6	NRV5	NRV4	NRV3	NRV2	NRV1	NRV0
		23:16	INVEN7	INVEN6	INVEN5	INVEN4	INVEN3	INVEN2	INVEN1	INVEN0
		31:24	FILTERVAL1[3:0]				FILTERVAL0[3:0]			
0x1C ... 0x1D	Reserved									
0x1E	DBGCTRL	7:0						FDDBD		DBGRUN
0x1F	Reserved									
0x20	EVCTRL	7:0	CNTSEL[1:0]		EVACT1[2:0]			EVACT0[2:0]		
		15:8	TCEI1	TCEI0	TCINV1	TCINV0		CNTEO	TRGEO	OVFEO
		23:16					MCEI3	MCEI2	MCEI1	MCEI0
		31:24					MCEO3	MCEO2	MCEO1	MCEO0
0x24	INTENCLR	7:0					ERR	CNT	TRG	OVF
		15:8	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS		
		23:16					MCx3	MCx2	MCx1	MCx0
		31:24								
0x28	INTENSET	7:0					ERR	CNT	TRG	OVF
		15:8	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS		
		23:16					MC3	MC2	MC1	MC0
		31:24								
0x2C	INTFLAG	7:0					ERR	CNT	TRG	OVF
		15:8	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS		
		23:16					MC3	MC2	MC1	MC0
		31:24								
0x30	STATUS	7:0	PERBUFV		PATTBUFV	SLAVE	DFS	UFS	IDX	STOP
		15:8	FAULT1	FAULT0	FAULTB	FAULTA	FAULT1IN	FAULT0IN	FAULTBIN	FAULTAIN
		23:16					CCBUFV3	CCBUFV2	CCBUFV1	CCBUFV0
		31:24					CMP3	CMP2	CMP1	CMP0
0x34	COUNT	7:0	COUNT[7:0]							
		15:8	COUNT[15:8]							
		23:16	COUNT[23:16]							
		31:24								

...........continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x38	PATT	7:0	PGE7	PGE6	PGE5	PGE4	PGE3	PGE2	PGE1	PGE0
		15:8	PGV7	PGV6	PGV5	PGV4	PGV3	PGV2	PGV1	PGV0
0x3A ... 0x3B	Reserved									
0x3C	WAVE	7:0	CIPEREN		RAMP[1:0]			WAVEGEN[2:0]		
		15:8					CICCEN3	CICCEN2	CICCEN1	CICCEN0
		23:16			POL5	POL4	POL3	POL2	POL1	POL0
		31:24					SWAP3	SWAP2	SWAP1	SWAP0
0x40	PER	7:0	PER[1:0]		DITHER[5:0]					
		15:8	PER[9:2]							
		23:16	PER[17:10]							
		31:24								
0x44	CC0	7:0	CC[1:0]		DITHER[5:0]					
		15:8	CC[9:2]							
		23:16	CC[17:10]							
		31:24								
0x48	CC1	7:0	CC[1:0]		DITHER[5:0]					
		15:8	CC[9:2]							
		23:16	CC[17:10]							
		31:24								
0x4C	CC2	7:0	CC[1:0]		DITHER[5:0]					
		15:8	CC[9:2]							
		23:16	CC[17:10]							
		31:24								
0x50	CC3	7:0	CC[1:0]		DITHER[5:0]					
		15:8	CC[9:2]							
		23:16	CC[17:10]							
		31:24								
0x54	CC4	7:0	CC[1:0]		DITHER[5:0]					
		15:8	CC[9:2]							
		23:16	CC[17:10]							
		31:24								
0x58	CC5	7:0	CC[1:0]		DITHER[5:0]					
		15:8	CC[9:2]							
		23:16	CC[17:10]							
		31:24								
0x5C ... 0x63	Reserved									
0x64	PATTBUF	7:0	PGEB7	PGEB6	PGEB5	PGEB4	PGEB3	PGEB2	PGEB1	PGEB0
		15:8	PGVB7	PGVB6	PGVB5	PGVB4	PGVB3	PGVB2	PGVB1	PGVB0
0x66 ... 0x6B	Reserved									
0x6C	PERBUF	7:0	PERBUF[1:0]		DITHERBUF[5:0]					
		15:8	PERBUF[9:2]							
		23:16	PERBUF[17:10]							
		31:24								
0x70	CCBUF0	7:0	CCBUF[1:0]		DITHERBUF[5:0]					
		15:8	CCBUF[9:2]							
		23:16	CCBUF[17:10]							
		31:24								
0x74	CCBUF1	7:0	CCBUF[1:0]		DITHERBUF[5:0]					
		15:8	CCBUF[9:2]							
		23:16	CCBUF[17:10]							
		31:24								
0x78	CCBUF2	7:0	CCBUF[1:0]		DITHERBUF[5:0]					
		15:8	CCBUF[9:2]							
		23:16	CCBUF[17:10]							
		31:24								

...........continued

Offset	Name	Bit Pos.	7	6	5	4	3	2	1	0
0x7C	CCBUF3	7:0	CCBUF[1:0]		DITHERBUF[5:0]					
		15:8	CCBUF[9:2]							
		23:16	CCBUF[17:10]							
		31:24								
0x80	CCBUF4	7:0	CCBUF[1:0]		DITHERBUF[5:0]					
		15:8	CCBUF[9:2]							
		23:16	CCBUF[17:10]							
		31:24								
0x84	CCBUF5	7:0	CCBUF[1:0]		DITHERBUF[5:0]					
		15:8	CCBUF[9:2]							
		23:16	CCBUF[17:10]							
		31:24								

41.8 Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Optional write protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write Protection" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable protection is denoted by the "Enable-Protected" property in each individual register description.

41.8.1 Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized (ENABLE, SWRST)

Bit	31	30	29	28	27	26	25	24
					CPTEN3	CPTEN2	CPTEN1	CPTEN0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DMAOS							
Access	R/W							
Reset	0							

Bit	15	14	13	12	11	10	9	8
	MSYNC	ALOCK	PRESCYNC[1:0]		RUNSTDBY	PRESCALER[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		RESOLUTION[1:0]					ENABLE	SWRST
Access		R/W	R/W				R/W	R/W
Reset		0	0				0	0

Bits 24, 25, 26, 27 – CPTENx Capture Channel x Enable
These bits are used to select the capture or compare operation on channel x.
Writing a '1' to CPTENx enables capture on channel x.
Writing a '0' to CPTENx disables capture on channel x.

Bit 23 – DMAOS DMA One-Shot Trigger Mode
This bit enables the DMA One-shot Trigger Mode.
Writing a '1' to this bit will generate a DMA trigger on TCC cycle following a TCC_CTRLBSET_CMD_DMAOS command.
Writing a '0' to this bit will generate DMA triggers on each TCC cycle.

Bit 15 – MSYNC Host Synchronization (only for TCC Client instance)
This bit must be set if the TCC counting operation must be synchronized on its Host TCC.
This bit is not synchronized.

Value	Description
0	The TCC controls its own counter.
1	The counter is controlled by its Host TCC.

Bit 14 – ALOCK Auto Lock
This bit is not synchronized.

Value	Description
0	The Lock Update bit in the Control B register (CTRLB.LUPD) is not affected by overflow/underflow, and re-trigger events
1	CTRLB.LUPD is set to '1' on each overflow/underflow or re-trigger event.

Bits 13:12 – PRESCYNC[1:0] Prescaler and Counter Synchronization

These bits select if on re-trigger event, the Counter is cleared or reloaded on either the next GCLK_TCCx clock, or on the next prescaled GCLK_TCCx clock. It is also possible to reset the prescaler on re-trigger event.

These bits are not synchronized.

Value	Name	Description	
		Counter Reloaded	Prescaler
0x0	GCLK	Reload or reset Counter on next GCLK	-
0x1	PRESC	Reload or reset Counter on next prescaler clock	-
0x2	RESYNC	Reload or reset Counter on next GCLK	Reset prescaler counter
0x3	Reserved		

Bit 11 – RUNSTDBY Run in Standby

This bit is used to keep the TCC running in Standby mode.

This bit is not synchronized.

Value	Description
0	The TCC is halted in standby.
1	The TCC continues to run in standby.

Bits 10:8 – PRESCALER[2:0] Prescaler

These bits select the Counter prescaler factor.

These bits are not synchronized.

Value	Name	Description
0x0	DIV1	Prescaler: GCLK_TCCx
0x1	DIV2	Prescaler: GCLK_TCCx/2
0x2	DIV4	Prescaler: GCLK_TCCx/4
0x3	DIV8	Prescaler: GCLK_TCCx/8
0x4	DIV16	Prescaler: GCLK_TCCx/16
0x5	DIV64	Prescaler: GCLK_TCCx/64
0x6	DIV256	Prescaler: GCLK_TCCx/256
0x7	DIV1024	Prescaler: GCLK_TCCx/1024

Bits 6:5 – RESOLUTION[1:0] Dithering Resolution

These bits increase the TCC resolution by enabling the dithering options.

These bits are not synchronized.

Table 41-9. Dithering

Value	Name	Description
0x0	NONE	The dithering is disabled.
0x1	DITH4	Dithering is done every 16 PWM frames. PER[3:0] and CCx[3:0] contain dithering pattern selection.
0x2	DITH5	Dithering is done every 32 PWM frames. PER[4:0] and CCx[4:0] contain dithering pattern selection.
0x3	DITH6	Dithering is done every 64 PWM frames. PER[5:0] and CCx[5:0] contain dithering pattern selection.

Bit 1 – ENABLE Enable

Due to synchronization there is delay from writing CTRLA.ENABLE until the peripheral is enabled/ disabled. The value written to CTRLA.ENABLE will read back immediately and the ENABLE bit in the SYNCBUSY register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

Value	Description
0	The peripheral is disabled.
1	The peripheral is enabled.

Bit 0 – SWRST Software Reset

Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the TCC (except DBGCTRL) to their initial state, and the TCC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence; all other writes in the same write-operation will be discarded.

Due to synchronization there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

Value	Description
0	There is no Reset operation ongoing.
1	The Reset operation is ongoing.

41.8.2 Control B Clear

Name: CTRLBCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

This register allows the user to change this register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set (CTRLBSET) register.

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]			IDXCMD[1:0]		ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:5 – CMD[2:0] TCC Command
Writing zero to this bit group has no effect.
Writing a '1' to any of these bits will clear the pending command.

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Clear start, restart or retrigger
0x2	STOP	Force stop
0x3	UPDATE	Force update of double buffered registers
0x4	READSYNC	Force COUNT read synchronization
0x5	DMAOS	One-shot DMA trigger

Bits 4:3 – IDXCMD[1:0] Ramp Index Command
These bits can be used to force cycle A and cycle B changes in RAMP2 and RAMP2A operation.
On timer/counter update condition, the command is executed, the IDX flag in STATUS register is updated and the IDXCMD command is cleared.
Writing zero to these bits has no effect.
Writing a '1' to any of these bits will clear the pending command.

Value	Name	Description
0x0	DISABLE	DISABLE Command disabled: IDX toggles between cycles A and B
0x1	SET	Set IDX: cycle B will be forced in the next cycle
0x2	CLEAR	Clear IDX: cycle A will be forced in next cycle
0x3	HOLD	Hold IDX: the next cycle will be the same as the current cycle.

Bit 2 – ONESHOT One-Shot
This bit controls one-shot operation of the TCC. When one-shot operation is enabled, the TCC will stop counting on the next overflow/underflow condition or on a stop command.
Writing a '0' to this bit has no effect
Writing a '1' to this bit will disable the one-shot operation.

Value	Description
0	The TCC will update the counter value on overflow/underflow condition and continue operation.
1	The TCC will stop counting on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update
This bit controls the update operation of the TCC buffered registers.
When CTRLB.LUPD is cleared, the hardware UPDATE registers with value from their buffered registers is enabled.
This bit has no effect when input capture operation is enabled.
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will enable the registers updates on hardware UPDATE condition.

Value	Description
0	The CCBx, PERB, PGVB, and PGEB buffer registers values *are* copied into the corresponding CCx, PER, PGV, and PGE registers on hardware update condition.
1	The CCBx, PERB, PGVB, and PGEB buffer registers values are *not* copied into the corresponding CCx, PER, PGV, and PGE registers on hardware update condition.

Bit 0 – DIR Counter Direction

This bit is used to change the direction of the counter.
Writing a '0' to this bit has no effect
Writing a '1' to this bit will clear the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

41.8.3 Control B Set

Name: CTRLBSET
Offset: 0x05
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

This register allows the user to change this register without doing a read-modify-write operation. Changes in this register will also be reflected in the Control B Set (CTRLBCLR) register.

Bit	7	6	5	4	3	2	1	0
	CMD[2:0]			IDXCMD[1:0]		ONESHOT	LUPD	DIR
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:5 – CMD[2:0] TCC Command
These bits can be used for software control of re-triggering and stop commands of the TCC. When a command has been executed, the CMD bit field will be read back as zero. The commands are executed on the next prescaled GCLK_TCCx clock cycle.
Writing zero to this bit group has no effect
Writing a valid value to this bit group, as shown in the following table, will set the associated command.

Value	Name	Description
0x0	NONE	No action
0x1	RETRIGGER	Force start, restart or retrigger
0x2	STOP	Force stop
0x3	UPDATE	Force update of double buffered registers
0x4	READSYNC	Force a read synchronization of COUNT
0x5	DMAOS	One-shot DMA trigger

Bits 4:3 – IDXCMD[1:0] Ramp Index Command
These bits can be used to force cycle A and cycle B changes in RAMP2 and RAMP2A operation.
On timer/counter update condition, the command is executed, the IDX flag in STATUS register is updated and the IDXCMD command is cleared.
Writing a zero to these bits has no effect.
Writing a valid value to these bits will set a command.

Value	Name	Description
0x0	DISABLE	Command disabled: IDX toggles between cycles A and B
0x1	SET	Set IDX: cycle B will be forced in the next cycle
0x2	CLEAR	Clear IDX: cycle A will be forced in next cycle
0x3	HOLD	Hold IDX: the next cycle will be the same as the current cycle.

Bit 2 – ONESHOT One-Shot
This bit controls one-shot operation of the TCC. When in one-shot operation, the TCC will stop counting on the next overflow/underflow condition or a stop command.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will enable the one-shot operation.

Value	Description
0	The TCC will count continuously.
1	The TCC will stop counting on the next underflow/overflow condition.

Bit 1 – LUPD Lock Update
This bit controls the update operation of the TCC buffered registers.

When CTRLB.LUPD is set, the hardware UPDATE registers with value from their buffered registers is disabled. Disabling the update ensures that all buffer registers are valid before an hardware update is performed. After all the buffer registers are loaded correctly, the buffered registers can be unlocked.
This bit has no effect when input capture operation is enabled.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will disable the registers updates on hardware UPDATE condition.

Value	Description
0	The CCBx, PERB, PGVB, and PGEB buffer registers values *are* copied into the corresponding CCx, PER, PGV, and PGE registers on hardware update condition.
1	The CCBx, PERB, PGVB, and PGEB buffer registers values are *not* copied into CCx, PER, PGV, and PGE registers on hardware update condition.

Bit 0 – DIR Counter Direction
This bit is used to change the direction of the counter.
Writing a '0' to this bit has no effect
Writing a '1' to this bit will clear the bit and make the counter count up.

Value	Description
0	The timer/counter is counting up (incrementing).
1	The timer/counter is counting down (decrementing).

41.8.4 Synchronization Busy

Name: SYNCBUSY
Offset: 0x08
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
			CC5	CC4	CC3	CC2	CC1	CC0
Access			R	R	R	R	R	R
Reset			0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PER	WAVE	PATT	COUNT	STATUS	CTRLB	ENABLE	SWRST
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 8, 9, 10, 11, 12, 13 – CC Compare/Capture Channel x Synchronization Busy

This bit is cleared when the synchronization of the Compare/Capture Channel x register between the clock domains is complete.

This bit is set when the synchronization of the Compare/Capture Channel x register between clock domains is started.

The CCx bit is available only for existing Compare/Capture Channels. For details on the CC channels number, refer to each TCC feature list.

This bit is set when the synchronization of the CCx register between clock domains is started.

Bit 7 – PER PER Synchronization Busy

This bit is cleared when the synchronization of the PER register between the clock domains is complete.

This bit is set when the synchronization of the PER register between clock domains is started.

Bit 6 – WAVE WAVE Synchronization Busy

This bit is cleared when the synchronization of the WAVE register between the clock domains is complete.

This bit is set when the synchronization of the WAVE register between clock domains is started.

Bit 5 – PATT PATT Synchronization Busy

This bit is cleared when the synchronization of the PATTERN register between the clock domains is complete.

This bit is set when the synchronization of the PATTERN register between clock domains is started.

Bit 4 – COUNT COUNT Synchronization Busy
This bit is cleared when the synchronization of the COUNT register between the clock domains is complete.
This bit is set when the synchronization of the COUNT register between clock domains is started.

Bit 3 – STATUS STATUS Synchronization Busy
This bit is cleared when the synchronization of the STATUS register between the clock domains is complete.
This bit is set when the synchronization of the STATUS register between clock domains is started.

Bit 2 – CTRLB CTRLB Synchronization Busy
This bit is cleared when the synchronization of the CTRLB register between the clock domains is complete.
This bit is set when the synchronization of the CTRLB register between clock domains is started.

Bit 1 – ENABLE ENABLE Synchronization Busy
This bit is cleared when the synchronization of the ENABLE bit between the clock domains is complete.
This bit is set when the synchronization of the ENABLE bit between clock domains is started.

Bit 0 – SWRST SWRST Synchronization Busy
This bit is cleared when the synchronization of the SWRST bit between the clock domains is complete.
This bit is set when the synchronization of the SWRST bit between clock domains is started.
Note: During a SWRST, access to registers/bits without SWRST are disallowed until SYNCBUSY.SWRST is cleared by hardware.

41.8.5 Fault Control A and B

Name: FCTRLn
Offset: 0x0C + n*0x04 [n=0..1]
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
					FILTERVAL[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
	BLANKVAL[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	BLANKPRESC	CAPTURE[2:0]			CHSEL[1:0]		HALT[1:0]	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	RESTART	BLANK[1:0]		QUAL	KEEP		SRC[1:0]	
Access	R/W	R/W	R/W	R/W	R/W		R/W	R/W
Reset	0	0	0	0	0		0	0

Bits 27:24 – FILTERVAL[3:0] Recoverable Fault n Filter Value
These bits define the filter value applied on MCEx (x=0,1) event input line. The value must be set to zero when MCEx event is used as synchronous event.

Bits 23:16 – BLANKVAL[7:0] Recoverable Fault n Blanking Value
These bits determine the duration of the blanking of the fault input source. Activation and edge selection of the blank filtering are done by the BLANK bits (FCTRLn.BLANK).
When enabled, the fault input source is internally disabled for BLANKVAL* prescaled GCLK_TCCx periods after the detection of the waveform edge.

Bit 15 – BLANKPRESC Recoverable Fault n Blanking Value Prescaler
This bit enables a factor 64 prescaler factor on used as base frequency of the BLANKVAL value.

Value	Description
0	Blank time is BLANKVAL* prescaled GCLK_TCCx.
1	Blank time is BLANKVAL* 64 * prescaled GCLK_TCCx.

Bits 14:12 – CAPTURE[2:0] Recoverable Fault n Capture Action
These bits select the capture and Fault n interrupt/event conditions.

Table 41-10. Fault n Capture Action

Value	Name	Description
0x0	DISABLE	Capture on valid recoverable Fault n is disabled
0x1	CAPT	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAG.FAULTn flag rises on each new captured value.

...........continued

Value	Name	Description
0x2	CAPTMIN	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0], if COUNT value is lower than the last stored capture value (CC). INTFLAG.FAULTn flag rises on each local minimum detection.
0x3	CAPTMAX	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0], if COUNT value is higher than the last stored capture value (CC). INTFLAG.FAULTn flag rises on each local maximun detection.
0x4	LOCMIN	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAG.FAULTn flag rises on each local minimum value detection.
0x5	LOCMAX	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAG.FAULTn flag rises on each local maximun detection.
0x6	DERIV0	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAG.FAULTn flag rises on each local maximun or minimum detection.
0x7	CAPTMARK	Capture with ramp index as MSB value.

Bits 11:10 – CHSEL[1:0] Recoverable Fault n Capture Channel

These bits select the channel for capture operation triggered by recoverable Fault n.

Value	Name	Description
0x0	CC0	Capture value stored into CC0
0x1	CC1	Capture value stored into CC1
0x2	CC2	Capture value stored into CC2
0x3	CC3	Capture value stored into CC3

Bits 9:8 – HALT[1:0] Recoverable Fault n Halt Operation

These bits select the halt action for recoverable Fault n.

Value	Name	Description
0x0	DISABLE	Halt action disabled
0x1	HW	Hardware halt action
0x2	SW	Software halt action
0x3	NR	Non-recoverable fault

Bit 7 – RESTART Recoverable Fault n Restart

Setting this bit enables restart action for Fault n.

Value	Description
0	Fault n restart action is disabled.
1	Fault n restart action is enabled.

Bits 6:5 – BLANK[1:0] Recoverable Fault n Blanking Operation

These bits, select the blanking start point for recoverable Fault n.

Value	Name	Description
0x0	START	Blanking applied from start of the Ramp period
0x1	RISE	Blanking applied from rising edge of the waveform output
0x2	FALL	Blanking applied from falling edge of the waveform output
0x3	BOTH	Blanking applied from each toggle of the waveform output

Bit 4 – QUAL Recoverable Fault n Qualification

Setting this bit enables the recoverable Fault n input qualification.

Value	Description
0	The recoverable Fault n input is not disabled on CMPx value condition.
1	The recoverable Fault n input is disabled when output signal is at inactive level (CMPx == 0).

Bit 3 – KEEP Recoverable Fault n Keep

Setting this bit enables the Fault n keep action.

Value	Description
0	The Fault n state is released as soon as the recoverable Fault n is released.
1	The Fault n state is released at the end of TCC cycle.

Bits 1:0 – SRC[1:0] Recoverable Fault n Source

These bits select the TCC event input for recoverable Fault n.
Event system channel connected to MCEx event input, must be configured to route the event asynchronously, when used as a recoverable Fault n input.

Value	Name	Description
0x0	DISABLE	Fault input disabled
0x1	ENABLE	MCEx (x=0,1) event input
0x2	INVERT	Inverted MCEx (x=0,1) event input
0x3	ALTFAULT	Alternate fault (A or B) state at the end of the previous period.

41.8.6 Waveform Extension Control

Name: WEXCTRL
Offset: 0x14
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
	DTHS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	DTLS[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
					DTIEN3	DTIEN2	DTIEN1	DTIEN0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
							OTMX[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 31:24 – DTHS[7:0] Dead-Time High Side Outputs Value
This register holds the number of GCLK_TCCx clock cycles for the dead-time high side.

Bits 23:16 – DTLS[7:0] Dead-time Low Side Outputs Value
This register holds the number of GCLK_TCCx clock cycles for the dead-time low side.

Bits 8, 9, 10, 11 – DTIENx Dead-time Insertion Generator x Enable
Setting any of these bits enables the dead-time insertion generator for the corresponding output matrix. This will override the output matrix [x] and [x+WO_NUM/2], with the low side and high side waveform respectively.

Value	Description
0	No dead-time insertion override.
1	Dead time insertion override on signal outputs[x] and [x+WO_NUM/2], from matrix outputs[x] signal.

Bits 1:0 – OTMX[1:0] Output Matrix
These bits define the matrix routing of the TCC waveform generation outputs to the port pins, according to Waveform Extension.

41.8.7 Driver Control

Name: DRVCTRL
Offset: 0x18
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
	FILTERVAL1[3:0]				FILTERVAL0[3:0]			
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	INVEN7	INVEN6	INVEN5	INVEN4	INVEN3	INVEN2	INVEN1	INVEN0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	NRV7	NRV6	NRV5	NRV4	NRV3	NRV2	NRV1	NRV0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	NRE7	NRE6	NRE5	NRE4	NRE3	NRE2	NRE1	NRE0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:28 – FILTERVAL1[3:0] Non-Recoverable Fault Input 1 Filter Value
These bits define the filter value applied on TCE1 event input line. When the TCE1 event input line is configured as a synchronous event, this value must be 0x0.

Bits 27:24 – FILTERVAL0[3:0] Non-Recoverable Fault Input 0 Filter Value
These bits define the filter value applied on TCE0 event input line. When the TCE0 event input line is configured as a synchronous event, this value must be 0x0.

Bits 16, 17, 18, 19, 20, 21, 22, 23 – INVENx Waveform Output x Inversion
These bits are used to select inversion on the output of channel x.
Writing a '1' to INVENx inverts output from WO[x].
Writing a '0' to INVENx disables inversion of output from WO[x].

Bits 8, 9, 10, 11, 12, 13, 14, 15 – NRVx NRVx Non-Recoverable State x Output Value
These bits define the value of the enabled override outputs, under non-recoverable fault condition.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – NREx Non-Recoverable State x Output Enable
These bits enable the override of individual outputs by NRVx value, under non-recoverable fault condition.

Value	Description
0	Non-recoverable fault tri-state the output.
1	Non-recoverable faults set the output to NRVx level.

41.8.8 Debug control

Name: DBGCTRL
Offset: 0x1E
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
						FDDBD		DBGRUN
Access						R/W		R/W
Reset						0		0

Bit 2 – FDDBD Fault Detection on Debug Break Detection

This bit is not affected by software Reset and must not be changed by software while the TCC is enabled.

By default this bit is zero, and the on-chip debug (OCD) fault protection is disabled. When this bit is written to '1', OCD break request from the OCD system will trigger non-recoverable fault. When this bit is set, OCD fault protection is enabled and OCD break request from the OCD system will trigger a non-recoverable fault.

Value	Description
0	No faults are generated when TCC is halted in Debug mode.
1	A non recoverable fault is generated and FAULTD flag is set when TCC is halted in Debug mode.

Bit 0 – DBGRUN Debug Running State

This bit is not affected by software Reset and must not be changed by software while the TCC is enabled.

Value	Description
0	The TCC is halted when the device is halted in Debug mode.
1	The TCC continues normal operation when the device is halted in Debug mode.

41.8.9 Event Control

Name: EVCTRL
Offset: 0x20
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected

Bit	31	30	29	28	27	26	25	24
					MCEO3	MCEO2	MCEO1	MCEO0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
					MCEI3	MCEI2	MCEI1	MCEI0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	TCEI1	TCEI0	TCINV1	TCINV0		CNTEO	TRGEO	OVFEO
Access	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset	0	0	0	0		0	0	0

Bit	7	6	5	4	3	2	1	0
	CNTSEL[1:0]		EVACT1[2:0]			EVACT0[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 24, 25, 26, 27 – MCEO Match or Capture Channel x Event Output Enable

These bits control if the match/capture event on channel x is enabled and will be generated for every match or capture.

Value	Description
0	Match/capture x event is disabled and will not be generated.
1	Match/capture x event is enabled and will be generated for every compare/capture on channel x.

Bits 16, 17, 18, 19 – MCEI Match or Capture Channel x Event Input Enable

These bits indicate if the match/capture x incoming event is enabled
These bits are used to enable match or capture input events to the CCx channel of TCC.

Value	Description
0	Incoming events are disabled.
1	Incoming events are enabled.

Bits 14, 15 – TCEIx Timer/Counter Event Input x Enable

This bit is used to enable input event x to the TCC.

Value	Description
0	Incoming event x is disabled.
1	Incoming event x is enabled.

Bits 12, 13 – TCINVx Timer/Counter Event x Invert Enable

This bit inverts the event x input.

Value	Description
0	Input event source x is not inverted.

Value	Description
1	Input event source x is inverted.

Bit 10 – CNTEO Timer/Counter Event Output Enable

This bit is used to enable the counter cycle event. When enabled, an event will be generated on begin or end of counter cycle depending of CNTSEL[1:0] settings.

Value	Description
0	Counter cycle output event is disabled and will not be generated.
1	Counter cycle output event is enabled and will be generated depend of CNTSEL[1:0] value.

Bit 9 – TRGEO Retrigger Event Output Enable

This bit is used to enable the counter retrigger event. When enabled, an event will be generated when the counter retriggers operation.

Value	Description
0	Counter retrigger event is disabled and will not be generated.
1	Counter retrigger event is enabled and will be generated for every counter retrigger.

Bit 8 – OVFEO Overflow/Underflow Event Output Enable

This bit is used to enable the overflow/underflow event. When enabled an event will be generated when the counter reaches the TOP or the ZERO value.

Value	Description
0	Overflow/underflow counter event is disabled and will not be generated.
1	Overflow/underflow counter event is enabled and will be generated for every counter overflow/underflow.

Bits 7:6 – CNTSEL[1:0] Timer/Counter Interrupt and Event Output Selection

These bits define on which part of the counter cycle the counter event output is generated.

Value	Name	Description
0x0	BEGIN	An interrupt/event is generated at begin of each counter cycle
0x1	END	An interrupt/event is generated at end of each counter cycle
0x2	BETWEEN	An interrupt/event is generated between each counter cycle.
0x3	BOUNDARY	An interrupt/event is generated at begin of first counter cycle, and end of last counter cycle.

Bits 5:3 – EVACT1[2:0] Timer/Counter Event Input 1 Action

These bits define the action the TCC will perform on TCE1 event input.

Value	Name	Description
0x0	OFF	Event action disabled.
0x1	RETRIGGER	Start, restart or re-trigger TC on event
0x2	DIR (asynch)	Direction control
0x3	STOP	Stop TC on event
0x4	DEC	Decrement TC on event
0x5	PPW	Period captured into CC0 Pulse Width on CC1
0x6	PWP	Period captured into CC1 Pulse Width on CC0
0x7	FAULT	Non-recoverable Fault

Bits 2:0 – EVACT0[2:0] Timer/Counter Event Input 0 Action

These bits define the action the TCC will perform on TCE0 event input 0.

Value	Name	Description
0x0	OFF	Event action disabled.
0x1	RETRIGGER	Start, restart or re-trigger TC on event
0x2	COUNTEV	Count on event.
0x3	START	Start TC on event
0x4	INC	Increment TC on EVENT

Value	Name	Description
0x5	COUNT (async)	Count on active state of asynchronous event
0x6	STAMP	Capture overflow times (Max value)
0x7	FAULT	Non-recoverable Fault

41.8.10 Interrupt Enable Clear

Name: INTENCLR
Offset: 0x24
Reset: 0x00000000
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set (INTENSET) register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					MCx3	MCx2	MCx1	MCx0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					ERR	CNT	TRG	OVF
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 16, 17, 18, 19 – MCx Match or Capture Channel x Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the corresponding Match or Capture Channel x Interrupt Disable/Enable bit, which disables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 15 – FAULT1 Non-Recoverable Fault x Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Non-Recoverable Fault x Interrupt Disable/Enable bit, which disables the Non-Recoverable Fault x interrupt.

Value	Description
0	The Non-Recoverable Fault x interrupt is disabled.
1	The Non-Recoverable Fault x interrupt is enabled.

Bit 14 – FAULT0 Non-Recoverable Fault x Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Non-Recoverable Fault x Interrupt Disable/Enable bit, which disables the Non-Recoverable Fault x interrupt.

Value	Description
0	The Non-Recoverable Fault x interrupt is disabled.
1	The Non-Recoverable Fault x interrupt is enabled.

Bit 13 – FAULTB Recoverable Fault B Interrupt Enable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Recoverable Fault B Interrupt Disable/Enable bit, which disables the Recoverable Fault B interrupt.

Value	Description
0	The Recoverable Fault B interrupt is disabled.
1	The Recoverable Fault B interrupt is enabled.

Bit 12 – FAULTA Recoverable Fault A Interrupt Enable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Recoverable Fault A Interrupt Disable/Enable bit, which disables the Recoverable Fault A interrupt.

Value	Description
0	The Recoverable Fault A interrupt is disabled.
1	The Recoverable Fault A interrupt is enabled.

Bit 11 – DFS Non-Recoverable Debug Fault Interrupt Enable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Debug Fault State Interrupt Disable/Enable bit, which disables the Debug Fault State interrupt.

Value	Description
0	The Debug Fault State interrupt is disabled.
1	The Debug Fault State interrupt is enabled.

Bit 10 – UFS Non-Recoverable Update Fault Interrupt Enable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Non-Recoverable Update Fault Interrupt Disable/Enable bit, which disables the Non-Recoverable Update Fault interrupt.

Value	Description
0	The Non-Recoverable Update Fault interrupt is disabled.
1	The Non-Recoverable Update Fault interrupt is enabled.

Bit 3 – ERR Error Interrupt Enable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Error Interrupt Disable/Enable bit, which disables the Compare interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 2 – CNT Counter Interrupt Enable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Counter Interrupt Disable/Enable bit, which disables the Counter interrupt.

Value	Description
0	The Counter interrupt is disabled.
1	The Counter interrupt is enabled.

Bit 1 – TRG Retrigger Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Retrigger Interrupt Disable/Enable bit, which disables the Retrigger interrupt.

Value	Description
0	The Retrigger interrupt is disabled.
1	The Retrigger interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Enable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Overflow Interrupt Disable/Enable bit, which disables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

41.8.11 Interrupt Enable Set

Name: INTENSET
Offset: 0x28
Reset: 0x00000000
Property: PAC Write-Protection

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
					MC3	MC2	MC1	MC0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		

Bit	7	6	5	4	3	2	1	0
					ERR	CNT	TRG	OVF
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 16, 17, 18, 19 – MC Match or Capture Channel x Interrupt Enable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the corresponding Match or Capture Channel x Interrupt Disable/Enable bit, which enables the Match or Capture Channel x interrupt.

Value	Description
0	The Match or Capture Channel x interrupt is disabled.
1	The Match or Capture Channel x interrupt is enabled.

Bit 15 – FAULT1 Non-Recoverable Fault x Interrupt Enable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Non-Recoverable Fault x Interrupt Disable/Enable bit, which enables the Non-Recoverable Fault x interrupt.

Value	Description
0	The Non-Recoverable Fault x interrupt is disabled.
1	The Non-Recoverable Fault x interrupt is enabled.

Bit 14 – FAULT0 Non-Recoverable Fault x Interrupt Enable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Non-Recoverable Fault x Interrupt Disable/Enable bit, which disables the Non-Recoverable Fault x interrupt.

Value	Description
0	The Non-Recoverable Fault x interrupt is disabled.
1	The Non-Recoverable Fault x interrupt is enabled.

Bit 13 – FAULTB Recoverable Fault B Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Recoverable Fault B Interrupt Disable/Enable bit, which enables the Recoverable Fault B interrupt.

Value	Description
0	The Recoverable Fault B interrupt is disabled.
1	The Recoverable Fault B interrupt is enabled.

Bit 12 – FAULTA Recoverable Fault A Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Recoverable Fault A Interrupt Disable/Enable bit, which enables the Recoverable Fault A interrupt.

Value	Description
0	The Recoverable Fault A interrupt is disabled.
1	The Recoverable Fault A interrupt is enabled.

Bit 11 – DFS Non-Recoverable Debug Fault Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Debug Fault State Interrupt Disable/Enable bit, which enables the Debug Fault State interrupt.

Value	Description
0	The Debug Fault State interrupt is disabled.
1	The Debug Fault State interrupt is enabled.

Bit 10 – UFS Non-Recoverable Update Fault Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Non-Recoverable Update Fault Interrupt Disable/Enable bit, which disables the Non-Recoverable Update Fault interrupt.

Value	Description
0	The Non-Recoverable Update Fault interrupt is disabled.
1	The Non-Recoverable Update Fault interrupt is enabled.

Bit 3 – ERR Error Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Error Interrupt Disable/Enable bit, which enables the Compare interrupt.

Value	Description
0	The Error interrupt is disabled.
1	The Error interrupt is enabled.

Bit 2 – CNT Counter Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Retrigger Interrupt Disable/Enable bit, which enables the Counter interrupt.

Value	Description
0	The Counter interrupt is disabled.
1	The Counter interrupt is enabled.

Bit 1 – TRG Retrigger Interrupt Enable

Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Retrigger Interrupt Disable/Enable bit, which enables the Retrigger interrupt.

Value	Description
0	The Retrigger interrupt is disabled.
1	The Retrigger interrupt is enabled.

Bit 0 – OVF Overflow Interrupt Enable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will set the Overflow Interrupt Disable/Enable bit, which enables the Overflow interrupt request.

Value	Description
0	The Overflow interrupt is disabled.
1	The Overflow interrupt is enabled.

41.8.12 Interrupt Flag Status and Clear

Name: INTFLAG
Offset: 0x2C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	23	22	21	20	19	18	17	16
					MC3	MC2	MC1	MC0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0
Bit	15	14	13	12	11	10	9	8
	FAULT1	FAULT0	FAULTB	FAULTA	DFS	UFS		
Access	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0		
Bit	7	6	5	4	3	2	1	0
					ERR	CNT	TRG	OVF
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 16, 17, 18, 19 – MC Match or Capture Channel x Interrupt Flag

This flag is set on the next CLK_TCC_COUNT cycle after a match with the compare condition or once the CCx register contains a valid capture value.
Writing a '0' to one of these bits has no effect.
Writing a '1' to one of these bits will clear the corresponding Match or Capture Channel x interrupt flag.
In the Capture operation, this flag is automatically cleared when the CCx register is read.

Bit 15 – FAULT1 Non-Recoverable Fault x Interrupt Flag

This flag is set on the next CLK_TCC_COUNT cycle after a Non-Recoverable Fault x occurs.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Non-Recoverable Fault x interrupt flag.

Bit 14 – FAULT0 Non-Recoverable Fault x Interrupt Enable

Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Non-Recoverable Fault x Interrupt Disable/Enable bit, which disables the Non-Recoverable Fault x interrupt.

Value	Description
0	The Non-Recoverable Fault x interrupt is disabled.
1	The Non-Recoverable Fault x interrupt is enabled.

Bit 13 – FAULTB Recoverable Fault B Interrupt Flag

This flag is set on the next CLK_TCC_COUNT cycle after a Recoverable Fault B occurs.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Recoverable Fault B interrupt flag.

Bit 12 – FAULTA Recoverable Fault A Interrupt Flag
This flag is set on the next CLK_TCC_COUNT cycle after a Recoverable Fault B occurs.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Recoverable Fault B interrupt flag.

Bit 11 – DFS Non-Recoverable Debug Fault State Interrupt Flag
This flag is set on the next CLK_TCC_COUNT cycle after a Debug Fault State occurs.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Debug Fault State interrupt flag.

Bit 10 – UFS Non-Recoverable Update Fault Interrupt Enable
This flag is set when the RAMP index changes and the Lock Update bit is set (CTRLBSET.LUPD).
Writing a '0' to this bit has no effect.
Writing a '1' to this bit will clear the Non-Recoverable Update Fault Interrupt Disable/Enable bit, which disables the Non-Recoverable Update Fault interrupt.

Value	Description
0	The Non-Recoverable Update Fault interrupt is disabled.
1	The Non-Recoverable Update Fault interrupt is enabled.

Bit 3 – ERR Error Interrupt Flag
This flag is set if a new capture occurs on a channel when the corresponding Match or Capture Channel x interrupt flag is one. In which case, there is nowhere to store the new capture.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the error interrupt flag.

Bit 2 – CNT Counter Interrupt Flag
This flag is set on the next CLK_TCC_COUNT cycle after a counter event occurs.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the CNT interrupt flag.

Bit 1 – TRG Retrigger Interrupt Flag
This flag is set on the next CLK_TCC_COUNT cycle after a counter retrigger occurs.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the re-trigger interrupt flag.

Bit 0 – OVF Overflow Interrupt Flag
This flag is set on the next CLK_TCC_COUNT cycle after an overflow condition occurs.
Writing a '0' to this bit has no effect.
Writing a '1' to this bit clears the Overflow interrupt flag.

41.8.13 Status

Name: STATUS
Offset: 0x30
Reset: 0x00000001
Property: -

Bit	31	30	29	28	27	26	25	24
					CMP3	CMP2	CMP1	CMP0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
					CCBUFV3	CCBUFV2	CCBUFV1	CCBUFV0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	15	14	13	12	11	10	9	8
	FAULT1	FAULT0	FAULTB	FAULTA	FAULT1IN	FAULT0IN	FAULTBIN	FAULTAIN
Access	R/W	R/W	R/W	R/W	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PERBUFV		PATTBUFV	SLAVE	DFS	UFS	IDX	STOP
Access	R/W		R/W	R	R/W	R/W	R	R
Reset	0		0	0	0	0	0	1

Bits 24, 25, 26, 27 – CMP Channel x Compare Value

This bit reflects the channel x output compare value.

Value	Description
0	Channel compare output value is 0.
1	Channel compare output value is 1.

Bits 16, 17, 18, 19 – CCBUFV Channel x Compare or Capture Buffer Valid

For a compare channel, this bit is set when a new value is written to the corresponding CCBUFx register. The bit is cleared either by writing a '1' to the corresponding location when CTRLB.LUPD is set, or automatically on an UPDATE condition.

For a capture channel, the bit is set when a valid capture value is stored in the CCBUFx register. The bit is automatically cleared when the CCx register is read.

Bits 14, 15 – FAULT Non-recoverable Fault x State

This bit is set by hardware as soon as non-recoverable Fault x condition occurs.

This bit is cleared by writing a one to this bit and when the corresponding FAULTxIN status bit is low. Once this bit is clear, the timer/counter will restart from the last COUNT value. To restart the timer/counter from BOTTOM, the timer/counter restart command must be executed before clearing the corresponding STATEx bit. For further details on timer/counter commands, refer to the available commands description (CTRLBSET.CMD).

Bit 13 – FAULTB Recoverable Fault B State

This bit is set by hardware as soon as recoverable Fault B condition occurs.

This bit can be cleared by hardware when the Fault B action is resumed or by writing a '1' to this bit when the corresponding FAULTBIN bit is low. If the software halt command is enabled (FAULTB.HALT=SW), clearing this bit will release the timer/counter.

Bit 12 – FAULTA Recoverable Fault A State

This bit is set by hardware as soon as the recoverable Fault A condition occurs.
This bit can be cleared by hardware when the Fault A action is resumed or by writing a '1' to this bit when the corresponding FAULTAIN bit is low. If the software halt command is enabled (FAULTA.HALT=SW), clearing this bit will release the timer/counter.

Bit 11 – FAULT1IN Non-Recoverable Fault 1 Input

This bit is set while an active Non-Recoverable Fault 1 input is present.

Bit 10 – FAULT0IN Non-Recoverable Fault 0 Input

This bit is set while an active Non-Recoverable Fault 0 input is present.

Bit 9 – FAULTBIN Recoverable Fault B Input

This bit is set while an active Recoverable Fault B input is present.

Bit 8 – FAULTAIN Recoverable Fault A Input

This bit is set while an active Recoverable Fault A input is present.

Bit 7 – PERBUFV Period Buffer Valid

This bit is set when a new value is written to the PERBUF register. This bit is automatically cleared by hardware on the UPDATE condition when CTRLB.LUPD is set or by writing a '1' to this bit.

Bit 5 – PATTBUFV Pattern Generator Value Buffer Valid

This bit is set when a new value is written to the PATTBUF register. This bit is automatically cleared by hardware on the UPDATE condition when CTRLB.LUPD is set or by writing a '1' to this bit.

Bit 4 – SLAVE Client

This bit is set when TCC is set in Client mode. This bit follows the CTRLA.MSYNC bit state.

Bit 3 – DFS Debug Fault State

This bit is set by hardware in Debug mode when the DDBGCTRL.FDDBD bit is set. The bit is cleared by writing a '1' to this bit and when the TCC is not in Debug mode.
When the bit is set, the counter is halted and the Waveforms state depends on the DRVCTRL.NRE and DRVCTRL.NRV registers.

Bit 2 – UFS Non-recoverable Update Fault State

This bit is set by hardware when the RAMP index changes and the Lock Update bit is set (CTRLBSET.LUPD). The bit is cleared by writing a one to this bit.
When the bit is set, the waveforms state depends on the DRVCTRL.NRE and DRVCTRL.NRV registers.

Bit 1 – IDX Ramp Index

In RAMP2 and RAMP2A operation, the bit is cleared during the cycle A and set during the cycle B. In RAMP1 operation, the bit always reads zero. See *Ramp Operations* from Related Links..

Bit 0 – STOP Stop

This bit is set when the TCC is disabled either on a STOP command or on an UPDATE condition when One-Shot operation mode is enabled (CTRLBSET.ONESHOT=1).
This bit is clear on the next incoming counter increment or decrement.

Value	Description
0	Counter is running.
1	Counter is stopped.

Related Links

Ramp Operations

41.8.14 Counter Value

Name: COUNT
Offset: 0x34
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Note: Prior to any read access, this register must be synchronized by user by writing the according TCC Command value to the Control B Set register (CTRLBSET.CMD=READSYNC).

Bit	31	30	29	28	27	26	25	24
Access								
Reset								
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
	COUNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	COUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:0 – COUNT[23:0] Counter Value
These bits hold the value of the Counter register.
Note: When the TCC is configured as 16-bit timer/counter, the excess bits are read zero.

Note: This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0 (depicted)
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6

41.8.15 Pattern

Name: PATT
Offset: 0x38
Reset: 0x0000
Property: Write-Synchronized

Bit	15	14	13	12	11	10	9	8
	PGV7	PGV6	PGV5	PGV4	PGV3	PGV2	PGV1	PGV0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PGE7	PGE6	PGE5	PGE4	PGE3	PGE2	PGE1	PGE0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 8, 9, 10, 11, 12, 13, 14, 15 – PGV Pattern Generation Output Value
This register holds the values of pattern for each waveform output.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PGE Pattern Generation Output Enable
This register holds the enable status of pattern generation for each waveform output. A bit written to '1' will override the corresponding SWAP output with the corresponding PGVn value.

41.8.16 Waveform

Name: WAVE
Offset: 0x3C
Reset: 0x00000000
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
					SWAP3	SWAP2	SWAP1	SWAP0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	23	22	21	20	19	18	17	16
			POL5	POL4	POL3	POL2	POL1	POL0
Access			R/W	R/W	R/W	R/W	R/W	R/W
Reset			0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
					CICCEN3	CICCEN2	CICCEN1	CICCEN0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CIPEREN		RAMP[1:0]			WAVEGEN[2:0]		
Access	R/W		R/W	R/W		R/W	R/W	R/W
Reset	0		0	0		0	0	0

Bits 24, 25, 26, 27 – SWAP Swap DTI Output Pair x
Setting these bits enables the output swap of DTI outputs [x] and [x+WO_NUM/2]. Note, the DTIxEN settings will not affect the swap operation.

Bits 16, 17, 18, 19, 20, 21 – POL Channel Polarity x
Setting these bits enables the output polarity in single-slope and dual-slope PWM operations.

Value	Name	Description
0	(single-slope PWM waveform generation)	Compare output is initialized to ~DIR and set to DIR when the TCC counter matches the CCx value
1	(single-slope PWM waveform generation)	Compare output is initialized to DIR and set to ~DIR when the TCC counter matches the CCx value.
0	(dual-slope PWM waveform generation)	Compare output is set to ~DIR when the TCC counter matches the CCx value
1	(dual-slope PWM waveform generation)	Compare output is set to DIR when the TCC counter matches the CCx value.

Bits 8, 9, 10, 11 – CICCEN Circular CC Enable x
Setting this bit enables the compare circular buffer option on the first four Compare/Capture channels. When the bit is set, the CCx register value is copied-back into the CCx register on the UPDATE condition.

Bit 7 – CIPEREN Circular Period Enable
Setting this bit enables the period circular buffer option. When the bit is set, the PER register value is copied-back into the PERB register on UPDATE condition.

Bits 5:4 – RAMP[1:0] Ramp Operation
These bits select the Ramp operation (RAMP). These bits are not synchronized.

Value	Name	Description
0x0	RAMP1	RAMP1 operation
0x1	RAMP2A	Alternative RAMP2 operation
0x2	RAMP2	RAMP2 operation
0x3	RAMP2C	Critical RAMP2 operation

Bits 2:0 – WAVEGEN[2:0] Waveform Generation Operation

These bits select the waveform generation operation. The settings impact the top value and control if the frequency or PWM waveform generation must be used. These bits are not synchronized.

Value	Name	Description						
		Operation	Top	Update	Waveform Output On Match	Waveform Output On Update	OVFIF/Event Up Down	
0x0	NFRQ	Normal Frequency	PER	TOP/Zero	Toggle	Stable	TOP	Zero
0x1	MFRQ	Match Frequency	CC0	TOP/Zero	Toggle	Stable	TOP	Zero
0x2	NPWM	Normal PWM	PER	TOP/Zero	Set	Clear	TOP	Zero
0x3	Reserved	—	—	—	—	—	—	—
0x4	DSCRITICAL	Dual-slope PWM	PER	Zero	~DIR	Stable	—	Zero
0x5	DSBOTTOM	Dual-slope PWM	PER	Zero	~DIR	Stable	—	Zero
0x6	DSBOTH	Dual-slope PWM	PER	TOP & Zero	~DIR	Stable	TOP	Zero
0x7	DSTOP	Dual-slope PWM	PER	Zero	~DIR	Stable	TOP	—

41.8.17 Period Value

Name: PER
Offset: 0x40
Reset: 0xFFFFFFFF
Property: Write-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	PER[17:10]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	PER[9:2]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	PER[1:0]		DITHER[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 23:6 – PER[17:0] Period Value

These bits hold the value of the TCC period count.

Note: When the TCC is configured as 16-bit timer/counter, the excess bits are read zero.

Note: This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6 (depicted)

Bits 5:0 – DITHER[5:0] Dithering Cycle Number

These bits hold the number of extra cycles that are added on the PWM pulse period every 64 PWM frames.

Note: This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	-
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)

41.8.18 Compare/Capture Channel x

Name: CC
Offset: 0x44 + n*0x04 [n=0..5]
Reset: 0x00000000
Property: Write-Synchronized, Read-Synchronized

The CCx register represents the 16-, 24- bit value, CCx. The register has two functions, depending of the mode of operation.

For capture operation, this register represents the second buffer level and access point for the CPU and DMA.

For compare operation, this register is continuously compared to the counter value. Normally, the output form the comparator is then used for generating waveforms.

CCx register is updated with the buffer value from their corresponding CCBUFx register when an UPDATE condition occurs.

In addition, in match frequency operation, the CC0 register controls the counter period.

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CC[17:10]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CC[9:2]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CC[1:0]		DITHER[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:6 – CC[17:0] Channel x Compare/Capture Value
These bits hold the value of the Channel x compare/capture register.
Notes:
1. When the TCC is configured as a 16-bit timer/counter, the excess bits are read as zero.
2. This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6 (depicted)

Bits 5:0 – DITHER[5:0] Dithering Cycle Number

These bits hold the number of extra cycles that are added on the PWM pulse width every 64 PWM frames.

Note: This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	-
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)

41.8.19 Pattern Buffer

Name: PATTBUF
Offset: 0x64
Reset: 0x0000
Property: Write-Synchronized, Read-Synchronized

Bit	15	14	13	12	11	10	9	8
	PGVB7	PGVB6	PGVB5	PGVB4	PGVB3	PGVB2	PGVB1	PGVB0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PGEB7	PGEB6	PGEB5	PGEB4	PGEB3	PGEB2	PGEB1	PGEB0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 8, 9, 10, 11, 12, 13, 14, 15 – PGVB Pattern Generation Output Value Buffer
This register is the buffer for the PGV register. If double buffering is used, valid content in this register is copied to the PGV register on an UPDATE condition.

Bits 0, 1, 2, 3, 4, 5, 6, 7 – PGEB Pattern Generation Output Enable Buffer
This register is the buffer of the PGE register. If double buffering is used, valid content in this register is copied into the PGE register at an UPDATE condition.

41.8.20 Period Buffer Value

Name: PERBUF
Offset: 0x6C
Reset: 0xFFFFFFFF
Property: Write-Synchronized, Read-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	PERBUF[17:10]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	15	14	13	12	11	10	9	8
	PERBUF[9:2]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	PERBUF[1:0]		DITHERBUF[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bits 23:6 – PERBUF[17:0] Period Buffer Value

These bits hold the value of the Period Buffer register. The value is copied to PER register on UPDATE condition.

Note: When the TCC is configured as 16-bit timer/counter, the excess bits are read zero.

Note: This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6 (depicted)

Bits 5:0 – DITHERBUF[5:0] Dithering Buffer Cycle Number

These bits represent the PER.DITHER bits buffer. When the double buffering is enabled, the value of this bit field is copied to the PER.DITHER bits on an UPDATE condition.

Note: This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	-
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)

41.8.21 Channel x Compare/Capture Buffer Value

Name: CCBUF
Offset: 0x70 + n*0x04 [n=0..5]
Reset: 0x00000000
Property: Write-Synchronized, Read-Synchronized

CCBUFx is copied into CCx at TCC update time

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
	CCBUF[17:10]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	CCBUF[9:2]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	CCBUF[1:0]		DITHERBUF[5:0]					
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 23:6 – CCBUF[17:0] Channel x Compare/Capture Buffer Value

These bits hold the value of the Channel x Compare/Capture Buffer Value register. The register serves as the buffer for the associated compare or capture registers (CCx). Accessing this register using the CPU or DMA will affect the corresponding CCBUFVx status bit.

Notes:

1. When the TCC is configured as a 16-bit timer/counter, the excess bits are read as zero.
2. This bit field occupies the MSB of the register, [23:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [23:m]
0x0 - NONE	23:0
0x1 - DITH4	23:4
0x2 - DITH5	23:5
0x3 - DITH6	23:6 (depicted)

Bits 5:0 – DITHERBUF[5:0] Dithering Buffer Cycle Number

These bits represent the CCx.DITHER bits buffer. When the double buffering is enable, DITHERBUF bits value is copied to the CCx.DITHER bits on an UPDATE condition.

Note: This bit field consists of the n LSB of the register. n is dependent on the value of the Resolution bits in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [n:0]
0x0 - NONE	-
0x1 - DITH4	3:0
0x2 - DITH5	4:0
0x3 - DITH6	5:0 (depicted)

42. Zigbee Bluetooth Radio Subsystem (ZBT)

42.1 Overview

The PIC32CX-BZ2 and the WBZ45 support on-chip IEEE 802.15.4 and 802.15.3 compliant Zigbee, Bluetooth® Low Energy 5.2 interface with integrated transceivers. The Wireless Subsystem block is comprised of on-chip Zigbee and Bluetooth 5.0 BBP/MAC, shared RF transceiver and Radio Arbiter. This section provides key features of the on-chip Wireless modules.

With integrated Ultra Low Power 2.4 GHz ISM band single transceiver, dual modem and dual MAC, the Radio supports dual Zigbee and Bluetooth 5.2 link protocols. An onboard intelligent Radio Arbiter HW module establishes both the links simultaneously using a single Radio Transmit/Receive with programmable QoS. The RF transceiver includes dual Power Amplifiers architecture and TR Switch. Therefore, medium to high power application use cases are supported without external FEM.

Arbitration between Application, Bluetooth link stack, Zigbee link stack and miscellaneous maintenance tasks are handled on the Cortex M4F (w/ DSP, FPU) CPU using available on-chip system memory resources via RTOS.

Note: Unique Bluetooth and 802.15.4 MAC address are available in OTP memory region. The software SDK and operational stacks provided by Microchip provide API's to access these addresses.

42.2 Features

2.4 GHz RF Transceiver

- Integrated 2.4 GHz Ultra Low Power RF Transceiver Shared Between Bluetooth® and Zigbee® Modems and Link (MAC) Controllers
- Integrated 16 MHz ±30 ppm Crystal Oscillator (External Low Cost Crystal)
- Two PA Design Architecture (LPA (+4 dBm) and MPA (+12 dBm)) to Improve TX Power Efficiency
- WBZ451H: 48-Pin QFN LPA/MPA Combined with External FEM Design to Achieve +20 dBm Output Power
- Low RBOM Two-Port TRX RFFE Architecture
  – Integrated balun (single-ended RF output) and TRX Switch
- Hardware Radio Arbiter with Programmable QoS:
  – Resolution: up to per packet level
  – Time-division coexistence between Bluetooth and 802.15.4
  – Based on shared transceiver and antenna
  – Maintains connections of 802.15.4 and Bluetooth simultaneously

Bluetooth

- Bluetooth Low Energy 5.2 Certified
- Programmable Transmit Output Power:
  – WBZ45 – Up to +12 dBm
  – WBZ451H – Up to +20 dBm
- Typical Receiver Power Sensitivity:
  – WBZ45:
    - -97 dBm for Bluetooth Low Energy 1 Mbps
    - -94 dBm for Bluetooth Low Energy 2 Mbps
    - -104 dBm for Bluetooth Low Energy 125 Kbps
    - -101 dBm for Bluetooth Low Energy 500 Kbps

    - Digital RSSI indicator (-50 dBm to -90 dBm)
  - WBZ451H:
    - -99 dBm for Bluetooth Low Energy 1 Mbps
    - -96 dBm for Bluetooth Low Energy 2 Mbps
    - -106 dBm for Bluetooth Low Energy 125 Kbps
    - -102 dBm for Bluetooth Low Energy 500 Kbps
- Bluetooth Supported Features:
  - 2M uncoded PHY
  - Long range (Coded PHY)
  - Channel selection algorithm #2
  - Advertising extensions, offloads CPU with hardware-based scheduler
  - High duty cycle non-connectible advertising
  - Data length extensions
  - Secure connections
  - Privacy upgrades (with hardware white-list support)
- ECDH P256 Hardware Engine for Link Key Generation when Bluetooth Pairing
- AES128 Hardware Module for Real-Time Bluetooth Payload Data Encryption
- HCI Interface via UART
- Bluetooth Low Energy Profiles:
  - Bluetooth Low Energy peripheral and central roles
  - Bluetooth Low Energy APIs for application layer to implement standard or customize GATT based profiles/services
  - Microchip Transparent UART Service
  - Battery Service
  - Device Information Service
  - Multi-link and multi-role
- Bluetooth Low Energy Services:
  - Provisioning
  - Over-The-Air (OTA) update (also known as DFU)
  - Advertisement/Beacon
  - Personalized configuration
  - Alert notification service

802.15.4/Zigbee/Thread

- 802.15.4/Zigbee PSDU data rate: 250 Kbps
- Programmable RX Mode:
  - Continuous mode:
    - WBZ45: -103 dBm RX sensitivity
    - WBZ451H: -104 dBm RX sensitivity
  - RPC mode:
    - WBZ45: -98 dBm sensitivity
    - WBZ451H: -103 dBm sensitivity

  - RPC mode provides lower power consumption in RX mode to support California Green Energy Specification at the system level
- Hardware-Assisted MAC:
  - Auto acknowledge
  - Auto retry
  - Channel access back-off
- SFD Detection, Spreading, De-Spreading, Framing, CRC-16 Computation
- Independent TX/RX Buffers for Improved CPU Offloading while Handling Zigbee Data:
  - 128-byte TX and 128-byte RX frame buffer
- Hardware Security:
  - Advanced Encryption Standard (AES)
  - True Random Number Generator (TRNG)
- Zigbee Stack Support:
  - Zigbee 3.0 ready
  - Zigbee Pro 2015
  - Zigbee green power support (proxy, sink and multi-sensor)
- Thread Stack Support:
  - Thread 1.3.0

Proprietary(1)

- 500 kbps and 1 Mbps are 2.4 GHz Proprietary with DSSS
- 2 Mpbs are 2.4 GHz Proprietary without DSSS
- TX Output Power:
  - WBZ45: Up to +12 dBm
  - WBZ451H: Up to +20 dBm
- Receiver Sensitivity:
  - WBZ45: Up to -96 dBm
  - WBZ451H: Up to -99 dBm
- Hardware-Assisted MAC:
  - Auto acknowledge
  - Auto retry
  - Channel access back-off
- SFD Detection, Spreading, De-Spreading, Framing, CRC-16 Computation
- Independent TX/RX Buffers for improved CPU Offloading while Handling Zigbee Data:
  - 128-byte TX and 128-byte RX frame buffer
- Hardware Security:
  - Advanced Encryption Standard (AES)
  - True Random Number Generator (TRNG)

Note:

1. Proprietary modes are compatible to AT86RF233 modes of similar data rate.

42.3 Wireless Subsystem Top Level Diagram

Figure 42-1. Wireless Subsystem Top Level Diagram

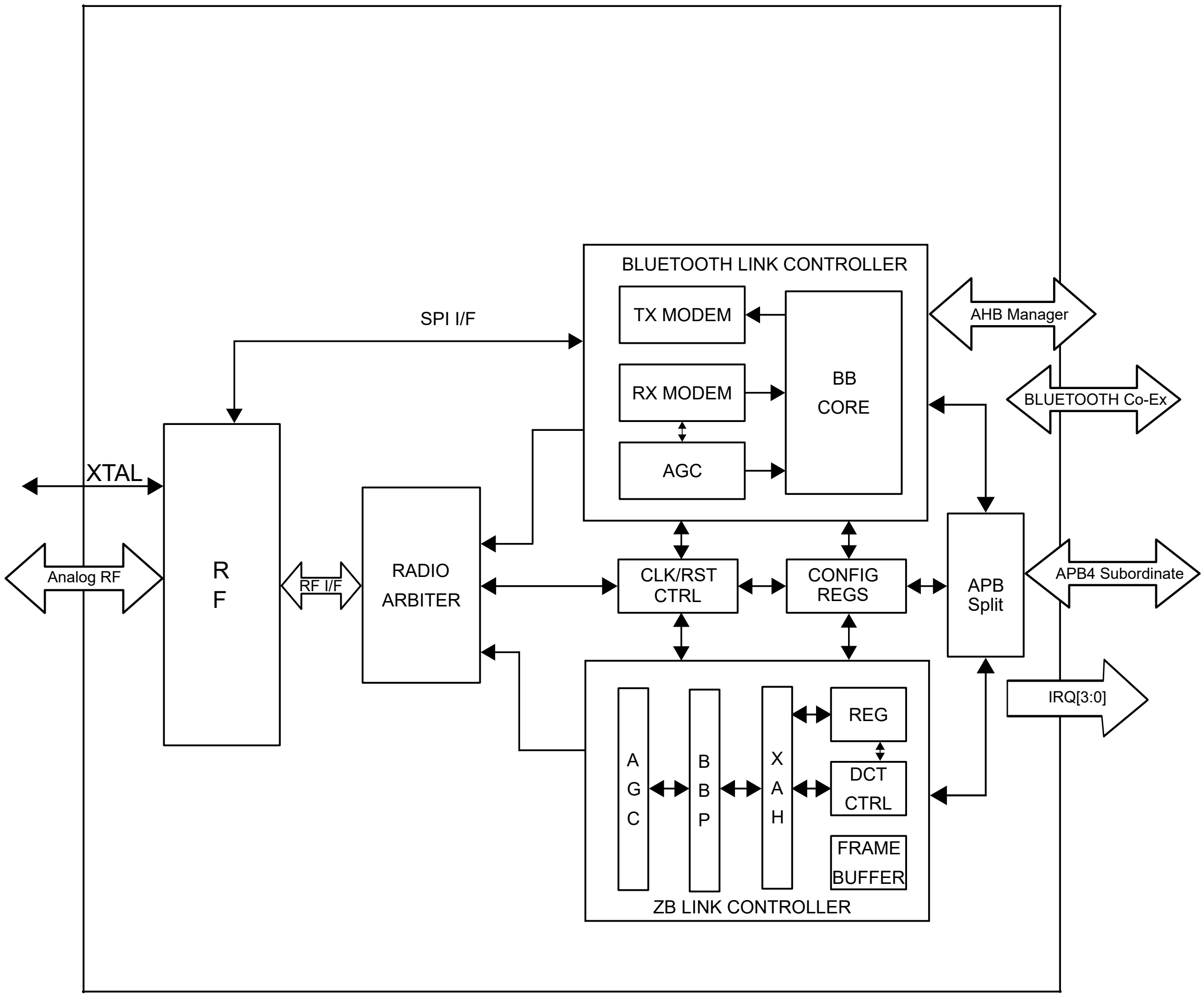
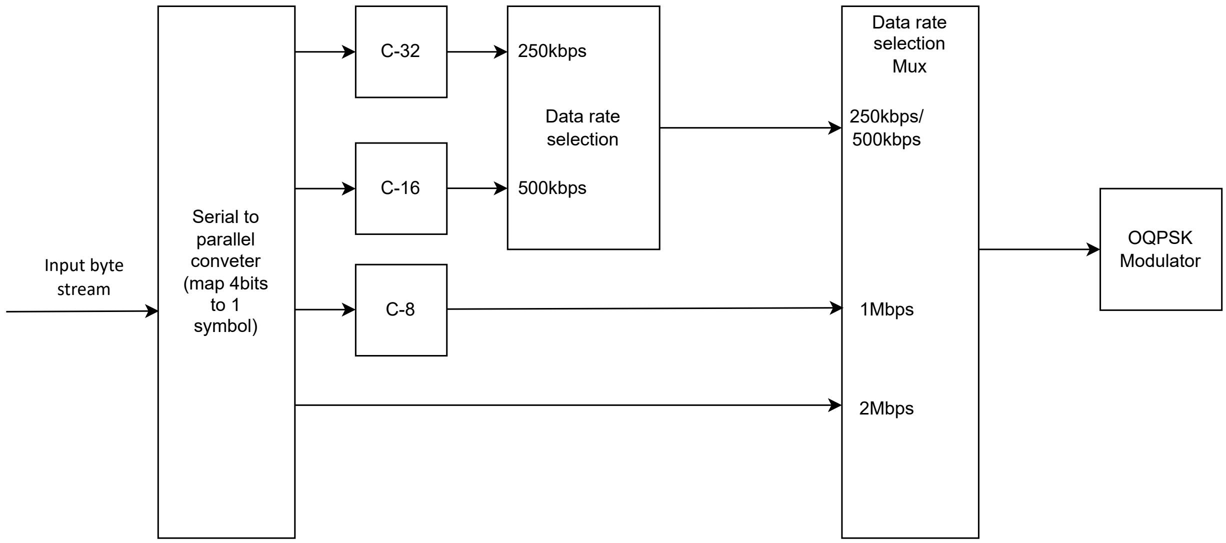


Figure 42-2. Zigbee Baseband Processor Block Diagram



42.4 Bluetooth Link Controller

The APB interface provides access to internal register banks of the macro. These registers are programmed by the host (firmware) to set various configurations, trigger commands, read status, service interrupts and other functions.

All Bluetooth operations are carried out as transmit or receive tasks within the Link controller. There are several task controllers:

- Firmware – Firmware can trigger tasks by writing the task controller registers.
- Hardware Schedule Controller – This is Bluetooth 5.2 Bluetooth Low Energy advertisement scheduler controller (Adv. role).
- Hardware Scanner – This is Bluetooth 5.2 Bluetooth Low Energy advertisement scanner (Central role).
- Bluetooth Low Energy advertisement controller – This is Bluetooth 5.2 advertisement controller (Adv. role).

The requests from the task controllers are arbitrated and is carried out by the task controller.

42.4.1 Hardware Schedule Controller

Hardware Schedule controller is a hardware accelerator that offloads the Bluetooth 5.2 advertising task from the firmware and executes it in hardware completely.

42.4.2 Hardware Scanner

Hardware Scanner is another hardware accelerator to be used in the Bluetooth Low Energy/central mode. This offloads the Bluetooth Low Energy task of scanning for advertisements from the firmware. This enables fast scanning and quick connections.

42.4.3 Bluetooth Low Energy Advertisement Controller

Bluetooth Low Energy advertisement controller is a hardware controller that supports offloading of Bluetooth 5.2 advertisements. This is a simpler advertising scenario requiring much smaller memory.

The task controller manages overall TX/RX functionality and starts TX control FSM / RX control FSM in the baseband as per requirement to transmit/receive a packet. The task controller also manages the coexistence interface with Wi-Fi. The task controller can also be used directly by the firmware to measure the RSSI across various Bluetooth channels, which can, then, be used to generate an AFH channel map.

42.4.4 Bluetooth Clock Controller

The Bluetooth clock controller/Slot timer provides information on Bluetooth slots and the slot boundary. The Bluetooth clock synchronization and clock adjustment due to RX window uncertainty is also handled by this controller. It controls the timings for Bluetooth Low Energy non-TIFS tasks.

TX/RX control FSM (State machines) provide sequencing and control of various phases of a task. These control various elements in the TX and RX data path.

The Crypto engine is used for AES encryption and decryption of transmit and receive data. This performs inline encryption as the data passes through the data path in the BB link controller. This controller is also used to perform offline CMAC operation directly under application firmware control. This controller is also used by the Bluetooth Low Energy privacy controller for the generation and decoding of hash needed for resolving private addresses.

42.4.5 Bluetooth Low Energy Privacy Controller

Bluetooth Low Energy Privacy controller is to implement the Bluetooth Low Energy privacy feature. It can be used in offline mode by the firmware to generate a Resolvable Private Address (RPA) to be used for a transmission. And it is also used inline by the RX Control FSM to resolve the RPA received in the packet before implementing the device filtering using the white list.

The Channel Hop Controller implements the logic needed to compute the next RF channel frequency to be used.

A dedicated math unit for big number (128-bit) operations is available for firmware to handle large number operations. This is programmed and used by the firmware directly. There is no direct use of this block by any other hardware block.

For simple, secure pairing, the P256 ECC module is available to perform computationally intensive key-matching procedures in hardware.

The transmit memory read controller reads the data from the common memory and feeds them to the transmit data path for Bluetooth PDU creations and transmit. The receive memory write controller receives data from the RX data path and writes them to the common memory.

42.5 Zigbee/Proprietary Data Rate Link Controller

The Zigbee Link Controller implements Zigbee 3.0 (802.15.4-2011) MAC and baseband functionality in hardware.

The CPU interface (APB Subordinate) provides access to internal registers of the macro. These registers are programmed by the host (firmware) to kick off transmit/receive functionality along with the programming of other features. The APB Subordinate contains shadow registers for the status registers in the design for single-cycle, contention-free read accesses. Interrupt controller logic also resides in the APB subordinate module.

Separate 128-byte frame buffers are provided for TX and RX.

The XAH module implements basic MAC functionality as well as a hardware accelerator for features such as automatic acknowledgement, CSMA-CA and retransmission, automatic FCS check and so on.

The BBP module implements Offset-QPSK PHY with 250 kb/s PSDU data rate. It also supports proprietary 500 kbps OQPSK PHY, 1 Mbps MSK PHY, and a 2 Mbps MSK non-spreading PHY.

42.5.1 Transmit Operation

A frame transmission comprises of two actions: a write to Frame Buffer and the transmission of its contents. Both actions can be run in parallel if required by critical protocol timing.

42.5.2 Receive Operation

A frame reception comprises of two actions: the transceiver listens for, receives and demodulates the frame to the Frame Buffer and signals the reception to the microcontroller. After that process, the microcontroller can read the available frame data from the Frame Buffer via the APB interface.

42.6 Radio Arbiter

The Radio Arbiter determines the ownership of the Radio between Zigbee and Bluetooth link controllers. It also generates control to select between Zigbee/Bluetooth to drive the controls and data to or from the RF.

By default, the Arbiter is IDLE and no Link controller has the ownership. The general intention of the design is to provide a radio arbiter that is flexible enough that the arbitration schemes can be tuned by the firmware with real application Bluetooth/Zigbee scenarios.

All design and intellectual property parts of this arbiter design are property of Microchip Technology Inc., released under appropriate NDA.

42.6.1 Arbiter Modes

The following are the modes supported by the arbiter:

- Bluetooth static – Radio ownership is with the Bluetooth Link controller
- Zigbee static – Radio ownership is with the Zigbee Link controller
- Dynamic – Radio ownership decided dynamically at every arbitration event

42.7 RF Physical Layer

The top level block diagram of the transceiver architecture is as follows.

Figure 42-3. WBZ45 Transceiver Architecture

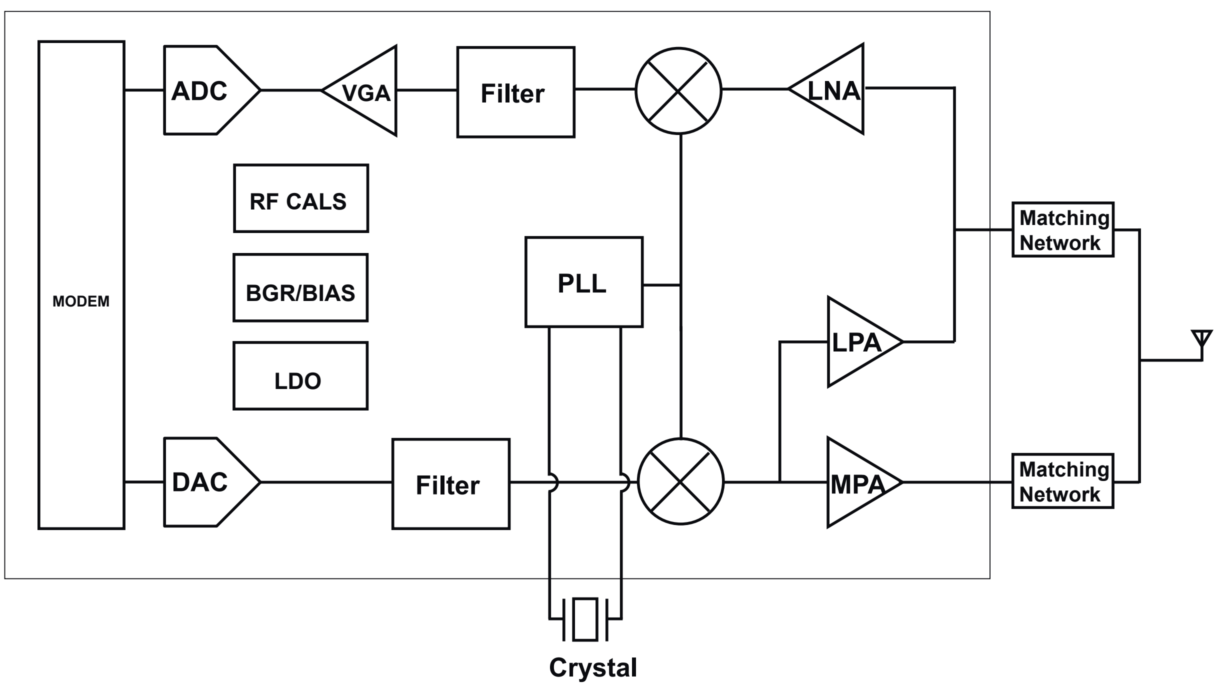
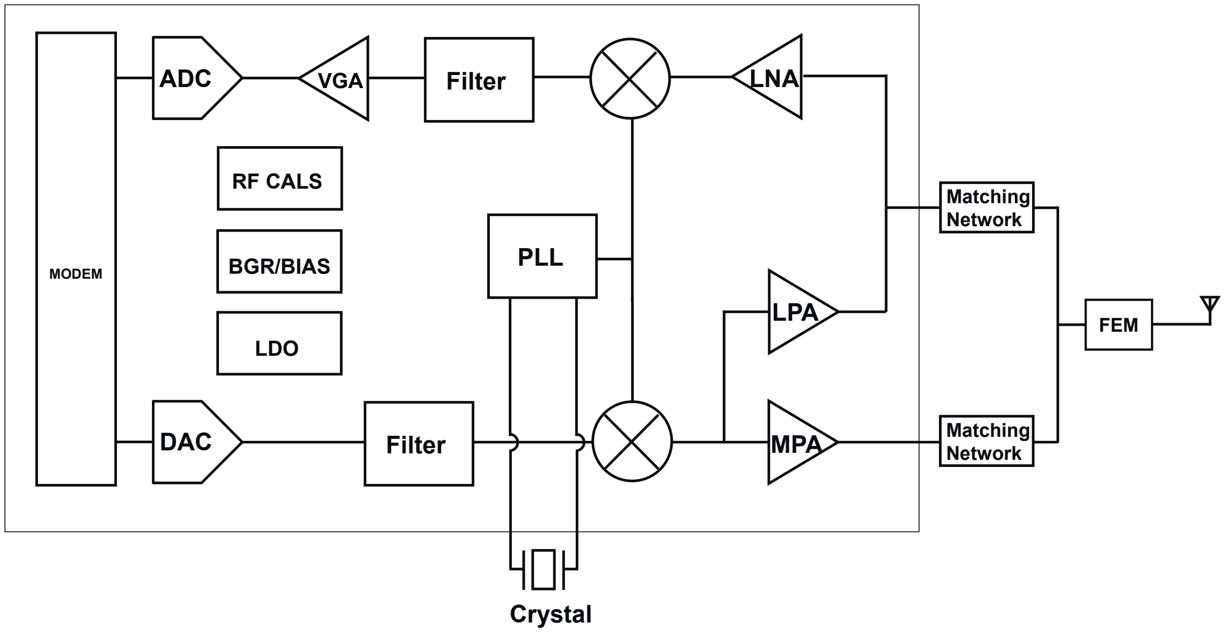


Figure 42-4. WBZ451H Transceiver Architecture



42.8 Frequency Synthesizer

The PIC32CX-BZ2 and the WBZ45 require 16 MHz for generating the local oscillator frequency between the 2.4 GHz to 2.48 GHz for the transmitter and receiver. The frequency synthesizer integrates all the passives for the loop filter inside the chip.

42.8.1 Transmit Mixer and Power Amplifier

The PIC32CX-BZ2 and WBZ45 implement a direct conversion I/Q transmitter. The I/Q from the low pass filter of the TX path is converted to the desired output frequency through an I/Q mixer that operates on the LO frequency from the Synthesizer. The VCO operates at 4x the LO frequency.

The supply for LPA and MPA is through separated power supply pins that can be connected to the output from the PMU with necessary decoupling.

The LPA is a single stage amplifier that provides ~5.5 dBm output power in standalone mode and ~4 dBm in LPA/MPA shared mode. Both LPA and MPA implement an on-chip BALUN. The LPA pin also acts as the input to the RX section.

The MPA is a single stage power amplifier designed to provide a maximum output power of ~12 dBm. MPA also implements an on-chip BALUN to get a single-ended TX output. MPA is NOT internally connected to the receiver.
It is mandatory that the LPA pin be used for the Receiver path. On a typical application, the LPA and MPA can be connected directly, eliminating the need for an external switch.
Note: For WBZ451H, the 48-pin QFN LPA/MPA is combined with the external FEM design to achieve +20 dBm output power. The WBZ451H module has the matching network for doing a combined match of the LPA and MPA path along with a harmonic filter followed by an antenna-matching circuit and an antenna.

42.8.2 Receiver

The receiver path starts with the LPA pin, which is shared with the LPA path and the LNA. PIC32CX-BZ2 implements a low-IF differential receiver. The synthesizer generates the LO for down-conversion on the mixer, which goes through a BPF filter to the ADC. The Receiver implements an AGC to adjust the LNA gain depending upon the input signal level.

42.9 RFLDO

The RF section has multiple LDOs to power the various power domains of the RF subsystem, All these LDOs can be powered up from the MLDO/DC-DC mode of the PMU and can get 1.35V and generate 1.2V internally to feed the corresponding RF sections. These LDOs need a bypass capacitor on the output for their operation. See *Power Subsystem* from Related Links.

- RF-PLL
- BUCK-LPA
- BUCK-MPA
- BUCK-BB

Related Links
Power Subsystem

43. Electrical Characteristics

This chapter provides the Electrical Specification and Characteristic of PIC32CX-BZ2 and WBZ45 Module across the operating temperature range of the product.

43.1 Absolute Maximum Electrical Characteristics

Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Table 43-1. Absolute Maximum Ratings

Parameter	Value
Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on V_{DD}/V_{DDIO} with respect to GND	-0.3V to +4.0V
Voltage on any pin(s), with respect to GND	-0.3V to (V_{DD} + 0.3V)
Maximum current out of GND pins	200 mA
Maximum current into V_{DD} pins	200 mA
Maximum output current sourced/sunk by any Low Current Mode I/O pin (8x drive strength)	15 mA
Maximum output current sourced/sunk by any Low Current Mode I/O pin (4x drive strength)	10 mA
Maximum output current sourced/sunk by any High Current Mode I/O pin (8x drive strength)	10 mA
Maximum output current sourced/sunk by any High Current Mode I/O pin (4x drive strength)	7 mA
Maximum current sink by all ports	120 mA
Maximum current sourced by all ports	120 mA
ESD Qualification	
Human Body Model (HBM) per JESD22-A114	2000V
Charged Device Model (CDM) (ANSI/ESD STM 5.3.1)...(All pins / Corner pins)	+500V/- 500V
Note: 1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.	

Related Links

Thermal Specifications

43.2 DC Electrical Characteristics

Table 43-2. Operating Frequency VS. Voltage

Param. No.	V_{DDIO}, V_{DDANA} Range	Temp. Range (in °C)	Max. MCU Frequency	Comments
DC_5	1.9V to 3.6V	-40°C to +85°C	64 MHz	Industrial
DC_7	1.9V to 3.6V	-40°C to +125°C	64 MHz	Extended
Note: The same voltage must be applied to V_{DDIN} and V_{DDIO}.				

43.3 Thermal Specifications

Table 43-3. Thermal Operating Conditions

Rating	Symbol	Min.	Typ	Max.	Unit
Industrial Temperature Devices:					
Operating ambient temperature range	T_A	-40	—	+85	°C
Operating junction temperature range	T_J	-40	—	+105	°C
Extended Temperature Range:					
Operating ambient temperature range	T_A	-40	—	+125	°C
Operating junction temperature range	T_J	-40	—	+145	°C
Maximum allowed power dissipation	P_{DMAX}	$(T_J – T_A)/Θ_{JA}$			W

Table 43-4. Thermal Packaging Characteristics

Characteristics	Symbol	Typ	Max.	Unit
Thermal Resistance, 48-pin VQFN (7 mm x 7 mm x 0.9 mm) Package	$Θ_{JA}$	31.6	—	°C/W(1)
Thermal Resistance, 32-pin VQFN (5 mm x 5 mm x 1 mm) Package	$Θ_{JA}$	35.1	—	°C/W(1)

Note:
1. The junction-to-ambient thermal resistance, $Θ_{JA}$, numbers are achieved by package simulations. JEDEC standard.

43.4 Power Supply Electrical Specifications

Table 43-5. Power Supply Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
REG_1	$VDDCORE\_C_{IN}$	VDDCORE (CLDO_OUT) input bypass parallel capacitor pair(5)	—	1	—	µF	Bulk ceramic or solid tantalum with ESR <0.5Ω. Min and max represent absolute values including cap tolerances
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature
REG_5	VDD33	VDD33 input bypass parallel capacitor pair(5)	—	10	—	µF	Bulk ceramic or solid tantalum with ESR <0.5Ω(5)
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature on all VDDIO pins(5)
REG_6	PMU_VDDIO	Input bypass parallel capacitor pair for the PMU power section(5)	—	4.7	—	µF	Bulk Ceramic or solid Tantalum with ESR <0.5Ω(5)
REG_7	PMU_VDDP	Input bypass parallel capacitor pair for the PMU power section(5)	—	1	—	µF	Bulk ceramic or solid tantalum with ESR <0.5Ω(5)
REG_9	$VDDFLASH\_C_{IN}$	VDD_FLASH bypass parallel capacitor pair(5)	—	10	—	µF	Bulk ceramic or solid tantalum with ESR <0.5Ω(5)
			—	100	—	nF	Ceramic XR7/X5R with ESR <0.5Ω depending on temperature on all VDDFLASH pins(5)
REG_17	$VDDANA\_C_{IN}$	VDDANA input bypass parallel capacitor pair(5)	—	10	—	µF	Bulk ceramic or solid tantalum with ESR <0.5Ω(5)
			—	0.1	—	nF	Ceramic XR7/X5R with ESR <0.5Ω

...........continued

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
REG_18	VDDANA_LEXT	VDDANA series ferrite bead DCR (DC resistance)	—	—	0.1	Ω	≥600Ω at 100 MHz
REG_19		Ferrite bead current Rating(1)	100	—	—	mA	—
REG_20	BUCK_PLL_CIN	VDD bypass capacitor on the BUCK_PLL input	—	1	—	µF	Ceramic XR7/X5R with ESR <0.5Ω
REG_21	BUCK_BB_CIN	VDD bypass capacitor on the BUCK_BB input	—	1	—	µF	Ceramic XR7 with ESR <0.5Ω
REG_22	BUCK_MPA_CIN	VDD bypass capacitor on the BUCK_LPA input	—	1	—	µF	Ceramic XR7 with ESR <0.5Ω
REG_23	BUCK_LPA_CIN	VDD bypass capacitor on the BUCK_MPA input	—	1	—	µF	Ceramic XR7 with ESR <0.5Ω
REG_24	BUCK_CLDO_CIN	VDD bypass capacitor on the BUCK_CLDO input	—	1	—	µF	Ceramic XR7 with ESR <0.5Ω
REG_25	R_EXT	Bias for reference current generation	—	30	—	kΩ	—
REG_27	VSW_L_{EXT}(2,3)	Buck Switch mode regulator inductor inductance	—	4.7	—	µH	Shielded inductor only
REG_29		Inductor DCR (DC resistance)	—	—	0.22	Ω	—
REG_31		Inductor I_{SAT} rating(2,6)	250	—	—	mA	—
REG_32	VSW_CAPEXT	Buck Switch mode regulator bulk capacitor capacitance	10	—	—	µF	—
REG_32A		Buck Switch mode regulator filtering capacitor capacitance	100	—	—	nF	—
REG_36	VDDCORE	VDDCORE voltage range	1.14	1.2	1.26	V	MCU Active, cache and prefetch disabled while executing from Flash
REG_37	VDD33(4)	VDD33 input voltage range	1.9	3.3	3.6	V	—
REG_39	VDDANA(4)	VDDANA input voltage range	1.9	3.3	3.6	V	—
REG_40	VDD_PMU	PMU output voltage	1.30	1.35	1.40	V	PMU output voltage
REG_43	SVDDIO_R	VDDIO rise ramp rate to ensure internal Power-on Reset signal	0.03	—	0.11	V/ms	Failure to meet this specification may lead to start-up or unexpected behaviors
REG_44	SVDDIO_F	VDDIO falling ramp rate to ensure internal Power-on Reset signal	—	—	1.39	V/ms	Failure to meet this specification may cause the device to not detect reset
REG_45	VPOR+	Power-on Reset	—	1.59	—	V	VDDIO power up/Down (See Param REG43, VDDIO Ramp Rate)
REG_45_A	VPOR-	Power-on Reset	—	1.56	—	V	VDDIO Power up/Down (See Param REG43, VDDIO Ramp Rate)
REG_47	VBOR33(4)	VDDIO BOD	—	1.8	—	V	—

...........continued

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
REG_48	VBOR12	BOR of the 1.2V regulator	—	1.1	—	V	—
REG_48A	VZPBOR33	Zero power BOR	2.1	—	—	V	Function available from 2.1V to 3.6V. Applicable for deep sleep wake-up condition.
REG_49	VBOR33L2H	BOR 3.3V low to high switch point	—	1.84	—	V	—
REG_50	VBOR1P2L2H	BOR 1.2V low to high switch point	—	1.1	—	V	—
REG_51	VBOD12	VBOD12 Hysteresis	—	10.5	—	mV	—
REG_52	VBOD33	VBOD33 Hysteresis	—	51.6	—	mV	—
REG_53	TRST(6)	External RESET valid active pulse width	—	11	—	µs	Minimum Reset active time to guarantee MCU Reset for the module. Reset filter circuit inside Module
			—	2.7	—	µs	Minimum Reset active time to guarantee MCU Reset for SoC with no Reset filter circuit

Notes:

1. Ferrite Bead ISAT(min) ≥ (IDDANA(max) * 1.15).
2. Buck Inductor ISAT(min) ≥ ((ICAPACITOR + IVDDCORE_MAX) * 1.2) when the BUCK mode is enabled (shielded inductor only).
3. User must select either LDO or BUCK Mode. The modes are exclusive to each other.
4. VDD33 and VDDANA must be at the same voltage level.
5. All bypass caps must be located immediately adjacent to pin(s) and on the same side of the PCB as the MCU. Each primary power supply group VDDIO, VDDANA, VDDCORE must have one bulk capacitor and all power pins with a 100 nF bypass cap.
6. The RESET pulse width is the minimum pulse width required on the I/O pin after any filtering on the $\overline{\text{MCLR}}$ pin.
7. Keep the DCR as low as possible to improve efficiency.
8. These parameters are characterized but not tested in manufacturing.

43.5 Active Current Consumption DC Electrical Specifications (85°C)

Table 43-6. Active Current Consumption DC Electrical Specifications

DC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp			
Param. No.	Symbol	Characteristics	Clock/Freq	Typ.(1)	Max.	Units	Conditions
APWR_1	I_{DD_ACTIVE}(2,3)	MCU I_{DD} in Active mode w/LDO mode selected	PLL 64 MHz	105	291	µA/MHz	V_{DD} = V_{DDANA} = 3.3V
			PLL 48 MHz	89	274	µA/MHz	V_{DD} = V_{DDANA} = 3.3V
APWR_13		MCU I_{DD} in Active mode w/BUCK mode selected	PLL 64 MHz	70	209	µA/MHz	V_{DD} = V_{DDANA} = 3.3V
			PLL 48 MHz	62	197	µA/MHz	V_{DD} = V_{DDANA} = 3.3V

...........continued

DC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp			
Param. No.	Symbol	Characteristics	Clock/Freq	Typ.(1)	Max.	Units	Conditions

Notes:

1. Typical value measured at 25°C and 3.3V.
2. The test conditions are as follows:
   - All GPIO are input and pulled up.
   - RF System ON with default settings.
   - All Peripherals disabled with PMD bits.
   - All PB clocks are divided by 16.
   - LPRC is set as LPCLK.
   - SOSC is disabled.
   - PMU 1 MHz clock is derived from FRC. FRC is divided by 8.
   - Cache is enabled and configured wait time as 0xF.
   - WCM memories configured in Retention + NAP mode.
   - DSU is disconnected.
3. MCU running while(1) loop with 50 NOP instructions.
4. These parameters are characterized but not tested in manufacturing.

43.6 Active Current Consumption DC Electrical Specifications (125°C)

Table 43-7. Active Current Consumption DC Electrical Specifications

DC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp			
Param. No.	Symbol	Characteristics	Clock/Freq	Typ.(1)	Max.	Units	Conditions
APWR_1	I_{DD_ACTIVE}(2,3)	MCU I_{DD} in Active mode w/LDO mode selected	PLL 64 MHz	105	411	µA/MHz	V_{DD} = V_{DDANA} = 3.3V
			PLL 48 MHz	89	395	µA/MHz	V_{DD} = V_{DDANA} = 3.3V
APWR_13		MCU I_{DD} in Active mode w/BUCK mode selected	PLL 64 MHz	70	291	µA/MHz	V_{DD} = V_{DDANA} = 3.3V
			PLL 48 MHz	62	279	µA/MHz	V_{DD} = V_{DDANA} = 3.3V

Notes:

1. Typical value measured at 25°C and 3.3V.
2. The test conditions are as follows:
   - All GPIO are input and pulled up.
   - RF System ON with default settings but not doing RF transmission.
   - All Peripherals disabled with PMD bits.
   - All PB clocks are divided by 16.
   - LPRC is set as LPCLK.
   - SOSC is disabled.
   - PMU 1 MHz clock is derived from FRC. FRC is divided by 8.
   - Cache is enabled and configured wait time as 0xF.
   - WCM memories configured in Retention + NAP mode.
   - DSU is disconnected.
3. MCU running while(1) loop with 50 NOP instructions.
4. These parameters are characterized but not tested in manufacturing.

Figure 43-1. Run Mode Current Consumption in Buck Mode at PLL 64 MHz

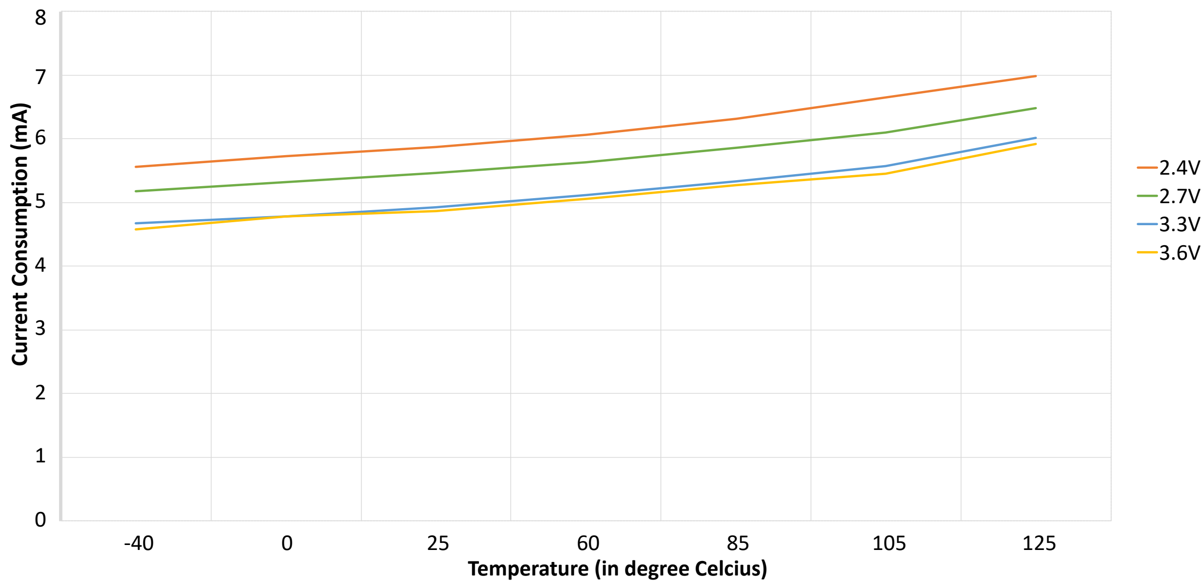
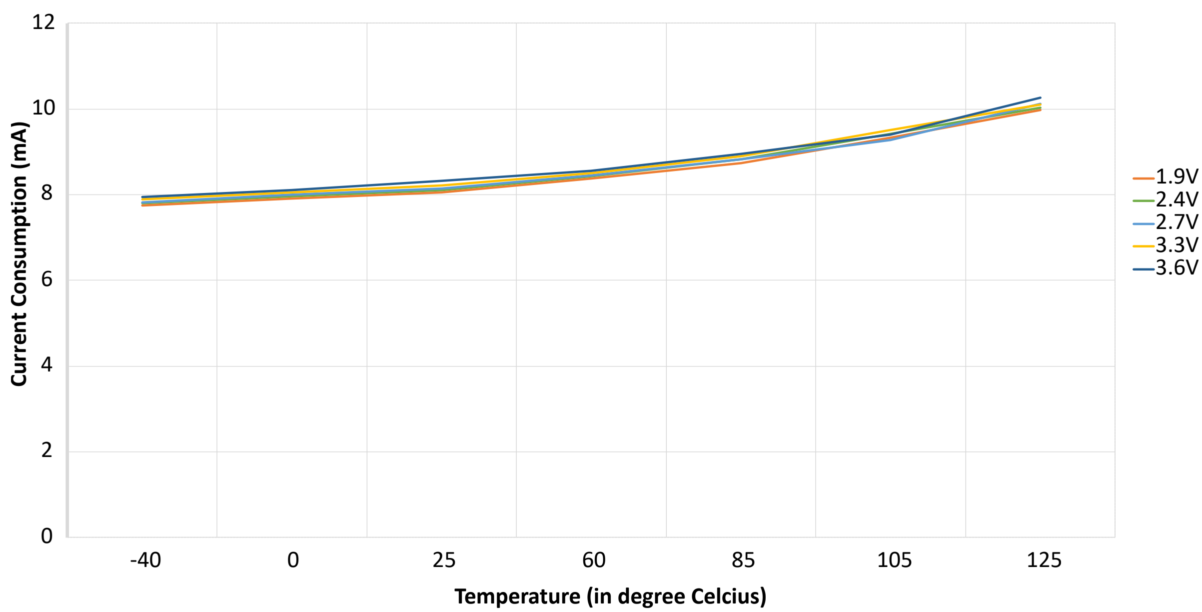


Figure 43-2. Run Mode Current Consumption in MLDO Mode at PLL 64 MHz



43.7 Idle Current Consumption DC Electrical Specifications (85°C)

Table 43-8. Idle Current Consumption DC Electrical Specifications

DC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp			
Param. No.	Symbol	Characteristics	Clock/Freq	Typ.(1)	Max.	Units	Conditions
IPWR_1	I_{DD_IDLE} (2)	MCU I_{DD} in IDLE mode w/LDO mode selected	PLL 64 MHz	54	184	µA/MHz	V_{DD} = V_{DDANA} = 3.3V
			PLL 48 MHz	68	249		
IPWR_3		MCU I_{DD} in IDLE mode w/ BUCK mode selected	PLL 64 MHz	77	258		
			PLL 48 MHz	49	178		

Notes:

1. Typical value measured at 25°C and 3.3V.
2. The test conditions are as follows:
   - All GPIO are input and pulled up.
   - All Peripherals disabled with PMD bits.
   - All PB clocks are divided by 16.
   - LPRC is set as LPCLK.
   - SOSC is disabled.
   - PMU 1 MHz clock is derived from FRC. FRC is divided by 8.
   - Cache is enabled and configured to wait time as 0xF.
   - WCM memories configured in Retention + NAP mode.
   - DSU is disconnected.
   - RF system OFF.
   - Entry to the Sleep mode is disabled and WFI instruction is executed.
   - On exit by External interrupt, verified RCON status to ensure system was in the IDLE mode.
3. These parameters are characterized but not tested in manufacturing.

43.8 Idle Current Consumption DC Electrical Specifications (125°C)

Table 43-9. Idle Current Consumption DC Electrical Specifications

DC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp			
Param. No.	Symbol	Characteristics	Clock/Freq	Typ.(1)	Max.	Units	Conditions
IPWR_1	I_{DD_IDLE} (2)	MCU I_{DD} in IDLE mode w/LDO mode selected	PLL 64 MHz	77	377	µA/MHz	V_{DD} = V_{DDANA} = 3.3V
			PLL 48 MHz	68	369		
IPWR_3		MCU I_{DD} in IDLE mode w/ BUCK mode selected	PLL 64 MHz	54	266		
			PLL 48 MHz	49	259		

...........continued

DC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp			
Param. No.	Symbol	Characteristics	Clock/Freq	Typ.[(1)]	Max.	Units	Conditions

Notes:

1. Typical value measured at 25°C and 3.3V.
2. The test conditions are as follows:
   – All GPIO are input and pulled up.
   – All peripherals disabled with PMD bits.
   – All PB clocks are divided by 16.
   – LPRC is set as LPCLK.
   – SOSC is disabled.
   – PMU 1 MHz clock is derived from FRC. FRC is divided by 8.
   – Cache is enabled and configured to wait time as 0xF.
   – WCM memories configured in Retention + NAP mode.
   – DSU is disconnected.
   – RF system OFF.
   – Entry to the Sleep mode is disabled and WFI instruction is executed.
   – On exit by External interrupt, verified RCON status to ensure system was in the IDLE mode.
3. These parameters are characterized but not tested in manufacturing.

Figure 43-3. Idle Mode Current Consumption in Buck Mode at PLL 64 MHz

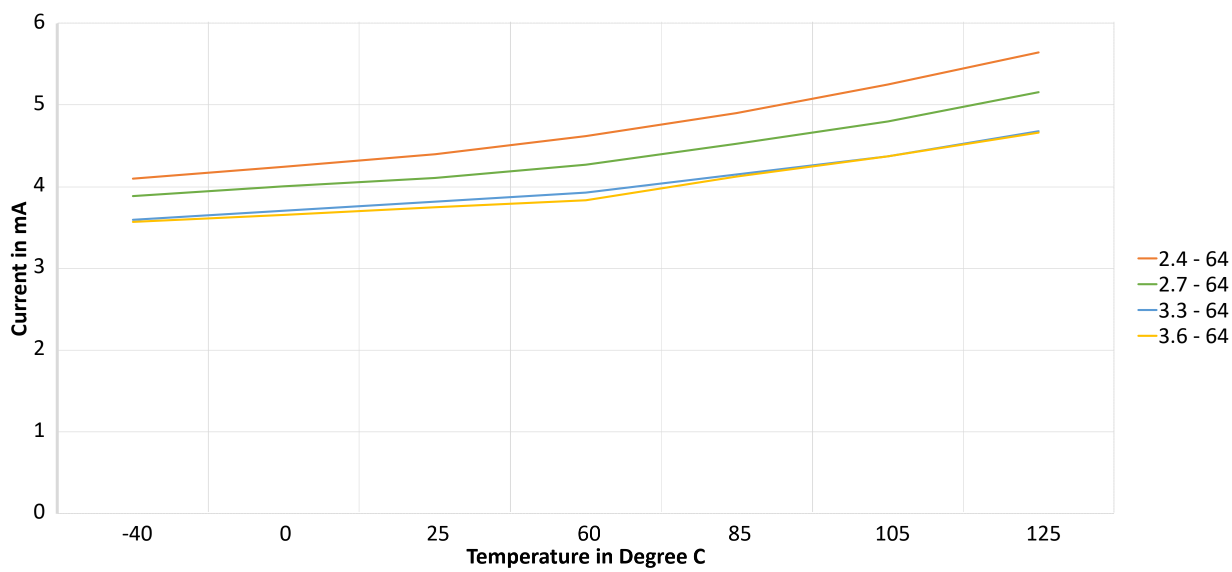
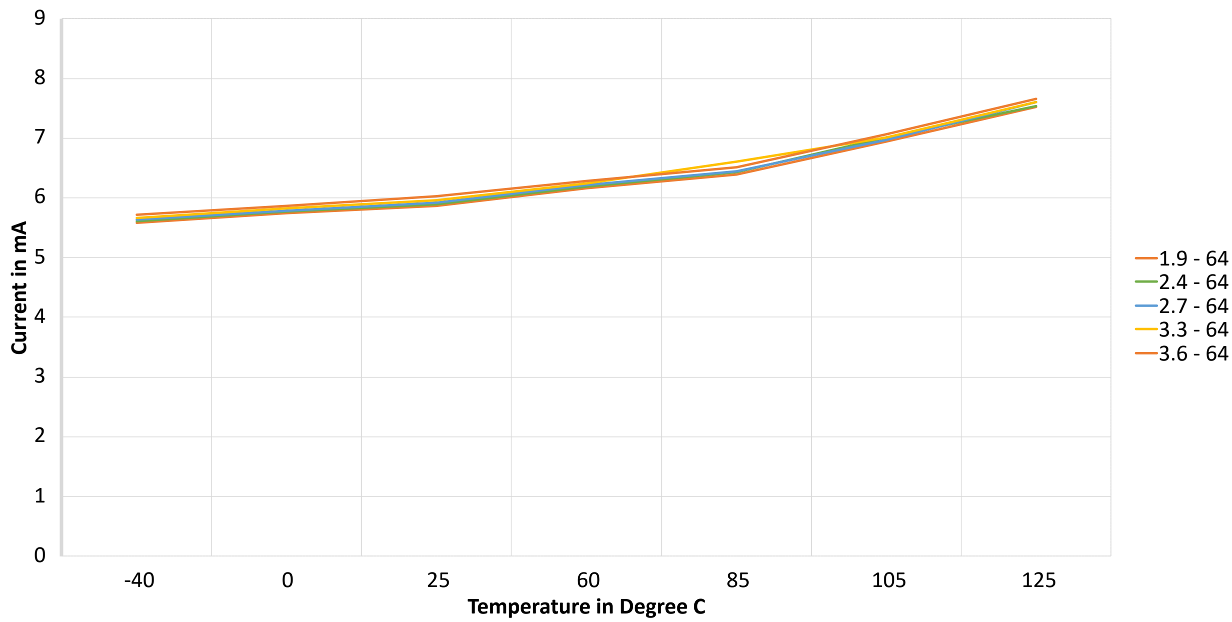


Figure 43-4. Idle Mode Current Consumption in MLDO Mode at PLL 64 MHz



43.9 Sleep Current Consumption DC Electrical Specifications (85°C)

Table 43-10. Sleep Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ.[1]	Max.	Units	Conditions
SPWR_1	I_{DD_SLEEP}	MCU I_{DD} in Sleep mode w/LDO mode selected	3.3V	0.58	10.6	mA	XTAL = OFF
SPWR_5			3.3V	0.88	10.1	mA	XTAL = ON
SPWR_29		MCU I_{DD} in Sleep mode w/ BUCK mode selected	3.3V	0.67	10.7	mA	XTAL = ON
SPWR_33			3.3V	0.49	11.0	mA	XTAL = OFF

...........continued

DC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ.(1)	Max.	Units	Conditions

Notes:

1. Typical value measured at 25°C and 3.3V.
2. The test conditions are as follows:
   - All GPIO are input and pulled up.
   - All peripherals disabled with PMD bits.
   - All PB clocks are divided by 16.
   - LPRC is set as LPCLK.
   - SOSC is disabled.
   - CLDO is configured at lowest possible voltage (VREG Trim = 0x07).
   - PMU is configured to the Buck PSM mode on the Sleep Mode Entry.
   - Cache is enabled and configured wait time as 0xF.
   - WCM memories configured in Retention + NAP mode.
   - DSU is disconnected.
   - RF system is in low power configuration.
   - Entry to the Sleep mode is enabled and WFI instruction is executed.
   - On exit by External interrupt, verified RCON status to ensure system was in Sleep mode.
   - In XTAL ON mode - PMU Buck clock is derived from POSC 16 MHz and scaled to 1 MHz. FRC is OFF.
   - In XTAL OFF mode - PMU is clocked from FRC and XTAL 16 MHz clock is disabled and clock configuration in CRU changed to FRC.
3. These parameters are characterized but not tested in manufacturing.

43.10 Sleep Current Consumption DC Electrical Specifications (125°C)

Table 43-11. Sleep Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ TA ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ.(1)	Max.	Units	Conditions
SPWR_1	I_{DD_SLEEP}	MCU I_{DD} in Sleep mode w/LDO mode selected	3.3V	0.58	16.3	mA	XTAL = OFF, T_A = 25°C
SPWR_5			3.3V	0.88	17.3	mA	XTAL = ON, T_A = 25°C
SPWR_29		MCU I_{DD} in Sleep mode w/BUCK mode selected	3.3V	0.67	13.0	mA	XTAL = ON, T_A = 25°C
SPWR_33			3.3V	0.49	12.6	mA	XTAL = OFF, T_A = 25°C

...........continued

DC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ TA ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ.[1]	Max.	Units	Conditions

Notes:

1. Typical value measured at 25°C and 3.3V.
2. The test conditions are as follows:
   - All GPIO are input and pulled up.
   - All peripherals disabled with PMD bits.
   - All PB clocks are divided by 16.
   - LPRC is set as LPCLK.
   - SOSC is disabled.
   - CLDO is configured at lowest possible voltage (VREG Trim = 0x07).
   - PMU is configured to the Buck PSM mode on the Sleep Mode Entry.
   - Cache is enabled and configured wait time as 0xF.
   - WCM memories configured in Retention + NAP mode.
   - DSU is disconnected.
   - RF system is in low power configuration.
   - Entry to the Sleep mode is enabled and WFI instruction is executed.
   - On exit by External interrupt, verified RCON status to ensure system was in Sleep mode
   - In XTAL ON mode - PMU Buck clock is derived from POSC 16 MHz and scaled to 1 MHz. FRC is OFF.
   - In XTAL OFF mode - PMU is clocked from FRC and XTAL 16 MHz clock is disabled and clock configuration in CRU changed to FRC.
3. These parameters are characterized but not tested in manufacturing.

Figure 43-5. Sleep Current with XTAL_OFF_MLDO

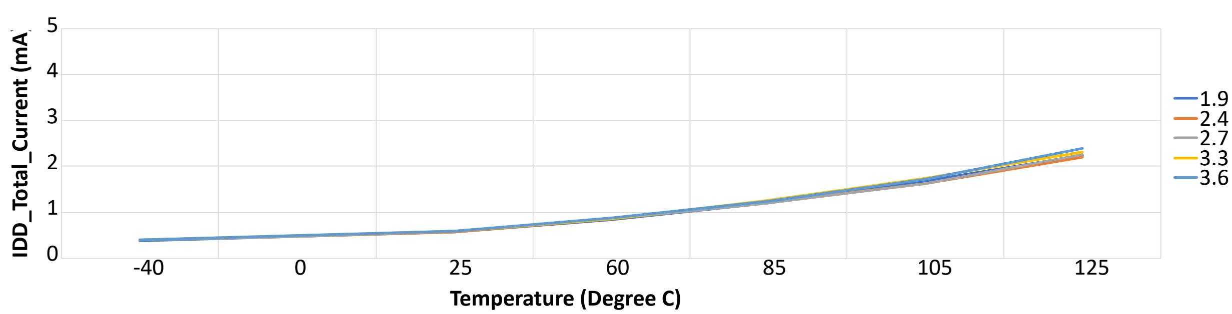


Figure 43-6. Sleep Current with XTAL_OFF_DC_DC

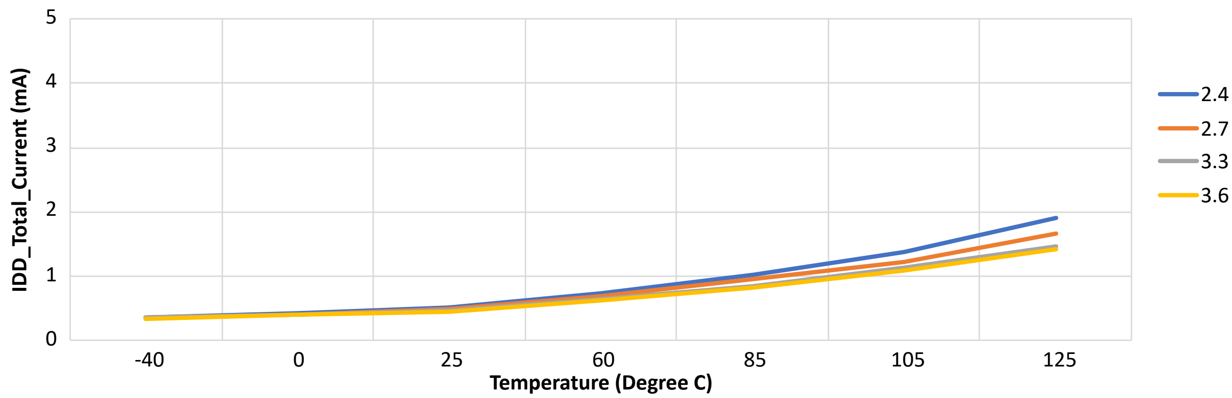


Figure 43-7. Sleep Current with XTAL_ON_MLDO

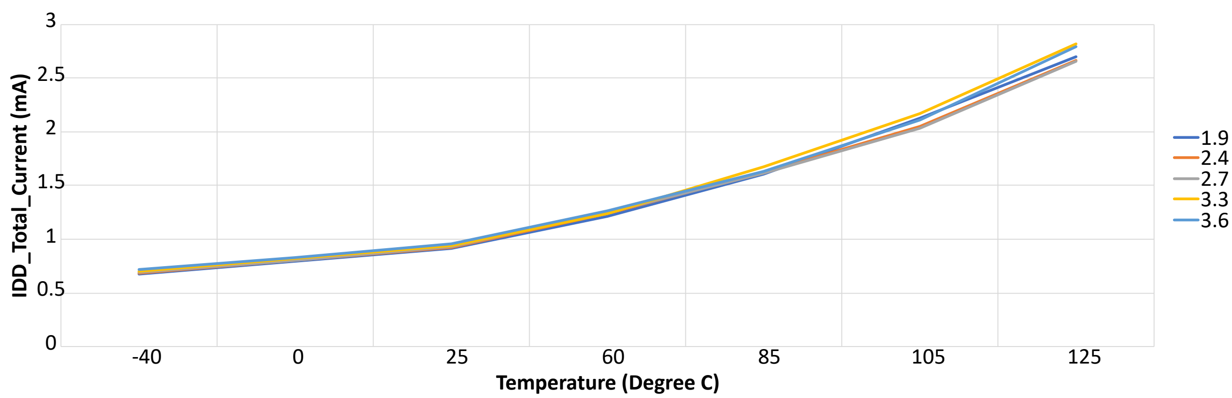
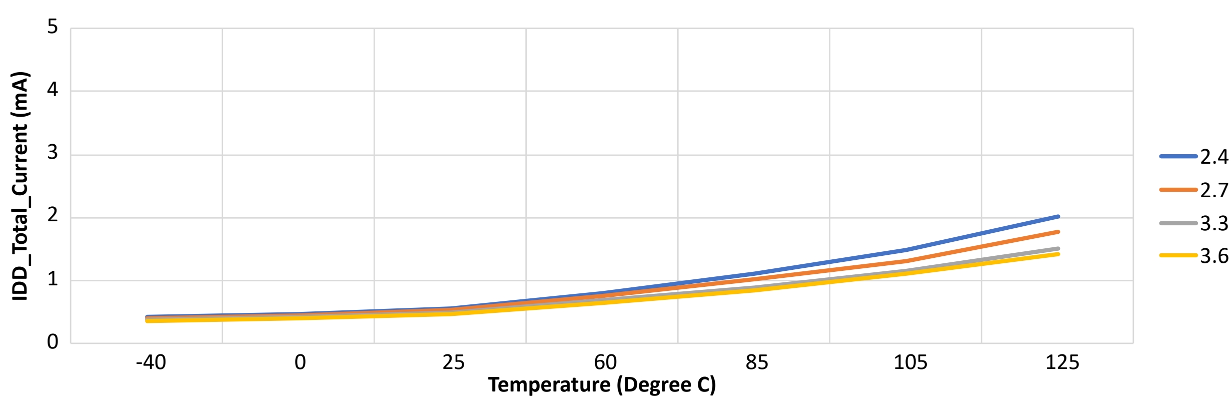


Figure 43-8. Sleep Current with XTAL_ON_DC_DC



43.11 Deep Sleep Current Consumption DC Electrical Specifications (85°C)

Table 43-12. Deep Sleep Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ.(1)	Max.	Units	Conditions
BPWR_1	I_{DD_BACKUP}(2)	MCU I_{DD} in Deep Sleep mode powered from V_{DDIO}	3.3V	1.5	7.1	µA	No backup RAM retained
BPWR_3			1.9V	1.1	4.3	µA	
BPWR_9			3.3V	1.7	11.7	µA	8 KB backup RAM retained
BPWR_11			1.9V	1.4	8.8	µA	8 KB backup RAM retained

Notes:

1. Typical value measured at 25°C and 3.3V.
2. The test conditions are as follows:
   - All GPIO are input and pulled up.
   - All peripherals disabled with PMD bits.
   - All PB clocks are divided by 16.
   - LPRC is set as LPCLK.
   - SOSC and POSC is disabled.
   - CLDO configured at lowest possible voltage (VREG Trim = 0x07).
   - DSU is disconnected.
   - RF system is in low power configuration.
   - DSWDT is enabled and configured for wake-up.
   - Deep sleep entry is configured and WFI instruction is executed.
   - 8 KB RAM WCM memory ON using WCMCFG.WCM1CFG[2:0]=1; WCMCFG.WCM2CFG[2:0]=1 for powered ON, RET + NAP mode.
   - 8 KB RAM WCM memory OFF using WCMCFG.WCM1CFG[2:0]=0; WCMCFG.WCM2CFG[2:0]=0 for powered OFF.
3. These parameters are characterized but not tested in manufacturing.

43.12 Deep Sleep Current Consumption DC Electrical Specifications (125°C)

Table 43-13. Deep Sleep Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ.(1)	Max.	Units	Conditions
BPWR_1	I_{DD_BACKUP}(2)	MCU I_{DD} in Deep Sleep mode powered from V_{DDIO}	3.3V	1.46	18.68	µA	No backup RAM retained
BPWR_3			1.9V	1.09	13.12	µA	
BPWR_9			3.3V	1.7	30.9	µA	8 KB backup RAM retained
BPWR_11			1.9V	1.34	25.17	µA	8 KB backup RAM retained

...........continued

DC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ.(1)	Max.	Units	Conditions

Notes:
1. Typical value measured at 25°C and 3.3V.
2. The test conditions are as follows:
   - All GPIO are input and pulled up.
   - All peripherals disabled with PMD bits.
   - All PB clocks are divided by 16.
   - LPRC is set as LPCLK.
   - SOSC and POSC is disabled.
   - CLDO configured at lowest possible voltage (VREG Trim = 0x07).
   - DSU is disconnected.
   - RF system is in low power configuration.
   - DSWDT is enabled and configured for wake-up.
   - Deep sleep entry is configured and WFI instruction is executed.
   - 8 KB RAM WCM memory ON using WCMCFG.WCM1CFG[2:0]=`1`; WCMCFG.WCM2CFG[2:0]=`1` for powered ON, RET + NAP Mode.
   - 8 KB RAM WCM memory OFF using WCMCFG.WCM1CFG[2:0]=`0`; WCMCFG.WCM2CFG[2:0]=`0` for powered OFF.
3. These parameters are characterized but not tested in manufacturing.

Figure 43-9. Deep Sleep Current RAM ON

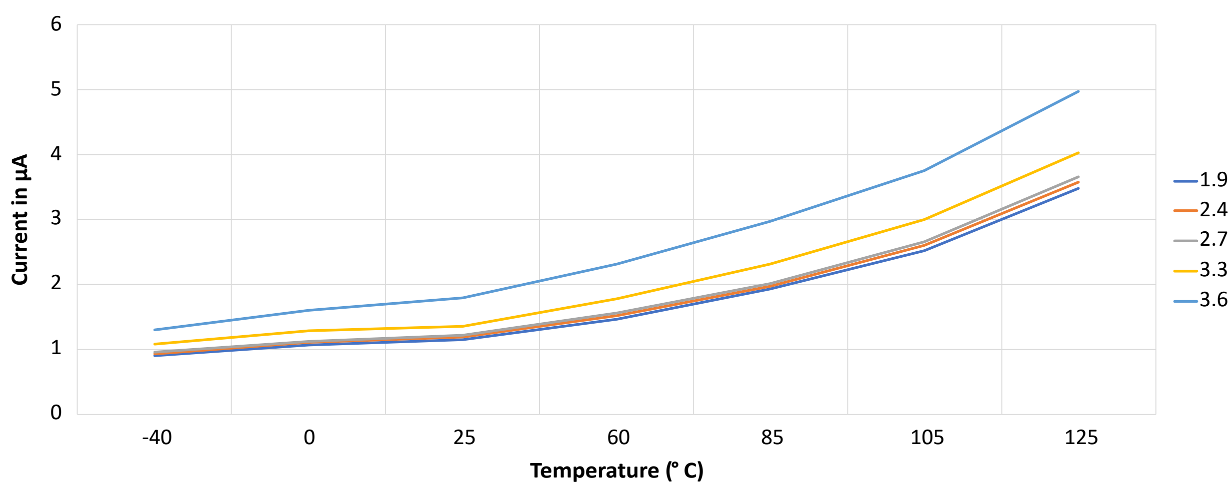
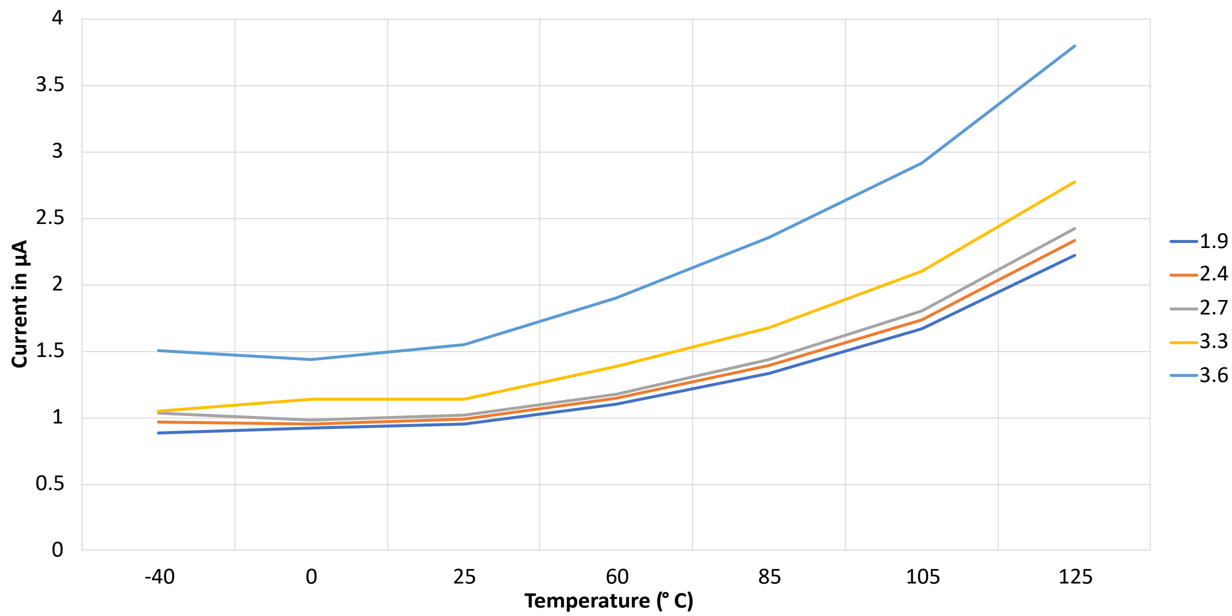


Figure 43-10. Deep Sleep Current RAM OFF



43.13 XDS (Extreme Deep Sleep) Current Consumption DC Electrical Specifications (85°C)

Table 43-14. XDS (Extreme Deep Sleep) Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ.(1)	Max.	Units	Conditions
OPWR_1	I_{DD_OFF}(2)	MCU I_{DD} in OFF mode powered from V_{DDIO}	3.3V	0.36	3.99	µA	In OFF mode, the device is entirely powered-off. **Note:** This mode is left by pulling the RESET pin low, or when a power Reset is done.
OPWR_3			1.9V	0.11	1.39		

Notes:
1. Typical value measured at 25°C and 3.3V.
2. The test conditions are as follows:
   - All GPIO are input and pulled up.
   - All peripherals disabled with PMD bits.
   - DSU is disconnected.
   - RF system is in low power configuration.
   - DSWDT is disabled.
   - RTCC and POSC is disabled.
   - Deep sleep entry is configured and WFI instruction is executed.
3. These parameters are characterized but not tested in manufacturing.

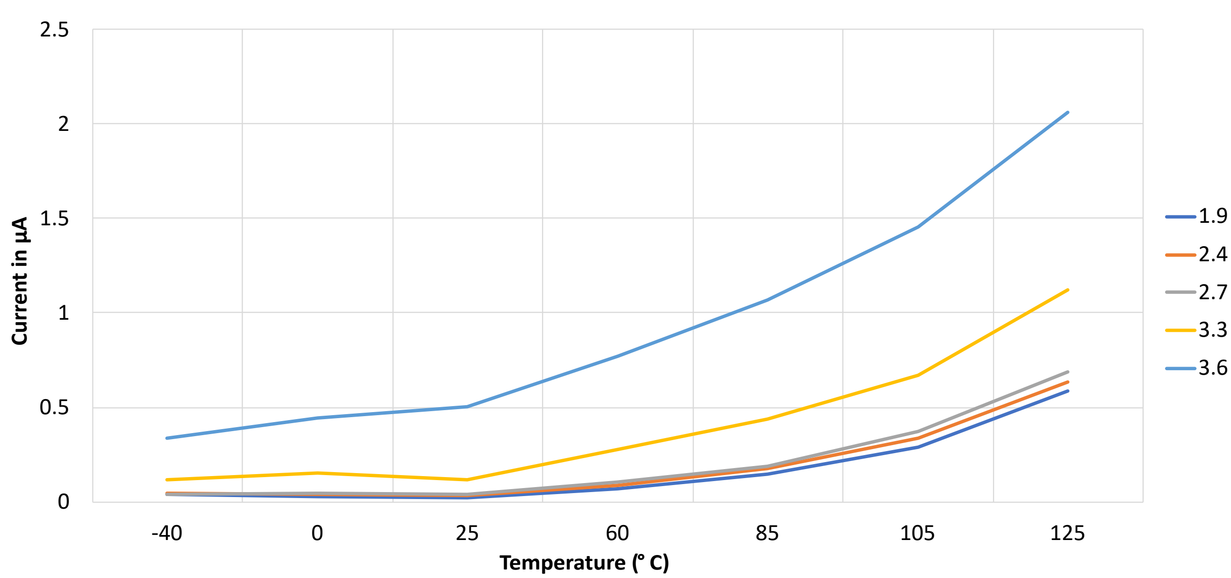
43.14 XDS (Extreme Deep Sleep) Current Consumption DC Electrical Specifications (125°C)

Table 43-15. XDS (Extreme Deep Sleep) Current Consumption DC Electrical Specifications

DC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	V_{DDIO}	Typ.(1)	Max.	Units	Conditions
OPWR_1	I_{DD_OFF}(2)	MCU I_{DD} in OFF mode powered from V_{DDIO}	3.3V	0.36	12.8	µA	In OFF mode, the device is entirely powered-off. **Note:** This mode is left by pulling the RESET pin low, or when a power Reset is done.
OPWR_3			1.9V	0.11	7.66		

Notes:
1. Typical value measured at 25°C and 3.3V.
2. The test conditions are as follows:
   - All GPIO are input and pulled up.
   - All peripherals disabled with PMD bits.
   - DSU is disconnected.
   - RF system is in low power configuration.
   - DSWDT is disabled.
   - RTCC and POSC is disabled.
   - Deep sleep entry is configured and WFI instruction is executed.
3. These parameters are characterized but not tested in manufacturing.

Figure 43-11. Extreme Deep Sleep Current



43.15 I/O PIN AC/DC Electrical Specifications

Table 43-16. I/O PIN AC/DC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ TA ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.[1]	Max.	Units	Conditions
DI_1	V_{OL}	Output voltage low (Drive strength, 8x)	—	0.25	0.53	V	V_{DDIO} = 3.6V at I_{OL}= 10 mA
		Output voltage low (Drive strength, 4x)		0.32	0.57		V_{DDIO} = 3.6V at I_{OL} = 10 mA
DI_2	V_{OL}	Output voltage low (Drive strength, 8x)	—	0.29	0.61	V	V_{DDIO} = 3.6V at I_{OL} = 13 mA
		Output voltage low (Drive strength, 4x)		0.40	0.72		V_{DDIO} = 3.6V at I_{OL}= 13 mA
DI_3	V_{OL}	Output voltage low (Drive strength, 8x)	—	0.32	0.67	V	V_{DDIO} = 3.6V at I_{OL} = 15 mA
DI_4	V_{OH}	Output voltage low (Drive strength, 8x)	2.67	3.09	—	V	V_{DDIO} = 3.6V at I_{OH} = 5 mA
		Output voltage low (Drive strength, 4x)	2.76	3.05	—		V_{DDIO} = 3.6V at I_{OH} = 5 mA
DI_5	V_{OH}	Output voltage low (Drive strength, 8x)	2.54	3.04	—	V	V_{DDIO} = 3.6V at I_{OH} = 7 mA
		Output voltage low (Drive strength, 4x)	2.54	2.95	—		V_{DDIO} = 3.6V at I_{OH} = 7 mA
DI_6	V_{OH}	Output voltage High (Drive strength, 8x)	2.319	2.96	—	V	V_{DDIO} = 3.6V at I_{OH} = 10 mA
DI_7	V_{IL}	Input voltage low (Drive strength, 8x)	—	1.46	1.56	V	V_{DDIO} = 3.6V
		Input voltage low (Drive strength, 4x)	—	1.34	1.46		V_{DDIO} = 3.6V
DI_8	V_{IH}	Input voltage high (Drive strength, 8x)	—	1.91	2.07	V	V_{DDIO} = 3.6V
		Input voltage high (Drive strength, 4x)	—	1.95	2.06		V_{DDIO} = 3.6V
DI_13	I_{IL}	Input pin leakage current	—	71.8	—	nA	With drive strength, 8x
DI_14	I_{IL}	Input pin leakage current	—	35.3	—	nA	With drive strength, 4x
DI_15	R_{PDWN}	Internal pull-down (Drive strength, 8x)	20.6	21.2	22	kΩ	V_{DDIO} = 3.6V
		Internal pull-down (Drive strength, 4x)	5.1	3.8	3.5	kΩ	
DI_17	R_{PUP}	Internal pull-up (Drive strength, 8x)	20.1	20.6	21.3	kΩ	
		Internal pull-up (Drive strength, 4x)	1.65	1.94	2.52	kΩ	
DI_19	I_{ICL}	Input low injection current	0	—	-5	mA	This parameter applies to all I/O pins. Except AV_{DD}, $\overline{MCLR}$[1,3]
DI_21	I_{ICH}	Input high injection current	0	—	5	mA	This parameter applies to all pins, with the exception of 5V tolerant I/O pins, AV_{DD}, $\overline{MCLR}$[2,3]
DI_23	$\sum I_{ICT}$	Total input injection current (sum of all I/O and control pins) Absolute value of | $\sum I_{ICT}$ |	-20	—	20	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins. (| I_{ICL} | + | I_{ICH} |) ≤ $\sum I_{ICT}$
DI_25	T_{RISE}	I/O pin rise time (High drive strength, high load)	—	2.0	7.5	ns	V_{DDIO} = 3.6V, C_{LOAD}, typical =50 $pf_{(MIN)}$
		I/O pin rise time (Low drive strength, high load)	—	10.7	19.1	ns	—
		I/O pin rise time (High drive strength, standard load)	—	2.0	5.1	ns	—
		I/O pin rise time (Low drive strength, standard load)	—	7.7	13.0	ns	—

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AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ TA ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.[1]	Max.	Units	Conditions
DI_27	T_{FALL}	I/O pin fall time (High drive strength, high load)	—	1.6	7.07	ns	—
		I/O pin fall time (Low drive strength, high load)	—	8.1	14.8	ns	—
		I/O pin fall time (High drive strength, standard load)	—	1.6	4.98	ns	—
		I/O pin fall time (Low drive strength, standard load)	—	5.1	9.9	ns	—

Notes:

1. V_{IL} source < (GND – 0.3). Characterized but not tested.
2. V_{IH} source > (VDDIO + 0.3).
3. Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted provided the absolute instantaneous sum of the input injection currents from all pins do not exceed the specified $\sum I_{ICT}$ limit. To limit the injection current, the user must insert a resistor in series R_{SERIES} (in other words, RS), between the input source voltage and device pin. The resistor value is calculated according to:
   – For negative Input voltages less than (GND – 0.3): RS ≥ absolute value of | ((V_{IL} source – (GND – 0.3)) / I_{ICL}) |
   – For positive input voltages greater than (V_{DDIO} + 0.3): RS ≥ ((V_{IH} source – (V_{DDIO} +0.3))/ I_{ICH})
   – For Vpin voltages greater than V_{DDIO} + 0.3 and less than GND – 0.3: RS = the larger of the values calculated above
4. High load = 50 pF and Standard load = 30 pF.

43.16 External XTAL and Clock AC Electrical Specifications

Table 43-17. External XTAL and Clock AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions[1]
XOSC_1	F_{OSC}_XOSC	XOSC crystal frequency	—	16	—	MHz	X_{IN}, X_{OUT} primary oscillator
XOSC_1A	TOSC	TOSC = 1/FOSC_XOSC	—	0.0625	—	µs	See parameter XOSC1 for FOSC_XOSC value
XOSC_2	XOSC_ST[2]	XOSC crystal start-up time	—	—	2.5	ms	Crystal stabilization time only not oscillator ready
XOSC_3	C_{XIN}	XOSC X_{IN} parasitic pin capacitance	—	0.35	—	pF	With default crystal trim settings
XOSC_5	C_{XOUT}	XOSC X_{OUT} parasitic pin capacitance	—	0.35	—	pF	With default crystal trim settings
XOSC_11	C_{LOAD}[3]	XOSC crystal FOSC = 16 MHz	—	9	—	pF	—
XOSC_21	ESR	XOSC crystal FOSC = 16 MHz	—	—	100	Ω	—
XOSC_33	D_{LEVEL}	MCU crystal oscillator power drive level	—	—	100	µW	—

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AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions(1)

Notes:

1. V_{DDIO} = V_{DDANA} = 3.3V.
2. This is for guidance only. A major component of crystal start-up time is based on the second party crystal MFG parasitic that are outside the scope of this specification.
3. The test conditions for crystal load capacitor calculation are as follows:
   - Standard PCB trace capacitance = 1.5 pF per 12.5 mm (0.5 inches) (in other words, PCB STD TRACE W = 0.175 mm, H = 36 µm, T = 113 µm).
   - Xtal PCB capacitance typical; therefore, ~= 2.5 pF for a tight PCB xtal layout.
   - For CXIN and CXOUT within 4 pF of each other, assume CXTAL_EFF = ((CXIN+CXOUT) / 2).
   - **Note:** Averaging CXIN and CXOUT will affect the final calculated CLOAD value by less than 0.25 pF.

   Equation 43-1. Equation 1:

   $$MFG\ \ CLOAD\ Spec = \{([CXIN + C1] * [CXOUT + C2])/[CXIN + C1 + C2 + CXOUT]\} + estimated\ oscillator\ PCB\ stray\ capacitance$$

   Assuming C1 = C2 and CXin ~= CXout, the formula can be further simplified and restated to solve for C1 and C2 by:

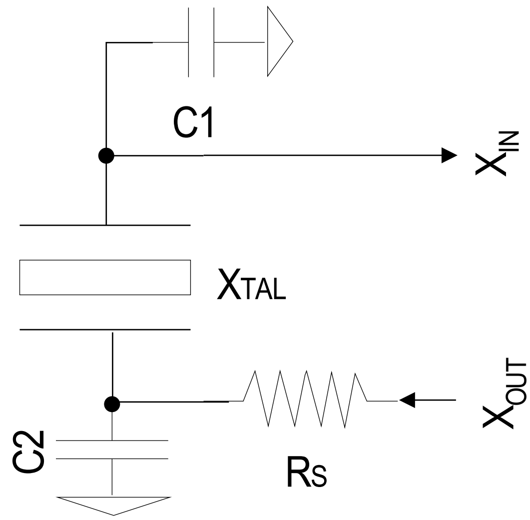
   Equation 43-2. Equation 2 (In other words: Simplified Equation 1)

   $$C1 = C2 = ((2 * MFG\ \ CLOAD\ Spec) - CXTAL\_EFF - (2 * PCB\ \ capacitance))$$

   Example:
   - XTAL Mfg CLOAD Data Sheet Spec = 12 pF
   - PCB XTAL trace Capacitance = 2.5 pF
   - CXIN pin = 6.5 pF, CXOUT pin = 4.5 pF; therefore, CXTAL_EFF = ((CXIN+CXOUT) / 2)

   CXTAL_EFF = ((6.5 + 4.5)/2) = 5.5 pF
   C1 = C2 = ((2 * MFG Cload spec) - CXTAL_EFF - (2 * PCB capacitance))
   C1 = C2 = (24 - 5.5 - (2 * 2.5))
   C1 = C2 = 13.5 pF (Always rounded down)
   C1 = C2 = 13 pF (in other words, for hypothetical example crystal external load capacitors)
   User C1 = C2 = 13 pF CLOAD (max) spec
4. These parameters are characterized but not tested in manufacturing.

Figure 43-12. External XTAL and Clock Diagram



43.17 XOSC32 AC Electrical Specifications

Table 43-18. XOSC32 AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions(1)
XOSC32_1	F_{OSC}_XOSC32	XOSC32 oscillator crystal frequency	—	32.79	—	kHz	XIN32, XOUT32 secondary oscillator
XOSC32_3	C_{XIN32}	XOSC32 XIN32 parasitic pin capacitance	—	0.4 2.4	—	pF	0.4 pF at the SOC pins and 2.4 pF on the module
XOSC32_5	C_{XOUT32}	XOSC32 XOUT32 parasitic pin capacitance	—	0.4 2.4	—	pF	0.4 pF at the SOC pins and 2.4 pF on the module
XOSC32_11	C_{LOAD}_X32(3)	32.768 kHz crystal load capacitance	—	11	—	pF	—
XOSC32_13	ESR_X32	32.768 kHz crystal ESR	—	75	100	KΩ	—
XOSC32_15	TOSC32	TOSC32 = 1/FOSC_XOSC32	—	30.5	—	µs	See parameter XOSC32_1 for FOSC_XOSC32 value
XOSC32_17	XOSC32_ST(2)	XOSC32 crystal start-up time	—	1024	—	TOSC	Crystal stabilization time only not oscillator ready

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AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions(1)

Notes:

1. V_{DDIO} = V_{DDANA} = 3.3V.
2. This is for guidance only. A major component of crystal start-up time is based on the second party crystal MFG parasitic that is outside the scope of this specification. If this is a major concern, the customer might need to characterize this based on their design choices.
3. The test conditions for crystal load capacitor calculation are as follows:
   – Standard PCB trace capacitance = 1.5 pF per 12.5 mm (0.5 inches) (in other words, PCB STD TRACE W = 0.175 mm, H = 36 µm, T = 113 µm)
   – Xtal PCB capacitance typical; therefore, ~= 2.5 pF for a tight PCB xtal layout
   – For CXIN and CXOUT within 4 pF of each other, assume CXTAL_EFF = ((CXIN / 2)
   – **Note:** Averaging CXIN and CXOUT will affect the final calculated CLOAD value by less than the tolerance of the capacitor selection.

   Equation 1:

   $$MFG\ \ CLOAD\ Spec = \{([CXIN + C1] * [CXOUT\ \ + C2])/[CXIN + C1 + C2 + CXOUT]\} + estimated\ oscillator\ PCB\ stray\ capacitance$$

   Assuming C1 = C2 and CXin ~= CXout, the formula can be further simplified and restated to solve for C1 and C2 by:

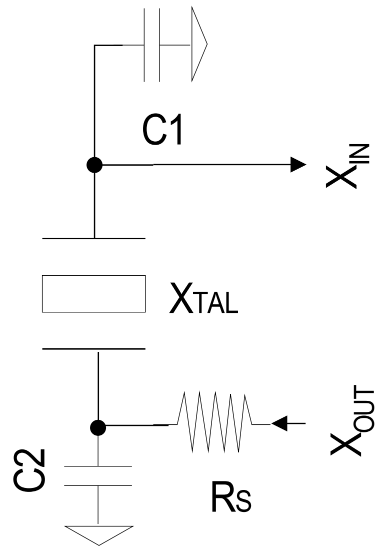
   Equation 43-3. Equation 2 (In other words: Simplified Equation 1)

   $$C1 = C2 = ((2 * MFG\ \ CLOAD\ Spec) - CXTAL\_EFF - (2 * PCB\ \ capacitance))$$

   Example:
   - XTAL Mfg CLOAD Data Sheet Spec = 12 pF
   - PCB XTAL trace Capacitance = 2.5 pF
   - CXIN pin = 6.5 pF, CXOUT pin = 4.5 pF therefore CXTAL_EFF = ((CXIN / 2)

   CXTAL_EFF = ((6.5 + 4.5)/2) = 5.5 pF
   C1 = C2 = ((2 * MFG Cload spec) - CXTAL_EFF - (2 * PCB capacitance))
   C1 = C2 = (24 - 5.5 - (2 * 2.5))
   C1 = C2 = (24 - 5.5 - 5)
   C1 = C2 = 13.5 pF (Always rounded down)
   C1 = C2 = 13 pF (in other words, for hypothetical example crystal external load capacitors)
   User C1 = C2 = 13 pF ≤ CLOAD_X32 (max.) spec
4. User selectable in OSC32KCTRL.STARTUP.
5. These parameters are characterized but not tested in manufacturing.

Figure 43-13. XOSC32 Block Diagram



43.18 Low Power Internal 32 kHz RC Oscillator AC Electrical Specifications

Table 43-19. Low Power Internal 32 kHz RC Oscillator AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
LP32K_1	FOSC_LPRC32K	Output frequency	23.5	—	40.3	kHz	V_{DDIO} = V_{DDANA} ≥ V_{DDANA}(min) -40°C ≤ T_A ≤ +125°C
LP32K_2	FOSC_LPRC32K	Output frequency	26.1	32.7	36.6	kHz	V_{DDIO} = V_{DDANA} ≥ V_{DDANA}(min) -40°C ≤ T_A ≤ +85°C (in other words, Factory default calibration)
LP32K_9	RC32K_Duty	LPRC32K OSC duty cycle	—	50	—	%	V_{DDIO} = V_{DDANA} ≥ V_{DDANA}(min)
Note: These parameters are characterized but not tested in manufacturing.							

43.19 FRC AC Electrical Specifications

Table 43-20. FRC AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
FRC1	FINTFREQ	Internal FRC frequency	—	8	—	MHz	Factory calibrated with tune bits set to 0x0
FRC2	TSUFRC	Start-up time of internal FRC	—	15	—	µs	—
FRC3	FACCU	FRC accuracy	—	5	—	%	—
FRC5	DUTY_CYCLE	FRC duty cycle	45	50	55	%	—

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AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
FRC6	C_USE	FRC user tune	-1.625	6.299	1.615	%	Frequency drift = [(Maximum frequency measured - Minimum frequency measured)/(Default frequency of 8 MHz)] * 100; Maximum frequency drift possible by using the frequency trim bits
FRC7	C_USER_STEP_SIZE	FRC user tune step size	0.0467	0.046	0.0472	%	Step size = (% Drift across Osc tune)/(Total number of trim bit combinations); Change in frequency with incremental trim bit
Note: These parameters are characterized but not tested in manufacturing.							

43.20 Frequency AC Electrical Specifications

Table 43-21. Frequency AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
MCU_1	FCY	MCU frequency of operation	—	—	64	MHz	$V_{DDIO(min)}$ to $V_{DDIO(max)}$
MCU_3	TCY	MCU clock period	1/FCY			ns	—
Note: These parameters are characterized but not tested in manufacturing.							

PLL (Phase Locked Loop) AC Electrical Specifications

Table 43-22. PLL MHz (Phase Locked Loop)

AC Characteristics FDPLLxxMHz (Fractional Digital Phase Locked Loop)			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
PLL_1	PLL_F_{IN}	PLL input frequency	—	16	—	MHz	Over full voltage and temperature operating ranges
PLL_3	PLL_F_{OUT}	PLL output clock frequency	—	96	—	MHz	—
PLL_4	PLL_VCO_FREQ	PLL VCO frequency	—	480	—	MHz	—
Notes: 1. PLL input clock is 16 MHz XTAL. 2. These parameters are characterized but not tested in manufacturing.							

43.21 ADC Electrical Specifications

Table 43-23. ADC AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
Device Supply							
ADC_1	V_{DDANA}	ADC module supply	$V_{DDANA(min)}$	—	$V_{DDANA(max)}$	V	$V_{DDIO} = V_{DDANA}$
Reference Inputs							
ADC_3	V_{REF}(4)	Reference voltage high (external reference buffers)	—	—	V_{DDANA}	V	ADC reference voltage
Analog Input Range							
ADC_7	A_{FS}	Full-scale analog input signal range (Single-ended)	0	—	V_{DDANA}	V	$V_{REF} = V_{DDANA(max)}$

Table 43-24. ADC Single-Ended Mode AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: $V_{DDIO} = V_{DDANA}$ 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
Single-Ended Mode ADC Accuracy							
SADC_11	Res	Resolution	6	—	12	bits	Selectable 8, 10, 12 bit resolution ranges
SADC_13	ENOB(3)	Effective number of bits	6.08	9.8	10.7	bits	2 Msps, Internal V_{REF}, $V_{DDANA} = V_{DDIO}$ = 3.3V
SADC_19	INL(3)	Integral non linearity	-2.9	-1.18	1.9	LSb	2 Msps, Internal V_{REF}, $V_{DDANA} = V_{DDIO}$ = 3.3V
SADC_25	DNL(3)	Differential non linearity	-1.4	1.29	2.59	LSb	2 Msps, Internal V_{REF}, $V_{DDANA} = V_{DDIO}$ = 3.3V
SADC_31	GERR(3)	Gain error	11.90	18.93	25.00	LSb	2 Msps, Internal V_{REF}, $V_{DDANA} = V_{DDIO}$ = 3.3V
SADC_37	EOFF(3)	Offset error	-8.1	-1.6	1.0	LSb	2 Msps, Internal V_{REF}, $V_{DDANA} = V_{DDIO}$ = 3.3V
Single-Ended Mode ADC Dynamic Performance							
SADC_49	SINAD(1,2,3)	Signal to noise and distortion	38.4	61.1	66.8	dB	$V_{REF} = V_{DDANA} = V_{DDIO}$ = 3.3V at 12-bit resolution, max sampling rate(1,2)
SADC_51	SNR(1,2,3)	Signal to noise ratio	38.4	61.8	67.3		
SADC_53	SFDR(1,2,3)	Spurious free dynamic range	61.5	70.3	81.3		
SADC_55	THD(1,2,3)	Total harmonic distortion	-84.0	-70.1	-59.8		

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AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions

Notes:

1. Characterized with an analog input sine wave = (FTP(max)/100). Example: FTP(max) = 1 Msps/100 = 10 kHz sine wave.
2. Sine wave peak amplitude = 96% ADC_ Full Scale amplitude input with 12-bit resolution.
3. Spec values collected under the following additional conditions:
   a. 12-bit resolution mode
   b. All registers at reset default value otherwise not mentioned
4. ADC measurements done with 3.3V V_{REF} voltage.
5. Value taken over 7 harmonics.
6. Referred to as AVDD in the pinout.

Table 43-25. ADC Conversion AC Electrical Requirements

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
ADC_ Clock Requirements							
ADC_57	TAD	ADC clock period	—	20.83	—	ns	V_{REF} = V_{DDANA} = 3.3V
ADC Single-Ended Throughput Rates							
ADC_59	F_{TPR} (Single-ended mode)	Throughput rate(3) (Single-ended)	0.01	—	2	Msps	12-bit resolution, DIV_SHR = 2

Note:

1. Throughput Rate = 1/((SAMC_SHR +15)*TADX)
   TADX=1/ (ADC Control Clock / DIV_SHR) ,SAMC_SHR = sampling rate

Table 43-26. ADC Sample AC Electrical Requirements

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
ADC_63	T_{SAMP}	ADC sample time [1,2,3,4]	1[1,4]	—	—	TAD	12-bit TAD(min), Ext Analog Input Rsource ≤ 147Ω
							10-bit TAD(min), Ext Analog Input Rsource ≤ 504Ω
							8-bit TAD(min), Ext Analog Input Rsource ≤ 1,000Ω
			2[1,4]	—	—		12-bit TAD(min), Ext Analog Input Rsource ≤ 2,272Ω
							10-bit TAD(min), Ext Analog Input Rsource ≤ 3,008Ω
							8-bit TAD(min), Ext Analog Input Rsource ≤ 4,000Ω
			3[1,4]	—	—		12-bit TAD(min), Ext Analog Input Rsource ≤ 4,416Ω
							10-bit TAD(min), Ext Analog Input Rsource ≤ 5,504Ω
							8-bit TAD(min), Ext Analog Input Rsource ≤ 6,976Ω
			4[1,2,4]	—	—		12-bit TAD(min), Ext Analog Input Rsource ≤ 6,560Ω
							10-bit TAD(min), Ext Analog Input Rsource ≤ 8,000Ω
							8-bit TAD(min), Ext Analog Input Rsource ≤ 9,984Ω
			5[1,4]	—	—		12-bit TAD(min), Ext Analog Input Rsource ≤ 8,704 Ω
							10-bit TAD(min), Ext Analog Input Rsource ≤ 10,496Ω
							8-bit TAD(min), Ext Analog Input Rsource ≤ 12,992Ω
			6[1,4,5]	—	—		12-bit TAD(min), Ext Analog Input Rsource ≤ 10,880Ω
							10-bit TAD(min), Ext Analog Input Rsource ≤ 12,992Ω
							8-bit TAD(min), Ext Analog Input Rsource ≤ 16,000Ω
ADC_65	T_{CNV}	Conversion time [3] (Single-Ended mode)	14			TAD	12-bit resolution
			12				10-bit resolution
			10				8-bit resolution
ADC_69	C_{SAMPLE}	ADC internal sample cap	4	5	6	pf	—
ADC_71	R_{SAMPLE}	ADC internal impedance	—	—	200	Ω	—

...........continued

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions

Notes:

1. When SAMPCTRL.OFFCOMP=`0`:
   - TSAMP = (((RSAMPLE + RSOURCE) * CSAMPLE * (#Bits Resolution + 2) * ln(2))/TAD)+1 rounded down to nearest whole integer
   - User SAMPCTRL.SAMPLEN = (TSAMP – 1)
2. When SAMPCTRL.OFFCOMP=`1`:
   - TSAMP = 4 (Forced by HDW)
   - User SAMPCTRL.SAMPLEN = (n/a, Ignored by HDW)
3. ADC Throughput Rate FTP = ((1/((TSAMP + TCNV) * TAD))/(# of user active analog inputs in use on specific target ADC module))
   Note: Specification values assume only one AINx channel in use.
4. TSAMP ≥ (INT[((RSAMPLE + RSOURCE) * CSAMPLE * (#Bits Resolution+2) * ln(2))/TAD]+1).
5. For RSOURCE values exceeding TSAMP = 6 sample time condition, use the formula in note 5 to calculate.

43.22 Comparator AC Electrical Specifications

Table 43-27. Comparator AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.(1)	Max.	Units	Conditions
CMP_1	VIOFF_00	Input offset voltage	-16	—	16	mV	V_{DDANA} = $V_{DDIO\ (min\text{-}to\text{-}max)}$
CMP_3	VICM	Input Common mode voltage	0	—	AV_{DD}	V	V_{DDANA} = $V_{DDIO\ (min\text{-}to\text{-}max)}$
CMP_4	VIN	Input voltage range	AV_{SS}	—	AV_{DD}	V	With respect to GND and V_{DDANA}
CMP_15	$TRESP_{SS}$	Small signal response time	—	100	160	ns	V_{DDANA} = $V_{DDIO\ (min\text{-}to\text{-}max)}$, Comparator ref voltage = V_{DDANA}/2, Input overdrive = ± 100 mV
CMP_19	C_{OUTVAL}	Comparator enabled to output valid	—	31	—	µs	Comparator module is configured before enabling it
CMP_21	AC_{IREF}	Comparator internal band gap voltage reference	1.164	—	1.236	V	V_{DDANA} = 3.3V, T = 25°C (±-3%) - Uncalibrated
CMP_22			1.194	—	1.206	V	V_{DDANA} = 3.3V, T = 25°C (±-0.5%) - Calibrated
CMP_23	$C_{VREFRNG}$	Comparator voltage reference input range	AV_{SS}	—	AV_{DD}	V	—
CMP_25	F_{GCLK_AC}	Analog comparator peripheral module clock freq	—	—	64	MHz	V_{DDANA} = $V_{DDIO\ (min\text{-}to\text{-}max)}$

...........continued

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.[1]	Max.	Units	Conditions

Notes:
1. These parameters are characterized but not tested in manufacturing.
2. Values in typical column area taken at 25°C.
3. Comparator Ref voltage cannot exceed: (VIN(max) – VIOFF(max) – CMP_5(max) - 50 mV) ≥ CMP VREF ≥ (VIN(min) + VIOFF(min) + CMP_5(max) + 50 mV)

43.23 SPI Module Electrical Specifications

Table 43-28. SPI Module Host Mode Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ TA ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
MSP_1	FSCK	SCK frequency	—	—	32	MHz	Fixed pins
			—	—	24		Remappable pins
MSP_2	TSCK	SCK time period	31.25		—	ns	Fixed pins
			41.66	—			Remappable pins
MSP_3	TSCL	SCK output low time	—	tsck/2	—	ns	—
MSP_5	TSCH	SCK output high time	—	tsck/2	—	ns	—
MSP_7	TSCF	SCK and MOSI output fall time	—	—	8.0	ns	C_{LOAD} = 50 pF See parameter DI27 I/O spec
					6.0		C_{LOAD} = 20 pF See parameter DI27 I/O spec
MSP_9	TSCR	SCK and MOSI output rise time	—	—	8.0	ns	C_{LOAD} = 50 pF See parameter DI27 I/O spec
					6.0		C_{LOAD} = 20 pF See parameter DI27 I/O spec
MSP_11	TMOV	MOSI Data output valid after SCK	—	11	17	ns	$V_{DDIO(Min)}$, C_{LOAD} = 30 $pF_{(MIN)}$
MSP_13	TMOH	MOSI hold after SCK	5	—	—	ns	
MSP_15	TMIS	MISO setup time of data input to SCK	5	—	—	ns	
MSP_17	TMIH	MISO hold time of data input to SCK	5	—	—	ns	

Figure 43-14. SPI Host Module CPHA=0 Timing Diagrams

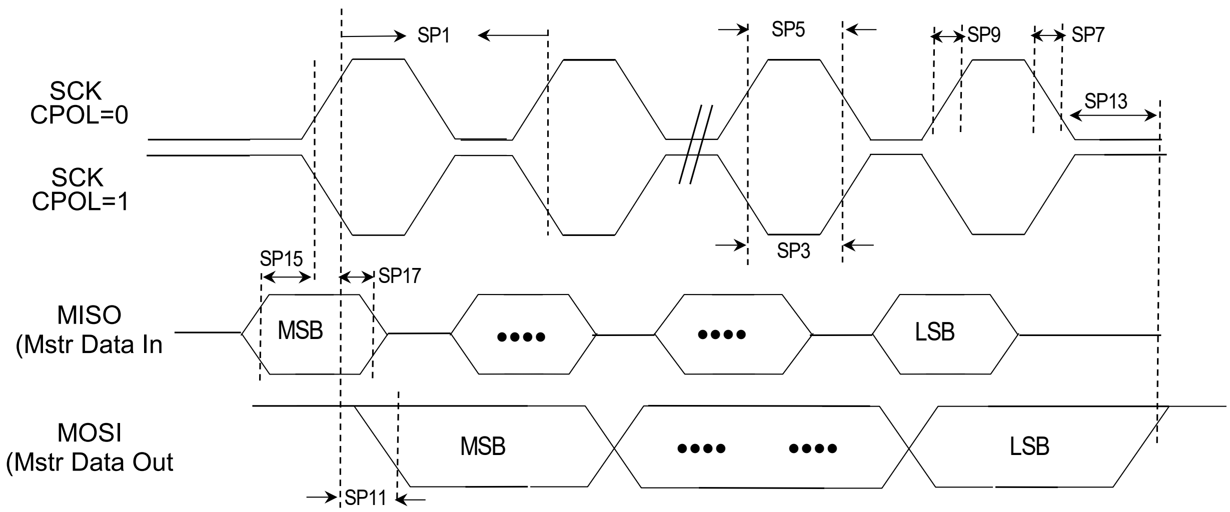
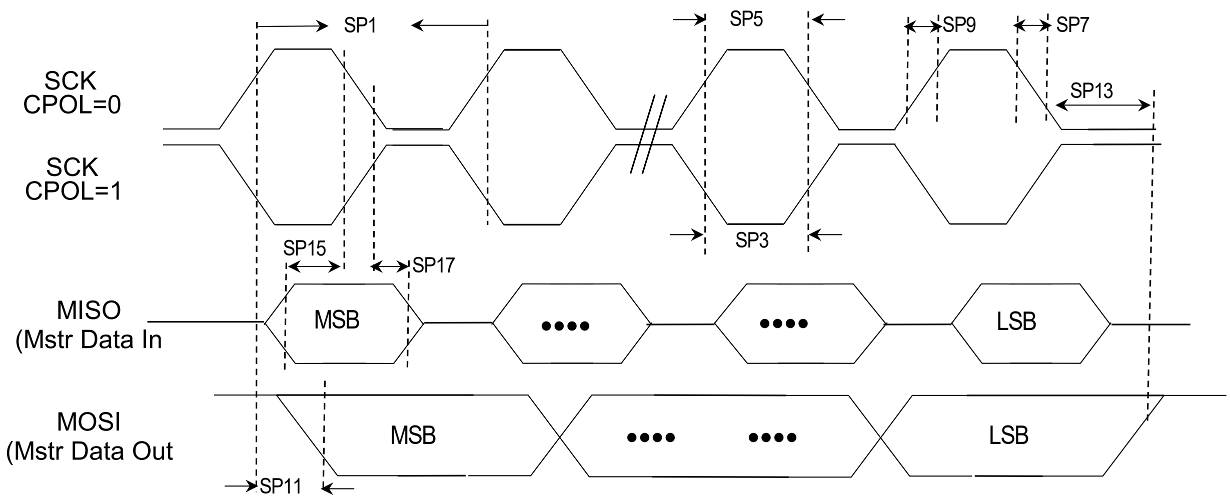


Figure 43-15. SPI Host Module CPHA=1 Timing Diagrams



Note:

1. Assumes $V_{DDIO(min)}$ and 30 pF external load on all SPIx pins unless otherwise noted.

Table 43-29. SPI Module Client Mode Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ TA ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
SSP_1	FSCK	SCK frequency	—	—	16	MHz	V_{DDIO} = 1.9V or $V_{DDIO(min)}$ whichever is greater, C_{LOAD} = 30 $pF_{(MIN)}$ fixed pins
			—	—	12		Remappable pins
SSP_2	TSCK	SCK time period	62.5	—	—	ns	V_{DDIO} = 1.9V or $V_{DDIO(min)}$ whichever is greater, C_{LOAD} = 30 $pF_{(MIN)}$
			83.3	—	—		—

...........continued

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ TA ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
SSP_3	TSCL	SCK output low time	—	tsck/2	—	ns	—
SSP_5	TSCH	SCK output high time	—	tsck/2	—	ns	—
SSP_7	TSCF	SCK and MOSI output fall time	—	—	8.0 6.0	ns	C_{LOAD} = 50 pF C_{LOAD} = 20 pF See parameter DI27 I/O spec
SSP_9	TSCR	SCK and MOSI output rise time	—	—	8.0 6.0	ns	C_{LOAD} = 50 pF C_{LOAD} = 20 pF See parameter DI27 I/O spec
SSP_11	TSOV	MOSI data output valid after SCK	—	—	17	ns	V_{DDIO} = 3.3V, C_{LOAD} = 30 $pF_{MIN)}$
SSP_15	TSIS	MISO setup time of data input to SCK	5	—	—	ns	
SSP_17	TSIH	MISO hold time of data input to SCK	0	—	—	ns	
SSP_23	SPI_GCLK	SERCOM SPI input clock frequency, GCLK_SPI	—	—	64	MHz	—

Figure 43-16. SPI Client Module CPHA=0 Timing Diagrams

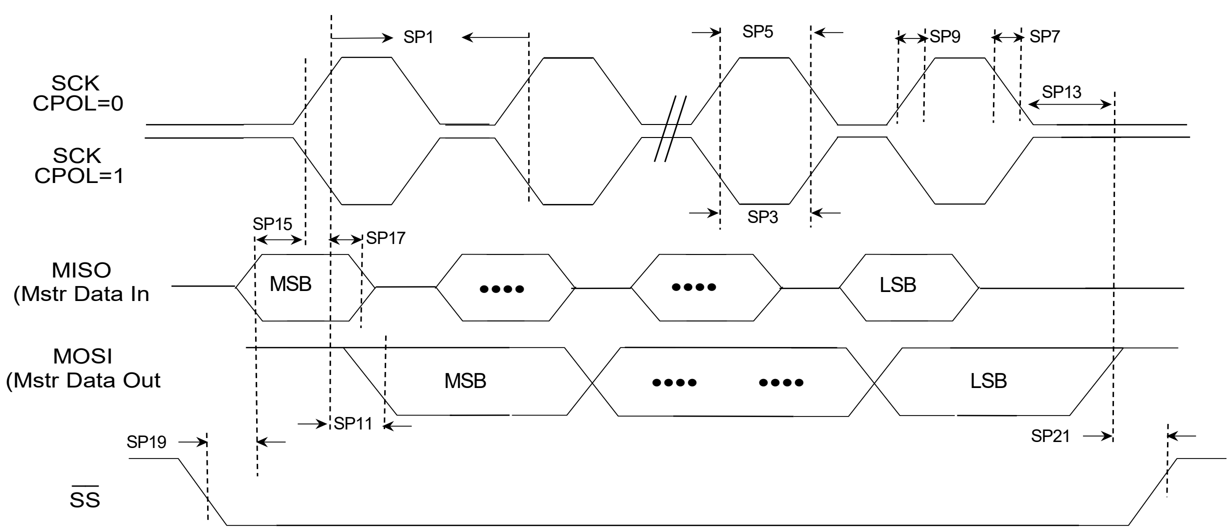
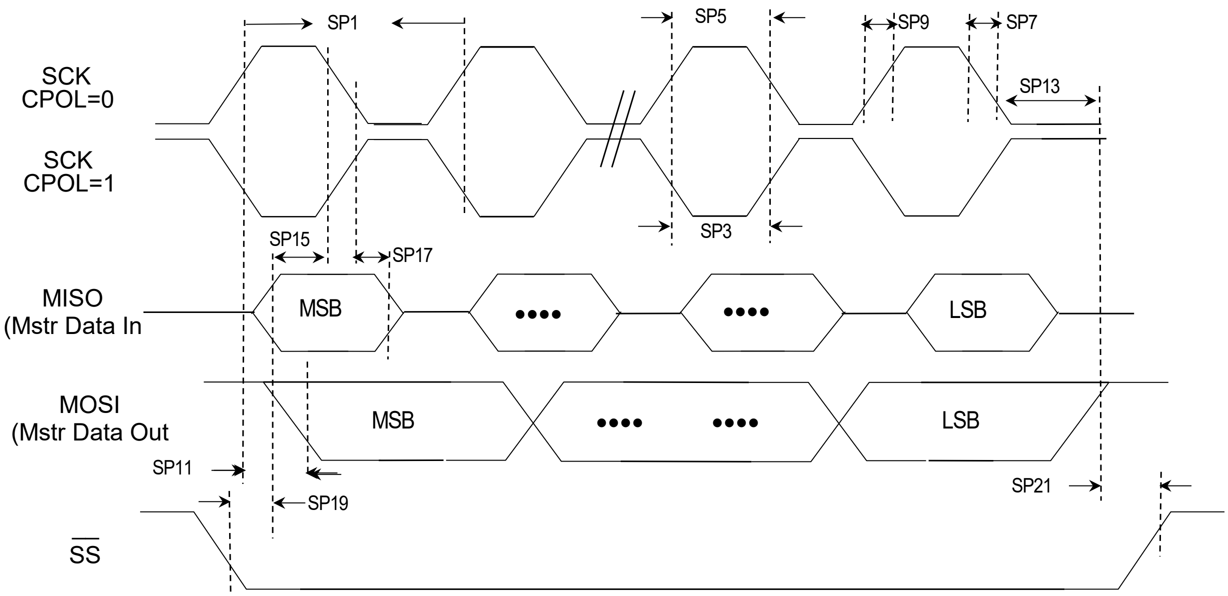


Figure 43-17. SPI Client Module CPHA=1 Timing Diagrams



43.24 UART AC Electrical Specifications

Table 43-30. UART AC Electrical Specifications

AC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics		Min.	Typ.	Max.	Units	Conditions
UT_1	F_{BRATE}	Baud rate	Asynchronous SAMPR = 16x mode	—	—	Asynchronous arithmetic formula(2)	Mbps	V_{DDIO} = 3.3V
UT_3			Asynchronous SAMPR = 8x mode	—	—	Asynchronous arithmetic formula(2)	Mbps	V_{DDIO} = 3.3V
UT_5			Asynchronous SAMPR = 3x mode	—	—	Asynchronous arithmetic formula(2)	Mbps	V_{DDIO} = 3.3V
UT_19			Synchronous mode	—	—	Synchronous formula(2)	Mbps	—
UT_23	F_{USART}	USART max GCLK_SERCOM		—	—	64	MHz	—
UT_25	F_{XCK}	USART external clock input		—	—	32	MHz	—

Notes:

1. These parameters are characterized, but not tested in manufacturing.
2.

Operating Mode	Condition	Baud Rate (Bits Per Second)	Baud Register Value Calculation
Asynchronous arithmetic	$f_{BAUD} \leq \frac{f_{ref}}{S}$	$f_{BAUD} = \frac{f_{ref}}{S}\left(1 - \frac{BAUD}{65536}\right)$	$BAUD = 65536 \cdot \left(1 - S \cdot \frac{f_{BAUD}}{f_{ref}}\right)$
Synchronous	$f_{BAUD} \leq \frac{f_{ref}}{2}$	$f_{BAUD} \leq \frac{f_{ref}}{2 \cdot (BAUD + 1)}$	$BAUD = \frac{f_{ref}}{2 \cdot f_{BAUD}} - 1$

43.25 I²C Module Electrical Specifications

Table 43-31. I²C Module Host Mode Electrical Specifications

AC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics		Min.	Typ.	Max.	Units	Conditions
I2CM_1	TLO:SCL	Host clock low time	100 kHz mode	4700	—	—	ns	V_{DDIO} = 3.3V, C_{LOAD} = 400 pf
			400 kHz mode	1300	—	—	ns	
			1 MHz mode	500	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pf
I2CM_3	THI:SCL	Host clock high time	100 kHz mode	450	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pf
			400 kHz mode	650	—	—	ns	
			1 MHz mode	130	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pf
I2CM_5	TF:SCL	SDAx and SCLx fall time	100 kHz mode	—	—	250	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	20 + (0.1 * C_{LOAD})	—	250	ns	
			1 MHz mode	20 + (0.1 * C_{LOAD})	—	250	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF REXT*CLOAD>13 ns. REXT, external series resistor, must not exceed 1Kohms.
I2CM_7	TR:SCL	SDAx and SCLx rise time	100 kHz mode	—	—	100	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	20 + (0.1 * C_{LOAD})	—	300	ns	
			1 MHz mode	—	—	120	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_9	TSU:DAT	Data input setup time	100 kHz mode	51	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	51	—	—	ns	
			1 MHz mode	51	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_11	THD:DAT	Data input hold time	100 kHz mode	71	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	71	—	—	ns	
			1 MHz mode	71	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_13	TSU:STA	Start condition setup time	100 kHz mode	tlow +7	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	tlow +7	—	—	ns	
			1 MHz mode	tlow +7	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF

...........continued

AC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics		Min.	Typ.	Max.	Units	Conditions
I2CM_15	THD:STA	Start condition hold time	100 kHz mode	tlow -9	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	tlow -9	—	—	ns	
			1 MHz mode	tlow -9	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_17	TSU:ST0	Stop condition setup time	100 kHz mode	Tlow +9	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	Tlow +9	—	—	ns	
			1 MHz mode	Tlow +9	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_19	THD:ST0	Stop condition hold time	100 kHz mode	tlow -9	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	tlow -9	—	—	ns	
			1 MHz mode	tlow -9	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_21	TAA:SCL	Output valid from clock	100 kHz mode	—	—	280	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	—	—	280	ns	
			1 MHz mode	—	—	280	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CM_23	TBF:SDA	Bus free time(1)	100 kHz mode	tlow	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	tlow	—	—	ns	
			1 MHz mode	tlow	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF

Note:

1. The amount of time the bus must be free before a new transmission can start (STOP condition to START condition).

Figure 43-18. I^2C Start/Stop Bits Host Mode AC Timing Diagram

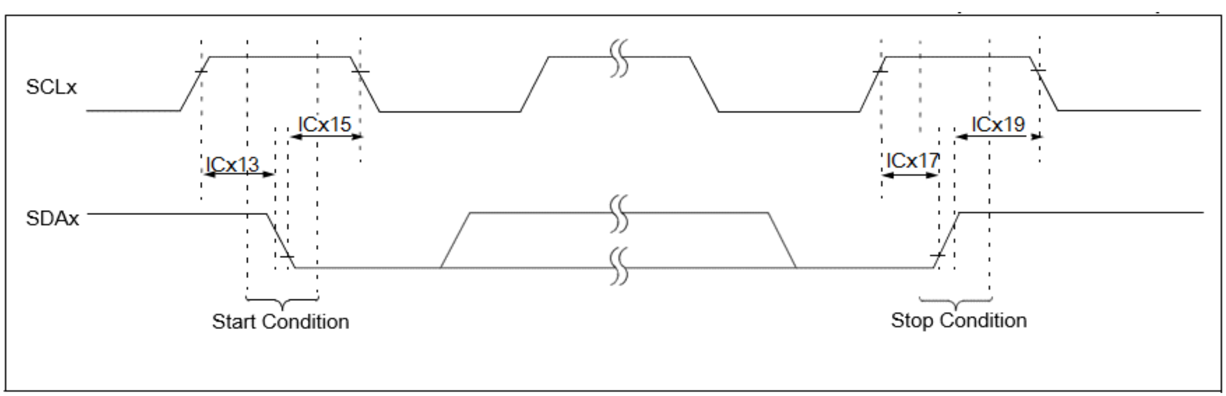


Figure 43-19. I^2C Bus Data Host Mode AC Timing Diagram

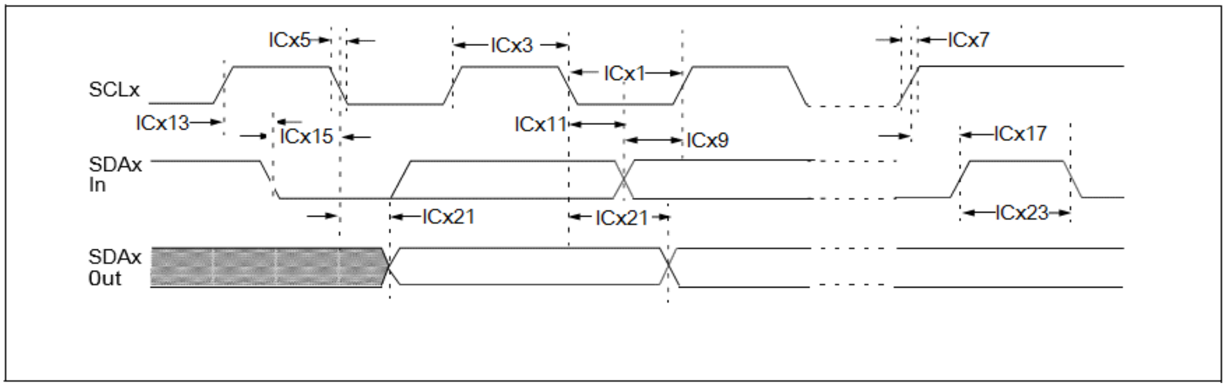


Table 43-32. I^2C Module Client Mode Electrical Specifications

AC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended Temp			
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
I2CS_1	TL0:SCL	Client clock low time	100 kHz mode	4700	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	1300	—	ns	
			1 MHz mode	500	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CS_3	THI:SCL	Client clock high time	100 kHz mode	4050	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	650	—	ns	
			1 MHz mode	130	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CS_5	TF:SCL	SDAx and SCLx fall time	100 kHz mode	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	20 + (0.1 * CLoad)	—	ns	
			1 MHz mode	20 + (0.1 * CLoad)	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CS_7	TR:SCL	SDAx and SCLx rise time	100 kHz mode	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	20 + (0.1 * CLoad)	—	ns	
			1 MHz mode	—	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CS_9	TSU:DAT	Data input setup time	100 kHz mode	51	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	51	—	ns	
			1 MHz mode	51	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF

...........continued

AC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended Temp			
Param. No.	Symbol	Characteristics		Min.	Max.	Units	Conditions
I2CS_11	THD:DAT	Data input hold time	100 kHz mode	71	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	71	—	ns	
			1 MHz mode	71	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CS_13	TSU:STA	Start condition setup time	100 kHz mode	tlow +7	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	tlow +7	—	ns	
			1 MHz mode	tlow +7	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CS_15	THD:STA	Start condition hold time	100 kHz mode	tlow -9	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	tlow -9	—	ns	
			1 MHz mode	tlow -9	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CS_17	TSU:ST0	Stop condition setup time	100 kHz mode	Tlow +9	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	Tlow +9	—	ns	
			1 MHz mode	Tlow +9	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CS_19	THD:ST0	Stop condition hold time	100 kHz mode	tlow -9	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	tlow -9	—	ns	
			1 MHz mode	tlow -9	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CS_21	TAA:SCL	Output valid from clock	100 kHz mode	—	220	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	—	220	ns	
			1 MHz mode	—	220	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF
I2CS_23	TBF:SDA	Bus free time(1)	100 kHz mode	tlow	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 3 mA, C_{LOAD} = 400 pF
			400 kHz mode	tlow	—	ns	
			1 MHz mode	tlow	—	ns	V_{DDIO} = 3.3V, $I_{PULL-UP}$ = 20 mA, C_{LOAD} = 550 pF

Note:

1. The amount of time the bus must be free before a new transmission can start (STOP condition to START condition).

Figure 43-20. I²C Start/Stop Bits Client Mode AC Timing Diagram

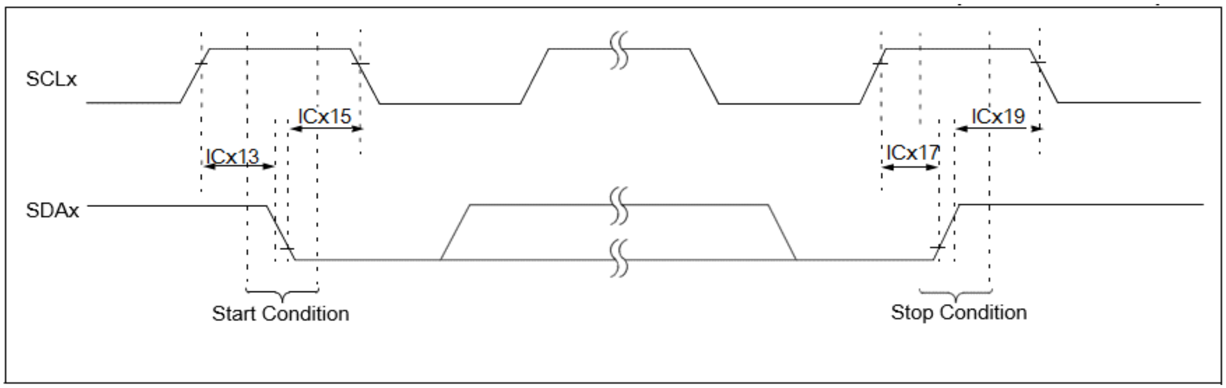
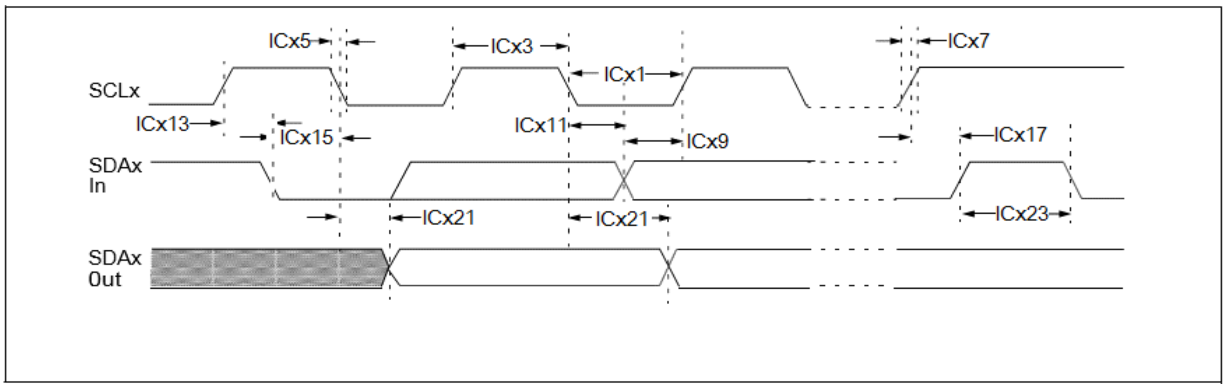


Figure 43-21. I²C Bus Data Client Mode AC Timing Diagram



43.26 QSPI Module Electrical Specifications

Table 43-33. QSPI Module Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.(1)	Max.	Units	Conditions
QSPI_1	FCLK	QSPI serial clock frequency • SDR Host mode 0 and 2	—	—	32	MHz	V_{DDIO} = 3.3V, C_{LOAD} = 30 $pF_{(MIN)}$
QSPI_2	FCLK	QSPI serial clock frequency • SDR Host mode 1 and 3	—	—	32	MHz	V_{DDIO} = 3.3V, C_{LOAD} = 30 $pF_{(MIN)}$
QSPI_3	TSCKH	Serial clock high time	—	8.9	—	ns	—
QSPI_5	TSCKL	Serial clock low time	—	7.8	—	ns	—
QSPI_7	TSCKR	Serial clock rise time	—	6.9	—	ns	See parameter DI27 I/O spec
QSPI_9	TSCKF	Serial clock fall time	—	7.6	—	ns	See parameter DI25 I/O spec
QSPI_11	TCSS	CS active setup time	—	7.3	—	ns	—
QSPI_13	TCSH	CS active hold time	—	10.4	—	ns	—

...........continued

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.(1)	Max.	Units	Conditions
QSPI_19	TDIS	Data in setup time	—	2.4	—	ns	—
QSPI_21	TDIH	Data in hold time	—	1.023	—	ns	—
QSPI_23	TDOH	Data out hold	—	1.17	—	ns	—
QSPI_25	TDOV	Data out valid	—	1.48	—	ns	—
QSPI_27	QSPI_GCLK	QSPI peripheral clock frequency	—	—	64	MHz	—

Notes:
1. Assumes V_{DDIO}(typ) and typical external load on all SQI pins unless otherwise noted.
2. These parameters are characterized but not tested in manufacturing.

Figure 43-22. QSPI SDR Host Mode 0,1,2,3 Module Timing Diagram

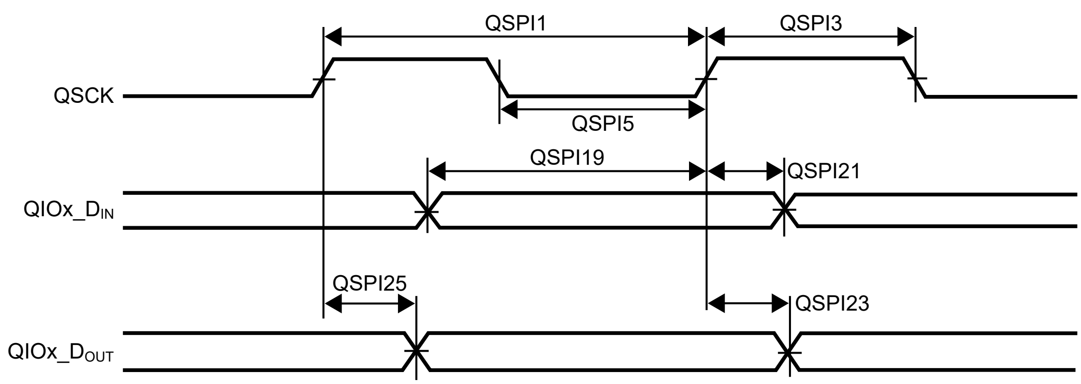


Figure 43-23. QSPI DDR Mode 0 Write Timing Diagram

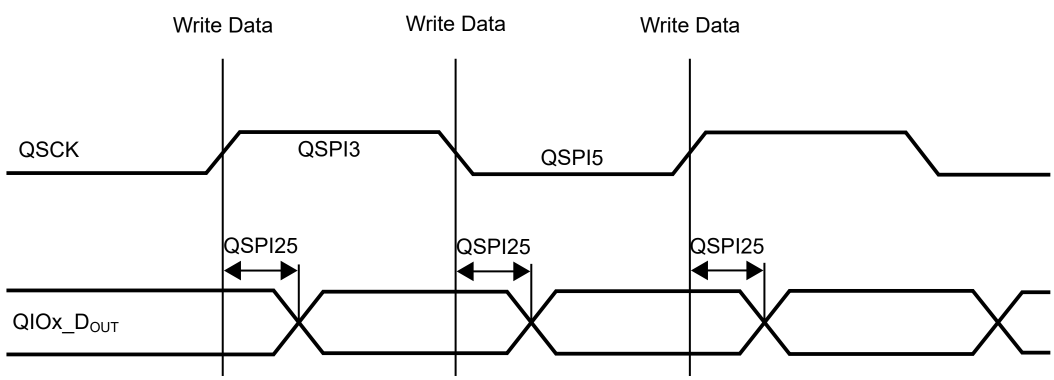
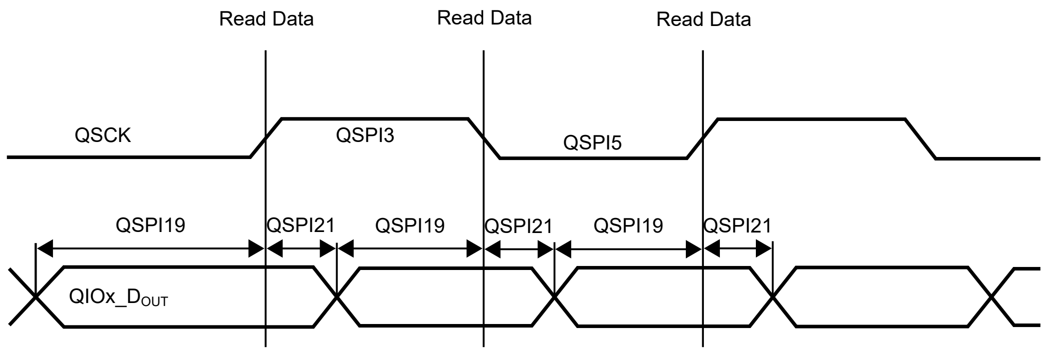


Figure 43-24. QSPI DDR Mode 0 Read Timing Diagram



43.27 TCx Timer Capture Module AC Electrical Specifications

Table 43-34. TCx Timer Capture Module AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
TC_1	TC_{INLOW}	Capture TCx input low time	2/fGLK_TCx	—	—	ns	V_{DDIO} = 3.3V and meet TC_5 spec
TC_3	TC_{INHIGH}	Capture TCx input high time	2/fGLK_TCx	—	—	ns	V_{DDIO} = 3.3V and meet TC_5 spec
TC_5	$TC_{INPERIOD}$	Capture input period	4/fGLK_TCx	—	—	ns	V_{DDIO} = 3.3V
TC_7	TC_{OUTLOW}	Compare TCx output low time	1/fGCLK_TCx	—	—	ns	V_{DDIO} = 3.3V and meet TC_11 spec
TC_9	$TC_{OUTHIGH}$	Compare TCx output high time	1/fGCLK_TCx	—	—	ns	V_{DDIO} = 3.3V and meet TC_11 spec
TC_11	$TC_{OUTPERIOD}$	Compare output period	2/fGCLK_TCx	—	—	ns	V_{DDIO} = 3.3V
TC_13	fGCLK_TCx	TC peripheral module clock frequency	—	—	64	MHz	$V_{DDIO(min)}$
Note: These parameters are characterized but not tested in manufacturing.							

Figure 43-25. TCx Timer Capture Input Module AC Timing Diagram

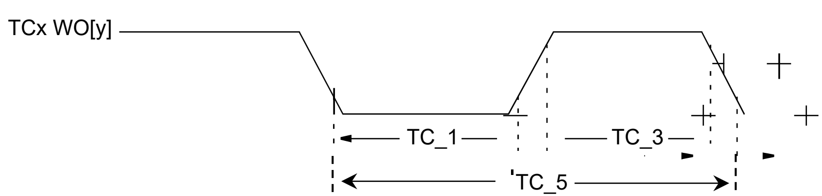
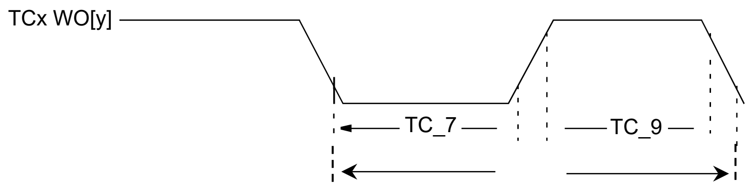


Figure 43-26. TCx Timer Capture Output Module AC Timing Diagram



43.28 TCCx Timer Capture Module AC Electrical Specifications

Table 43-35. TCCx Timer Capture Module AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
TCC_1	TCC_{INLOW}	Capture TCCx input low time	2/fGLK_TCCx	—	—	ns	$V_{DDIO(min)}$ and meet TCC_5 spec
TCC_3	TCC_{INHIGH}	Capture TCCx input high time	2/fGLK_TCCx	—	—	ns	$V_{DDIO(min)}$ and meet TCC_5 spec
TCC_5	$TCC_{INPERIOD}$	Capture input period	4/fGLK_TCCx	—	—	ns	$V_{DDIO(min)}$
TCC_7	TCC_{OUTLOW}	Compare TCCx output low time	1/fGCLK_TCx	—	—	ns	$V_{DDIO(min)}$ and meet TCC_11 spec
TCC_9	$TCC_{OUTHIGH}$	Compare TCCx output high time	1/fGCLK_TCx	—	—	ns	$V_{DDIO(min)}$ and meet TCC_11 spec
TCC_11	$TCC_{OUTPERIOD}$	Compare output period	2/fGCLK_TCx	—	—	ns	$V_{DDIO(min)}$
TCC_13	fGCLK_TCCx	TCC peripheral module clock frequency	—	—	64	MHz	
TCC_15	TCC_{FD}	Fault input to I/O pin change	—	—	63	ns	
TCC_17	TCC_{FLT}	Fault input pulse width	10	—	—	ns	

Figure 43-27. TCCx Timer Capture Input Module AC Timing Diagram

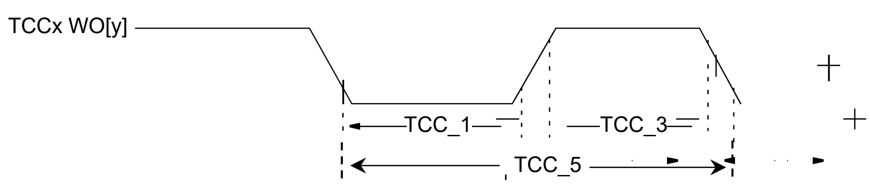


Figure 43-28. TCCx Timer Capture Output Module AC Timing Diagram

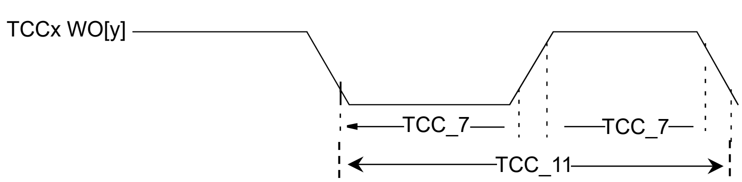
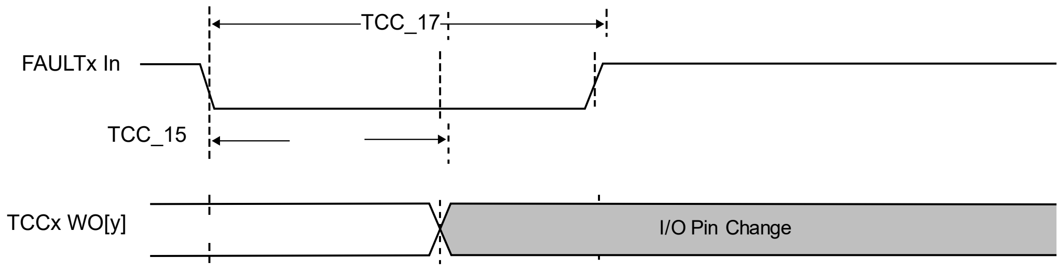


Figure 43-29. TCC_x Timer Compare Fault Output Module AC Timing Diagram



43.29 FLASH NVM AC Electrical Specifications

Table 43-36. FLASH NVM AC Electrical Specifications

AC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics		Min.	Typ.	Max.	Units	Conditions
NVM_1	F_{RETEN}	Flash data retention		—	15	—	Yrs	Under all conditions less than absolute maximum ratings specifications
NVM_3	EP	Cell endurance (Flash erase and Write operation)		—	100k	—	Cycles	
NVM_5	F_{READ}	Flash read	0 wait states	—	—	16	MHz	V_{DDIO} = 3.3V
			1 wait states	—	—	32		
			2 wait states	—	—	64		
			3 wait states	—	—	64		
			4 wait states	—	—	64		
			5 wait states	—	—	64		
NVM_7	T_{FPW}	Program cycle time	Row write	—	2.5	—	ms	—
NVM_9	T_{CE}		Erase chip	—	20	—	ms	

Note:

1. The maximum FLASH operating frequencies are given in the table above but are limited by the Embedded Flash access time when the processor is fetching code out of it. This field defines the number of Wait states required to access the Embedded Flash Memory.

43.30 Frequency Meter AC Electrical Specifications

Table 43-37. Frequency Meter AC Electrical Specifications

AC Characteristics			Standard Operating Conditions: V_{DD} = 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
FM_1	FM_{LOW}	GCLK_IOx input low time	—	15.625	—	ns	$V_{DDIO\ (min)}$ and meet FM5 spec
FM_3	FM_{HIGH}	GCLK_IOx input high time	—	15.625	—	ns	
FM_5	FM_{PERIOD}	GCLK_IOx input period	—	31.25	—	ns	$V_{DDIO\ (min)}$
FM_7	fGCLK_FREQM_REF	FREQM reference	—	—	64	MHz	
FM_9	fGCLK_FREQM_MSR	FREQM measure	—	—	64	MHz	

43.31 Bluetooth® Low Energy RF Characteristics

Table 43-38. WBZ45 Bluetooth Low Energy RF Characteristics

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ TA ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
BTG1	FREQ	Frequency range of operation	2402	—	2480	MHz	—
BTTX1	TXPWR:MPA	Bluetooth® transmit power MPA	—	11.67	—	dBm	—
BTTX2	TXPWR:LPA	Bluetooth transmit power LPA	—	3.95	—	dBm	—
BTX3	TXIB:1MBPS	In-band emission for FTX ± -2 MHz	—	-32	—	dBm	—
		In-band emission for FTX ± -(3+N) MHz	—	-45	—	dBm	—
BTX4	TXIB:2MBPS	In-band emission for FTX ± -4 MHz	—	-43	—	dBm	—
		In-band emission for FTX ± -5 MHz	—	-48	—	dBm	—
		In-band emission for FTX ± -(6+N) MHz	—	-51	—	dBm	—
BTRX1	RXSENSE	Receiver sensitivity at 1 Mbps	—	-97	—	dBm	—
		Receiver sensitivity at 2 Mbps	—	-94	—	dBm	—
		Receiver sensitivity at S = 8	—	-104	—	dBm	—
		Receiver sensitivity at S = 2	—	-101	—	dBm	—
BTRX2	MAXINSIG	Maximum input signal level at 1 Mbps	—	0	—	dBm	—
		Maximum input signal level at 2 Mbps	—	0	—	dBm	
		Maximum input signal level at S = 2	—	0	—	dBm	
		Maximum input signal level at S = 8	—	0	—	dBm	
BTRX3(3)	CI1M:COCH	C/I Co channel rejection	—	8	—	dB	—
	CI1M: ± -1MHz	C/I adjacent channel rejection	—	1	—	dB	—
	CI1M: ± -2MHz	C/I adjacent channel rejection	—	-30	—	dB	—
	CI1M:ADJ(3+n)	C/I alternate channel rejection	—	-48	—	dB	—
	CI1M:IMG	C/I image frequency rejection	—	-24	—	dB	—
	CI1M:IMG ± -1 MHz	C/I adjacent channel to image freq rejection	—	-31	—	dB	—
BTRX4(3)	CIS2:COCH	C/I Co channel rejection	—	6	—	dB	—
	CIS2: ± -1MHz	C/I adjacent channel rejection	—	-6	—	dB	—
	CIS2: ± -2MHz	C/I adjacent channel rejection	—	-38	—	dB	—
	CIS2:ADJ(3+n)	C/I alternate channel rejection	—	-50	—	dB	—
	CIS2:IMG	C/I image frequency rejection	—	-27	—	dB	—
	CIS2:IMG ± -1 MHz	C/I adjacent channel to image freq rejection	—	-37	—	dB	—
BTRX5(3)	CIS8:COCH	C/I Co channel rejection	—	7	—	dB	—
	CIS8: ± -1 MHz	C/I adjacent channel rejection	—	-7	—	dB	—
	CIS8: ± -2 MHz	C/I adjacent channel rejection	—	-38	—	dB	—
	CIS8:ADJ(3+n)	C/I alternate channel rejection	—	-48	—	dB	—
	CIS8:IMG	C/I image frequency rejection	—	-27	—	dB	—
	CIS2:IMG ± -1MHz	C/I adjacent channel to image freq rejection	—	-41	—	dB	—

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AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ TA ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
BTRX6(3)	CI2M:COCH	C/I Co channel rejection	—	8	—	dB	—
	CI2M: ± -2MHz	C/I adjacent channel rejection	—	1	—	dB	—
	CI2M: ± -4MHz	C/I adjacent channel rejection	—	-29	—	dB	—
	CI2M:ADJ(6+2n)	C/I alternate channel rejection	—	-42	—	dB	—
	CI2M:IMG	C/I image frequency rejection	—	-23	—	dB	—
	CI2M:IMG ± -2MHz	C/I adjacent channel to image freq rejection	—	-28	—	dB	—
BTRX7(3)	BLOCK1M:<2GHZ	Blocking performance from 30-2 GHz	—	-10	—	dBm	—
	BLOCK1M:2 GHZ<SIG<2399MHz	Blocking performance from 2003-2399 MHz	—	-21	—	dBm	—
	BLOCK1M:2484 MHZ<SIG<2977MHz	Blocking performance between 2484-2997 MHz	—	-15	—	dBm	—
	BLOCK1M:3 GHZ<SIG<12.75GHz	Blocking performance between 3-12.5 GHz	—	-10	—	dBm	—
BTRX8(3)	BLE1M:INTERMOD	Inter modulation performance for BLEM	—	-36	—	dBm	—
	BLE2M:INTERMOD	Inter modulation performance for BLEM	—	-28.5	—	dBm	—

Notes:

1. Measured at 25℃ averaged across all voltages and channels.
2. Measured on a board with the reference schematic.
3. All measurement across voltage based on the SIG specifications.
4. PDU length = 37, channels = 2402/2426/2440/2480 MHz.

Table 43-39. WBZ451H Bluetooth Low Energy RF Characteristics

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
BTG1	FREQ	Frequency range of operation	2402	—	2480	MHz	—
BTX1	TXPWR:WBZ451H	Bluetooth® transmit power at 3.3V	—	19.8	—	dBm	—
		Bluetooth transmit power at 2.5V	—	18.6	—	dBm	—
		Bluetooth transmit power at 1.9V	—	16.8	—	dBm	—
BTX2	TXIB:1MBPS	In-band emission for FTX ± 2 MHz	—	-26.2	—	dBm	—
		In-band emission for FTX ± (3+N) MHz	—	-37.8	—	dBm	—
BTX3	TXIB:2MBPS	In-band emission for FTX ± 4MHz	—	-34.6	—	dBm	—
		In-band emission for FTX ± 5 MHz	—	-40.1	—	dBm	—
		In-band emission for FTX ± (6+N) MHz	—	-43.3	—	dBm	—
BTRX1	RXSENSE	Receiver sensitivity at 1 Mbps	—	-99.6	—	dBm	—
		Receiver sensitivity at 2 Mbps	—	-96.6	—	dBm	—
		Receiver sensitivity at S = 8	—	-107.1	—	dBm	—
		Receiver sensitivity at S = 2	—	-103.6	—	dBm	—

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AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
BTRX2	MAXINSIG	Maximum input signal level at 1 Mbps	—	-10	—	dBm	—
		Maximum input signal level at 2 Mbps	—	-10	—	dBm	—
		Maximum input signal level at S = 2	—	-10	—	dBm	—
		Maximum input signal level at S = 8	—	-10	—	dBm	—
BTRX3	CI1M:COCH	C/I Co channel rejection	—	14	—	dB	—
	CI1M:± 1MHz	C/I adjacent channel rejection	—	14	—	dB	—
	CI1M:± 2MHz	C/I adjacent channel rejection	—	12	—	dB	—
	CI1M:ADJ(3+n)	C/I alternate channel rejection	—	9	—	dB	—
	CI1M:IMG	C/I image frequency rejection	—	13	—	dB	—
	CI1M:IMG± 1MHz	C/I adjacent channel to image frequency rejection	—	12	—	dB	—
BTRX4	CIS2:COCH	C/I Co channel rejection	—	12	—	dB	—
	CIS2:± 1MHz	C/I adjacent channel rejection	—	19	—	dB	—
	CIS2:± 2MHz	C/I adjacent channel rejection	—	15	—	dB	—
	CIS2:ADJ(3+n)	C/I alternate channel rejection	—	15	—	dB	—
	CIS2:IMG	C/I image frequency rejection	—	11	—	dB	—
	CIS2:IMG± 1MHz	C/I adjacent channel to image frequency rejection	—	16	—	dB	—
BTRX5	CIS8:COCH	C/I Co channel rejection	—	8	—	dB	—
	CIS8:± 1MHz	C/I adjacent channel rejection	—	15	—	dB	—
	CIS8:± 2MHz	C/I adjacent channel rejection	—	11	—	dB	—
	CIS8:ADJ(3+n)	C/I alternate channel rejection	—	14	—	dB	—
	CIS8:IMG	C/I image frequency rejection	—	7	—	dB	—
	CIS2:IMG± 1MHz	C/I Adjacent channel to image frequency rejection	—	14	—	dB	—
BTRX6	CI2M:COCH	C/I Co channel rejection	—	15	—	dB	—
	CI2M:± 2MHz	C/I adjacent channel rejection	—	18	—	dB	—
	CI2M:± 4MHz	C/I adjacent channel rejection	—	16	—	dB	—
	CI2M:ADJ(6+2n)	C/I alternate channel rejection	—	9	—	dB	—
	CI2M:IMG	C/I image frequency rejection	—	13	—	dB	—
	CI2M:IMG± 2MHz	C/I adjacent channel to image frequency rejection	—	18	—	dB	—
BTRX7	BLOCK1M:<2GHZ	Blocking performance from 30 MHz to 2 GHz	—	20	—	dB	—
	BLOCK1M:2GHZ<SIG<2399MHz	Blocking performance from 2003 MHz to 2399 MHz	—	20	—	dB	—
	BLOCK1M:2484MHZ<SIG<2977MHz	Blocking performance between 2484 MHz to 2997 MHz	—	20	—	dB	—
	BLOCK1M:3GHZ<SIG<12.75GHz	Blocking Performance between 3 GHz to 12.5 GHz	—	20	—	dB	—
BTRX8	BLE1M:INTERMOD	Inter-modulation performance for BLEM	—	10.5	—	dB	—
	BLE2M:INTERMOD	Inter-modulation performance for BLEM	—	14.5	—	dB	—

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AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions

Notes:
1. Sensitivity related items are covering voltage range from 1.9V to 3.6V.
2. Except for the dedicated voltage condition case, the TX related items are operating voltage from 1.9V to 3.6V.

Table 43-40. WBZ45 Bluetooth Low Energy LPA RF Characteristics

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ	Max.	Units	Conditions
BTLG1	FREQ	Frequency range of operation	2402	—	2480	MHz	—
BTLTX2	TXPWR:LPA	Bluetooth® transmit power LPA	—	5.47	—	dBm	—
BTLX3	TXIB:1MBPS	In-band emission for FTX ± 2 MHz	—	-40	—	dBm	—
		In-band emission for FTX ± (3+N) MHz	—	-49	—	dBm	—
BTX4	TXIB:2MBPS	In-band emission for FTX ± 4 MHz	—	-46	—	dBm	—
		In-band emission for FTX ± 5 MHz	—	-51	—	dBm	—
		In-band emission for FTX ± (6+N) MHz	—	-54	—	dBm	—
BTLRX1	RXSENSE	Receiver sensitivity at 1Mbps	—	-97	—	dBm	—
		Receiver sensitivity at 2 Mbps	—	-94	—	dBm	—
		Receiver sensitivity at S = 8	—	-104	—	dBm	—
		Receiver sensitivity at S = 2	—	-101	—	dBm	—
BTLRX2	MAXINSIG	Maximum Input signal level at 1 Mbps	—	0	—	dBm	—
		Maximum Input signal level at 2 Mbps	—	0	—	dBm	—
		Maximum Input signal level at S = 2	—	0	—	dBm	—
		Maximum Input signal level at S = 8	—	0	—	dBm	—

Notes:
1. Measured at 25℃ averaged across all voltages and channels.
2. Measured on a board with the reference schematic.
3. All measurement across voltage based on the SIG specifications.
4. PDU length = 37, channels = 2402/2426/2440/2480 MHz.

Table 43-41. WBZ45 Bluetooth Low Energy RF Current Characteristics

AC Characteristics					Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	RF Power	CPU Frequency	Min.	Typ.	Max.	Units	Conditions
IBLETX1	IDDTXMPA	Current consumption with output power in DC-DC mode 1 Mbps	+12 dBm	64 MHz	—	42.8	—	mA	—
IBLETX4		Current consumption at +12 dBm output power in MLDO mode	+12 dBm	64 MHz	—	96.7	—	mA	—
IBLETX7	IDDTXLPA	Current consumption at +4 dBm output power in DC-DC mode 1 Mbps	4 dBm	64 MHz	—	24.9	—	mA	—
IBLETX10		Current consumption at +4 dBm output power in MLDO mode	4 dBm	64 MHz	—	55.5	—	mA	—
IBLETX7	IDDTXLPA0	Current consumption at +0 dBm output power in DC-DC mode 1 Mbps	0 dBm	64 MHz	—	22.7	—	mA	—
IBLETX10		Current consumption at 0 dBm output power in MLDO mode	0 dBm	64 MHz	—	47.6	—	mA	—
IBLERX1	IDDRXBLE1M	Current consumption at RX signal level -80 dBm in DC-DC mode	-80 dBm	64 MHz	—	20.6	—	mA	—
IBLERX4		Current consumption at RX signal level -80 dBm in MLDO mode	-80 dBm	64 MHz	—	40.6	—	mA	—

Notes:
- Current consumption is measured on a board based upon the Microchip Technology Reference Design.
- Current consumption is for the entire SoC (including the MCU) measured at the input power rail.
- Current reported is the average of the current during the transmit or receive burst (exclude off cycle of the transmit/ receive operation).

Table 43-42. WBZ451H Bluetooth Low Energy RF Current Characteristics

AC Characteristics					Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp				
Param. No.	Symbol	Characteristics	RF Power	CPU Frequency	Min.	Typ.	Max.	Units	Conditions
IBLETX1	IDDTXWBZ451H	Current consumption at +19.5 dBm output power in DC-DC mode 1 Mbps	+19.5 dBm	64 MHz	—	139.7	—	mA	—
IBLETX2			+19.5 dBm	48 MHz	—	138.9	—	mA	—
IBLETX3	IDDTXWBZ451H	Current consumption at +15 dBm output power in DC-DC mode 1 Mbps	+15 dBm	64 MHz	—	87.9	—	mA	—
IBLETX4			+15 dBm	48 MHz	—	86.8	—	mA	—
IBLETX5		Current consumption at +15 dBm output power in MLDO mode	+15 dBm	64 MHz	—	96.9	—	mA	—
IBLETX6			+15 dBm	48 MHz	—	94.5	—	mA	—
IBLETX7	IDDTXWBZ451H	Current consumption at +10 dBm output power in DC-DC mode 1 Mbps	+10 dBm	64 MHz	—	64.1	—	mA	—
IBLETX8			+10 dBm	48 MHz	—	62.9	—	mA	—
IBLETX9		Current consumption at +10 dBm output power in MLDO mode	+10 dBm	64 MHz	—	76.5	—	mA	—
IBLETX10			+10 dBm	48 MHz	—	74.3	—	mA	—
IBLETX11	IDDTXWBZ451H	Current consumption at 0 dBm output power in DC-DC mode 1 Mbps	+0 dBm	64 MHz	—	44.6	—	mA	—
IBLETX12			+0 dBm	48 MHz	—	43.6	—	mA	—
IBLETX13		Current consumption at 0 dBm output power in MLDO mode	+0 dBm	64 MHz	—	60.5	—	mA	—
IBLETX14			+0 dBm	48 MHz	—	57.9	—	mA	—
IBLETX15	IDDTXBYP	Current consumption at -4 dBm output power in DC-DC mode 1 Mbps	-4 dBm	64 MHz	—	25.4	—	mA	—
IBLETX16			-4 dBm	48 MHz	—	24.2	—	mA	—
IBLETX17		Current consumption at -4 dBm output power in MLDO mode	-4 dBm	64 MHz	—	48.2	—	mA	—
IBLETX18			-4 dBm	48 MHz	—	46.1	—	mA	—

...........continued

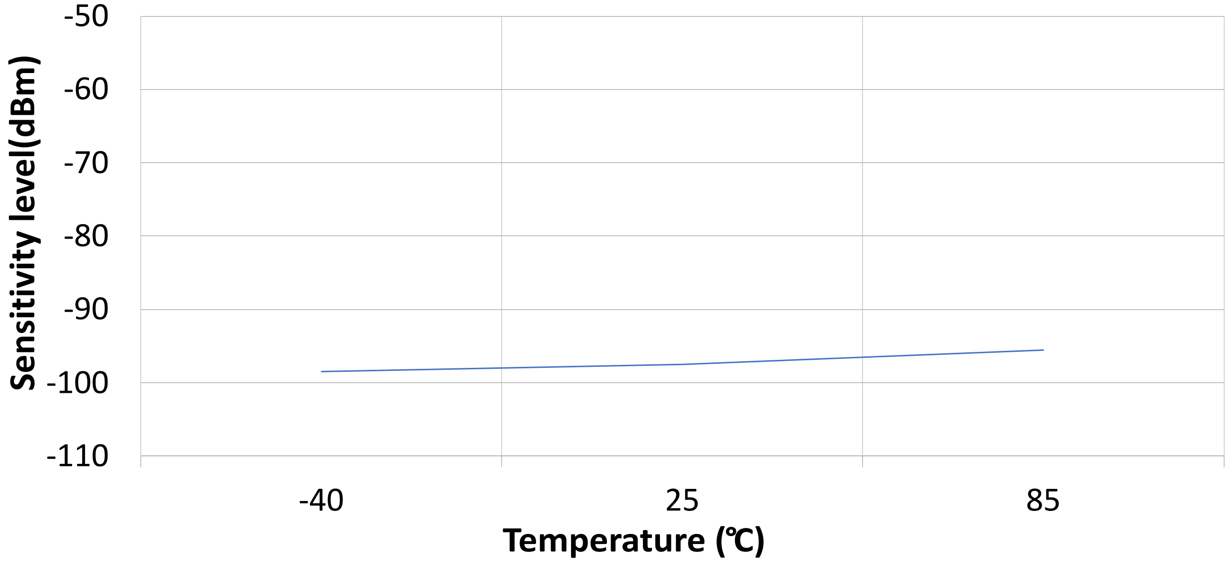
AC Characteristics					Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp				
Param. No.	Symbol	Characteristics	RF Power	CPU Frequency	Min.	Typ.	Max.	Units	Conditions
IBLERX1	IDDRXBLE1M	Current consumption at RX signal level -80 dBm in DC-DC mode	-80 dBm	64 MHz	—	25.8	—	mA	—
IBLERX2			-80 dBm	48 MHz	—	24.6	—	mA	—
IBLERX3		Current consumption at RX signal level -80 dBm in MLDO mode	-80 dBm	64 MHz	—	43.9	—	mA	—
IBLERX4			-80 dBm	48 MHz	—	41.5	—	mA	—

Note:
1. DC-DC mode operation in 3.3V; MLDO mode operation in 1.9V.

Table 43-43. WBZ45 Bluetooth Low Energy RF Current LPA Characteristics

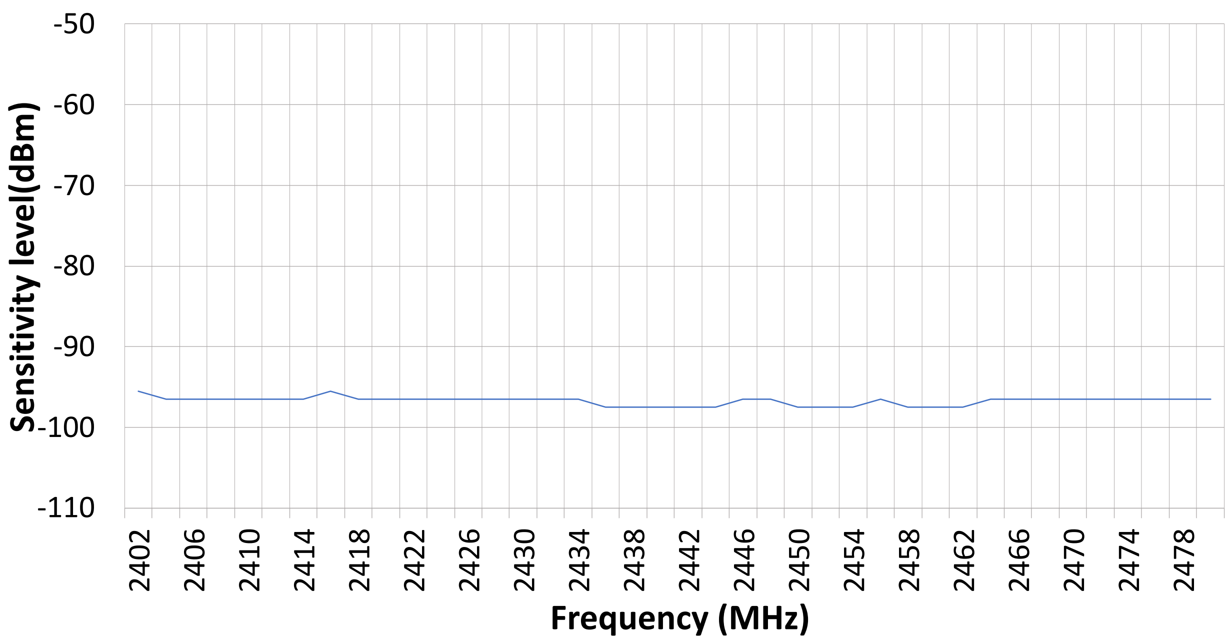
AC Characteristics					Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9-3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	RF Power	CPU Frequency	Min.	Typ.	Max.	Units	Conditions
IBLETX1	IDDTXMPA	Current consumption with output power 5.5 dBm in DC-DC mode 1 Mbps	+5.5 dBm	64 MHz	—	24.1	—	mA	V_{DD} = 3.3V
IBLETX4		Current consumption at +5.5 dBm output power in MLDO mode	+5.5 dBm	64 MHz	—	46.9	—	mA	V_{DD} = 3.3V
IBLETX7	IDDTXLPA	Current consumption at +0 dBm output power in DC-DC mode 1 Mbps	0 dBm	64 MHz	—	20.6	—	mA	V_{DD} = 3.3V
IBLETX10		Current consumption at +0 dBm output power in MLDO mode 1 Mbps	0 dBm	64 MHz	—	40.4	—	mA	V_{DD} = 3.3V
IBLETX7	IDDTXLPA0	Current consumption at -5 dBm output power in DC-DC mode 1 Mbps	-5 dBm	64 MHz	—	19.2	—	mA	V_{DD} = 3.3V
IBLETX10		Current consumption at -5 dBm output power in MLDO mode 1 Mbps	-5 dBm	64 MHz	—	37.5	—	mA	V_{DD} = 3.3V
IBLERX1	IDDRXBLE1M	Current consumption at RX signal level -80 dBm in DC-DC mode	-80 dBm	64 MHz	—	21.2	—	mA	V_{DD} = 3.3V
IBLERX4		Current consumption at RX signal level -80 dBm in MLDO mode	-80 dBm	64 MHz	—	39.9	—	mA	V_{DD} = 3.3V

Figure 43-30. Module Bluetooth Low Energy Receive Sensitivity vs Temperature



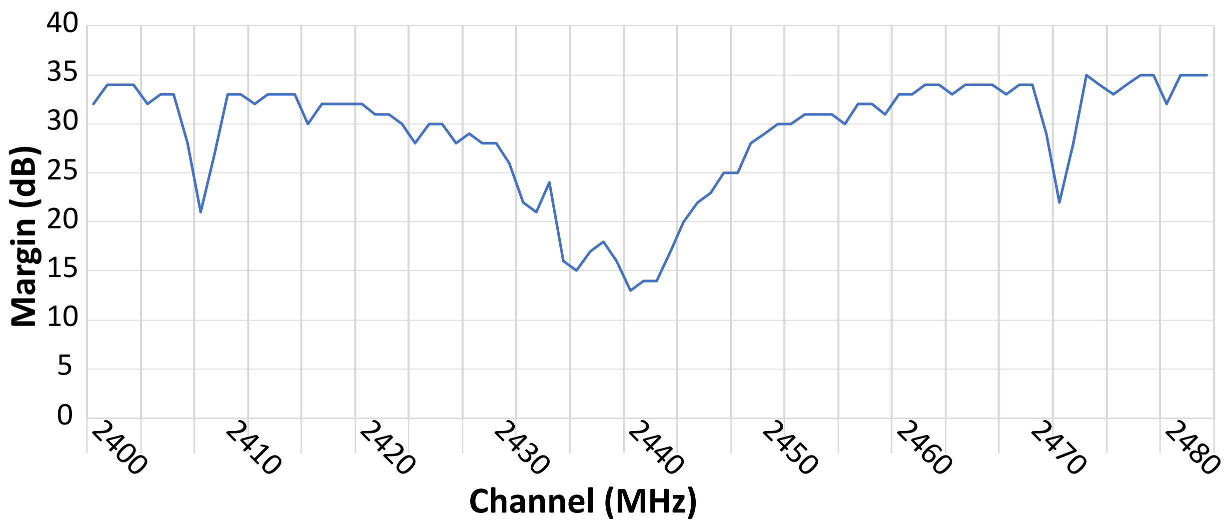
Notes:
- Bluetooth Low Energy receive sensitivity is measured across temperature at 3.6V, 2440 MHz, uncoded data at 1 Ms/s.
- PDU length = 37.
- Sensitivity is measured according to the SIG specifications.

Figure 43-31. Module Bluetooth Low Energy Receive Sensitivity vs Frequency



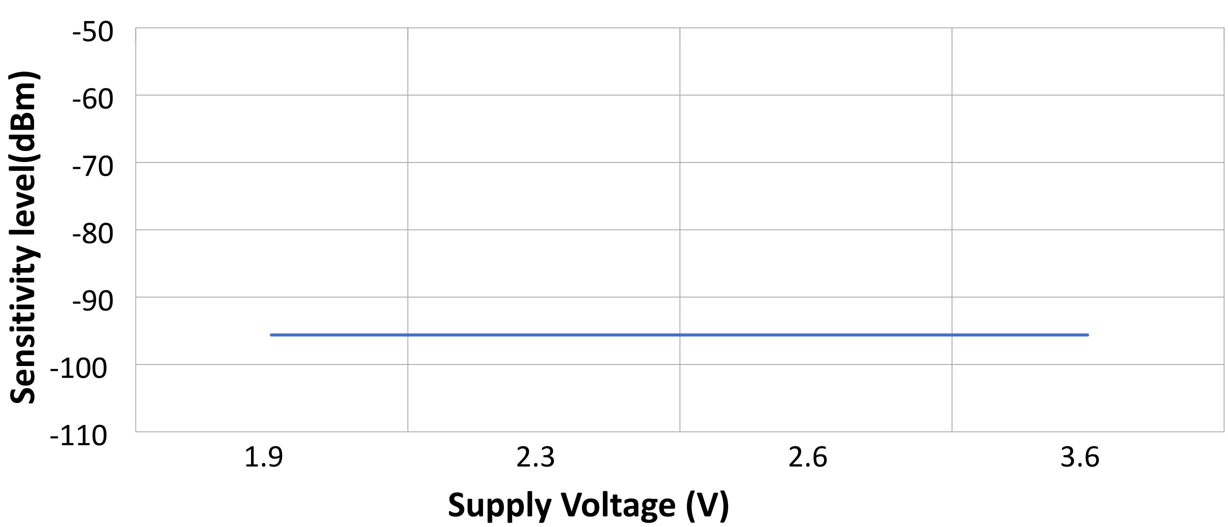
Notes:
- Bluetooth Low Energy sensitivity is measured across channels at 3.6V at 25℃, uncoded data at 1 Ms/s.
- PDU length = 37.
- Sensitivity is measured according to the SIG specifications.

Figure 43-32. Bluetooth Low Energy 1M CI Margin



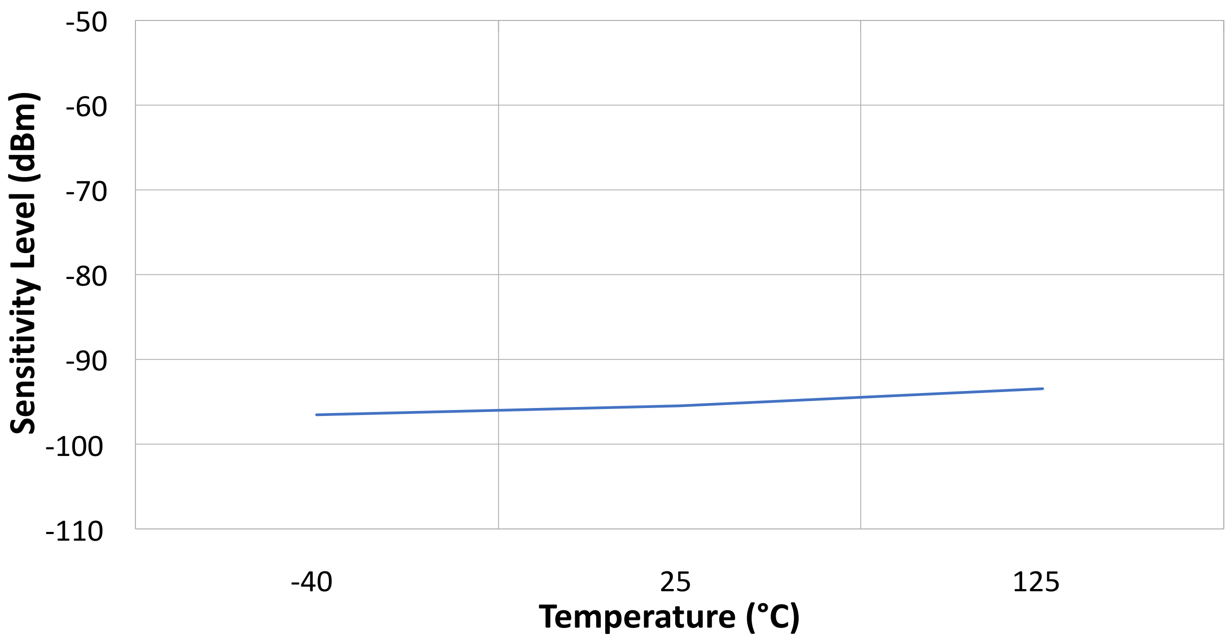
Notes:
- Bluetooth Low Energy 1M C/I Margin is measured at 2440 MHz at 25℃, 3.6V, uncoded data at 1 Ms/s.
- Reported C/I margin is the margin above the C/I specifications from SIG.

Figure 43-33. Bluetooth Low Energy Receive Sensitivity vs Voltage



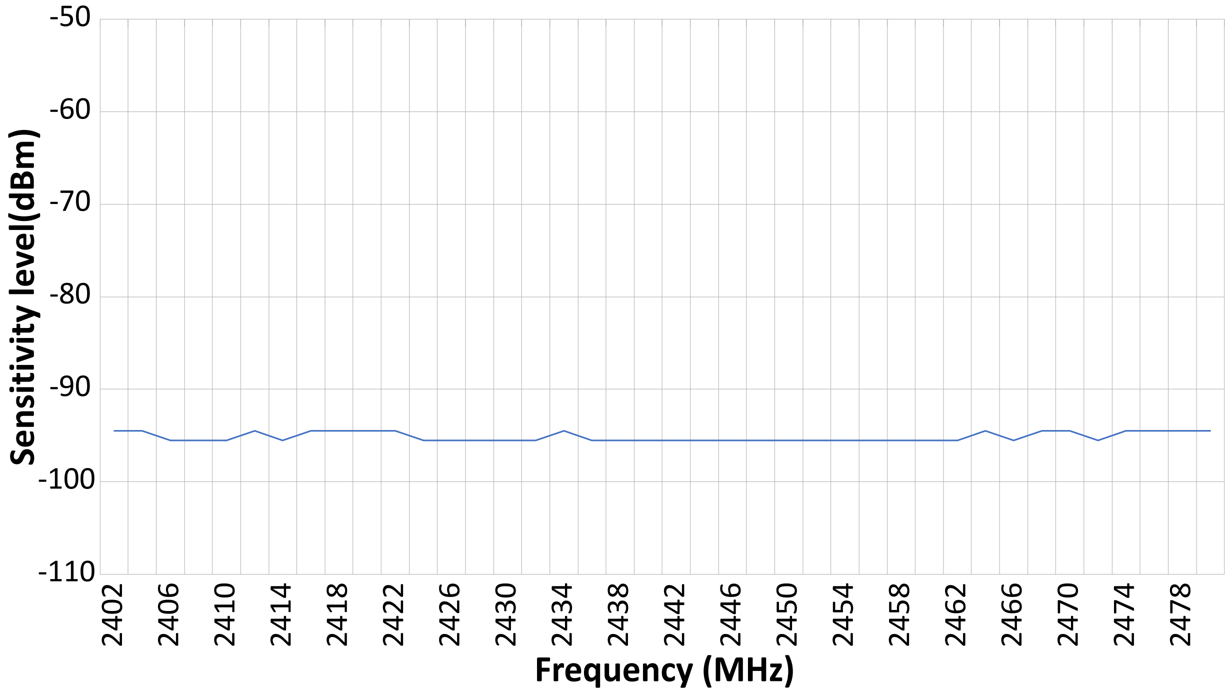
Notes:
- Bluetooth Low Energy receive sensitivity is measured at 2440 MHz at 25℃, uncoded data at 1 Ms/s.
- PDU length = 37.
- Sensitivity is measured according to the SIG specifications.

Figure 43-34. Bluetooth Low Energy Receive Sensitivity vs Temperature



Notes:
- Bluetooth Low Energy receive sensitivity is measured across channels at 3.6V, 2440 MHz, uncoded data at 1 Ms/s.
- PDU length = 37.
- Sensitivity is measured according to the SIG specifications.

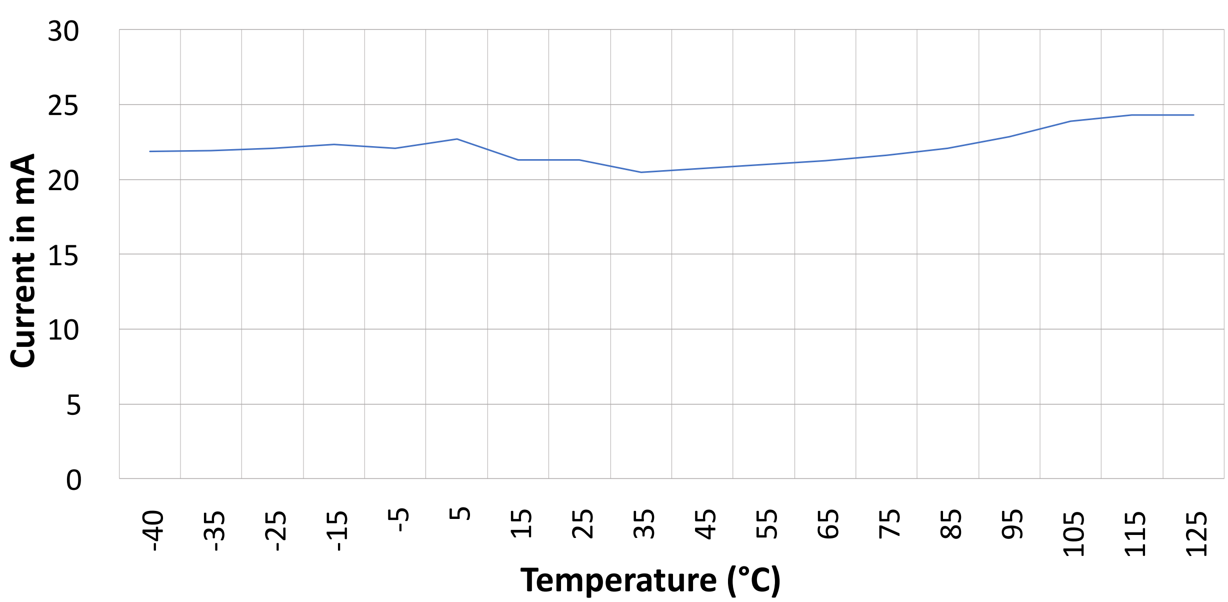
Figure 43-35. Bluetooth Low Energy Receive Sensitivity vs Frequency



Notes:

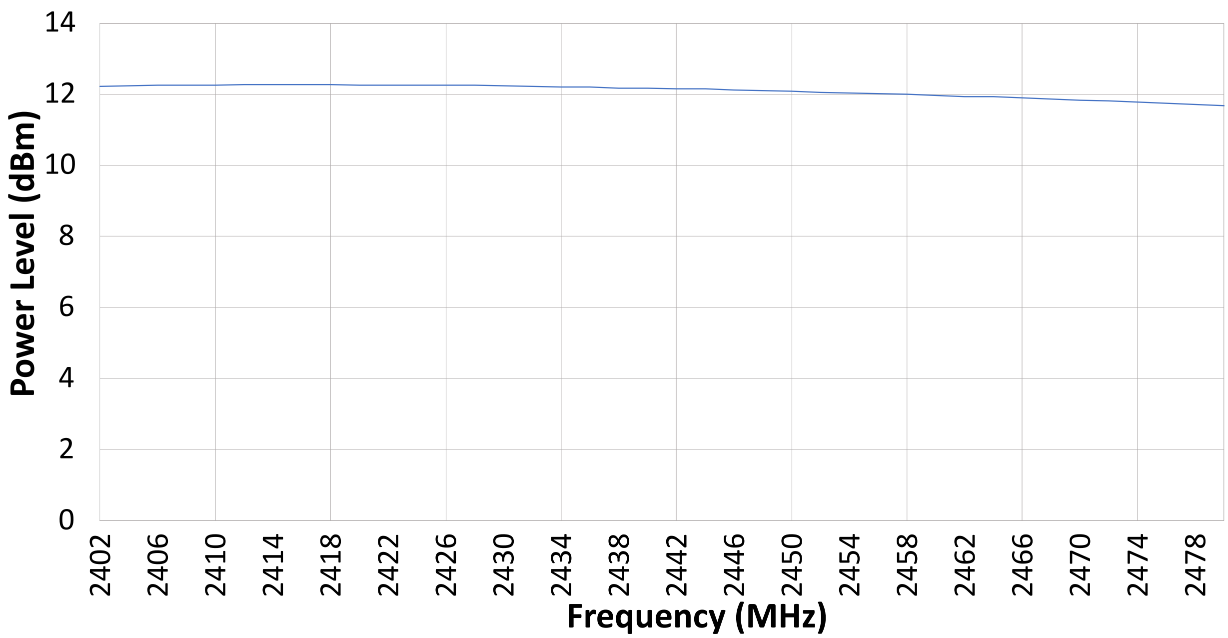
- Bluetooth Low Energy receiver sensitivity is measured across channels at 3.6V at 25℃, uncoded data at 1 Ms/s.
- PDU length = 37.
- Sensitivity is measured according to the SIG specifications.

Figure 43-36. Bluetooth Low Energy Receive Current vs Temperature



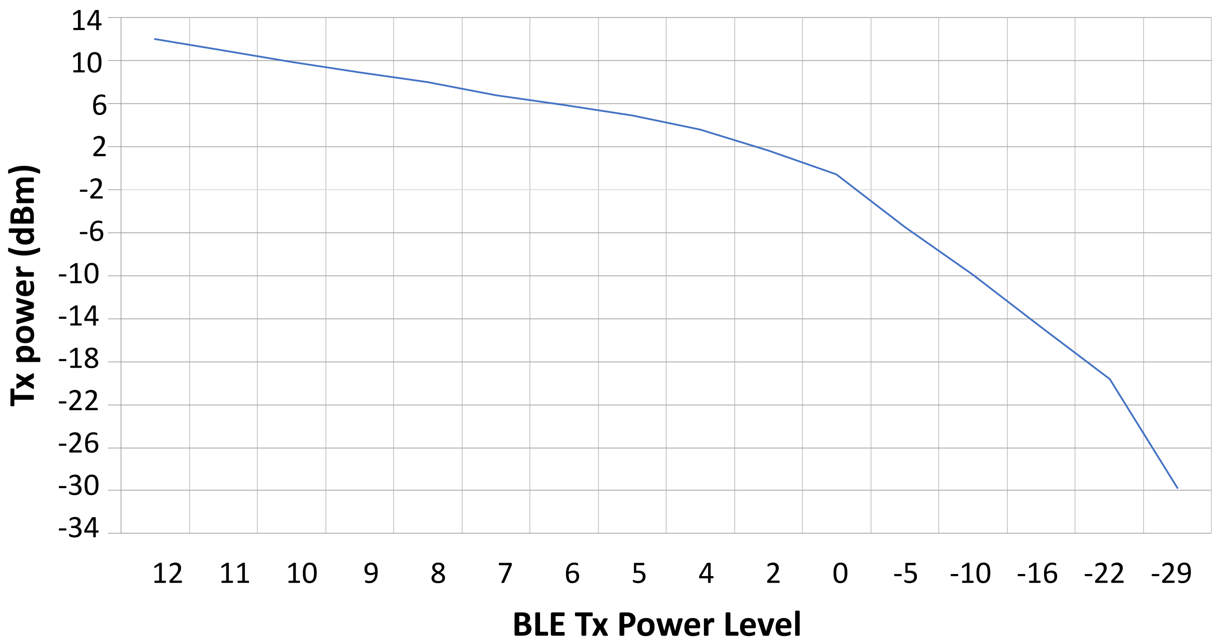
Notes:
- Bluetooth Low Energy receive current is measured at 3.3V (Buck mode), uncoded data at 1 Ms/s with LNA configured at maximum gain.
- PDU length = 37.
- Current is measured on input power rail to SoC (includes processor current as well).

Figure 43-37. Bluetooth Low Energy Transmit Power vs Frequency



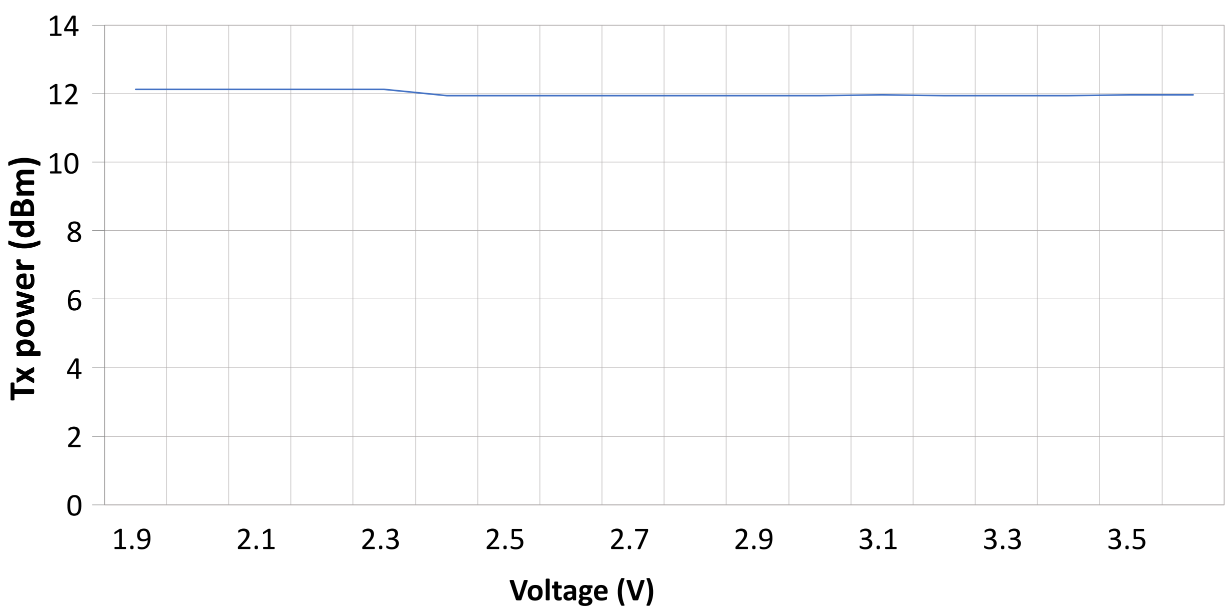
Notes:
- Bluetooth Low Energy transmit power is measured across frequency after transmit power calibration at 3.3V (Buck mode).
- Transmit power is measured after the PA matching and LPF.

Figure 43-38. Bluetooth Low Energy Transmit Power vs Transmit Power Level



Notes:
- Bluetooth Low Energy transmit power is measured at 2440 MHz after transmit power calibration.
- Transmit power is measured on board based on Microchip Technology Reference Design.
- Transmit power is measured after PA match and LPF.

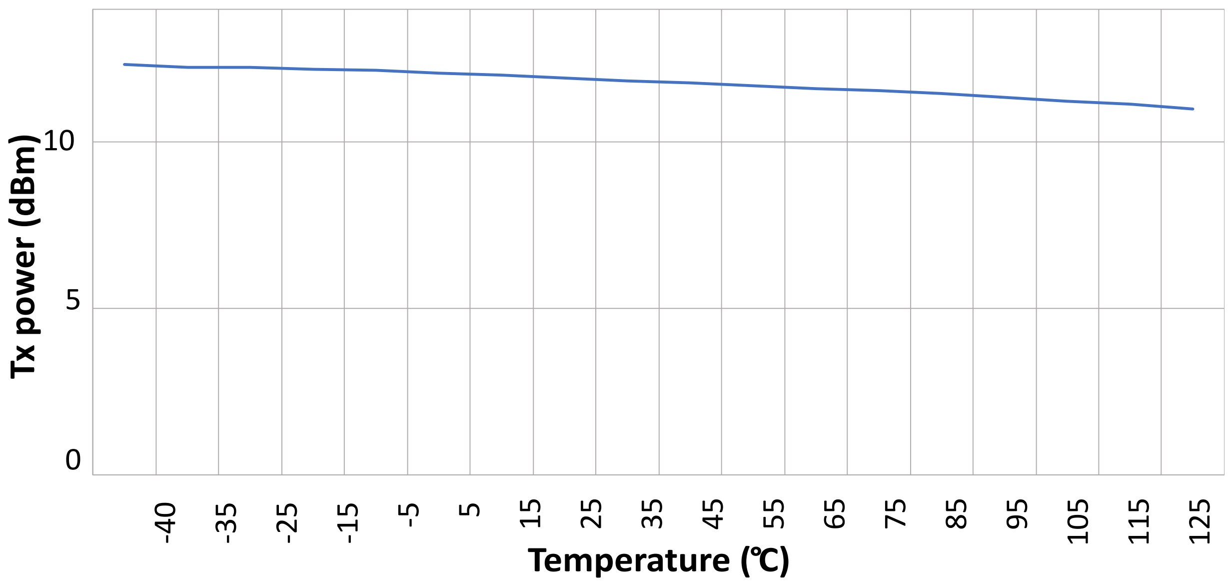
Figure 43-39. Bluetooth Low Energy Transmit Power vs VDD Supply Voltage



Notes:

- Bluetooth Low Energy transmit power is measured across voltage after transmit power calibration.
- Transmit power is measured after calibration at +12 dBm (± 0.5 dBm).
- Transmit power is measured on board based on the Microchip Reference Design.
- Transmit power is measured after the LPA and PA match section.

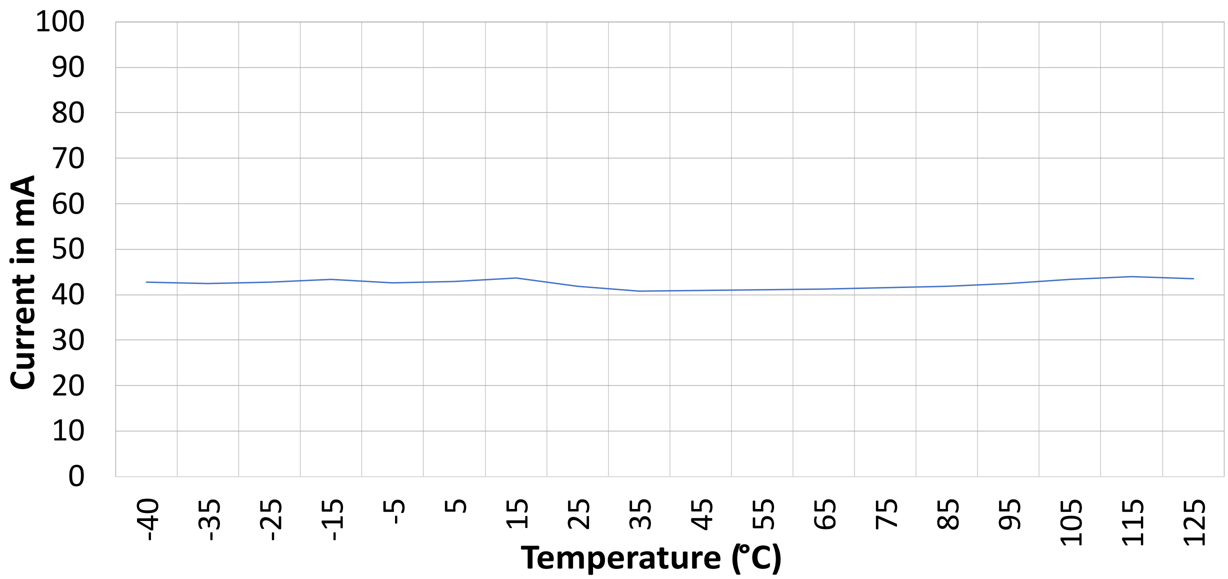
Figure 43-40. Bluetooth Low Energy Transmit Power vs. Temperature



Notes:

- Bluetooth Low Energy transmit power is measured across temperature after transmit power calibration at 3.6V and 2440 MHz.
- Temperature power compensation is triggered before power measurement.
- Transmit power is measured after the PA matching and LPF.

Figure 43-41. Bluetooth Low Energy Transmit Current vs Temperature



Notes:

- Bluetooth Low Energy transmit current is measured at 3.3V (Buck mode) at 2440 MHz across temperature.
- Transmit current is measured after calibration at +12 dBm (± 0.5 dBm).
- Current is measured on input power rail to SoC.

43.32 Zigbee® RF Characteristics

Table 43-44. WBZ45 Zigbee RF Characteristics

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.(1,2)	Max.	Units	Conditions
ZBG1	FREQ	Frequency range	2405	—	2480	MHz	—
ZBG2	FCH	Channel spacing	—	5	—	MHz	—
ZBG3	PSDU	Bit rate	—	250	—	kbps	—
ZBT1	TXOPMPA	Transmit output power MPA	—	11.67	—	dBm	—
ZBT2	TXOPLPA	Transmit output power LPA	—	3.95	—	dBm	—
ZBT3	POWERRANGE	Output power range	-14	—	12	dBm	—
ZBT4	EVM	Error vector magnitude	—	10	—	%RMS	—
ZBT5	MPA2HAR	Second harmonic from MPA	—	-47.2	—	dBm	—
ZBT6	MPA3HAR	Third harmonic from MPA	—	-45.1	—	dBm	—
ZBT7	LPA2HAR	Second harmonic from LPA	—	-57.8	—	dBm	—
ZBT8	LPA3HAR	Third harmonic from LPA	—	-52.9	—	dBm	—
ZBRX1	SENS250	Receiver sensitivity in 250 kbps	—	-100	—	dBm	—
	SENS500	Receiver sensitivity in 500 kbps	—	-96	—	dBm	—
	SENS1M	Receiver sensitivity in 1 Mbps	—	-94	—	dBm	—
	SENS2M	Receiver sensitivity in 2 Mbps	—	-88	—	dBm	—
ZBRX2	PMAX	Maximum input level	—	0	—	dBm	—

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AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.(1,2)	Max.	Units	Conditions
ZBRX3	PACRP	Adjacent channel rejection +5 MHz	—	35	—	dB	—
ZBRX4	PACRN	Adjacent channel rejection -5 MHz	—	31	—	dB	—
ZBRX5	PALRP	Alternate channel rejection +10 MHz	—	47	—	dB	—
ZBRX6	PALRN	Alternate channel rejection -10 MHz	—	47	—	dB	—
ZBRX7	LOLEAK	LO leakage	—	-28/-34	—	dB	—
ZBRX8	RSSIRANGE	Dynamic range of RSSI	—	40	—	dB	—
ZBRX9	RSSIRES	Resolution of RSSI	—	1	—	dB	—
ZBRX10	RSSIBASEVAL	Minimum value of RSSI	—	-103	—	dBm	—

Notes:
1. Measured on a board based on the Microchip Technology reference design.
2. Measured across channels at 3.3V and according to the 802.15.4 standard specifications.
3. Measured across channels and voltages.
4. LO leakage on LPA mode, measured across voltage.
5. All results are based on measurement conditions as per the 802.15.4 standards.

Table 43-45. WBZ451H Zigbee RF Characteristics

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +70°C for Commercial -40°C ≤ T_A ≤ +85°C for Industrial Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
ZBG1	FREQ	Frequency range	2405	—	2480	MHz	—
ZBG2	FCH	Channel spacing	—	5	—	MHz	—
ZBG3	PSDU	Bit rate	—	250	—	kbps	—
ZBT1	TXOPWBZ451H	Transmit output power at 3.3V	—	19.9	—	dBm	—
		Transmit output power at 2.5V	—	18.7	—	dBm	—
		Transmit output power at 1.9V	—	16.9	—	dBm	—
ZBT2	POWERRANGE	Output power range	-26	—	20	dBm	—
ZBT3	EVM	Error vector magnitude	—	10	—	%RMS	—
ZBT4	WBZ451H2HAR	Second harmonic from WBZ451H	—	-41	—	dBm	—
ZBT5	WBZ451H3HAR	Third harmonic from WBZ451H	—	-45	—	dBm	—
ZBRX1	SENS	Receiver sensitivity in 250 kbps	—	-104.1	—	dBm	—
		Receiver sensitivity in 500 kbps	—	-99.7	—	dBm	—
		Receiver sensitivity in 1 Mbps	—	-97.2	—	dBm	—
		Receiver sensitivity in 2 Mbps	—	-91.2	—	dBm	—
ZBRX2	PMAX	Maximum input level	—	-20	—	dBm	—
ZBRX3	PACRP	Adjacent channel rejection +5 MHz	—	36	—	dB	—
ZBRX4	PACRN	Adjacent channel rejection -5 MHz	—	32	—	dB	—
ZBRX5	PALRP	Alternate channel rejection +10 MHz	—	15	—	dB	—

...........continued

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +70°C for Commercial -40°C ≤ T_A ≤ +85°C for Industrial Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
ZBRX6	PALRN	Alternate channel rejection -10 MHz	—	15	—	dB	—
ZBRX7	LOLEAK	LO leakage	—	-26	—	dB	—
ZBRX8	RSSIRANGE	Dynamic range of RSSI	—	40	—	dB	—
ZBRX9	RSSIRES	Resolution of RSSI	—	1	—	dB	—
ZBRX10	RSSIBASEVAL	Minimum value of RSSI	—	-100	—	dBm	—

Notes:
1. Sensitivity related items are covering voltage range from 1.9V to 3.6V.
2. Except dedicated voltage condition case, the TX related items are operating voltage from 1.9V to 3.6V.

Table 43-46. WBZ45 Zigbee LPA RF Characteristics

AC Characteristics			Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units	Conditions
ZBLG1	FREQ	Frequency range	2405	—	2480	MHz	—
ZBLG2	FCH	Channel spacing	—	5	—	MHz	—
ZBLG3	PSDU	Bitrate	—	250	—	kbps	—
ZBLT2	TXOPLPA	Transmit output power LPA	—	5.38	—	dBm	—
ZBLT3	POWERRANGE	Output power range	-16	—	5.5	dB	—
ZBLT4	EVM	Error vector magnitude	—	10	—	%RMS	—
ZBLT7	LPA2HAR	Second harmonic from LPA	—	-53	—	dBm	Conductive measurement
ZBLT8	LPA3HAR	Third harmonic from LPA	—	-49	—	dBm	Conductive measurement
ZBLRX1	SENS	Receiver sensitivity in 250 kbps	—	-101	—	dBm	—
		Receiver sensitivity in 500 kbps	—	-97	—	dBm	—
		Receiver sensitivity in 1 Mbps	—	-95	—	dBm	—
		Receiver sensitivity in 2 Mbps	—	-89	—	dBm	—
ZBLRX2	PMAX	Maximum input level	—	0	—	dBm	—
ZBLRX7	LOLEAK	LO leakage	—	-34	—	dB	—
ZBLRX8	RSSIRANGE	Dynamic range of RSSI	—	40	—	dB	—

Notes:
1. Measured on a board based on the Microchip Technology reference design.
2. Measured across channels at 3.3V and according to the 802.15.4 standard specifications.
3. Specified value is the margin above the 802.15.4 standard limits.
4. Measured across channels and voltages.
5. LO leakage on LPA mode, measured across voltage.
6. All results are based on measurement conditions as per the 802.15.4 standards.

Table 43-47. WBZ45 Zigbee RF Current Characteristics

AC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	CPU Frequency	Min.	Typ.	Max.	Units	Conditions
IZBTX1	IDDTXMPA	Current consumption at +12 dBm output power in DC-DC mode 250 kbps	64 MHz	—	43.3	—	mA	—
IZBTX4		Current consumption at +12 dBm output power in MLDO mode	64 MHz	—	96.4	—	mA	—
IZBTX7	IDDTXLPA	Current consumption at +4 dBm output power in DC-DC mode 250 kbps	64 MHz	—	27.3	—	mA	—
IZBTX10		Current consumption at +12 dBm output power in MLDO mode	64 MHz	—	51.7	—	mA	—
IZBRX1	IDDRXZB	Current consumption at RX signal level -95 dBm in DC-DC mode	64 MHz	—	19.4	—	mA	—
IZBRX4		Current consumption at RX signal level -95 dBm in MLDO mode	64 MHz	—	38.5	—	mA	—
IZBRX1	IDDRXZBRPC	Current consumption at RX signal level -95 dBm in DC-DC mode	64 MHz	—	13.6	—	mA	—
IZBRX4		Current consumption at RX signal level -95 dBm in MLDO mode	64 MHz	—	29	—	mA	—

Notes:
- Current consumption is measured on a board based upon the Microchip Technology Reference Design.
- Current consumption is for the entire SoC (including the MCU).
- Current reported is the average of the current during the transmit burst (exclude off cycle of the transmission).

Table 43-48. WBZ451H Zigbee RF Current Characteristics

AC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp				
Param. No.	Symbol	Characteristics	CPU Frequency	Min.	Typ.	Max.	Units	Conditions
IZBTX1	IDDTXWBZ451H	Current consumption at +20 dBm output power in DC-DC mode 250 kbps	64 MHz	—	146.7	—	mA	—
IZBTX2			48 MHz	—	144.3	—	mA	—
IZBTX3	IDDTXWBZ451H	Current consumption at +15 dBm output power in DC-DC mode 250 kbps	64 MHz	—	93.1	—	mA	—
IZBTX4			48 MHz	—	91.1	—	mA	—
IZBTX5		Current consumption at +15 dBm output power in MLDO mode	64 MHz	—	98.7	—	mA	—
IZBTX6			48 MHz	—	96.8	—	mA	—
IZBTX7	IDDTXWBZ451H	Current consumption at +10 dBm output power in DC-DC mode 250 kbps	64 MHz	—	69.7	—	mA	—
IZBTX8			48 MHz	—	67.8	—	mA	—
IZBTX9		Current consumption at +10 dBm output power in MLDO mode	64 MHz	—	80.1	—	mA	—
IZBTX10			48 MHz	—	77.8	—	mA	—

...........continued

AC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp				
Param. No.	Symbol	Characteristics	CPU Frequency	Min.	Typ.	Max.	Units	Conditions
IZBTX11	IDDTXWBZ451H	Current consumption at 0 dBm output power in DC-DC mode 250 kbps	64 MHz	—	45.5	—	mA	—
IZBTX12			48 MHz	—	44.3	—	mA	—
IZBTX13		Current consumption at 0 dBm output power in MLDO mode	64 MHz	—	59.8	—	mA	—
IZBTX14			48 MHz	—	57.8	—	mA	—
IZBTX15	IDDTXBYP	Current consumption at -4 dBm output power in DC-DC mode 250 kbps	64 MHz	—	24.7	—	mA	—
IZBTX16			48 MHz	—	23.6	—	mA	—
IZBTX17		Current consumption at -4 dBm output power in MLDO mode	64 MHz	—	47.3	—	mA	—
IZBTX18			48 MHz	—	45.1	—	mA	—
IZBRX1	IDDRXZB	Current consumption at RX signal level -95 dBm in DC-DC mode	64 MHz	—	25.2	—	mA	—
IZBRX2			48 MHz	—	24.2	—	mA	—
IZBRX3		Current consumption at RX signal level -95 dBm in MLDO mode	64 MHz	—	42.6	—	mA	—
IZBRX4			48 MHz	—	40.5	—	mA	—
IZBRX5	IDDRXZBRPC	Current consumption at RX signal level -95dBm in DC-DC mode	64 MHz	—	25.2	—	mA	—
IZBRX6			48 MHz	—	24.2	—	mA	—
IZBRX7		Current consumption at RX signal level -95 dBm in MLDO mode	64 MHz	—	42.7	—	mA	—
IZBRX8			48 MHz	—	40.3	—	mA	—

Note:

1. DC-DC mode operation in 3.3V; MLDO mode operation in 1.9V.

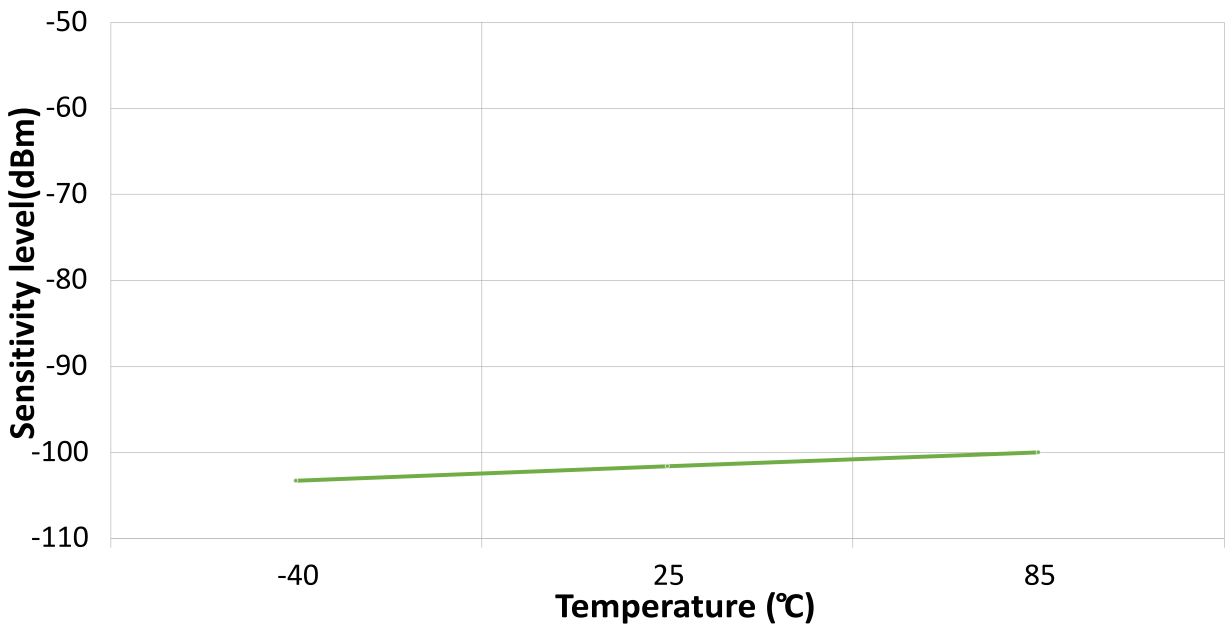
Table 43-49. WBZ45 Zigbee RF Current LPA Characteristics

AC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	CPU Frequency	Min.	Typ.	Max.	Units	Conditions
IZBTX1	IDDTXMPA	Current consumption at +5.5 dBm output power in DC-DC mode 250 kbps	64 MHz	—	24.5	—	mA	V_{DD} = 3.3V
IZBTX4		Current consumption at +5.5 dBm output power in MLDO mode	64 MHz	—	47.4	—	mA	V_{DD} = 3.3V
IZBTX7	IDDTXLPA	Current consumption at 0 dBm output power in DC-DC mode 250 kbps	64 MHz	—	22.3	—	mA	V_{DD} = 3.3V
IZBTX10		Current consumption at 0 dBm output power in MLDO mode	64 MHz	—	39.9	—	mA	V_{DD} = 3.3V
IZBRX1	IDDRXZB	Current consumption at RX signal level -95 dBm in DC-DC mode	64 MHz	—	21.3	—	mA	V_{DD} = 3.3V
IZBRX4		Current consumption at RX signal level -95 dBm in MLDO mode	64 MHz	—	39.5	—	mA	V_{DD} = 3.3V

...........continued

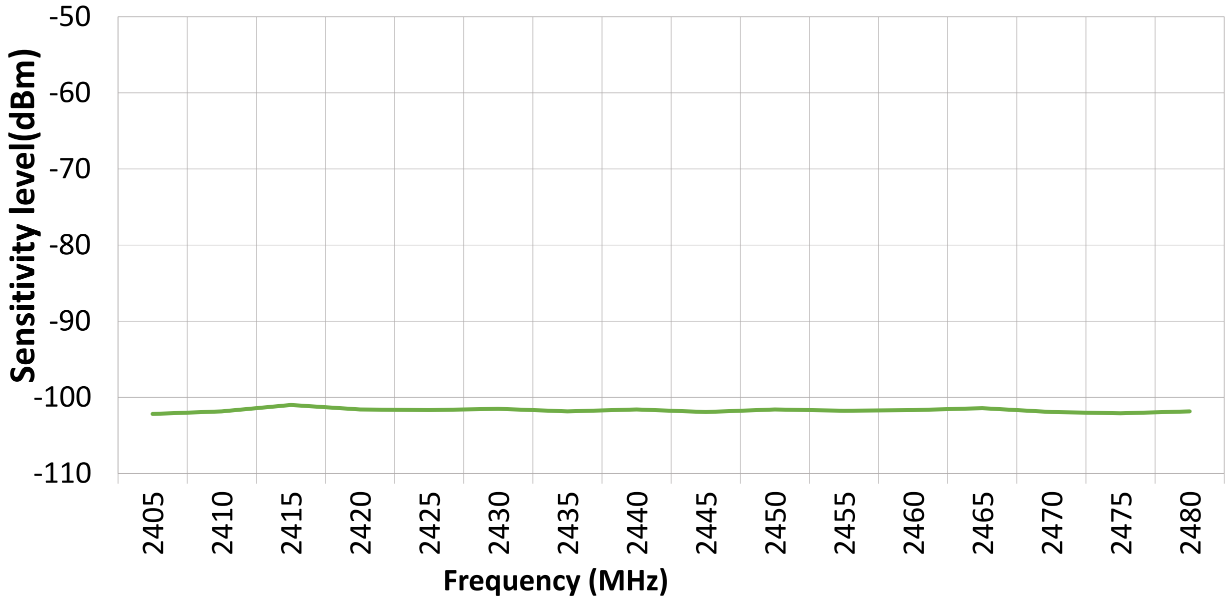
AC Characteristics				Standard Operating Conditions: V_{DDIO} = V_{DDANA} 1.9V to 3.6V (unless otherwise stated) Operating Temperature: -40°C ≤ T_A ≤ +85°C for Industrial Temp -40°C ≤ T_A ≤ +125°C for Extended Temp				
Param. No.	Symbol	Characteristics	CPU Frequency	Min.	Typ.	Max.	Units	Conditions
IZBRX1	IDDRXZBRPC	Current consumption at RX signal level -95 dBm in DC-DC mode	64 MHz	—	14.8	—	mA	V_{DD} = 3.3V
IZBRX4		Current consumption at RX signal level -95 dBm in MLDO mode	64 MHz	—	29.7	—	mA	V_{DD} = 3.3V

Figure 43-42. Module Zigbee Receive Sensitivity vs. Temperature



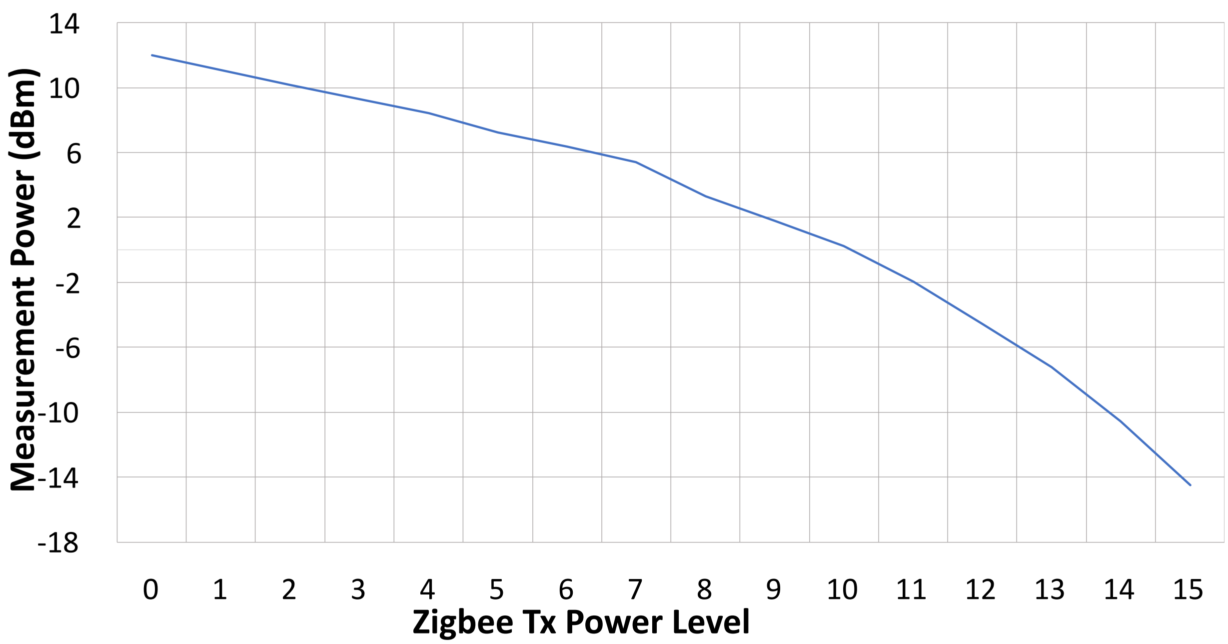
Notes:
- Receiver sensitivity is measured based on the 802.15.4 specifications.
- Receiver sensitivity is measured at 2440 MHz at 3.6V, 250 kbps.
- Measured after receiver calibration.

Figure 43-43. Module Zigbee Receive Sensitivity vs. Frequency



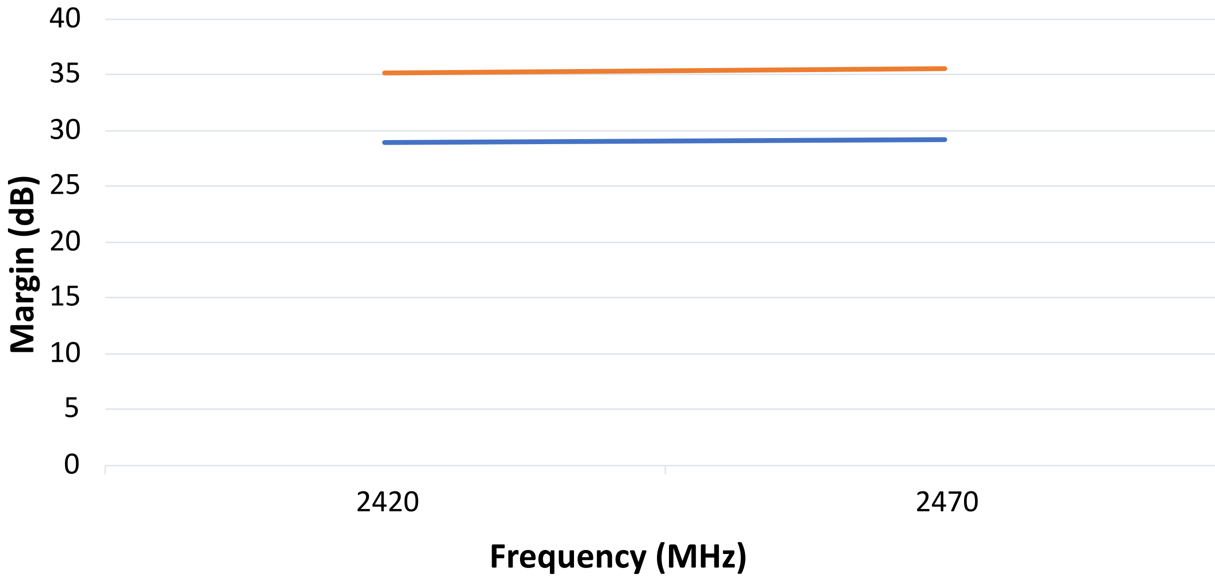
Notes:
- RX sensitivity across channels is measured at 3.6V at 25℃, 250 kbps.
- Sensitivity is measured according to the 802.15.4 specifications.

Figure 43-44. Zigbee TX Setting vs. Measurement Power



Notes:
- Transmit power is measured after calibration.
- Transmit power is measured across power levels at 2440 MHz at 3.6V, 25℃.
- Transmit power is measured after the PA matching and LPF.

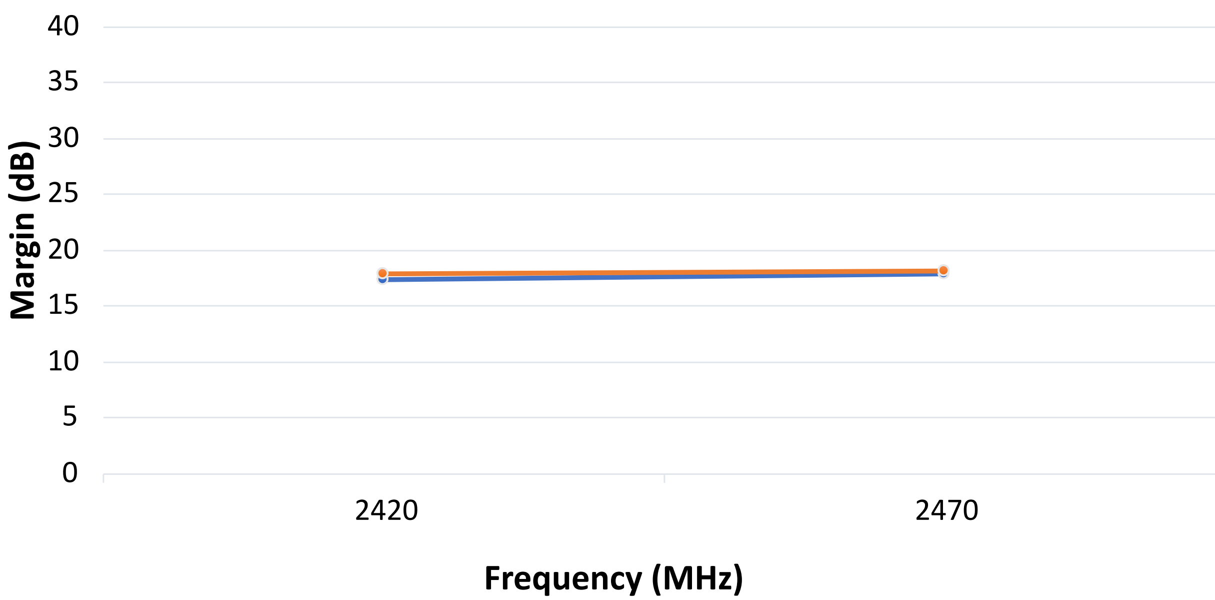
Figure 43-45. Zigbee ACR +-5M Margin



Notes:

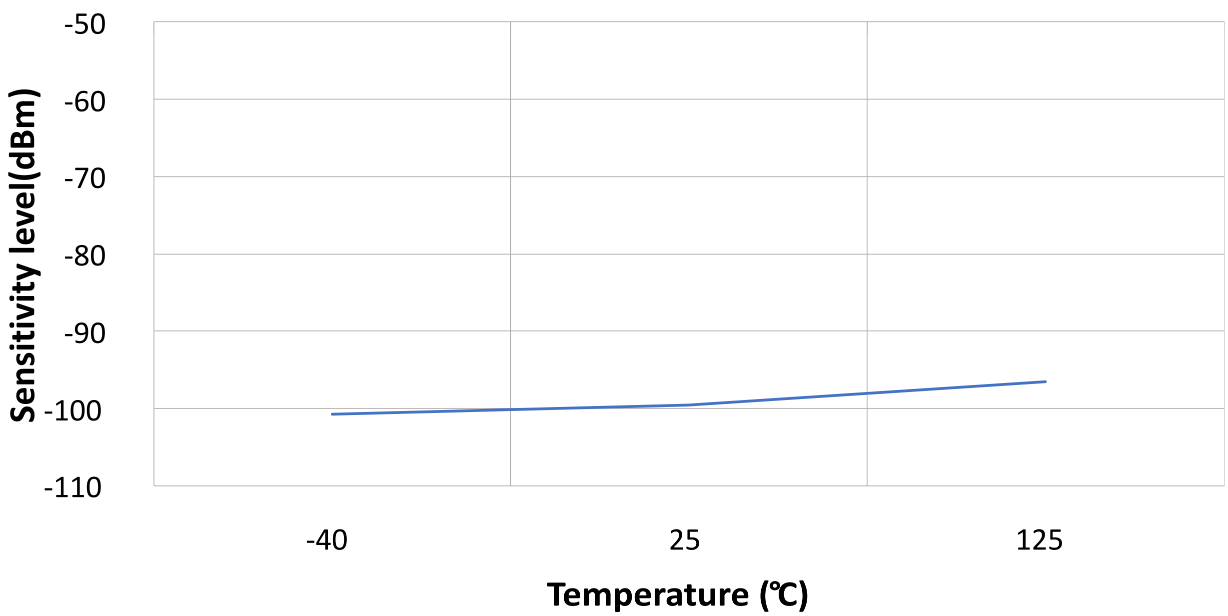
- Adjacent channel rejection is measured at 3.6V at 25℃, 250 kbps.
- Measured based on the 802.15.4 adjacent channel relative jamming specification.
- Margin specified is the margin above the 802.15.4 specifications.
- Measured after receiver calibration.

Figure 43-46. Zigbee ACR +-10M Margin



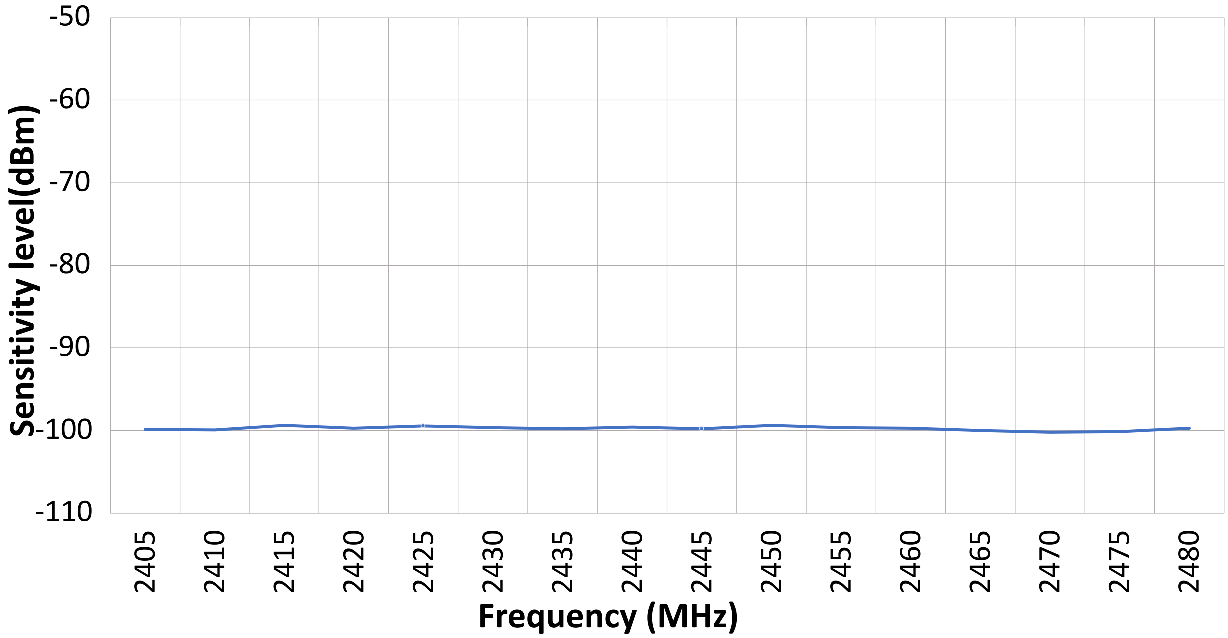
Notes:
- Adjacent channel rejection is measured at 3.6V at 25℃, 250 kbps.
- Measured based on the 802.15.4 adjacent channel relative jamming specification.
- Margin specified is the margin above the 802.15.4 specifications.
- Measured after receiver calibration.

Figure 43-47. Zigbee Receive Sensitivity vs. Temperature



Notes:
- Receiver sensitivity is measured based on the 802.15.4 specifications.
- Sensitivity measured at 3.6V, 25℃ on 2440 MHz across temperature, 250 kbps.
- Measured after receiver calibration.

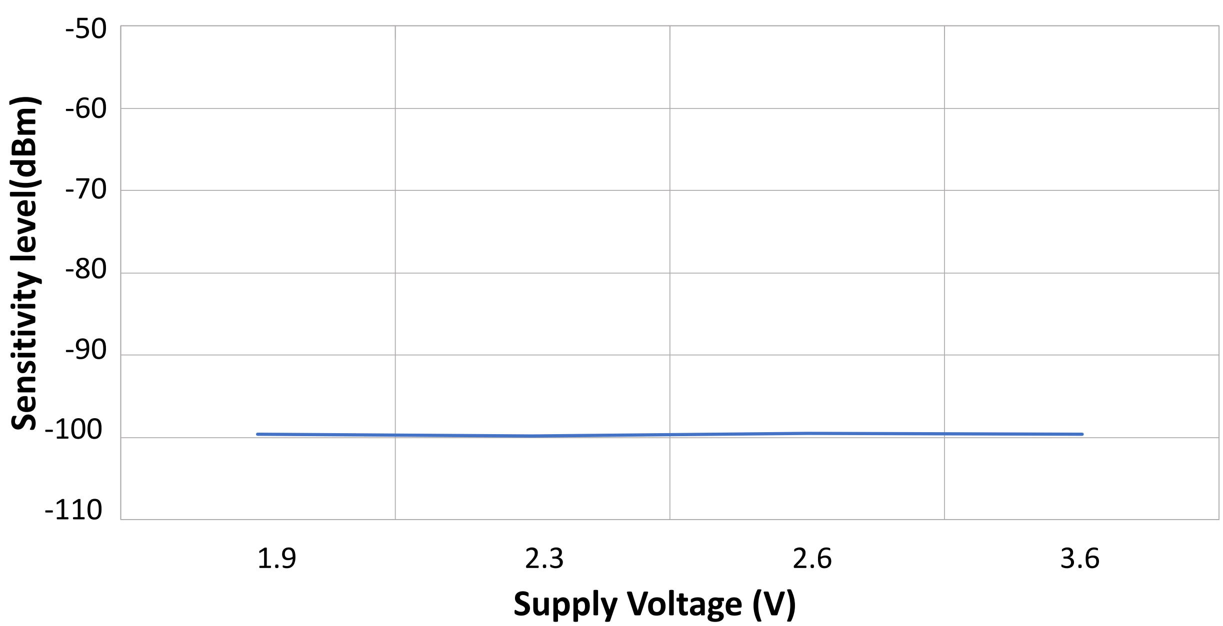
Figure 43-48. Zigbee Receive Sensitivity vs. Frequency



Notes:

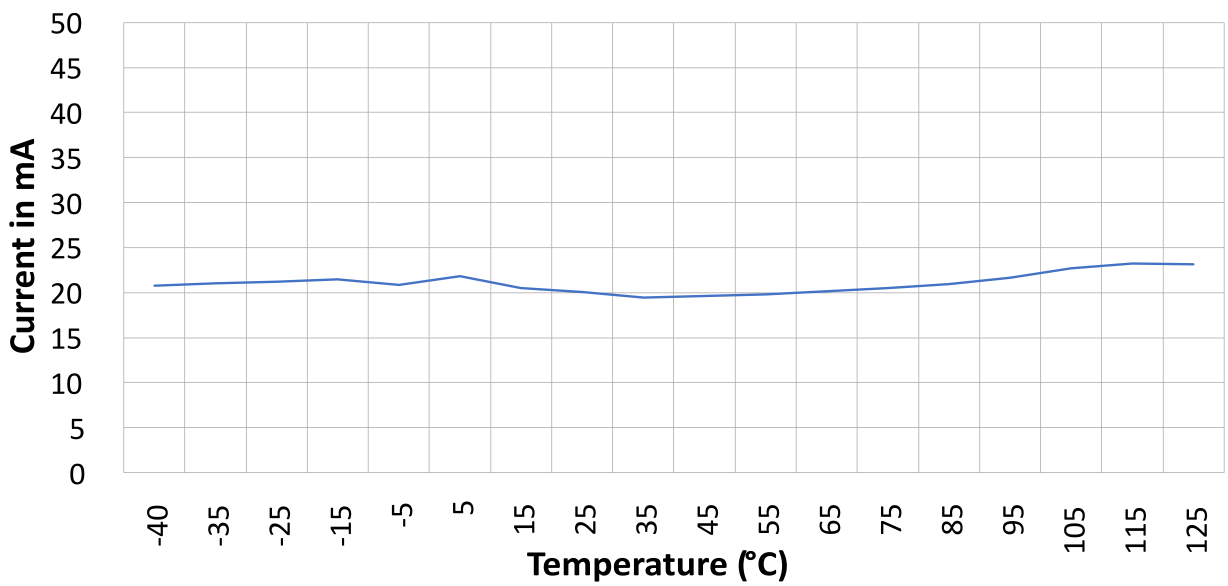
- RX sensitivity is measured across channels at 3.6V at 25℃, 250 kbps.
- Sensitivity is measured according to the 802.15.4 specifications.
- Sensitivity is measured after RX calibration.

Figure 43-49. Zigbee Receive Sensitivity vs. VDD Supply Voltage



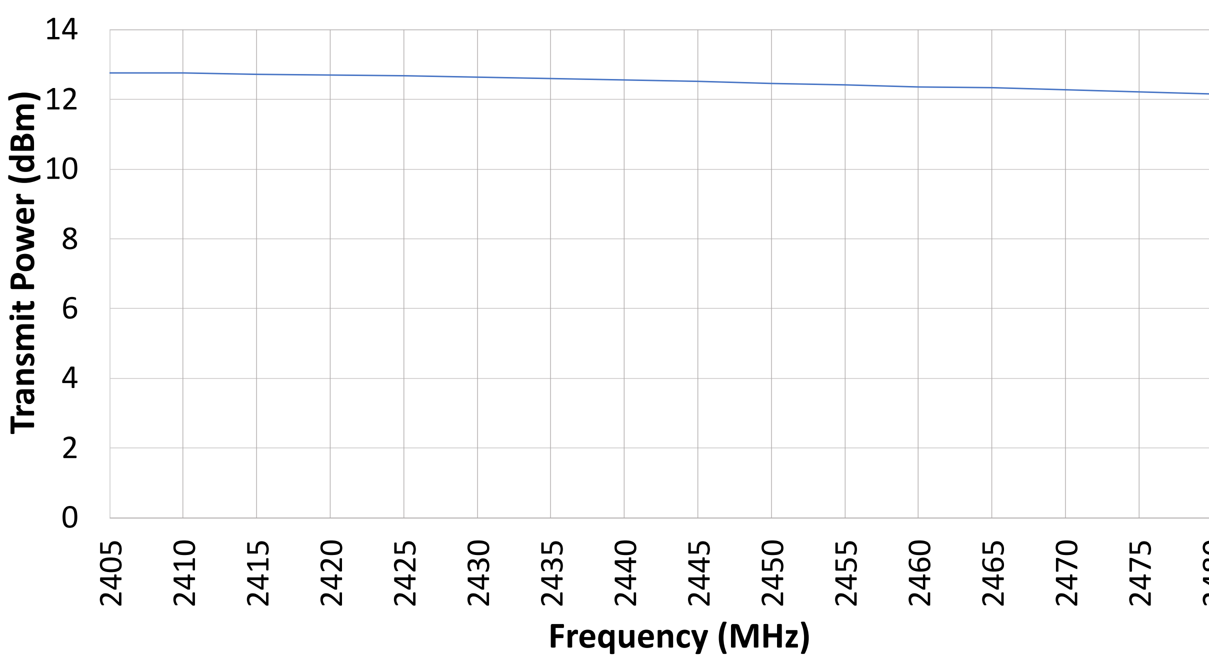
Notes:
- RX sensitivity is measured at 2440 MHz at 25℃ across voltage, 250 kbps.
- Sensitivity is measured according to the 802.15.4 specifications.
- Sensitivity is measured after RX calibration.

Figure 43-50. Zigbee Receive Current vs. Temperature



Notes:
- Receiver operating at 2440 MHz, 3.3V, 25℃ at maximum LNA gain.
- Measured after receiver calibration.

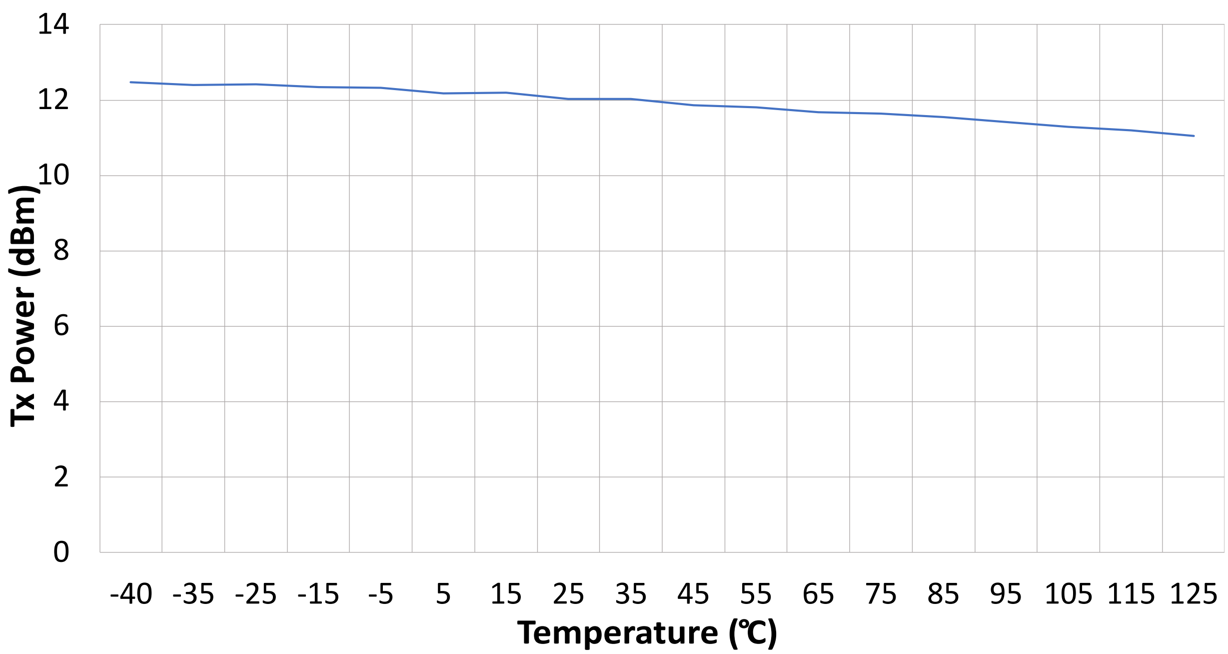
Figure 43-51. Zigbee Transmit Power vs Frequency



Notes:

- Transmit power is measured after calibration.
- Transmit power is measured across the channels at 3.6V at 25℃.
- Transmit power is measured after the PA matching and LPF.

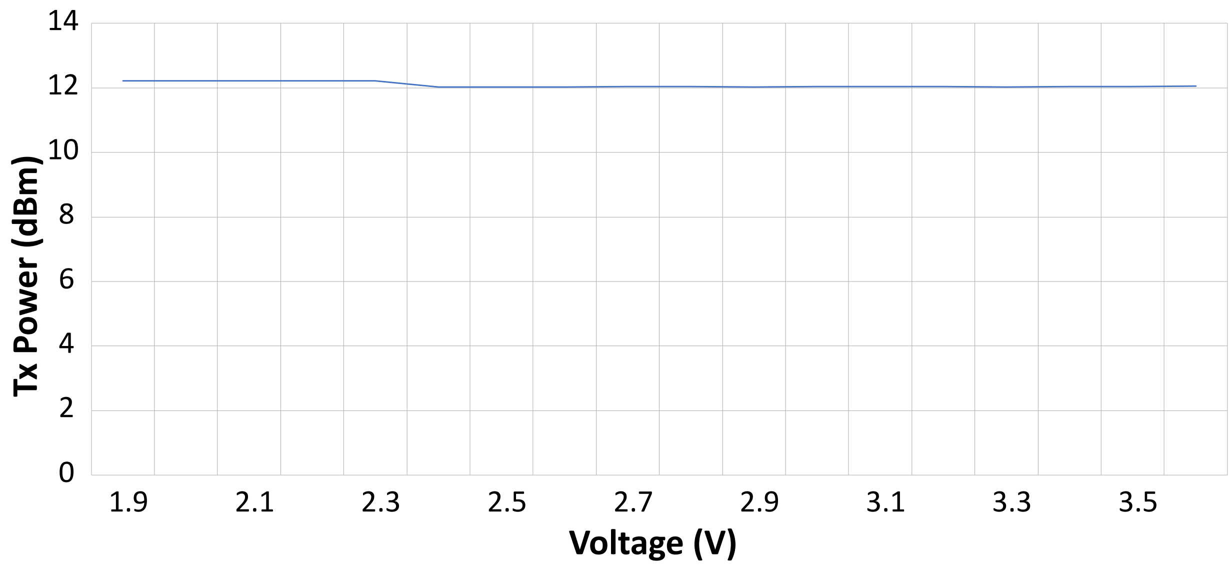
Figure 43-52. Zigbee Transmit Power vs Temperature



Notes:

- Transmit power is measured after calibration.
- Transmit power is measured at 2440 MHz at 3.6V across temperature.
- Transmit power is measured after the PA matching and LPF.
- Transmit power compensation is triggered before measurement across temperature.

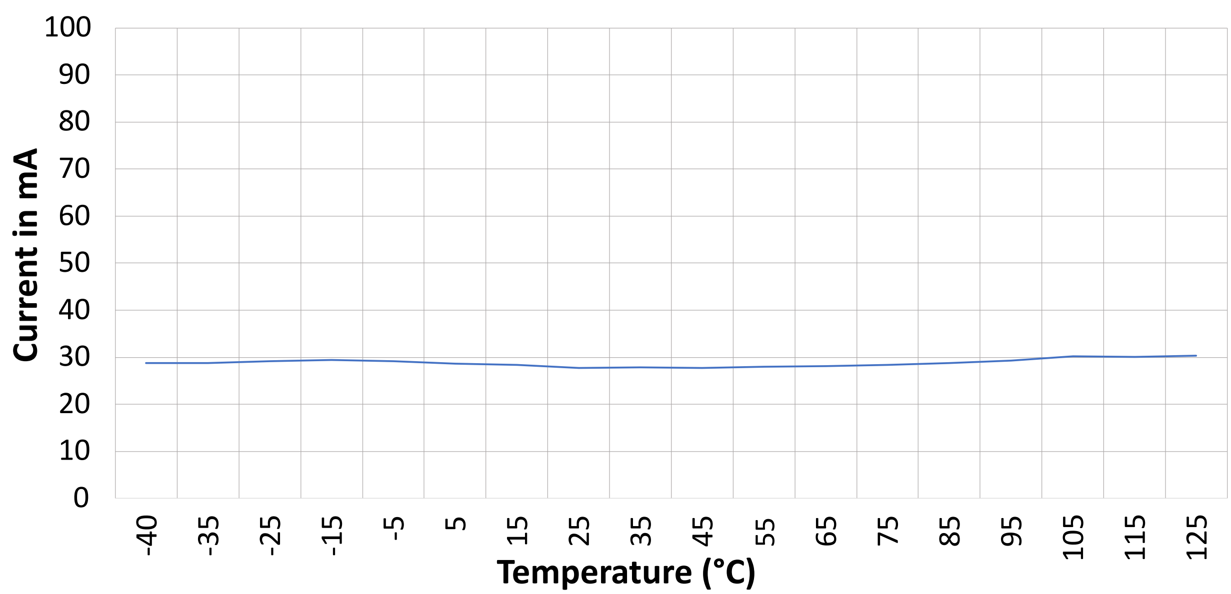
Figure 43-53. Zigbee Transmit Power vs. VDD Supply Voltage



Notes:

- Transmit power is measured after calibration.
- Transmit power is measured across voltage at 2440 MHz and 25℃.
- Transmit power is measured on reference board after the PA matching and LPF.

Figure 43-54. Zigbee Transmit Current vs. Temperature



Notes:

- Transmit current is measured at input to SoC (includes SoC power consumption).
- Transmit current is measured at 2440 MHz at 3.3V (Buck mode).
- Transmit power is calibrated to +12 dBm (± 0.5 dBm on MPA mode).

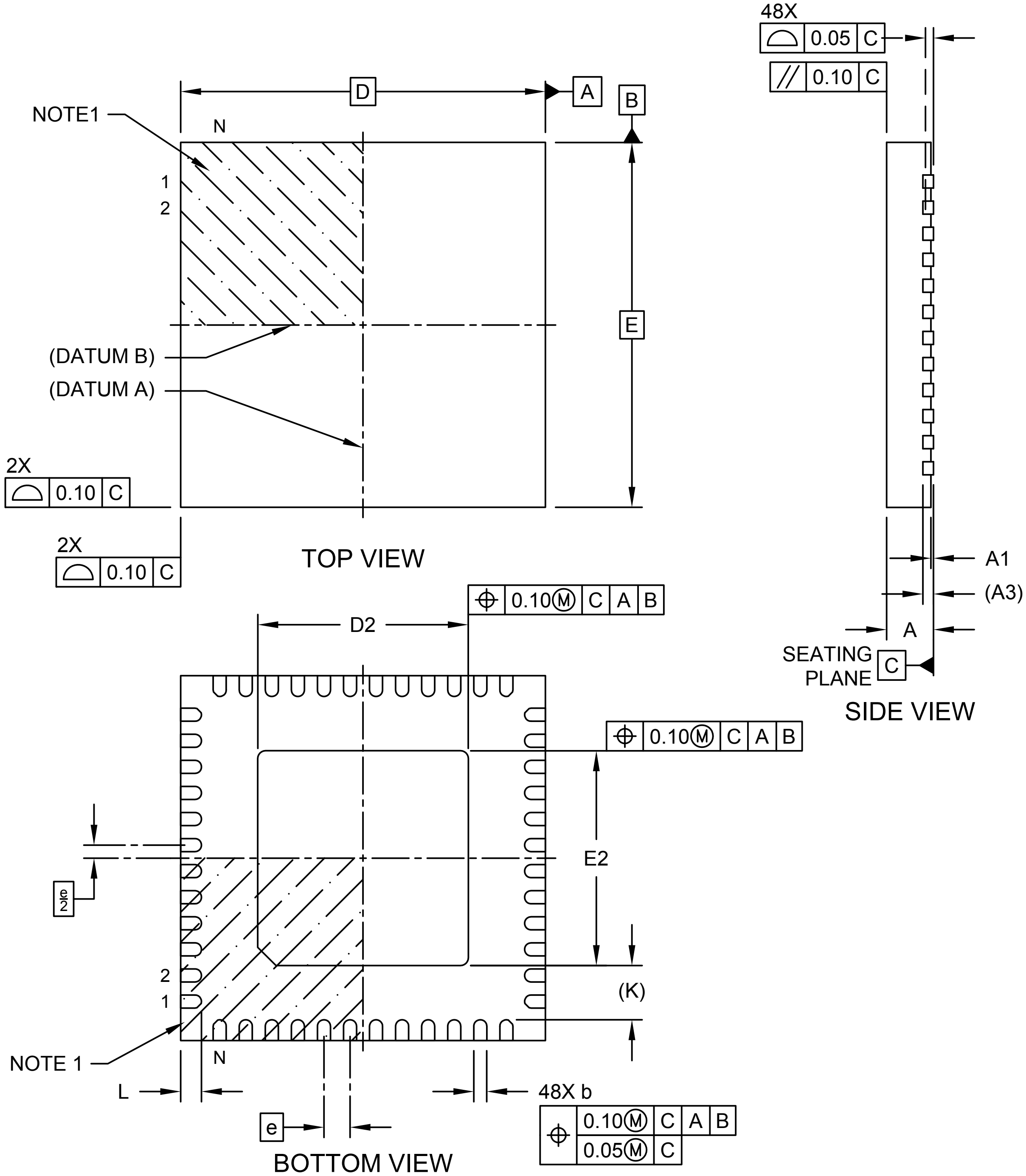
44. Packaging Information

This chapter provides the information on package markings, dimension and footprint of the PIC32CX-BZ2 and WBZ45 family.

44.1 PIC32CX1012BZ25048 SoC Packaging Information

48-Lead Very Thin Quad Flat, No Lead Package (MYX) 7x7x0.9 mm Body [VQFN] With 4.04x4.12 mm Exposed Pad

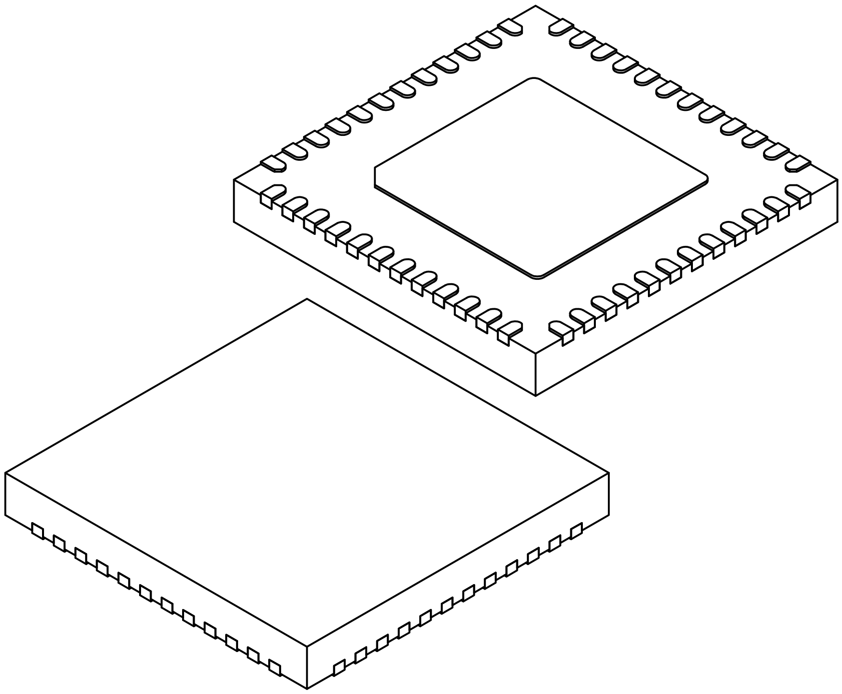
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-507 Rev A Sheet 1 of 2

48-Lead Very Thin Quad Flat, No Lead Package (MYX) 7x7x0.9 mm Body [VQFN] With 4.04x4.12 mm Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		7.00 BSC	
Exposed Pad Length	D2	3.94	4.04	4.14
Overall Width	E		7.00 BSC	
Exposed Pad Width	E2	4.02	4.12	4.22
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		1.04 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

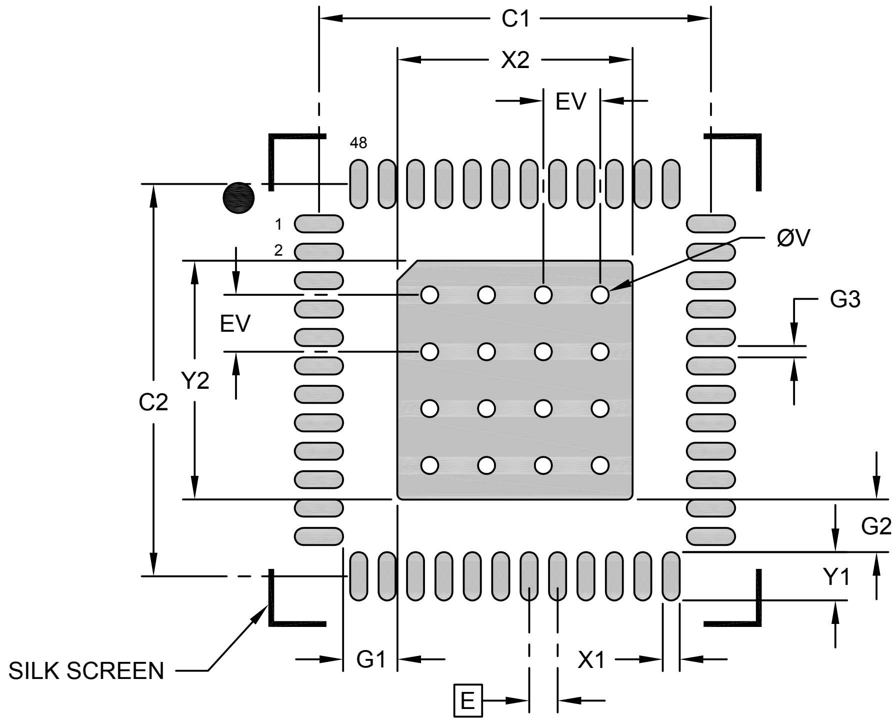
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-507 Rev A Sheet 2 of 2

48-Lead Very Thin Quad Flat, No Lead Package (MYX) 7x7x0.9 mm Body [VQFN] With 4.04x4.12 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			4.14
Optional Center Pad Length	Y2			4.20
Contact Pad Spacing	C1		6.90	
Contact Pad Spacing	C2		6.90	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			0.85
Contact Pad to Center Pad (X24)	G1	0.96		
Contact Pad to Center Pad (X24)	G2	0.93		
Contact Pad to Contact Pad (X44)	G3	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

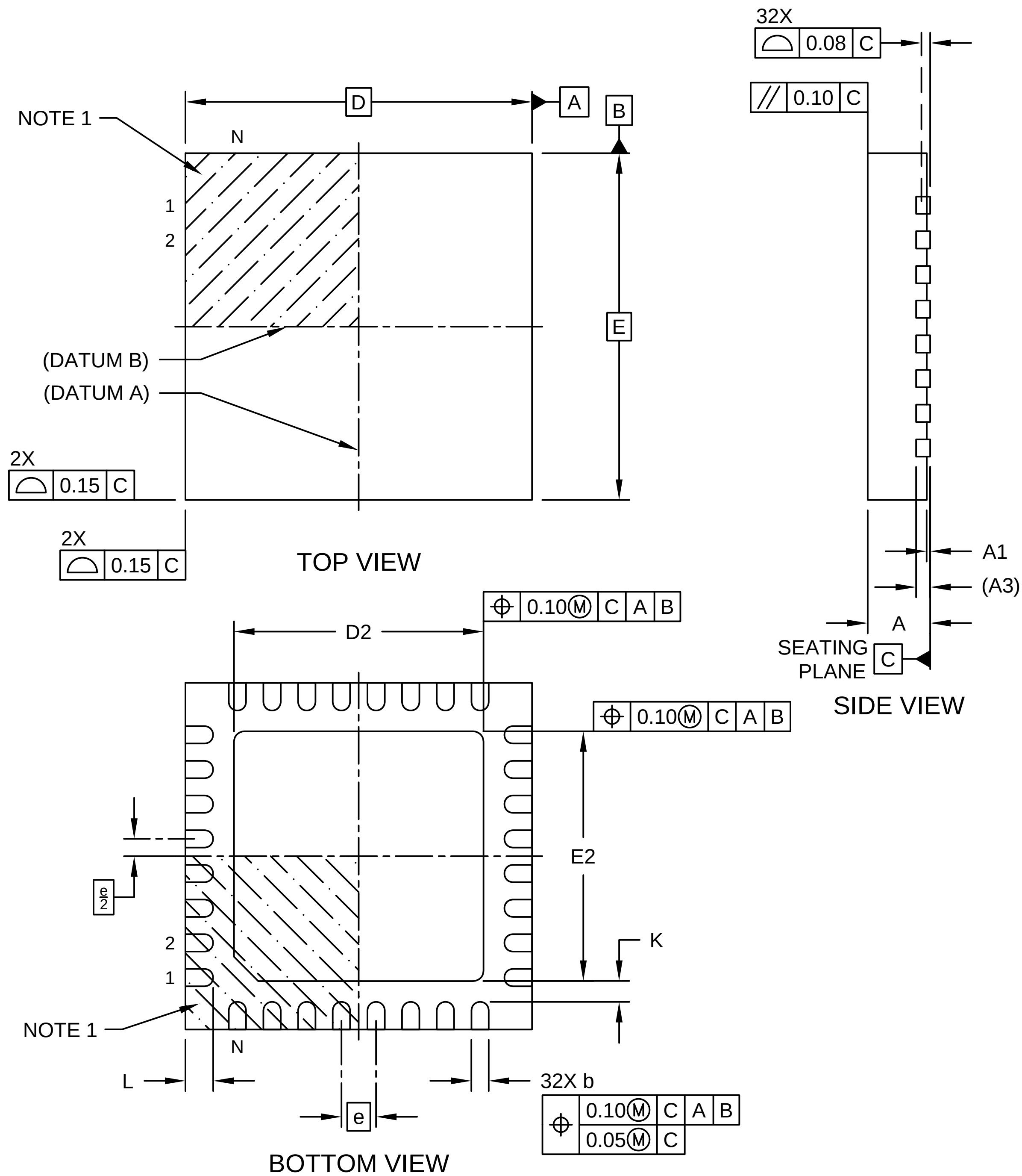
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2507 Rev A

44.2 PIC32CX1012BZ24032 SoC Packaging Information

32-Lead Very Thin Plastic Quad Flat, No Lead Package (S8B) - 5x5 mm Body [VQFN] With 3.60 mm Exposed Pad; Atmel Legacy Global Package Code ZKV

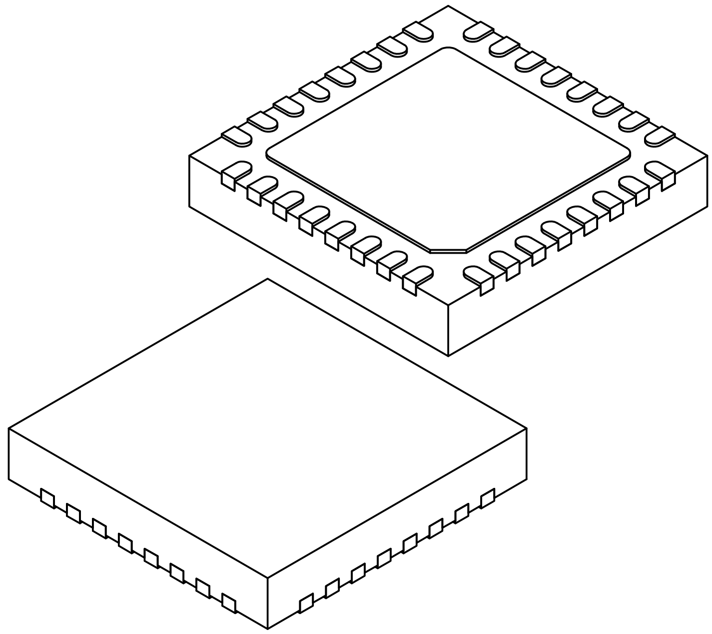
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21402 Rev A Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (S8B) - 5x5 mm Body [VQFN] With 3.60 mm Exposed Pad; Atmel Legacy Global Package Code ZKV

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.50	3.60	3.70
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.50	3.60	3.70
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

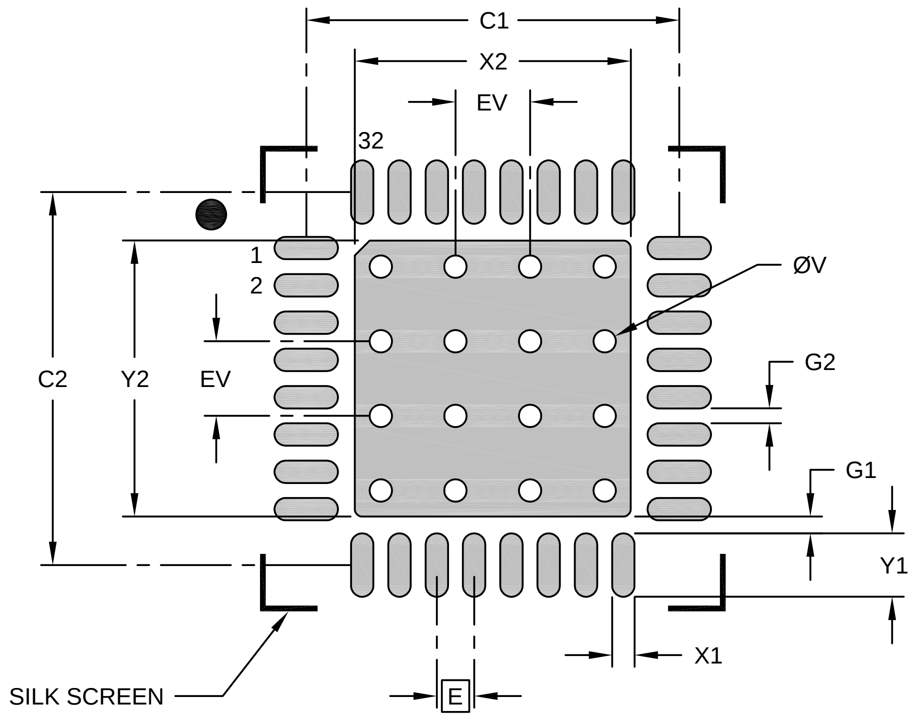
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21402 Rev A Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (S8B) - 5x5 mm Body [VQFN] With 3.60 mm Exposed Pad; Atmel Legacy Global Package Code ZKV

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.70
Optional Center Pad Length	Y2			3.70
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.85
Contact Pad to Center Pad (X32)	G1	0.23		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

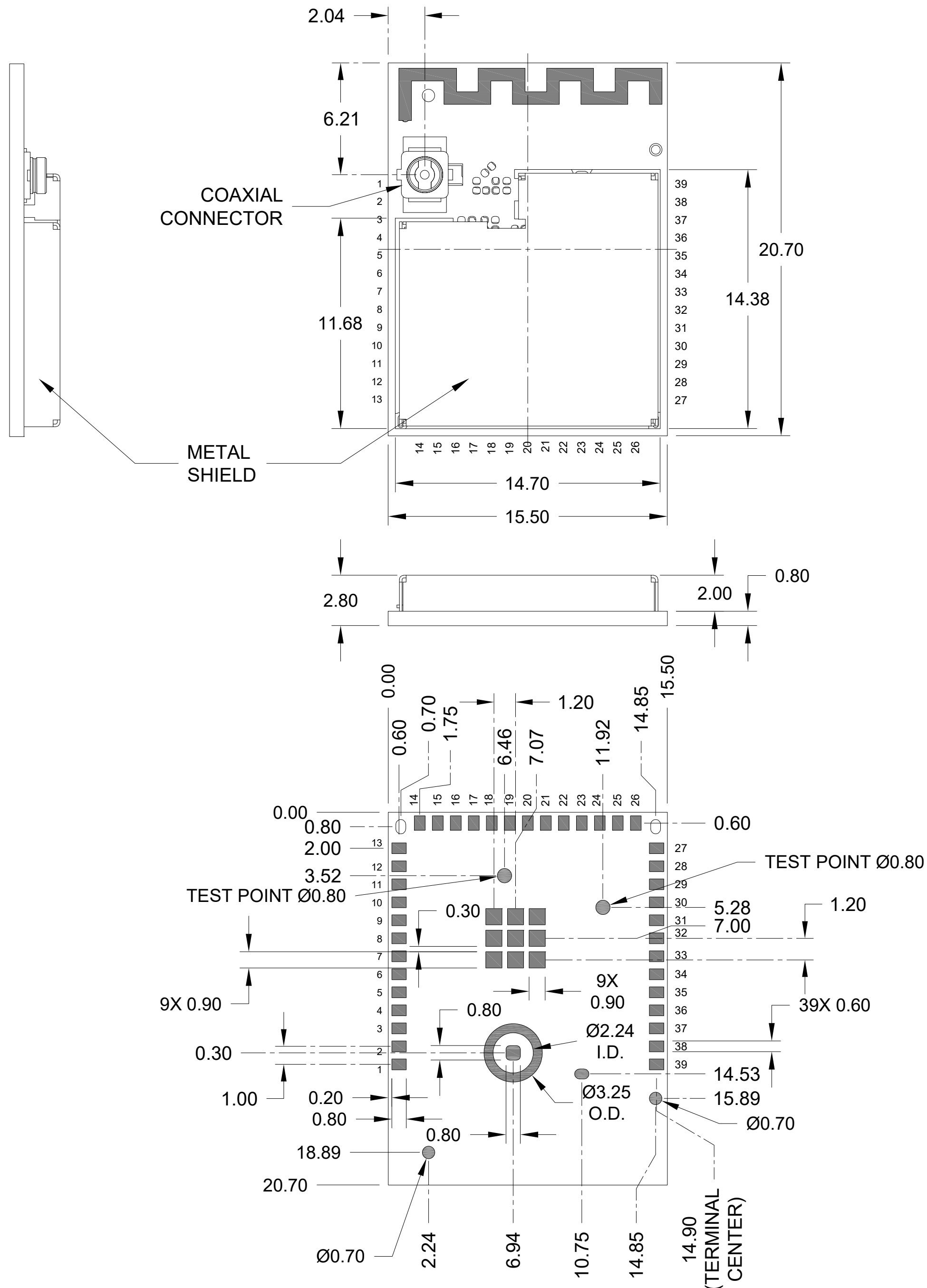
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23402 Rev A

44.3 WBZ451 Module Packaging Information

39-Lead PCB Module (ZSX) - 15.5x20.7x2.8 mm Body [MODULE] With Metal Shield and Coaxial Connector

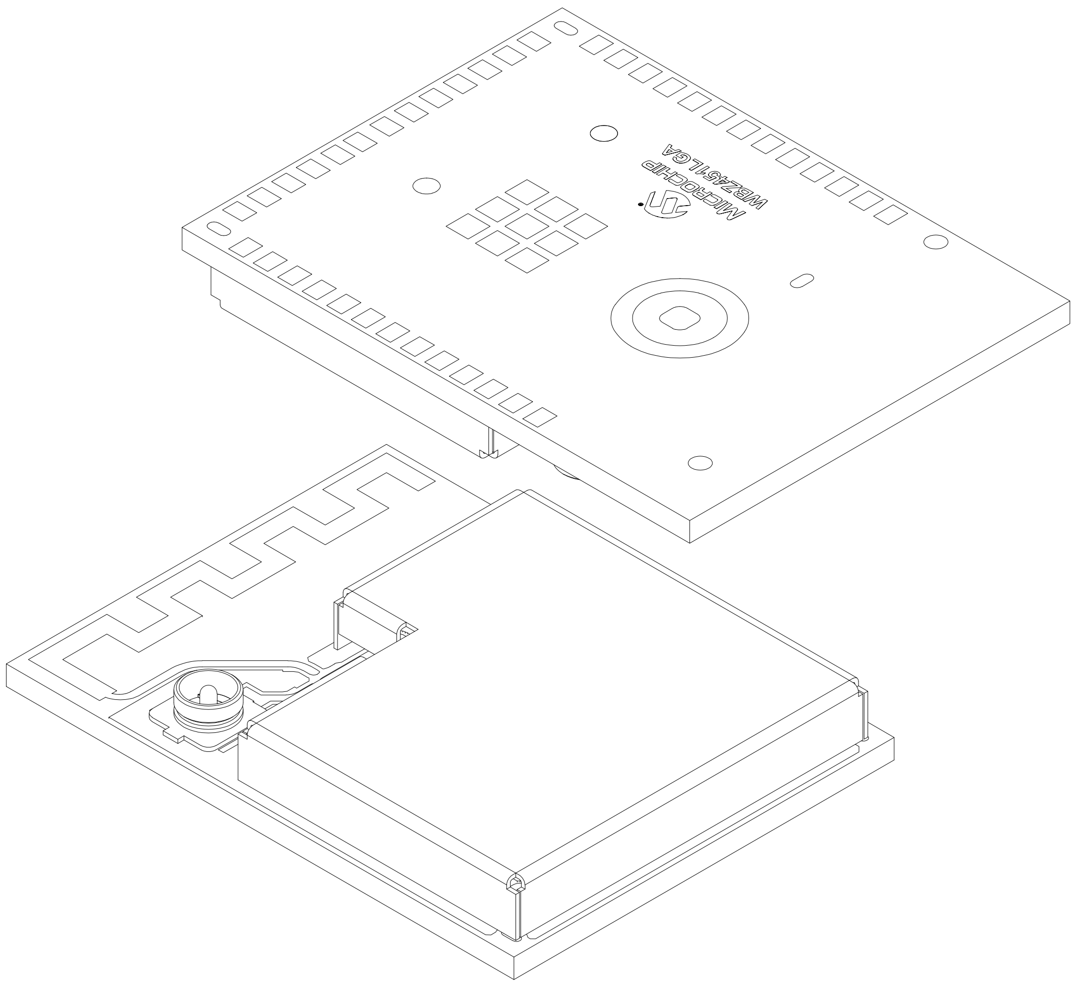
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-10052 Rev B Sheet 1 of 2

39-Lead PCB Module (ZSX) - 15.5x20.7x2.8 mm Body [MODULE]
With Metal Shield and Coaxial Connector

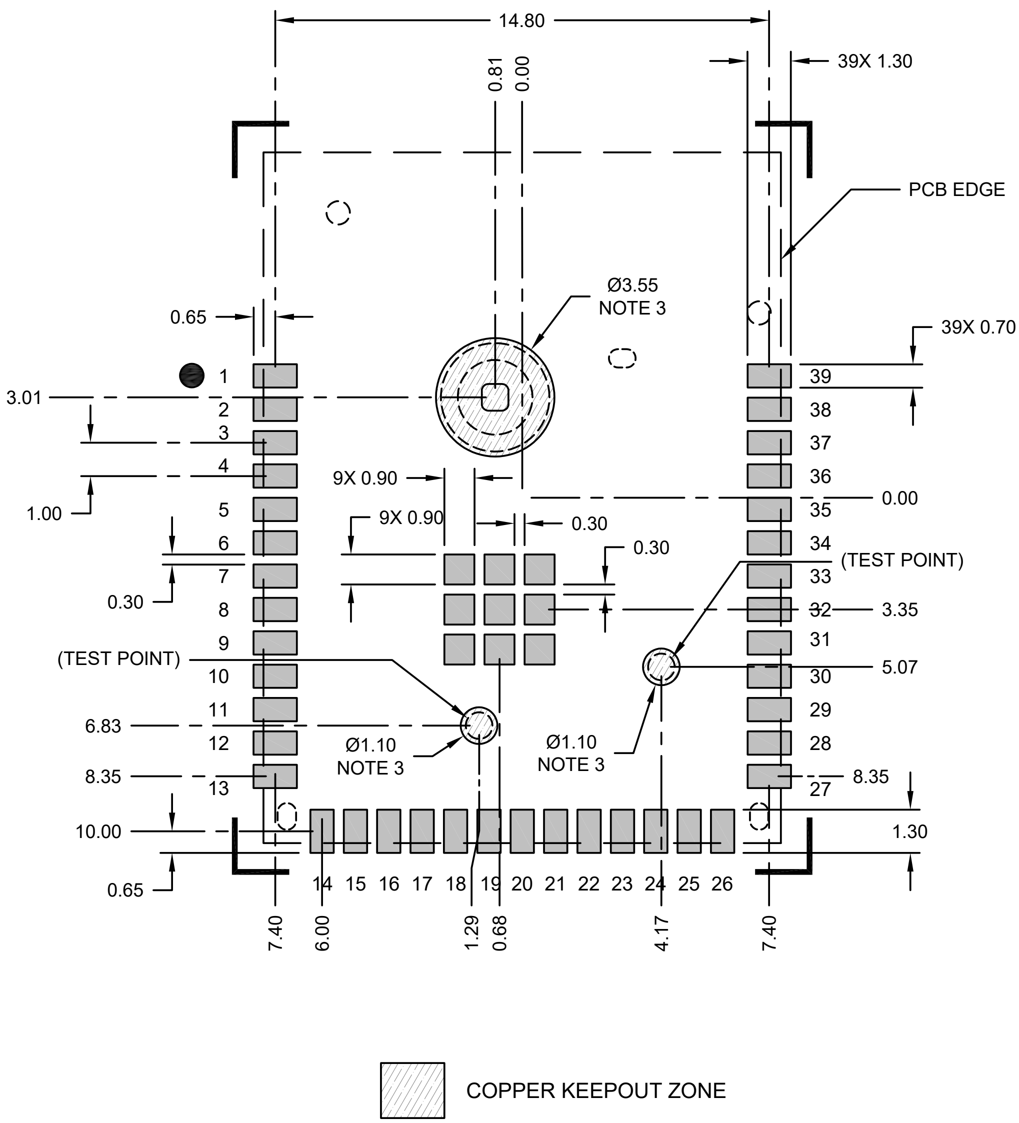
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-10052 Rev B Sheet 2 of 2

39-Lead PCB Module (ZSX) - 15.5x20.7x2.8 mm Body [MODULE]
With Metal Shield and Coaxial Connector

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Notes:

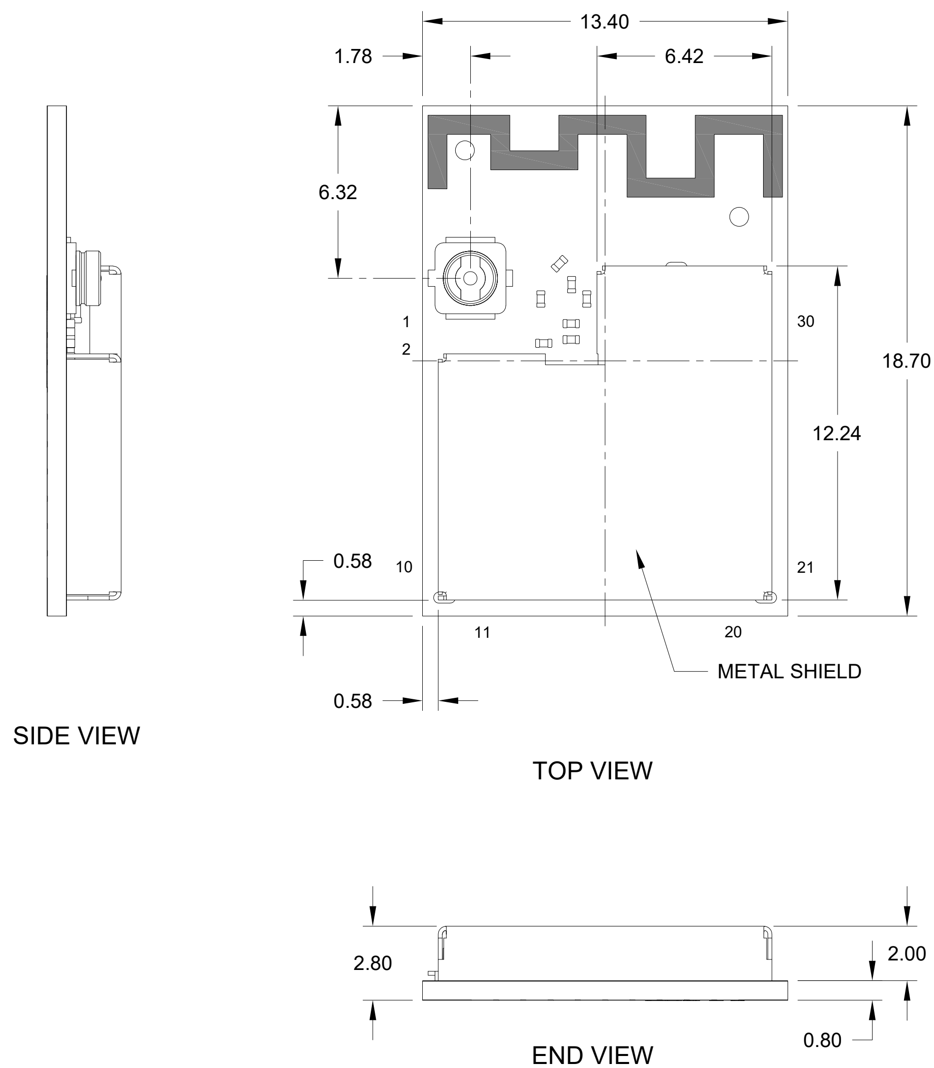
1. All dimensions are in millimeters.
2. Keep this area free from all metal, including ground fill.
3. Keep these areas free from routes and exposed copper. Ground fill with solder mask may be placed here.

Microchip Technology Drawing C04-12052 Rev B

44.4 WBZ450 Module Packaging Information

30-Lead PCB Module (ZRX) -13.4x18.7x2.8 mm Body [MODULE] For WBZ450 With Metal Shield and Coaxial Connector

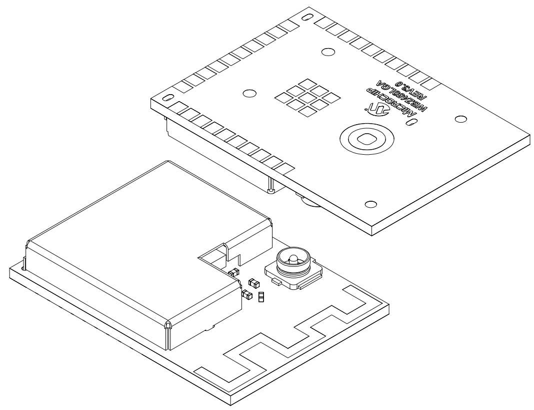
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

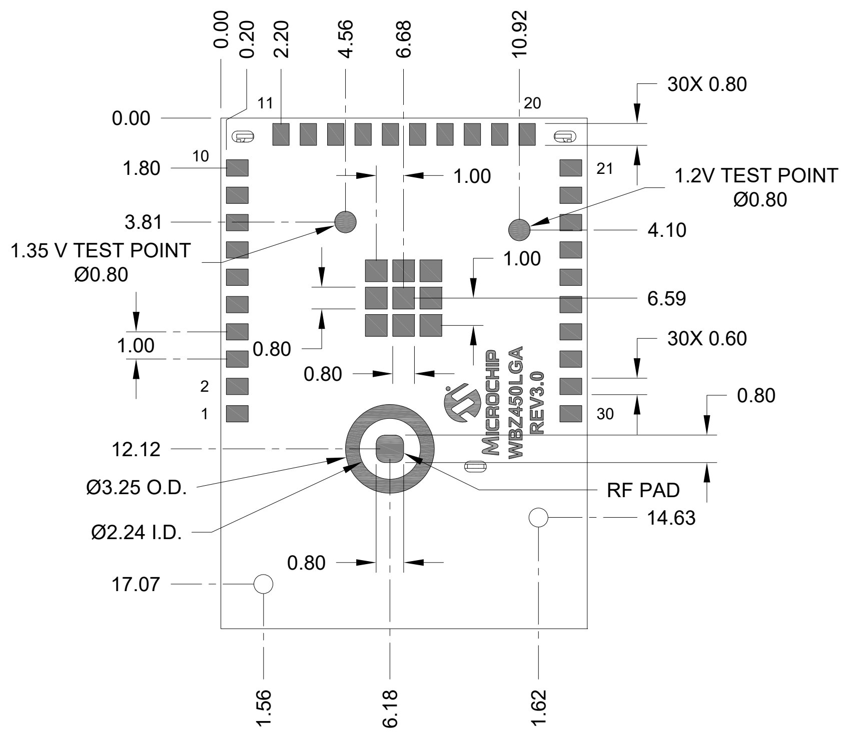


Microchip Technology Drawing C04-10051 Rev A Sheet 1 of 2

30-Lead PCB Module (ZRX) -13.4x18.7x2.8 mm Body [MODULE] For WBZ450 With Metal Shield and Coaxial Connector

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





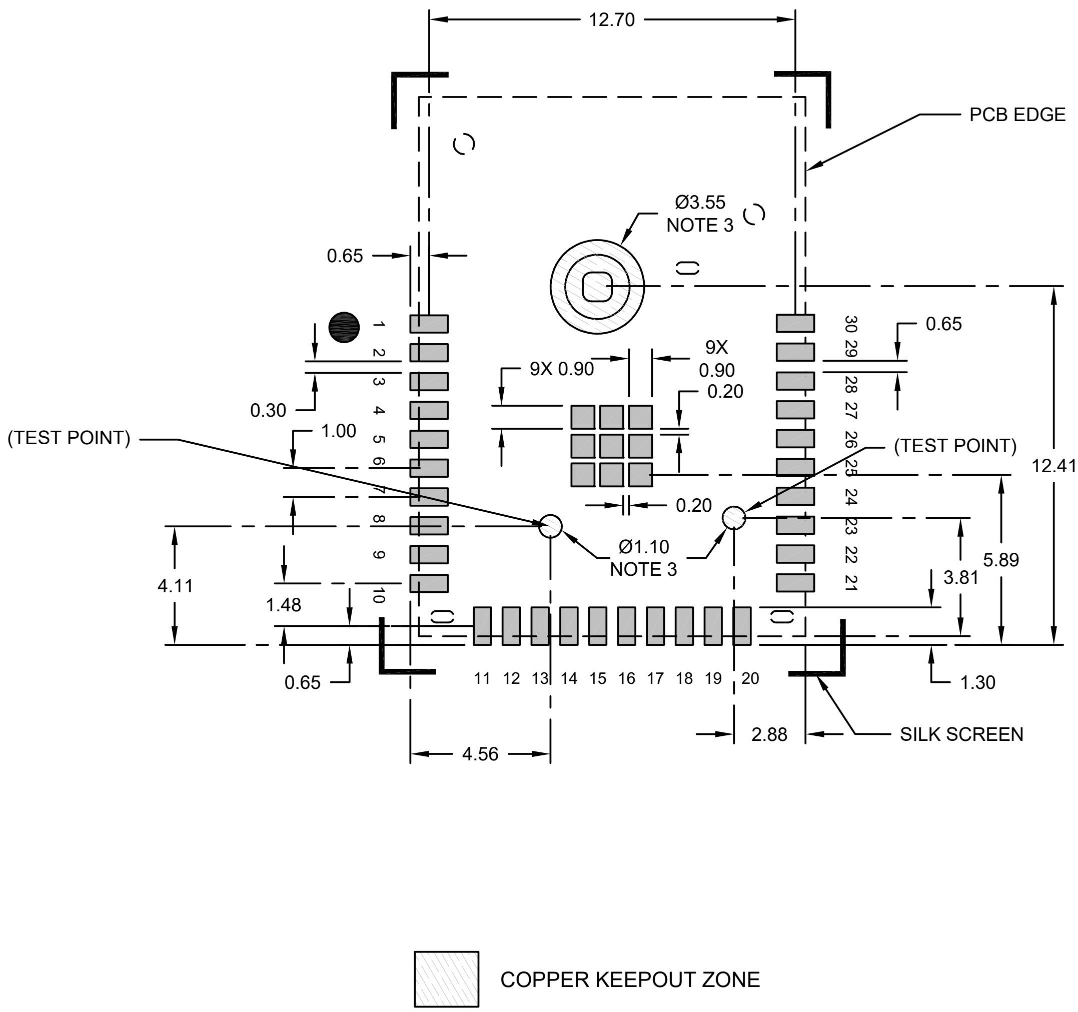
BOTTOM VIEW

Notes:

Microchip Technology Drawing C04-10051 Rev A Sheet 2 of 2

30-Lead PCB Module (ZRX) - 13.4x18.7X2.8 mm Body [Module] For WBZ450 With Metal Shield and Coaxial Connector

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Notes:

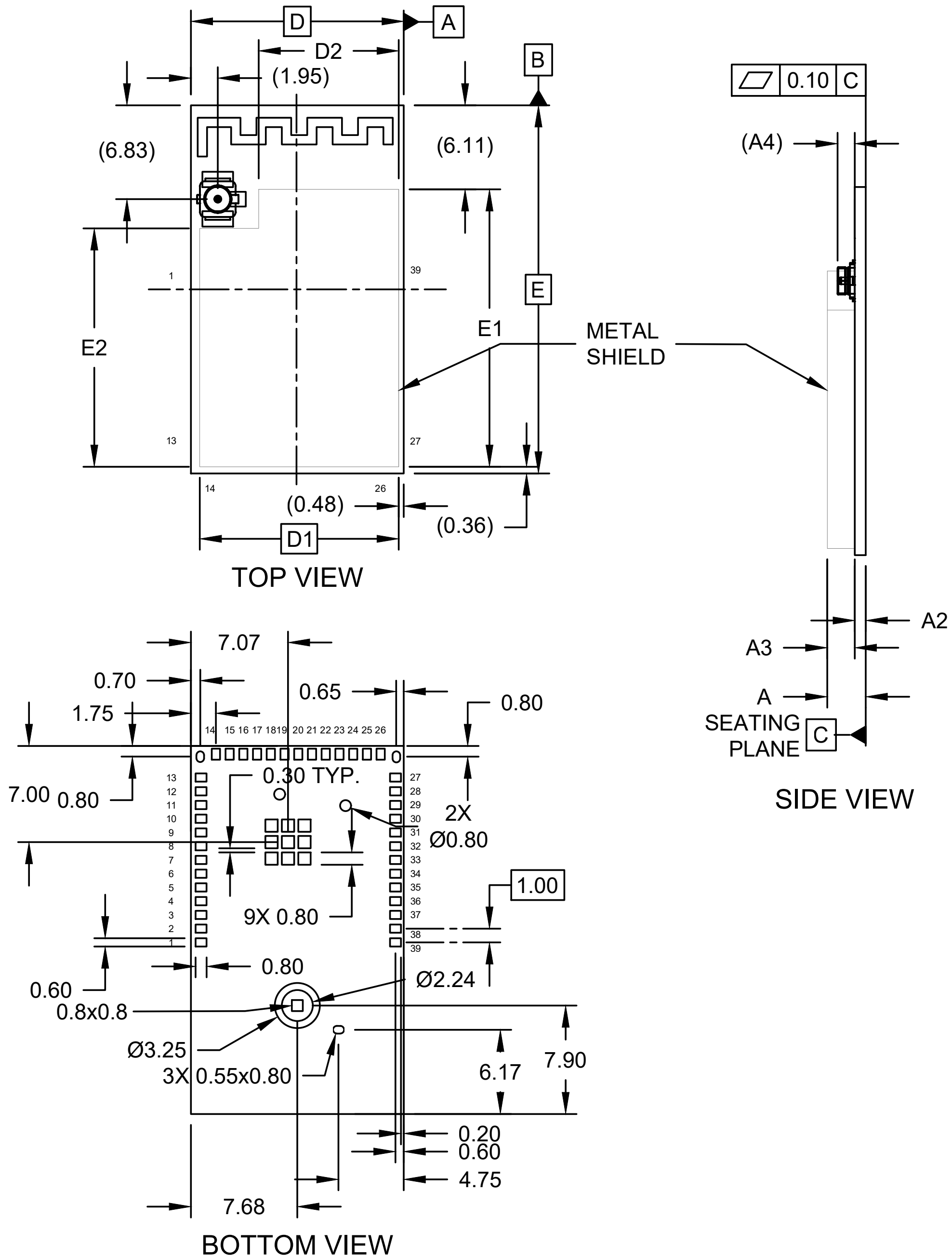
1. All dimensions are in millimeters.
2. Keep this area free from all metal, including ground fill.
3. Keep these areas free from routes and exposed copper. Ground fill with solder mask may be placed here.

Microchip Technology Drawing C04-12051 Rev A

44.5 WBZ451H Module Packaging Information

39-Lead PCB Module (4SW) - 15.5x26.8x2.8mm [MODULE] for WBZ451H With Metal Shield and Coaxial Connector

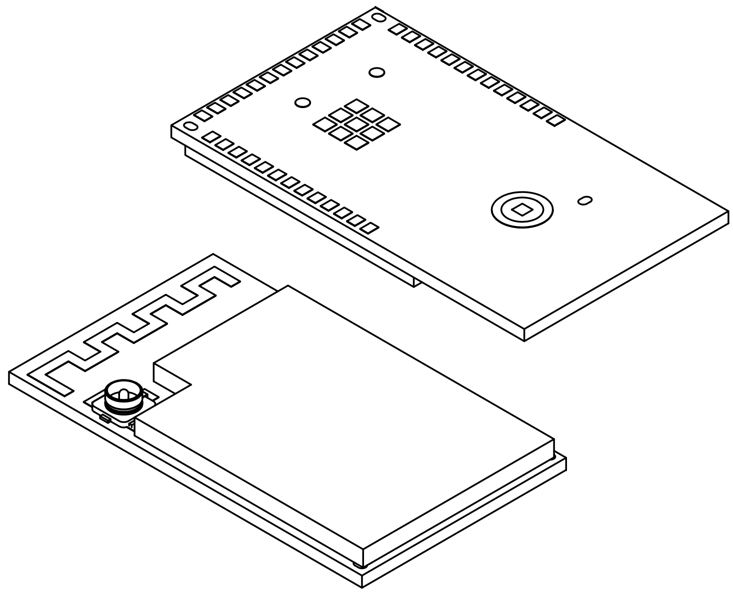
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-10056 Rev C Sheet 1 of 2

39-Lead PCB Module (4SW) - 15.5x26.8x2.8mm [MODULE] for WBZ451H With Metal Shield and Coaxial Connector

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		39	
Terminal Pitch	e		1.00 BSC	
Overall Height	A	-	2.80	-
PCB Thickness	A2	0.70	0.80	0.90
Shield Height	A3		2.00 REF	
UFL Connector Height	A4		1.25 REF	
Overall Length	D		15.50 BSC	
Overall Width	E		26.80 BSC	
Shield Length	D1	14.60	14.70	14.80
Shield Length	D2	10.24	10.34	10.44
Shield Width	E1	20.38	20.48	20.58
Shield Width	E2	17.50	17.60	17.70
Terminal Width	b	0.50	0.60	0.70
Terminal Length	L	0.70	0.80	0.90

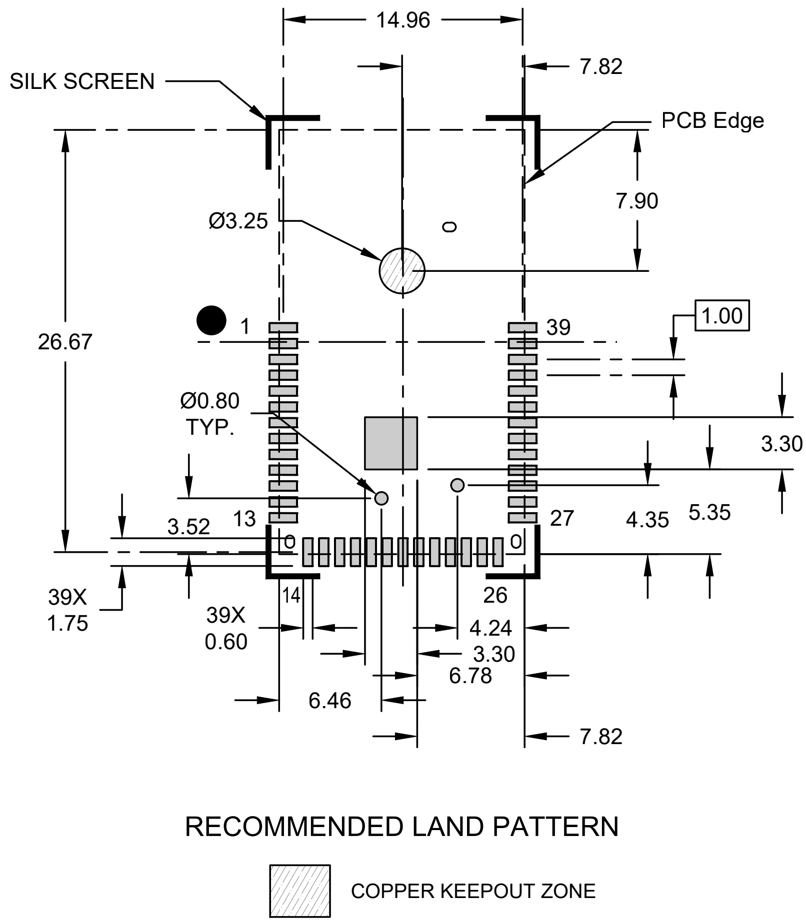
Notes:

1. All Dimensions are in Millimeters
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-10056 Rev C Sheet 2 of 2

39-Lead PCB Module (4SW) - 15.5x26.8x2.8mm [MODULE] for WBZ451H With Metal Shield and Coaxial Connector

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-12056 Rev C

45. Appendix A: Regulatory Approval

The WBZ450PC module has received regulatory approval for the following countries:

- Bluetooth Special Interest Group (SIG) QDID: 176567
- United States/FCC ID: 2ADHKWBZ450
- Canada/ISED:
  - IC: 20266-WBZ450
  - HVIN: WBZ450PC
- Europe/CE
- Japan/MIC: 020-220278
- Korea/KCC: R-R-mcp-WBZ450UE
- Taiwan/NCC: CCAN23Y10012T8

The WBZ450PE module has received regulatory approval for the following countries:

- Bluetooth Special Interest Group (SIG) QDID: 176567
- United States/FCC ID: 2ADHKWBZ450
- Canada/ISED:
  - IC: 20266-WBZ450
  - HVIN: WBZ450PE
- Europe/CE
- Japan/MIC: 020-220278
- Korea/KCC: R-R-mcp-WBZ450UE
- Taiwan/NCC: CCAN23Y10010T4
- China/SRRC: 2023DJ2426

The WBZ450UC module has received regulatory approval for the following countries:

- Bluetooth Special Interest Group (SIG) QDID: 176567
- United States/FCC ID: 2ADHKWBZ450
- Canada/ISED:
  - IC: 20266-WBZ450
  - HVIN: WBZ450UC
- Europe/CE
- Japan/MIC: 020-220278
- Korea/KCC: R-R-mcp-WBZ450UE
- Taiwan/NCC: CCAN23Y10013T0

The WBZ450UE module has received regulatory approval for the following countries:

- Bluetooth Special Interest Group (SIG) QDID: 176567
- United States/FCC ID: 2ADHKWBZ450
- Canada/ISED:
  - IC: 20266-WBZ450
  - HVIN: WBZ450PE
- Europe/CE
- Japan/MIC: 020-220278

- Korea/KCC: R-R-mcp-WBZ450UE
- Taiwan/NCC: CCAN23Y10011T6
- China/SRRC: 2023DJ2427(M)

The WBZ451PC module has received regulatory approval for the following countries:

- Bluetooth Special Interest Group (SIG) QDID: 176567
- United States/FCC ID: 2ADHKWBZ451
- Canada/ISED:
  - IC: 20266-WBZ451
  - HVIN: WBZ451PC
- Europe/CE
- Japan/MIC: 020-220180
- Korea/KCC: R-R-mcp-WBZ451PE
- Taiwan/NCC: CCAN22Y10503T6

The WBZ451PE module has received regulatory approval for the following countries:

- Bluetooth Special Interest Group (SIG) QDID: 176567
- United States/FCC ID: 2ADHKWBZ451
- Canada/ISED:
  - IC: 20266-WBZ451
  - HVIN: WBZ451PE
- Europe/CE
- Japan/MIC: 020-220180
- Korea/KCC: R-R-mcp-WBZ451PE
- Taiwan/NCC: CCAN22Y10501T2
- China/SRRC: 2023DJ2471

The WBZ451UC module has received regulatory approval for the following countries:

- Bluetooth Special Interest Group (SIG) QDID: 176567
- United States/FCC ID: 2ADHKWBZ451
- Canada/ISED:
  - IC: 20266-WBZ451
  - HVIN: WBZ451UC
- Europe/CE
- Japan/MIC: 020-220180
- Korea/KCC: R-R-mcp-WBZ451PE
- Taiwan/NCC: CCAN22Y10500T0

The WBZ451UE module has received regulatory approval for the following countries:

- Bluetooth Special Interest Group (SIG) QDID: 176567
- United States/FCC ID: 2ADHKWBZ451
- Canada/ISED:
  - IC: 20266-WBZ451
  - HVIN: WBZ451UE
- Europe/CE

- Japan/MIC: 020-220180
- Korea/KCC: R-R-mcp-WBZ451PE
- Taiwan/NCC: CCAN22Y10502T4
- China/SRRC: 2023DJ2475(M)

The WBZ451HPE module has received regulatory approval for the following countries:

- Bluetooth Special Interest Group (SIG) QDID: 176567
- United States/FCC ID: 2ADHKWBZ451H
- Canada/ISED:
  - IC: 20266-WBZ451H
  - HVIN: WBZ451HPE
- Europe/CE
- Japan/MIC: 020-240157
- Korea/KCC: R-R-mcp-WBZ451H
- Taiwan/NCC: CCAN24Y10470T7
- China/SRRC: 24J999P6Z250

The WBZ451HUE module has received regulatory approval for the following countries:

- Bluetooth Special Interest Group (SIG) QDID: 176567
- United States/FCC ID: 2ADHKWBZ451H
- Canada/ISED:
  - IC: 20266-WBZ451H
  - HVIN: WBZ451HUE
- Europe/CE
- Japan/MIC: 020-240157
- Korea/KCC: R-R-mcp-WBZ451H
- Taiwan/NCC: CCAN24Y10480T0
- China/SRRC: 24J999P6U904(M)

The WBZ451PE-E module has received regulatory approval for the following countries:

- Bluetooth Special Interest Group (SIG) QDID: 176567
- United States/FCC ID: 2ADHKWBZ451
- Canada/ISED:
  - IC: 20266-WBZ451
  - HVIN: TBD
- Europe/CE
- Japan/MIC: TBD
- Korea/KCC: TBD
- Taiwan/NCC: TBD
- China/SRRC: TBD

45.1 United States

The WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E received Federal Communications Commission (FCC) CFR47 Telecommunications, Part 15 Subpart C “Intentional Radiators” single-modular approval in accordance with Part 15.212 Modular Transmitter approval. Single-modular transmitter approval is defined as a complete RF transmission sub-assembly, designed to be incorporated into another device, that must demonstrate compliance with FCC rules and policies independent of any host. A transmitter with a modular grant can be installed in different end-use products (referred to as a host, host product or host device) by the grantee or other equipment manufacturer, then the host product may not require additional testing or equipment authorization for the transmitter function provided by that specific module or limited module device.

The user must comply with all of the instructions provided by the Grantee, which indicate installation and/or operating conditions necessary for compliance.

A host product itself is required to comply with all other applicable FCC equipment authorization regulations, requirements, and equipment functions that are not associated with the transmitter module portion. For example, compliance must be demonstrated: to regulations for other transmitter components within a host product; to requirements for unintentional radiators (Part 15 Subpart B), such as digital devices, computer peripherals, radio receivers, etc.; and to additional authorization requirements for the non-transmitter functions on the transmitter module (i.e., Suppliers Declaration of Conformity (SDoC) or certification) as appropriate (e.g., Bluetooth and Wi-Fi transmitter modules may also contain digital logic functions).

45.1.1 Labeling and User Information Requirements

The WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E been labeled with its own FCC ID number, and if the FCC ID is not visible when the module is installed inside another device, then the outside of the finished product into which the module is installed must display a label referring to the enclosed module. This exterior label must use the following wording:

For the WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE module	Contains Transmitter Module FCC ID: 2ADHKWBZ450 or Contains FCC ID: 2ADHKWBZ450 **This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation**.
For the WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451PE-E module	Contains Transmitter Module FCC ID: 2ADHKWBZ451 or Contains FCC ID: 2ADHKWBZ451 **This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation**.
For the WBZ451HPE/WBZ451HUE module	Contains Transmitter Module FCC ID: 2ADHKWBZ451H or Contains FCC ID: 2ADHKWBZ451H **This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation**.

The user's manual for the finished product must include the following statement:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

Additional information on labeling and user information requirements for Part 15 devices can be found in KDB Publication 784748, which is available at the FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB) apps.fcc.gov/oetcf/kdb/index.cfm.

45.1.2 RF Exposure

All transmitters regulated by FCC must comply with RF exposure requirements. KDB 447498 General RF Exposure Guidance provides guidance in determining whether proposed or existing transmitting facilities, operations or devices comply with limits for human exposure to Radio Frequency (RF) fields adopted by the Federal Communications Commission (FCC).

From the FCC Grant: Output power listed is conducted. This grant is valid only when the module is sold to OEM integrators and must be installed by the OEM or OEM integrators. This transmitter is restricted for use with the specific antenna(s) tested in this application for Certification and must not be co-located or operating in conjunction with any other antenna or transmitters within a host device, except in accordance with FCC multi-transmitter product procedures.

WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E: These modules are approved for installation into mobile or/and portable host platforms at least 4 cm away from the human body.

45.1.3 Helpful Web Sites

- Federal Communications Commission (FCC): www.fcc.gov.
- FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB) apps.fcc.gov/oetcf/kdb/index.cfm.

45.2 Canada

The WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E been certified for use in Canada under Innovation, Science and Economic Development Canada (ISED, formerly Industry Canada) Radio Standards Procedure (RSP) RSP-100, Radio Standards Specification (RSS) RSS-Gen and RSS-247. Modular approval permits the installation of a module in a host device without the need to recertify the device.

45.2.1 Labeling and User Information Requirements

Labeling Requirements (from RSP-100 - Issue 12, Section 5): The host product shall be properly labeled to identify the module within the host device.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host device; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number of the module, preceded by the word “Contains” or similar wording expressing the same meaning, as follows:

For the WBZ450PC/WBZ450PE/ WBZ450UC/WBZ450UE module	**Contains IC: 20266-WBZ450**
For the WBZ451PC/WBZ451PE/ WBZ451UC/WBZ451UE /WBZ451PE-E module	**Contains IC: 20266-WBZ451**
For the WBZ451HPE/WBZ451HUE module	**Contains IC: 20266-WBZ451H**

User Manual Notice for License-Exempt Radio Apparatus (from Section 8.4 RSS-Gen, Issue 5, February 2021): User manuals for license-exempt radio apparatus shall contain the following or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both:

This device contains license-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's license-exempt RSS(s). Operation is subject to the following two conditions:

(1) This device may not cause interference;

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1. L'appareil ne doit pas produire de brouillage;

2. L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Transmitter Antenna (From Section 6.8 RSS-GEN, Issue 5, February 2021): User manuals, for transmitters shall display the following notice in a conspicuous location:

This radio transmitter IC: 20266-WBZ450, IC: 20266-WBZ451 and IC: 20266-WBZ451H have been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Le présent émetteur radio IC: 20266-WBZ450, IC: 20266-WBZ451 and IC: 20266-WBZ451H a été approuvé par Innovation, Sciences et Développement économique Canada pour fonctionner avec les types d'antenne énumérés cidessous et ayant un gain admissible maximal. Les types d'antenne non inclus dans cette liste, et dont le gain est supérieur au gain maximal indiqué pour tout type figurant sur la liste, sont strictement interdits pour l'exploitation de l'émetteur.

Immediately following the above notice, the manufacturer shall provide a list of all antenna types approved for use with the transmitter, indicating the maximum permissible antenna gain (in dBi) and required impedance for each.

45.2.2 RF Exposure

All transmitters regulated by Innovation, Science and Economic Development Canada (ISED) must comply with RF exposure requirements listed in RSS-102 - Radio Frequency (RF) Exposure Compliance of Radiocommunication Apparatus (All Frequency Bands).

This transmitter is restricted for use with a specific antenna tested in this application for certification, and must not be co-located or operating in conjunction with any other antenna or transmitters within a host device, except in accordance with Canada multi-transmitter product procedures.

WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/ WBZ451HPE/WBZ451HUE/WBZ451PE-E: The devices operate at an output power level which is within the ISED SAR test exemption limits at any user distance greater than 20 cm.

45.2.3 Helpful Web Sites

Innovation, Science and Economic Development Canada (ISED): www.ic.gc.ca/.

45.3 Europe

The WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E is/are a Radio Equipment Directive (RED) assessed radio module that is CE marked and has been manufactured and tested with the intention of being integrated into a final product.

The WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E has/have been tested to RED 2014/53/EU Essential Requirements mentioned in the following European Compliance table.

Table 45-1. European Compliance Information

Certification	Standard	Article
Safety	EN 62368	3.1a
Health	EN 62311	
EMC	EN 301 489-1	3.1b
	EN 301 489-17	
Radio	EN 300 328	3.2

The ETSI provides guidance on modular devices in the "*Guide to the application of harmonised standards covering articles 3.1b and 3.2 of the RED 2014/53/EU (RED) to multi-radio and combined radio and non-radio equipment*" document available at http://www.etsi.org/deliver/etsi_eg/203300_203399/20 3367/01.01.01_60/eg_203367v010101p.pdf.

Note: To maintain conformance to the standards listed in the preceding European Compliance table, the module shall be installed in accordance with the installation instructions in this data sheet and shall not be modified. When integrating a radio module into a completed product, the integrator becomes the manufacturer of the final product and is therefore responsible for demonstrating compliance of the final product with the essential requirements against the RED.

45.3.1 Labeling and User Information Requirements

The label on the final product that contains the WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E must follow CE marking requirements.

45.3.2 Conformity Assessment

From ETSI Guidance Note EG 203367, section 6.1, when non-radio products are combined with a radio product:

If the manufacturer of the combined equipment installs the radio product in a host non-radio product in equivalent assessment conditions (i.e. host equivalent to the one used for the assessment of the radio product) and according to the installation instructions for the radio product, then no additional assessment of the combined equipment against article 3.2 of the RED is required.

45.3.2.1 Simplified EU Declaration of Conformity

Hereby, Microchip Technology Inc. declares that the radio equipment type WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E is/are in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity, for this product, is available at www.microchip.com/design-centers/wireless-connectivity/.

45.3.3 Helpful Websites

A document that can be used as a starting point in understanding the use of Short Range Devices (SRD) in Europe is the European Radio Communications Committee (ERC) Recommendation 70-03 E, which can be downloaded from the European Communications Committee (ECC) at: http://www.ecodocdb.dk/.

Additional helpful web sites are:

- Radio Equipment Directive (2014/53/EU):
  https://ec.europa.eu/growth/single-market/european-standards/harmonised-standards/red_en
- European Conference of Postal and Telecommunications Administrations (CEPT):
  http://www.cept.org
- European Telecommunications Standards Institute (ETSI):
  http://www.etsi.org
- The Radio Equipment Directive Compliance Association (REDCA):
  http://www.redca.eu/

45.4 Japan

The WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E received type certification and is required to be labeled with its own technical conformity mark and certification number as required to conform to the technical standards regulated by the Ministry of Internal Affairs and Communications (MIC) of Japan pursuant to the Radio Act of Japan.

Integration of this module into a final product does not require additional radio certification provided installation instructions are followed and no modifications of the module are allowed. Additional testing may be required:

- If the host product is subject to electrical appliance safety (for example, powered from an AC mains), the host product may require Product Safety Electrical Appliance and Material (PSE) testing. The integrator should contact their conformance laboratory to determine if this testing is required
- There is an voluntary Electromagnetic Compatibility (EMC) test for the host product administered by VCCI: www.vcci.jp/vcci_e/index.html

45.4.1 Labeling and User Information Requirements

The label on the final product which contains the WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E module(s) must follow Japan marking requirements. The integrator of the module should refer to the labeling requirements for Japan available at the Ministry of Internal Affairs and Communications (MIC) website.

For the WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E modules, due to a limited module size, the technical conformity logo and ID is displayed in the data sheet and/or packaging and cannot be displayed on the module label. The final product in which this module is being used must have a label referring to the type certified module inside:	
WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE module	R 020-220278
WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451PE-E module	R 020-220180

WBZ451HPE/WBZ451HUE module	020-240157

45.4.2 Helpful Web Sites

- Ministry of Internal Affairs and Communications (MIC): www.tele.soumu.go.jp/e/index.htm.
- Association of Radio Industries and Businesses (ARIB): www.arib.or.jp/english/.

45.5 Korea

The WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E received certification of conformity in accordance with the Radio Waves Act. Integration of this module into a final product does not require additional radio certification provided installation instructions are followed and no modifications of the module are allowed.

45.5.1 Labeling and User Information Requirements

The label on the final product which contains the WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E module(s) must follow KC marking requirements. The integrator of the module should refer to the labeling requirements for Korea available on the Korea Communications Commission (KCC) website.

The WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E modules are labeled with its own KC mark. The final product requires the KC mark and certificate number of the module:	
WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE module	**R-R-mcp-WBZ450UE**
WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451PE-E module	**R-R-mcp-WBZ451PE**
WBZ451HPE/WBZ451HUE module	**R-R-mcp-WBZ451H**

45.5.2 Helpful Websites

- Korea Communications Commission (KCC): www.kcc.go.kr.
- National Radio Research Agency (RRA): rra.go.kr.

45.6 Taiwan

The WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E received compliance approval in accordance with the Telecommunications Act. Customers seeking to use the compliance approval in their product should contact Microchip Technology sales or distribution partners to obtain a Letter of Authority.

Integration of this module into a final product does not require additional radio certification provided installation instructions are followed and no modifications of the module are allowed.

45.6.1 Labeling and User Information Requirements

For the WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E modules, due to the limited module size, the NCC mark and ID are displayed in the data sheet only and cannot be displayed on the module label:	
WBZ450PC module	CCAN23Y10012T8
WBZ450PE module	CCAN23Y10010T4
WBZ450UC module	CCAN23Y10013T0
WBZ450UE module	CCAN23Y10011T6
WBZ451PC module	CCAN22Y10503T6
WBZ451PE module	CCAN22Y10501T2

WBZ451UC module	CCAN22Y10500T0
WBZ451UE module	CCAN22Y10502T4
WBZ451HPE	CCAN24Y10470T7
WBZ451HUE	CCAN24Y10480T0
WBZ451PE-E	CCANTBD

The user's manual should contain following warning (for RF device) in traditional Chinese:

根據 NCC LP0002 低功率射頻器材技術規範_章節 3.8.2：

取得審驗證明之低功率射頻器材，非經核准，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。

低功率射頻器材之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。

前述合法通信，指依電信管理法規定作業之無線電通信。

低功率射頻器材須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

此模組於取得認證後將依規定於模組本體標示審驗合格標籤，並要求平台廠商於平台上標示本產品內含發射器模組

45.6.2 Helpful Web Sites

National Communications Commission (NCC): www.ncc.gov.tw

45.7 China

The WBZ450PE/WBZ451PE/WBZ451HPE/WBZ451PE-E modules has/have received certification of conformity in accordance with the China MIIT Notice 2014-01 of State Radio Regulation Committee (SRRC) certification scheme. Integration of this module into a final product does not require additional radio certification, provided installation instructions are followed and no modifications of the module are allowed. Refer to SRRC certificate available in WBZ450PE/WBZ451PE/WBZ451HPE/WBZ451PE-E product page for expiry date.

The WBZ450UE/WBZ451UE/WBZ451HUE modules have received certification of conformity in accordance with the China MIIT Notice 2014-01 of State Radio Regulation Committee (SRRC) certification scheme under Limited Modular Approval (LMA). Integration of this module into a final product does require additional radio certification (radiated spurious emission test and EMC test), provided installation instructions are followed and no modifications of the module are allowed. Refer to SRRC certificate available in WBZ450UE/WBZ451UE/WBZ451HUE product page for expiry date.

45.7.1 Labeling and User Information Requirements

The WBZ450PE/WBZ451PE, WBZ450UE/WBZ451UE and WBZ451HPE/WBZ451HUE/WBZ451PE-E modules are labeled with its own CMIIT ID as follows:	
WBZ450PE module	CMIIT ID: 2023DJ2426
WBZ451PE module	CMIIT ID: 2023DJ2471
WBZ450UE module	CMIIT ID: 2023DJ2427(M)
WBZ451UE module	CMIIT ID: 2023DJ2475(M)
WBZ451HPE module	CMIIT ID: 24J999P6Z250
WBZ451HUE module	CMIIT ID: 24J999P6U904(M)
WBZ451PE-E	CMIIT ID: TBD

When Host system is using an approved Full Modular Approval (FMA) radio: The host must bear a label containing the statement "This device contains SRRC approved Radio module CMIIT ID: 24J999P60003,CMIIT ID: 2023DJ14927, CMIIT ID: 24J999P60004(M),CMIIT ID: 2023DJ14948(M).

45.8 UKCA (UK Conformity Assessed)

The WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E module is a UK conformity assessed radio module that meets all the essential requirements according to CE RED requirements.

45.8.1 Labeling Requirements for Module and User's Requirements

The label on the final product that contains the WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E module must follow UKCA marking requirements.

The UKCA mark above is printed on the module itself or on the packing label.

Additional details for the label requirement are available at:

https://www.gov.uk/guidance/using-the-ukca-marking#check-whether-you-need-to-use-the-new-ukca-marking.

45.8.2 UKCA Declaration of Conformity

Hereby, Microchip Technology Inc. declares that the radio equipment type the WBZ450PC/WBZ450PE/WBZ450UC/WBZ450UE and WBZ451PC/WBZ451PE/WBZ451UC/WBZ451UE/WBZ451HPE/WBZ451HUE/WBZ451PE-E modules are in compliance with the Radio Equipment Regulations 2017. The full text of the UKCA declaration of conformity for this product is available (under *Documents > Certifications*) at: www.microchip.com/en-us/product/WBZ451PE.

45.8.3 Helpful Websites

For more information on the UKCA regulatory approvals, refer to the www.gov.uk/guidance/placing-manufactured-goods-on-the-market-in-great-britain.

45.9 Other Regulatory Information

- For information about other countries' jurisdictions not covered here, refer to the www.microchip.com/design-centers/wireless-connectivity/certifications.
- Should other regulatory jurisdiction certification be required by the customer, or the customer needs to recertify the module for other reasons, contact Microchip for the required utilities and documentation.

46. Appendix B: Acronyms and Abbreviations

Table 46-1. Acronyms and Abbreviations

Acronyms	Abbreviations
AC	Analog Comparator
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AGC	Automatic Gain Control
AHB	Advanced High-Speed Bus
Apple® NCS	Apple Notification Center Service
AON	Always ON
APB	Advanced Peripheral Bus
API	Application Programming Interface
Arb	Arbiter
BFM	Boot Flash Memory
BG	Bandgap
Bluetooth® LE	Bluetooth Low Energy
BOD	Brown-out Detect
BOM	Bill of Material
BOR	Brown-out Reset
Bluetooth QTF	Bluetooth Qualification Test Facility
CCL	Configurable Custom Logic
CDM	Charged Device Model
CFG	System Configuration and Register Locking
CFGCON	Configuration Control
CLDO	Core Low Dropout Regulator
CLK	Clock
CM	Configuration Mismatch Reset
CM4CPU	Cortex M4F Processor
CMCC	Cortex M Cache Controller
CMR	Configuration Mismatch Reset
CN	Change Notification
CNCON	Change Notice Control
CNEN	Change Notice Enable
CNF	Change Notice Flag
CNPDE	Change Notice Pull-down Enable
CNPUE	Change Notice Pull-up Enable
CNSTAT	Change Notice Status
CP	Charge Pump
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CRM	Continuous Read Mode
CoreSight™ ROM	CoreSight ROM
CRU	Clock and Reset Unit
CS	Chip Select
CSD	Controlled Switching Device

...........continued

Acronyms	Abbreviations
CVD	Capacitive Voltage Divider
DAC	Digital-to-Analog Converter
DAP	Debug Access Port
DCC	Debug Communication Channel
DDR	Double Data Rate
DED	Double-bit Error Detected
DFE	Digital Front-End
DMAC	Direct Memory Access Controller
DMA RD	DMA-Read
DMA WR	DMA-Read
DMT	Deadman Timer
DMTCON	Deadman Timer Control
DMTEN	Deadman Timer Enable
DMTR	Deadman Timer Reset
DSCTRL	Deep Sleep System Controller
DSP	Digital Signal Processor
DSU	Device Service Unit
DSWDT	Deep Sleep WDT
DTI	Dead-Time Insertion
ECC	Error Correction Code
ECDH	Elliptic-Curve Diffie-Hellman encryption
EIC	External Interrupt Controller
EOC	End-Of-Convert
EOS	Electrical Overstress
ERR	Error
ESD	Electrostatic Discharge
ETB	Embedded Trace Buffer
ETM	Embedded Trace Module
EVSYS	Event System Interface
FC	Flash Controller
FCS	Frame Check Sequence
FEM	Front-End Module
FPB	Flash Patch and Breakpoint Unit
FPU	Floating Point Unit
FRC	Fast RC Oscillator
FRCDIV	FRC Divider
FREQM	Frequency Meter
FSCM	Fail-Safe Clock Monitor
FSM	Finite State Machine
GATT	Generic Attribute Profile (Bluetooth)
GCLK	Generic Clock Controller
GCM	Galois Counter Mode
GND	Ground
GPIO	General Purpose I/O
HBM	Human Body Model

...........continued

Acronyms	Abbreviations
HCI	Host Controller Interface
I2C	Inter-Integrated Circuit
ICM	Integrity Check Module
IoT	Internet of Things
IRQ	Interrupt Request
ITM	Instrumentation Trace Macrocell
LDO	Low Dropout Regulator
LE	Low-Energy
LIN	Local Interconnect Network
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPCLK	Low Power Clock Generation
LPRC	Low Power RC Oscillator
LUT	Each Look-Up Table
LVD	Low-Voltage Detect
MCLRF	Master Clear Filter
MCS	Master Clock Switch
MCU	Microcontroller Unit
MFRQ	Match Frequency
MLDO	Main LDO
MPU	Memory Protection Unit
NDA	Non-Disclosure Agreement
NFRQ	Normal Frequency
NMCLR	External Reset
NMI	Non-Maskable Interrupt
NMITR	NMI Time-out Reset
NPWM	Normal Pulse-Width Modulation
NVIC	Nested Vector Interrupt Controller
NVM	Non-Volatile Memory
NVMOP	Non-Volatile Memory Operation
OCD	On-Chip Debug
OTA	Over-The-Air
OTF	On-The-Fly
OTMX	Output Matrix
OTP	One Time Programmable
PA	Power Amplifier
PAC	Peripheral Access Controller
PCHE	Prefetch Cache
PFM	Program Flash Memory
PHY	Physical Layer
PLL	Phase-Locked Loop
PMD	Peripheral Module Disable
PMU	Power Management Unit
POR	Power-on Reset
POSC	Primary Crystal Oscillator

...........continued

Acronyms	Abbreviations
PPS	Peripheral Pin Select
PPW	Period and Pulse-Width
PSDU	PLCP Service Data Unit
PSM	Pulse Skipping Mode
PUKCC	Public Key Cryptography Controller
PUKCL	Public Key Cryptography Library
PWM	Pulse Width Modulation
QoS	Quality of Service
QSPI	Quad I/O Serial Peripheral Interface
QSPI	Quad SPI interface
RAMECC	RAM Error Correction Code
RCON	Reset Control
REG	Register
RF	Radio Frequency
RFFE	RF Front-End
RoT	Root of Trust
RPC	Remote Procedure Call
RSSI	Receive Signal Strength Indication
RTC	Real-Time Counter
RTCC	Real-Time Clock Calender
RTOS	Real-Time Operating System
RTSP	Run-Time Self Programming
RX	Receive
RXC	Receive Complete
SEC	Single-bit Error Corrected
SERCOM	Serial Communication Interface
SERCOM I^2C	SERCOM Inter-Integrated Circuit
SFD	Start Frame Delimiter (Zigbee®)
SFR	Special Function Register
SHA	Secure Hash Algorithm
SMBus™	System Management Bus
SoC	System-on-Chip
SOSC	Secondary Crystal Oscillator
SPI	Serial Peripheral Interface
SRCON	Slew Rate Control
SSL	SPI Select Low
SWD	Serial Wire Debug
SWR	Software Reset
SWV	Serial Wire Viewer
Synth	Synthesizer
SYSRST	System Reset
TC	Timer Counter
TCC	Timer Counter Control
TCM	Tightly Coupled Memory
TPIU	Trace Port Interface Unit

...........continued

Acronyms	Abbreviations
TRNG	True Random Number Generator
TRX	Transmit/Receive
TX	Transmit
TXC	Transmit Complete
UART	Universal Asynchronous Receiver/Transmitter
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
VGA	Variable Gain Amplifier
WDT	Watchdog Timer
WDTO	Watchdog Time-Out Reset
WDTR	Watchdog Timer Reset
XDS	Extreme Deep Sleep
xIP	Execute-In-Place
XTAL	Crystal Oscillator
ZPBOR	Zero-Power BOR

47. Document Revision History

Table 47-1. Revision - C, Date - 09/2024

Section	Description
Introduction	Updated the trademark symbol
Operating Conditions	Added WBZ451H operating conditions
Bluetooth	Added WBZ451H "Typical Receiver Power Sensitivity"
802.15.4/Zigbee Modulation Scheme	• Added WBZ451H " RX sensitivity" • Added WBZ451H "TX Output Power" • Updated the sensitivity value for RPC mode
System Peripherals	Removed the feature "One Analog Comparator (AC) with Window Compare function"
Core: 64 MHz ARM Cortex-M4	Updated 3.35 Coremark®/MHz to 2.42 Coremark/MHz
WBZ45 Module Variants	Added WBZ451H module
Acronyms and Abbreviations	Added new
WBZ45 Module Ordering Information	Added WBZ451H ordering information
Configuration Summary	Added WBZ451H "Configuration Summary"
WBZ45 Module Description	Added WBZ451H "Module Block Diagram"
Pinout Diagram	Added WBZ451H "Pinout Diagram"
Power Pins	Added WBZ451H power pin details
Reset Requirements	Added new topic for WBZ451H
WBZ451H Module Interface Specifications	Added new topic for WBZ451H
Figure 4-11	Added the figure for WBZ451H
WBZ45 Module RF Considerations	Added "RF Specifications" for WBZ451H
Pinout and Signal Descriptions List	Added "Pinout and Signal Descriptions List" for WBZ451H
INTFLAG	"This flag is set when a new measurement is completed" added as a note
CTRLC	Added a note regarding LIN specification for bits 8 to 9 and 0 to 2
LUTCTRL	Added a note for bit 1: "Prevents/protects write access to the other bits in the LUTCTRL registers"
• Event Capture Action • Period and Pulse-Width (PPW) Capture Action • Pulse-Width Capture Action • Timestamp Capture • Waveform Output Generation Operations • Capture Operations	Added "The user needs to clear INTFLAG.MCx at the beginning of the interrupt routine and poll the bit until INTFLAG.MCx is cleared, before exiting the ISR" as additional sentence
CTRLBCLR	Updated register description for bit 0
CTRLBCLR	Updated register description for bit 0
Features	• Updated the values for Bluetooth® receiver power sensitivity • Updated the values for Zigbee® RX sensitivity • Added "Programmable Transmit Output Power" for WBZ451H • Added "Typical Receiver Power Sensitivity" for WBZ451H

RF Physical Layer	Added “Transceiver Architecture” figure for WBZ451H
Transmit Mixer and Power Amplifier	Added note related to WBZ451H
Absolute Maximum Electrical Characteristics	Removed tolerant pin
Power Supply Electrical Specifications	• Updated the topic title • Updated REG_51 and REG_52 characteristics • Added 2.1 minimum value and added the condition for REG_48A
Active Current Consumption DC Electrical Specifications (85°C), Active Current Consumption DC Electrical Specifications (125°C), Idle Current Consumption DC Electrical Specifications (85°C), Idle Current Consumption DC Electrical Specifications (125°C), Sleep Current Consumption DC Electrical Specifications (85°C), Sleep Current Consumption DC Electrical Specifications (125°C), Deep Sleep Current Consumption DC Electrical Specifications (85°C), Deep Sleep Current Consumption DC Electrical Specifications (125°C), XDS (Extreme Deep Sleep) Current Consumption DC Electrical Specifications (85°C), XDS (Extreme Deep Sleep) Current Consumption DC Electrical Specifications (125°C)	Changed the note “Typical value measured during characterization across voltage and temperature” into “Typical value measured at 25°C and 3.3V”
I/O PIN AC/DC Electrical Specifications	• Updated min and max values • Removed note related to 5V pin • Changed all VDDIO from 3.3 to 3.6V
External XTAL and Clock AC Electrical Specifications	• Removed Typ value for XOSC_2 • Removed note related to XOSCCTRL.STARTUP
XOSC32 AC Electrical Specifications	Removed XOSC32_12 and XOSC32_14
TCCx Timer Capture Module AC Electrical Specifications	Updated the timing diagram
Frequency AC Electrical Specifications	Removed min and max values for PLL_3
Bluetooth Low Energy RF Characteristics	• Updated typical values for BTRX1, BTRX3, BTRX4, BTRX5, BTRX6, BTRX7 and BTRX8 • Added WBZ451H-related characteristic data
Zigbee RF Characteristics	• Removed the conditions for ZBT3 • Updated the typical value for ZBRX1 • Added WBZ451H related characteristic data
Appendix A: Regulatory Approval	Added “Regulatory Approval” for WBZ451H

Table 47-2. Revision - B, Date - 12/2023

Section	Description
Bluetooth	• Typical receiver power sensitivity values updated • Updated digital RSSI indicator -30 dBm to -50 dBm
802.15.4/Zigbee Modulation Scheme	Changed RX sensitivity 103 dBm to 100 dBm
System Peripherals	Minor change
Package	Updated with WBZ450 information
WBZ45 Module Features	Updated the sentence
WBZ45 Module Variants	Updated with WBZ450 information
Package and Operating Conditions	
Certifications	Added one of the notes
PIC32CX-BZ2 SoC Ordering Information	Added PIC32CX1012BZ24032 ordering information

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Section	Description
WBZ45 Module Ordering Information	Added WBZ450 ordering information
Configuration Summary	Updated with WBZ450 information
Pinout Diagram	Added PIC32CX1012BZ24032 pinout diagram
Pinout Diagram	Added WBZ450 pinout diagram
Basic Connection Requirement	Added WBZ450 diagram
Unused I/O Pins	Removed the note
PCB Antenna	Added antenna radiation pattern images
External Antenna Placement Recommendations	Updated the figure
Pinout and Signal Descriptions List	Updated with WBZ450 information
CHECON	Minor change
PBxDIV, REFOxTRIM, REFOxCON, SLEWCON, CLK_DIAG, SPLLCON	Updated the Reset values
Power Modes	Minor change
DSCON	Added new topic
CFGCON0(L)	Minor change
CFGCON1(L)	Added new bits
CFGPCLKGEN1	Minor change
Features	Added COMP and COMP1 related points
Features	Typical receiver power sensitivity values updated
RF Physical Layer	Updated transceiver architecture block diagram
Transmit Mixer and Power Amplifier	Minor change
Electrical Characteristics	Updated all the topics for this chapter
WBZ450 Module Packaging Information	Added WBZ450 packaging information
Appendix A: Regulatory Approval	• Updated with WBZ450 information • Added Japan, Korea, Taiwan, China

Table 47-3. Revision - A, Date - 10/2022

Section	Description
Document	Initial revision

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