Inforce 67X1

User Guide

Rev A

November 18, 2021

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Preface

This User Guide explains Usage of the Inforce 67X1 board.

Intended Audience

This Hardware Reference Manual is intended for technically qualified personnel. It is not intended for general audiences.

Document Organization

The chapters in this document are arranged as follows:

1. Scope
2. Hardware Specifications
3. Mechanical Specifications
4. Appendix A
5. Contact Information

Conventions

The following conventions are used in this document:

 **CAUTION**

Cautions warn the user about how to prevent damage to hardware or loss of data.

 **NOTE**

Notes call attention to important information.

Note

- This document is subject to change without notice.
- Carrier parts are shown in some of the sections for better understanding.

Support Information

Every effort has been made to ensure the accuracy of the Hardware Reference Manual. If you have any comments, questions, or ideas regarding this document, contact SMART Wireless's technical support at **TechSupport-wc@smartwirelesscompute.com**.

Terminology

The table below gives descriptions to some common terms used in the Hardware Reference Manual.

Term	Description
BLE	Bluetooth Low Energy
bps	Bits Per Second
CSI	Camera Serial Interface
DDR	Double Data Rate
DS	Default Speed
DSI	Display Serial Interface
DSP	Digital Signal Processing
GPIO	General-Purpose Input/Output
GPS	Global Positioning System
GPU	Graphical Processing Unit
HPH	Head Phone
HS	High Speed
HVX	Hexagon Vector Extensions
I2C	Inter-Integrated Circuit
JTAG	Joint Test Action Group
LDO	Low Drop Out
LED	Light-Emitting Diode
LPDDR	Low-power DDR
MIC	Microphone
MIPI	Mobile Industry Processor Interface
OTG	On The Go
PCIe	Peripheral Component Interconnect Express
PMIC	Power Management IC
PoP	Package On Package
PU	Pull Up
RF	Radio Frequency
SDC	Secure digital controller
SDIO	Secured Data Input/output
SDR	Single Data Rate
SLIM bus	Serial Low-power Inter-chip Media Bus
SOC	System On Chip
SOM	System on Module
SPI	Serial Peripheral Interface
SPMI	System power management interface
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
WLAN	Wireless local area network

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1. SCOPE

This document describes the Usage of Qualcomm SDA845-based Inforce 67X1 SOM.

Overview

The table below presents a brief overview of Inforce 67X1 board.

Table 1: Inforce 67X1 Board Overview

Processor		
Processor	Qualcomm® Snapdragon™845 Processor (PoP package) SDA845 SoC	
Memory Devices		
Main Memory and Storage	4GB LPDDR4X, 1866Mhz 64GB UFS 2.1	
SOM Interfaces		
Interfaces	1× USB v3.1 Gen 1 (Host) 1× USB v3.1 Gen 1Type C (Device mode, Host mode, DP, Debug) 2x 4 lane MIPI-DSI 1×UART(Debug) 3× 4 Lane MIPI-CSI(D-PHY & C-PHY) 2x Camera Control I2C, 1× PCIe Gen 2 1x PCIe Gen 3 2× MHF4-WiFi/BT, 1× MHF4 – GPS	1× 4 bit SDC for SDcard 2× Line Out 1x Ear out 5× Mic In 1× Headphone Out, 1xSlimBUS[1] 1x MI2S 1x Sensor Core I2C 1x Backlight Regulator 10x Regulator Out
Form Factor		
Mechanical	50mm×28mm Tolerance +/- 0.2mm	
Power		
Power Input	VBAT (+3.2 to +4.5V)	
Others		
Temperature Specification	Commercial Grade	

NOTE

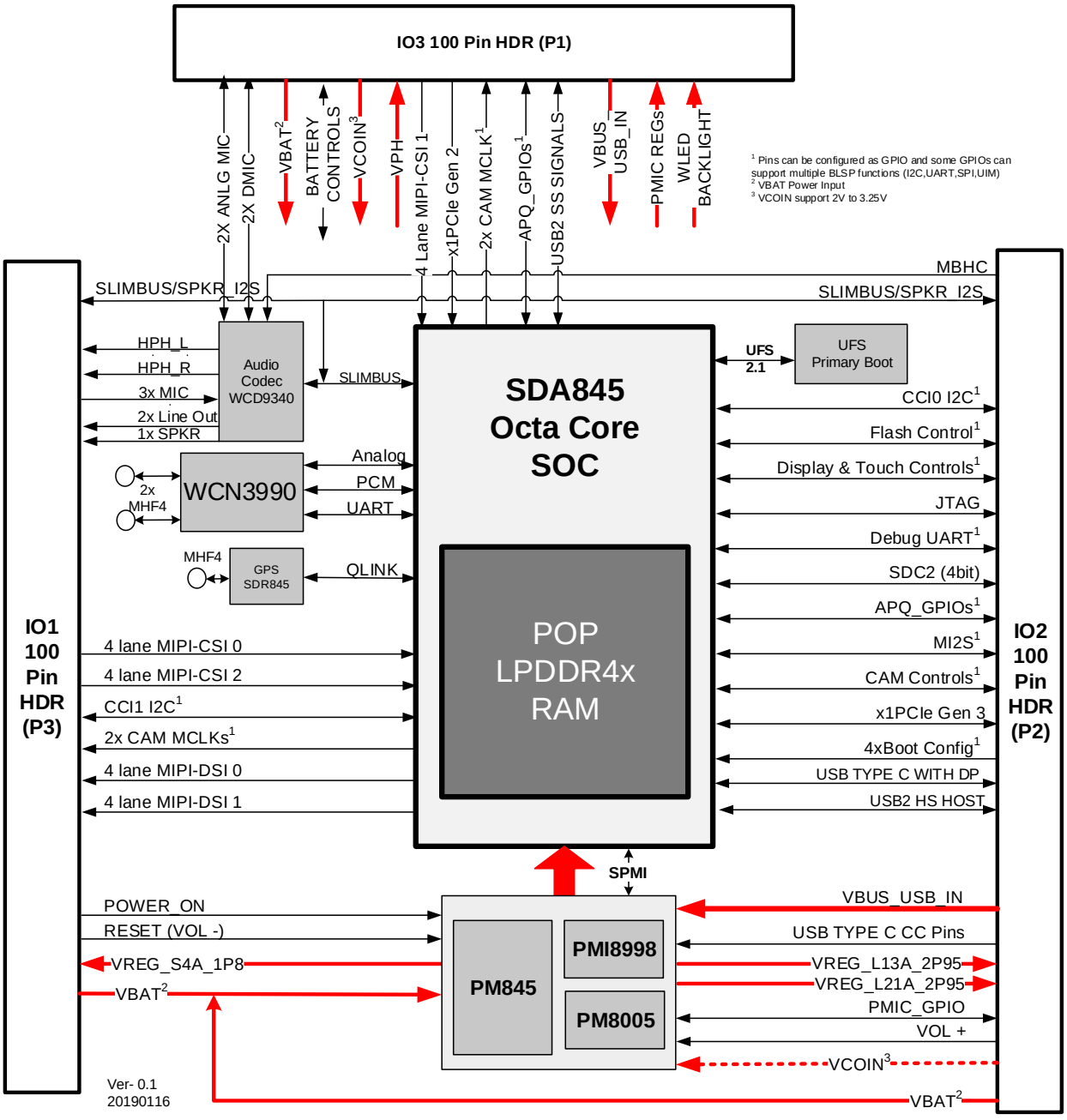
1. *Speaker I2S function multiplexed.*
2. *Pins can have dedicated functions and other multiple functions - GPIO, QUP functions (I2C, UART, SPI),MI2S, Camera Controls, Debug.*

2. HARDWARE SPECIFICATIONS

2.1 ARCHITECTURE

The functional diagram of the Inforce 67X1 SOM is shown below.

Figure 1: Block Diagram



2.1.1 SYSTEM OVERVIEW

The Inforce 67X1 SOM is based on the Qualcomm Octa-core SDA845.

Figure 2: Inforce 67X1 Board (Top Side)

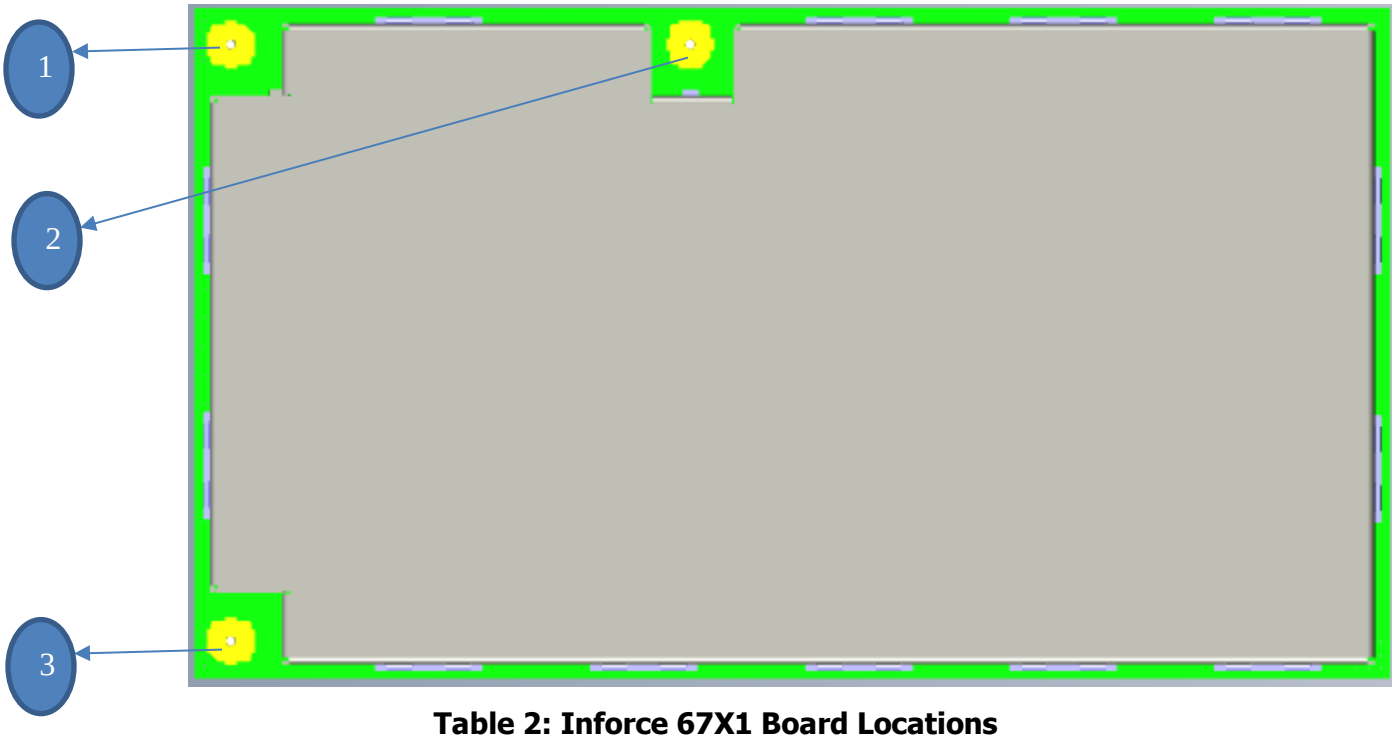
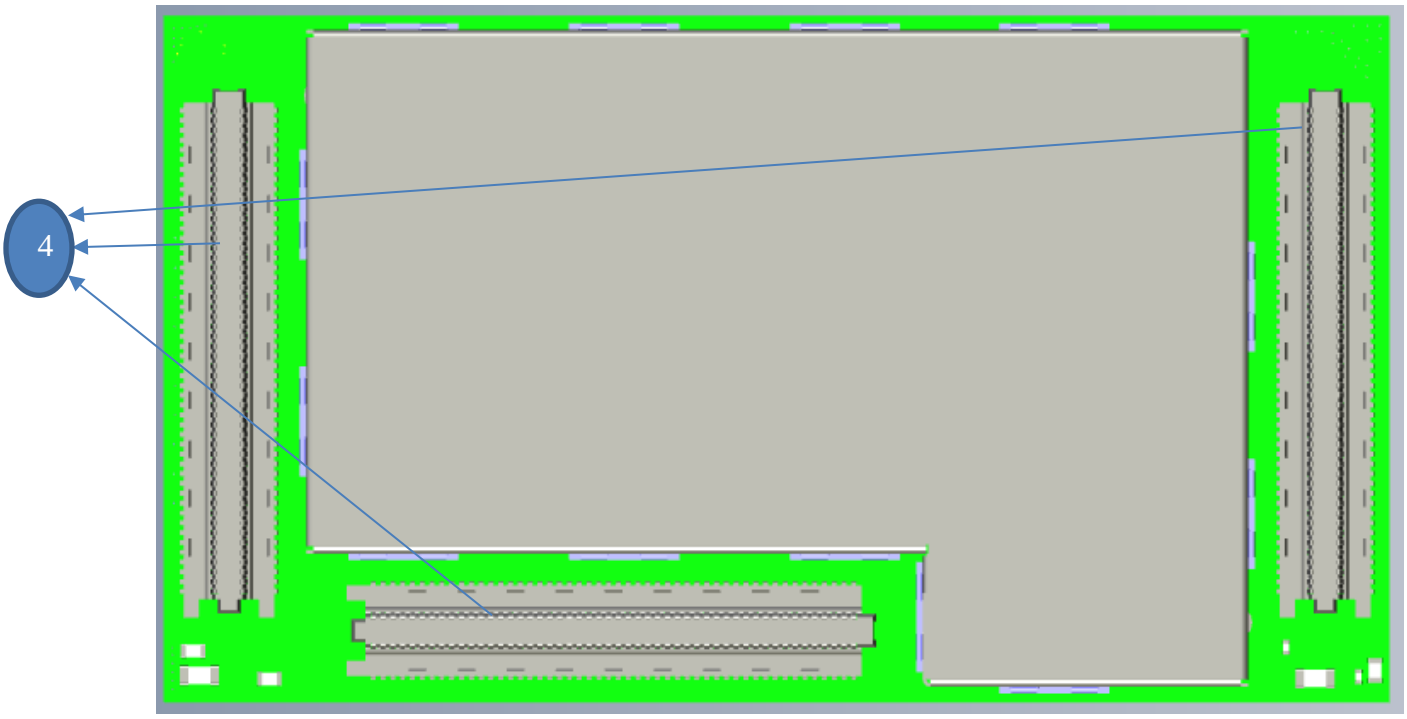


Table 2: Inforce 67X1 Board Locations

1	WIFI/BT connector
2	WIFI connector
3	GPS Connector
4	SOM Connectors

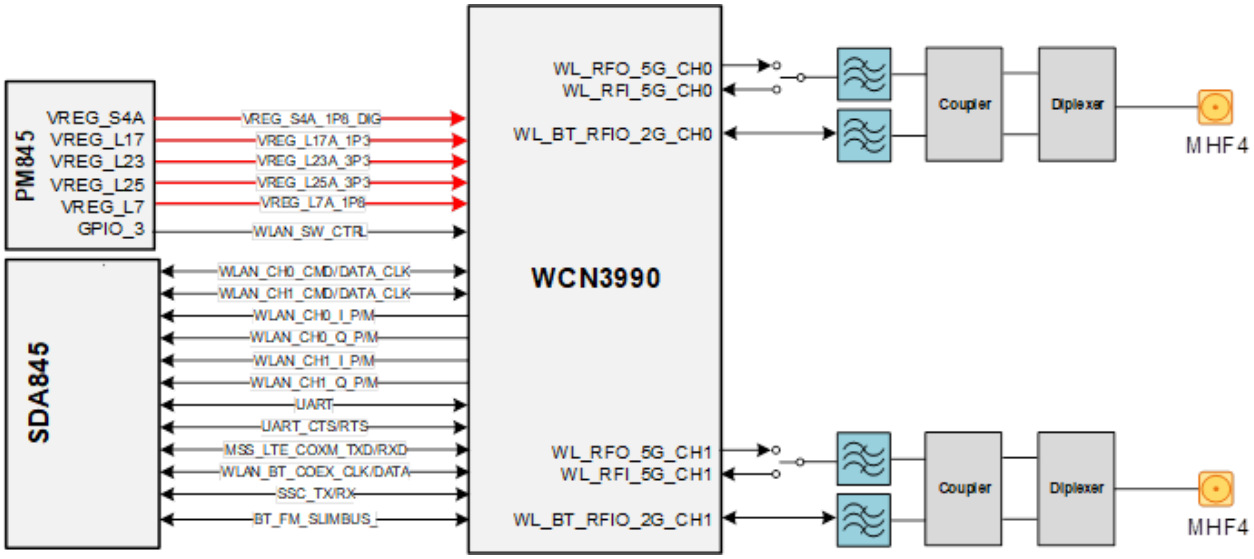
Figure 3: Inforce 67X1 Board (Bottom Side)



2.1.2 WI-FI AND BLUETOOTH INTERFACE

- WCN3990 WiFi/Bluetooth SoC
- WLAN: 802.11ac, MU-MIMO
- 160 MHz & DBS(Dual Band Simultaneous) support
- Support Bluetooth 5.0
- BT audio over SLIMbus
- 2× MHF4 Connector for external antenna

Figure 4: Wi-Fi and Bluetooth Implementation

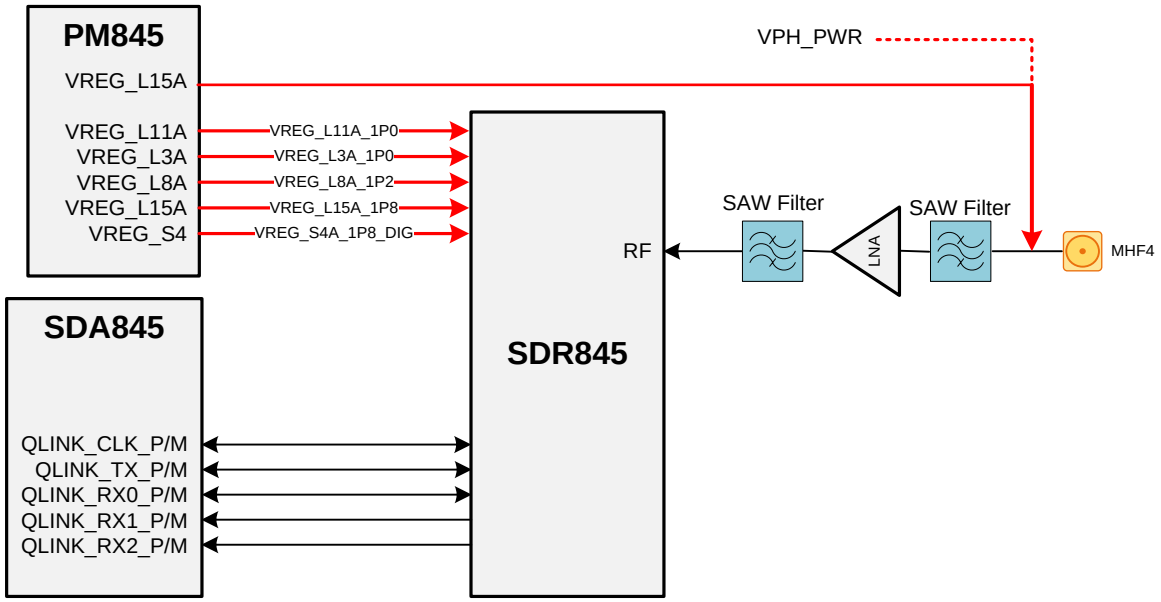


2.1.3 GPS INTERFACE

Support for location via SDR845

- Support GPS, GLONASS, Galileo, BeiDou
- QLINK interface to host
- MHF4 connector for external antenna interface
- Support for external active antenna (default 1.8V power)

Figure 5: GPS

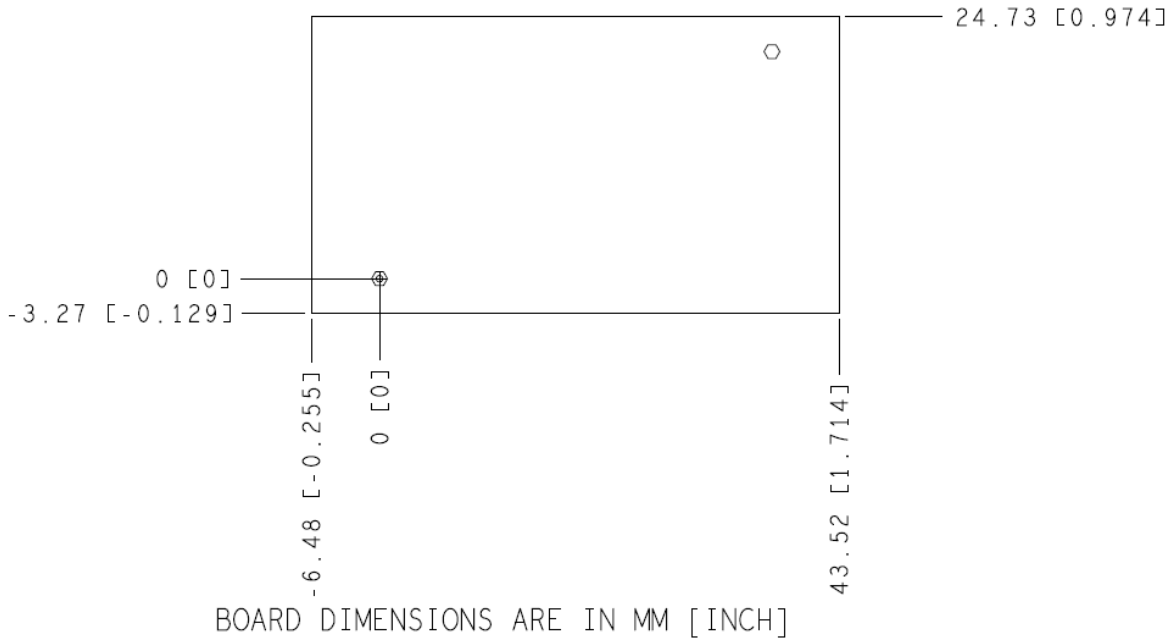


3. MECHANICAL SPECIFICATIONS

3.1 BOARD DIMENSIONS

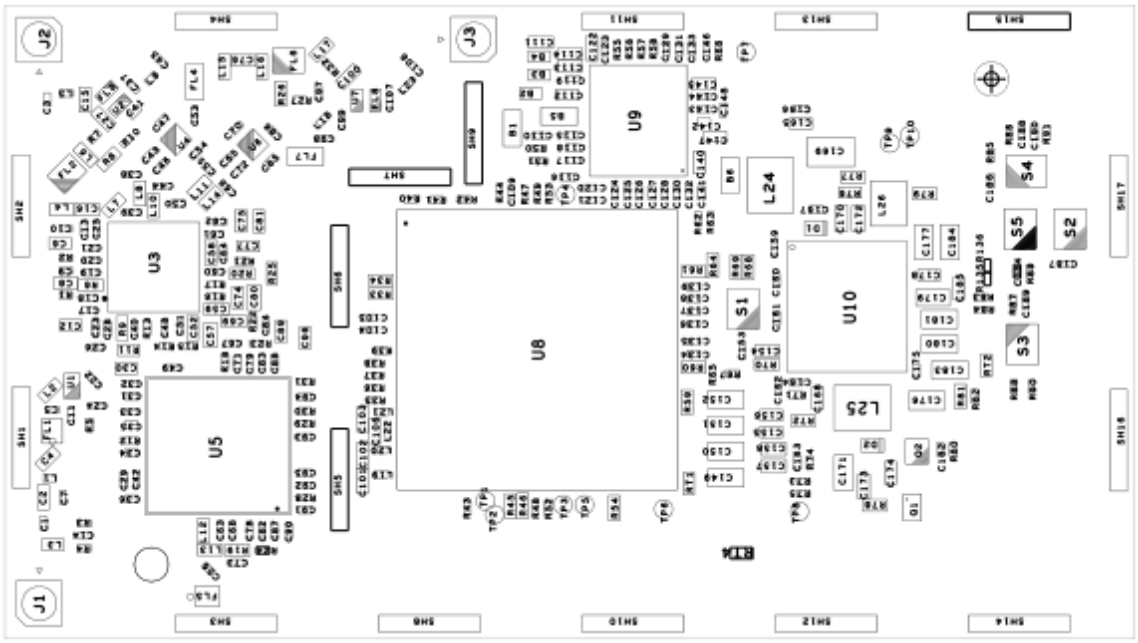
Dimensions : 50 × 28mm
Tolerance : +/-0.2mm
Layers : 10
PCB Thickness : 1mm

Figure 6: Board Dimensions



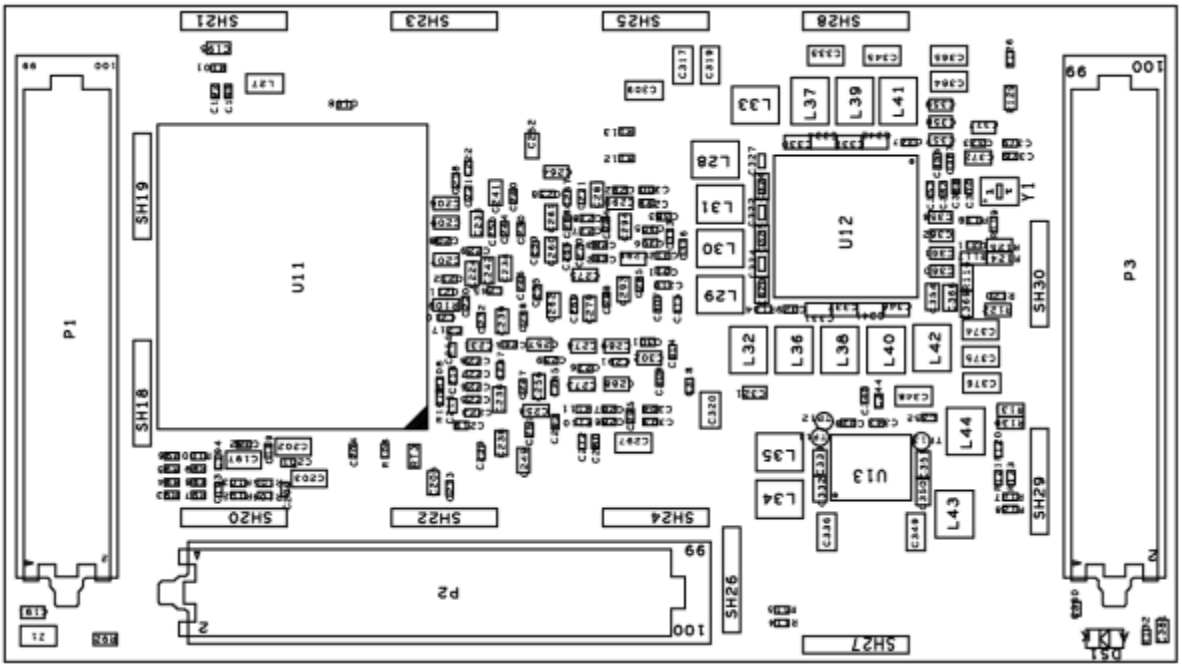
3.2 TOP FLOOR PLAN

Figure 7: Top Floor Plan



3.3 BOTTOM FLOOR PLAN

Figure 8: Bottom Floor Plan



4. USAGE

- Connect SOM on Inforce Development Kit or custom carrier based on the design
- Make sure respective RF antennas are connected as per the hardware reference manual before powering the device

5. APPENDIX A

5.1 SOM CONNECTORS

Manufacturer : Samtec
Manufacturer Part : ST4-50-1.50-L-D-P-TR

Table 3: Connector IO interface 1 Pin out (Ref Des P1)

Pin	Net	Comments	QUP	Pin	Net	Comments	Voltage
1	VBAT	Power input		2	V3V3	Leave as NC	
3	VBAT	Power input		4	VBAT	Power input	
5	CDC_LINE_OUT2_P	Audio		6	CAM_MCLK2		
7	CDC_IN3_P	Audio		8	CODEC_MCLK		
9	CDC_EAR_P	Audio		10	CCI_I2C_SCL1		QUP_L3(1)
11	CDC_EAR_M	Audio		12	CAM_MCLK0		
13	CDC_IN4_P	Audio		14	CCI_I2C_SDA1		QUP_L2(1)
15	CDC_LINE_OUT1_P	Audio		16	GND		
17	SLIMBUS_DATA1_CARRIER			18	MIPI_CSI0_LANE0_N	Camera	
19	GND			20	MIPI_CSI0_LANE0_P	Camera	
21	MIPI_CSI2_LANE3_P	Camera		22	GND	Camera	
23	MIPI_CSI2_LANE3_N	Camera		24	MIPI_CSI0_CLK_N	Camera	
25	GND	Camera		26	MIPI_CSI0_CLK_P	Camera	
27	MIPI_CSI2_LANE2_N	Camera		28	GND	Camera	
29	MIPI_CSI2_LANE2_P	Camera		30	MIPI_CSI0_LANE1_P	Camera	
31	GND	Camera		32	MIPI_CSI0_LANE1_N	Camera	
33	MIPI_CSI2_LANE1_P	Camera		34	GND	Camera	
35	MIPI_CSI2_LANE1_N	Camera		36	MIPI_CSI0_LANE2_N	Camera	
37	GND	Camera		38	MIPI_CSI0_LANE2_P	Camera	
39	MIPI_CSI2_CLK_N	Camera		40	GND	Camera	
41	MIPI_CSI2_CLK_P	Camera		42	MIPI_CSI0_LANE3_N	Camera	
43	GND	Camera		44	MIPI_CSI0_LANE3_P	Camera	
45	MIPI_CSI2_LANE0_N	Camera		46	GND	Camera	
47	MIPI_CSI2_LANE0_P	Camera		48			
49	GND	Camera		50			
51	MIPI_DSI1_LANE3_P	Display		52	GND		
53	MIPI_DSI1_LANE3_N	Display		54			
55	GND	Display		56			
57	MIPI_DSI1_LANE2_P	Display		58	GND		
59	MIPI_DSI1_LANE2_N	Display		60			
61	GND	Display		62			
63	MIPI_DSI1_LANE1_N	Display		64	GND		
65	MIPI_DSI1_LANE1_P	Display		66			
67	GND	Display		68			
69	MIPI_DSI1_LANE0_P	Display		70	GND		
71	MIPI_DSI1_LANE0_N	Display		72	MIPI_DSI0_LANE3_N	Display	
73	GND	Display		74	MIPI_DSI0_LANE3_P	Display	
75	MIPI_DSI1_CLK_N	Display		76	GND	Display	
77	MIPI_DSI1_CLK_P	Display		78	MIPI_DSI0_LANE2_N	Display	
79	GND	Display		80	MIPI_DSI0_LANE2_P	Display	
81	CDC_IN2_P	Mic In		82	GND	Display	
83	CDC_HPH_R	Headphone Out		84	MIPI_DSI0_LANE1_P	Display	
85	CDC_HPH_REF	Headphone Out		86	MIPI_DSI0_LANE1_N	Display	
87	CDC_HPH_L	Headphone Out		88	GND	Display	
89	PHONE_ON_N	Power ON		90	MIPI_DSI0_LANE0_P	Display	
91	PM_RESIN_N	Vol-/ Reset		92	MIPI_DSI0_LANE0_N	Display	
93	APQ_GPIO_93	GPIO	QUP_L0(7)	94	GND	Display	
95	APQ_GPIO_94	GPIO	QUP_L1(7)	96	MIPI_DSI0_CLK_P	Display	
97	VREG_S4A_1P8	1.8V Out		98	MIPI_DSI0_CLK_N	Display	
99	VREG_S4A_1P8	1.8V Out		100	GND	Display	

Table 4: Connector IO interface 2 Pin out (Ref Des P3)

Pin	Net	Comments	QUP	Pin	Net	Comments	Voltage
1	VBAT	Power input		2	VBAT	Power input	
3	VBAT	Power input		4	VBAT	Power input	
5	CAM2_RST_N		QUP_L0(0)	6	FLASH_STROBE_TRIG		
7	CAM0_STANDBY_N			8	WDOG_DISABLE		
9	USB_CC2_R	USB		10	VOL_UP_N		
11	FORCE_USB_BOOT			12	APQ_GPIO_81_OR_82		QUP_L0(15)
13	BOOT_CONFIG_1			14	USB_VBUS		

15	CAM0_RST_N		QUP_L3(0)	16	APQ_GPIO_84_OR_81		QUP_L3(15)
17	FLASH_STROBE_EN			18	APQ_GPIO_82_OR_83		QUP_L1(15)
19	CCI_I2C_SDA0		QUP_L0(1)	20	APQ_GPIO_83_OR_80		QUP_L2(15)
21	CCI_I2C_SCL0		QUP_L1(1)	22	USB_CC1	USB	
23	GND			24		USB	
25	USB1_SS_RX1_M	USB		26	USB_SBU1	USB	
27	USB1_SS_RX1_P	USB		28	USB_SBU2	USB	
29	GND	USB		30	GND	USB	
31	USB1_HS_DP	USB		32	USB1_SS_TX1_M	USB	
33	USB1_HS_DM	USB		34	USB1_SS_TX1_P	USB	
35	GND	USB		36	GND	USB	
37	USB2_HS_DP	USB		38	USB1_SS_RX0_M	USB	
39	USB2_HS_DM	USB		40	USB1_SS_RX0_P	USB	
41	GND	USB		42	GND	USB	
43	TS_I2C_SCL	Touch	QUP_L1(5)	44	USB1_SS_TX0_M	USB	
45	TS_I2C_SDA	Touch	QUP_L0(5)	46	USB1_SS_TX0_P	USB	
47	BACKLIGHT_EN	Backlight Enable Out	QUP_L3(5)	48	APQ_GPIO_31_OR_SSC_0		QUP_L0(11)
49	APQ_GPIO_90		QUP_L1(4)	50	APQ_GPIO_32_OR_SSC_1		QUP_L1(11)
51	TP_INT_N	Touch		52	MSM_RESOUT_N		
53	PMI8998_GPIO_05	PMIC GPIO/PWM Out		54	APQ_GPIO_58		
55	TP_RST_N	Touch	QUP_L2(0)	56	BOOT_CONFIG_2		
57	LCD_RST_N	Display Reset	QUP_L2(5)	58	JTAG_PS_HOLD		
59	APQ_GPIO_89		QUP_L0(4)	60	SD_CARD_DET_N	Sdcard	
61	MSM_UART_TX	Debug UART	QUP_L2(9)	62	VREG_L13A_2P95	Sdcard	
63	MSM_UART_RX	Debug UART	QUP_L3(9)	64	SDC2_DATA2	Sdcard	
65	GND			66	SDC2_DATA1	Sdcard	
67	SLIMBUS_DATA0_CARRIER	Slim Bus		68	SDC2_CLK	Sdcard	
69	SLIMBUS_CLK_CARRIER	Slimbus		70	SDC2_DATA3	Sdcard	
71	GND			72	SDC2_CMD	Sdcard	
73	PCIE1_REFCLK_P	pcie		74	SDC2_DATA0	Sdcard	
75	PCIE1_REFCLK_N	pcie		76	VREG_L21A_2P95	Sdcard	
77	GND	pcie		78	MSM_JTAG_TRST_N	jtag	
79	PCIE1_TX_P	pcie		80	MSM_JTAG_SRST_N	jtag	
81	PCIE1_TX_M	pcie		82	MSM_JTAG_TDO	jtag	
83	GND	pcie		84	MSM_JTAG_TDI	jtag	
85	PCIE1_RX_P	pcie		86	MSM_JTAG_TCK	jtag	
87	PCIE1_RX_M	pcie		88	MSM_JTAG_TMS	jtag	
89	GND	pcie		90	CDC_HSDET_L	Headset Detect	
91	PCIE1_CLKREQ_N	pcie		92	APQ_GPIO_1		QUP_L1(0)
93	PCIE1_WAKE_N	pcie		94	CAM2_STANDBY_N		QUP_L0(2)
95	PCIE1_RST_N	pcie		96	SOM_OPTION	Options (Auto Boot/ Charger Disable)	Leave As NC
97	APQ_GPIO_95		QUP_L2(7)	98	VCOIN_R	Options	
99	APQ_GPIO_96		QUP_L3(7)	100	USB_VBUS_R	Options	

Table 5: Connector IO interface 3 Pin out (Ref Des P2)

Pin	Net	Comments	Voltage
1	GND	PCIE	
3	PCIE0_REFCLK_N	PCIE	
5	PCIE0_REFCLK_P	PCIE	
7	GND	PCIE	
9	PCIE0_RX_M	PCIE	
11	PCIE0_RX_P	PCIE	
13	GND	PCIE	
15	PCIE0_TX_M	PCIE	
17	PCIE0_TX_P	PCIE	
19	GND	PCIE	
21	PCIE0_RST_N	PCIE	
23	PCIE0_CLKREQ_N	PCIE	
25	PCIE0_WAKE_N	PCIE	
27	VCOIN	RTC	
29	WLED_SINK1	Backlight	
31	WLED_SINK2	Backlight	
33	WLED_SINK3	Backlight	
35	WLED_SINK4	Backlight	
37	VREG_WLED	Backlight	
39	VREG_WLED	Backlight	
41	GND	Backlight	
43	CABC	Backlight	
45			
47			
49	VBAT	Power	
51	VBAT	Power	
53	VREG_BOB	LDO	
55	VREG_L16A_2P7	LDO	
57	VREG_L18A_2P7	LDO	
59	VREG_L19A_3P0	LDO	
61	VREG_L19A_3P0	LDO	
63	VREG_L14A_1P8	LDO	
65	VREG_L28A_3P0	LDO	
67	VREG_L22A_2P85	LDO	
69			
71	CDC_IN1_P	Audio	
73	CDC_IN1_M	Audio	
75	MIC_BIAS1	Audio	
77	CDC_IN5_P	Audio	
79	CDC_IN5_M	Audio	
81	CDC_DMIC_CLK1	Audio	
83	CDC_DMIC_DATA1	Audio	
85	CDC_DMIC_CLK2	Audio	
87	CDC_DMIC_DATA2	Audio	
89	GND		
91			
93			
95			
97			
99			

Pin	Net	Comments	Voltage
2	GND	Camera	
4	MIPI_CSI1_CLK_N	Camera	
6	MIPI_CSI1_CLK_P	Camera	
8	GND	Camera	
10	MIPI_CSI1_LANE0_N	Camera	
12	MIPI_CSI1_LANE0_P	Camera	
14	GND	Camera	
16	MIPI_CSI1_LANE1_P	Camera	
18	MIPI_CSI1_LANE1_N	Camera	
20	GND	Camera	
22	MIPI_CSI1_LANE2_N	Camera	
24	MIPI_CSI1_LANE2_P	Camera	
26	GND	Camera	
28	MIPI_CSI1_LANE3_N	Camera	
30	MIPI_CSI1_LANE3_P	Camera	
32	GND	Camera	
34	USB2_SS_RX_M	USB	
36	USB2_SS_RX_P	USB	
38	GND	USB	
40	USB2_SS_TX_M	USB	
42	USB2_SS_TX_P	USB	
44	GND	USB	
46	CAM_MCLK3		
48	CAM_MCLK1		
50	CAM1_STANDBY_N		
52	CAM1_RST_N		QUP_L1(2)
54	GND		
56			
58	USB_VBUS	Power and battery	
60	USB_VBUS	Power and battery	
62	USB_VBUS	Power and battery	
64	VBAT	Power and battery	
66	VBAT	Power and battery	
68	GND	Power and battery	
70	VPH_PWR	Power and battery	
72	VPH_PWR	Power and battery	
74	VPH_PWR	Power and battery	
76	BATT_THERM	Power and battery	
78	BATT_ID	Power and battery	
80	VBATT_CONN_VSENSE_M	Power and battery	
82	VBATT_CONN_VSENSE_P	Power and battery	
84	MIC_BIAS3		
86	MIC_BIAS4		
88	GND		
90			
92			
94			
96			
98			
100			

5.2 IO CONNECTOR GPIOS

- Refer processor datasheet for more details

Table 6: IO CONNECTOR GPIOs

IO interface	pin	Net Name	Comments	QUP	QUP Number	GPIO	I2X/UART	Wake Capable
2	5	CAM2_RST_N		QUP_L0(0)	0	GPIO_0	I2C	
2	92	APQ_GPIO_1		QUP_L1(0)	0	GPIO_1	I2C	Y
2	55	TP_RST_N		QUP_L2(0)	0	GPIO_2	UART	
2	15	CAM0_RST_N		QUP_L3(0)	0	GPIO_3	UART	Y
2	19	CCI_I2C_SDA0		QUP_L0(1)	1	GPIO_17	I2C	
2	21	CCI_I2C_SCL0		QUP_L1(1)	1	GPIO_18	I2C	
1	14	CCI_I2C_SDA1		QUP_L2(1)	1	GPIO_19	UART	
1	10	CCI_I2C_SCL1		QUP_L3(1)	1	GPIO_20	UART	Y
2	94	CAM2_STANDBY_N		QUP_L0(2)	2	GPIO_27	I2C	
3	52	CAM1_RST_N		QUP_L1(2)	2	GPIO_28	I2C	
2	59	APQ_GPIO_89		QUP_L0(4)	4	GPIO_89	I2C	Y
2	49	APQ_GPIO_90		QUP_L1(4)	4	GPIO_90	I2C	
2	45	TS_I2C_SDA		QUP_L0(5)	5	GPIO_85	I2C	Y
2	43	TS_I2C_SCL		QUP_L1(5)	5	GPIO_86	I2C	Y
2	57	LCD_RST_N		QUP_L2(5)	5	GPIO_87	UART	
2	47	BACKLIGHT_EN		QUP_L3(5)	5	GPIO_88	UART	
1	93	APQ_GPIO_93		QUP_L0(7)	7	GPIO_93	I2C	Y
1	95	APQ_GPIO_94		QUP_L1(7)	7	GPIO_94	I2C	
2	97	APQ_GPIO_95		QUP_L2(7)	7	GPIO_95	UART	Y
2	99	APQ_GPIO_96		QUP_L3(7)	7	GPIO_96	UART	Y
2	61	MSM_UART_TX		QUP_L2(9)	9	GPIO_4	UART-Debug	Y
2	63	MSM_UART_RX		QUP_L3(9)	9	GPIO_5	UART-Debug	
2	48	APQ_GPIO_31_OR_SSC_0		QUP_L0(11)	11	GPIO_31	I2C/UART/SSC i2c	
2	50	APQ_GPIO_32_OR_SSC_1		QUP_L1(11)	11	GPIO_32	I2C/UART/SSC i2c	
2	12	APQ_GPIO_81_OR_82	MI2S_DATA0	QUP_L0(15)	15	GPIO_81	I2C/MI2S	Y
2	18	APQ_GPIO_82_OR_83	MI2S_DATA1	QUP_L1(15)	15	GPIO_82	I2C/MI2S	Y
2	20	APQ_GPIO_83_OR_80	MI2S_SCK	QUP_L2(15)	15	GPIO_83	UART/MI2S	
2	16	APQ_GPIO_84_OR_81	MI2S_WS	QUP_L3(15)	15	GPIO_84	UART/MI2S	
2	54	APQ_GPIO_58				GPIO_58		
2	13	BOOT_CONFIG_1				GPIO_99		
2	56	BOOT_CONFIG_2				GPIO_100		
1	12	CAM_MCLK0				GPIO_13		
3	48	CAM_MCLK1				GPIO_14		
1	6	CAM_MCLK2				GPIO_15		
3	46	CAM_MCLK3				GPIO_16		
2	7	CAM0_STANDBY_N				GPIO_79		Y
3	50	CAM1_STANDBY_N				GPIO_8		
1	8	CODEC_MCLK				GPIO_69		
2	17	FLASH_STROBE_EN				GPIO_21		
2	6	FLASH_STROBE_TRIG				GPIO_24		Y
2	11	FORCE_USB_BOOT				GPIO_57		Y
3	23	PCIE0_CLKREQ_N	PCIE			GPIO_36		Y
3	21	PCIE0_RST_N	PCIE			GPIO_35		
3	25	PCIE0_WAKE_N	PCIE			GPIO_37		Y
2	91	PCIE1_CLKREQ_N	pcie			GPIO_103		Y
2	95	PCIE1_RST_N	pcie			GPIO_102		
2	93	PCIE1_WAKE_N	pcie			GPIO_104		Y
2	53	PMI8998_GPIO_05				PMI8998_GPIO_05		
2	60	SD_CARD_DET_N	Sdcard			GPIO_126		Y
2	51	TP_INT_N				GPIO_125		Y
2	8	WDOG_DISABLE				GPIO_101		Y

5.3 ELECTRICAL SPECIFICATIONS OF PINS

Table 7: IO CONNECTOR Power specifications

Voltage rail	Min V	Typical V	Max V
VBAT	3.2	3.8V	4.5
1.8V Out	1.7	1.8	1.9
SDCard Power	2.7	2.95	3.6
SDC2 IO	1.7/2.7	1.8/2.95	1.9/3.04
VCOIN	2	3	3.25
USB_VBUS	3.6	5	13.2

Table 8: IO specifications

1.8V GPIO	Min V	Typical V	Max V
VIH	1.26	-	2.1
VIL	-0.3	-	0.54
VOH	1.35	-	1.8
VOL	0	-	0.45
SDCard IO 2.95V	**Min V**	**Typical V**	**Max V**
VIH	1.84	-	3.25
VIL	-0.3	-	0.735
VOH	2.21	-	2.95
VOL	0	-	0.36
SDCard IO 1.8V	**Min V**	**Typical V**	**Max V**
VIH	1.27	-	2
VIL	-0.3	-	0.58
VOH	1.4	-	-
VOL	-	-	0.45

5.4 RF CONNECTORS

Manufacturer : Murata

Manufacturer Part : MM4829-2702RB0

Description : MHF4 Coaxial RF connector

Functions : GPS, WiFi, Bluetooth

CAUTION

Make sure that RF cable crimps are not touching any components nearby after assembled.

6. COMPLIANCE INFORMATION

6.1 FCC COMPLIANCE STATEMENT

a. "This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation."

"Warning: Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment."

6.2 EU COMPLIANCE STATEMENT

1) The IFC67X1 complies with the essential requirements and other relevant provisions of the RE Directive 2014/53/EU.
2) This device is restricted to indoor use only when operating in the 5150 to 5350 MHz frequency range.
3) A minimum separation distance 20cm is required.

6.3 THE (A) FREQUENCY BAND(S) IN WHICH THE RADIO EQUIPMENT OPERATES AND (B) MAXIMUM RADIO FREQUENCY POWER TRANSMITTED IN THE FREQUENCY BAND(S) IN WHICH THE RADIO EQUIPMENT OPERATES.

WIFI 2.4GHz:	20MHz: 2412MHz – 2472MHz, < 20 dBm EIRP 40MHz: 2422MHz – 2462MHz, < 20 dBm EIRP
WIFI 5GHz:	5150MHz – 5250MHz, 5250MHz – 5350MHz: 20MHz: < 20 dBm EIRP 40MHz: < 20 dBm EIRP 80MHz: < 20 dBm EIRP 80MHz + 80MHz: < 20 dBm EIRP 5470MHz – 5725MHz: 20MHz: < 20 dBm EIRP 40MHz: < 20 dBm EIRP 80MHz: < 20 dBm EIRP 80MHz + 80MHz: < 20 dBm EIRP
Bluetooth Classic:	2402MHz – 2480MHz, 7.80dBm EIRP
BLE:	2402MHz – 2480MHz, 4.79dBm EIRP
GNSS:	1559MHz – 1610MHz

6.4 FCC RADIATION EXPOSURE STATEMENT

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20cm between the radiator & your body.

7. JAPAN WARNING STATEMENT

a. Please add below warning text:

5.2 GHz帯域は屋内での使用のみに制限されています

（5.2 GHz高電力基地局または中継局と通信する場合を除く）

電波法により5.3 GHz帯は屋内使用に限ります

Translation: 5.2 GHz band is restricted to indoor use only

(Except when communicating with 5.2GHz high power base stations or relay stations)

5.3 GHz band is restricted to indoor use due to the Radio Law

b. A minimum separation distance 20cm is required.

8. CONTACT INFORMATION

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