MD-5XR

(MD-5XRAH33)

Application Note

Module Features

-Bluetooth system v3.0+EDR, 2.1+EDR, 2.0+EDR Compliant

-Class 2 Level Output Power Available

-UART Bypass Mode Support

-Scatternet Support

-Support of all Bluetooth packet types (voice and data)

-Support of low power modes: Park, Sniff and Hold

-UART, USB and PCM Interface Available

-Built-in Reference Clock: 26MHz

-High performance Stereo Codec

(Default : SBC, applicable : apt-X, AAC, MP3)

-16Mbits Flash Memory

-Enhanced Audibility and Noise Cancellation

-RoHS Compliant

Applications

-High Quality Stereo Wireless Headsets

-Hands-Free Car Kits

-Wireless Speakers

-Analogue and USB Multimedia Dongles

-Bluetooth-Enabled Automotive wireless Gateways.

Features

-Size (12.0 X 20.0 X 2.3 mm)

-Class2 Support

-Surface Mountable

-1.8V Power Supply for core

-3.3V Power Supply for Memory, USB, UART, GPIO

-Not built-in Antenna (Antenna gain: 0dBi)

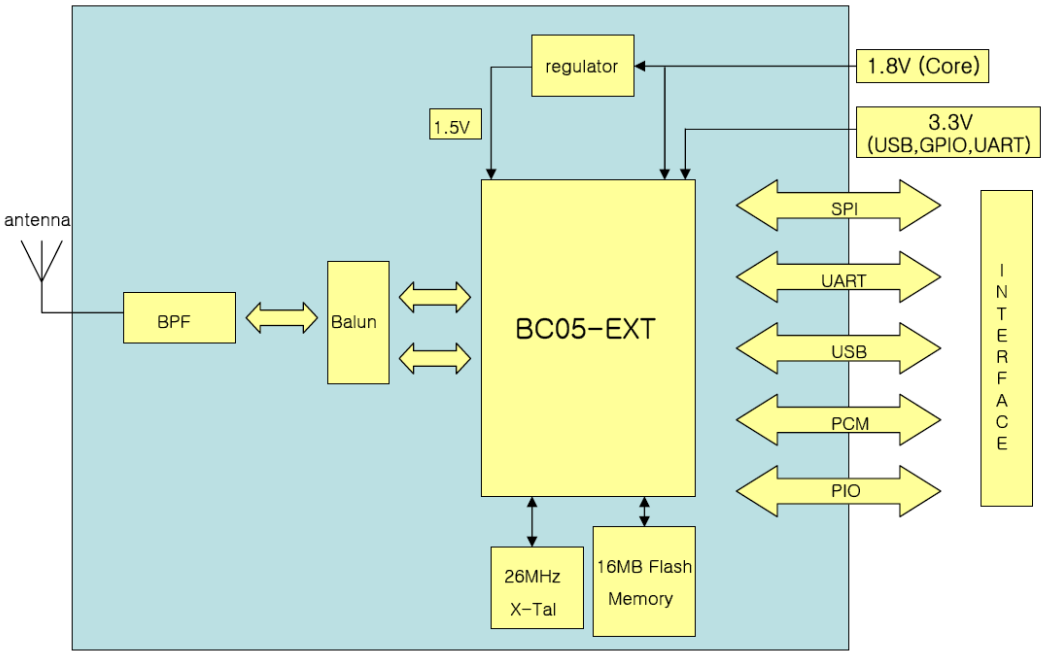
※ Caution

1. POP Noise issue 발생 시 당사에서 지원이 불가능하기 때문에 I2S Audio 출력을 권장합니다.
2. If bag is opened and a module is not reflowed within 168 hours, then you must bake modules as below

- Module with Reel Packing : 45℃/ 12hours

- Module out of Reel Packing : 125℃/ 2hours

Overview



1. Electrical Characteristics

Absolute Maximum Ratings			
Parameter	**Min**	**Max**	**Unit**
Storage Temperature	-40	+85	°C
VCC	-0.4	2.7	V
VDD_USB	-0.4	3.6	V
Other Pin Voltage	VSS-0.4	VDD_USB+0.4	V

Recommended Operating Conditions				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Operating Temperature	-40	/	+85	°C
Humidity	/	+85	/	%
VCC	1.7	1.8	1.95	V
VDD_USB	3.0	3.3	3.6	V

Power Consumption (+25℃)						
Parameter			**Min**	**Typ**	**Max**	**Unit**
Current	Discoverable	VCC	/	3.328	37.760	mA
		VDD_USB	/	0.590	2.600	mA
	Stand-by	VCC	/	3.071	8.995	mA
		VDD_USB	/	0.591	2.720	mA
	HFP (with Alango)	VCC	/	43.992	51.400	mA
		VDD_USB	/	8.314	8.830	mA
	A2DP	VCC	/	33.299	41.400	mA
		VDD_USB	/	0.591	8.650	mA

2. RF specification

Transmitter Performance					
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Output Power	Normal/extreme test	-6	0	5	dBm
Power Density	Normal/extreme test	-	-	20	dBm
Power Control	Normal/extreme test				
Frequency Range	Normal/extreme test	2402	-	2480	MHz
20dB Bandwidth	Normal/extreme test	-	850	1000	KHz
Adjacent channel power	±2MHz	-	-	-20	dBm
	±3MHz	-	-	-40	dBm
	±4MHz	-	-	-40	dBm
Modulation Characteristics	ΔF1avg	140	-	175	KHz
	ΔF2max	115	-	-	KHz
	ΔF2avg/ΔF1avg	-	-	80	%
Initial Carrier Frequency Tolerance		-75	-	75	KHz
Carrier Frequency Drift	One slot Packet(DH1)	-25	-	25	KHz
	Three slot Packet(DH3)	-40	-	40	KHz
	Five slot Packet(DH5)	-40	-	40	KHz
Transceiver Performance					
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Out-of Band spurious Emissions	30MHz-1GHz	-	-	-36	dBm
	1GHz-12.75GHz	-	-	-30	dBm
	1.8GHz-5.3GHz	-	-	-47	dBm
	5.1GHz-5.3GHz	-	-	-47	dBm
Receiver Performance					
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Unit**
Sensitivity level	Single slot packets	-70	-83	-	dBm
Sensitivity level	Multi slot packets	-70	-	-	dBm
C/I performance	C/I co-channel	-	9	11	dB
	$C/I_{1MHz(adjacent\ channel)}$		-2	0	dB
	$C/I_{2MHz(2nd\ Adjacent\ channel)}$		-34	-30	dB
	$C/I_{\geq 3MHz(3^{rd}adiacentchannel)}$		-43	-40	dB
Blocking performance	30MHz-2000MHz	-10	-	-	dBm
	2000MHz-2400MHz	-27	-	-	dBm
	2500MHz-3000MHz	-27	-	-	dBm

	3000MHz-12.75MHz	-10	-	-	dBm
Intermodulation Performance	N=5	-39	-	-	dBm
Maximum Input Level		-20	-5	-	dBm

3. Pin Description

PIO No.	Pin Name	Description	Pad Type
1	PIO_11	Programmable input/output line	Bi-directional
2	PIO_12	Programmable input/output line	Bi-directional
3	PIO_13	Programmable input/output line	Bi-directional
4	PIO_14	Programmable input/output line	Bi-directional
5	USB_DP	USB Data Plus with selectable internal 1.5KΩ Pull-up resistor	Bi-directional
6	USB_DN	USB Data minus	Bi-directional
7	VDD_USB	POWER FOR USB(3.3V)	Power
8	UART_RTS	UART request to send to active low	Bi-directional
9	UART_CTS	UART request to clear to active low	CMOS Input
10	UART_TX	UART Data Output	Bi-directional
11	UART_RX	UART Data Input	CMOS input
12	PIO_10	Programmable input/output line	Bi-directional
13	PIO_9	Programmable input/output line	CMOS Output
14	PIO_8	Programmable input/output line	CMOS Input
15	PIO_7	Programmable input/output line	Bi-directional
16	VSS	Common Ground	Ground
17	PIO_6	Programmable input/output line	Bi-directional
18	PIO_5	Programmable input/output line	Bi-directional
19	PIO_4	Programmable input/output line	Bi-directional
20	PIO_3	Programmable input/output line	Bi-directional
21	SPI_MOSI	SPI data input	CMOS input
22	SPI_CLK	SPI clock	Input
23	SPI_CSB	Chip select for SPI, active low	Input
24	SPI_MISO	SPI data output	CMOS output
25	LED_1	LED driver	Open drain
26	LED_0	LED driver	Open drain
27	PCM_CLK	Synchronous data clock	Bi-directional
28	PCM_SYNC	Synchronous data sync	Bi-directional

29	PCM_IN	Synchronous data input	CMOS Input
30	PCM_OUT	Synchronous data output	CMOS output
31	VBAT	Battery Power	Power
32	PIO_2	Programmable input/output line	Bi-directional
33	PIO_1	Programmable input/output line	Bi-directional
34	PIO_0	Programmable input/output line	Bi-directional
35	VCHG	Charging Power	Power
36	VCC	Core Power(1.8V)	Power
37	MIC_BIAS	Microphone bias	Power
38	MIC_B_P	Microphone input positive, right	Analogue
39	MIC_B_N	Microphone input negative, right	Analogue
40	MIC_A_P	Microphone input positive, left	Analogue
41	MIC_A_N	Microphone input negative, left	Analogue
42	SPKR_B_N	Speaker output negative, right	Analogue
43	SPKR_B_P	Speaker output positive, right	Analogue
44	SPKR_A_N	Speaker output negative, left	Analogue
45	SPKR_A_P	Speaker output positive, left	Analogue
46	VSS	Common Ground	Ground
47	RF	RF connection to Antenna	Bi-directional
48	VSS	Common Ground	Ground
49	AIO_1	Analogue programmable in/out line	Bi-directional
50	AIO_0	Analogue programmable in/out line	Bi-directional
51	RST#	Reset if low. Input debounced so must be low for>5ms to cause a reset	CMOS Input
52	VSS	Common Ground	Ground

*** If you want to use the MIC_BIAS of module, connect VBAT(31) to 3.3V.**
(MIC_BIAS Voltage range: 1.7 ~ 3.3V)
But we don't recommend using the Internal MIC_BIAS because of noise issue.

*** VCHG(35) pin can't be used.**

4. UART Interface

This is a standard UART interface for communicating with other serial devices.

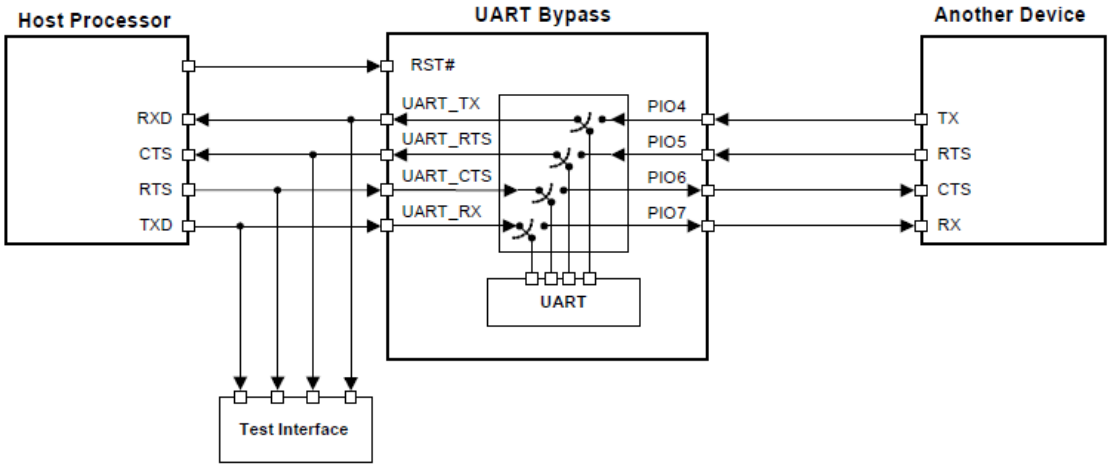
MD-5XR UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

UART configuration parameters, such as baud rate and packet format, are set using MD-5XR firmware.

Parameter		Possible Values
Data Rate	Minimum	1200 bits/s (≤2%Error)
		9600 bits/s (≤1%Error)
	Maximum	3M bit/s (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Channel		8

4.1 UART Bypass Mode

To apply the UART bypass mode, a BCCMD command is issued to MD-5XR. Upon this issue, it switches the bypass to PIO[7:4] as shown in figure. When the bypass mode has been invoked, MD-5XR enters the Deep Sleep state indefinitely.



5. USB Interface

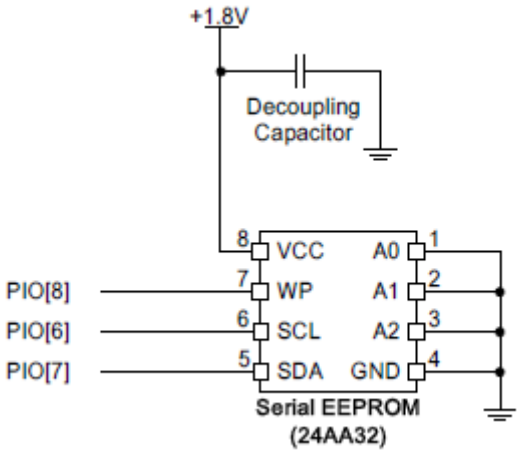
This is a full speed (12Mbits/s) USB interface for communicating with other compatible digital devices. MD-5XR acts as a USB peripheral, responding to requests from a master host controller such as a PC.

The USB interface is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported.

As USB is a master/slave oriented system (in common with other USB peripherals), MD-5XR only supports USB Slave operation.

6. I2C Interface

PIO[8:6] can be used to form a Master I2C interface. The interface is formed using software to drive these lines. Therefore it is suited only to relatively slow functions such as driving a dot matrix LCD, keyboard scanner or EEPROM.



<Example Connection>

7. PCM Interface

The audio PCM interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.

PCM is a standard method used to digitize audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, MD-5XR has hardware support for continual transmission and reception of PCM data, so reducing processor overhead. MD-5XR offers a bi-directional digital audio interface that route directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Parameter	Possible Value
Mode	Slave, Master
Clock	Master Mode : 128/256/512/1536/2400 KHz Slave Mode : up to 2400KHz
Sync	Master Mode : 8 / 48kHz Slave Mode : 8 / 48kHz
Sync format	Long frame sync, Short frame sync

8. Audio Interface

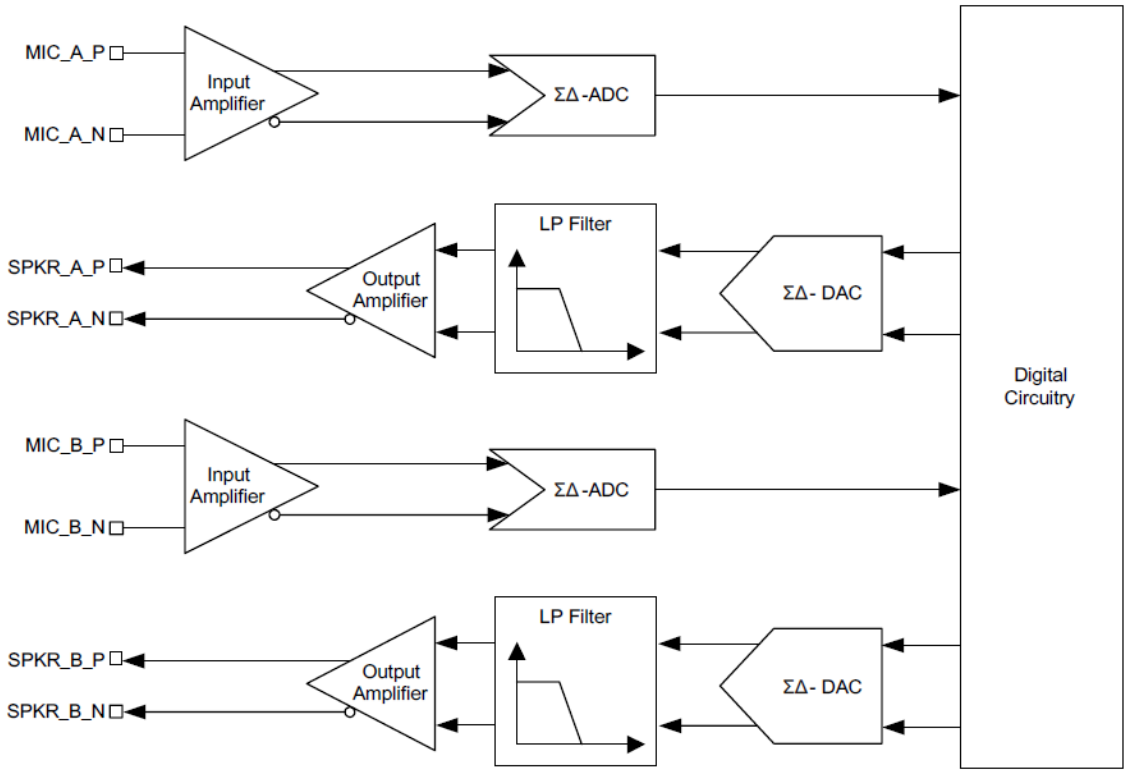
The audio interface circuit consists of:

- Stereo audio codec
- Dual audio inputs and outputs
- A configurable PCM, I2S or SPDIF interface

8.1 Audio Input Output

The audio input circuitry consists of a dual audio input that can be configured to be either single-ended or fully differential and programmed for either microphone or line input. It has an analogue and digital programmable gain stage for optimization of different microphones.
The audio output circuitry consists of a dual differential class A-B output stage.

8.2 Stereo Audio Codec Interface



The Stereo audio codec uses a fully differential architecture in the analogue signal path, which results in low noise sensitivity and good power supply rejection while effectively doubling the signal amplitude.

The ADC consists of:

- Two second-order Sigma Delta converters allowing two separate channels that are identical in functionality.
- Two gain stages for each channel, one of which is an analogue gain stage and the other is a digital gain stage.

Each ADC supports the following sample rates:

■ 8kHz ■ 11.025kHz ■ 16kHz ■ 22.05kHz ■ 24kHz ■ 32kHz ■ 44.1kHz

The DAC consists of:

- Two second-order Sigma Delta converters allowing two separate channels that are identical in functionality.
- Two gain stages for each channel, one of which is an analogue gain stage and the other is a digital gain stage.

Each DAC supports the following samples rates:

■ 8kHz ■ 11.025kHz ■ 12kHz ■ 16kHz ■ 22.050kHz ■ 24kHz ■ 32kHz
■ 44.1kHz ■ 48kHz

8.3 Digital Audio Interface (I^2S)

The digital audio interface supports the industry standard formats for I2S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage.

The digital audio interface supports the industry standard formats for I2S, left-justified or right-justified. The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage.

Table 8.3.1 lists these alternative functions. Figure 8.3.1 shows the timing diagram.

PCM Interface	I2S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

Table 8.3.1 Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

Table 8.3.2 describes the values for the PS Key (PSKEY_DIGITAL_AUDIO_CONFIG) that is used to set-up the digital audio interface. For example, to configure an I2S interface with 16-bit SD data set PSKEY_DIGITAL_CONFIG to 0x0406.

Bit	Mask	Name	Description
D[0]	0x0001	CONFIG_JUSTIFY_FORMAT	0 for left justified, 1 for right justified.
D[1]	0x0002	CONFIG_LEFT_JUSTIFY_DELAY	For left justified formats: 0 is MSB of SD data occurs in the first SCLK period following WS transition. 1 is MSB of SD data occurs in the second SCLK period.
D[2]	0x0004	CONFIG_CHANNEL_POLARITY	For 0, SD data is left channel when WS is high. For 1 SD data is right channel.
D[3]	0x0008	CONFIG_AUDIO_ATTEN_EN	For 0, 17 bit SD data is rounded down to 16 bits. For 1, the audio attenuation defined in CONFIG_AUDIO_ATTEN is applied over 24 bits with saturated rounding. Requires CONFIG_16_BIT_CROP_EN to be 0.
D[7:4]	0x00F0	CONFIG_AUDIO_ATTEN	Attenuation in 6 dB steps.
D[9:8]	0x0300	CONFIG_JUSTIFY_RESOLUTION	Resolution of data on SD_IN, 00=16 bit, 01=20 bit, 10=24 bit, 11=Reserved. This is required for right justified format and with left justified LSB first.
D[10]	0x0400	CONFIG_16_BIT_CROP_EN	For 0, 17 bit SD_IN data is rounded down to 16 bits. For 1 only the most significant 16 bits of data are received.

Table 8.3.2 PSKEY_DIGITAL_AUDIO_CONFIG

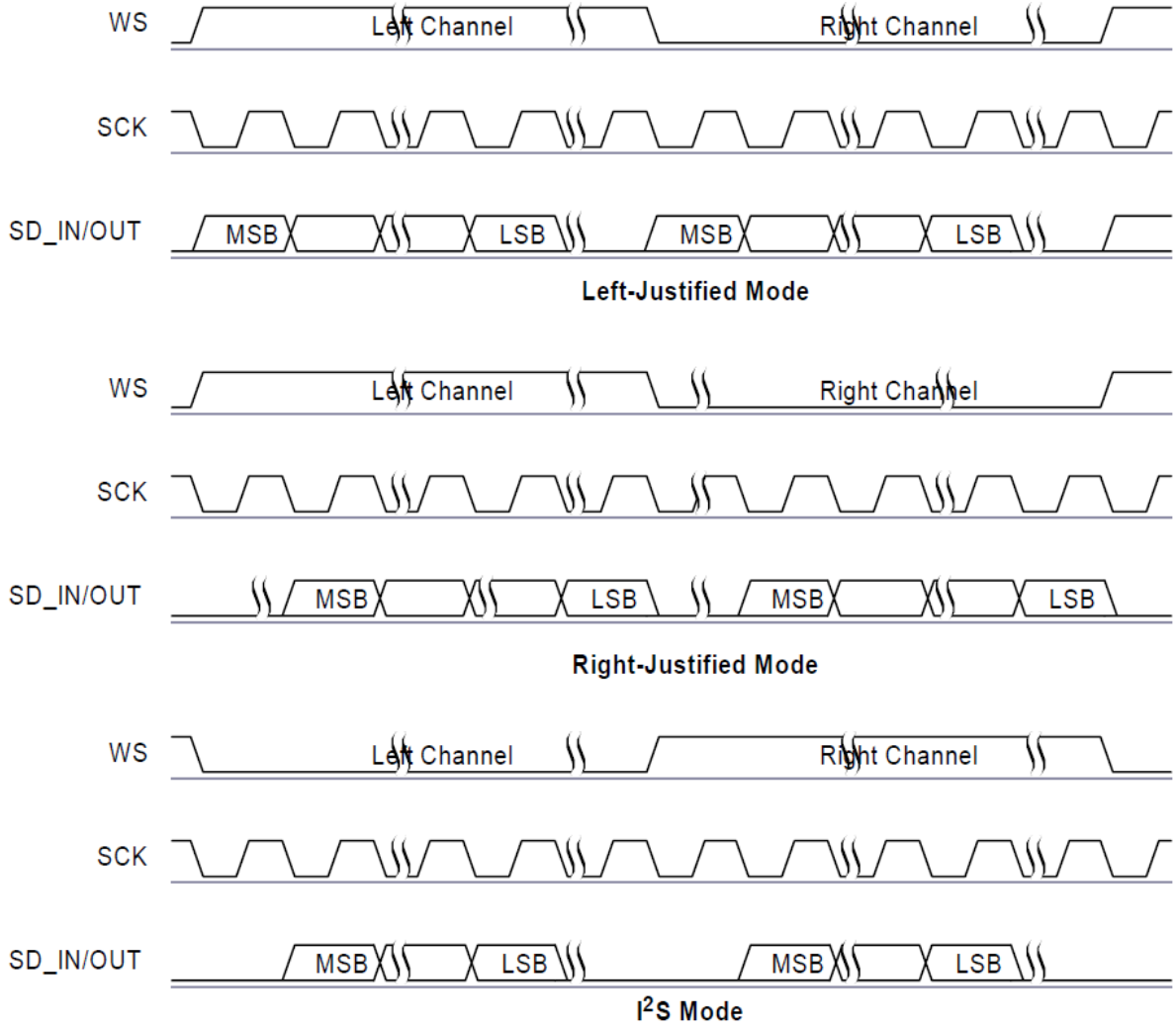


Figure 8.3.1: Digital Audio Interface Modes

The internal representation of audio samples within MD-5XR is 16-bit and data on SD_OUT is limited to 16-bit per channel.

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{ch}	SCK high time	80	-	-	ns
t_{cl}	SCK low time	80	-	-	ns
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{ssu}	WS to SCK set-up time	20	-	-	ns
t_{sh}	WS to SCK hold time	20	-	-	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	20	-	-	ns

Table 8.3.3: Digital Audio Interface Slave Timing

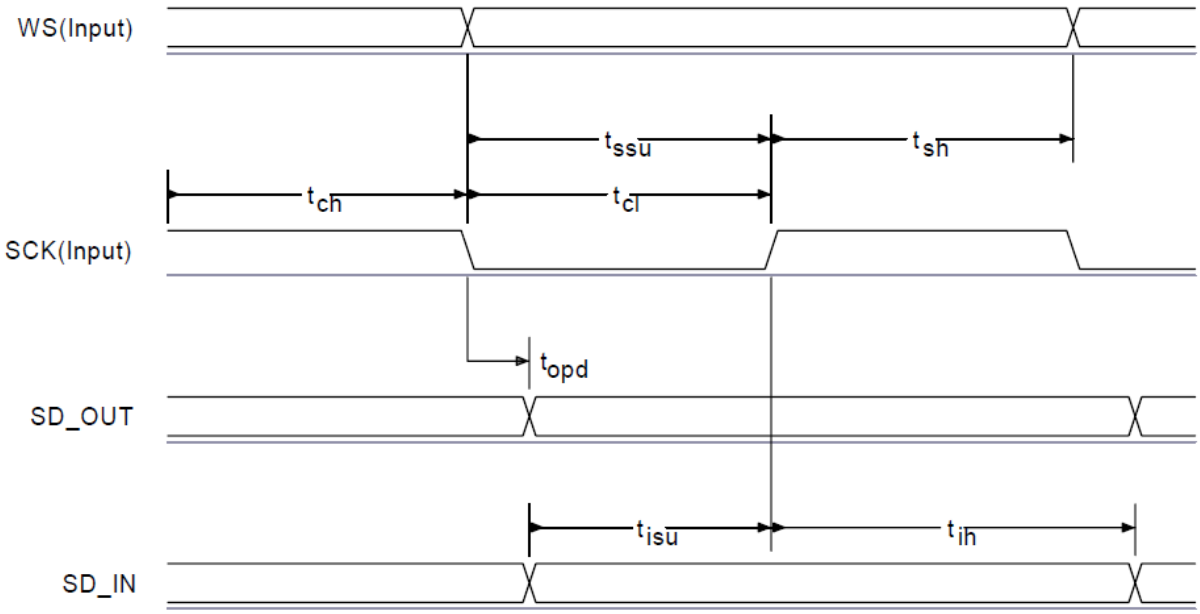


Figure 8.3.2: Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typ	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{spd}	SCK to WS delay	-	-	20	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	10	-	-	ns

Table 8.3.4: Digital Audio Interface Master Timing

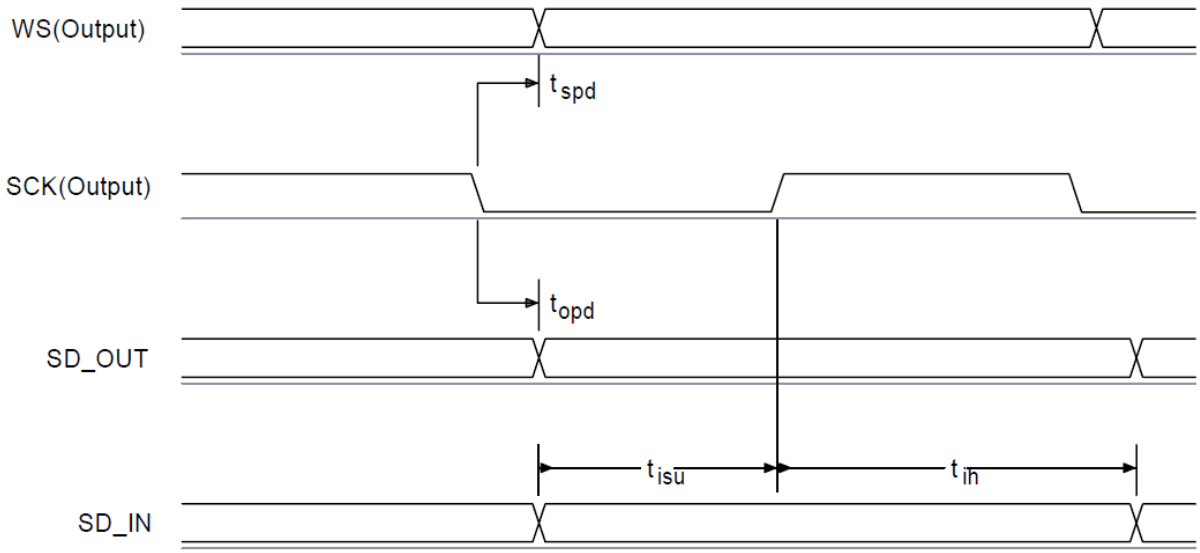


Figure 8.3.3: Digital Audio Interface Master Timing

8.4 SPDIF(IEC 60958) Interface

The SPDIF interface signals are SPDIF_IN and SPDIF_OUT and are shared on the PCM interface pins. The input and output stages of the SPDIF pins can interface to:

- A 75Ω coaxial cable with an RCA connector (Figure 8.4.1)
- An optical link that uses Toslink optical components (Figure 8.4.2)

PCM Interface	SPDIF Interface
PCM_OUT	SPDIF_OUT
PCM_IN	SPDIF_IN
PCM_SYNC	
PCM_CLK	

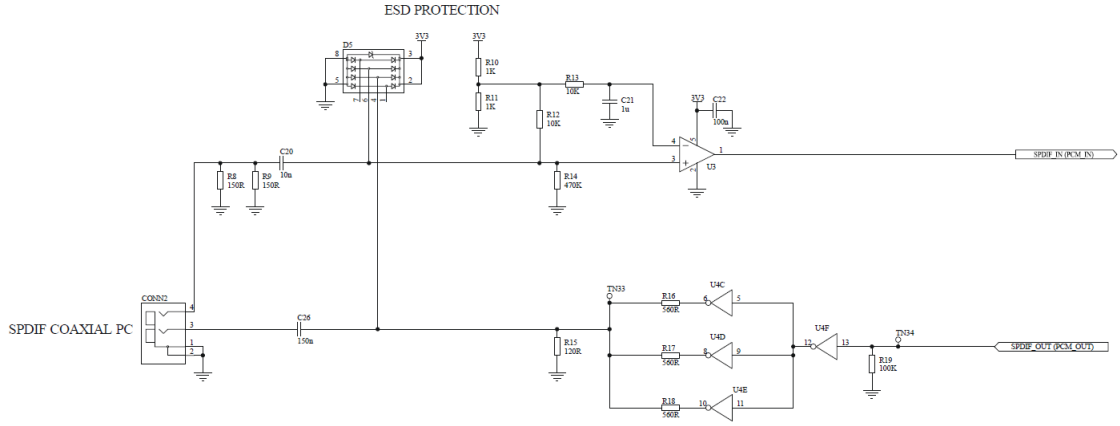


Figure 8.4.1 Example Circuit for SPDIF Interface (Co-Axial)

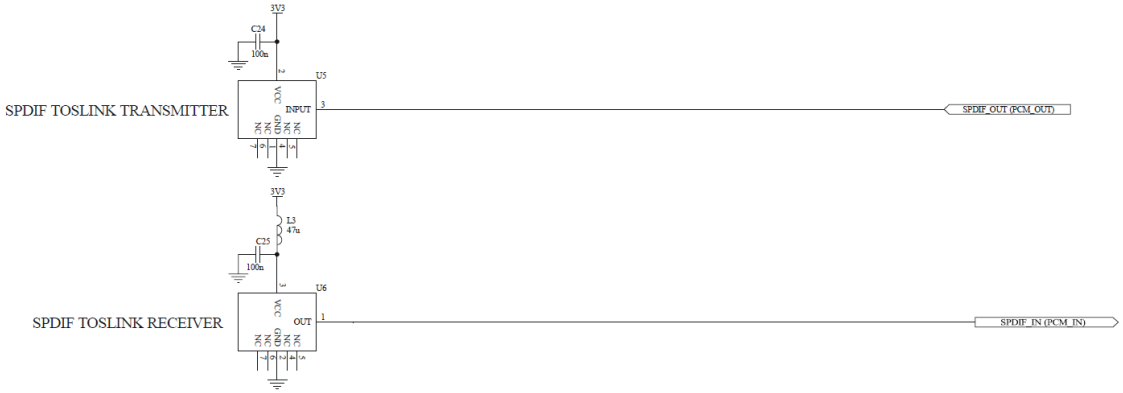


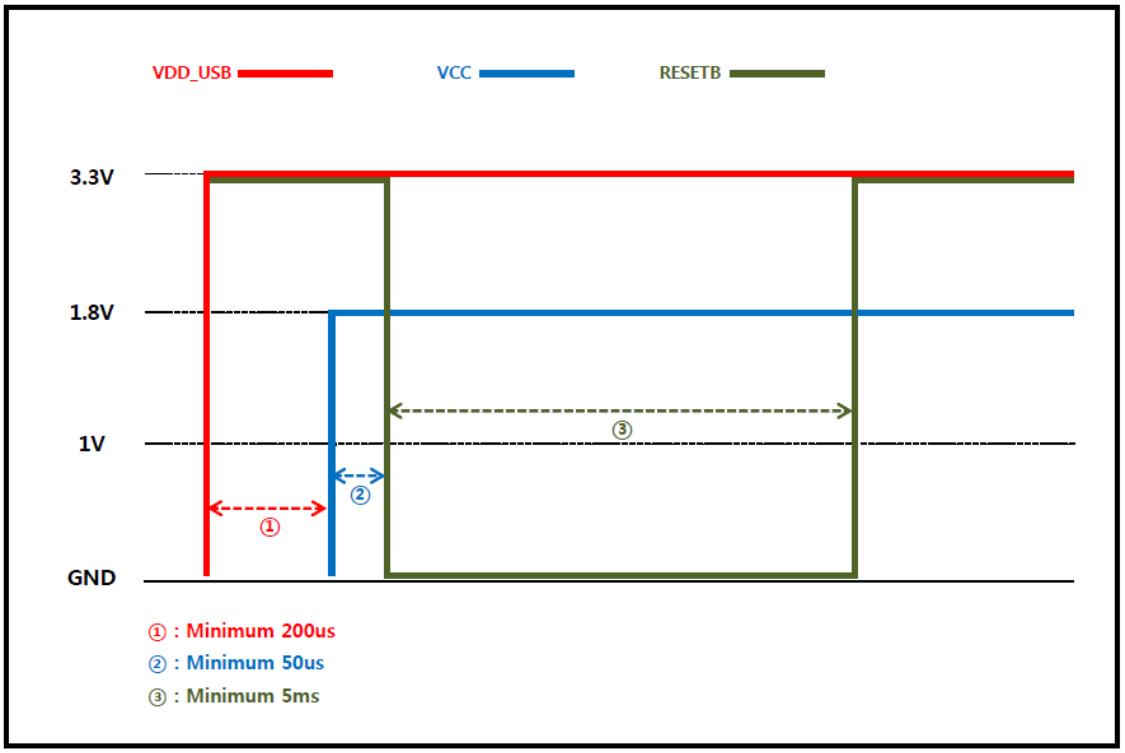
Figure 8.4.2 Example Circuit for SPDIF Interface (Optical)

9. Power Sequence

MD-5XR has two power ports, VDD_USB(3.3V) and Vcc(1.8V).

VDD_USB : Supply the power to internal I/O port and Flash Memory.

VCC : Supply the power to internal Low Voltage Regulator which generates 1.5V.
1.5V power is used on RF, Core, Audio block, etc.



Upper graph shows recommended power sequence of MD-5XR.

① : The time to required to stabilized the Flash Memory

② : The time to required to set the internal Low Voltage Regulator.

③ : A reset performed between 1.5 and 4.0ms following RESETB being active.
CSR recommends that RESETB be applied for a period greater than 5ms.

For normal operation, VDD_USB must be stable before or at the same time as Vcc is powered up and make MD-5XR in reset mode after two power sources are stable.

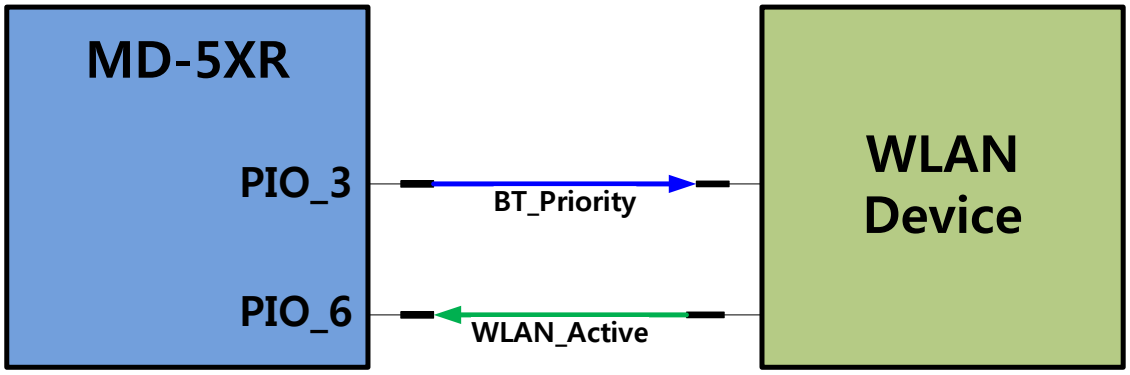
※ Note

At power up, MD-5XR fetches its first instruction from the internal flash memory. It is essential that the flash memory is ready at this point. This means VDD_USB must be above the minimum operating voltage(3.0V). If the flash is not ready, it may return an invalid op code to CSR chip when read. This can crash the firmware or lead to unpredictable results.

10. Co-existence with WLAN

10.1 2-wire Co-existence

As the name implies, CSR's 2-wire coexistence scheme uses only two wires. These two signals are ***BT_Priority*** and ***WLAN_Active***.



BT_Priority is an output from the Bluetooth device, which indicates to the WLAN device that it should stop transmitting immediately and remain silent until this signal is de-asserted. This signal is normally asserted for the following transactions:

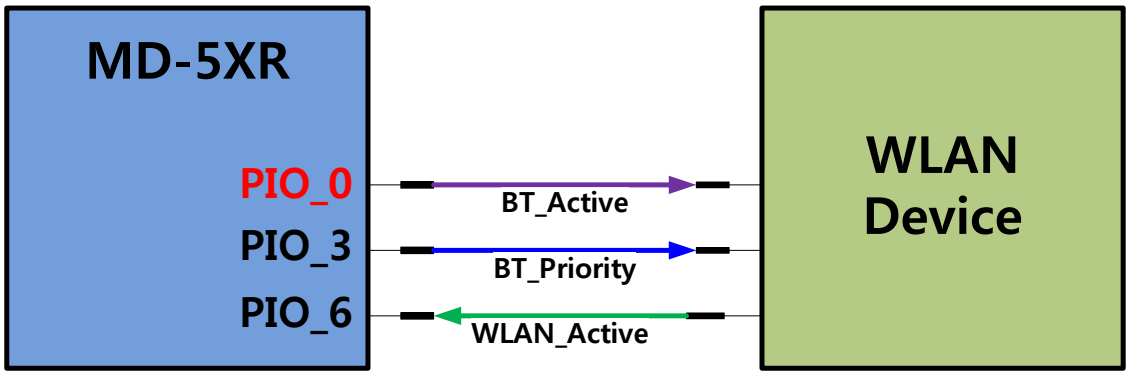
- Inquiry, Inquiry Scan and Inquiry Response
- Paging, Page Scanning and Page Response
- Master Poll and Slave Response
- LMP Data and Response SCO TX and RX data Broadcasts
- Park beacons plus Access Window Slots following the start of a sniff window

PSkey Setting

 # BT Priority (active high),
 # PSKEY_CLOCK_REQUEST_Disable
psset 0x0246 0x0000
 # pskey_lc_combo_priority_pio_mask,
 # use pio[3]
psset 0x0029 0x0008 0x0000
 # pskey_lc_combo_disable_pio_mask,
 # WLAN Active,
 # use pio[6]
psset 0x0028 0x0040 0x0000 0x0000

10.2 Traditional 3-wire Co-existence

The traditional 3-wire coexistence scheme is the same as the 2-wire scheme, mentioned in Section 2, with the addition of a third signal, ***BT_Active***.



BT_Active is an output from the BT device indicating activity which can take the form of a high or low priority transmission or reception. This signal is expected to be useful in designs where an antenna may be shared with another RF device (typically a WLAN device) and/or where a basic activity signal is required in addition to the priority signal already provided by the 2-wire coexistence scheme. *PIO[0] by default and cannot be modified*

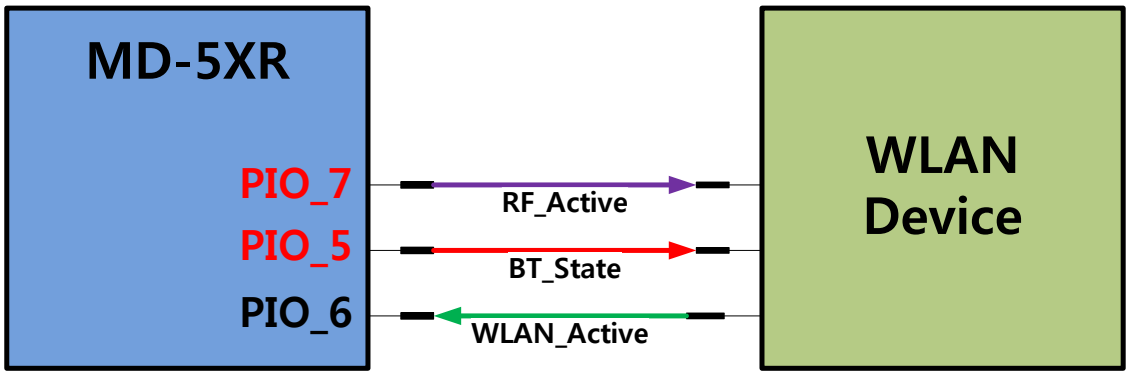
PSkey Setting

```
# BT Priority (active high),
# PSKEY_CLOCK_REQUEST_Disable
psset 0x0246 0x0000
# pskey_lc_combo_priority_pio_mask,
# use pio[3]
psset 0x0029 0x0008 0x0000
# pskey_lc_combo_disable_pio_mask,
# WLAN Active,
# use pio[6]
psset 0x0028 0x0040 0x0000 0x0000
# txrx_pio_control to 0x1
# BT Active signal is made from pio[0] operation
psset 0x0209 0x01                    // PIO_0=High when receive data
# tx_avoid_pa_class1_pio
psset 0x03b3 0x00                    // PIO_0=High when transmit data
# Tx power table change (Add to original table)
psset 0x0031 0x0000 0x0001 0x0000 0x0000 0x0800
```

10.3 Enhanced 3-wire (Packet Traffic Arbitration) Co-existence

The ***Packet Traffic Arbitration*** **(PTA)**, otherwise known as the enhanced 3-wire coexistence, signaling scheme is similar to the traditional 3-wire scheme. However, the timing diagrams for the enhanced scheme are more complex and contain more information regarding the transaction. This scheme should not be confused with the traditional 3-wire scheme.

The enhanced 3-wire scheme consists of the signals, ***RF_Active, BT_State*** & ***WLAN_Active***:



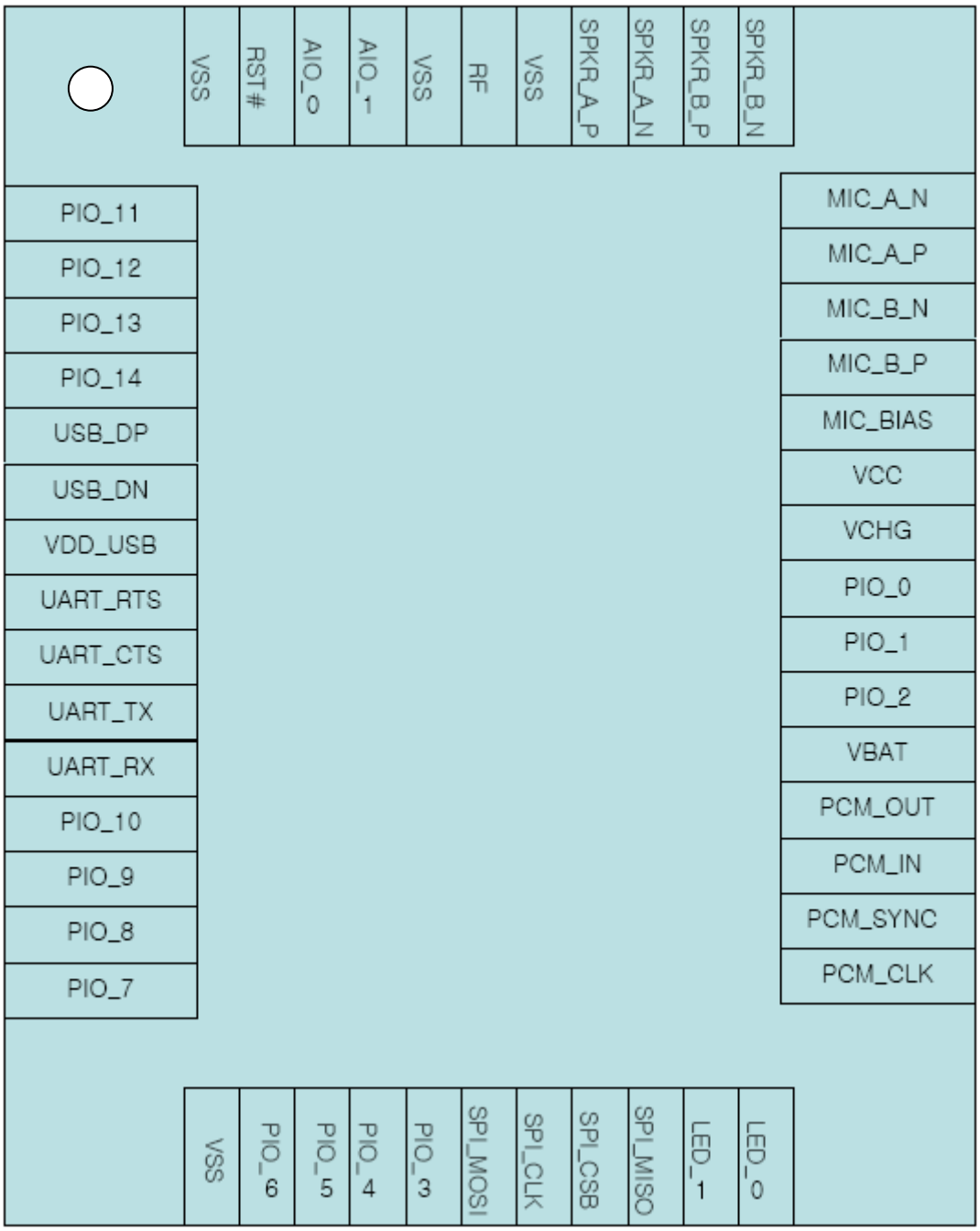
RF_Active is an output from the Bluetooth device that is asserted for all Bluetooth transmission and reception, high or low priority. This signal stays asserted for the entire Bluetooth transmit-receive pair or receive-transmit pair. This signal differs from the ***BT_Active*** signal in that it stays asserted in between transmit-receive or receive-transmit slot pair gap. Due to hardware timing requirements, this signal is assigned to *PIO[7] by default and cannot be modified*.

BT_State is an output from the Bluetooth device indicating if future transaction is a high or low priority and whether the operation is a transmission or reception. The conditions considered high priority are the same as the 2-wire coexistence scheme. Because of hardware timing requirements, this signal is assigned to *PIO[5] by default and cannot be modified*.

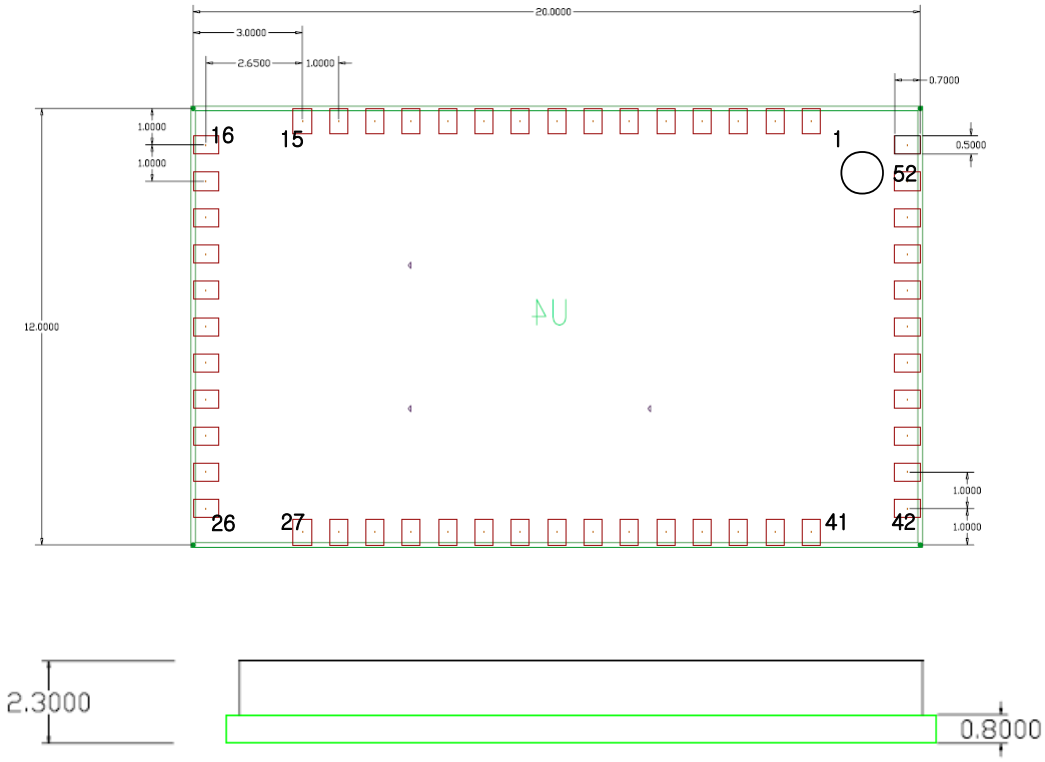
PSkey Setting

```
# BT State, RF active
# pskey_lc_combo_dot11_channel_pio_base to 0x11
psset 0x002a 0x11
# pskey_lc_combo_disable_pio_mask,
# WLAN Active,
# use pio[6]
psset 0x0028 0x0040 0x0000 0x0000
```

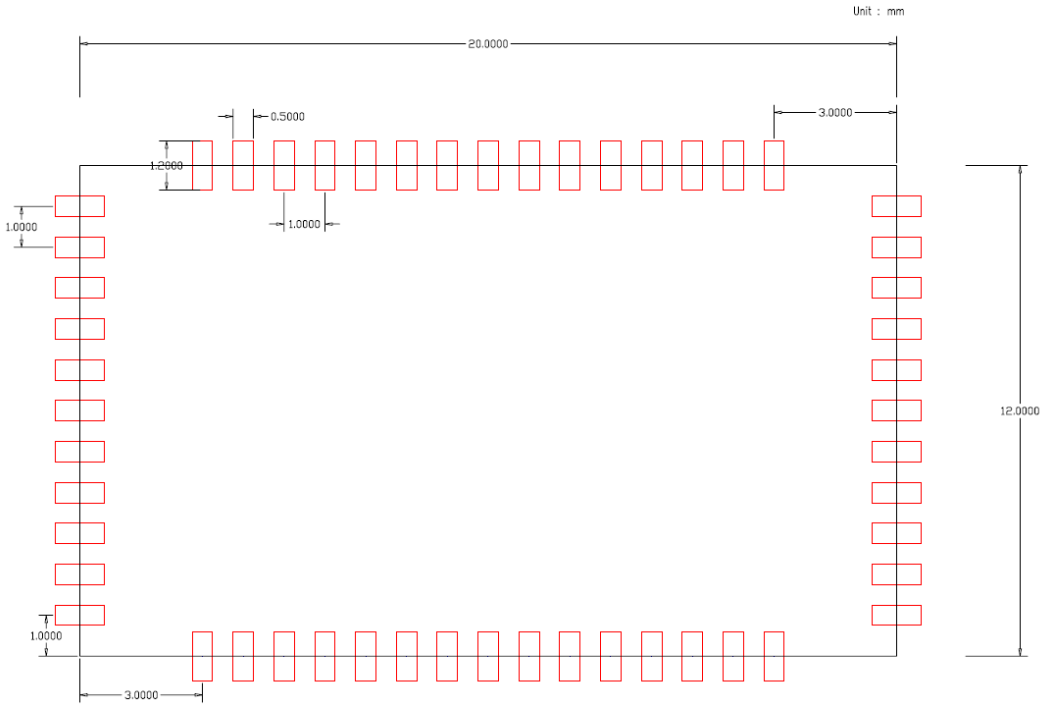
11. Pin Map (TOP View)



12. Dimension



13. Recommended PCB Pattern



FCC compliance Information

FCC Information to User

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

• Reorient or relocate the receiving antenna.

• Increase the separation between the equipment and receiver.

• Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

• Consult the dealer or an experienced radio/TV technician for help.

Caution

Modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Compliance Information : This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) this device must accept any interference received, including interference that may cause undesired operation

This device is intended only for OEM integrators under the following conditions:

1) The transmitter module may not be co-located with any other transmitter or antenna,

2) OEM shall not supply any tool or info to the end-user regarding to Regulatory Domain change.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

IMPORTANT NOTE: In the event that these conditions can not be met (for example certain

laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

End Product Labeling

To satisfy FCC exterior labeling requirements, the following text must be placed on the exterior of the end product : **Contains Transmitter Module FCC ID : 2AD5E-MD5XR**

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.