The Equipment Under Test (EUT) is a Speed Sensor which is mounted on a baseball bat and used to measure swing speed and swing radius. The EUT can operate while connected and controlled by an IOS device (Apple iphone) via Bluetooth radio link. The EUT can only support Bluetooth 4.0 BLE. The Bluetooth portion occupies frequency range of 2402MHz to 2480MHz (40 channels with channel spacing of 2MHz). The EUT is powered by a CR2032 3.0V Lithium battery.

The main components are described below:

1. U1 (CC2541) is a System-On-Chip (SOC) solution incorporating with Bluetooth 4.0 BLE Compliant radio, 8051 MCU, 8k RAM, CODEC and other I/O peripherals.
2. B241 (LFB182G45BG2D280) is the balance matching band-pass filter for the 2.4GHz ISM band.
3. C242 and L243 are components of the antenna matching network.
4. X1 (32MHz crystal) provides system clock for U1 (CC2541).
5. X2 (32.768kHz crystal) provides a slow clock for reducing operating energy.
6. U3 and U4 (ADXL377) are accelerometers for sensing motions.
7. BC1 is CR2032 3.0V Lithium battery.
8. U2 (TPS62730) is DC/DC converter provides 3.3V regulated power supply.
9. J2 is 2 character LCD display.
10. S1 is ON/OFF button.
11. D1 is green LED indicator.

Bluetooth Portion
Modulation Type: GFSK
Antenna Type: Internal, Internal (PCB Trace)
Frequency Range: 2402MHz to 2480MHz, 2MHz channel spacing, 40 channels

Antenna Gain: 0dBi
Normal rated field strength: 91.8dBμV/m @ 3m
Maximum allowed field strength of production tolerance: +/-4dB

CC2541 Bluetooth 4.0 BLE Channel Table

Channel	Frequency (MHz)
1	2402
2	2404
3	2406
4	2408
5	2410
6	2412
7	2414
8	2416
9	2418
10	2420
11	2422
12	2424
13	2426
14	2428
15	2430
16	2432
17	2434
18	2436
19	2438
20	2440
21	2442
22	2444
23	2446
24	2448
25	2450
26	2452
27	2454
28	2456
29	2458
30	2460
31	2462
32	2464
33	2466
34	2468
35	2470
36	2472
37	2474
38	2476
39	2478
40	2480

2.4-GHz *Bluetooth*™ low energy and Proprietary System-on-Chip

Check for Samples: CC2541

FEATURES

- RF
  - 2.4-GHz *Bluetooth* low energy Compliant and Proprietary RF System-on-Chip
  - Supports 250-kbps, 500-kbps, 1-Mbps, 2-Mbps Data Rates
  - Excellent Link Budget, Enabling Long-Range Applications Without External Front End
  - Programmable Output Power up to 0 dBm
  - Excellent Receiver Sensitivity (–94 dBm at 1 Mbps), Selectivity, and Blocking Performance
  - Suitable for Systems Targeting Compliance With Worldwide Radio Frequency Regulations: ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)
- Layout
  - Few External Components
  - Reference Design Provided
  - 6-mm × 6-mm QFN-40 Package
  - Pin-Compatible With CC2540 (When Not Using USB or I^2C)
- Low Power
  - Active-Mode RX Down to: 17.9 mA
  - Active-Mode TX (0 dBm): 18.2 mA
  - Power Mode 1 (4-µs Wake-Up): 270 µA
  - Power Mode 2 (Sleep Timer On): 1 µA
  - Power Mode 3 (External Interrupts): 0.5 µA
  - Wide Supply-Voltage Range (2 V–3.6 V)
- TPS62730 Compatible Low Power in Active Mode
  - RX Down to: 14.7 mA (3-V supply)
  - TX (0 dBm): 14.3 mA (3-V supply)
- Microcontroller
  - High-Performance and Low-Power 8051 Microcontroller Core With Code Prefetch
  - In-System-Programmable Flash, 128- or 256-KB
  - 8-KB RAM With Retention in All Power Modes
  - Hardware Debug Support
  - Extensive Baseband Automation, Including Auto-Acknowledgment and Address Decoding
  - Retention of All Relevant Registers in All Power Modes
- Peripherals
  - Powerful Five-Channel DMA
  - General-Purpose Timers (One 16-Bit, Two 8-Bit)
  - IR Generation Circuitry
  - 32-kHz Sleep Timer With Capture
  - Accurate Digital RSSI Support
  - Battery Monitor and Temperature Sensor
  - 12-Bit ADC With Eight Channels and Configurable Resolution
  - AES Security Coprocessor
  - Two Powerful USARTs With Support for Several Serial Protocols
  - 23 General-Purpose I/O Pins (21 × 4 mA, 2 × 20 mA)
  - I^2C interface
  - 2 I/O Pins Have LED Driving Capabilities
  - Watchdog Timer
  - Integrated High-Performance Comparator
- Development Tools
  - CC2541 Evaluation Module Kit (CC2541EMK)
  - CC2541 Mini Development Kit (CC2541DK-MINI)
  - SmartRF™ Software
  - IAR Embedded Workbench™ Available

SOFTWARE FEATURES

- *Bluetooth* v4.0 Compliant Protocol Stack for Single-Mode BLE Solution
  - Complete Power-Optimized Stack, Including Controller and Host
    - GAP – Central, Peripheral, Observer, or Broadcaster (Including Combination Roles)
    - ATT / GATT – Client and Server
    - SMP – AES-128 Encryption and Decryption
    - L2CAP
  - Sample Applications and Profiles
    - Generic Applications for GAP Central and Peripheral Roles
    - Proximity, Accelerometer, Simple Keys, and Battery GATT Services
    - More Applications Supported in BLE Software Stack
  - Multiple Configuration Options
    - Single-Chip Configuration, Allowing Applications to Run on CC2541
    - Network Processor Interface for Applications Running on an External Microcontroller
  - BTool – Windows PC Application for Evaluation, Development, and Test

APPLICATIONS

- 2.4-GHz *Bluetooth* low energy Systems
- Proprietary 2.4-GHz Systems
- Human-Interface Devices (Keyboard, Mouse, Remote Control)
- Sports and Leisure Equipment
- Mobile Phone Accessories
- Consumer Electronics

CC2541 WITH TPS62730

- TPS62730 is a 2-MHz Step-Down Converter With Bypass Mode
- Extends Battery Lifetime by up to 20%
- Reduced Current in All Active Modes
- 30-nA Bypass Mode Current to Support Low-Power Modes
- RF Performance Unchanged
- Small Package Allows for Small Solution Size
- CC2541 Controllable

DESCRIPTION

The CC2□□1 is a power□optimi□ed true system□on□chip □SoC□solution for both *Bluetooth* low energy and proprietary 2.□G□□ applications. It enables robust network nodes to be built with low total bill□of□material costs. The CC2□□1 combines the excellent performance of a leading R□ transceiver with an industry□standard enhanced □0□1 □CU, in□system programmable flash memory, □□□B RA□, and many other powerful supporting features and peripherals. The CC2□□1 is highly suited for systems where ultralow power consumption is re□uired. This is specified by various operating modes. Short transition times between operating modes further enable low power consumption.

The CC2□□1 is pin□compatible with the CC2□□0 in the □□mm □ □□mm □ □N□0 package, if the USB is not used on the CC2□□0 and the I^2C extra I□O is not used on the CC2□□1. Compared to the CC2□□0, the CC2□□1 provides lower R□ current consumption. The CC2□□1 does not have the USB interface of the CC2□□0, and provides lower maximum output power in T□ mode. The CC2□□1 also adds a □W I^2C interface.

The CC2□□1 is pin□compatible with the CC2□33 R□□CE□optimi□ed IEEE □02.1□.□ SoC.

The CC2□□1 comes in two different versions□ CC2□□1□12□□□2□□, with 12□ □B and 2□□ □B of flash memory, respectively.

□or the CC2□□1 block diagram, see □igure 1.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

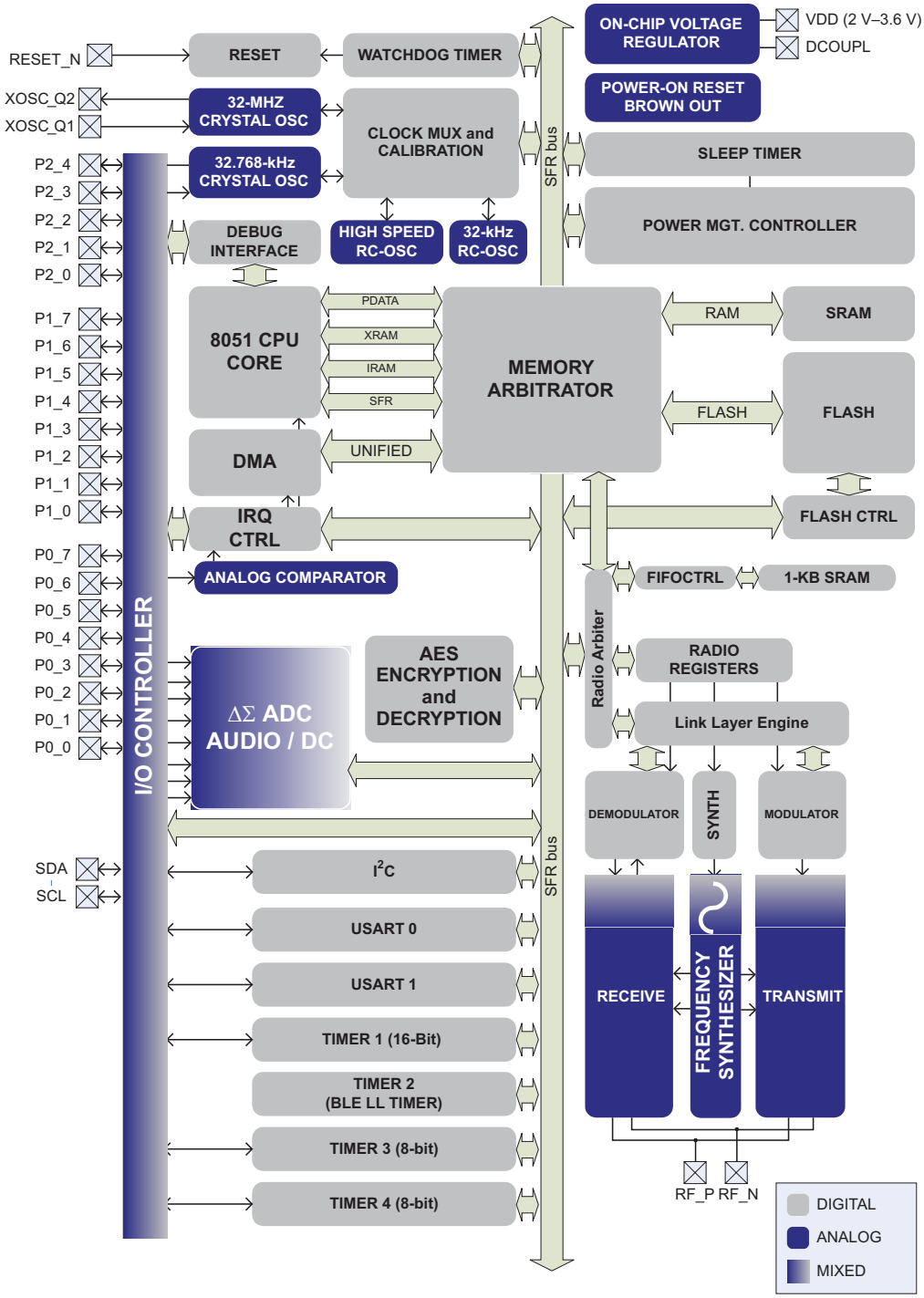


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	All supply pins must have the same voltage	–0.3	3.6	V
Voltage on any digital pin		–0.3	VDD + 0.3 ≤ 3.6	V
Input RF level			10	dBm
Storage temperature range		–40	125	°C
ESD (2)	All pins, excluding pins 20 and 21, according to human-body model, JEDEC STD 22, method A114		2	kV
	All pins, according to human-body model, JEDEC STD 22, method A114		1	kV
	According to charged-device model, JEDEC STD 22, method C101		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) **CAUTION:** ESD sesnsitive device. Precautions should be used when handling the device in order to prevent permanent damage.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Operating ambient temperature range, T_A	–40		85	°C
Operating supply voltage	2		3.6	V

ELECTRICAL CHARACTERISTICS

Measured on Texas Instruments CC2541 EM reference design with T_A = 25°C and VDD = 3 V,
1 Mbps, GFSK, 250-kHz deviation, *Bluetooth* low energy mode, and 0.1% BER

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{core}	Core current consumption	RX mode, standard mode, no peripherals active, low MCU activity		19.6		mA
		RX mode, high-gain mode, no peripherals active, low MCU activity		20.2		
		TX mode, –20 dBm output power, no peripherals active, low MCU activity		18.6		
		TX mode, 0 dBm output power, no peripherals active, low MCU activity		18.2		
		Power mode 1. Digital regulator on, 16-MHz RCOSC and 32-MHz crystal oscillator off, 32.768-kHz XOSC, POR, BOD and sleep timer active, RAM and register retention		270		µA
		Power mode 2. Digital regulator off, 16-MHz RCOSC and 32-MHz crystal oscillator off, 32.768-kHz XOSC, POR, and sleep timer active, RAM and register retention		1		
		Power mode 3. Digital regulator off, no clocks, POR active, RAM and register retention		0.4		
		Low MCU activity, 32-MHz XOSC running. No radio or peripherals. Limited flash access, no RAM access.		6.5		mA
I_{peri}	Peripheral current consumption Adds to core current I_{core} for each peripheral unit activated	Timer 1. Timer running, 32-MHz XOSC used		210		µA
		Timer 2. Timer running, 32-MHz XOSC used		150		
		Timer 3. Timer running, 32-MHz XOSC used		150		
		Timer 4. Timer running, 32-MHz XOSC used		150		
		Sleep timer, including 32.3-kHz RCOSC		0.9		
		ADC, when converting		1.2		mA

GENERAL CHARACTERISTICS

□easured on Texas Instruments CC2□□1 E□ reference design with T_A □ 2□□C and VDD □ 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
WAKE-UP AND TIMING					
Power mode 1 → Active	Digital regulator on, 1□□□ □□RCOSC and 32□□ □□crystal oscillator off. Start□up of 1□□□ □□RCOSC		□		µs
Power mode 2 or 3 → Active	Digital regulator off, 1□□□ □□RCOSC and 32□□ □□crystal oscillator off. Start□up of regulator and 1□□□ □□RCOSC		120		µs
Active → T□ or R□	Crystal ESR □ 1□ Ω. Initially running on 1□□□ □□RCOSC, with 32□□ □□□OSC O□□		□00		µs
	With 32□□ □□□OSC initially on		1□0		µs
R□□T□ turnaround	Proprietary auto mode		130		µs
	B□E mode		1□0		
RADIO PART					
R□ fre□uency range	Programmable in 1□□ □□steps	23□□		2□□□	□□□
Data rate and modulation format	2 □bps, G□S□, □00□k□□deviation 2 □bps, G□S□, 320□k□□deviation 1 □bps, G□S□, 2□0□k□□deviation 1 □bps, G□S□, 1□0□k□□deviation □00 kbps, □S□ 2□0 kbps, G□S□, 1□0□k□□deviation 2□0 kbps, □S□				

RF RECEIVE SECTION

□easured on Texas Instruments CC2□□1 E□ reference design with T_A □ 2□□C, VDD □ 3 V, f_c □ 2□□0 □□□

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
2 Mbps, GFSK, 500-kHz Deviation, 0.1% BER					
Receiver sensitivity			–□0		dBm
Saturation	BER □ 0.1□		–1		dBm
Co□channel re□ection	Wanted signal at –□□ dBm		–□		dB
In□band blocking re□ection	□2 □□□offset, 0.1□ BER, wanted signal –□□ dBm		–2		dB
	□□ □□□offset, 0.1□ BER, wanted signal –□□ dBm		3□		
	□□ □□□or greater offset, 0.1□ BER, wanted signal –□□ dBm		□1		
□re□uency error tolerance [1]	Including both initial tolerance and drift. Sensitivity better than –□□dBm, 2□0 byte payload. BER 0.1□	–300		300	k□□
Symbol rate error tolerance [2]	□aximum packet length. Sensitivity better than–□□dBm, 2□0 byte payload. BER 0.1□	–120		120	ppm
2 Mbps, GFSK, 320-kHz Deviation, 0.1% BER					
Receiver sensitivity			–□□		dBm
Saturation	BER □ 0.1□		–□		dBm
Co□channel re□ection	Wanted signal at –□□ dBm		–12		dB
In□band blocking re□ection	□2 □□□offset, 0.1□ BER, wanted signal –□□ dBm		–1		dB
	□□ □□□offset, 0.1□ BER, wanted signal –□□ dBm		3□		
	□□ □□□or greater offset, 0.1□ BER, wanted signal –□□ dBm		3□		
□re□uency error tolerance [1]	Including both initial tolerance and drift. Sensitivity better than –□□ dBm, 2□0 byte payload. BER 0.1□	–300		300	k□□
Symbol rate error tolerance [2]	□aximum packet length. Sensitivity better than –□□ dBm, 2□0 byte payload. BER 0.1□	–120		120	ppm

□1□ Difference between center fre□uency of the received R□ signal and local oscillator fre□uency
□2□ Difference between incoming symbol rate and the internally generated symbol rate

RF RECEIVE SECTION (continued)

Measured on Texas Instruments CC2541 EM reference design with T_A = 25°C, VDD = 3 V, f_c = 2440 MHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
1 Mbps, GFSK, 250-kHz Deviation, *Bluetooth* low energy Mode, 0.1% BER					
Receiver sensitivity[3]	High gain mode		–92		dBm
	Standard mode		–94		
Saturation[1]	BER = 0.1%		5		dBm
Co-channel rejection[2]	Wanted signal –67 dBm		–9		dB
In-band blocking rejection[2]	1 MHz offset, 0.1% BER, wanted signal –67 dBm		–2		dB
	2 MHz offset, 0.1% BER, wanted signal –67 dBm		29		
	3 MHz offset, 0.1% BER, wanted signal –67 dBm		31		
	≥ 4 MHz offset, 0.1% BER, wanted signal –67 dBm		33		
Out-of-band blocking rejection[2]	Minimum interferer level 2 GHz, Wanted signal –67 dBm		–21		dBm
	Minimum interferer level 2 GHz, 3 GHz, Wanted signal –67 dBm		–29		
	Minimum interferer level 3 GHz, Wanted signal –67 dBm		–9		
Intermodulation[2]	Minimum interferer level		–36		dBm
Frequency error tolerance[3]	Including both initial tolerance and drift. Sensitivity better than 1 dBm, 250 byte payload. BER 0.1%	–250		250	kHz
Symbol rate error tolerance[4]	Maximum packet length. Sensitivity better than –92 dBm, 250 byte payload. BER 0.1%	–50		50	ppm
1 Mbps, GFSK, 160-kHz Deviation, 0.1% BER					
Receiver sensitivity[5]			–91		dBm
Saturation	BER = 0.1%		0		dBm
Co-channel rejection	Wanted signal 10 dB above sensitivity level		–9		dB
In-band blocking rejection	1 MHz offset, 0.1% BER, wanted signal –67 dBm		2		dB
	2 MHz offset, 0.1% BER, wanted signal –67 dBm		29		
	3 MHz offset, 0.1% BER, wanted signal –67 dBm		29		
	≥ 4 MHz offset, 0.1% BER, wanted signal –67 dBm		32		
Frequency error tolerance[3]	Including both initial tolerance and drift. Sensitivity better than –92 dBm, 250 byte payload. BER 0.1%	–200		200	kHz
Symbol rate error tolerance[4]	Maximum packet length. Sensitivity better than –92 dBm, 250 byte payload. BER 0.1%	–50		50	ppm
500 kbps, MSK, 0.1% BER					
Receiver sensitivity[5]			–92		dBm
Saturation	BER = 0.1%		0		dBm
Co-channel rejection	Wanted signal –67 dBm		–9		dB
In-band blocking rejection	1 MHz offset, 0.1% BER, wanted signal –67 dBm		20		dB
	2 MHz offset, 0.1% BER, wanted signal –67 dBm		29		
	2 MHz offset, 0.1% BER, wanted signal –67 dBm		29		
Frequency error tolerance	Including both initial tolerance and drift. Sensitivity better than –92 dBm, 250 byte payload. BER 0.1%	–150		150	kHz
Symbol rate error tolerance	Maximum packet length. Sensitivity better than –92 dBm, 250 byte payload. BER 0.1%	–50		50	ppm

[3] The receiver sensitivity setting is programmable using a TI BLE stack vendor-specific API command. The default value is standard mode.
[1] Results based on standard gain mode.
[2] Difference between center frequency of the received RF signal and local oscillator frequency
[3] Difference between incoming symbol rate and the internally generated symbol rate
[4] Results based on high gain mode.

RF RECEIVE SECTION (continued)

Measured on Texas Instruments CC2541 EM reference design with T_A = 25°C, VDD = 3 V, f_c = 2440 MHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
250 kbps, GFSK, 160 kHz Deviation, 0.1% BER					
Receiver sensitivity [1]			–94		dBm
Saturation	BER = 0.1%		0		dBm
Co-channel rejection	Wanted signal –79 dBm		–3		dB
In-band blocking rejection	1 MHz offset, 0.1% BER, wanted signal –67 dBm		23		dB
	2 MHz offset, 0.1% BER, wanted signal –67 dBm		25		
	2 MHz offset, 0.1% BER, wanted signal –67 dBm		25		
Frequency error tolerance [2]	Including both initial tolerance and drift. Sensitivity better than –94 dBm, 20-byte payload. BER 0.1%	–150		150	kHz
Symbol rate error tolerance [10]	Maximum packet length. Sensitivity better than –94 dBm, 20-byte payload. BER 0.1%	–40		40	ppm
250 kbps, MSK, 0.1% BER					
Receiver sensitivity [11]			–92		dBm
Saturation	BER = 0.1%		0		dBm
Co-channel rejection	Wanted signal –79 dBm		–9		dB
In-band blocking rejection	1 MHz offset, 0.1% BER, wanted signal –67 dBm		20		dB
	2 MHz offset, 0.1% BER, wanted signal –67 dBm		25		
	2 MHz offset, 0.1% BER, wanted signal –67 dBm		30		
Frequency error tolerance	Including both initial tolerance and drift. Sensitivity better than –94 dBm, 20-byte payload. BER 0.1%	–150		150	kHz
Symbol rate error tolerance	Maximum packet length. Sensitivity better than –94 dBm, 20-byte payload. BER 0.1%	–40		40	ppm
ALL RATES/FORMATS					
Spurious emission in RX. Conducted measurement	f < 1 GHz		–57		dBm
Spurious emission in RX. Conducted measurement	f > 1 GHz		–47		dBm

[1] Results based on standard gain mode.
[2] Difference between center frequency of the received RF signal and local oscillator frequency
[10] Difference between incoming symbol rate and the internally generated symbol rate
[11] Results based on high gain mode.

RF TRANSMIT SECTION

Measured on Texas Instruments CC2541 EM reference design with T_A = 25°C, VDD = 3 V and f_c = 2440 MHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output power	Delivered to a single-ended 50-Ω load through a balun using maximum recommended output power setting		0		dBm
	Delivered to a single-ended 50-Ω load through a balun using minimum recommended output power setting		–23		
Programmable output power range	Delivered to a single-ended 50-Ω load through a balun using minimum recommended output power setting		23		dB
Spurious emission conducted measurement	f < 1 GHz		–36		dBm
	f > 1 GHz		–30		dBm
	Suitable for systems targeting compliance with worldwide radio frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)				
Optimum load impedance	Differential impedance as seen from the RF port (RFP and RFN) toward the antenna		50 + j30		Ω

Designs with antenna connectors that require conducted ETSI compliance at 2.4 GHz should insert an LC resonator in front of the antenna connector. Use a 1.8-nH inductor in parallel with a 1.2-pF capacitor. Connect both from the signal trace to a good RF ground.

CURRENT CONSUMPTION WITH TPS62730

Measured on Texas Instruments CC2541 TPA2430 EM reference design with T_A = 25°C, VDD = 3 V and f_c = 2440 MHz, **1 Mbps, GFSK, 250-kHz deviation, Bluetooth™ low energy Mode, 1% BER**(1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current consumption	RF mode, standard mode, no peripherals active, low MCU activity, MCU at 1 MHz		16.5		mA
	RF mode, high-gain mode, no peripherals active, low MCU activity, MCU at 1 MHz		16.5		
	TX mode, –20 dBm output power, no peripherals active, low MCU activity, MCU at 1 MHz		13.1		
	TX mode, 0 dBm output power, no peripherals active, low MCU activity, MCU at 1 MHz		16.3		

(1) 0.1% BER maps to 30.8% PER

32-MHz CRYSTAL OSCILLATOR

Measured on Texas Instruments CC2541 EM reference design with T_A = 25°C and VDD = 3 V

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Crystal frequency			32		MHz
	Crystal frequency accuracy requirement(1)		–40		40	ppm
ESR	Equivalent series resistance				60	Ω
C_0	Crystal shunt capacitance		1		7	pF
C_L	Crystal load capacitance		10		18	pF
	Start-up time			0.2		ms
	Power-down guard time	The crystal oscillator must be in power down for a guard time before it is used again. This requirement is valid for all modes of operation. The need for power-down guard time can vary with crystal type and load.	3			ms

(1) Including aging and temperature dependency, as specified by (1)

32.768-kHz CRYSTAL OSCILLATOR

□easured on Texas Instruments CC2□□1 E□ reference design with T_A □ 2□□C and VDD □ 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Crystal fre□uency			32.□□□		k□□
	Crystal fre□uency accuracy re□uirement [1□]		–□0		□0	ppm
ESR	E□uivalent series resistance			□0	130	kΩ
C_0	Crystal shunt capacitance			0.□	2	p□
$C_□$	Crystal load capacitance			12	1□	p□
	Start□up time			0.□		s

□1□ Including aging and temperature dependency, as specified by □1□

32-kHz RC OSCILLATOR

□easured on Texas Instruments CC2□□1 E□ reference design with T_A □ 2□□C and VDD □ 3 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Calibrated fre□uency [1□]			32.□□3		k□□
□re□uency accuracy after calibration			□0.2□		
Temperature coefficient [2□]			0.□		□ □C
Supply□voltage coefficient [3□]			3		□ □V
Calibration time [□□□]			2		ms

□1□ The calibrated 32□k□□RC oscillator fre□uency is the 32□□ □□ □TA□ fre□uency divided by □□□.
□2□ □re□uency drift when temperature changes after calibration
□3□ □re□uency drift when supply voltage changes after calibration
□□□ When the 32□k□□RC oscillator is enabled, it is calibrated when a switch from the 1□□□ □□RC oscillator to the 32□□ □□crystal oscillator is performed while S□EEPC□ D.OSC32□□CA□DIS is set to 0.

16-MHz RC OSCILLATOR

□easured on Texas Instruments CC2□□1 E□ reference design with T_A □ 2□□C and VDD □ 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
□re□uency [1□]			1□		□□□
Uncalibrated fre□uency accuracy			□1□□		
Calibrated fre□uency accuracy			□0.□□		
Start□up time			10		µs
Initial calibration time [2□]			□0		µs

□1□ The calibrated 1□□□ □□RC oscillator fre□uency is the 32□□ □□ □TA□ fre□uency divided by 2.
□2□ When the 1□□□ □□RC oscillator is enabled, it is calibrated when a switch from the 1□□□ □□RC oscillator to the 32□□ □□crystal oscillator is performed while S□EEPC□ D.OSC□PD is set to 0.

RSSI CHARACTERISTICS

□easured on Texas Instruments CC2□□1 E□ reference design with T_A □ 2□□C and VDD □ 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
2 Mbps, GFSK, 320-kHz Deviation, 0.1% BER and 2 Mbps, GFSK, 500-kHz Deviation, 0.1% BER					
Useful RSSI range [1]	Reduced gain by AGC algorithm		□□		dB
	□igh gain by AGC algorithm		□□		
RSSI offset [1]	Reduced gain by AGC algorithm		□□		dBm
	□igh gain by AGC algorithm		□□		
Absolute uncalibrated accuracy [1]			□□		dB
Step si□e □□SB value□			1		dB
All Other Rates/Formats					
Useful RSSI range [1]	Standard mode		□□		dB
	□igh□gain mode		□□		
RSSI offset [1]	Standard mode		□□		dBm
	□igh□gain mode		10□		
Absolute uncalibrated accuracy [1]			□3		dB
Step si□e □□SB value□			1		dB

□1□ Assuming CC2□□1 E□ reference design. Other R□ designs give an offset from the reported value.

FREQUENCY SYNTHESIZER CHARACTERISTICS

□easured on Texas Instruments CC2□□1 E□ reference design with T_A □ 2□□C, VDD □ 3 V and f_c □ 2□□0 □ □□

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase noise, unmodulated carrier	At □1□□ □□offset from carrier		–10□		dBc□□□
	At □3□□ □□offset from carrier		–112		
	At □□□□ □□offset from carrier		–11□		

ANALOG TEMPERATURE SENSOR

□easured on Texas Instruments CC2□□1 E□ reference design with T_A □ 2□□C and VDD □ 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output	□easured using integrated ADC, internal band□gap voltage reference, and maximum resolution		1□□0		12□bit
Temperature coefficient			□.□		□1□C
Voltage coefficient			1		0.1 V
Initial accuracy without calibration			□10		□C
Accuracy using 1□point calibration			□□		□C
Current consumption when enabled			0.□		mA

COMPARATOR CHARACTERISTICS

T_A □ 2□□C, VDD □ 3 V. All measurement results are obtained using the CC2□□1 reference designs, post□calibration.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common□mode maximum voltage			VDD		V
Common□mode minimum voltage			–0.3		
Input offset voltage			1		mV
Offset vs temperature			1□		□V□C
Offset vs operating voltage			□		mV□V
Supply current			230		nA
□ysteresis			0.1□		mV

ADC CHARACTERISTICS

T_A = 25°C and VDD = 3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage	VDD is voltage on AVDD5 pin	0		VDD	V
	External reference voltage	VDD is voltage on AVDD5 pin	0		VDD	V
	External reference voltage differential	VDD is voltage on AVDD5 pin	0		VDD	V
	Input resistance, signal	Simulated using 32 kHz clock speed		100		kΩ
	Full scale signal [1]	Peak to peak, defines 0 dBFS		2.00		V
ENOB [1]	Effective number of bits	Single ended input, 8 bit setting		7.0		bits
		Single ended input, 9 bit setting		8.0		
		Single ended input, 10 bit setting		9.3		
		Single ended input, 12 bit setting		10.3		
		Differential input, 8 bit setting		7.0		
		Differential input, 9 bit setting		8.3		
		Differential input, 10 bit setting		10		
		Differential input, 12 bit setting		11.0		
		10 bit setting, clocked by RCOSC		9.0		
		12 bit setting, clocked by RCOSC		10.0		
	Useful power bandwidth	9 bit setting, both single and differential		0–20		kHz
THD	Total harmonic distortion	Single ended input, 12 bit setting, –6 dBFS [1]		–66.2		dB
		Differential input, 12 bit setting, –6 dBFS [1]		–80.0		
	Signal to nonharmonic ratio	Single ended input, 12 bit setting [1]		70.2		dB
		Differential input, 12 bit setting [1]		80.3		
		Single ended input, 12 bit setting, –6 dBFS [1]		80.0		
		Differential input, 12 bit setting, –6 dBFS [1]		80.0		
CMRR	Common mode rejection ratio	Differential input, 12 bit setting, 1 kHz sine 0 dBFS, limited by ADC resolution		90		dB
	Crosstalk	Single ended input, 12 bit setting, 1 kHz sine 0 dBFS, limited by ADC resolution		90		dB
	Offset	Midscale		–3		mV
	Gain error			0.000		
DNL	Differential nonlinearity	12 bit setting, mean [1]		0.00		LSB
		12 bit setting, maximum [1]		0.5		
INL	Integral nonlinearity	12 bit setting, mean [1]		1.0		LSB
		12 bit setting, maximum [1]		13.3		
		12 bit setting, mean, clocked by RCOSC		10		
		12 bit setting, max, clocked by RCOSC		20		
SINAD (–THD+N)	Signal to noise and distortion	Single ended input, 8 bit setting [1]		38.0		dB
		Single ended input, 9 bit setting [1]		50.0		
		Single ended input, 10 bit setting [1]		60.0		
		Single ended input, 12 bit setting [1]		70.0		
		Differential input, 8 bit setting [1]		50.0		
		Differential input, 9 bit setting [1]		61.0		
		Differential input, 10 bit setting [1]		61.0		
		Differential input, 12 bit setting [1]		70.0		
	Conversion time	8 bit setting		20		µs
		9 bit setting		36		
		10 bit setting		68		
		12 bit setting		132		

[1] Measured with 300 Hz sine wave input and VDD as reference.

ADC CHARACTERISTICS (continued)

T_A □ 2□□C and VDD □ 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power consumption			1.2		mA
Internal reference VDD coefficient			□		mV□V
Internal reference temperature coefficient			0.□		mV□10□C
Internal reference voltage			1.2□		V

CONTROL INPUT AC CHARACTERISTICS

T_A □ –□0□C to □□□C, VDD □ 2 V to 3.□ V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System clock, f_{SYSC}□□ t_{SYSC}□□ □ 1□f_{SYSC}□□	The undivided system clock is 32 □ □□when crystal oscillator is used. The undivided system clock is 1□ □ □□when calibrated 1□□□ □□RC oscillator is used.	1□		32	□□□
RESET□N low duration	See item 1, □igure 2. This is the shortest pulse that is recogni□ed as a complete reset pin re□uest. Note that shorter pulses may be recogni□ed but do not lead to complete reset of all modules within the chip.	1			□s
Interrupt pulse duration	See item 2, □igure 2.This is the shortest pulse that is recogni□ed as an interrupt re□uest.	20			ns

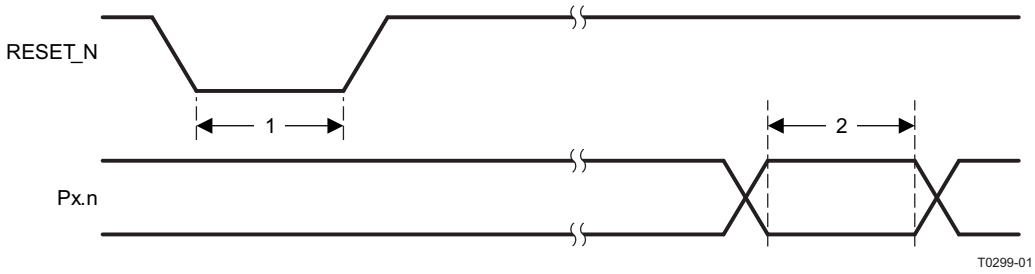


Figure 2. Control Input AC Characteristics

SPI AC CHARACTERISTICS

T_A □ –□0□C to □□□C, VDD □ 2 V to 3.□ V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	SC□ period	□aster, R□ and T□	2□0			ns
		Slave, R□ and T□	2□0			
	SC□ duty cycle	□aster		□0□		
t_2	SSN low to SC□	□aster	□3			ns
		Slave	□3			
t_3	SC□ to SSN high	□aster	□3			ns
		Slave	□3			
$t_□$	□OSI early out	□aster, load □ 10 p□			□	ns
$t_□$	□OSI late out	□aster, load □ 10 p□			10	ns
$t_□$	□ISO setup	□aster	□0			ns
$t_□$	□ISO hold	□aster	10			ns
	SC□ duty cycle	Slave		□0□		ns
t_{10}	□OSI setup	Slave	3□			ns
t_{11}	□OSI hold	Slave	10			ns
$t_□$	□ISO late out	Slave, load □ 10 p□			□□	ns
	Operating fre□uency	□aster, T□ only			□	□□□
		□aster, R□ and T□			□	
		Slave, R□ only			□	
		Slave, R□ and T□			□	

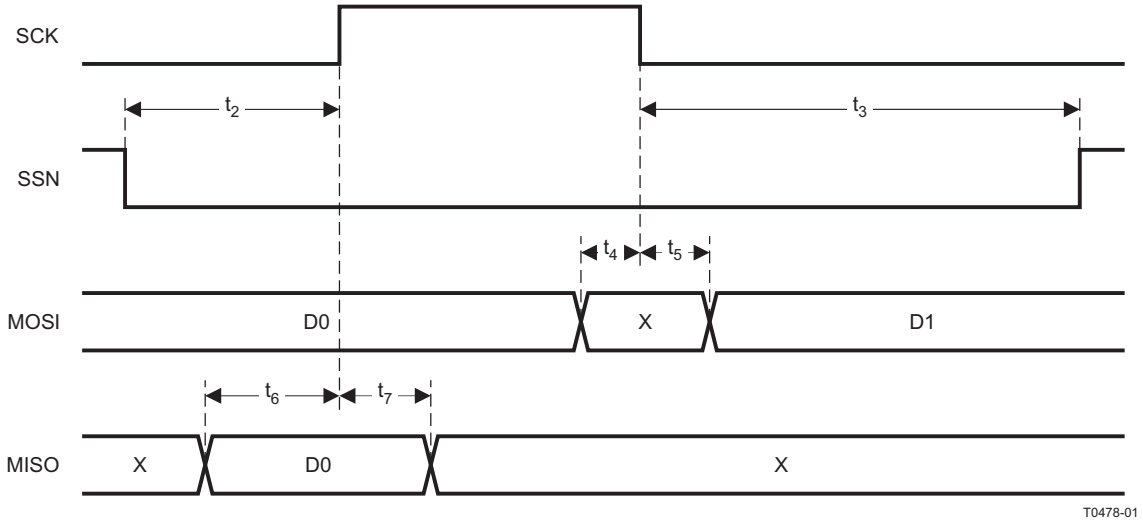


Figure 3. SPI Master AC Characteristics

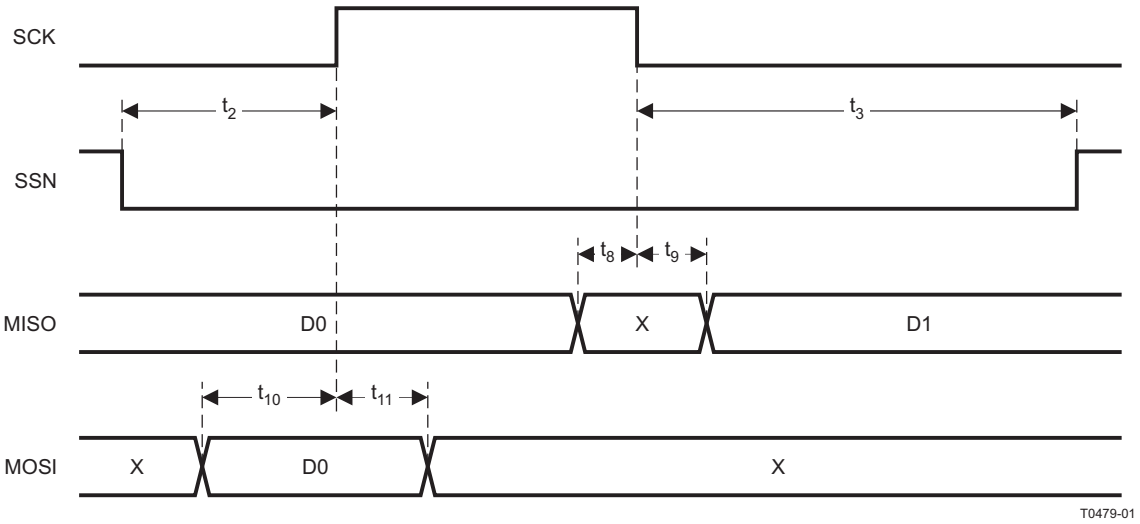


Figure 4. SPI Slave AC Characteristics

DEBUG INTERFACE AC CHARACTERISTICS

T_A □ –□0□C to □□□C, VDD □ 2 V to 3.□ V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk_dbg}	Debug clock fre□uency □see □igure □□				12	□ □□
t_1	Allowed high pulse on clock □see □igure □□		3□			ns
t_2	Allowed low pulse on clock □see □igure □□		3□			ns
t_3	E□T□RESET□N low to first falling edge on debug clock □see □igure □□		1□□			ns
$t_□$	□alling edge on clock to E□T□RESET□N high □see □igure □□		□3			ns
$t_□$	E□T□RESET□N high to first debug command □see □igure □□		□3			ns
$t_□$	Debug data setup □see □igure □□		2			ns
$t_□$	Debug data hold □see □igure □□		□			ns
$t_□$	Clock□to□data delay □see □igure □□	□oad □ 10 p□			30	ns

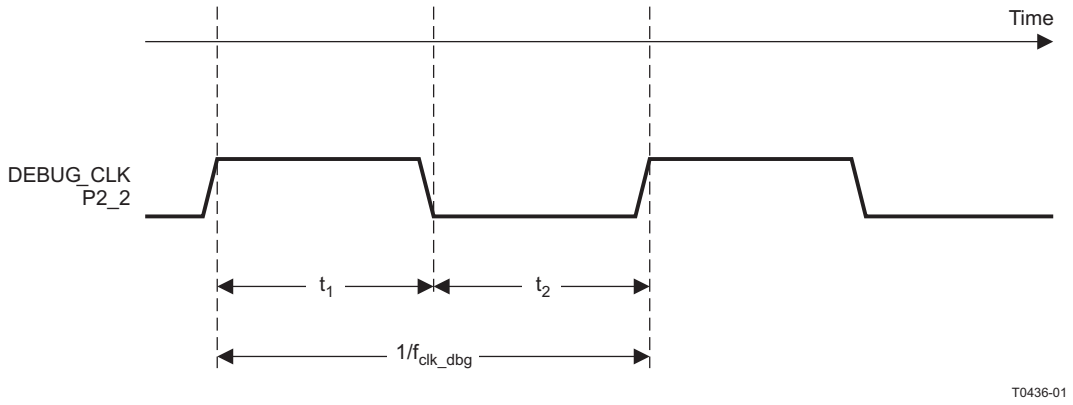


Figure 5. Debug Clock – Basic Timing

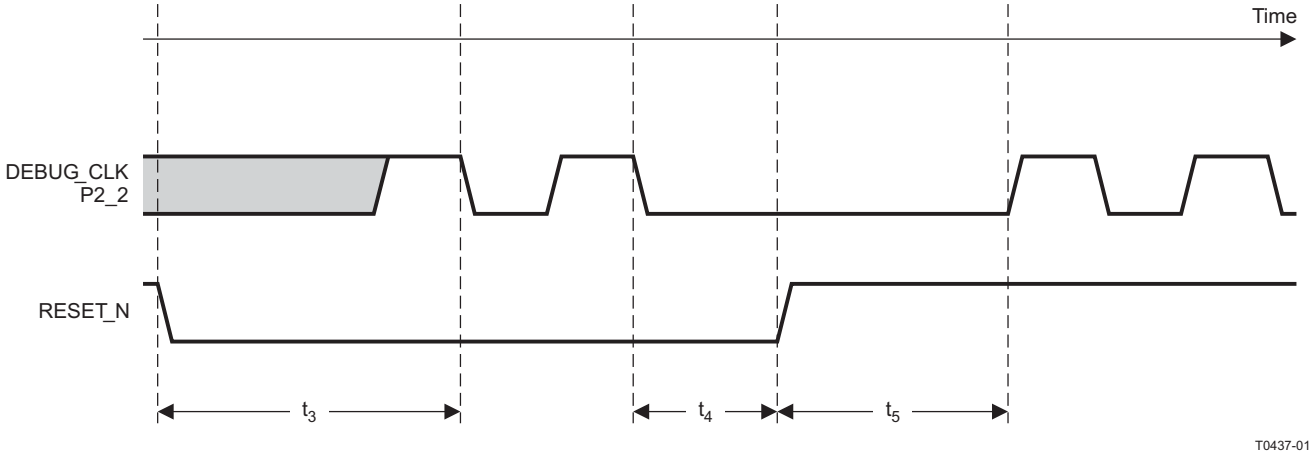


Figure 6. Debug Enable Timing

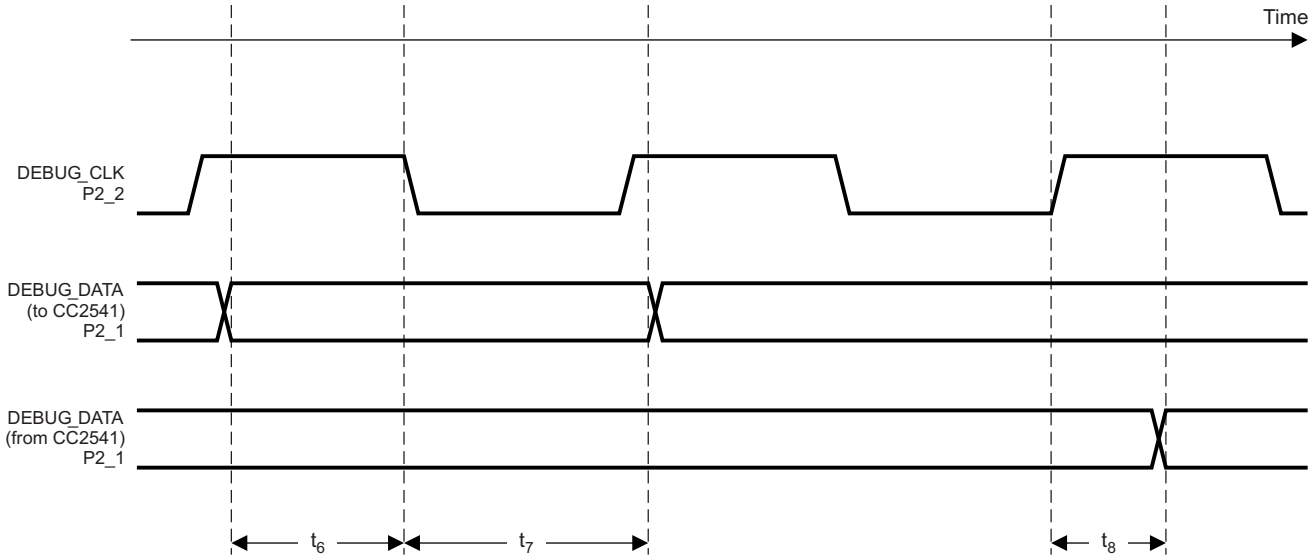


Figure 7. Data Setup and Hold Timing

TIMER INPUTS AC CHARACTERISTICS

T_A □ –□0□C to □□□C, VDD □ 2 V to 3.□ V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input capture pulse duration	Synchroni□ers determine the shortest input pulse that can be recogni□ed. The synchroni□ers operate at the current system clock rate □1□ □ □□or 32 □ □□.	1.□			t_{SYSC}□□

DC CHARACTERISTICS

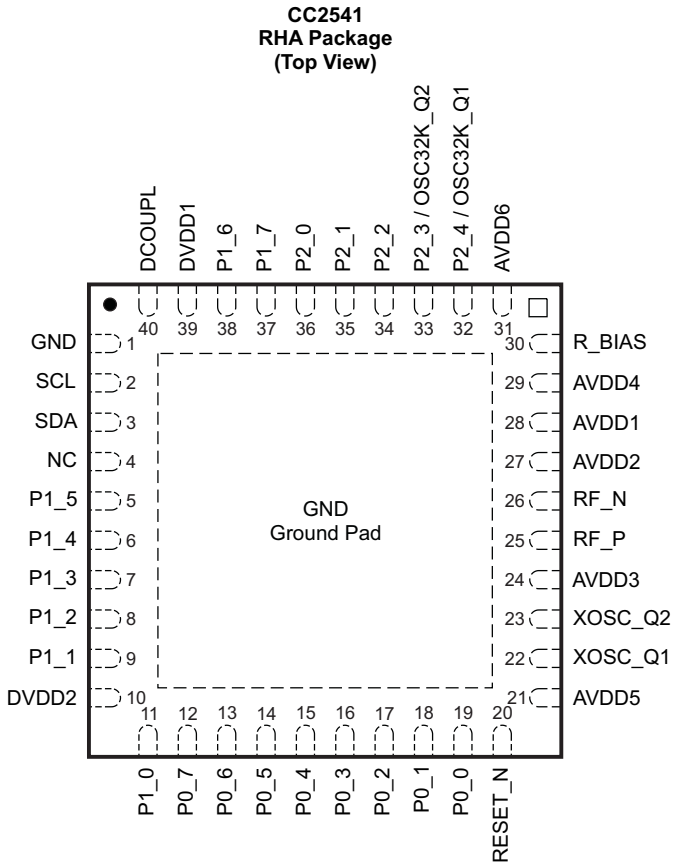
T_A = 25°C, VDD = 3 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic 0 input voltage				0.8	V
Logic 1 input voltage		2.0			V
Logic 0 input current	Input equals 0 V	–50		50	nA
Logic 1 input current	Input equals VDD	–50		50	nA
I/O pin pullup and pulldown resistors			20		kΩ
Logic 0 output voltage, 2 mA pins	Output load 2 mA			0.5	V
Logic 1 output voltage, 2 mA pins	Output load 2 mA	2.3			V
Logic 0 output voltage, 20 mA pins	Output load 20 mA			0.5	V
Logic 1 output voltage, 20 mA pins	Output load 20 mA	2.3			V

DEVICE INFORMATION

PIN DESCRIPTIONS

The CC2541 pinout is shown in Figure 8 and a short description of the pins follows.



NOTE: The exposed ground pad must be connected to a solid ground plane, as this is the ground connection for the chip.

Figure 8. Pinout Top View

PIN DESCRIPTIONS

PIN NAME	PIN	PIN TYPE	DESCRIPTION
AVDD1	2□	Power □analog□	2□V–3.□□V analog power□supply connection
AVDD2	2□	Power □analog□	2□V–3.□□V analog power□supply connection
AVDD3	2□	Power □analog□	2□V–3.□□V analog power□supply connection
AVDD□	2□	Power □analog□	2□V–3.□□V analog power□supply connection
AVDD□	21	Power □analog□	2□V–3.□□V analog power□supply connection
AVDD□	31	Power □analog□	2□V–3.□□V analog power□supply connection
DCOUP□	□0	Power □digital□	1.□□V digital power□supply decoupling. Do not use for supplying external circuits.
DVDD1	3□	Power □digital□	2□V–3.□□V digital power□supply connection
DVDD2	10	Power □digital□	2□V–3.□□V digital power□supply connection
GND	1	Ground pin	Connect to GND
GND	□	Ground	The ground pad must be connected to a solid ground plane.
NC	□	Unused pins	Not connected
P0□0	1□	Digital I□O	Port 0.0
P0□1	1□	Digital I□O	Port 0.1
P0□2	1□	Digital I□O	Port 0.2
P0□3	1□	Digital I□O	Port 0.3
P0□□	1□	Digital I□O	Port 0.□
P0□□	1□	Digital I□O	Port 0.□
P0□□	13	Digital I□O	Port 0.□
P0□□	12	Digital I□O	Port 0.□
P1□0	11	Digital I□O	Port 1.0 – 20□mA drive capability
P1□1	□	Digital I□O	Port 1.1 – 20□mA drive capability
P1□2	□	Digital I□O	Port 1.2
P1□3	□	Digital I□O	Port 1.3
P1□□	□	Digital I□O	Port 1.□
P1□□	□	Digital I□O	Port 1.□
P1□□	3□	Digital I□O	Port 1.□
P1□□	3□	Digital I□O	Port 1.□
P2□0	3□	Digital I□O	Port 2.0
P2□1□DD	3□	Digital I□O	Port 2.1 □debug data
P2□2□DC	3□	Digital I□O	Port 2.2 □debug clock
P2□3□ OSC32□□□2	33	Digital I□O, Analog I□O	Port 2.3□32.□□□ k□□□OSC
P2□□□ OSC32□□□1	32	Digital I□O, Analog I□O	Port 2.□32.□□□ k□□□OSC
RBIAS	30	Analog I□O	External precision bias resistor for reference current
RESET□N	20	Digital input	Reset, active□low
R□□N	2□	R□ I□O	Negative R□ input signal to □NA during R□ Negative R□ output signal from PA during T□
R□□P	2□	R□ I□O	Positive R□ input signal to □NA during R□ Positive R□ output signal from PA during T□
SC□	2	I^2C clock or digital I□O	Can be used as I^2C clock pin or digital I□O. □eave floating if not used. If grounded disable pull up
SDA	3	I^2C clock or digital I□O	Can be used as I^2C data pin or digital I□O. □eave floating if not used. If grounded disable pull up
□OSC□□1	22	Analog I□O	32□□ □□crystal oscillator pin 1 or external clock input
□OSC□□2	23	Analog I□O	32□□ □□crystal oscillator pin 2

BLOCK DIAGRAM

A block diagram of the CC2541 is shown in Figure 9. The modules can be roughly divided into one of three categories: CPU-related modules; modules related to power, test, and clock distribution; and radio-related modules. In the following subsections, a short description of each module is given.

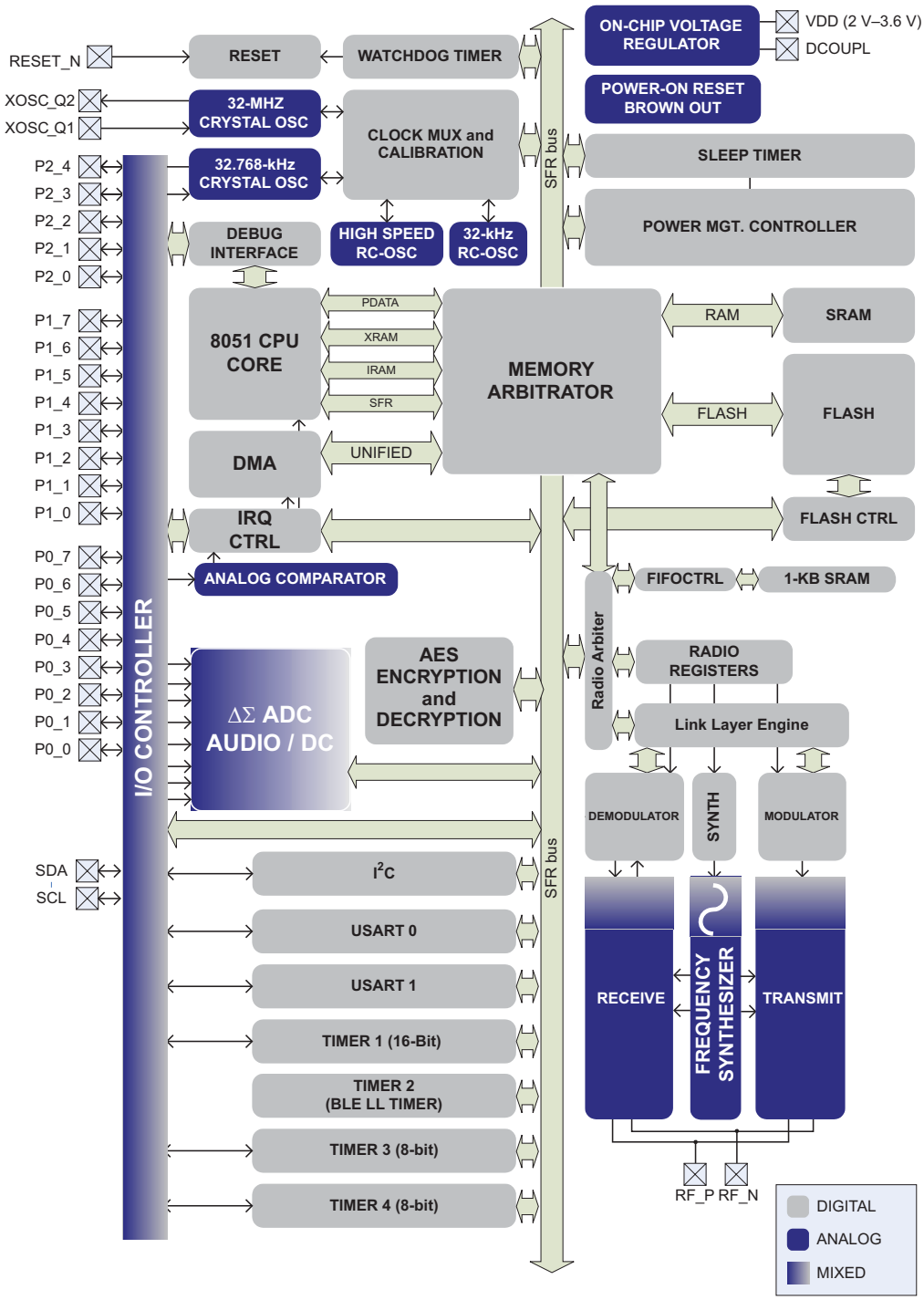


Figure 9. CC2541 Block Diagram

BLOCK DESCRIPTIONS

A block diagram of the CC2541 is shown in Figure 9. The modules can be roughly divided into one of three categories: CPU-related modules; modules related to power, test, and clock distribution; and radio-related modules. In the following subsections, a short description of each module is given.

CPU and Memory

The **8051 CPU core** is a single-cycle 8051-compatible core. It has three different memory access busses (SFR, DATA, and CODE/DATA), a debug interface, and an 18-input extended interrupt unit.

The **memory arbiter** is at the heart of the system, as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus. The memory arbiter has four memory-access points, access of which can map to one of three physical memories: an SRAM, flash memory, and XREG/SFR registers. It is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The **SFR bus** is drawn conceptually in Figure 9 as a common bus that connects all hardware peripherals to the memory arbiter. The SFR bus in the block diagram also provides access to the radio registers in the radio register bank, even though these are indeed mapped into XDATA memory space.

The **8-KB SRAM** maps to the DATA memory space and to parts of the XDATA memory spaces. The SRAM is an ultralow-power SRAM that retains its contents even when the digital part is powered off (power mode 2 and mode 3).

The **128/256 KB flash block** provides in-circuit programmable non-volatile program memory for the device, and maps into the CODE and XDATA memory spaces.

Peripherals

Writing to the flash block is performed through a **flash controller** that allows page-wise erasure and 4-bytewise programming. See User Guide for details on the flash controller.

A versatile five-channel **DMA controller** is available in the system, accesses memory using the XDATA memory space, and thus has access to all physical memories. Each channel (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) is configured with DMA descriptors that can be located anywhere in memory. Many of the hardware peripherals (AES core, flash controller, USARTs, timers, ADC interface, etc.) can be used with the DMA controller for efficient operation by performing data transfers between a single SFR or XREG address and flash/SRAM.

Each CC2541 contains a unique 48-bit IEEE address that can be used as the public device address for a *Bluetooth* device. Designers are free to use this address, or provide their own, as described in the *Bluetooth* specfication.

The **interrupt controller** services a total of 18 interrupt sources, divided into six interrupt groups, each of which is associated with one of four interrupt priorities. I/O and sleep timer interrupt requests are serviced even if the device is in a sleep mode (power modes 1 and 2) by bringing the CC2541 back to the active mode.

The **debug interface** implements a proprietary two-wire serial interface that is used for in-circuit debugging. Through this debug interface, it is possible to erase or program the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute instructions on the 8051 core, set code breakpoints, and single-step through instructions in the code. Using these techniques, it is possible to perform in-circuit debugging and external flash programming elegantly.

The **I/O controller** is responsible for all general-purpose I/O pins. The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so, whether each pin is configured as an input or output and if a pullup or pulldown resistor in the pad is connected. Each peripheral that connects to the I/O pins can choose between two different I/O pin locations to ensure flexibility in various applications.

The **sleep timer** is an ultralow-power timer that can either use an external 32.8-k crystal oscillator or an internal 32.53-k RC oscillator. The sleep timer runs continuously in all operating modes except power mode 3. Typical applications of this timer are as a real-time counter or as a wake-up timer to get out of power mode 1 or mode 2.

A built-in **watchdog timer** allows the CC2541 to reset itself if the firmware hangs. When enabled by software, the watchdog timer must be cleared periodically; otherwise, it resets the device when it times out.

Timer 1 is a 16-bit timer with timer/counter/PWM functionality. It has a programmable prescaler, a 16-bit period value, and five individually programmable counter/capture channels, each with a 16-bit compare value. Each of the counter/capture channels can be used as a PWM output or to capture the timing of edges on input signals. It can also be configured in IR generation mode, where it counts timer 3 periods and the output is ANDed with the output of timer 3 to generate modulated consumer IR signals with minimal CPU interaction.

Timer 2 is a 40-bit timer. It has a 16-bit counter with a configurable timer period and a 24-bit overflow counter that can be used to keep track of the number of periods that have transpired. A 40-bit capture register is also used to record the exact time at which a start-of-frame delimiter is received/transmitted or the exact time at which transmission ends. There are two 16-bit output compare registers and two 24-bit overflow compare registers that can be used to give exact timing for start of RX or TX to the radio or general interrupts.

Timer 3 and timer 4 are 8-bit timers with timer/counter/PWM functionality. They have a programmable prescaler, an 8-bit period value, and one programmable counter channel with an 8-bit compare value. Each of the counter channels can be used as PWM output.

USART 0 and USART 1 are each configurable as either an SPI master/slave or a UART. They provide double buffering on both RX and TX and hardware flow control and are thus well suited to high-throughput full-duplex applications. Each USART has its own high-precision baud-rate generator, thus leaving the ordinary timers free for other uses. When configured as SPI slaves, the USARTs sample the input signal using SCK directly instead of using some oversampling scheme, and are thus well-suited for high data rates.

The **AES encryption/decryption core** allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys. The AES core also supports ECB, CBC, CFB, OFB, CTR, and CBC-MAC, as well as hardware support for CCM.

The **ADC** supports 7 to 12 bits of resolution with a corresponding range of bandwidths from 30-kHz to 4-kHz, respectively. DC and audio conversions with up to eight input channels (I/O controller pins) are possible. The inputs can be selected as single-ended or differential. The reference voltage can be internal, AVDD, or a single-ended or differential external signal. The ADC also has a temperature-sensor input channel. The ADC can automate the process of periodic sampling or conversion over a sequence of channels.

The **I^2C** module provides a digital peripheral connection with two pins and supports both master and slave operation. I^2C support is compliant with the NXP I^2C specification version 2.1 and supports standard mode (up to 100 kbps) and fast mode (up to 400 kbps). In addition, 7-bit device addressing modes are supported, as well as master and slave modes.

The ultralow-power **analog comparator** enables applications to wake up from P0_2 or P0_3 based on an analog signal. Both inputs are brought out to pins; the reference voltage must be provided externally. The comparator output is connected to the I/O controller interrupt detector and can be treated by the MCU as a regular I/O pin interrupt.

TYPICAL CHARACTERISTICS

RX CURRENT vs TEMPERATURE

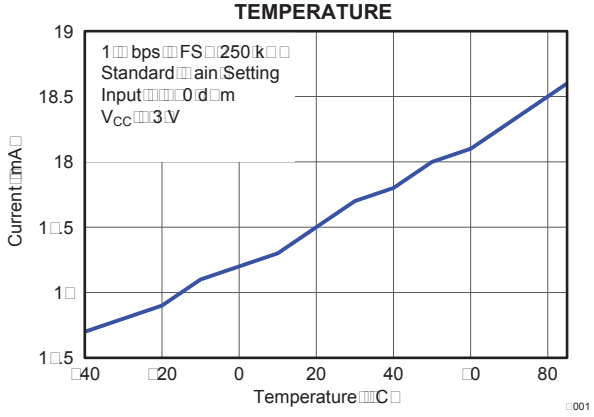


Figure 10.

TX CURRENT vs TEMPERATURE

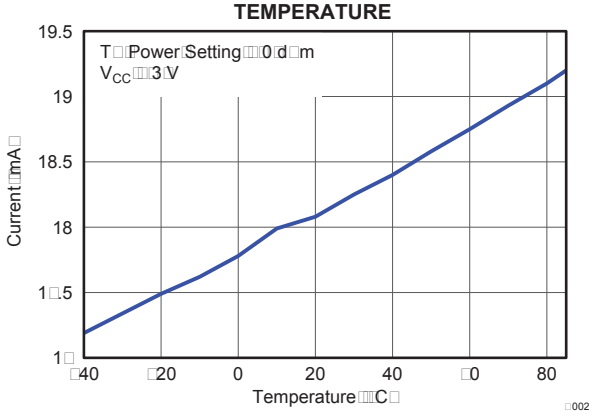


Figure 11.

RX SENSITIVITY vs TEMPERATURE

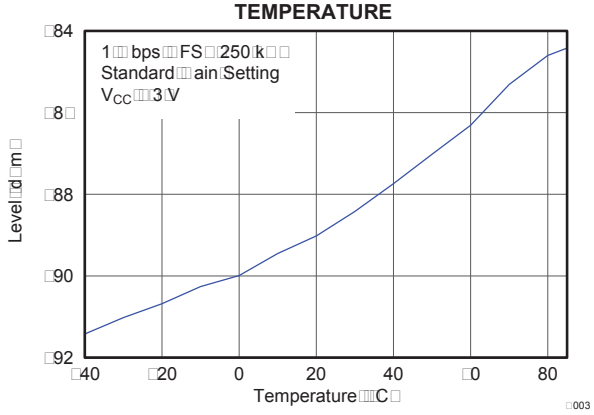


Figure 12.

TX POWER vs TEMPERATURE

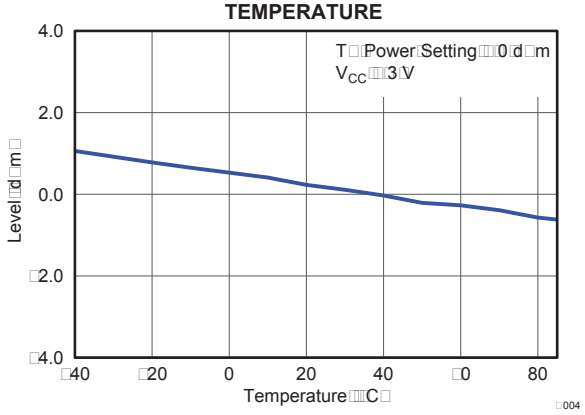


Figure 13.

RX CURRENT vs SUPPLY VOLTAGE

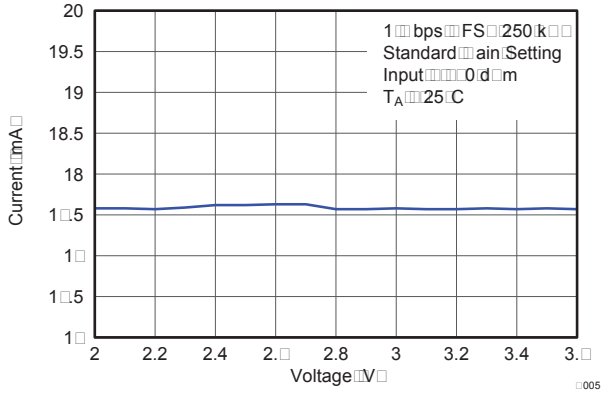


Figure 14.

TX CURRENT vs SUPPLY VOLTAGE

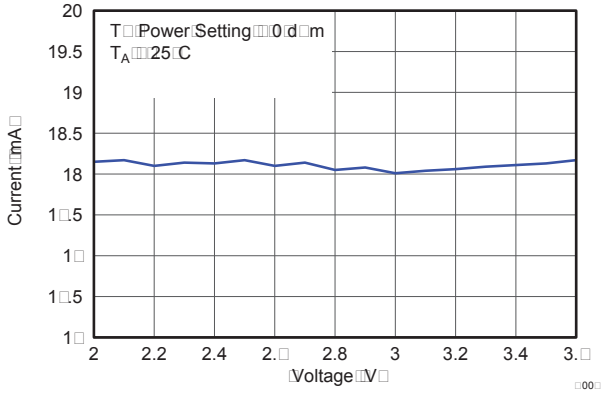


Figure 15.

TYPICAL CHARACTERISTICS (continued)

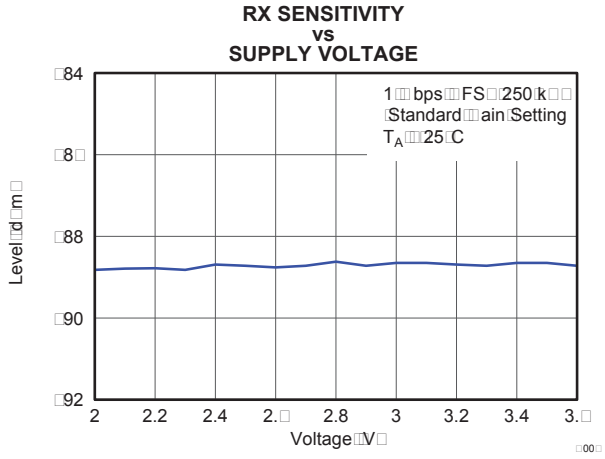


Figure 16.

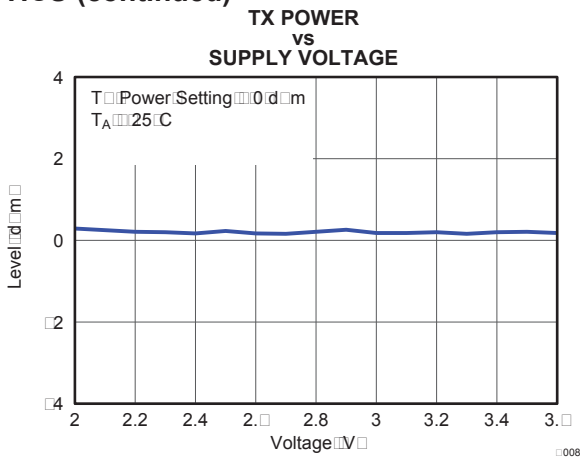


Figure 17.

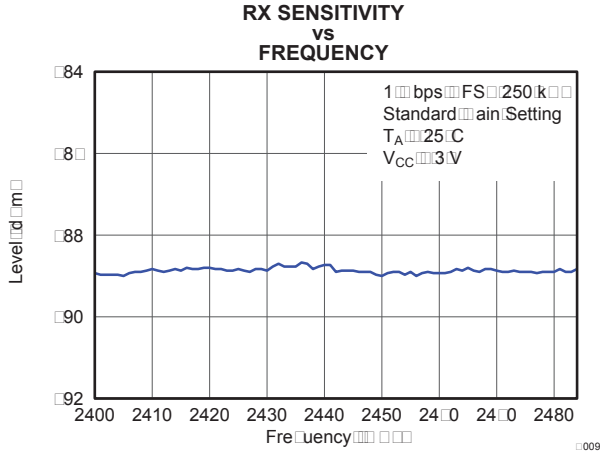


Figure 18.

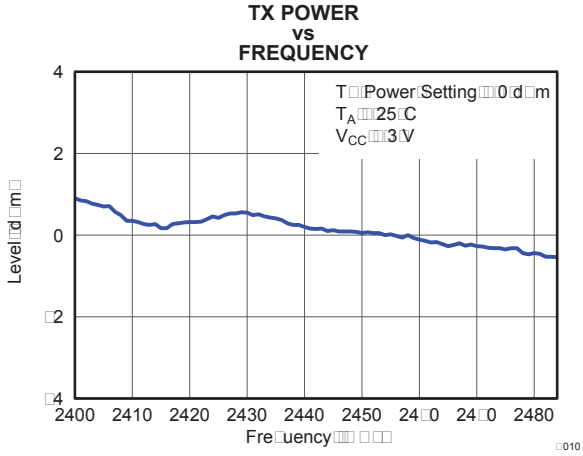


Figure 19.

Table 1. Output Power(1)(2)

TXPOWER Setting	Typical Output Power (dBm)
0xE1	0
0xD1	–2
0xC1	–4
0x 1	–
0xA1	–8
0x91	–10
0x81	–12
0x 1	–14
0x 1	–1
0x51	–18
0x41	–20
0x31	–23

1 easured on Texas Instruments CC2541 E reference design with T_A 25 C, VDD 3 V and f_c 2440 . See SWRU191 for recommended register settings.
2 1 bsp, FS, 250-k deviation, luetooth low energy mode, 1 ER

Table 2. Output Power and Current Consumption

Typical Output Power (dBm)	Typical Current Consumption (mA)(1)	Typical Current Consumption With TPS62730 (mA)(2)
0	18.2	14.3
–20	1□.8	13.1

□1□ □easured on Texas Instruments CC2541 E□ reference design with T_A □25□C, VDD □3 V and f_c □2440 □□□. See SWRU191 for recommended register settings.
□2□ □easured on Texas Instruments CC2541 TPS□2□30 E□ reference design with T_A □25□C, VDD □3 V and f_c □2440 □□□. See SWRU191 for recommended register settings.

TYPICAL CURRENT SAVINGS WHEN USING TPS62730

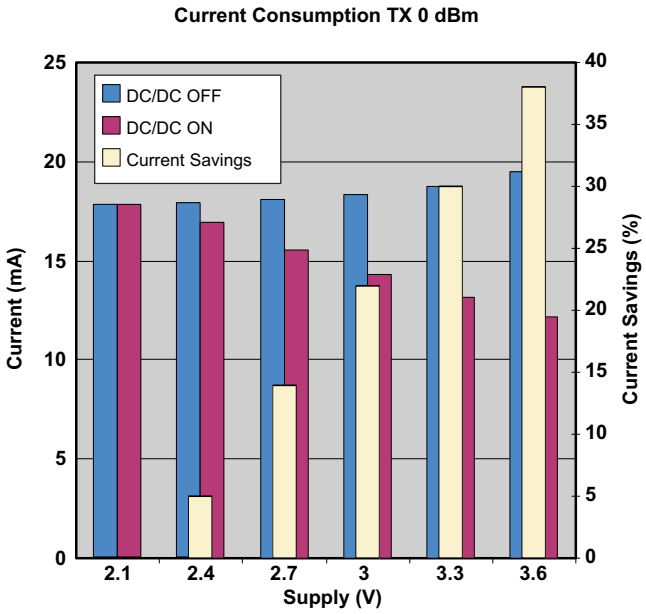


Figure 20. Current Savings in TX at Room Temperature

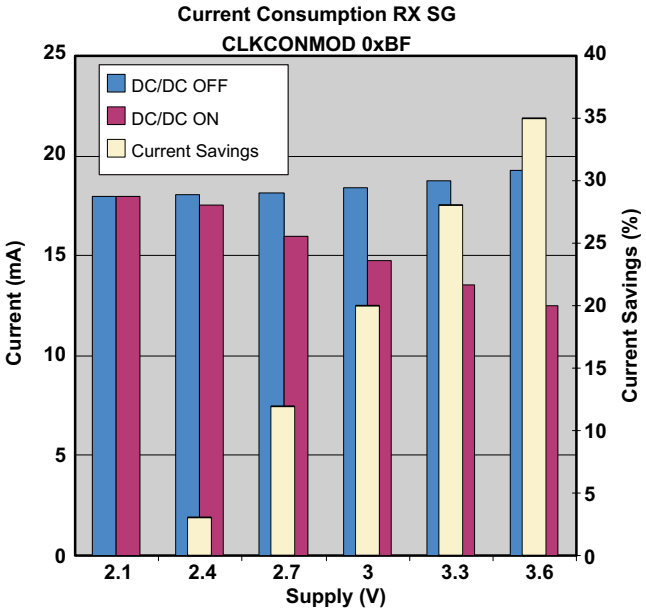
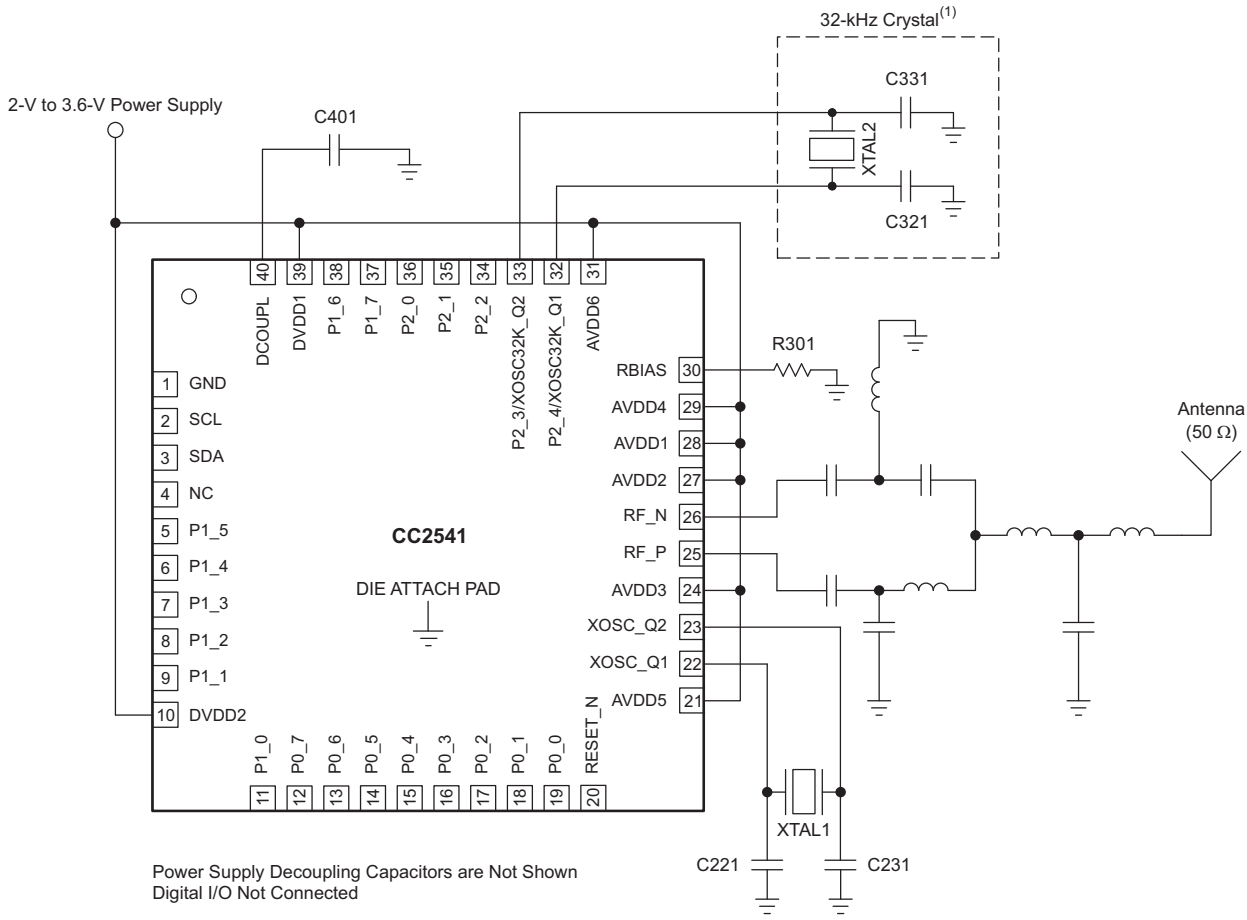


Figure 21. Current Savings in RX at Room Temperature

The application note □SWRA3□5□has information regarding the CC2541 and TPS□2□30 combo board and the current savings that can be achieved using the combo board.

APPLICATION INFORMATION

Few external components are required for the operation of the CC2541. A typical application circuit is shown in Figure 22.



(1) A 32-kHz crystal is mandatory when running the BLE protocol stack in low-power modes, except if the link layer is in the standby state (Vol. 6 Part B Section 1.1 in [1]).

NOTE: Different antenna alternatives will be provided as reference designs.

Figure 22. CC2541 Application Circuit

Table 3. Overview of External Components (Excluding Supply Decoupling Capacitors)

Component	Description	Value
C401	Decoupling capacitor for the internal 1.8-V digital voltage regulator	1 µF
R301	Precision resistor (1%), used for internal biasing	56 kΩ

Input/Output Matching

When using an unbalanced antenna such as a monopole, a balun should be used to optimize performance. The balun can be implemented using low-cost discrete inductors and capacitors. See reference design, CC2541EM, for recommended balun.

Crystal

An external 32-□ □□ crystal, □TAL1, with two loading capacitors □C221 and C231□ is used for the 32-□ □□ crystal oscillator. See 32-□ □□ CRYSTAL □SCILLAT□R for details. The load capacitance seen by the 32-□ □□ crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{221}} + \frac{1}{C_{231}}} + C_{parasitic} \quad (1)$$

□TAL2 is an optional 32.□□8-k□□ crystal, with two loading capacitors □C321 and C331□ used for the 32.□□8-k□□ crystal oscillator. The 32.□□8-k□□ crystal oscillator is used in applications where both very low sleep-current consumption and accurate wake-up times are needed. The load capacitance seen by the 32.□□8-k□□ crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{321}} + \frac{1}{C_{331}}} + C_{parasitic} \quad (2)$$

A series resistor may be used to comply with the ESR re□uirement.

On-Chip 1.8-V Voltage Regulator Decoupling

The 1.8-V on-chip voltage regulator supplies the 1.8-V digital logic. This regulator re□uires a decoupling capacitor □C401□ for stable operation.

Power-Supply Decoupling and Filtering

Proper power-supply decoupling must be used for optimum performance. The placement and si□e of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application. TI provides a compact reference design that should be followed very closely.

References

1. *Bluetooth*□ Core Technical Specification document, version 4.0
   http:□www.bluetooth.com□SiteCollectionDocuments□Core□V40.□ip
2. CC253x System-on-Chip Solution for 2.4-□ □□ IEEE 802.15.4 and □ig□ee□ Applications□CC2541 System-on-Chip Solution for 2.4-□ □□ *Bluetooth* low energy Applications □SWRU191□
3. Current Savings in CC254x Using the TPS□2□30 □SWRA3□5□.

Additional Information

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- E2E interaction

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- Low-power RF and ig ee module solutions and development tools
- RF certification services and RF circuit manufacturing

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REVISION HISTORY

Changes from Original (January 2012) to Revision A	Page
Changed data sheet status from Product Preview to Production Data	1

Changes from Revision A (February 2012) to Revision B	Page
Changed the Temperature coefficient Unit value From: mV C To: 0.1 C	10
Changed Figure 22 text From: ptional 32-k Crystal To: 32-k Crystal	24

Changes from Revision B (August 2012) to Revision C	Page
Changed the Internal reference voltage TYP value From 1.15 V To: 1.24 V	12
Changed pin SC 1 Pin Type From Analog To: Analog I , and changed the Pin Description	1
Changed pin SC 2 Pin Type From Analog To: Analog I	1

Changes from Revision C (November 2012) to Revision D	Page
Changed the RF TRANS IT SECTI N, utput power TYP value From: –20 To: –23	8
Changed the RF TRANS IT SECTI N, Programmable output power range TYP value From: 20 To: 23	8
Added row 0x31 to Table 1	22

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC2541F128R□AR	ACTIVE	V□FN	R□A	40	2500	□reen□Ro□S □□no Sb□□r□	CU□NIPDAU□□ CU□NIPDAUA□	Level-3-2□0C-1□8□□R		CC2541 F128	Samples
CC2541F128R□AT	ACTIVE	V□FN	R□A	40	250	□reen□Ro□S □□no Sb□□r□	CU□NIPDAU□□ CU□NIPDAUA□	Level-3-2□0C-1□8□□R		CC2541 F128	Samples
CC2541F25□R□AR	ACTIVE	V□FN	R□A	40	2500	□reen□Ro□S □□no Sb□□r□	CU□NIPDAU□□ CU□NIPDAUA□	Level-3-2□0C-1□8□□R		CC2541 F25□	Samples
CC2541F25□R□AT	ACTIVE	V□FN	R□A	40	250	□reen□Ro□S □□no Sb□□r□	CU□NIPDAU□□ CU□NIPDAUA□	Level-3-2□0C-1□8□□R		CC2541 F25□	Samples

(1) The□marketing□status□values□are□defined□as□follows:
ACTIVE: □Product□device□recommended□for□new□designs.
LIFEBUY: □TI□has□announced□that□the□device□will□be□discontinued,□and□a□lifetime-buy□period□is□in□effect.
NRND: □Not□recommended□for□new□designs.□Device□is□in□production□to□support□existing□customers,□but□TI□does□not□recommend□using□this□part□in□a□new□design.
PREVIEW: □Device□has□been□announced□but□is□not□in□production.□Samples□may□or□may□not□be□available.
OBSOLETE: □TI□has□discontinued□the□production□of□the□device.

(2) □Eco□Plan□-□The□planned□eco-friendly□classification:□Pb-Free□□Ro□S□,□Pb-Free□□Ro□S□Exempt□,□or□□reen□□Ro□S□□□no□Sb□□r□□-□please□check□http:□□www.ti.com□productcontent□for□the□latest□availability□information□and□additional□product□content□details.
TBD: □The□Pb-Free□□reen□conversion□plan□has□not□been□defined.
Pb-Free□(RoHS): □TI□s□terms□□Lead-Free□□or□□Pb-Free□□mean□semiconductor□products□that□are□compatible□with□the□current□Ro□S□re□uirements□for□all□□substances,□including□the□re□uirement□that□lead□not□exceed□0.1□□by□weight□in□homogeneous□materials.□Where□designed□to□be□soldered□at□high□temperatures,□TI□Pb-Free□products□are□suitable□for□use□in□specified□lead-free□processes.
Pb-Free□(RoHS□Exempt): □This□component□has□a□Ro□S□exemption□for□either□1□□lead-based□flip-chip□solder□bumps□used□between□the□die□and□package,□or□2□□lead-based□die□adhesive□used□between□the□die□and□leadframe.□The□component□is□otherwise□considered□Pb-Free□□Ro□S□compatible□as□defined□above.
Green□(RoHS□&□no□Sb/Br): □TI□defines□□□reen□□to□mean□Pb-Free□□Ro□S□compatible□,□and□free□of□□romine□□r□□and□Antimony□Sb□based□flame□retardants□□□r□or□Sb□do□not□exceed□0.1□□by□weight□in□homogeneous□material□

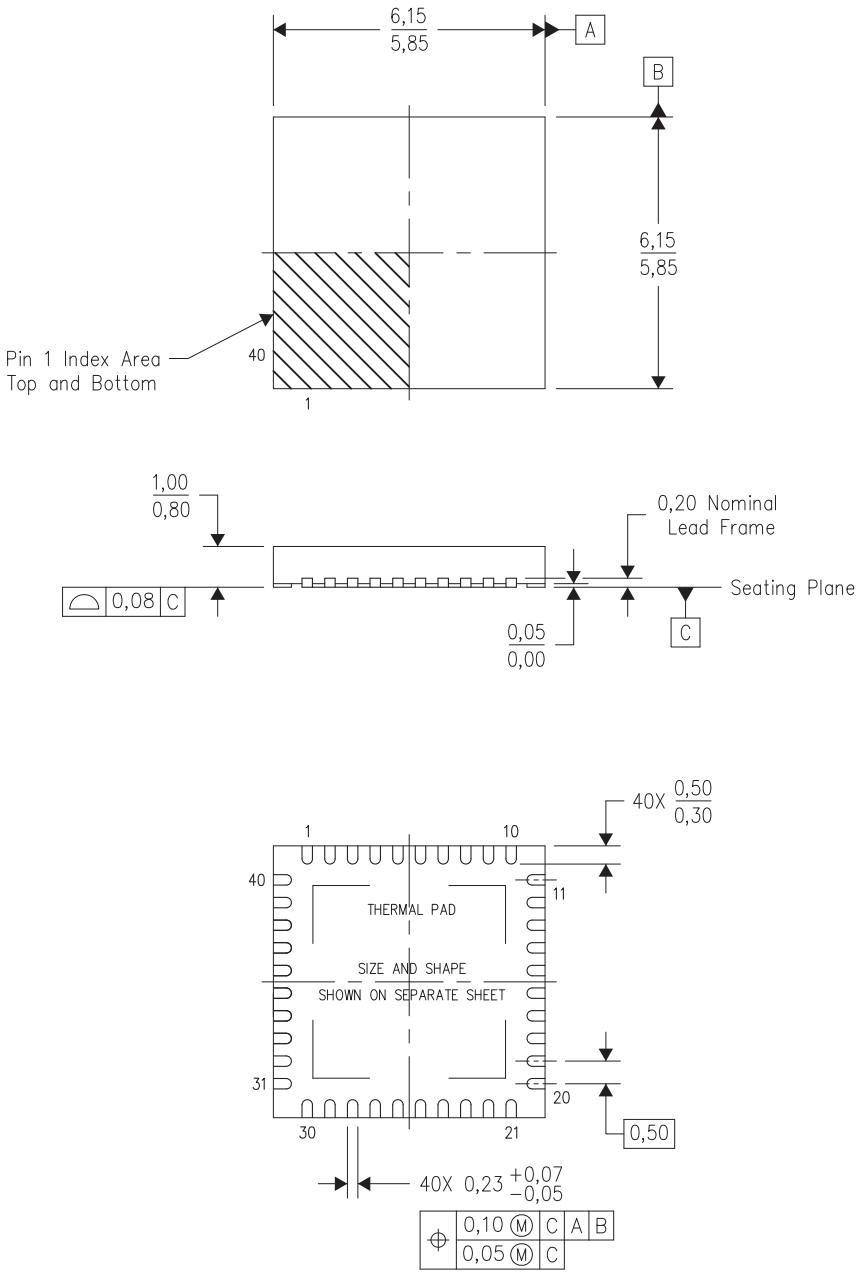
(3) □□SL,□Peak□Temp.□-□The□□oisture□Sensitivity□Level□rating□according□to□the□JEDEC□industry□standard□classifications,□and□peak□solder□temperature.

(4) □There□may□be□additional□marking,□which□relates□to□the□logo,□the□lot□trace□code□information,□or□the□environmental□category□on□the□device.

(5) □□ultiple□Device□□arkings□will□be□inside□parentheses.□□nly□one□Device□□arking□contained□in□parentheses□and□separated□by□a□□□□will□appear□on□a□device.□If□a□line□is□indented□then□it□is□a□continuation□of□the□previous□line□and□the□two□combined□represent□the□entire□Device□□arking□for□that□device.

(6) □Lead□□all□Finish□-□□rderable□Devices□may□have□multiple□material□finish□options.□Finish□options□are□separated□by□a□vertical□ruled□line.□Lead□□all□Finish□values□may□wrap□to□two□lines□if□the□finish□value□exceeds□the□maximum□column□width.

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



4204276/E 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220 variation VJJD–2.

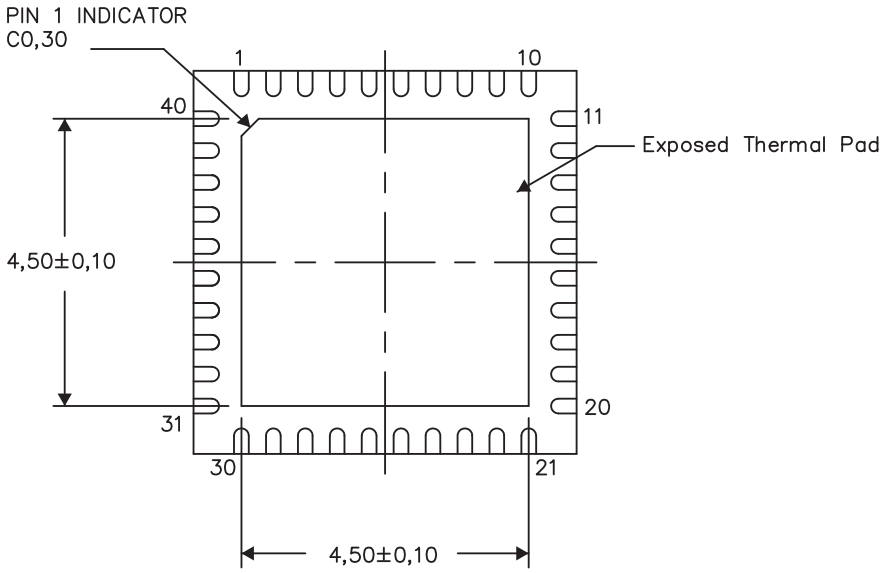
RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



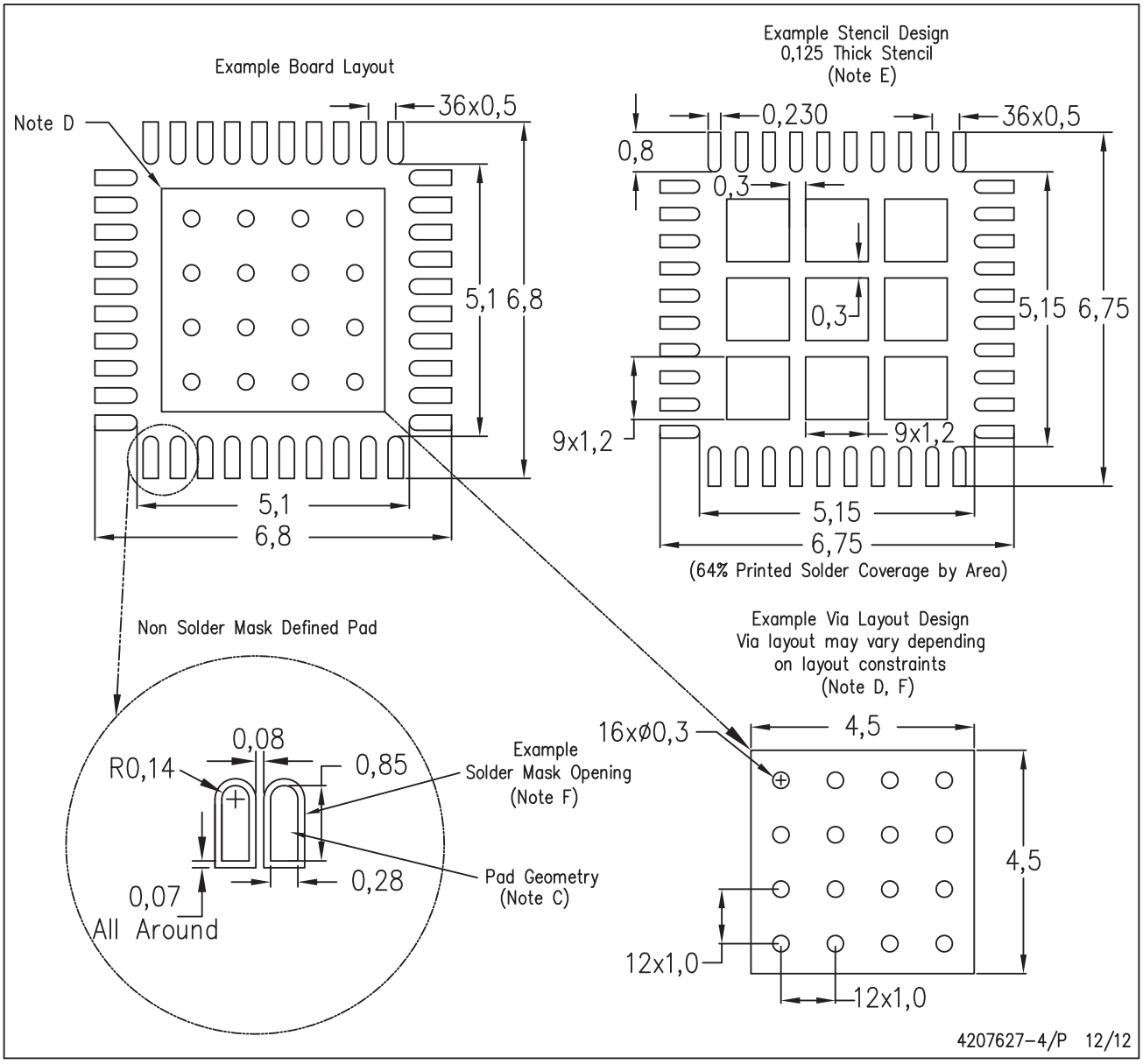
Bottom View

Exposed Thermal Pad Dimensions

4206355–4/U 12/12

NOTES: A. All linear dimensions are in millimeters

RHA (S–PVQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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