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THEORY OF OPERATION – GENERAL, RX

The Atheros 9331 SoC contains two receive chains, each with a separate LNA. In the EPCR5, only one input is used, the other is grounded and disabled in firmware. The EPCR5 antenna is switched between input and PA sections using a single physical antenna port, effectively half-duplex operation. A ¼ wave tuned stub prevents ESD damage. The receiver block internal to the 9331 converts the received RF signal into baseband I and Q outputs. In the EPCR5, only the 802.11n operational mode is supported. The I and Q signals are amplified internally in the 9331 using a PGA before being filtered and passed to the internal ADC. The DC offset in the receive chain is compensated via an Atheros proprietary design. Final decimation of the ADC outputs is performed internally in the 9331 SoC. The receive chain power-down mode is not supported in the EPCR5.

THEORY OF OPERATION, TX CHAIN

The EPCR5 transmit section is based on a precise TXCO oscillator and the 9331 SoC transmitter. The oscillator drives a PLL multiplier which generates all internal reference frequencies. Inside the 9331 transmit section, the transmitter converts I & Q inputs to 2.4GHz RF. The outputs of the modulation DAC are low-pass filtered through an on-chip filter network to remove spectral images and out-of-band quantization noise. The I&Q signals from the filter are converted to RF using an integrated up-conversion architecture. The internal power amplifier sends output RF through a switch via an external filter network directly to the antenna. The only external components in the EPCR5 transmit section are in the filter network recommended as by Atheros. The 9331 provides a TX power-down mode which is not supported in the EPCR5 design. The Atheros uses an on-chip detector for closed-loop output power control. Power settings requested by the firmware are filtered by the Atheros Hardware Abstraction Layer (HAL) before being sent to the PA PGA. No power adjustments are available to the user.