ROHM GROUP
LAPIS SEMICONDUCTOR

PEDK71050-03-06
Issue Date : Dec,15,2014

MK71050-03

Preliminary

Bluetooth® Low Energy wireless module

■Overview

MK71050-03 is a Bluetooth® Low Energy (here in after LE) wireless module which is integrating ML7105C-001 Bluetooth LE SoC, E2PROM, 26MHz crystal oscillator, 2.4GHz PCB pattern antenna and passive components.
It has Bluetooth® LE compliant 2.4GHz band radio communication capability.
MK71050-03 is suitable for applications such as Healthcare device, Remote Controller or PC peripherals.

■Features

- Bluetooth® SIG Core Spec v4.0 compliant
- Radio certification
  - MIC JAPAN(certification no:006-000238）
  - FCC（FCC ID:2ACIJ71050-3）
  - CE（R&TTE）
- Integrating ML7105C-001 Bluetooth® LE single mode LSI
- Integrating 26MHz xtal oscillator
- Integrating 128kbit EEPROM
- Single power supply 1.8V to 3.6V
- Operating Temperature -20 deg.C to 70 deg.C
- Current Consumptions
  - Deep Sleep Mode 0.8uA（Typ.） (with external Low Power Clock)
  - Idle Mode 3mA （Typ.）
  - TX mode 9mA （Typ.）
  - RX mode 9mA （Typ.）
- Dimension 10.7mm(W) x 13.6mm (L) x 1.78mm (H)
- Pb Free, RoHS compliant
- Product Name MK71050-03

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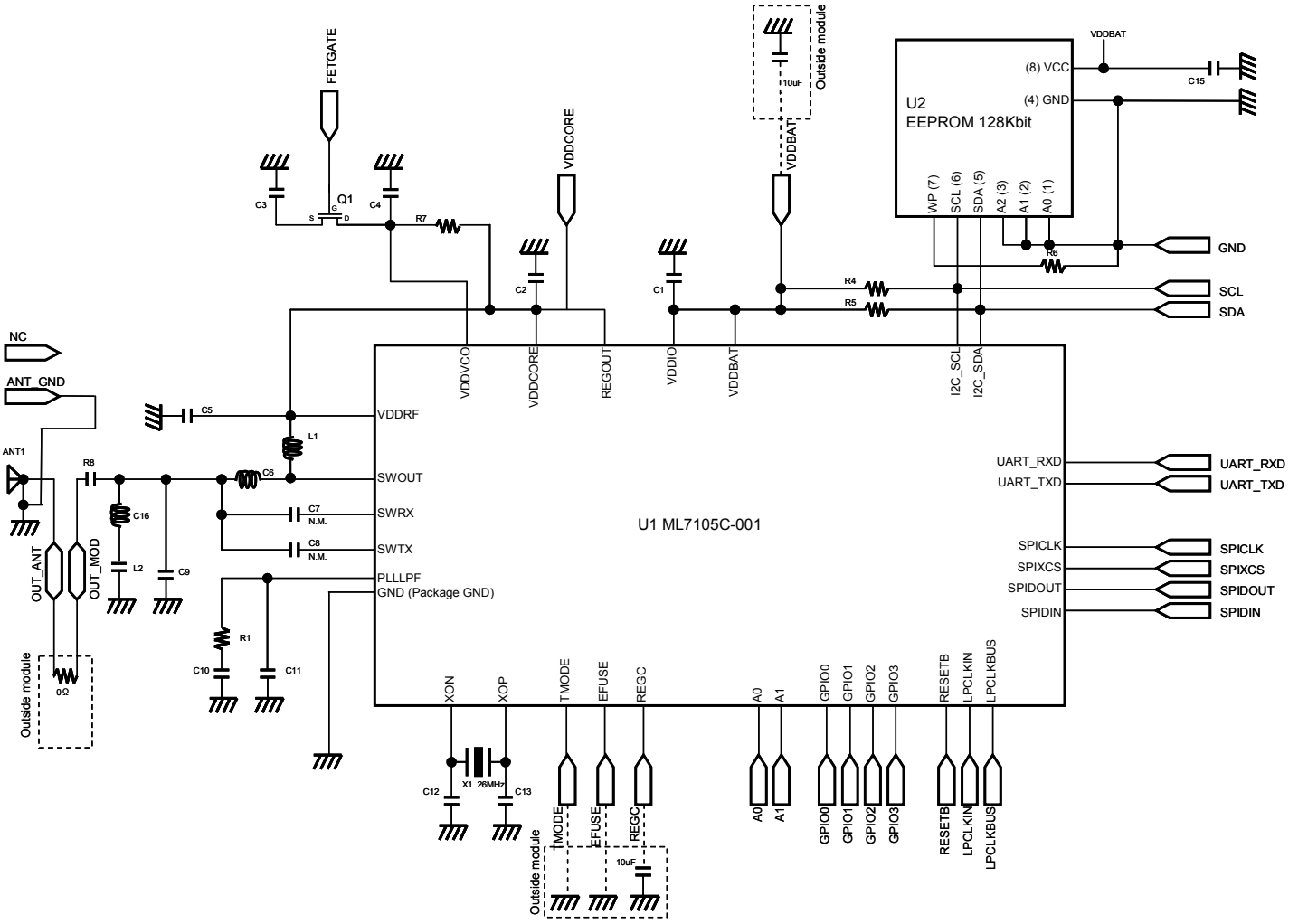
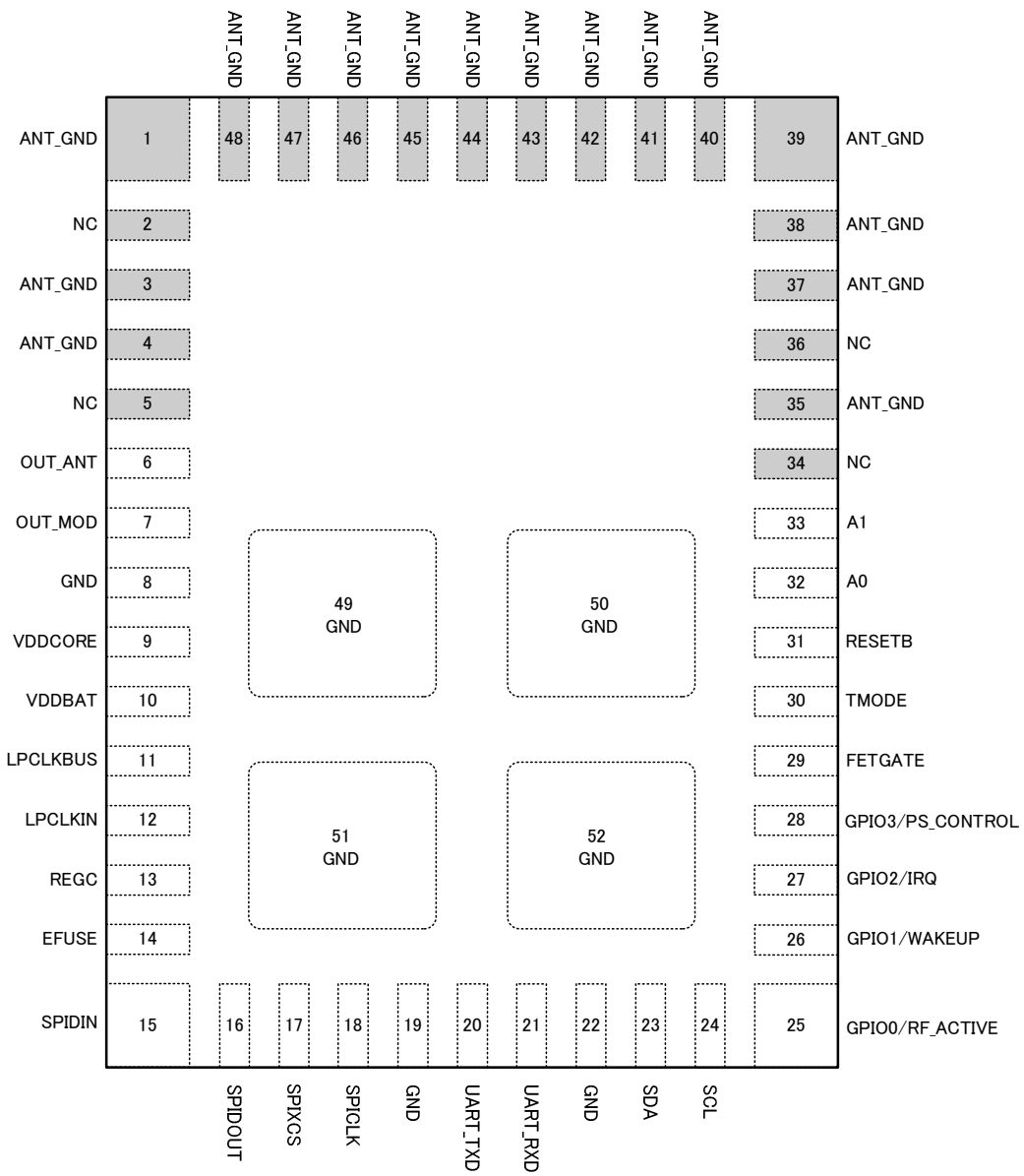
■Schematics


FETGATE
Q1
C3
C4
R7
VDDCORE
C2
C1
Outside module
10uF
VDDBAT
U2
EEPROM 128Kbit
(8) VCC
(4) GND
C15
WP (7)
SCL (6)
SDA (5)
A2 (3)
A1 (2)
A0 (1)
R6
GND
R4
R5
SCL
SDA
NC
ANT_GND
ANT1
C5
L1
R8
C6
C16
C7
N.M.
C8
N.M.
L2
C9
OUT_ANT
OUT_MOD
R1
C10
C11
0Ω
VDDRF
SWOUT
SWRX
SWTX
PLLLPF
GND (Package GND)
U1 ML7105C-001
VDDVCO
REGOUT
VDDIO
I2C_SCL
I2C_SDA
UART_RXD
UART_TXD
SPICLK
SPIXCS
SPIDOUT
SPIDIN
XON
XOP
TMODE
EFUSE
REGC
A0
A1
GPIO0
GPIO1
GPIO2
GPIO3
RESETB
LPCLKIN
LPCLKBUS
C12
X1 26MHz
C13
10uF

■Pin assignment



TOP VIEW

■Pin definitions

No	Pin Name	I/O	Ana/Dig	I/O type	Function
1	ANT_GND	---	---	---	Antenna GND（※Refer to PIN descriptions.）
2	NC	---	---	---	No connection（※Refer to PIN descriptions.）
3-4	ANT_GND	---	---	---	Antenna GND（※Refer to PIN descriptions.）
5	NC	---	---	---	No connection（※Refer to PIN descriptions.）
6	OUT_ANT	INOUT	ANA	---	Output from Antenna (to be connected to OUT_MOD by user's PCB)
7	OUT_MOD	INOUT	ANA	---	Output from Module (to be connected to OUT_ANT by user's PCB)
8	GND	---	GND	GND	GND
9	VDDCORE	---	PWR	VCC	Internally generated power supply,
10	VDDBAT	---	PWR	VCC	Power supply 1.8 to 3.6V, require 10uF capacitor.
11	LPCLKBUS	INOUT	ANA	DIRIO	Please use this pin open.
12	LPCLKIN	INOUT	ANA	DIRIO	Low Power clock input
13	REGC	OUT	ANA	DIRIO	REGOUT, require 10uF capacitor.
14	EFUSE	---	DIG	DIRIO	Control signal for EFUSE programming, fix to GND for normal usage
15	SPIDIN	IN	DIG	CMOS, IN	Data input for SPI slave
16	SPIDOUT	INOUT	DIG	CMOS, BiDIR	Data output for SPI slave
17	SPIXCS	IN	DIG	CMOS, IN	Chip select for SPI slave
18	SPICLK	IN	DIG	CMOS, IN	Clock input for SPI slave
19	GND	---	GND	GND	GND
20	UART_TXD	OUT	DIG	CMOS, OUT	Data TX port for UART
21	UART_RXD	IN	DIG	CMOS, IN	Data RX port for UART
22	GND	---	GND	GND	GND
23	SDA	INOUT	DIG	CMOS, BiDIR	SDA data port for I2C
24	SCL	INOUT	DIG	CMOS, BiDIR	SCL clock port for I2C
25	GPIO0/RF_ACTIVE	INOUT	DIG	CMOS, BiDIR	GPIO inout/RF_Active
26	GPIO1/WAKEUP	INOUT	DIG	CMOS, BiDIR	GPIO inout/WAKEUP
27	GPIO2/IRQ	INOUT	DIG	CMOS, BiDIR	GPIO inout/IRQ
28	GPIO3/PS_CONTROL	INOUT	DIG	CMOS, BiDIR	GPIO inout/external switch control (Q1) (To be connected to FETGATE by user's PCB.)
29	FETGATE	IN	DIG	---	Gate control Pin of internal FET (To be connected to PS_CONTROL by user's PCB.)
30	TMODE	IN	DIG	CMOS, IN	Test mode control, fix to GND for normal usage
31	RESETB	IN	DIG	CMOS, IN	Reset, low active
32	A0	IN	ANA	DIRIO	Analog Test Pin0
33	A1	IN	ANA	DIRIO	Analog Test Pin1
34	NC	---	---	---	No connection（※Refer to PIN descriptions.）
35	ANT_GND	---	---	---	Antenna GND（※Refer to PIN descriptions.）

36	NC	---	---	---	No connection（※Refer to PIN descriptions.）
37-48	ANT_GND	---	---	---	Antenna GND（※Refer to PIN descriptions.）
49-52	GND	---	GND	GND	GND

■PIN descriptions

I/O symbol
I_{RF} : RF input output pin
I : Digital input pin
I_{pd} : Digital input with pull-down resistor
I_{AH} : Analog High voltage input pin
I_{SH} : Low power clock input pin
X_{SH} : Low power clock oscillator pin
O_2 : Digital output pin with 2mA load capability
B_2 : Digital bidirectional pin with 2mA load capability
B_{2PU} : Digital bidirectional pin with 2mA load capability and pull-up resistor

●RF, Analog signals

#	Pin Name	Status/Value at reset	I/O	Active Level	Function
6	OUT_ANT		I_{RF}	---	Output from Antenna (to be connected to OUT_MOD by user's PCB)
7	OUT_MOD		I_{RF}	---	Output from Module (to be connected to OUT_ANT by user's PCB)
32	A0	Hi-Z	I_{AH}	---	Analog test pin0
33	A1	Hi-Z	$I_{AH,}$	---	Analog test pin1

●XO、LPXO signals

#	Pin Name	Status/Value at reset	I/O	Active Level	Function
11	LPCLKBUS	0V	X_{SH}	---	Please use this pin open.
12	LPCLKIN	I_{SH}	X_{SH}, I_{SH}	---	Low power clock input

●SPI signals

#	Pin Name	Status/Value at reset	I/O	Active Level	Function
15	SPIDIN	Input	I	---	SPI SLAVE Data input
16	SPIDOUT	Input	B_2	---	SPI SLAVE Data output
17	SPIXCS	Input	I	Low	SPI SLAVE Chip Select
18	SPICLK	Input	I	---	SPI SLAVE Clock

●UART signals

#	Pin Name	Status/Value at reset	I/O	Active Level	Function
20	UART_TXD	Output High	O_2	---	UART TXD output
21	UART_RXD	Input	I_{pd}	---	UART RXD input

●I2C signals

#	Pin Name	Status/Value at reset	I/O	Active Level	Function
24	SCL	Input	B2PU	---	I2C_SCL monitor pin.Please use this pin open.
23	SDA	Input	B2PU	---	I2C_SDA monitor pin. Please use this pin open.

●GPIO signals

#	Pin Name	Status/Value at reset	I/O	Active Level	Function
25	GPIO0 /RF_ACTIVE	Output Low	B2	---	GPIO inout/RF_ACTIVE output (default: RF_ACTIVE)
26	GPIO1 /WAKEUP	Input	B2	---	GPIO inout/WAKEUP input (default: WAKEUP)
27	GPIO2 /IRQ	Output High	B2	---	GPIO inout/IRQ output (default: IRQ)
28	GPIO3 /PS_CONTROL	Output Low	B2	---	GPIO inout/Control signal for external Switch (default: PS_CONTROL) (To be connected to FETGATE by user's PCB.)

● Miscellaneous signals

#	Pin Name	Status/Value at reset	I/O	Active Level	Function
31	RESETB	Input	I	Low	Reset input (Low = Reset)
14	EFUSE	---	---	---	E-Fuse writing voltage supply(Fixed to Low)
30	TMODE	Input	I	---	TESTMODE input (Fixed to Low)
29	FETGATE	Input	I	---	FET gate control input (To be connected to PS_CONTROL by user's PCB.)

●Regulator signal

#	Pin Name	Status/Value at reset	I/O	Active Level	Function
9	VDDCORE	---	---	---	Internally generated power supply. (Note)Don't short this pin.
13	REGC	1.2V 出力	---	---	Pin for de-coupling capacitor, require 10uF capacitor.

●Power supply and Ground

#	Pin Name	Status/Value at reset	I/O	Active Level	Function
10	VDDBAT	---	---	---	Power supply 1.8 to 3.6V,require 10uF capacitor.
8	GND	---	---	---	GND
19	GND	---	---	---	GND
22	GND	---	---	---	GND
49-52	GND	---	---	---	GND

●ANT_GND signals

#	Pin Name	Status/Value at reset	I/O	Active Level	Function
1,3-4 35 37-48	ANT_GND	---	---	---	Antenna GND pins. ANT_GND pins has to be connected to board, but not to be connected any components on board. （Note）The pins are connected to GND in the module, but please use this pins open.

●NC signals

#	Pin Name	Status/Value at reset	I/O	Active Level	Function
2,5 34,36	NC	---	---	---	NC pins has to be connected to board, but not to be connected any components on board. Please use this pins open.

●Unused pins

Followings are recommendation for unused pins.

#	Pin Name	Recommendation
2,5,34,36	NC	OPEN(NC pins has to be connected to board, but not to be connected any components on board.)
1,3-4,35 37-48	ANT_GND	Open(ANT_GND pins has to be connected to board, but not to be connected any components on board.)
11	LPCLKBUS	Open
14	EFUSE	Fix to 0V
15	SPIDIN	Fix to High
16	SPIDOUT	Fix to High
17	SPIXCS	Fix to High
18	SPICLK	Fix to High
20	UART_TXD	Open
21	UART_RXD	Fix to Low (See section for operating mode)
23	SDA	Open（Pull-up resistor in the module）
24	SCL	Open（Pull-up resistor in the module）
25	GPIO0/RF_ACTIVE	Open
26	GPIO1/WAKEUP	Fix to High or Low See section for operating mode
27	GPIO2/IRQ	Open
28	GPIO3/PS_CONTROL	To be connected to FETGATE by user's PCB.
29	FETGATE	To be connected to PS_CONTROL by user's PCB.
32	A0	Open
33	A1	Open

Remarks

If input pins are left open with High Impedance status, significant current consumption might be observed. All input pins have to be fixed high or low level to avoid such current consumption.

■Electrical Characteristics

●Absolute Maximum Rating

Item	Symbol	Condition	Rating	Unit
Power supply (*1)	V_{DDBAT}	Ta = –20 to +70 deg.C GND=0V	–0.3 to +4.6	V
Digital input voltage (*2)	V_{DIN}		–0.3 to V_{DD}+0.3	V
Digital output voltage (*3)	V_{DO}		–0.3 to V_{DD}+0.3	V
Analog HV IO voltage (*4)	V_{AH}		–0.3 to V_{DD}+0.3	V
Digital IO load current (*2)(*3)	I_{DO}		–10 to +10	mA
Analog IO current (*4)	I_A		–2 to +2	mA
Power Dissipation	P_D		T.B.D.	W
Storage temperature	T_{stg}	–	-40 to +85	deg.C

(*1) VDDBATpin
(*2) IO pins with I, I_{PD}, B_2 symbol in pin definition
(*3) IO pins with O_2,B_2 symbol in pin definition
(*4) IO pins with I_{AH}, $I_{SH,}$ $X_{SH,}$ symbol in pin definition

●Recommended Operating Conditions

Item	Symbol	Condition	Min	Typ	Max	Unit
Power Supply	V_{DD}	VDDBAT pin	1.8	3.3	3.6	V
Ambient Temperature	T_a	–	–20	+25	+70	°C
Rising time digital input pins	t_{IR1}	Digital input/inout pins	–	–	20	Ns
Falling time digital input pins	t_{IF1}	Digital input/inout pins	–	–	20	Ns
Load capacitance digital	C_{DL}	Digital output/inout pins	–	–	20	pF
Low Power Clock (32.768 kHz)	F_{LPCK1}	LPCLKIN pin	–250 ppm	32.768	+250 ppm	kHz
Low Power Clock Input Duty Ratio	D_{LPCK1}	External input from LPCLKIN, LPCLKBUS pin left OPEN	30	50	70	%
RF Channel frequency (*1)	F_{RF}	OUT_MOD pin	2402	–	2480	MHz
RF input level	P_{RFIN}	–	-70	–	-10	dBm

(*1) Frequency range F = 2402 + 2 x k [MHz] here k=0, 1,2,…,39.

●Current consumption

(Ta = 25 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Current Consumption	I_{DD1}	Deep Sleep state (External Low Power Clock)	–	0.8	–	uA
	I_{DD2}	Idle state	–	3	–	mA
	I_{DD3}	RF RX state	–	9	–	mA
	I_{DD4}	RF TX state（-6dBm）	–	9	–	mA
		RF TX state（0dBm）	–	10.9	–	mA

（note）Condition:Ta=25dec.C、VDDBAT=3.3V

●DC characteristics

(Ta = –20 to +70 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
H level Voltage Input	V_{IH1}	(*1) (*2) (*5)	V_{DD} X0.7	–	V_{DD}	V
L level Voltage input	V_{IL1}	(*1) (*2) (*5)	0	–	V_{DD} X0.3	V
LPCLKIN pin H level Voltage Input	V_{IH2}	(*3)	1	–	V_{DD}	V
LPCLKIN pin L level Voltage input	V_{IL2}	(*3)	0	–	0.3	V
H level Voltage Output	V_{OH}	I_{OH} = –2mA (*4) (*5)	V_{DD} × 0.75	–	V_{DD}	V
L level Voltage Output	V_{OL}	I_{OL} = 2mA (*4) (*5)	0	–	V_{DD} × 0.25	V
Input pin capacitance	C_{IN}	F=1MHz (*1) (*2) (*4) (*5)	–	8	–	pF

(*1) IO pins with I symbol in pin definition
(*2) IO pins with I_{PD} symbol in pin definition
(*3) IO pins with I_{SH} symbol in pin definition
(*4) IO pins with O_2 symbol in pin definition
(*5) IO pins with B_2 symbol in pin definition

●RF Characteristics

(Ta = –20 to +70 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
TX						
Maxium TX power	P_{OUT}	0dBm setting	–	0	–	dBm
Centre Frequency tolerance	F_{CERR}	Master Clock tolerance < 40 ppm	–40	–	40	ppm
Modulation data rate	D_{RATE}	–	–	1	–	Mbps
Modulation index	F_{IDX}	–	0.45	0.50	0.55	–
Bandwidth-bit rate products BT	BT	GFSK	–	0.5	–	–
RX						
Receiver Sensitivity	P_{SENS}	PER =30.8% (*1)	–	-85	-70	dBm
Maximum input level(*2)	P_{RXMAX}	PER=30.8% (*1)	–	–	-10	dBm
RSSI detection range	$P_{RSSIMAX}$	Upper	-50	–	–	dBm
	$P_{RSSIMIN}$	Lower	–	–	-80	dBm

(*1) PER=30.8% is corresponding to BER=0.1%

(*2) Condition: Ta = 25℃、VDDHV = 3.3V

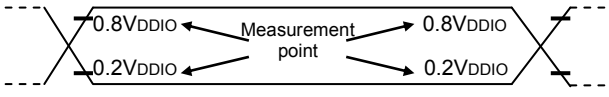
●SPI interface

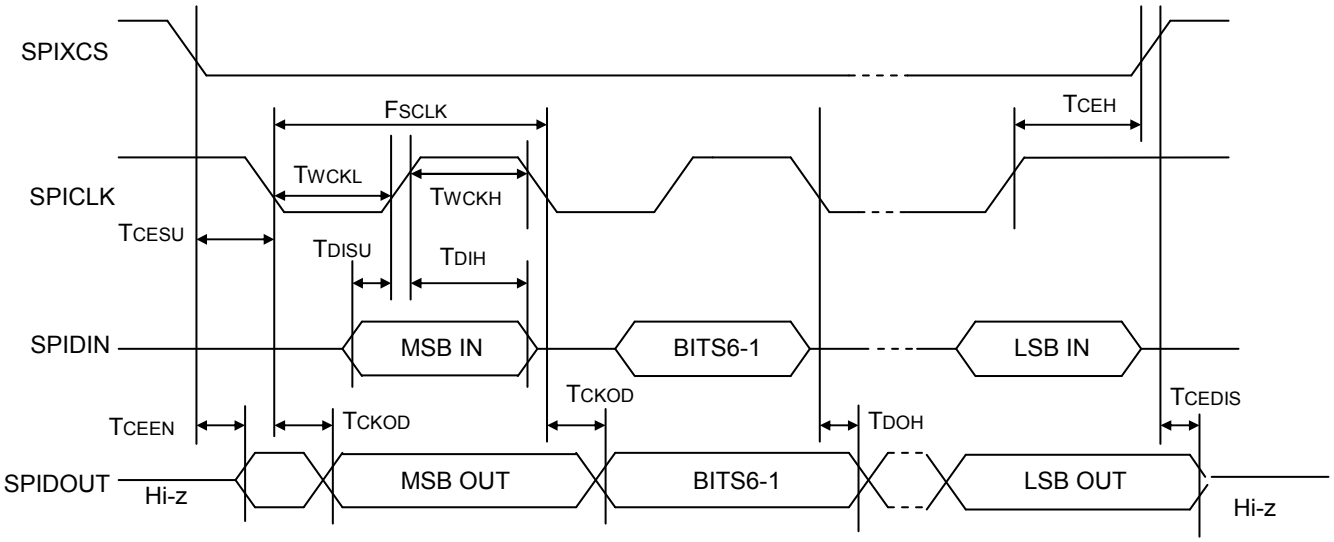
(Ta = –20～+70°C)

Item	Symbol	Condition	Min	Typ	Max	Unit
SPICLK Clock Frequency	F_{SCLK}	Load capacitance CL=20pF	16.384	32.768	1625	kHz
SPIXCS input setup time	T_{CESU}		1/Fsclk	–	–	ms
SPIXCS input hold time	T_{CEH}		1/Fsclk	–	–	ms
SPICLK high pluse width	T_{WCKH}		250	–	–	ns
SPICLK low pluse width	T_{WCKL}		250	–	–	ns
SPIDIN input setup time	T_{DISU}		5	–	–	ns
SPIDIN input hold time	T_{DIH}		250	–	–	ns
SPICLK output delay time	T_{CKOD}		–	–	250	ns
SPIDOUT output hold time	T_{DOH}		5	–	–	ns
SPIXCS output enable delay time	T_{CEEN}		0	–	300	ns
SPIXCS output disable delay time	T_{CEDIS}		150	–		ns

Remarks: All timing specification is defined at V_{DDIO} x 20% and V_{DDIO} x 80%
SPIXCS input setup/hold time have to be at least 1cycle of SPICLK clock frequency

Measurement point



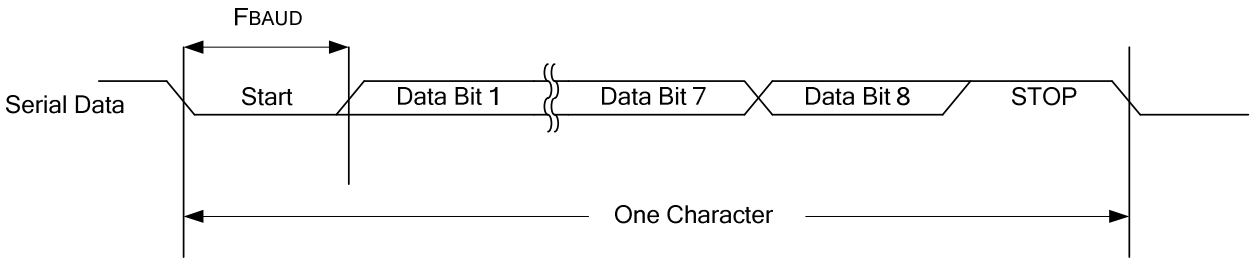


(*) SPIDOUT becomes Hi-Z input when SPIXCS is High.So please insert the pull-up or pull-down resister .

●UART interface

(Ta = –20 to +70 deg.C)

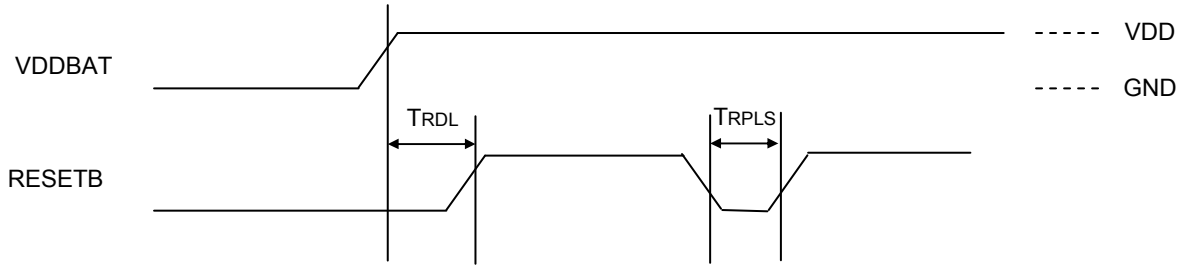
Item	Symbol	Condition	Min	Typ	Max	Unit
Baud Rate	FBAUD	Load capacitance CL=20pF	–	57600	–	bps(Hz)



●Reset operation

(Ta = –20 to +70 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
RESETB propagation delay time (Power on)	TRDL	Start supplying power (VDDBAT)	20	–	–	ms
Reset pulse width	TRPLS	RESETB pin	1	–	–	us



Power on reset function

Reset function from RESETB pin

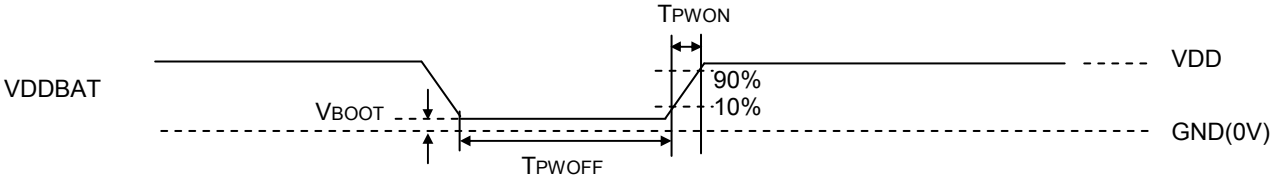
It is possible to reset internal circuit by asserting RESETB after power supply is on.

It is possible to reset internal circuit by same way even if it is not power sequence. Internal circuit will move to normal state after oscillation circuit become stable by clock stabilizing circuit after reset function.

●Power on

(Ta = –20 to +70 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
VDD pin rising time	TPWON	While power on VDD pins (VDDBAT)	0.2	1	5	ms
Power off Time	TPWOFF	VDD pins(VDDBAT)	10	–	–	ms
Initial power level	VBOOT	VDD pins(VDDBAT)	–	–	0.3	V



■Operating mode

Following 3 operating modes are available to use

BACI Mode: Application mode using SPI-SLAVE interface
HCI Mode: HCI mode (Bluetooth LE standard compliant) using UART interface.
RAM Mode: Function extention mode downloading user program to internal memory

■Operating mode configuration

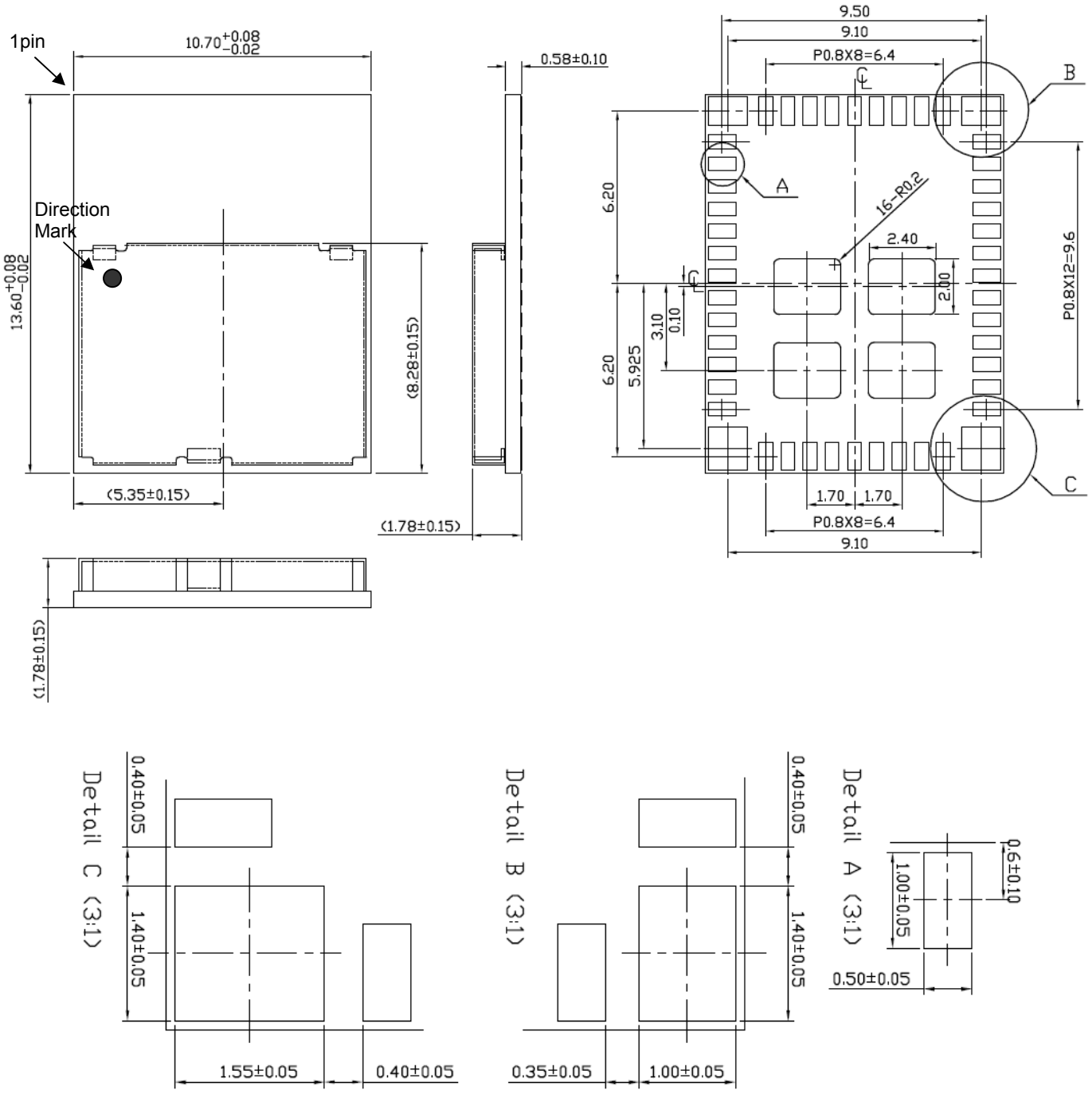
Configuration of operating mode will be done by pin status shown in table below. The symbol “X“ is don’t care, it has to be used as normal function. When configure operating mode, reset has to be issued.
RAM mode and Debug mode is distinguished by configuration parameter.

Operating mode	Pin confitions
	UART_RXD
BLI Mode	Low
HCI Mode(*1)	High
RAM Mode	X

(*1)Please fix wakeup pin to low level when using in HCI mode.

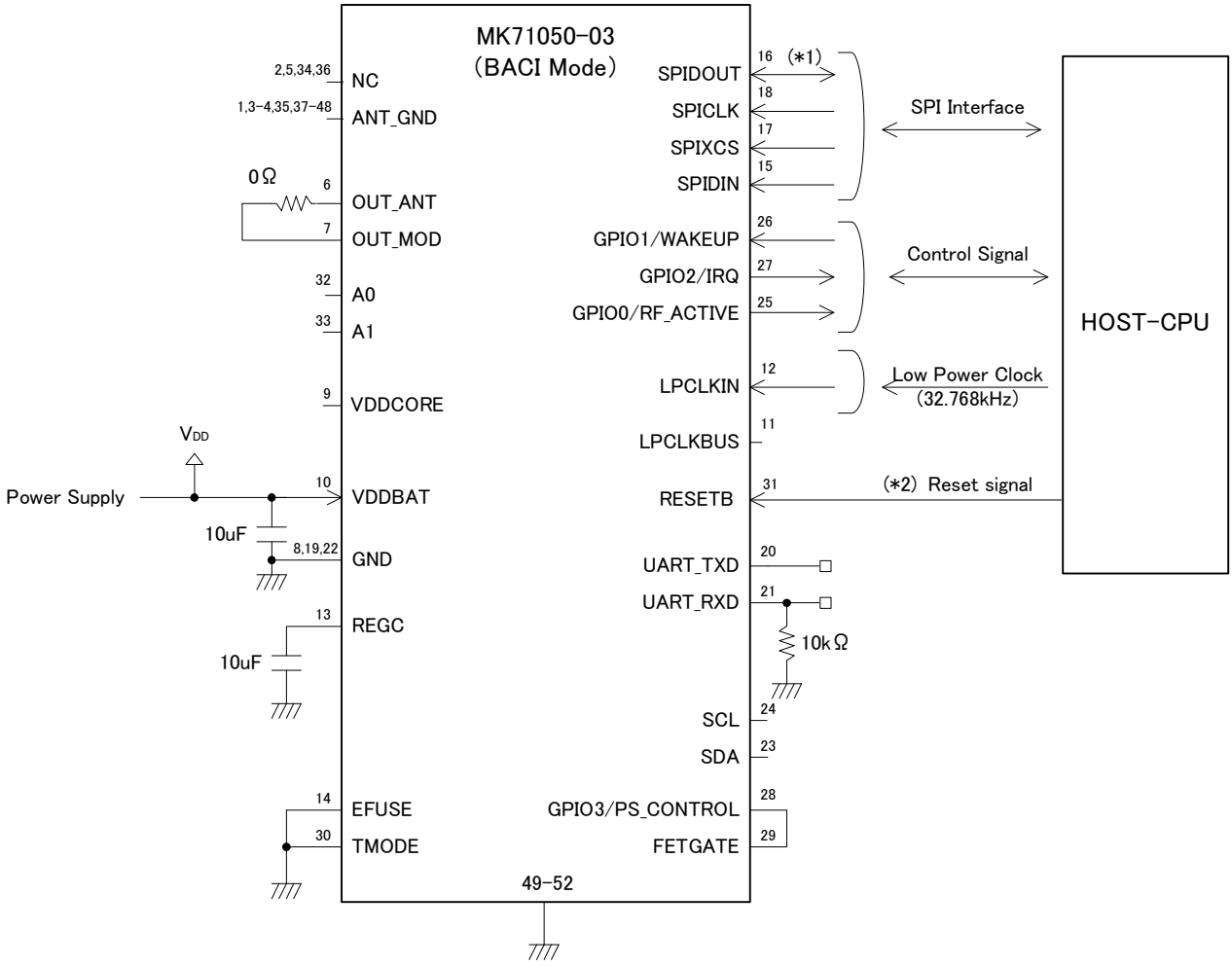
Please refer to ML7105C-001 data sheet and associtated documentation for more detail.

■Module dimension



Unit:mm

■Application example

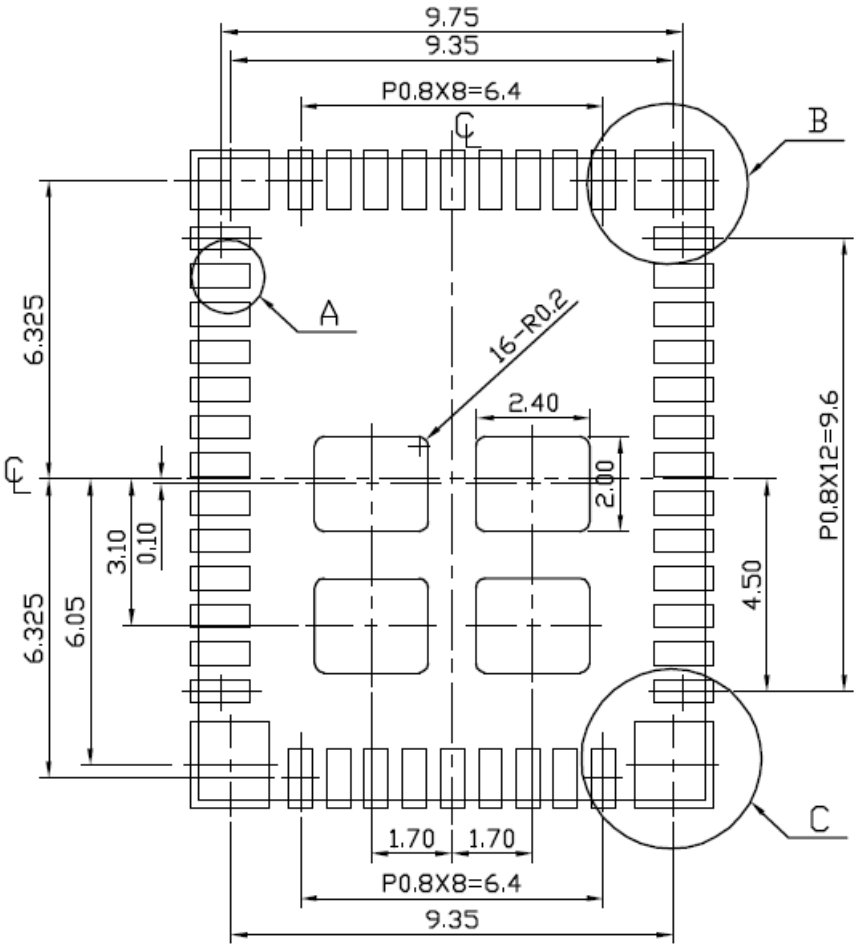


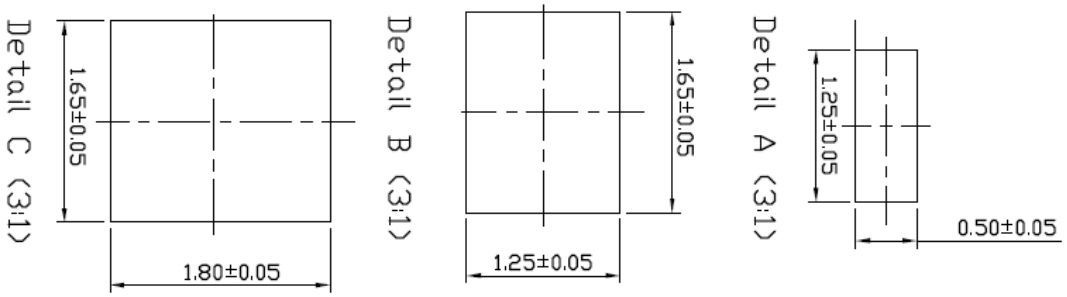
(*1) SPIDOUT becomes Hi-Z input when SPIXCS is High.So please insert the pull-up or pull-down resister .

(*2) Please be careful to satisfy the RESETB propagation delay time(T_{RDL}) .
And if the state of reset signal is undefined after power on reset of HOST-CPU , please insert the pull-up or pull-down resistor.

■Appendix

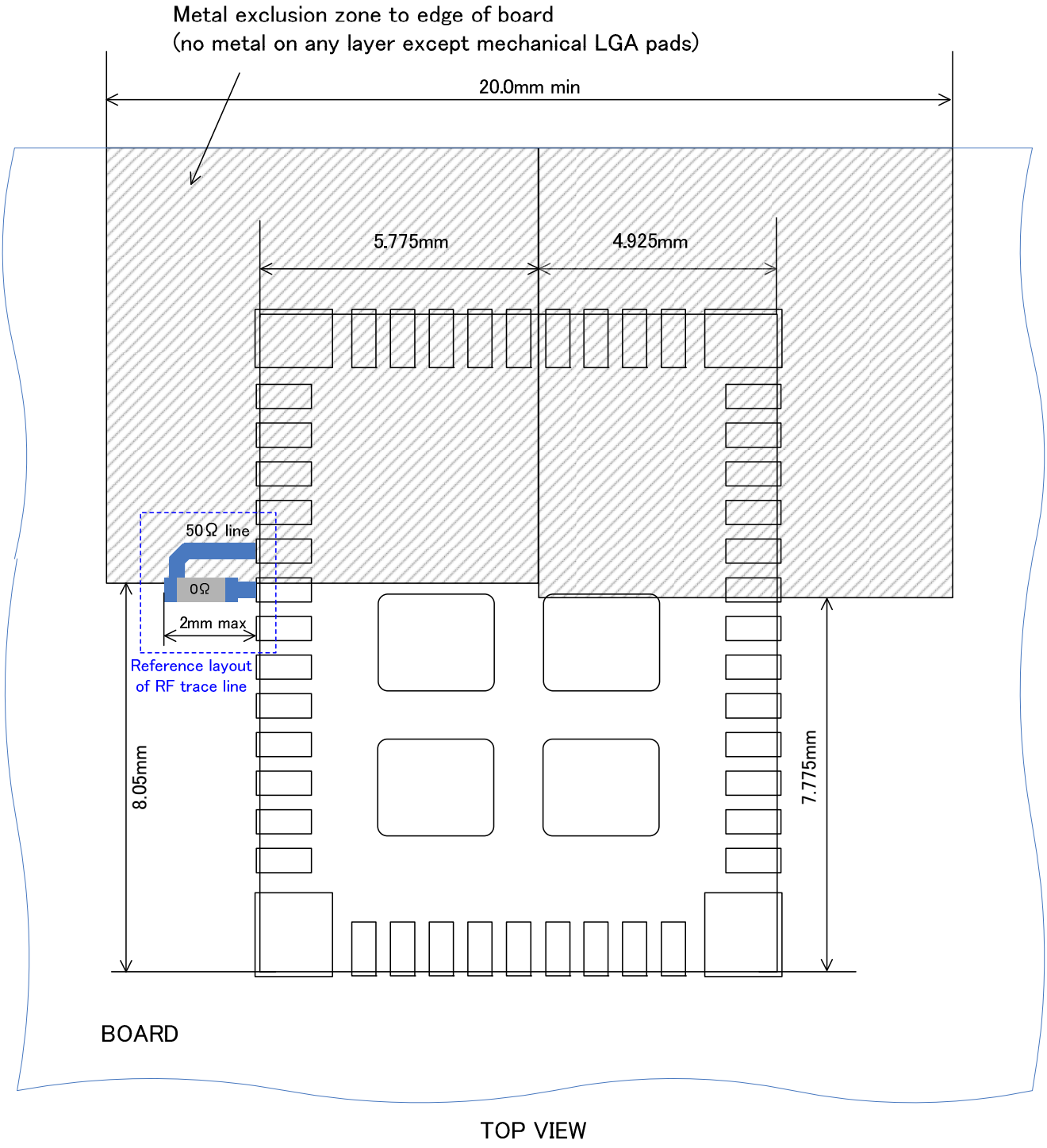
●PCB Land Pattern





Unit:mm

●Metal Keep-Out Area / Reference layout of RF trace line



TOP VIEW

●Radio certitication

MIC JAPAN(certification no:006-000238）
MK71050-03 complies with MIC JAPAN radio certification.(certification no:006-000238)

FCC（FCC ID: 2ACIJ71050-3）
This device complies with Part 15 of the FCC Rules.
Operation is subject to the following two conditions:
(1)this device may not cause harmful interference, and (2)this device must accept any interference received, including interference that may cause undesired operation.

The regulatory label on the final system must include the statement: “Contains FCC ID: 2ACIJ71050-3" or using electronic labeling method as documented in KDB 784748.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.
The antenna used for this transmitter must not be collocated or operating in conjunction with any other antenna or transmitter within a host device, except in accordance with FCC multi-transmitter product procedures.

The final system integrator must ensure there is no instruction provided in the user manual or customer documentation indicating how to install or remove the transmitter module except such device has implemented two-ways authentication between module and the host system.

OEM Responsibilities to comply with FCC Regulations
This module has been certified for integration into products only by OEM integrators under the following condition:
- The transmitter module must not be colocated or operating in conjunction with any other antenna or transmitter.

As long as the conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

IMPORTANT NOTE:
In the event that any of these conditions can not be met (for example the reference trace specified in this manual, or use of a different antenna), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

CE（R&TTE）
MK71050-03 complies with the radio test requirements (EN 300 328 V1.8.1) ,which is based on the R&TTE Directive (1999/5/EC).
EMC and Safety test that is required for the CE marking should be done in the final end-product.

■Caution

When implementing this product to double-sided printed board,please do not implement this product for the first time reflow side.(Opposite side reflow is prohibited due to module weight.)

■Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDK71050-03-01	May,01,2014	–	–	Preliminary edition 1
PEDK71050-03-02	May,28,2014	3	3	Deleted 1 Pin Mark.
		8	8	Storage temperature [OLD]-40～+125℃ → [New]-40～+85℃
		14	14	Added 1pin direction and direction Mark.
PEDK71050-03-03	Jul,03,2014	8	8	Deleted Power Dissipation.
PEDK71050-03-04	Jul,17,2014	3,5,6,15	3,5,6,15	Name changed. [OLD]G1～G4 [New]49pin～52pin
		14	14	Module dimension is updated.
		15	15	Added the note about reset signal.
PEDK71050-03-05	Nov,14,2014	1	1,18	Added the description of Radio certification.
		-	18	Caution was added.
		14,16	14,16	Unit:mm was added.
		4-5	4-5	Changed the explanation of LPCLKBUS.
		10	10	Changed the condion and specification of Tx Power.
PEDK71050-03-06	Dec,15,2014	17	17	Added the reference layout of RF trace line.
		18	18	Added the note of FCC certification.

NOTES

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