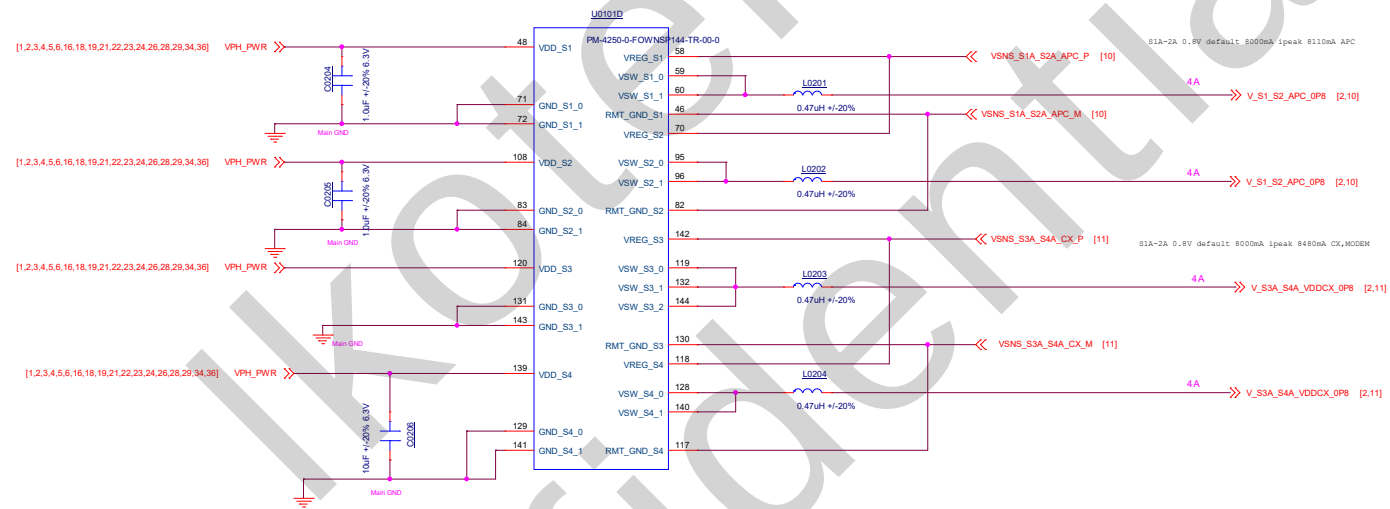
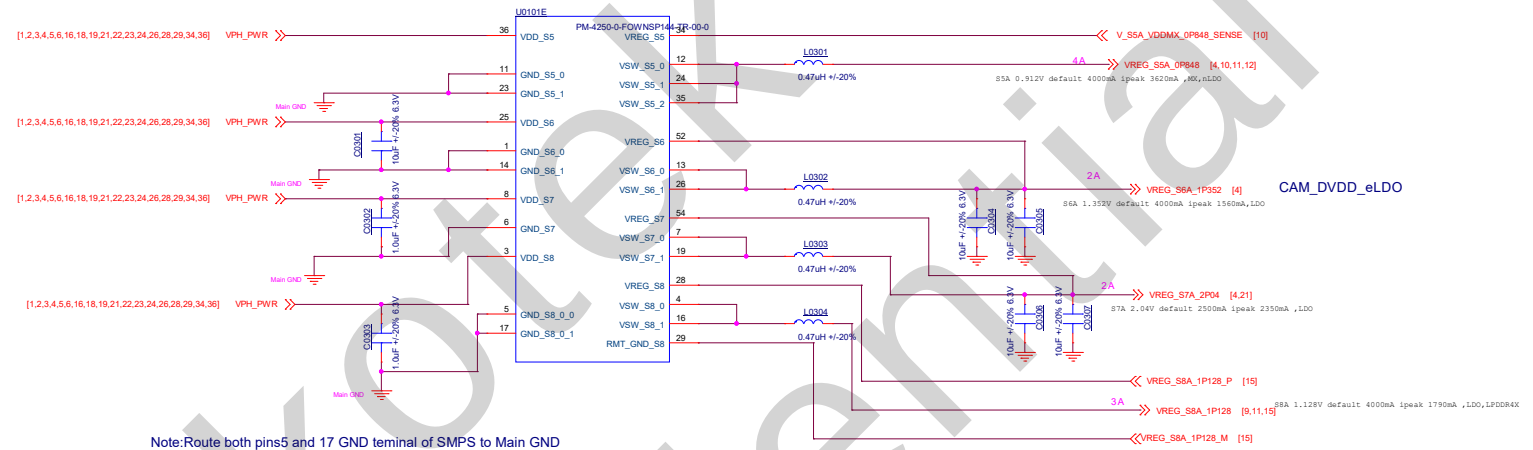
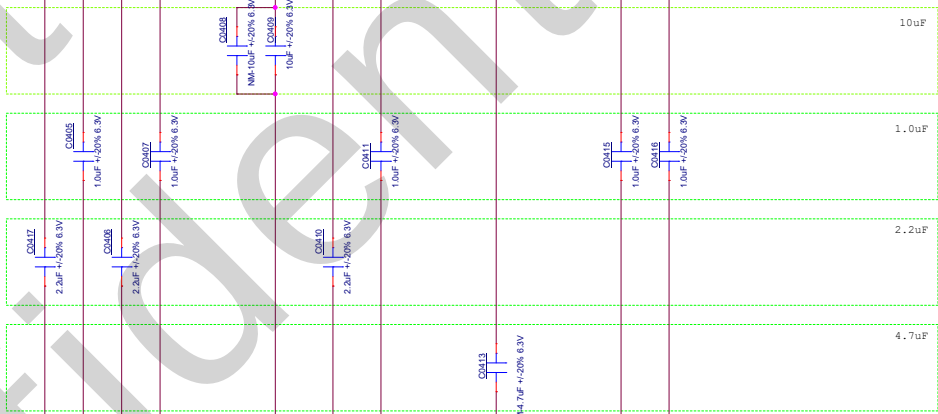
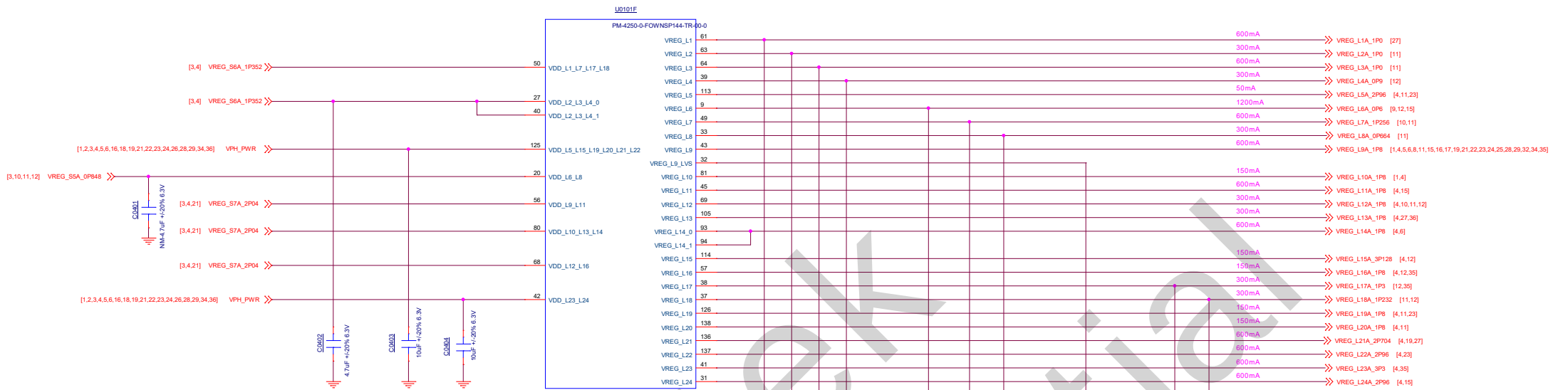
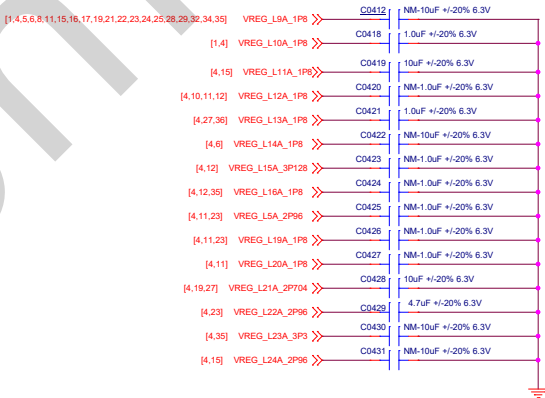


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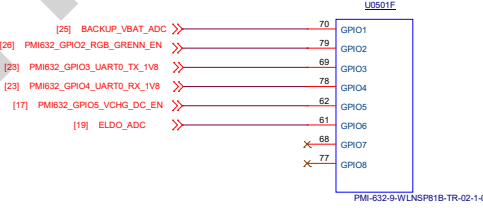
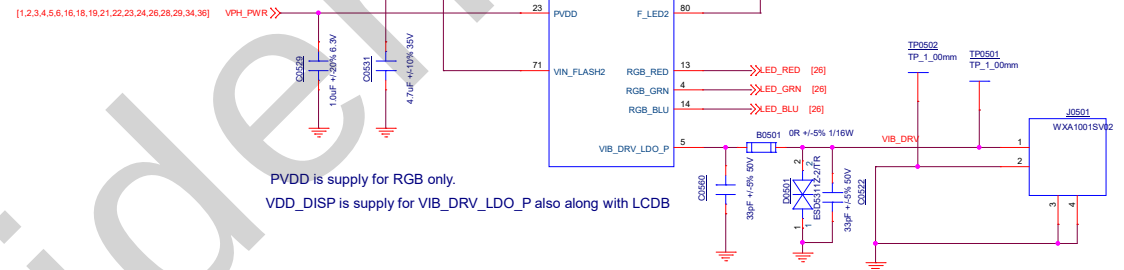
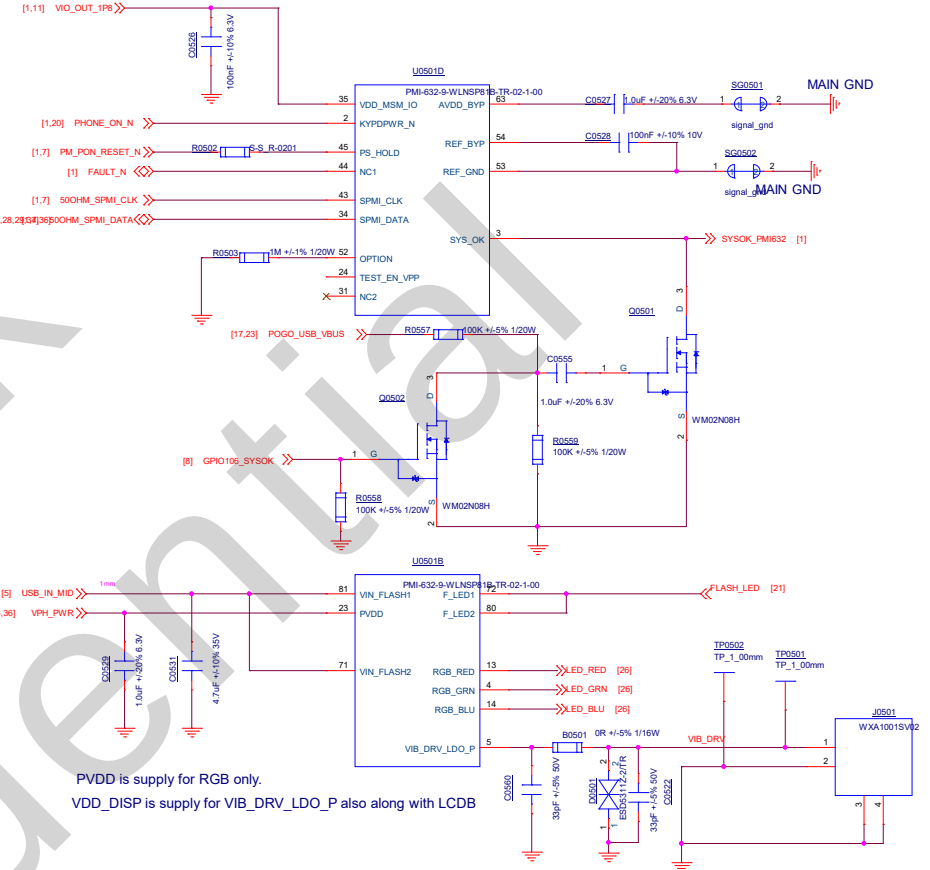
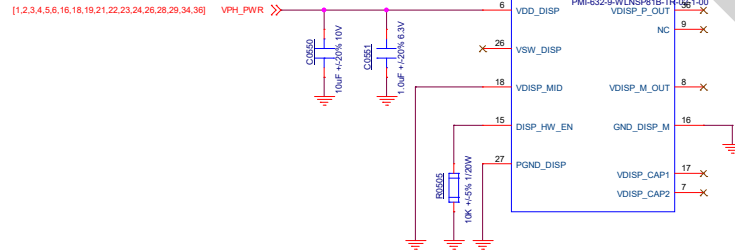
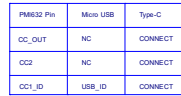


Rated current		DEFAULT ON	Expected use
B1	0.8V/4000mA	Y	AFC0_AFC1
B2	0.8V/4000mA	Y	AFC0_AFC1
B3	0.8V/4000mA	Y	CK_HES
B4	0.8V/4000mA	Y	CK_HES
B5	0.856V/4000mA	Y	MX, EBI_VDDIO, WCSS_MX, LPDDR4X_VDDQ (Subreg), WCSS_CK (Subreg)
B6	1.322V/2000mA	Y	RV sub-regulation
B7	2.04V/2000mA	Y	RV sub-regulation
B8	1.123V/3000mA	Y	1V sub-regulation, LPDDR4X_VDD2, SDR_VDDPX_1
L1	1.2V/600mA	N	QIM(1,2), QDS(1,2), SDR(1,2)
L2	1.0V/300mA	N	SDR(A1V)
L3	1.0V/600mA	Y	SDR(D1V)
L4	0.928V/350mA	Y	BB1PLL (0.93 V), USB2 (ADPP), USB3 (ADPP), QLINP, QREF, MIPI_DS1, UFS (0.9)
L5	2.95V/50mA	Y	PK2
L6	0.924V/1200mA	Y	LPDDR4X_VDDQ (0.8), VDDIO_EBT, VDDIO_CK_EBT
L7	0.928V/600mA	Y	USB 0.9 V
L8	0.664V/200mA	Y	VDD_WCSS_CK (0.73)
L9	1.8V/600mA	Y	LPDDR4X_VDD1 (1.8), VDD_PX3, VDD_PX7, WCD (1.8 V), WCN (1.8 V), Sensors (1.8 V), RFFE (1.8 V), WSA (1.8 V)
L10	1.8V/150mA	Y	USB2 (1.8 V), USB3_1 (1.8 V), QFPROM (1.8 V), UFS (1.8 V), VDDPX_11
L11	1.8V/600mA	Y	EMMC1_VDDQ (1.8 V), UFS (1.8 V)
L12	1.8V/300mA	Y	Camera sensors (1.8 V), USB_RxDriver, MIPI_VDDIO (1.8 V)
L13	1.8V/300mA	N	SDR (1.8 V), QPM (1.8 V), QDM (1.8 V)
L14	1.8V/600mA	N	WCD_VDD_RUCK (1.8 V)
L15	3.128V/150mA	Y	USB3 (3.1)
L16	1.8V/150mA	N	WCN (1.8 V), WCSS_PLL
L17	1.304V/300mA	N	WCN (1.3 V), WCSS_ADC_DAC (1.3 V)
L18	1.232V/350mA	Y	EBT_PLL (1.23), MIPI_DS1, MIPI_DS2 (1.23), VDDPX_10
L19	1.8V/150mA	N	UIM2 (1.8), PK5
L20	1.8V/150mA	N	UIM2 (1.8), PK6
L21	2.704V/600mA	N	ABDIV_BW, GAT (2.7), RF_Switch
L22	2.94V/600mA	Y	MEM_SD_NMC_VDD (2.96)
L23	3.304V/600mA	N	WCN (3.3)
L24	2.96V/600mA	Y	EMMC1_VCC (2.96)/UFS_MEM (2.96)



LDOs L5/L9/L10/L12/L13/L14/L15/L16/L19/L20/L21/L22/L23/L24 are Pseudo-capless LDOs,so DNI their decaps
insert the 10uF Load cap for VREG_L9A for spec compliance

NOTE1: Dedicated via to main ground plane/CAD
NOTE 2: Place Near to the IC Pin/CAD
NOTE 3: VBAT1 SNS M VBAT1 SNS P route as kelvin sense/VBAT1_SNS_M should have a dedicated route to battery connector negative sense/CAD
NOTE 4: TVSS1 OVP are to be placed near to USB connector/CAD
NOTE 5: Trace from VBAT1 to the cap, and cap to main GND plane with a dedicated via/Avoid routing VBAT1 trace directly under SW_CH3 trace to avoid coupling/CAD
NOTE 6: Place cap as close as possible to the USB_IN AUSB_MID cap respectively/Connect bottom of USBIN cap to bottom of USB_M cap/DN cap/DN NOT connect with any other ground

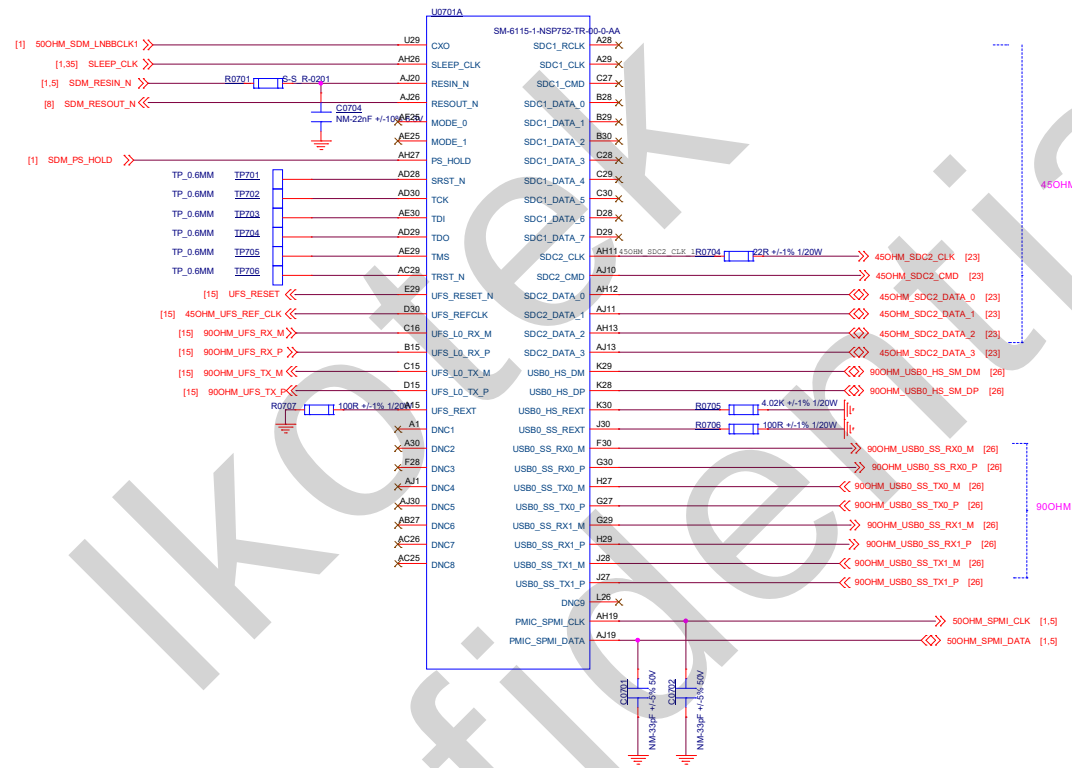


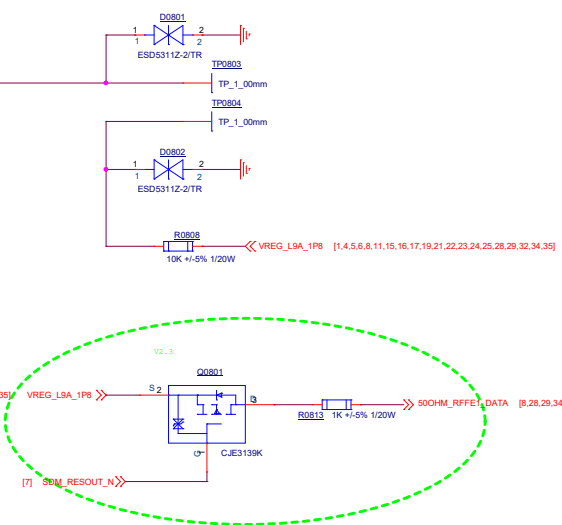
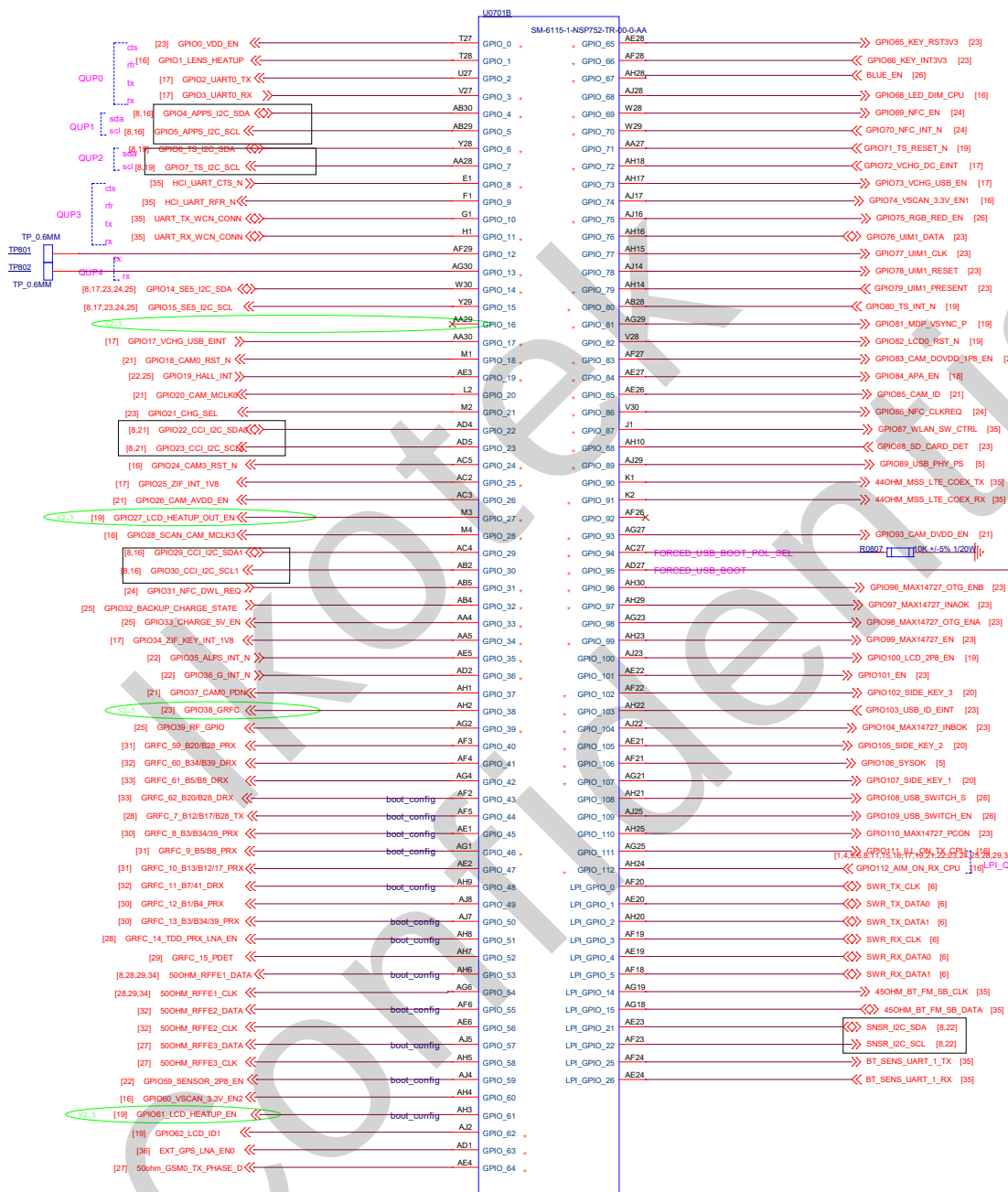
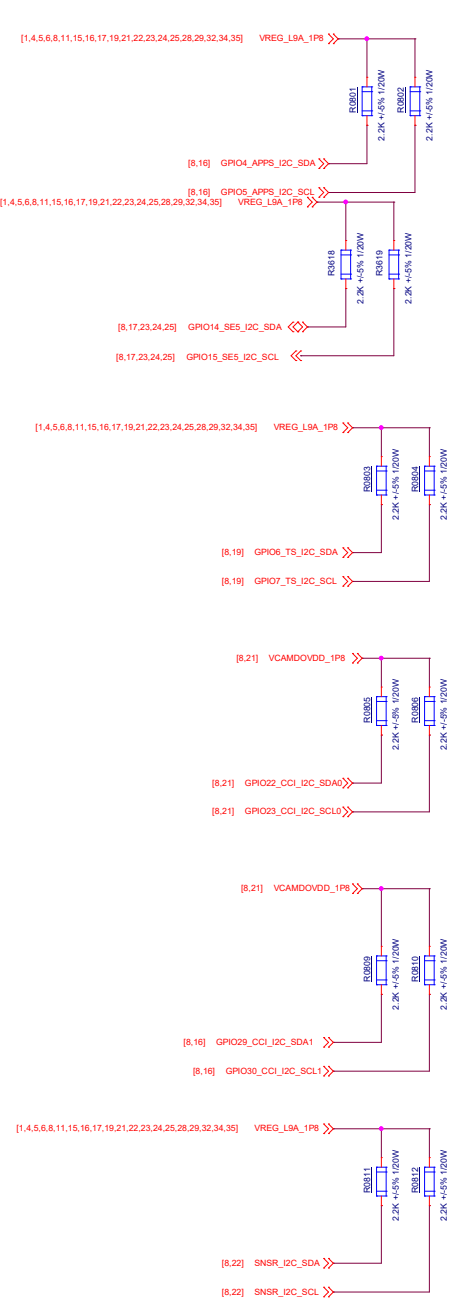
Layout Note: VDISP_CAPx
Place fly cap as close to the pin as possible.
Avoid routing VDISP_CAP1 trace under VDISP_M_OUT.

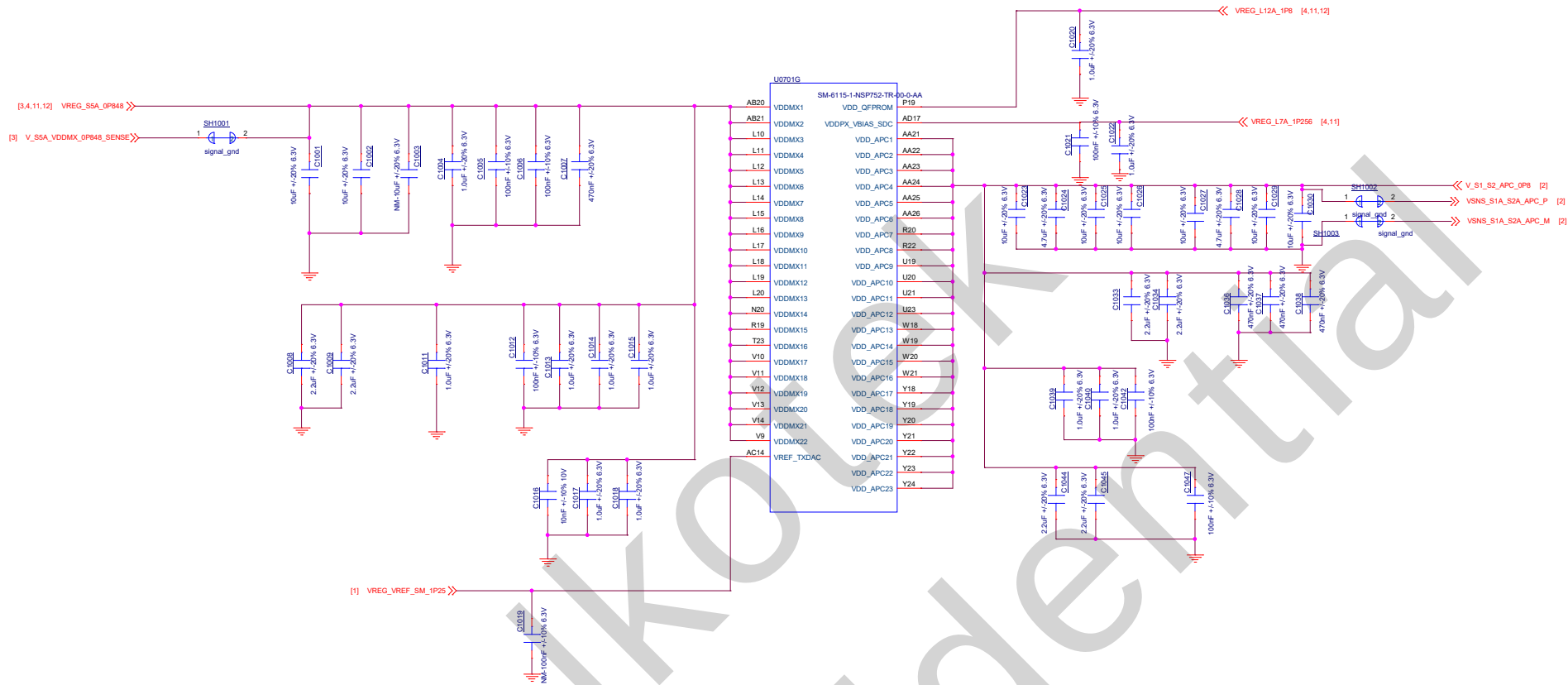
Layout Note: DISP_HW_EN
This signal is used for "Display Tap to Wake"
If unused in HW, this pin should be connected to GND

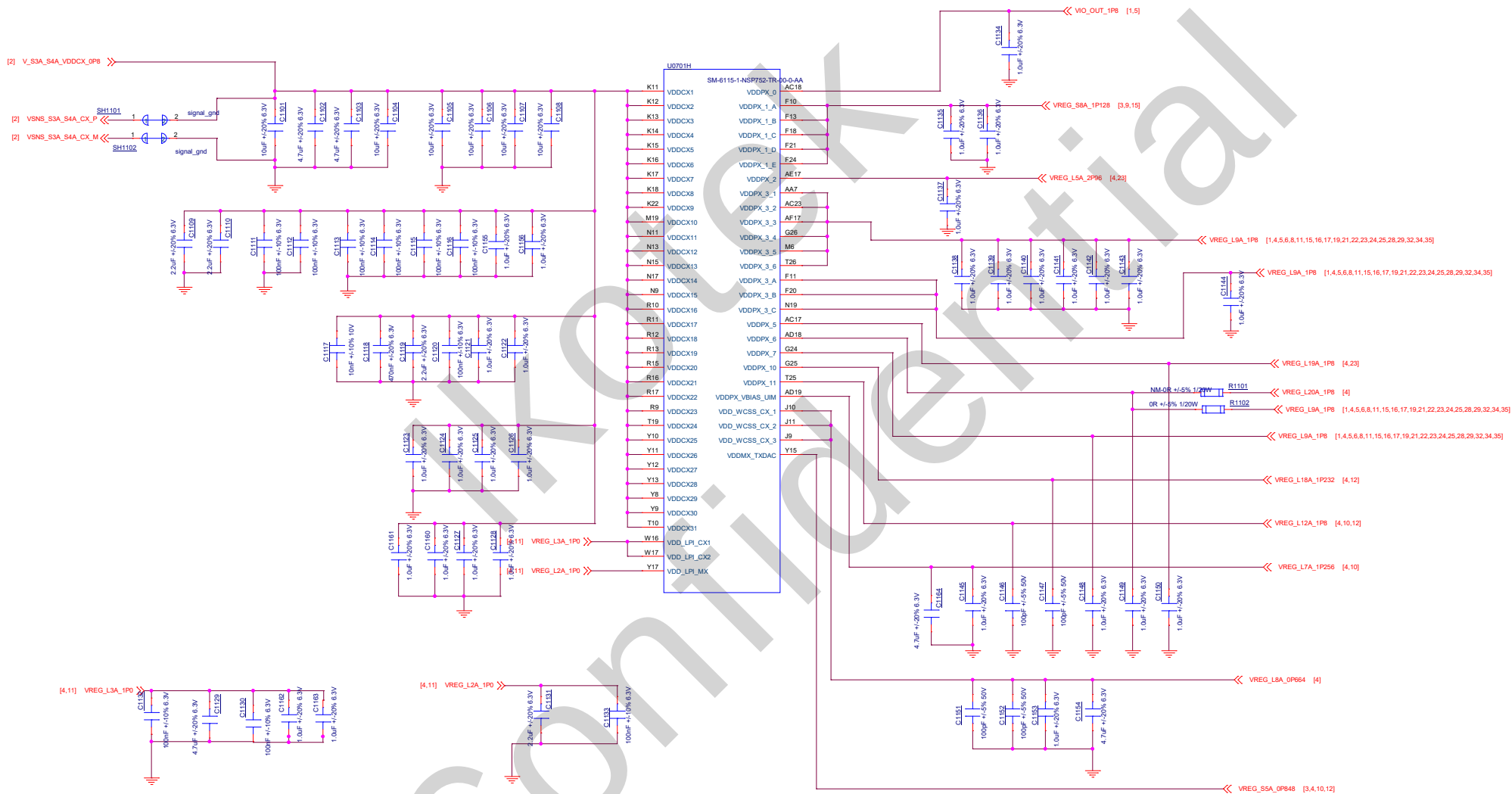
GPIO1_MUX (Mv)	FMS1 (Output mode) / TypeC_CONN_THERM_SNS / MSMNMIC_THERM
GPIO2 (Mv)	SMB_EN / H/RED (SRK required) / Fmsd 10nm)
GPIO3_MUX (Mv)	Skin_Therm_Sns / FLASH_THERM_SNS / VSYNC
GPIO4_MUX (Mv)	SMB_THERM_SNS / Flash_Strobe
GPIO5 (Lv)	I2C_1RQ (Output) / FMS2 (Output) /Flash_Strobe
GPIO6 (Lv)	WLED_PWM / CLK_IN_19M2
GPIO7_MUX (Lv)	SMB_VCHD_P / VSYNC
GPIO8_MUX (Lv)	FMS2 (Output) / SMB_VCHD_M

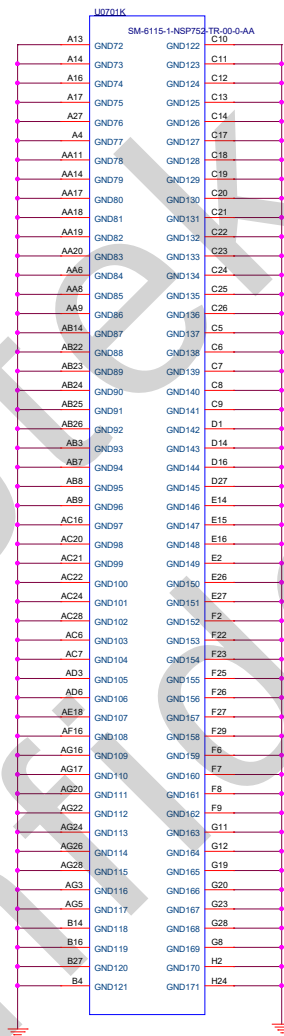
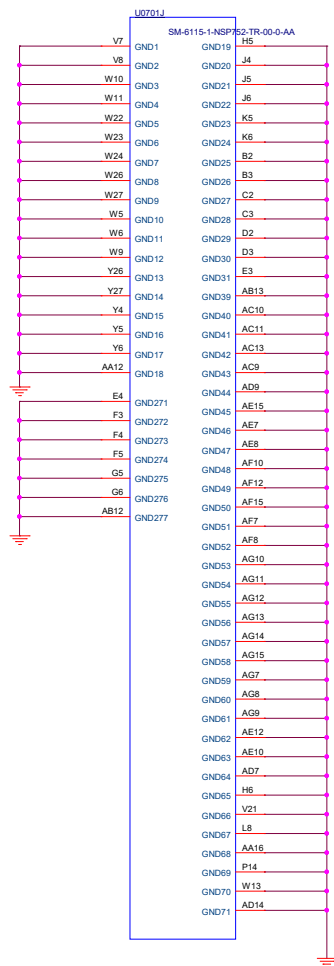
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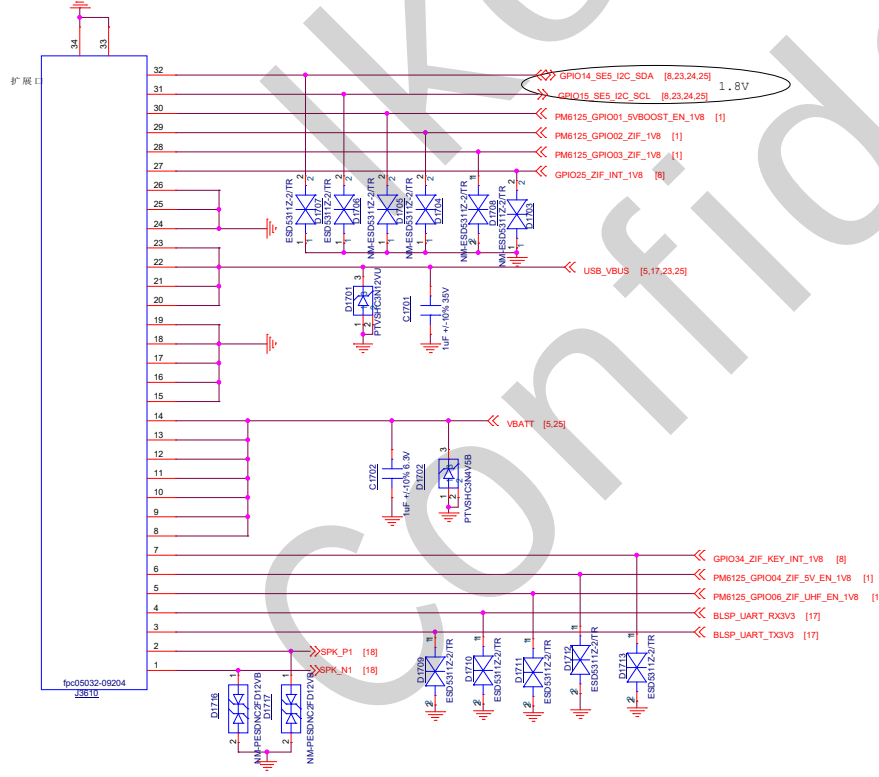
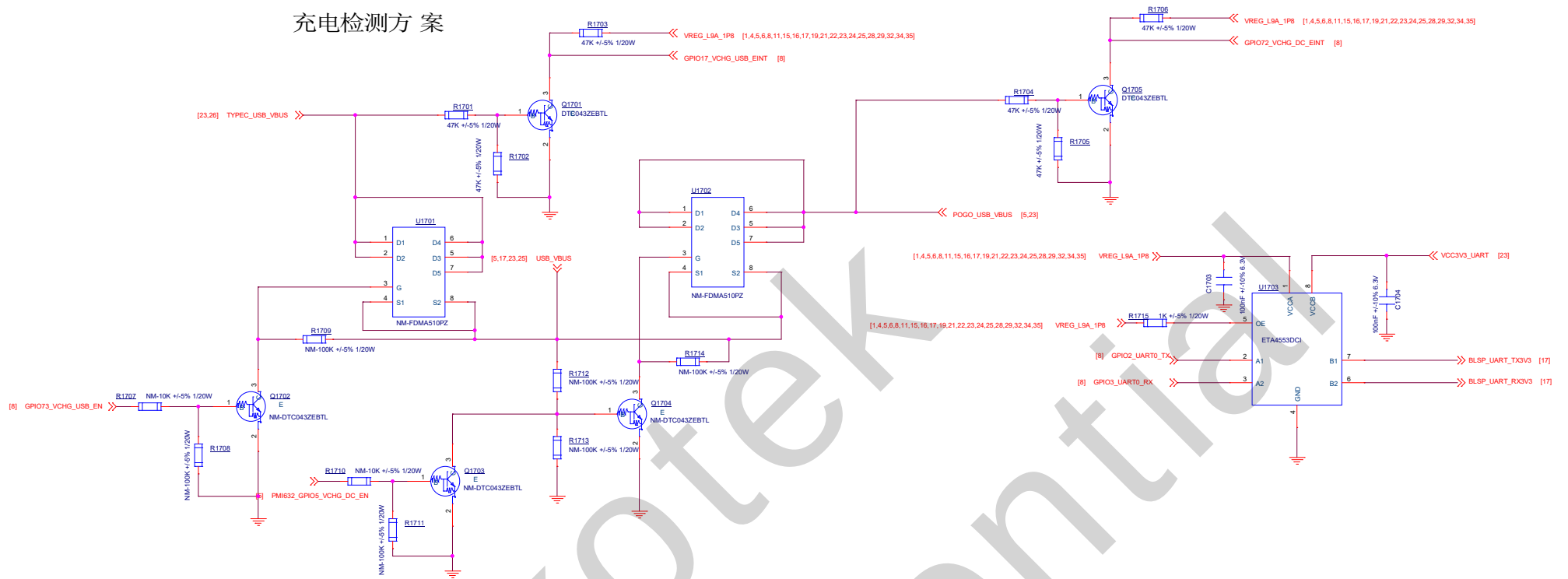








充电检测方案

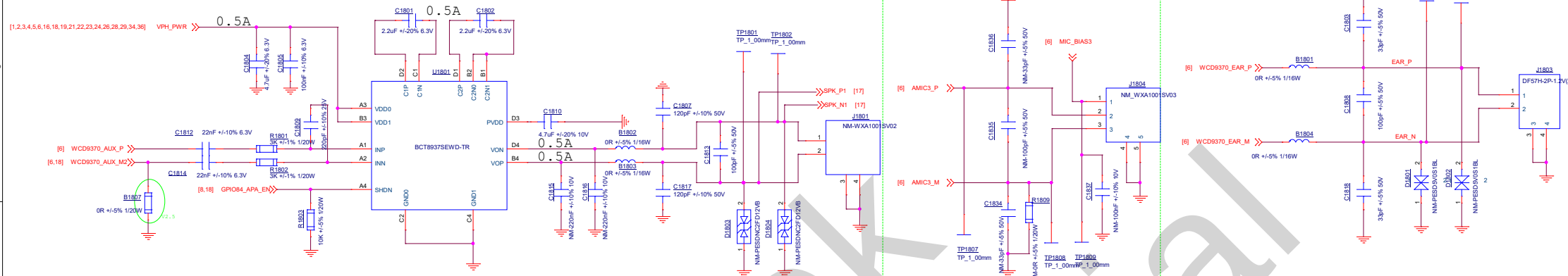


AUDIO PA1

Audio PA1

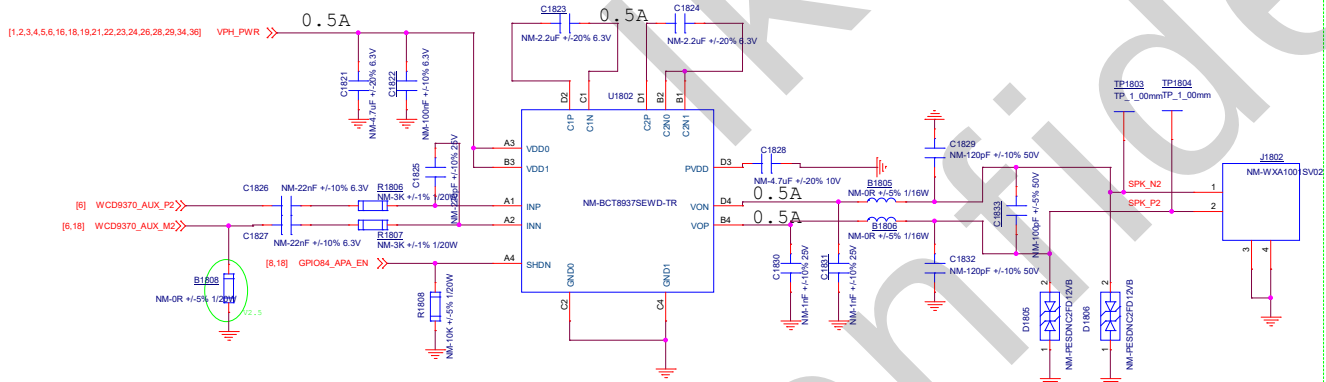
Main MIC nearby codec

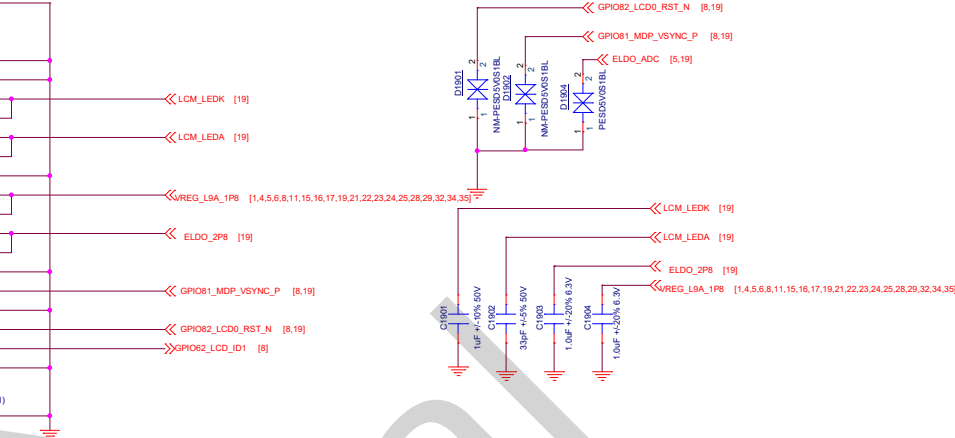
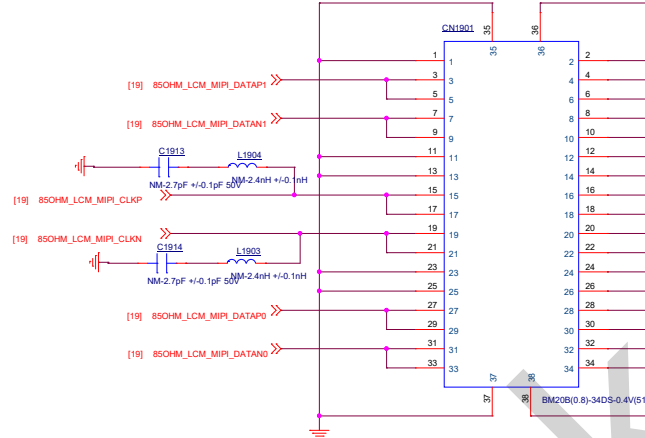
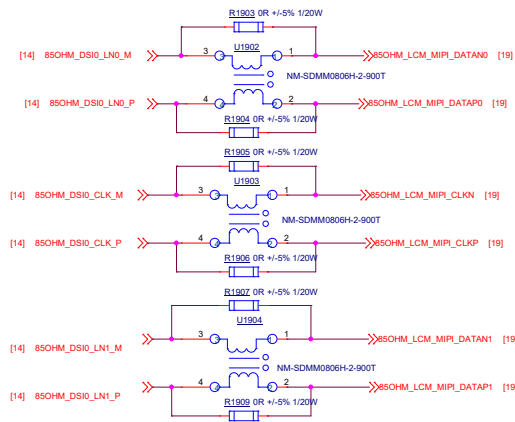
REC



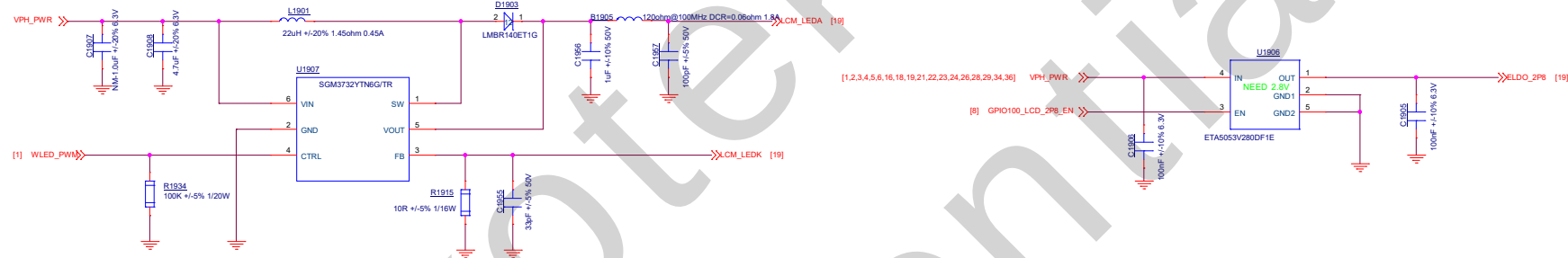
AUDIO PA2

Audio PA2

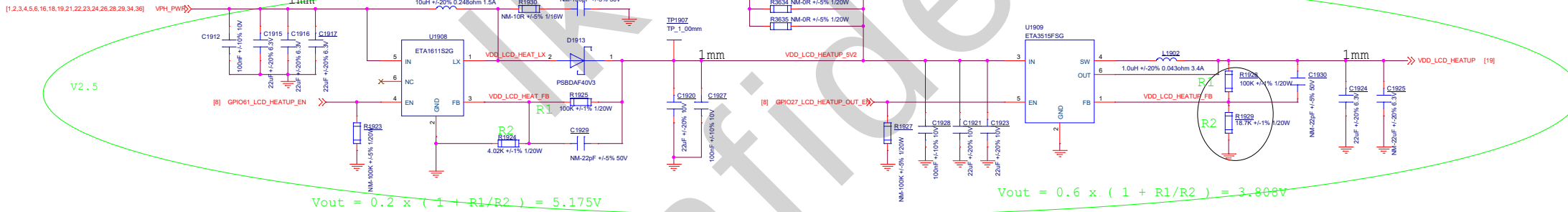




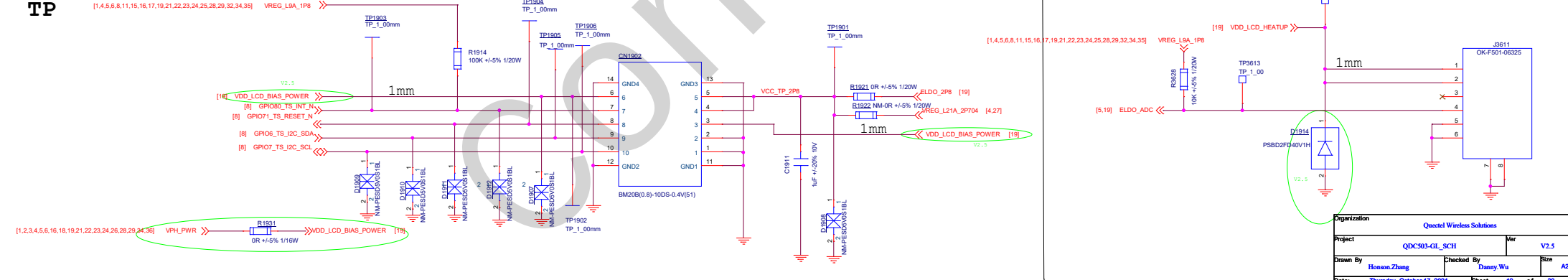
LCD Power



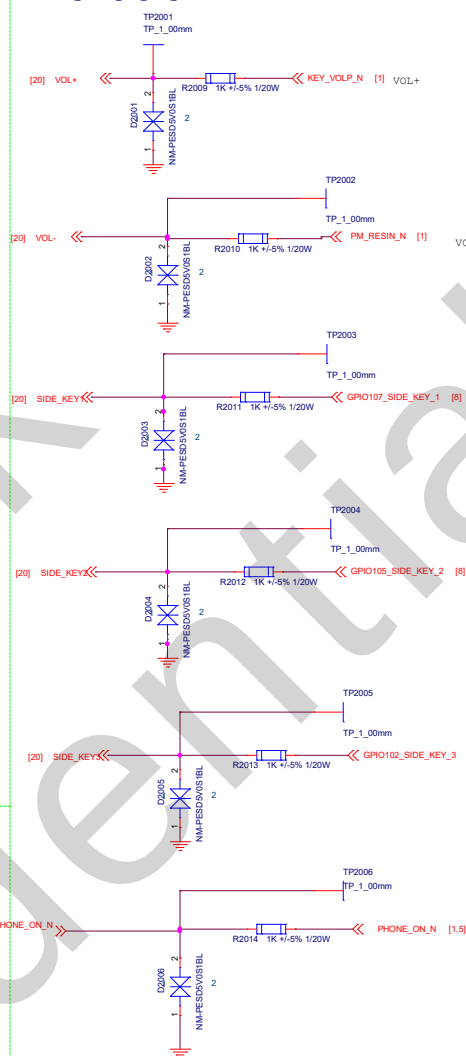
LCD Heat up



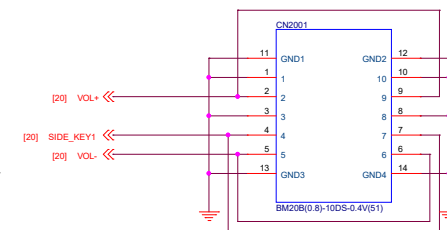
TP



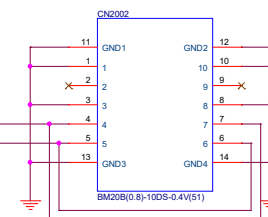
SCAN_VOLUM_PTT_PWR_KEY

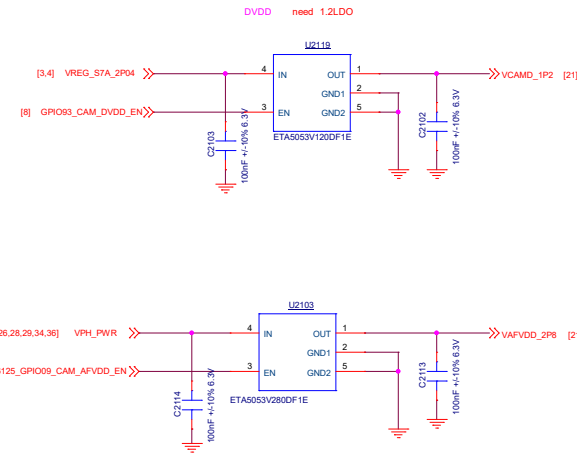
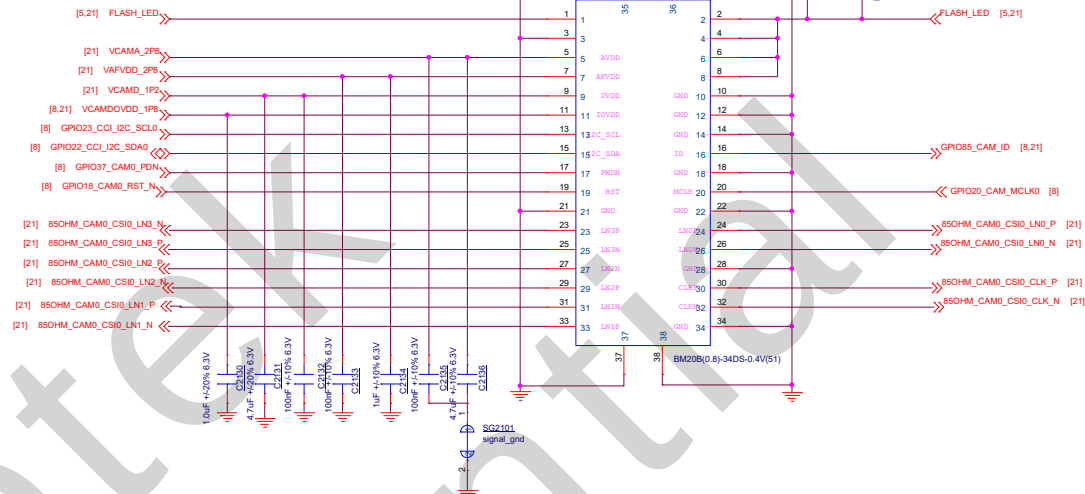


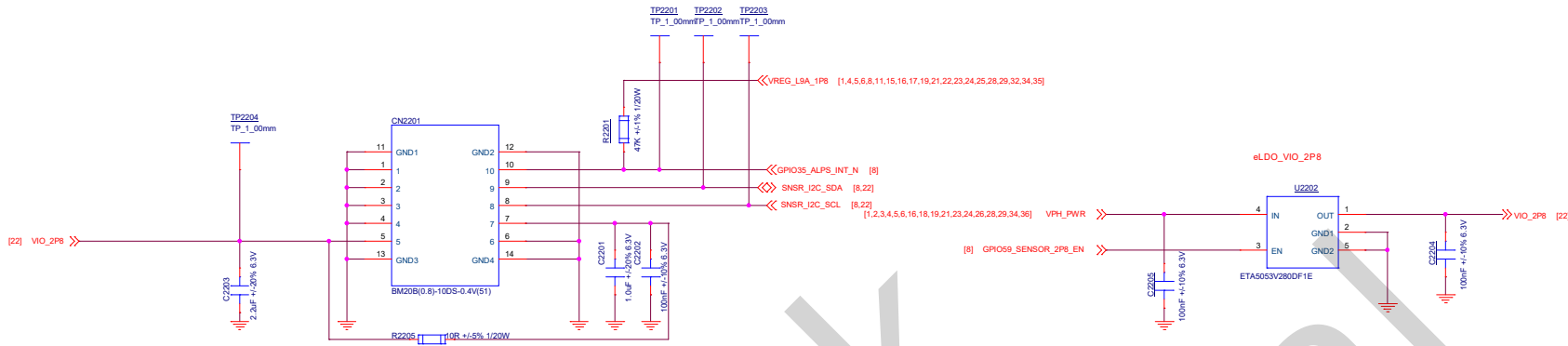
Left_SIDE_KEY



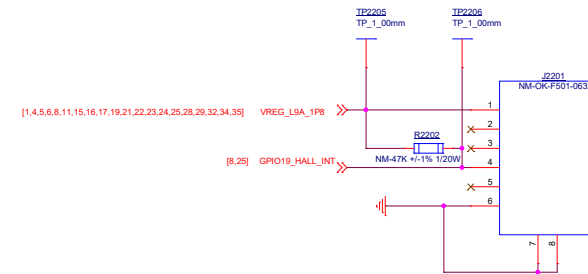
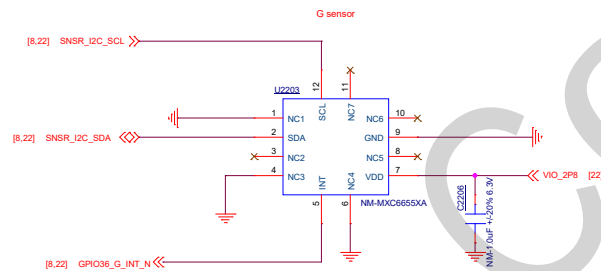
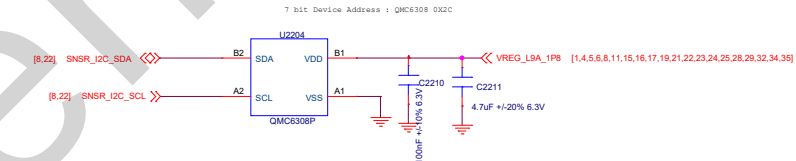
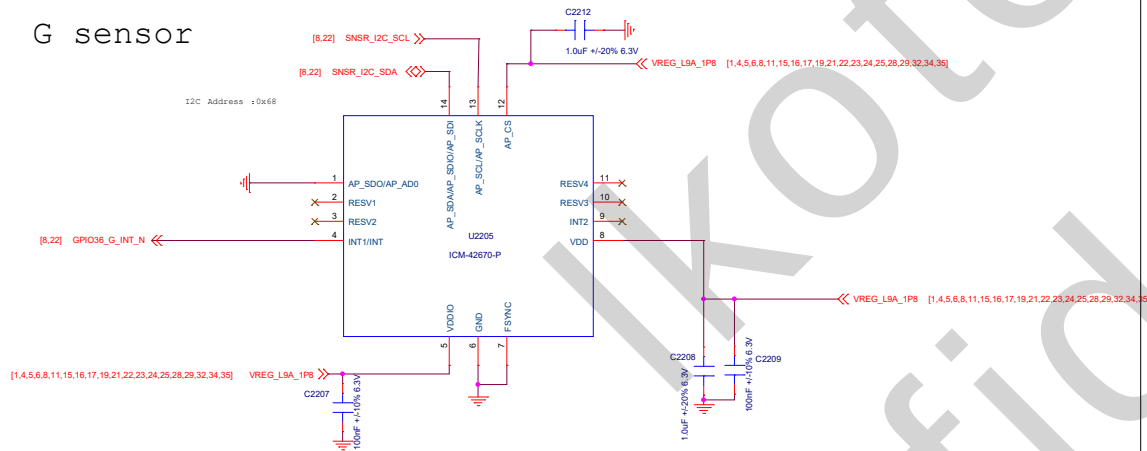
Right_SIDE_KEY

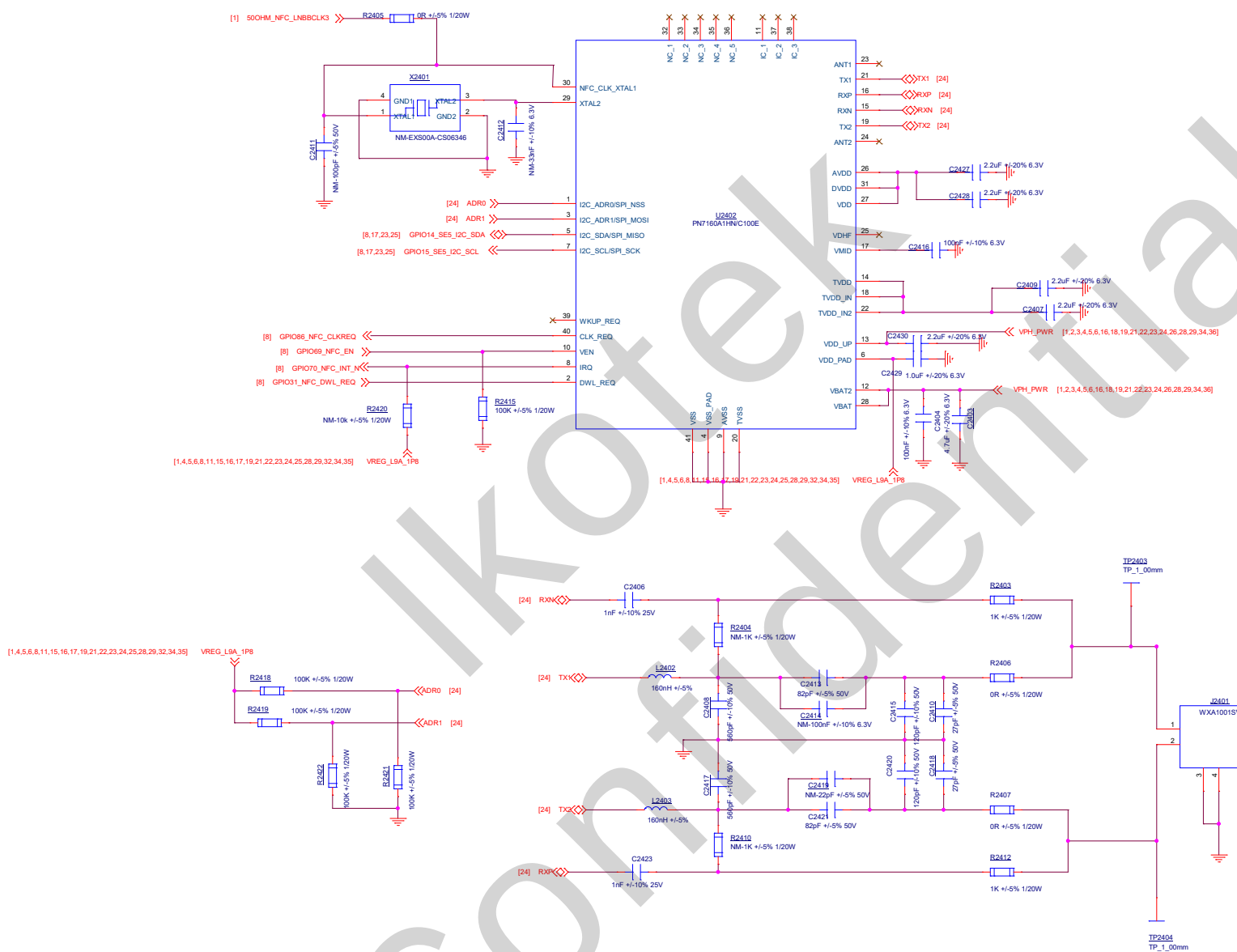


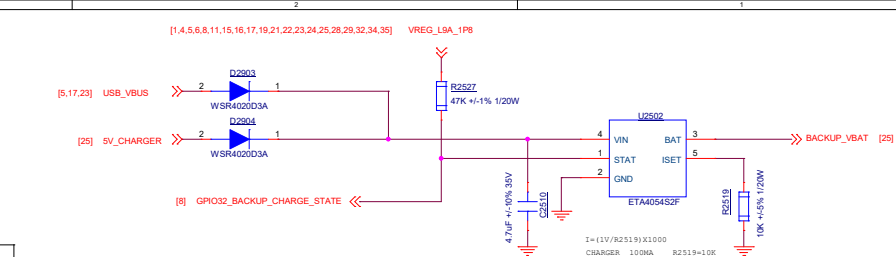




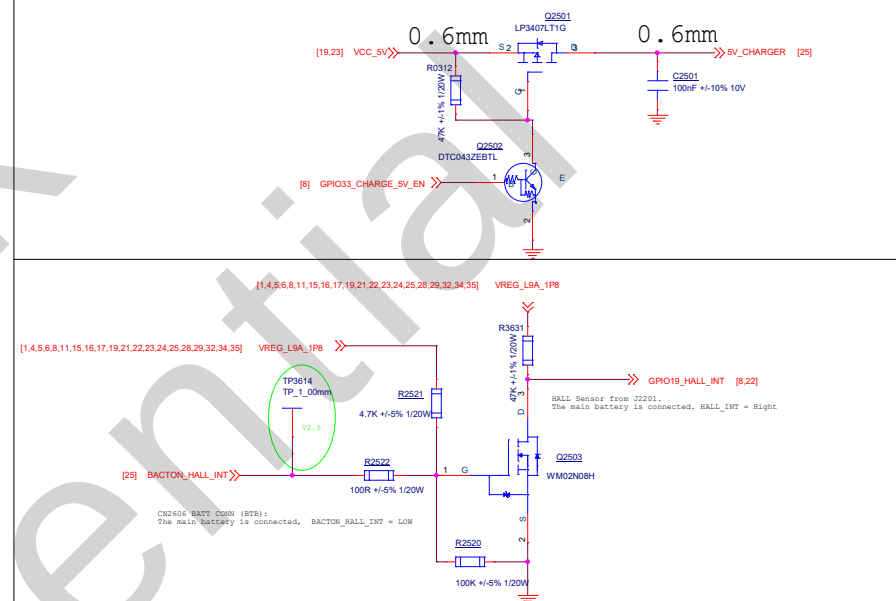
G sensor



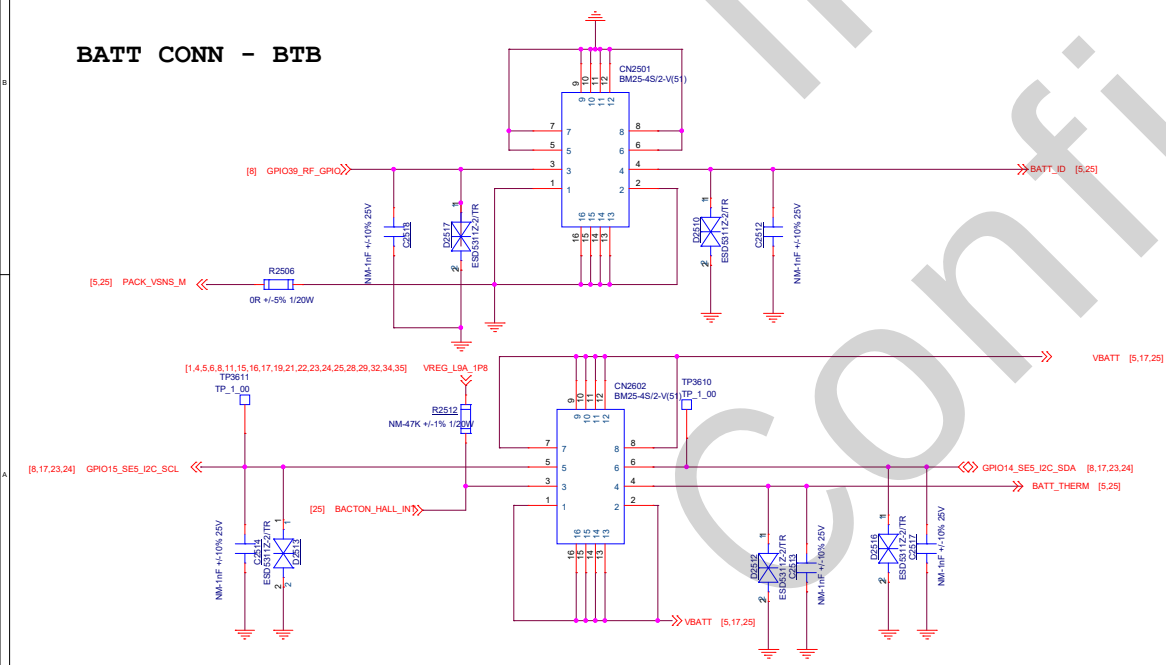




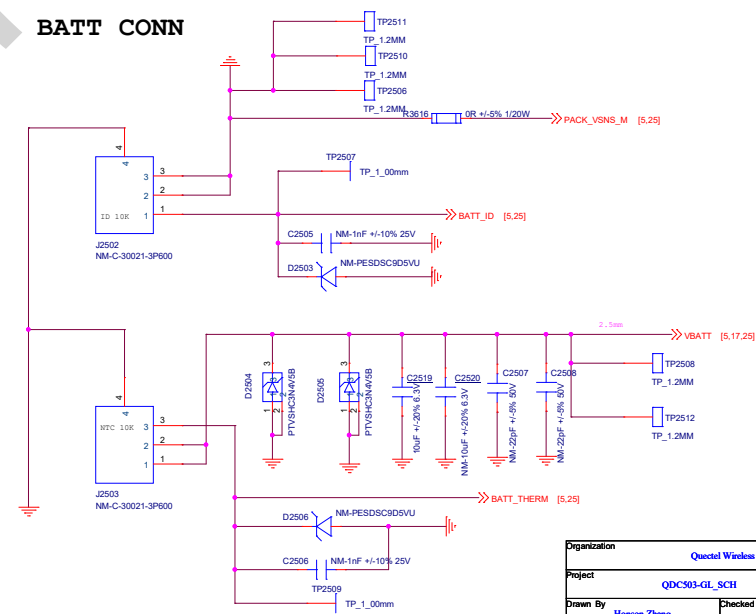
The schematic diagram illustrates the power management section of the TMS320C6748. It shows the connection of VBAT to the backup supply of the Q2501 (WSR4020D3A) and the Q2504 (NM-PP68N30V9) MOSFET. The Q2504 is controlled by the BACKUP_VBAT_CTRL signal. The Q2505 (NM-WM02N08H) MOSFET is controlled by the BACTON_HALL_INT signal. The diagram includes various resistors (R2523, R2524, R2525, R2526) and their values (100K, 100K, NM-100R, NM-4.7K).

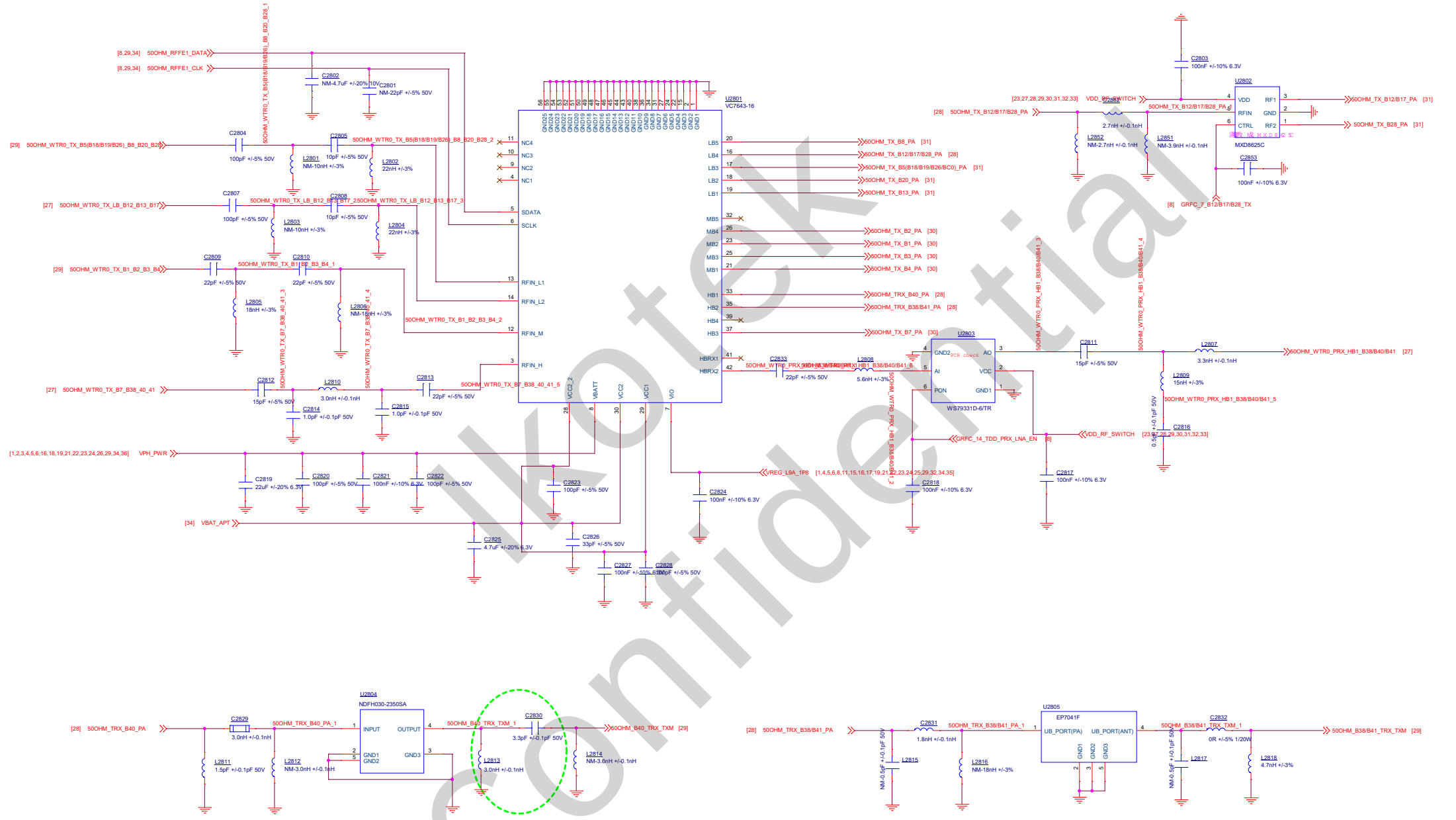


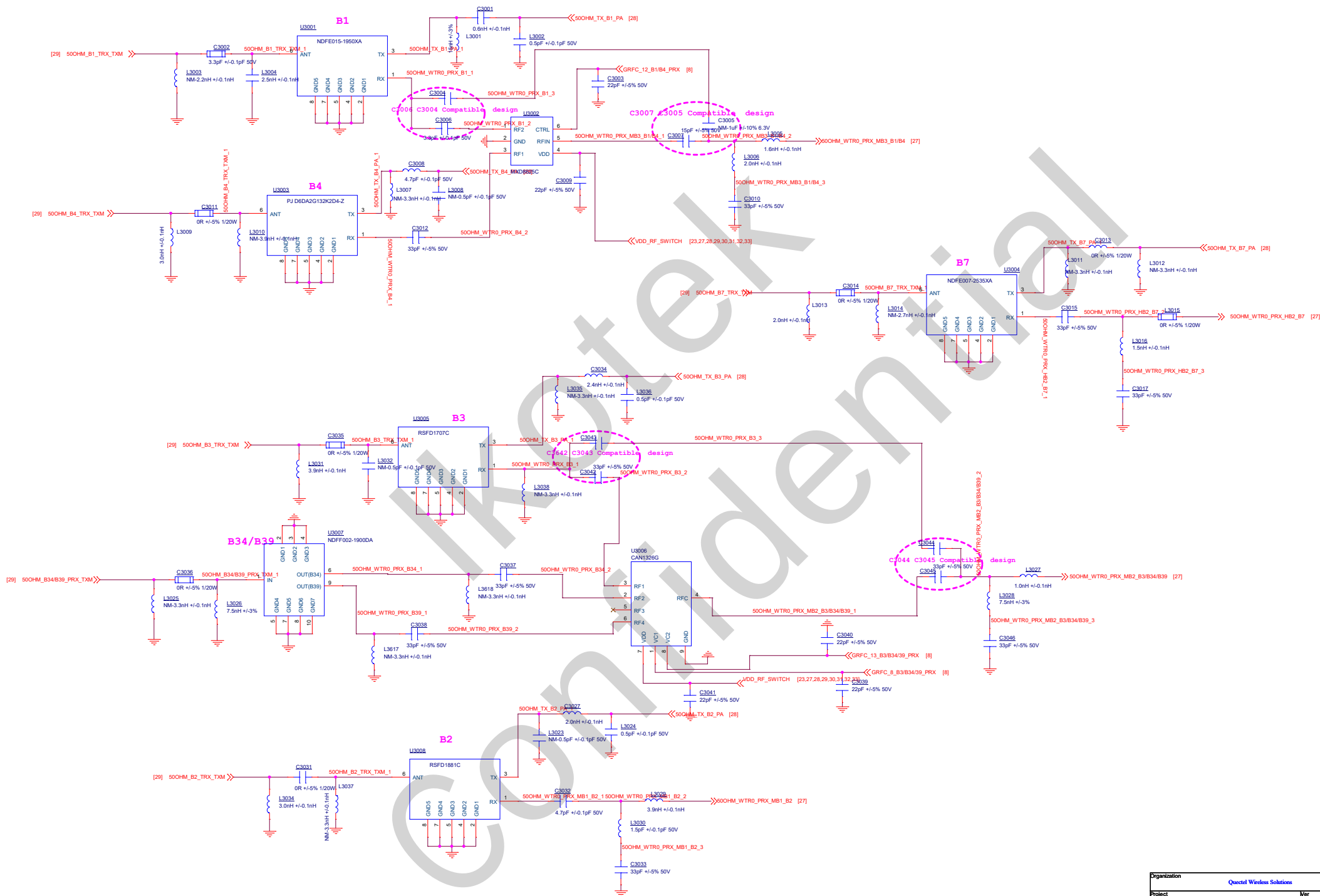
BATT CONN - BTB

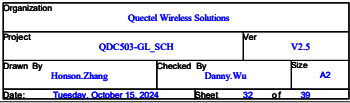


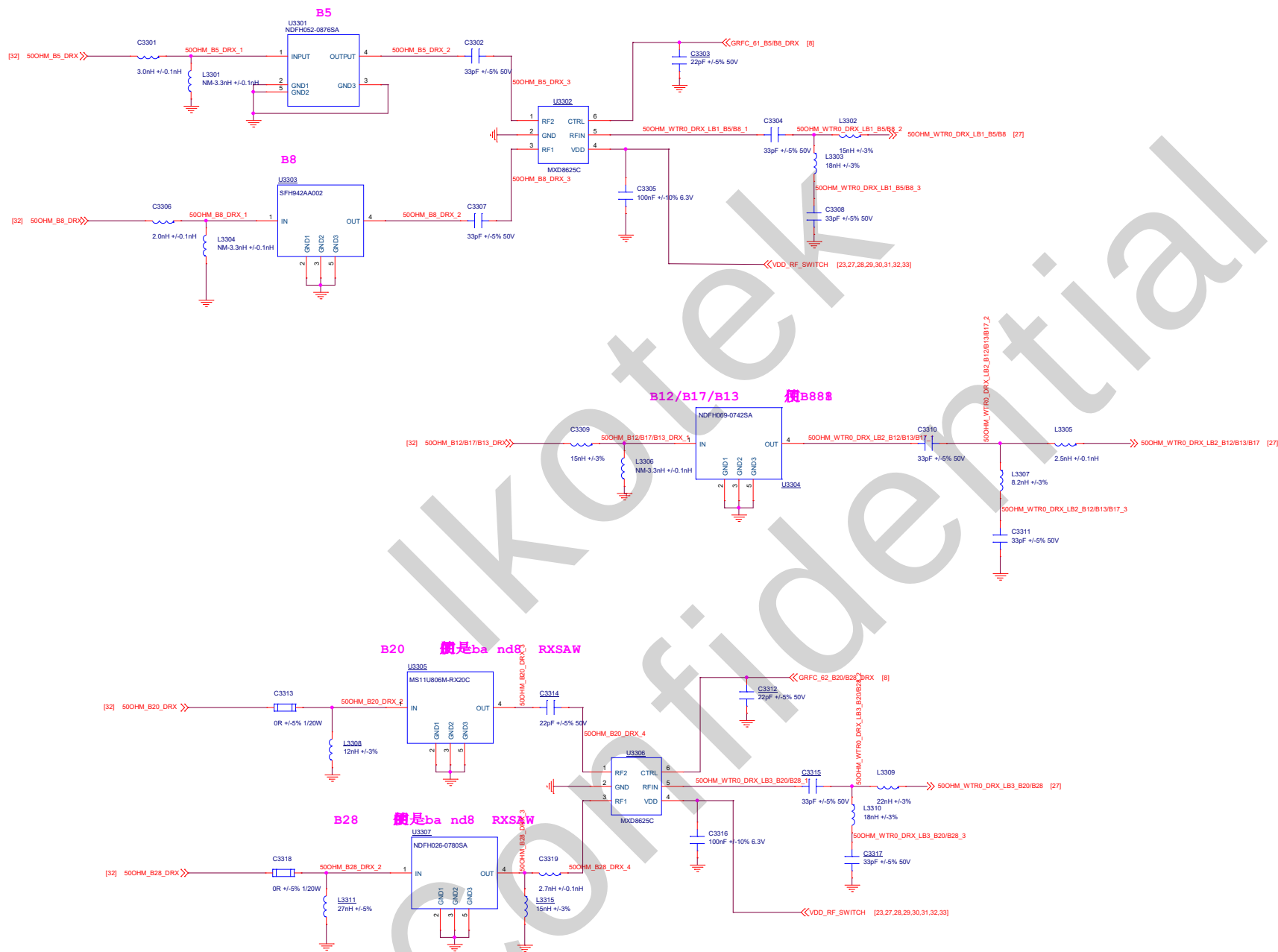
BATT CONN

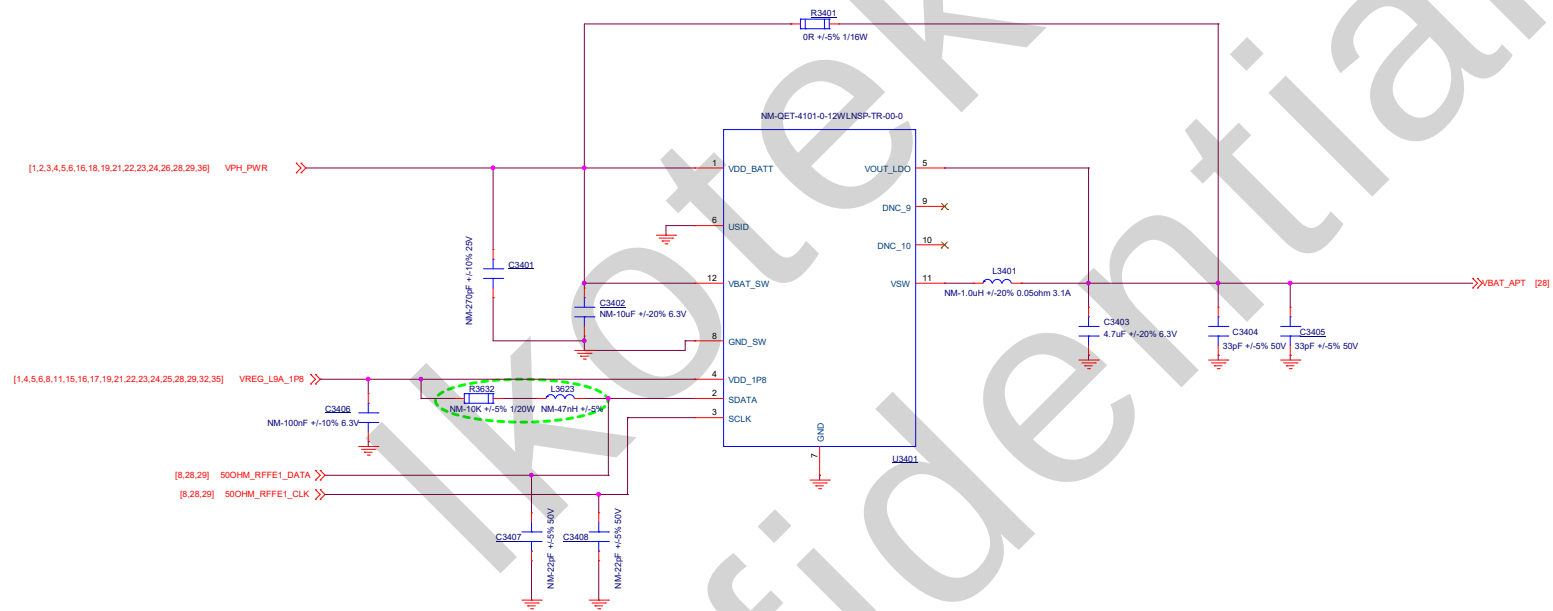


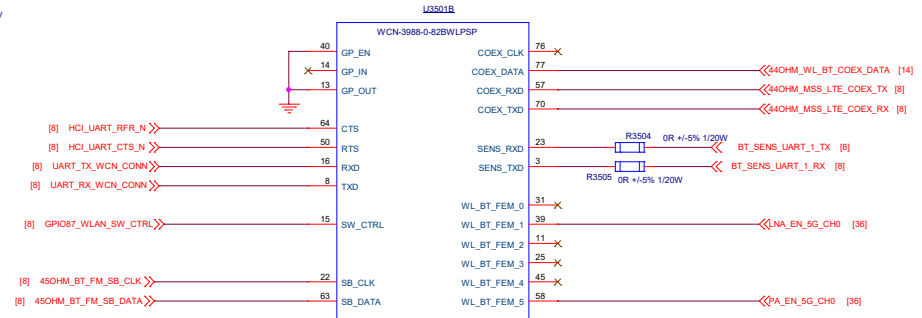
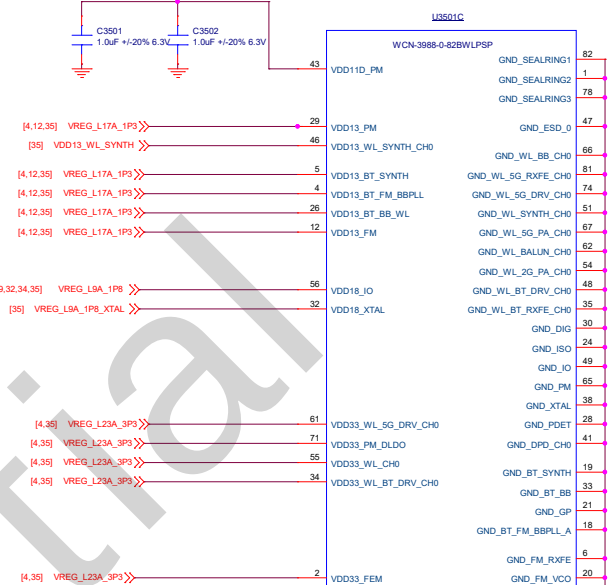
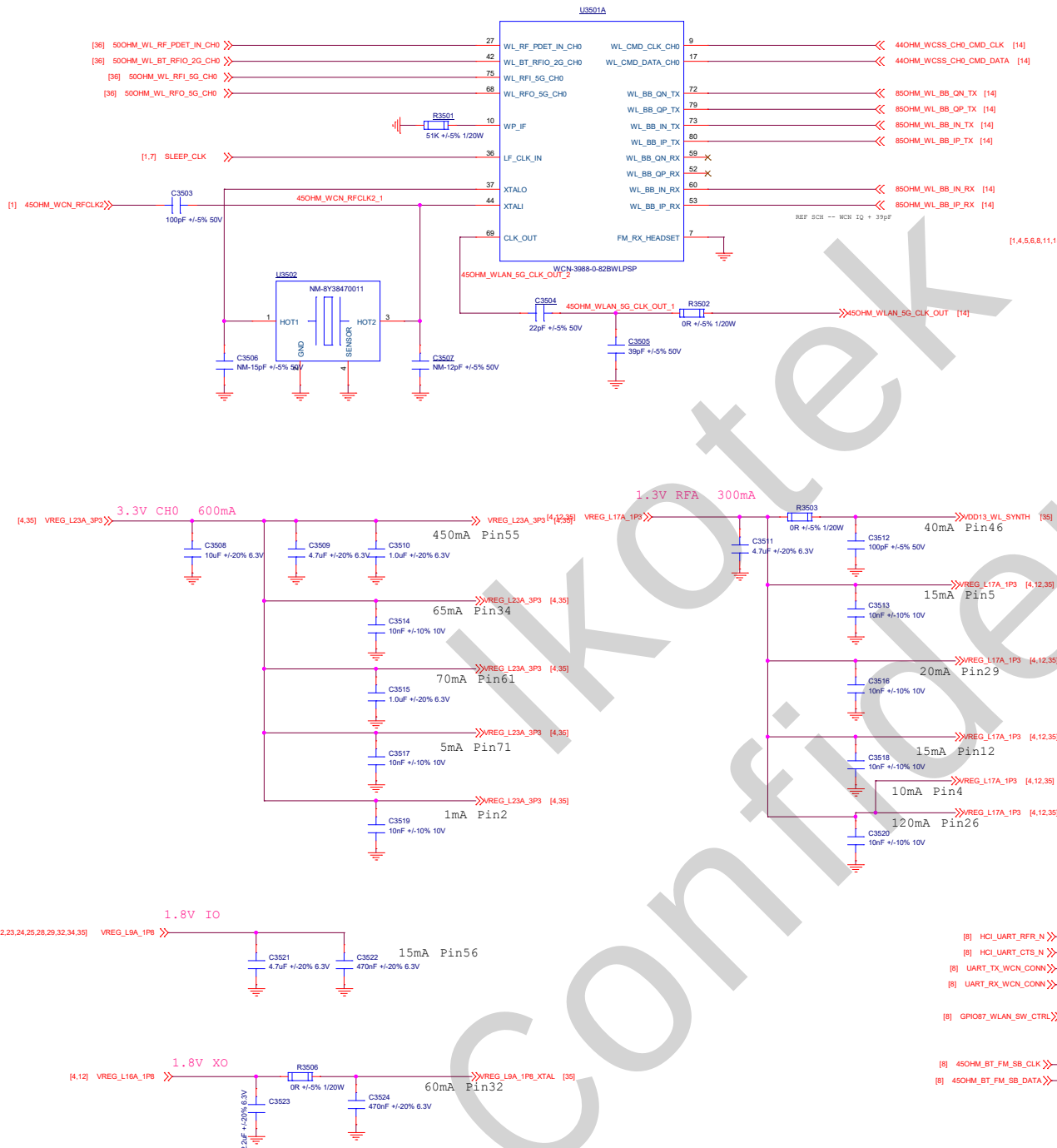




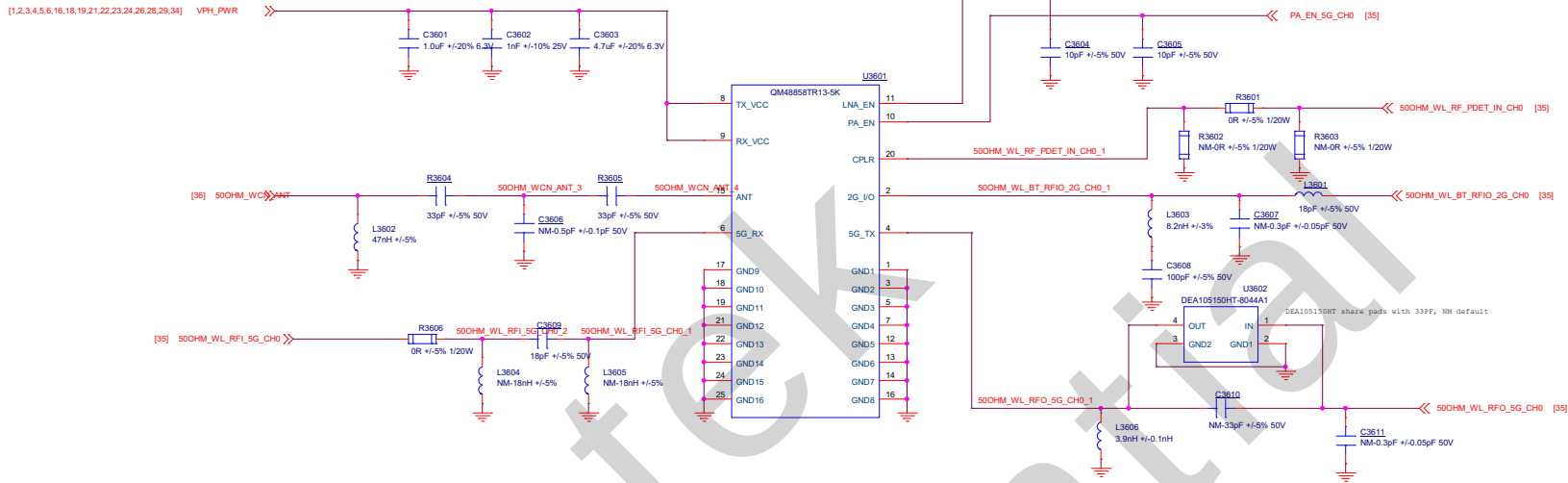




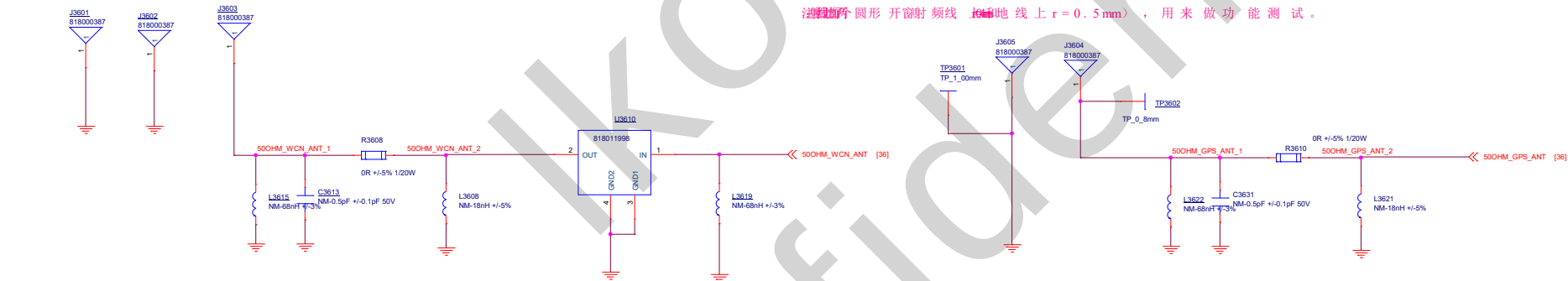




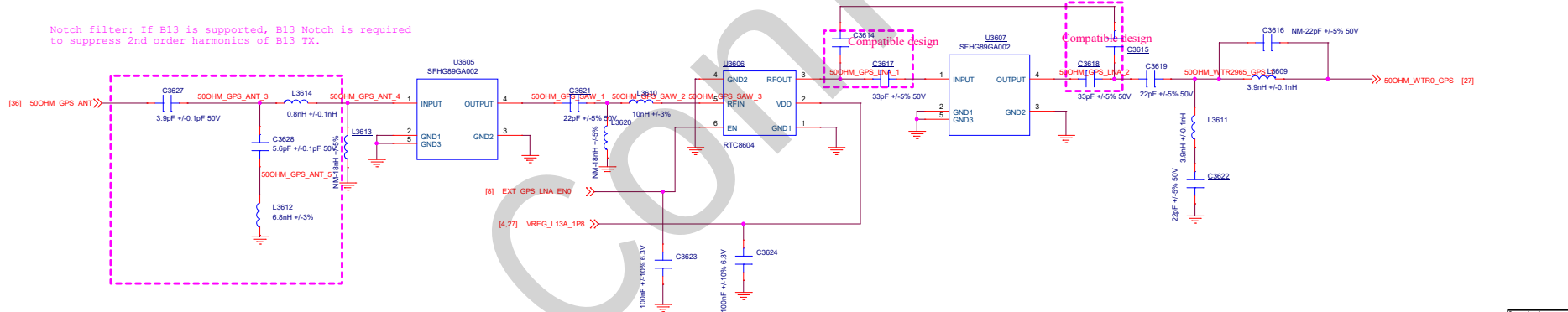
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注：圆形开窗射频线 10mm 地上 $r=0.5\text{mm}$ ，用来做功能测试。

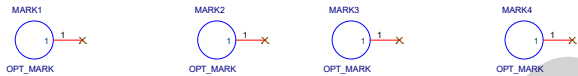


Notch filter: If B13 is supported, B13 Notch is required to suppress 2nd order harmonics of B13 TX.



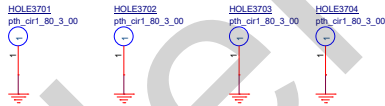
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MARK



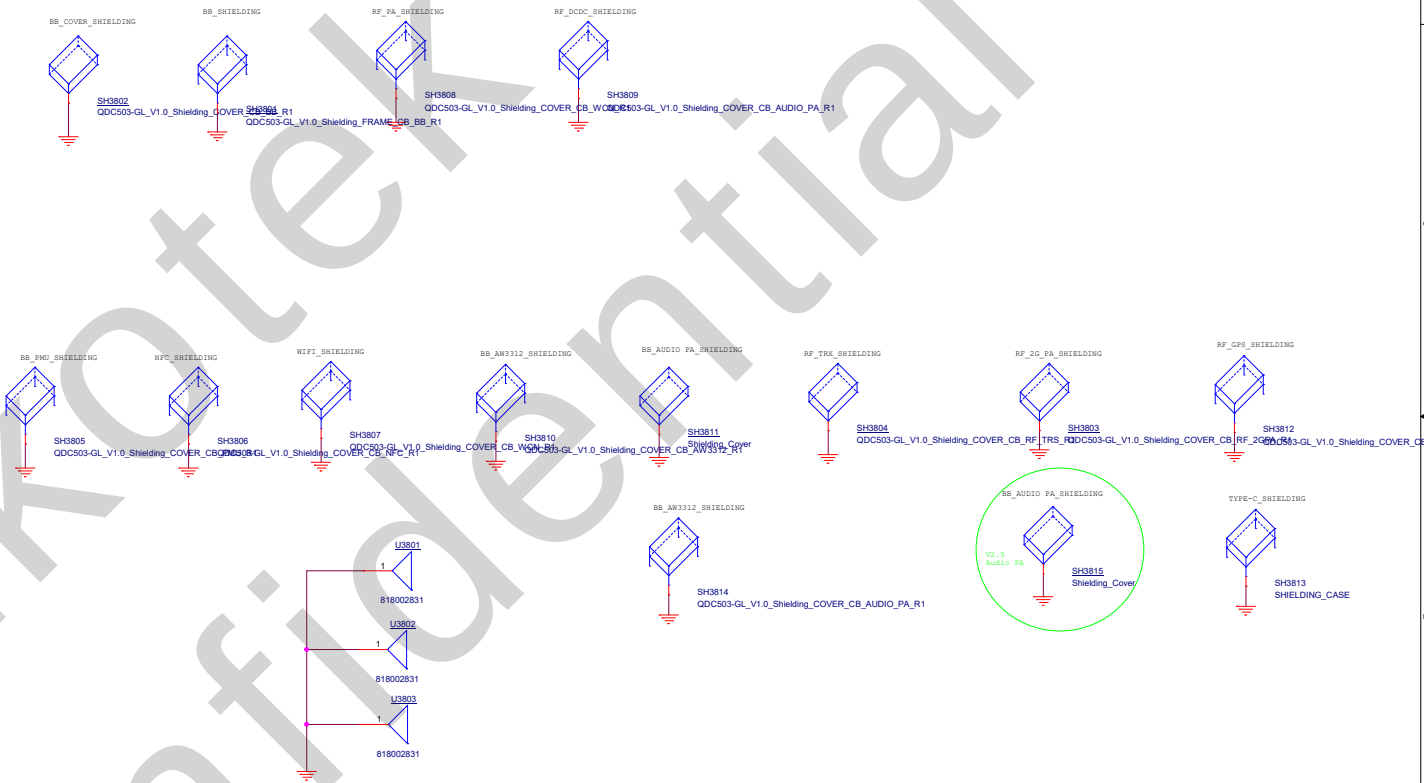
lable

PCB



TOP

BOTTOM



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2020-08-06
1.ADD R2326 R2324 R2325 Q2604

2020-08-11
1.ADD R2327 R2328

2020-08-12
1.TP0803,TP0804 change to 1mm testpoint
2.ADD TP2510,TP2511 TP1801-1809 TP0501-0502 TP2403-2404

2020-08-13
1.ADD C1625 R1615
2.DEL C1155 C1156

QDC503 V1.2 FROM QDC503_GL_SCH_V1.1_20200922

2020-12-04
1.ADD R2334 R2336 Q2304-----NC
2.ADD R2335 R2337 R2338 Q2303
3.U0501.3 FROM U0101.10(PM6125_GPIO07_SENSOR_2P8_EN) TO U0701.AJ4(GPIO59_SENSOR_2P8_EN)
4.ADD R1809 0201 0R
5.ADD R1614/R1618-----NC
6.ADD R1616/R1617-----OR
7.Delete Q2601 R2613 R2614 C1166
8.ADD C1244 0201 470NF
9.ADD L3038 0201 3.3NH-----NC
10.ADD L3136 0201 3.3NH-----NC
11.ADD L3137 0201 68NH
12.ADD L3315 0201 15NH
13.ADD L3223 0201 3.6NH
14.ADD L3225 0201 6.2NH
15.ADD R0557-R0559 Q0501 Q0502 C0555
16.ADD R1620/R1621-----NC
17.ADD R1619/R1622-----OR
18.R2504.1 change to A_VBAT
19.ADD TP2608 FOR CC1
20. ADD RT0102 100K NTC,U0101.10 ADD CONNECT SKIN_THERM
21.U2501 change to max14741
22.ADD U1908 R1936-1937 C1910 C1912
23.add Q2501 DTC043ZEBTL
24.R2516 change to 47K
25.del D2501/D2502
26.ADD U2502 R2518 R2519 C2510 C2509 R2511
27.Exchange SM6115 GPIO_39 and GPIO_68

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