WCN3680B/WCN3660B

Device Specification

80-WL007-1 Rev. D

August 29, 2014

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Revision history

Bars appearing in the left margin (as shown here) indicate where technical changes have occurred for this revision. The following table lists the technical content changes for all revisions.

Revision	Date	Description
A	October 2013	Initial release
B	February 2014	■ Table 3-22: BT Tx performance specifications: basic rate, class: for RF output power (GFSK) parameter, changed Max value and added footnotes 2 and 3
C	March 2014	■ Updated Section 5.1.1: Tape and reel information – Changed 4000 devices to 5000 devices
D	July 2014	■ Updated Table 3-2: Operating Conditions - Changed the VDD_xxx_ 1P3 parameter maximum value from 1.35 to 1.38. ■ Updated Table 3.4:Power Sequencing - Added power up and power down information for MS8916 and other platforms. ■ Updated Table 3-8, Reference Requirements:Changed voltage swing in master reference clock requirements to 2.0 ■ Updated Table 4-1, WCN3680B part marking line description and Table 4-2, WCN3660B part marking line description

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Figures

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Tables

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1 Introduction

1.1 Documentation overview

Technical information for the WCN3680B/WCN3660B IC is primarily covered by the documents listed in Table 1-1. Each is a self-contained document, but a thorough understanding of the device and its applications requires familiarization with all of them. The device description in Section 2.1 is a good place to start. All released WCN3680B/WCN3660B documents are posted at the CDMATech Support Website (https://support.cdmatech.com) and are available for download.

Table 1-1 Primary WCN3680B/WCN3660B documentation

Document no.	Title/description
80-WL007-1 (this document)	*WCN3680B/WCN3660B Device Specification* Conveys all WCN3680B/WCN3660B IC electrical and mechanical specifications. Additional material includes pin assignments; shipping, storage, and handling instructions; printed circuit board (PCB) mounting guidelines; and part reliability. This document can be used by company purchasing departments to facilitate procurement.
80-N8644-2	*48 MHz Crystal 20 PPM Overall Tolerance for 5 GHz WLAN Connectivity Products Mini-Specification*
80-WL302-4	*WCN3660B Device Revision Guide*
80-WL007-4	*WCN3680B Device Revision Guide*
80-WL300-5	*WLAN/BT/FM Design Guidance and Training Using WCN3660, WCN3660A, or WCN3680 Design Guidelines*
80-WL300-21	*WLAN/BT/FM Training Using WCN3660, WCN3660A, or WCN3680*
80-WL300-25	*WCN36x0(A) Training WLAN Tx CLPC Characterization Using QSPR Tools*
80-WL300-26	*WCN36x0 Training WLAN Tx SCPC Characterization Using QSPR Tools*
80-WL300-29	*WCN36x0(A) WLAN RSSI Calibration Procedure*
80-WL300-15	*WCN36x0(A) RF Matching Guidelines*
80-WL005-43	*WCN3660/A/B, WCN3680/B Reference Schematic*

Additional reference documents are listed in Table 1-2.

Table 1-2 Reference documents

Reference	Document
1	*IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June 2007*
2	*IEEE Std 802.11b, IEEE Std 802.11d, IEEE Std 802.11e, IEEE Std 802.11g, IEEE Std 802.11i: IEEE 802.11-2007 WLAN MAC and PHY, June 2007i*

Table 1-2 Reference documents (cont.)

Reference	Document
3	*IEEE P802.11ac/D4.0, Draft Standard for Information Technology Telecommunications and Information Exchange Between Systems – Local and Metropolitan Area Networks – Specific Requirements*
3	*Bluetooth Specification Version 4.0*, December 17, 2009
4	*Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1 + EDR/3.0/3.0 + HS*, August 6, 2009
5	*Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0,* December 15, 2009

This WCN3680B/WCN3660B device specification is organized as follows:

Chapter 1 Provides an overview of the WCN3680B/WCN3660B documentation, gives a high-level functional description of the device, lists the device features, and defines marking conventions, terms, and acronyms used throughout this document.

Chapter 2 Defines the device pin assignments.

Chapter 3 Defines the device electrical performance specifications, including absolute maximum and operating conditions.

Chapter 4 Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.

Chapter 5 Describes shipping, storage, and handling of the WCN3680B/WCN3660B devices.

Chapter 6 Presents procedures and specifications for mounting the WCN3680B/WCN3660B device onto printed circuit boards (PCBs).

Chapter 7 Presents WCN3680B/WCN3660B device reliability data, including a definition of the qualification samples and a summary of qualification test results.

1.2 WCN3680B/WCN3660B device introduction

The WCN3680B/WCN3660B IC integrates four different wireless connectivity technologies into a single device suitable for handsets and other mobile devices:

- Dual-band 2.4 GHz and 5 GHz wireless local area network (WLAN) compliant with the IEEE 802.11a/b/g/n specification and supports optional external PA for both 2 GHz and 5 GHz bands
- WCN3680B supports 11ac (including 256QAM rates MCS8 and MCS9) for data rates of up to 433 Mbps
- Bluetooth (BT) compliant with the BT specification version 4.0 (BR/EDR + BLE); ANT+ support
- Worldwide FM radio, supporting the Radio Data System (RDS) for Europe and the Radio Broadcast Data System (RBDS) for the USA

The WCN3680B/WCN3660B is a highly integrated IC using the 3.805 × 3.82 × 0.63 mm, 79-pin wafer-level nanoscale package (79B WLNSP) – and is supplemented by modem IC processing

(the host IC) to create a wireless connectivity solution that reduces the part count and PCB area. The WCN3680B/WCN3660B IC ensures hardware and software compatibility with companion Qualcomm Atheros, Inc. (QCA) chipsets to simplify the design cycle and reduce OEM time-to-market.

The WCN3680B/WCN3660B IC uses low-power 65 nm RF CMOS fabrication technology, making it perfectly suited for battery-operated devices where power consumption and performance are critical.

As shown in Figure 1-1, the WCN3680B/WCN3660B device's major functional blocks are:

- Dual-band WLAN RF
- BT radio (RF and digital processing)
- FM radio (RF and digital processing)
- Shared WLAN + BT RF front-end (RF FE) circuits
- Top-level support circuits that interface with the modem IC, buffer the TCXO input, generate the wireless connectivity network (WCN) internal clocks, and gate and distribute DC power to the other blocks.

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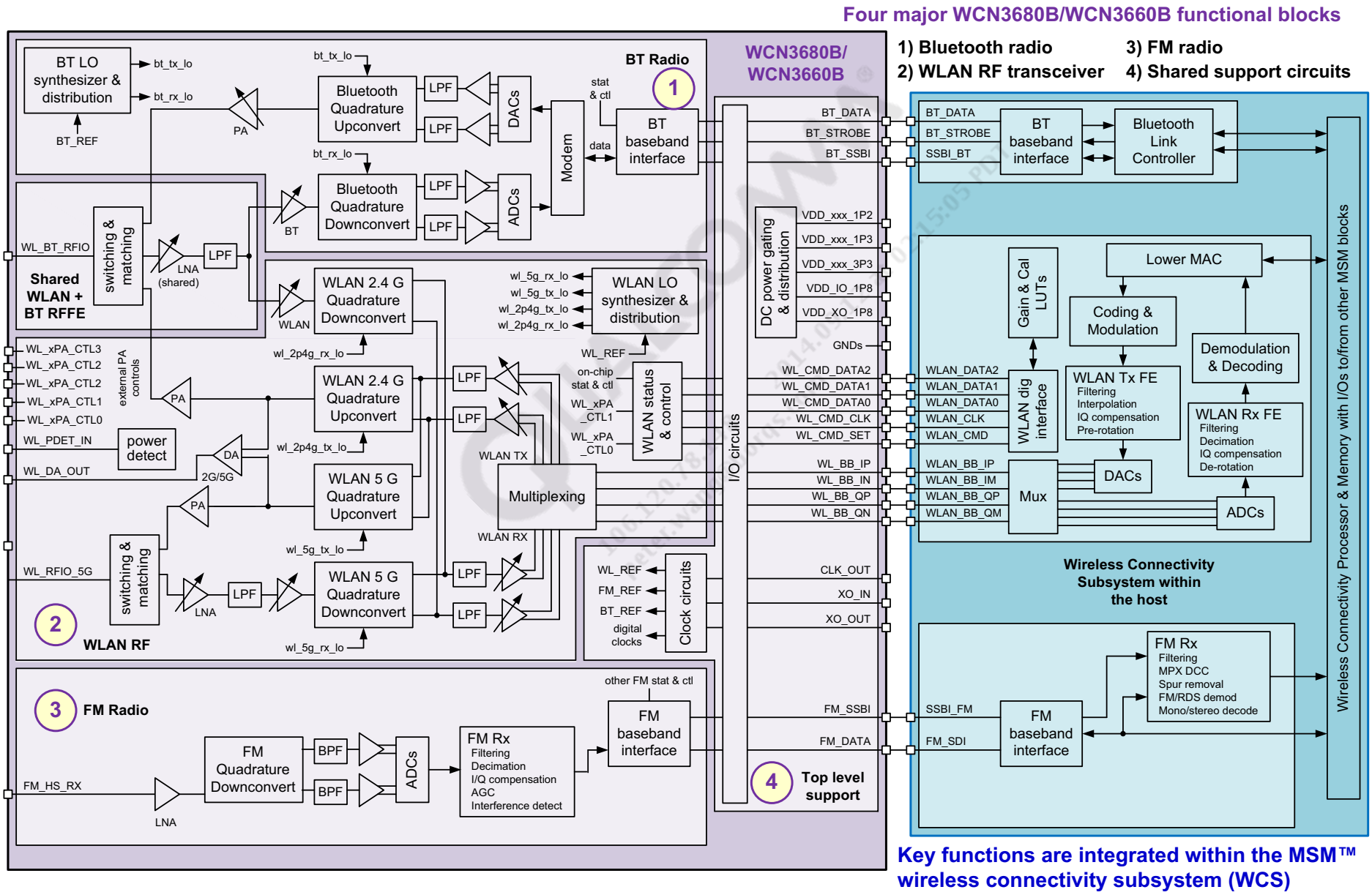

Figure 1-1 WCN3680B/WCN3660B functional block diagram

Since the WCN3680B/WCN3660B IC includes so many diverse functions, its operation is more easily understood by considering each major functional block individually. Therefore, the WCN3680B/WCN3660B document set is organized according to the block partitioning listed before Figure 1-1. Most information contained in this device specification is organized accordingly – including the circuit groupings within its functional block diagram (Figure 1-1), pin descriptions (Chapter 2), and detailed electrical specifications (Chapter 3).

1.3 WCN3680B/WCN3660B features

NOTE Some hardware features integrated within the WCN3680B IC must be enabled by software. Refer to the latest revision of the applicable software release notes to identify the enabled features.

1.3.1 WCN3680B/WCN3660B common WLAN features IC

- Integration of WLAN, BT, and FM radio functionality
- Optional support for 2.4 GHz and 5 GHz external PAs/LNAs for additional performance
- Highly integrated front-end eliminates external PA and LNA matching, and antenna Tx/Rx switching
- Support for the IEEE 802.11a/b/g/n radio standard
- Clock – 48 MHz crystal or 19.2 MHz
- 65 nm RF CMOS technology in the small 79 WLNSP package
- Dual-band WLAN: 2.4 GHz and 5 GHz RF transceivers
- Compliant with BT specification version 4.0
- Concurrent WLAN + BT reception in the 2.4 GHz band
- Small IC footprint, low parts count, and less PCB area overall

1.3.2 Additional features integrated into WCN3680B

- Added support for 802.11ac
- Support 256QAM modulation schemes (MCS8 and MCS9) for data rates of up to 433 Mbps
- Master clock – 48 MHz support only (no 19.2 MHz support)

1.3.3 WLAN features

- Advanced power management minimizes power consumption in nonactive modes.
- Supports both 2.4 GHz and 5 GHz RF transceivers and compliant with IEEE 802.11a/b/g/n and IEEE 802.11ac (WCN3680B only)
- Support for an external PA and an external LNA for applications requiring enhanced 2.4 GHz and 5 GHz performance

- Integrated PA and LNA provides high dynamic Tx output power and excellent Rx sensitivity for extended range
- Internal PAs and T/R switches for both 2.4 GHz and 5 GHz, with the option for an external PA and T/R switch for 2 GHz and 5 GHz
- Concurrent WLAN + BT reception in the 2.4 GHz band
- LTE/ISM coexistence support
- No manufacturing calibration needed
- Host interfaces:
  - 4-line analog baseband interface with Rx/Tx multiplexing
  - 5-line digital command-and-control interface
- Other solution-level features
  - **WCN3660B**: Support for HT20 and HT40
  - **WCN3680B**: Support for HT20, HT40, VHT20, VHT40, and VHT80
  - Support for 802.11n (WCN3660B and WCN3680B) and 802.11ac (WCN3680B only)
  - Space-time block coding (STBC) support
  - Support for short guard interval
  - Support for other optional 11ac features (WCN3680B only), i.e., LDPC. MU-MIMO, Tx beam-forming (dependent on the host MSM platform)

1.3.4 BT features

- BT 4.0 + BR/EDR + BLE
- Support for ANT protocol
- Support for BT-WLAN coexistence operation, including optional concurrent receive
- Up to 3.5 piconets (master, slave, and page scanning)
- Support for class 1 and class 2 power-level transmissions without requiring an external PA
- No factory calibration required
- MSM interfaces:
  - Two-line digital data interface supports Rx and Tx.
  - Single-wire serial bus interface (SSBI) for status and control

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1.3.5 FM radio features

- Worldwide FM band support (76 to 108 MHz) with 50 kHz channel spacing
- Integrated FM modem receiver with integrated frequency synthesizer
- RDS for Europe/RBDS for USA
  - Integrated RDS/RBDS encoder and decoder (with enable/disable function)
- Automatic gain control
- Standby mode
- Desense-free FM reception when operating with a phone
- Host interfaces:
  - Single-line digital data interface supports Rx
  - SSBI for status and control
- Supports external wired-headset antenna for Rx-only

1.3.6 Top-level support features

- System clock options
  - 19.2 MHz TCXO clock for 2.4 GHz band only
  - 48 MHz XO for 2.4G and 5G configuration
- Clock buffering, gating, and distribution to all other blocks
- All WLAN, BT, and FM interfaces with the modem IC are managed by the support block.
- DC power-supply gating and distribution to all other blocks

1.3.7 Package and other features

- Small package – 3.805 × 3.82 × 0.63 mm 79B WLNSP, 0.4 mm pitch
- Many ground pins for improved electrical grounding, mechanical strength, and thermal continuity
- Few external components required
- Pb-free, BrCl-free, RoHS compliant, and SAC405 compliant

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1.3.8 Summary of key WCN3680B/WCN3660B features

Table 1-3 Key WCN3680B/WCN3660B features

Feature	WCN3680B/WCN3660B capability
System	
Highly integrated	■ Combo IC with WLAN, BT, and FM radio functionality ■ Lower parts count and less PCB area overall ■ Eliminates external PA and LNA matching, and Tx/Rx RF switching
WLAN + BT	■ Concurrent reception in the 2.4 GHz band ■ PTA modes for coexistence
Automated calibration	No factory calibration required
WLAN RF (digital processing in companion modem IC)	
Dual-band support	■ 2.4 GHz and 5 GHz RF transceivers ■ Supports 2 GHz and 5 GHz external PA ■ LTE/ISM coexistence support ■ **WCN3660B**: Supports HT20 and HT40 rates ■ **WCN3680B**: Supports HT20/VHT20, HT40VHT40, and VHT80 rates
Simple host interfaces	■ 4-line analog baseband interface with Rx/Tx multiplexing ■ 5-line digital command-and-control interface
IEEE 802.11a/b/g/n compliant	With companion modem IC
Other solution-level features	■ WoWLAN support ■ Support for MCS 0 through 7; up to 150 Mbps data rates ■ Support for MCS 0 through 9; up to 433 Mbps data rates on WCN3680B ■ STBC support ■ Support for short guard interval ■ Infrastructure, ad-hoc, AP, and Wi-Fi direct operating modes
BT radio	
BT specification compliance	4.0 compliant; 1.x, 2.x + EDR, and 3.0 backward compatible
Highly integrated	Baseband modem and 2.4 GHz transceiver; improved Rx sensitivity
Simple host interfaces	■ 2-line digital data interface supports Rx and Tx ■ SSBI for status and control
Supported modulation	GFSK, π/4-DQPSK, and 8DPSK (in both directions)
Connectivity	■ Up to seven total wireless connections ■ Up to 3.5 piconets (master, slave, and page scanning) ■ One SCO or eSCO connection
Digital processing	■ Modem ■ Support for all BR, EDR, and BLE packet types
RF Tx power levels	Class 1 and 2 transmissions without requiring an external PA
LPPS	Reduced device power consumption
ANT	Enables communication between self-powered devices

Table 1-3 Key WCN3680B/WCN3660B features (cont.)

Feature	WCN3680B/WCN3660B capability
FM radio	
Worldwide FM band support	76 to 108 MHz, with 50 kHz channel spacing
Highly integrated	■ Baseband processing and RF receiver ■ Data system support □ Radio data system for Europe (RDS) □ Radio broadcast data system for U.S.A. (RBDS)
Simple host interfaces	■ Single-line digital data interface supports Rx and Tx. ■ SSBI for status and control
Rx support	External wired-headset antenna for Rx-only
Highly automated	Search and seek; gain control; frequency control; noise cancellation; soft mute; high-cut control; mono/stereo blend; adjustment-free stereo decoder; programmable de-emphasis
Top-level support	
Clock	■ 48 MHz crystal ■ 19.2 MHz for single-band 2.4G configuration only ■ Clock buffering, gating, and distribution to all other blocks
Modem IC interfaces	Manages all WLAN, BT, and FM interfaces
DC power	Gates and distributes power to all other blocks
Fabrication technology	
Single die	65 nm RF CMOS
Package	
Small, thermally efficient package	79 WLNSP: 3.805 × 3.82 × 0.63 mm; 0.4 mm pitch

1.4 Terms and acronyms

Table 1-4 defines terms and acronyms commonly used throughout this document.

Table 1-4 Terms and acronyms

Term	Definition
π/4 DQPSK	π/4 rotated differential quadrature phase shift keying
8DPSK	8-state differential phase shift keying
16QAM	16-state quadrature amplitude modulation
64QAM	64-state quadrature amplitude modulation
ACL	Asynchronous connection-oriented link
ADC	Analog-to-digital converter
AGC	Automatic gain control
AP	Access point
BB	Baseband

Table 1-4 Terms and acronyms (cont.)

Term	Definition
BER	Bit error rate
BLE	Bluetooth low energy
BMPS	Beacon-mode power save
BOM	Bill of materials
BPF	Bandpass filter
bps	Bits per second
BPSK	Binary phase shift keying
BR	Basic rate
BT	Bluetooth
CCK	Complimentary code keying
CDM	Charged device model
CDMA	Code Division Multiple Access
CLPC	Closed loop power control
DAC	Digital-to-analog converter
DBPSK	Differential binary phase shift keying
DEVM	Differential error vector magnitude
DNC	Do not connect
DQPSK	Differential quadrature phase shift keying
DTIM	Delivery traffic indication message
EDR	Enhanced data rate
EIRP	Effective isotropic radiated power
eSCO	Extended synchronous connection-oriented
ESD	Electrostatic discharge
ESR	Effective series resistance
ETSI	European Telecommunications Standards Institute
EVM	Error vector magnitude
FBPR	Forbidden band power ratio
FCC	Federal Communication Commission
FDD	Frequency division duplexing
FEM	Front-end module
FM	Frequency modulation
GFSK	Gaussian frequency shift keying
HBM	Human-body model
HCI	Host controller interface
Hi-Z	High impedance
I/O	Input/output

Table 1-4 Terms and acronyms (cont.)

Term	Definition
kbps	Kilobits per second
LSBit or LSByte	Defines whether the LSB is the least significant bit or least significant byte. All instances of LSB used in this manual are assumed to be LSByte, unless otherwise specified.
MSBit or MSByte	Defines whether the MSB is the most significant bit or most significant byte. All instances of MSB used in this manual are assumed to be MSByte, unless otherwise specified.
LNA	Low-noise amplifier
LO	Local oscillator
LPF	Low-pass filter
LPO	Low-power oscillator
LPPS	Low-power page scan
MAC	Medium access controller
MCS	Modulation coding scheme
MPX	Multiplex
MRC	Master reference clock
NVM	Nonvolatile memory
OEM	Original equipment manufacturer
PA	Power amplifier
PCB	Printed circuit board
PCM	Pulse-coded modulation
PDET	Power detector
PER	Packet error rate
PHY	Physical layer
PLL	Phase-locked loop
PM	Power management
PMIC	Power management integrated circuit
PTA	Packet traffic arbitration
QAM	Quadrature amplitude modulation
QCA	Qualcomm Atheros, Inc.
QoS	Quality of service
QPSK	Quadrature phase shift keying
RBDS	Radio broadcast data system for U.S.A.
RDS	Radio data system for Europe
RF	Radio frequency
RH	Relative humidity
RoHS	Restriction of hazardous substances

Table 1-4 Terms and acronyms (cont.)

Term	Definition
Rx	Receive, receiver
SBI	Serial bus interface
SCO	Synchronous connection-oriented
SCPC	Self-calibrated power control
SMT	Surface-mount technology
SoC	System-on-Chip
Sps	Symbols per second (or samples per second)
SSBI	Single-wire SBI
STBC	Space-time block coding
TCXO	Temperature-compensated crystal oscillator
TDD	Time-division duplexing
TIM	Traffic indication map
TKIP	Temporal key integrity protocol
T/R	Transmit/receive
Tx	Transmit, transmitter
uAPSD	Unscheduled automatic power-save delivery
VoIP	Voice-over-internet protocol
WAN	Wide area network
WEP	Wired-equivalent privacy
WLAN	Wireless local area network
WLNSP	Wafer-level nanoscale package
WMM	Wi-Fi multimedia
WMM-AC	Wi-Fi multimedia access categories
WoWLAN	Wake-on-WLAN
WPA	Wi-Fi protected access
XO	Crystal oscillator
ZIF	Zero intermediate frequency

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1.5 Special marks

Table 1-5 defines special marks used in this document.

Table 1-5 Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, DATA[7:4] may indicate a range that is 4 bits in length, or DATA[7:0] may refer to all eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, RESIN_N.
0x0000	Hexadecimal numbers are identified with an x in the number, for example, 0x0000. All numbers are decimal (base 10) unless otherwise specified. Nonobvious binary numbers have the term binary enclosed in parentheses at the end of the number, for example, 0011 (binary).
|	A vertical bar in the outside margin of a page indicates that a change was made since the previous revision of this document.

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2 Pin Definitions

The highly integrated WCN3680B/WCN3660B device is available in the 79B WLNSP that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 for package details. A high-level view of the pin assignments is shown in Figure 2-1.

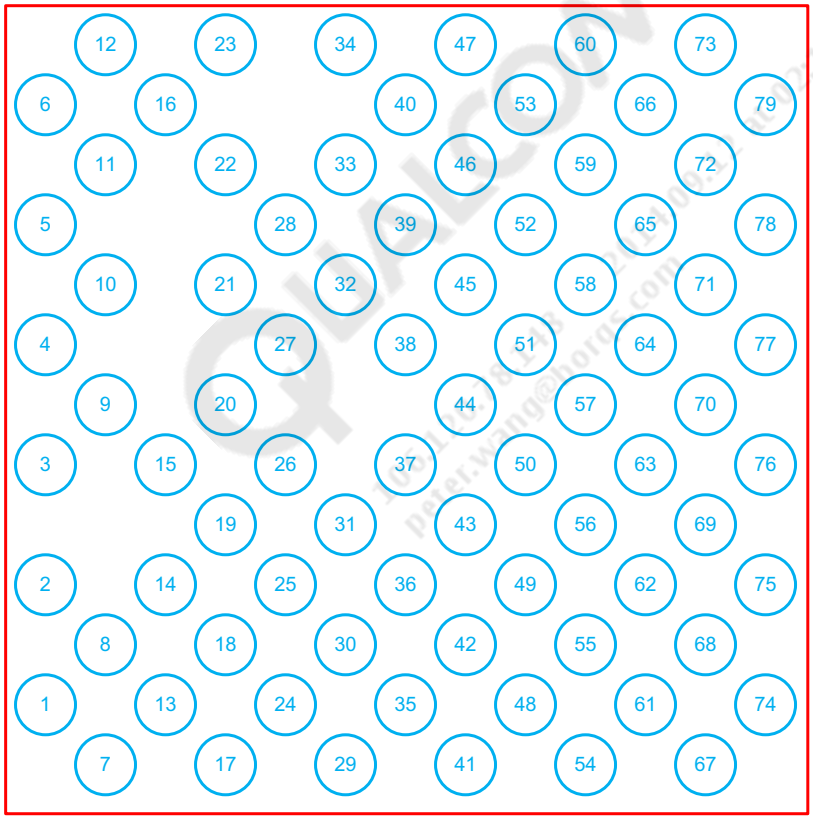

Figure 2-1 WCN3680B/WCN3660B pin assignments (top view)

The WCN3680B/WCN3660B IC pin assignment in numeric order and location is shown in Table 2-1.

Table 2-1 WCN3680B/WCN3660B IC pin assignment in numeric order and location

Ball pad number	Ball pad name	Ball pad center (x)	Ball pad center (y)	Ball pad size (x)	Ball pad size (y)
1	GND	1705.5	-1415	260	260
2	GND	1705.5	-849	260	260
3	VDD_BT_RXRF_1P3	1705.5	-283	260	260
4	VDD_BT_TXRF_3P3	1705.5	283	260	260
5	WL_BT_RFIO_2P4G	1705.5	849	260	260
6	VDD_WL_2GPA_1P3	1705.5	1415	260	260
7	VDD_BT_VCO_1P3	1422.5	-1698	260	260
8	GND	1422.5	-1132	260	260
9	VDD_WL_2GLNA_1P3	1422.5	0	260	260
10	GND	1422.5	566	260	260
11	VDD_WL_2GPA_3P3	1422.5	1132	260	260
12	GND	1422.5	1698	260	260
13	GND	1139.5	-1415	260	260
14	VDD_BT_BB_1P3	1139.5	-849	260	260
15	GND	1139.5	-283	260	260
16	WL_PDET_IN	1139.5	1415	260	260
17	VDD_BT_PLL_1P3	856.5	-1698	260	260
18	GND	856.5	-1132	260	260
19	BT_CTL	856.5	-566	260	260
20	GND	856.5	0	260	260
21	GND	856.5	566	260	260
22	GND	856.5	1132	260	260
23	GND	856.5	1698	260	260
24	BT_SSBI	573.5	-1415	260	260
25	VDD_BT_FM_DIG_1P3	573.5	-849	260	260
26	VDD_XO_1P8	573.5	-283	260	260
27	GND	573.5	283	260	260
28	NC	573.5	849	260	260
29	BT_DATA	290.5	-1698	260	260
30	VDD_DIG_1P2	290.5	-1132	260	260
31	XO_IN	290.5	-566	260	260
32	VDD_WL_LO_1P3	290.5	566	260	260
33	WL_CMD_CLK	290.5	1132	260	260
34	WL_EXTPA_CTRL1	290.5	1698	260	260
35	VDD_IO_1P8	7.5	-1415	260	260

Table 2-1 WCN3680B/WCN3660B IC pin assignment in numeric order and location (cont.)

Ball pad number	Ball pad name	Ball pad center (x)	Ball pad center (y)	Ball pad size (x)	Ball pad size (y)
36	CLK_OUT	7.5	-849	260	260
37	GND	7.5	-283	260	260
38	GND	7.5	283	260	260
39	GND	7.5	849	260	260
40	VDD_WL_UPC_1P3	7.5	1415	260	260
41	FM_DATA	-275.5	-1698	260	260
42	GND	-275.5	-1132	260	260
43	XO_OUT	-275.5	-566	260	260
44	GND	-275.5	0	260	260
45	VDD_WL_BB_1P3	-275.5	566	260	260
46	GND	-275.5	1132	260	260
47	WL_RF_DA_OUT	-275.5	1698	260	260
48	FM_SSBI	-558.5	-1415	260	260
49	WL_EXTPA_CTRL2	-558.5	-849	260	260
50	VDD_WL_PLL_1P3	-558.5	-283	260	260
51	WL_BB_QP	-558.5	283	260	260
52	WL_EXTPA_CTRL0	-558.5	849	260	260
53	GND	-558.5	1415	260	260
54	VDD_FM_RXBB_1P3	-841.5	-1698	260	260
55	GND	-841.5	-1132	260	260
56	WL_EXTPA_CTRL4	-841.5	-566	260	260
57	WL_BB_QN	-841.5	0	260	260
58	WL_BB_IP	-841.5	566	260	260
59	VDD_WL_5GPA_1P3	-841.5	1132	260	260
60	GND	-841.5	1698	260	260
61	FM_HS_RX	-1124.5	-1415	260	260
62	GND	-1124.5	-849	260	260
63	WL_CMD_SET	-1124.5	-283	260	260
64	WL_BB_IN	-1124.5	283	260	260
65	GND	-1124.5	849	260	260
66	GND	-1124.5	1415	260	260
67	GND	-1407.5	-1698	260	260
68	WL_EXTPA_CTRL3	-1407.5	-1132	260	260
69	VDD_FM_PLL_1P3	-1407.5	-566	260	260
70	WL_CMD_DATA1	-1407.5	0	260	260

Table 2-1 WCN3680B/WCN3660B IC pin assignment in numeric order and location (cont.)

Ball pad number	Ball pad name	Ball pad center (x)	Ball pad center (y)	Ball pad size (x)	Ball pad size (y)
71	WL_CMD_DATA0	-1407.5	566	260	260
72	WL_RFIO_5G/RF_5GHZ_RX	-1407.5	1132	260	260
73	VDD_WL_5GPA_3P3	-1407.5	1698	260	260
74	VDD_FM_RXFE_1P3	-1690.5	-1415	260	260
75	VDD_FM_VCO_1P3	-1690.5	-849	260	260
76	GND	-1690.5	-283	260	260
77	WL_CMD_DATA2	-1690.5	283	260	260
78	VDD_WL_5GLNA_1P3	-1690.5	849	260	260
79	GND	-1690.5	1415	260	260

2.1 I/O parameter definitions

Table 2-2 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
Z	High-impedance (high-Z) output
Pad pull details for digital I/Os	
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltages for digital I/Os	
DIO	Digital interfaces with the modem IC VDD_IO_1P8
EPA	Control signals to 5 GHz WLAN external PA (VDD_WL_5GPA_3P3)

2.2 Pin descriptions

Descriptions of all pins are presented in the following tables, organized by functional group:

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Table 2-3 Pin descriptions – WLAN functions [1]

Pad no.	Pad name	Pad voltage	Pad type vs. operating mode			Functional description
			active	standby	sleep	
RF input/output pins						
47	WL_RF_DA_OUT		AI, AO	AI, AO	AI, AO	WLAN 2 GHz and 5 GHz driver amp output port for external PA
72	WL_RFIO_5G	–	AI, AO	AI, AO	AI, AO	WLAN 5 GHz RF input/output port
16	WL_PDET_IN	–	AI	AI	AI	WLAN Tx power detector input (2.4 and 5 GHz)
–	***Also see Table 2-7 for shared WLAN + BT RF front-end pins***					
Rx/Tx analog baseband interface with modem IC						
58	WL_BB_IP	–	AI, AO	AI, AO	AI, AO	WLAN baseband differential in-phase – positive (multiplexed Rx/Tx)
64	WL_BB_IN	–	AI, AO	AI, AO	AI, AO	WLAN baseband differential in-phase – negative (multiplexed Rx/Tx)
51	WL_BB_QP	–	AI, AO	AI, AO	AI, AO	WLAN baseband differential quadrature – positive (multiplexed Rx/Tx)
57	WL_BB_QN	–	AI, AO	AI, AO	AI, AO	WLAN baseband differential quadrature – negative (multiplexed Rx/Tx)
External RF component controls						
34	WL-EXTPA_CTRL1	EPA	DO-PD	DO-PD (L)	DO-NP	WLAN external PA control bit 1 (5 GHZ) NC; an external PA is not used
49	WL_EXTPA_CTRL2	EPA	DO-PD	DO-PD (L)	DO-NP	WLAN external WLAN external PA control bit 2 (2.4 GHz) NC; an external PA is not used
56	WL_EXTPA_CTRL4	EPA	DO-PD	DO-PD (L)	DO-NP	WLAN external WLAN external PA control bit 4 (2.4 GHz) NC; an external PA is not used
68	WL_EXTPA_CTRL3	EPA	DO-PD	DO-PD (L)	DO-NP	WLAN external WLAN external PA control bit 3 (2.4 GHz) NC; an external PA is not used
52	WL-EXTPA_CTRL0	EPA	DO-PD	DO-PD (L)	DO-NP	WLAN external PA control bit 0 (5 GHZ) NC; an external PA is not used

1. Refer to Table 2-2 for parameter and acronym definitions.

Table 2-4 WLAN pad type vs. operating mode

Pad no.	Pad name	WLAN off BT/FM off	WLAN off BT/FM on	WLAN on BT/FM off	WLAN on BT/FM on	WLAN low-power mode BT/FM off	WLAN low-power mode BT/FM on	Notes
WLAN command interface with modem IC								
77	WL_CMD_DATA2	Z	DO-NP	DO-NP/ DI-PD	DO-NP/ DI-PD	Z	DO-NP	In active mode, the CMD_DATA lines will be to DO-NP, then changes to DO-PD when CMD_SET signal changes state
70	WL_CMD_DATA1	Z	DO-NP	DO-NP/ DI-PD	DO-NP/ DI-PD	Z	DO-NP	In active mode, the CMD_DATA lines will be to DO-NP, then changes to DO-PD when CMD_SET signal changes state
71	WL_CMD_DATA0	Z	DO-NP	DO-NP/ DI-PD	DO-NP/ DI-PD	Z	DO-NP	In active mode, the CMD_DATA lines will be to DO-NP, then changes to DO-PD when CMD_SET signal changes state

Table 2-4 WLAN pad type vs. operating mode (cont.)

Pad no.	Pad name	WLAN off BT/FM off	WLAN off BT/FM on	WLAN on BT/FM off	WLAN on BT/FM on	WLAN low-power mode BT/FM off	WLAN low-power mode BT/FM on	Notes
63	WL_CMD_SET	Z	DI-PD	DI-PD	DI-PD	Z	DI-PD	Z when WLAN/BT/FM is off or in power collapse, otherwise DI-PD
33	WL_CMD_CLK	Z	DI-PD	DI-PD	DI-PD	Z	DI-PD	Z when WLAN/BT/FM is off or in power collapse, otherwise DI-PD

Table 2-5 Pin descriptions – BT functions [1]

Pad no.	Pad name	Pad voltage	Pad type vs. operating mode			Functional description
			active	standby	sleep	
RF input/output pins						
–	***See Table 2-7 for shared WLAN + BT RF front-end pins***					

1. Refer to Table 2-2 for parameter and acronym definitions.

Table 2-6 BT pad type vs. operating mode

Pad no.	Pad name	BT off FM off	BT off FM on	BT on, active FM off	BT on, active FM on	BT on, idle FM off	BT on, idle FM on	Notes
BT data interface with modem IC								
29	BT_DATA	Z	Z	B-PD	B-PD	B-PD/Z	B-PD/Z	Z when WLAN is off or in power collapse, otherwise P-PD
19	BT_CTL	Z	Z	DI-PD	DI-PD	DI-PD/Z	DI-PD/Z	Z when WLAN is off or in power collapse, otherwise DI-PD
BT status and control interface with modem IC								
24	BT_SSBI	Z	Z	B-PD	B-PD	B-PD/Z	B-PD/Z	Z when WLAN is off or in power collapse, otherwise B-PD

Table 2-7 Pin descriptions – shared WLAN and BT RF front-end functions [1]

Pad no.	Pad name	Pad voltage	Pad type vs. operating mode			Functional description
			active	standby	sleep	
5	WL_BT_RFIO_2P4G	–	AI, AO	AI, AO	AI, AO	WLAN 2.4 GHz and BT RF input/output port

1. Refer to Table 2-2 for parameter and acronym definitions.

Table 2-8 Pin descriptions – FM radio functions [1]

Pad no.	Pad name	Pad voltage	Pad type vs. operating mode			Functional description
			active	standby	sleep	
RF input/output pins						
61	FM_HS_RX	–	AI	AI	AI	FM radio headset RF receiver input port

1. Refer to Table 2-2 for parameter and acronym definitions.

Table 2-9 FM pad type vs. operating mode

Pad no.	Pad name	BT off FM off	BT off FM on	BT on, active FM off	BT on, active FM on	BT on, idle FM off	BT on, idle FM on	Notes
FM data interface with modem IC								
41	FM_DATA	Z	B-PD	Z	B-PD	Z	B-PD	
FM status and control interface with modem IC								
48	FM_SSBI	Z	B-PD	Z	B-PD	Z	B-PD	

Table 2-10 Pin descriptions – top-level support functions [1]

Pad no.	Pad name	Pad voltage	Pad type vs. operating mode			Functional description
			active	standby	sleep	
31	XO_IN	–	AI	AI	AI	Dual function: ■ XTAL input connection if external crystal is used ■ XO input if external clock source is used
43	XO_OUT	–	AO	AO	AO	Dual function: ■ XTAL output connection if external crystal is used ■ Do not connect (DNC) if external clock source is used
36	CLK_OUT	DIO	DO-PD	DO-PD	DO-NP	24 MHz clock output to WCN subsystem block in the host for synchronization

1. Refer to Table 2-2 for parameter and acronym definitions.

Table 2-11 Pin descriptions – No connection, do not connect, and reserved pins

Pad no.	Pad name	Functional description
28	NC	No connect; not connected internally

Table 2-12 Pin descriptions – power supply pins

Pad no.	Pad name	Functional description
25	VDD_D_FM_DIG_1P3	Power for BT/FM digital circuits (1.3 V)
14	VDD_BT_BB_1P3	Power for BT baseband circuits (1.3 V)
17	VDD_BT_PLL_1P3	Power for BT PLL circuits (1.3 V)
3	VDD_BT_RXRF_1P3	Power for BT RF receiver circuits (1.3 V)
4	VDD_BT_TXRF_3P3	Power for BT RF transmitter circuits (3.3 V)
7	VDD_BT_VCO_1P3	Power for BT VCO circuits (1.3 V)
30	VDD_DIG_1P2	Output voltage from WCN3680B/WCN3660B internal LDO for external decoupling capacitor connections
35	VDD_IO_1P8	Power for WCN digital I/O circuits (1.8 V)
69	VDD_FM_PLL_1P3	Power for FM PLL circuits (1.3 V)
54	VDD_FM_RXBB_1P3	Power for FM baseband receiver circuits (1.3 V)
74	VDD_FM_RXFE_1P3	Power for FM receiver front-end circuits (1.3 V)
75	VDD_FM_VCO_1P3	Power for FM VCO circuits (1.3 V)
9	VDD_WL_2GLNA_1P3	Power for WLAN 2.4 GHz LNA circuits (1.3 V)
6	VDD_WL_2GPA_1P3	Power for WLAN 2.4 GHz PA circuits (1.3 V)
11	VDD_WL_2GPA_3P3	Power for WLAN 2.4 GHz PA circuits (3.3 V)
78	VDD_WL_5GLNA_1P3	Power for WLAN 5 GHz LNA circuits (1.3 V)
59	VDD_WL_5GPA_1P3	Power for WLAN 5 GHz PA circuits (1.3 V)
73	VDD_WL_5GPA_3P3	Power for WLAN 5 GHz PA circuits (3.3 V)
45	VDD_WL_BB_1P3	Power for WLAN baseband circuits (1.3 V)
32	VDD_WL_LO_1P3	Power for WLAN LO circuits (1.3 V)
50	VDD_WL_PLL_1P3	Power for WLAN PLL circuits (1.3 V)
40	VDD_WL_UPC_1P3	Power for WLAN upconverter circuits (1.3 V)
26	VDD_XO_1P8	Power for XO circuits (1.8 V)

Table 2-13 Pin descriptions – ground pins

Pad no.	Pad name	Functional description
1, 2, 8, 10, 12, 13, 15, 18, 20, 21, 22, 23, 27, 37, 38, 39, 42, 44, 46, 53, 55, 60, 62, 65, 66, 67, 76, 79	GND	Ground

3 Electrical Specifications

3.1 Absolute maximum ratings

Operating the WCN3680B/WCN3660B IC under conditions beyond its absolute maximum ratings (Table 3-1) could damage the device. Absolute maximum ratings are limiting values to consider individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, is not guaranteed or implied. Exposure could affect device reliability.

Table 3-1 Absolute maximum ratings [1]

Parameter		Min	Max	Units
VDD_xxx_1P3	Power for WCN analog, digital, and RF core circuits	-0.5	3.0	V
VDD_IO_1P8	Power for WCN digital I/O circuits	-0.5	3.0	V
VDD_XO_1P8	Power for WCN XO circuits	-0.5	3.0	V
VDD_xxx_3P3	Power for WLAN 5 GHz and 2.4 GHz PA driver amplifier circuits	-0.5	3.6	V
V_{IN}	Voltage applied to any non-power I/O pin [2]	-0.5	V_{DDX} + 0.3	V
ESD protection – see Section 7.1.				
Thermal considerations – see Section 7.1.				

1. The characters “xxx” are used in this table to indicate several missing characters in a power-supply pin’s name. For example, the parameter values listed for VDD_xxx_1P3 apply to VDD_BT_FM_DIG_1P3, VDD_BT_BB_1P3, and so on.
2. V_{DDX} is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.2 Operating conditions

Operating conditions include parameters under user control, such as the power-supply voltage and ambient temperature. If the absolute maximum ratings have never been exceeded, the WCN3680B/WCN3660B device meets all performance specifications listed in Section 3.3 through Section 3.11 when used within the operating conditions, unless otherwise noted in those sections.

Table 3-2 Operating conditions [1]

Parameter		Min	Typ	Max	Units
VDD_xxx_1P3	Power for WCN analog, digital, and RF core circuits	1.25	1.30	1.38	V
VDD_IO_1P8	Power for WCN digital I/O circuits	1.70	1.80	1.90	V
VDD_XO_1P8	Power for XO circuits	1.70	1.80	1.90	V
VDD_xxx_3P3	Power for WLAN 5 GHz and 2.4 GHz PA driver amplifier circuits	2.90	3.30	3.37	V
T_{OP}	Operating temperature	-30	25	85	°C

1. The characters “xxx” are used in this table to indicate several missing characters in a power-supply pin’s name. For example, the parameter values listed for VDD_xxx_1P3 apply to VDD_BT_FM_DIG_1P3, VDD_BT_BB_1P3, and so on.

3.3 DC power characteristics

3.3.1 Power mode definitions

The WCN3680B/WCN3660B device’s DC power consumption, expressed in terms of supply current, is specified as the typical total input current into the device during active operation. This is the current drawn from the primary power source that powers the internal regulator and other circuits.

Values specified in this section are estimates to use as general guidelines for WCN3680B/WCN3660B IC product designs. The stated modes assume that the WLAN, Bluetooth + FM wireless technology circuits are operating in compliance with applicable standards. The average power consumption values for different operating modes depend on the system state.

3.3.2 Maximum currents

Maximum current information is intended for use by designers to determine supply-source requirements, and for board designers to calculate trace widths.

This information will be included in future revisions of this document.

3.3.3 Power consumption

Table 3-3 lists the typical measured supply currents into the WCN3680B/WCN3660B devices. They are the average measurement based on operation at room temperature (+25ºC) using default settings and nominal supply voltages, such as VDD_XO_1P8 = 1.8 V, VDD_IO_1P8 = 1.8 V, VDD_xxx_1P3 = 1.3 V, and VDD_xxx_3P3 = 3.3 V.

Table 3-3 Input power supply current from primary source

Mode	1.8 V IO	1.8 V XO	VDD_xxx_1P3	VDD_xxx_3P3[1]
Shutdown	1.2 µA	0.5 µA	35 µA	2 µA
BT current consumption				
BT Tx class 2, 4 dBm	500 µA	2 mA	50 mA	0
BT Tx class1, 11 dBm	500 µA	2 mA	35 mA	30 mA
BT Rx	2.4 mA	2 mA	25 mA	0
FM current consumption				
FM Rx	400 µA	2 mA	15 mA	1 µA
WLAN current consumption				
2.4 GHz				
2.4G, 11b, 11 Mbps, 19 dBm	1.32 mA	2.0 mA	107 mA	180 mA
2.4G, 11g, 6 Mbps, 17 dBm	1.32 mA	2.0 mA	98 mA	143 mA
2.4G, 11g, 6 Mbps, 15 dBm	1.32 mA	2.0 mA	96 mA	117 mA
2.4G, 11n, 72 Mbps, 13 dBm	1.32 mA	2.0 mA	95 mA	100 mA
WLAN Rx 2G	24 µA	2.18 mA	65 mA	41 µA
5 GHz				
5G, 11a, 6 Mbps, 16 dBm	1.33 mA	7.0 mA	198 mA	180 mA
5G, 11a, 54 Mbps, 14 dBm	1.33 mA	7.0 mA	196 mA	151 mA
5G, 11a, 72 Mbps, 12 dBm	1.33 mA	7.0 mA	195 mA	133 mA
WLAN Rx 5G	24 µA	6.6 mA	75 mA	40 µA

1. For internal PA only

3.4 Power sequencing

The WCN3680B/WCN3660B device requires the following powerup sequence:

- For MSM8916: 1.3 V(S3) → 1.8_IO (L5) → 1.8V_XO(L7) → 3.3V_PA (L9)
- For all other platforms:
  - Either VDD_XO_1P8 or VDD_IO_1P8
  - Either VDD_xxx_1P3 or VDD_xxx_3P3

To power down the device, the following sequence is required:

- For MSM8916: 3.3V_PA (L9) → 1.8V_IO (L5) → 1.8_XO (L7) → 1.3V(S3)
- For all other platforms:
  - VDD_xxx_1P3 and VDD_xxx_3P3
  - Either VDD_XO_1P8 or VDD_IO_1P8

NOTE If 1.3 V is off before 3.3 V, the interval between 1.3 V off and 3.3 V off should be very short. Any leakage current can be ignored.

3.5 WCN3680B/WCN3660B internal LDO regulator

The WCN3680B/WCN3660B has an on-chip LDO regulator to provide power supply to the WCN3680B/WCN3660B 1.2 V digital core. The integrated LDO input voltage is applied from the VDD_XO_1P8 voltage. The output pin of this internal LDO is VDD_DIG_1P2 (pin 30). The output at this pin is used to connect decoupling capacitors to reduce supply noise. The WCN3680B/WCN3660B device integrated regulator is intended for use with an on-chip load only. They are not designed to supply external loads.

3.6 Digital logic characteristics

Specifications for the digital I/Os depend on the associated supply voltage (identified as V_{IO} in Table 3-4).

Table 3-4 Baseband digital I/O characteristics

Parameter		Comments	Min	Typ	Max	Units
V_{IH}	High-level input voltage		0.70 · V_{IO}	–	V_{IO} + 0.3	V
V_{IL}	Low-level input voltage		-0.3	–	0.30 · V_{IO}	V
V_{SHYS}	Schmitt hysteresis voltage		–	300	–	mV
I_{IH}	Input high leakage current	V_IN = V_{IO} max	-1.0	–	1.0	µA
I_{IL}	Input low leakage current	V_IN = 0 V; supply = V_{IO} max	-1.0	–	1.0	µA
R_{PULL}	Input pull resistor [1]	Up or down	–	375 k	–	kΩ
V_{OH}	High-level output voltage		V_{IO} - 0.4	–	V_{IO}	V

Table 3-4 Baseband digital I/O characteristics (cont.)

Parameter		Comments	Min	Typ	Max	Units
V_{OL}	Low-level output voltage		0	–	0.4	V
I_{OH}	High-level output current		1.0	–	–	mA
I_{OL}	Low-level output current		–	–	-1.0	mA
C_{IN}	Input capacitance [2]		–	–	5	pF

1. Resistor values may drop by 50% when 3.3 V I/O is used.
2. Guaranteed by design but not 100% tested.

3.7 Timing characteristics

Specifications for the device timing characteristics are included, where appropriate, under each function's section, along with its other performance specifications. Some general comments about timing characteristics are included here.

NOTE All WCN3680B/WCN3660B devices are characterized with actively terminated loads, so all baseband timing parameters in this document assume no bus loading. This is described in Section 3.7.2.

3.7.1 Timing diagram conventions

Figure 3-1 shows the conventions used within timing diagrams throughout this document.

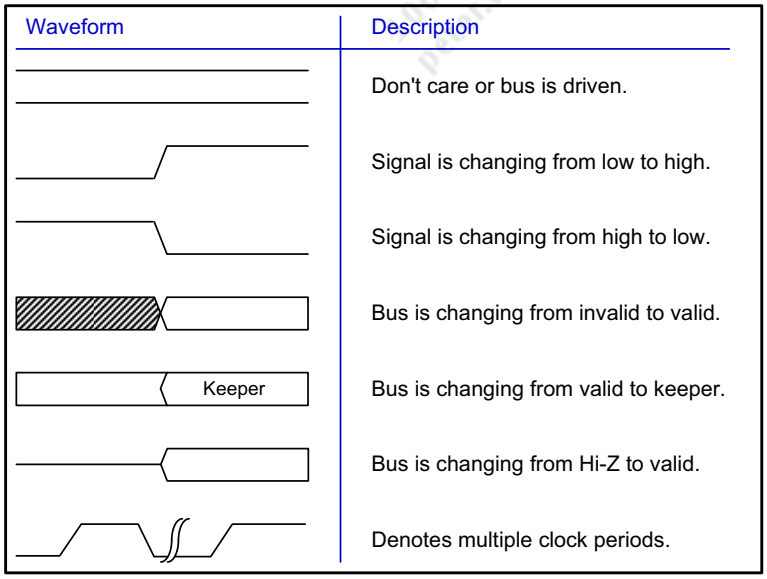


Figure 3-1 Timing diagram conventions

3.7.2 Rise and fall time specifications

The testers that characterize WCN3680B/WCN3660B devices have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). Figure 3-2 shows the impact that different external load conditions have on rise and fall times.

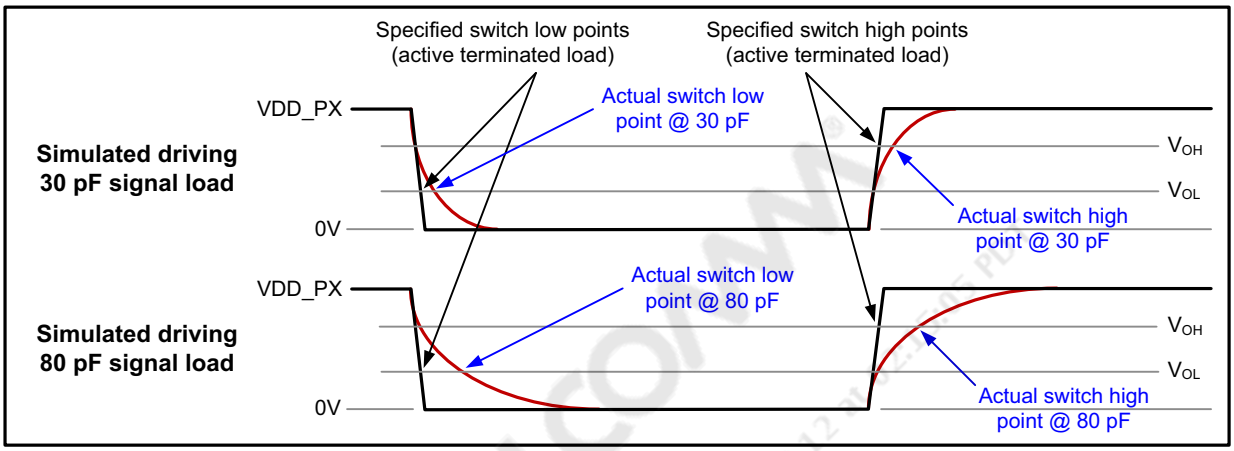


Figure 3-2 Rise and fall times under different load conditions

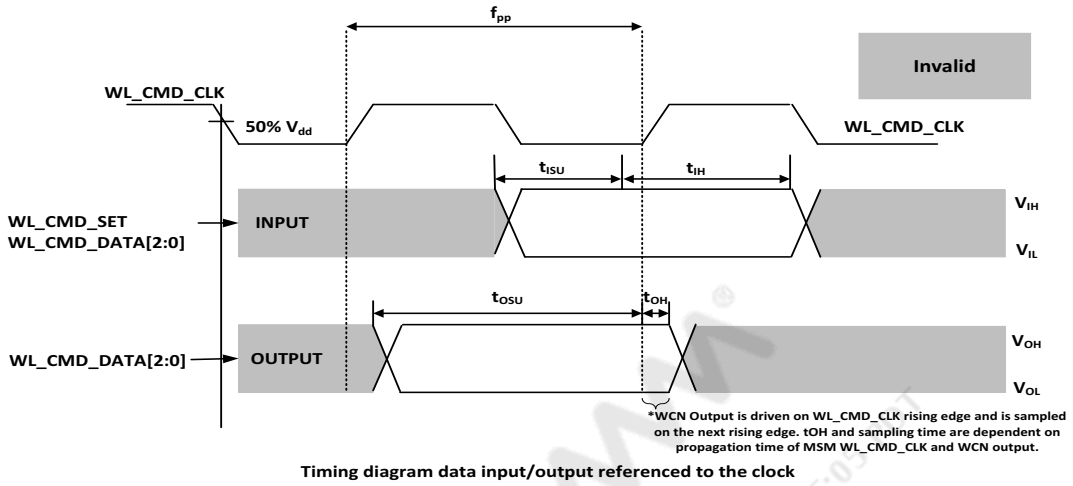
To account for external load conditions, rise or fall times must be added to parameters that start timing at the WCN device and terminate at an external device (or vice versa). Adding these rise and fall times is equivalent to applying capacitive load derating factors, and Table 3-5 lists the recommended derating factors.

Table 3-5 Capacitive load derating factors

Parameter	1.8 V I/O Drive = 1.0 mA	Units
Rise time, 10% to 90%	0.29 max	ns/pF
Fall time, 90% to 10%	0.19 max	ns/pF

3.8 Top-level support

Top-level support consists of the 5-wire interface, the master reference clock, and the DC power gate and distribution. Figure 3-3 shows the timing diagram for data input.



Timing diagram data input/output referenced to the clock

Figure 3-3 Timing diagram – data input and output

Table 3-6 WCN3680B/WCN3660B read and write for 5-wire interface between the WCN3680B/WCN3660B and MSM devices

Parameter	Symbol	Min	Units	Comments
Input setup time	t_{ISU}	3	ns	
Input hold time	t_{IH}	1	ns	
Output setup time	t_{OSU}	2	ns	
Output hold	t_{OH}	0.37	ns	

Table 3-7 Typical duty cycle

Frequency (f_{PP})	60 MHz[1]	30 MHz[1]	Units	Comments
Typical duty cycle	12.5/50[2]	25/50[2]	%	MSM/APQ chipset dependent. See note 2.

1. The WL_CMD_CLK frequency can be 30 MHz or 60 MHz, depending on the command type.
2. For MSM8960, MSM8960PRO, MSM8x30, and APQ8064 ICs, the duty cycle for WL_CMD_CLK is 12.5% for 30 MHz and 25% for 60 MHz clock frequencies. For other MSM devices, the WL_CMD_CLK duty cycle is 50%.

3.8.1 I/O block

Modem IC interfaces for WLAN, BT, and FM radio are supported by this block; pertinent specifications are covered within Section 3.5.

3.8.2 Master reference clock requirements

For 2.4 GHz WLAN operation only, the WCN3660B device requires one 19.2 MHz clock signal that can be generated externally (usually by the PMIC), or can be generated by the external 19.2 MHz crystal. This master reference clock (MRC) is the timing source for all operational functions during active modes. When an external source is used, that signal must be AC-coupled into the XO_IN pin.

For single-band operation at 5.0 GHz or dual-band operation at 2.4 and 5.0 GHz, the WCN3680B/WCN3660B device requires a 48.0 MHz clock from an external crystal. This clock signal is required due to more stringent phase noise requirements when operating the device at 5.0 GHz.

Table 3-8 lists the requirements for operation at 5.0 GHz only or operation at both 2.4 GHz and 5.0 GHz (MRC = 48 MHz).

Table 3-8 Reference requirements

Parameter	Condition	Min	Typ	Max	Units
19.2 MHz TCXO					
Output frequency		–	19.2	–	MHz
Frequency variation over temperature		-5	–	5	ppm
Duty cycle of output signal		43.5	50	55	%
Voltage swing		0.8		2.0	V_{pp}
Output phase noise	f = 1 kHz	–	-130	-128	dBc/Hz
	f = 10 kHz	–	-144	-142	dBc/Hz
	f = 100 kHz	–	-151	-148	dBc/Hz
	f = 1 MHz	–	-152	-150	dBc/Hz
Output spur specification		–	–	-30	dBc
48 MHz XTAL **– See *48 MHz Crystal for 5 GHz WLAN Connectivity Products Mini-Specification* (80-N8644-2) for the WCN3680B/WCN3660B 48 MHz crystal mini-specifications.**					
48 MHz XO					
Operating frequency		–	48	–	MHz

3.8.3 DC power gating and distribution

See Section 3.3 and Section 3.4.

3.9 WLAN RF circuits

The following sections provide performance specifications for the WLAN RF transmitter and receiver circuits over the full operating power-supply voltage range and temperature range shown in Table 3-2. **Unless noted otherwise, all measurements are taken at the chip RF I/O pins and all typical performance specifications, are based on operation at room temperature (+25°C) using default parameter settings and nominal supply voltages, such as VDD_xxx_1P3 = 1.3 V, VDD_IO_1P8 = 1.8 V, VDD_XO_1P8 = 1.8 V, and VDD_xxx_3P3 = 3.3 V.** Maximum and minimum ratings are guaranteed specifications for production-qualified parts. The WCN3680B/WCN3660B device complies with 802.11d requirements, where transmit output power is limited per country code. Figure 3-4 and Figure 3-5 illustrate dual-band and single-band RF connections of the WCN3680B/WCN3660B using SCPC as the default power-control mechanism.

The WCN3680B/WCN3660B supports an external RF coupler or SCPC power control. The default option in the WCN3680B/WCN3660B is SCPC. For designs that require very tight output power variation range, an external coupler option is available.

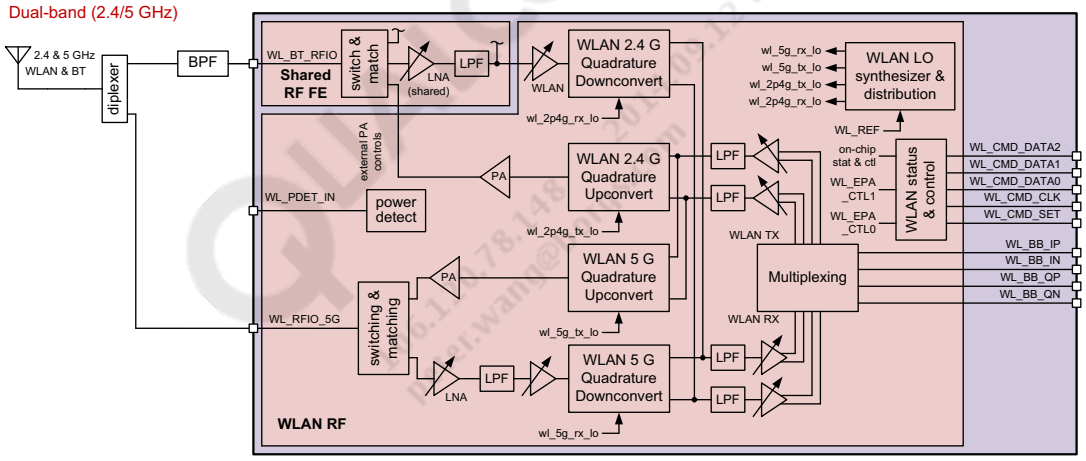


Figure 3-4 WCN3680B/WCN3660B RF connections for dual-band (2.4 GHz and 5.0 GHz) using SCPC

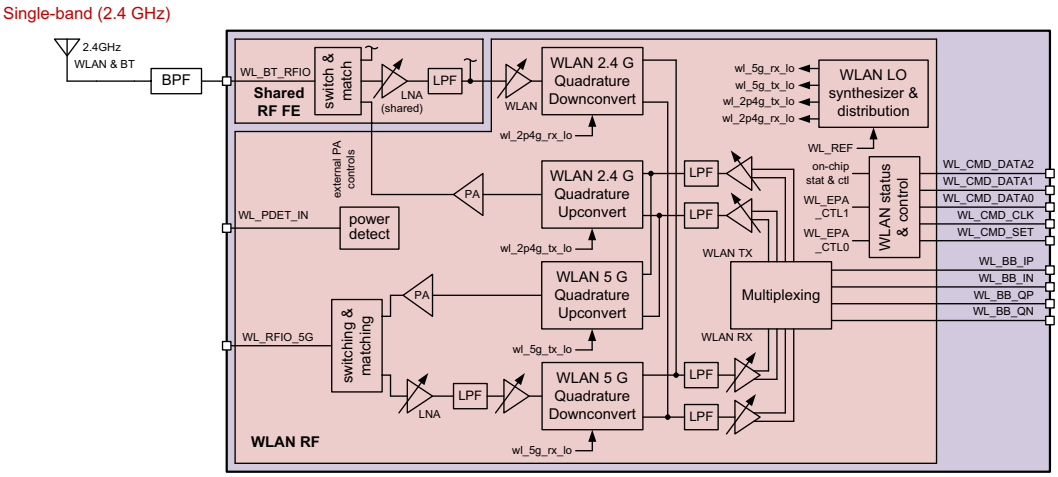


Figure 3-5 WCN3680B/WCN3660B RF connections for single-band (2.4 GHz) using SCPC

3.9.1 WLAN 2.4 GHz RF Tx

The WCN3680B/WCN3660B IC WLAN RF transmitter is specified for WLAN 802.11n and 802.11ac standards, while guaranteeing FCC transmit-mask compliance across the band.

3.9.1.1 Internal PA

Table 3-9 WLAN 2.4 GHz RF Tx performance specifications [1]

Parameter	Condition	Min	Typ	Max	Units
RF output frequency range		2.4	–	2.496	GHz
11b (1 Mbps)	Mask and EVM compliant	–	20.8	–	
11b (11 Mbps)	Mask and EVM compliant	–	20.8	–	
11g (6 Mbps)	Mask and EVM compliant	–	18.8	–	dBm
11g (54 Mbps)	Mask and EVM compliant	–	16.8	–	dBm
11n, HT20 (MCS0)	Mask and EVM compliant	–	17.8	–	dBm
11n, HT20 (MCS7)	Mask and EVM compliant	–	15.2	–	dBm
11ac, VHT20 (MCS0)	WCN3680B only; mask and EVM compliant	–	17.8	–	dBm
11ac, VHT20 (MCS7)	WCN3680B only; mask and EVM compliant	–	15.2	–	dBm
11ac, VHT20 (MCS8)	WCN3680B only; mask and EVM compliant	–	14.8	–	dBm
Tx output range at antenna	At any rate	8	–	20	dBm
Self-calibrated power control (SCPC)	At room temperature and VSWR ≤ 1.5:1	–	±2.0	–	dB
Closed-loop power control (CLPC) with external coupler	At room temperature and VSWR ≤ 1.5:1	–	±1.1	–	dB

1. Refer to the IEEE 802.11 specifications for transmit spectrum limits:
   - 802.11b mask (18.4.7.3)
   - 802.11g mask (19.5.4)
   - 802.11g EVM (17.3.9.6.3)
   - 802.11n HT20 mask (20.3.21.1)
   - 802.11n HT20 EVM (20.3.21.7.3)
   - 802.11ac mask (22.3.18.1, draft 4.0)
   - 802.11ac EVM (22.3.18.4.3 and 22.3.18.4.4, draft 4.0)

NOTE HT40, VHT40, and VHT80 are not supported in 2.4 GHz.

3.9.1.2 WLAN 2.4 GHz RF Tx desensitization of WAN receivers

The WLAN transmissions can leak into the handset's wide area network (WAN) and GPS receivers and cause desensitization, potentially limiting concurrency. To evaluate concurrency limitations, the following factors were considered:

- WLAN to WAN
  - Worst-case WLAN-to-WAN antenna isolation = 10 dB
  - Tolerable WAN desensitization = 0.3 dB
  - WAN receiver noise figure = 6 dB
- WLAN to GPS
  - Worst-case WLAN-to-GPS antenna isolation = 10 dB
  - Tolerable GPS receiver desensitization = 0.2 dB
  - GPS receiver noise figure = 3 dB
- WLAN transmitter characteristics
  - WLAN effective isotropic radiated power (EIRP) = 15 dBm
  - A highly selective bandpass filter (integrated in a FEM) is shared by Tx and Rx

The resulting WLAN Tx requirements for WAN concurrency are summarized in Table 3-10.

Table 3-10 WLAN RF Tx emission specifications for WAN concurrency [1]

WAN or GPS band	Frequency range	Max Tx level in Rx band
GPS	1574 to 1577 MHz	-136 dBm/Hz
CDMA bands		
Cell (BC0)	869 to 894 MHz	-128 dBm/Hz
PCS (BC1)	1930 to 1990 MHz	-128 dBm/Hz
JCDMA (BC3)	832 to 870 MHz	-128 dBm/Hz
KPCS (BC4)	1840 to 1870 MHz	-128 dBm/Hz
IMT (BC6)	2110 to 2170 MHz	-128 dBm/Hz
AWS (BC15)	2110 to 2155 MHz	-128 dBm/Hz
GSM bands		
GSM 850	869 to 894 MHz	-128 dBm/Hz
GSM 900	925 to 960 MHz	-128 dBm/Hz
GSM 1800	1805 to 1880 MHz	-128 dBm/Hz
GSM 1900	1930 to 1990 MHz	-128 dBm/Hz

1. Specifications apply under the following conditions: 11g signal at 17.5 dBm, 45°C ambient temperature, over voltage, and over process.

3.9.2 WLAN 2.4 GHz RF Rx

The WCN3680B/WCN3660B device WLAN RF receiver is specified for the WLAN 802.11n and 802.11ac standard.

3.9.2.1 WLAN 2.4 GHz RF Rx performance

Table 3-11 WLAN 2.4 GHz RF Rx performance specifications

Parameter	Condition	Min	Typ	Max	Units
RF output frequency range		2.4	–	2.496	GHz
11b (1 Mbps)	At WCN3680B/WCN3660B	–	-97.8	–	dBm
11b (11 Mbps)	At WCN3680B/WCN3660B	–	-89.8	–	dBm
11g (6 Mbps)	At WCN3680B/WCN3660B	–	-91.8	–	dBm
11g (54 Mbps)	At WCN3680B/WCN3660B	–	-75.1	–	dBm
11n, HT20 (MCS0)	At WCN3680B/WCN3660B	–	-91.8	–	dBm
11n, HT20 (MCS7)	At WCN3680B/WCN3660B	–	-73.5	–	dBm
11ac, VHT20 (MCS0)	At WCN3680B only	–	-91.8	–	dBm
11ac, VHT20 (MCS7)	At WCN3680B only	–	-73.5	–	dBm
11ac, VHT20 (MCS8)	At WCN3680B only	–	-66.9	–	dBm

NOTE HT40, VHT40, and VHT80 are not supported in 2.4 GHz.

3.9.2.2 WLAN 2.4 GHz Rx desense due to WAN concurrency

The handset's WAN transmissions can leak into the WLAN receiver and cause desensitization. Table 3-12, Table 3-13, and Table 3-14 characterize the WLAN desense due to WAN transmissions. The following conditions apply:

- The desensitization is limited to 1 dB in all test cases.
- The antenna isolation (WAN Tx to WLAN Rx) is assumed to be 10 dB in all cases.
- Only the WAN Tx channel power is included; other Tx levels such as harmonics and spurious emissions are not included.

Table 3-12 WLAN 2 GHz sensitivity degradation with WAN blockers

WAN, aggressor					WLAN, victim				WLAN desense			
Band		CH_ID	Frequency	WAN output power	Mode	Data rate	CH_ID	Frequency	WAN power at WLAN antenna	Coex. filter attn. [1]	WAN power at WCN 3660 input	Desense caused by blocker
WCDMA	BC1	9888	1977.6 MHz	23 dBm	11g	54 Mbps	6	2437 MHz	13 dBm	43 dB	-30 dBm	<1.0 dB
	BC2	9538	1907.6 MHz	23 dBm					13 dBm	41 dB	-28 dBm	<1.0 dB
	BC5	4233	846.6 MHz	23 dBm					13 dBm	40 dB	-27 dBm	<1.0 dB
	BC8	2863	912.6 MHz	23 dBm					13 dBm	39 dB	-26 dBm	<1.0 dB
GSM	GSM850	251	848.8 MHz	33 dBm	11g	54 Mbps	6	2437 MHz	23 dBm	40 dB	-17 dBm	<1.0 dB
	GSM900	124	914.8 MHz	33 dBm					23 dBm	39 dB	-16 dBm	<1.0 dB
	DCS1800	885	1784.8 MHz	30 dBm					20 dBm	38 dB	-18 dBm	<1.0 dB
	PCS1900	810	1909.8 MHz	30 dBm					20 dBm	41 dB	-21 dBm	<1.0 dB

1. Not a requirement, but attenuations are measured on a particular board.

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Table 3-13 WLAN 5G sensitivity degradation with WAN blockers - Part 1

WAN, aggressor					WLAN, victim				WLAN desense			
Band		CH_ID	Frequency	WAN output power	Mode	Data rate	CH_ID	Frequency	WAN power at WLAN antenna	Diplexer attn. [1]	WAN power at WCN 3660 input	Desense caused by blocker
WCDMA	BC1	9888	1977.6 MHz	23 dBm	11a	54 Mbps	44	5220 MHz	13 dBm	59 dB	-46 dBm	<1.0 dB
							60	5300 MHz	13 dBm	59 dB	-46 dBm	<1.0 dB
							120	5600 MHz	13 dBm	59 dB	-46 dBm	<1.0 dB
							157	5785 MHz	13 dBm	59 dB	-46 dBm	<1.0 dB
WCDMA	BC2	9538	1907.6 MHz	23 dBm	11a	54 Mbps	44	5220 MHz	13 dBm	58 dB	-45 dBm	<1.0 dB
							60	5300 MHz	13 dBm	58 dB	-45 dBm	<1.0 dB
							120	5600 MHz	13 dBm	58 dB	-45 dBm	<1.0 dB
							157	5785 MHz	13 dBm	58 dB	-45 dBm	<1.0 dB
WCDMA	BC5	4233	846.6 MHz	23 dBm	11a	54 Mbps	44	5220 MHz	13 dBm	40 dB	-27 dBm	<1.0 dB
							60	5300 MHz	13 dBm	40 dB	-27 dBm	<1.0 dB
							120	5600 MHz	13 dBm	40 dB	-27 dBm	<1.0 dB
							157	5785 MHz	13 dBm	40 dB	-27 dBm	<1.0 dB
WCDMA	BC8	2863	912.6 MHz	23 dBm	11a	54 Mbps	44	5220 MHz	13 dBm	40 dB	-27 dBm	<1.0 dB
							60	5300 MHz	13 dBm	40 dB	-27 dBm	<1.0 dB
							120	5600 MHz	13 dBm	40 dB	-27 dBm	<1.0 dB
							157	5785 MHz	13 dBm	40 dB	-27 dBm	<1.0 dB

1. Not a requirement, but attenuations are measured on a particular board.

Table 3-14 WLAN 5G sensitivity degradation with WAN blockers - Part 2

WAN, aggressor					WLAN, victim				WLAN desense			
Band		CH_ID	Frequency	WAN output power	Mode	Data rate	CH_ID	Frequency	WAN power at WLAN antenna	Diplexer attn. [1]	WAN power at WCN 3660 input	Desense caused by blocker
GSM	GSM 850	251	848.8 MHz	33 dBm	11a	54 Mbps	44	5220 MHz	23 dBm	40 dB	-17 dBm	<1.0 dB
							60	5300 MHz	23 dBm	40 dB	-17 dBm	<1.0 dB
							120	5600 MHz	23 dBm	40 dB	-17 dBm	<1.0 dB
							157	5785 MHz	23 dBm	40 dB	-17 dBm	<1.0 dB
GSM	GSM 900	124	914.8 MHz	33 dBm	11a	54 Mbps	44	5220 MHz	23 dBm	40 dB	-17 dBm	<1.0 dB
							60	5300 MHz	23 dBm	40 dB	-17 dBm	<1.0 dB
							120	5600 MHz	23 dBm	40 dB	-17 dBm	<1.0 dB
							157	5785 MHz	23 dBm	40 dB	-17 dBm	<1.0 dB
GSM	DCS 1800	885	1784.8 MHz	30 dBm	11a	54 Mbps	44	5220 MHz	20 dBm	55 dB	-35 dBm	<1.0 dB
							60	5300 MHz	20 dBm	55 dB	-35 dBm	<1.0 dB
							120	5600 MHz	20 dBm	55 dB	-35 dBm	<1.0 dB
							157	5785 MHz	20 dBm	55 dB	-35 dBm	<1.0 dB
GSM	PCS 1900	810	1909.8 MHz	30 dBm	11a	54 Mbps	44	5220 MHz	20 dBm	59 dB	-39 dBm	<1.0 dB
							60	5300 MHz	20 dBm	59 dB	-39 dBm	<1.0 dB
							120	5600 MHz	20 dBm	59 dB	-39 dBm	<1.0 dB
							157	5785 MHz	20 dBm	59 dB	-39 dBm	<1.0 dB

1. Not a requirement, but attenuations measured on a particular board.

3.9.3 WLAN 5 GHz RF Tx

The WCN3680B/WCN3660B IC RF transmitter integrates a 5 GHz power amplifier designed to comply with FCC transmit-mask and mandatory EVM levels defined in 802.11n and 802.11ac (WCN3680-only) IEEE standards.

The WCN3680B/WCN3660B IC also supports the use of an external 2 GHz and 5 GHz PA for applications requiring higher transmit power.

3.9.3.1 Internal PA

Table 3-15 WLAN 5 GHz RF Tx performance specifications [1]

Parameter	Condition	Min	Typ	Max	Units
RF output frequency range		4.9	-	5.85	GHz
11a (6 Mbps)	Mask and EVM compliant	–	17.6	–	dBm
11a (54 Mbps)	Mask and EVM compliant	–	15.6	–	dBm
11n, HT20 (MCS0)	Mask and EVM compliant	–	16.6	–	dBm
11n, HT20 (MCS7)	Mask and EVM compliant	–	14.6	–	dBm
11n, HT40 (MCS0)	Mask and EVM compliant	–	15.6	–	dBm
11n, HT40 (MCS7)	Mask and EVM compliant	–	13.6	–	dBm
11ac, VHT20 (MCS0)	WCN3680B only; mask and EVM compliant	–	16.6	–	dBm
11ac, VHT20 (MCS7)	WCN3680B only; mask and EVM compliant	–	14.6	–	dBm
11ac, VHT20 (MCS8 [2])	WCN3680B only; mask and EVM compliant	–	13.6	–	dBm
11ac, VHT40 (MCS0)	WCN3680B only; mask and EVM compliant	–	15.6	–	dBm
11ac, VHT40 (MCS7)	WCN3680B only; mask and EVM compliant	–	13.6	–	dBm
11ac, VHT40 (MCS8 [2])	WCN3680B only; mask and EVM compliant	–	12.6	–	dBm
11ac, VHT80 (MCS0)	WCN3680B only; mask and EVM compliant	–	14.6	–	dBm
11ac, VHT80 (MCS7)	WCN3680B only; mask and EVM compliant	–	12.6	–	dBm
11ac, VHT80 (MCS8 [2])	WCN3680B only; mask and EVM compliant	–	11.6	–	dBm
Tx output range at antenna	At any rate	8	–	20	dBm
Self-calibrated power control (SCPC)	At room temperature and VSWR ≤ 1.5:1	–	±2.0	–	dB
Closed-loop power control (CLPC) with external coupler	At room temperature and VSWR ≤ 1.5:1	–	±1.1	–	dB

1. MCS9 is an optional 11ac data rate. If MCS9 is an OEM product requirement, use the external FEM.
2. MCS8 is an optional 11ac data rate.

3.9.3.2 External PA

For applications requiring higher transmit power in the 2 GHz and 5 GHz bands, the WCN3680B/WCN3660B device supports the option for an external PA for 2 GHz and 5 GHz paths. In this configuration, the WCN's digital amplifier output is routed to pin 47 to bypass the internal PA. If using an external PA for 5G, the WL_RFIO_5G pin 72 is set to Rx mode only, and if using an external PA for 2G, the WL_BT_RFIO_2P4G pin 5 is set to WLAN Rx 2 GHz and BT Tx/Rx paths. The internal PAs are turned off to allow external front-end modules (FEM) to be used as the primary 2G and 5G amplifiers.

By using external FEMs for the 2G and 5G paths, WCN3660B Wi-Fi performance achieves higher output power than the internal PA case. For WCN3680B, using an external FEM achieves compliance with the MCS9 data rates per the IEEE 802.11ac specification. In addition to the modified 2G and 5G RF configuration, the WCN device also enables five RF control pins, depending on which bands have an external FEM enabled. These pins are WL_EXTPA_CTRL0 (pin 52), WL_EXTPA_CTRL1 (pin 34) for 5 GHz FEM control, and WL_EXTPA_CTRL2 (pin 49), WL_EXTPA_CTRL3 (pin 68), and WL_EXTPA_CTRL4 (pin 56) for 2 GHz FEM control. All of these pins are sourced from the 5G PA supply voltage. Each of the five pins is intended to be used as a control line for the front-end hardware and to have software-configurable polarity.

Refer to the *WCN3660/WCN3680(A) Reference Schematic* (80-WL005-43) and the *WCN36x0(A) NV Guide* (80-WL300-30) for reference schematics and a list of recommended FEMs.

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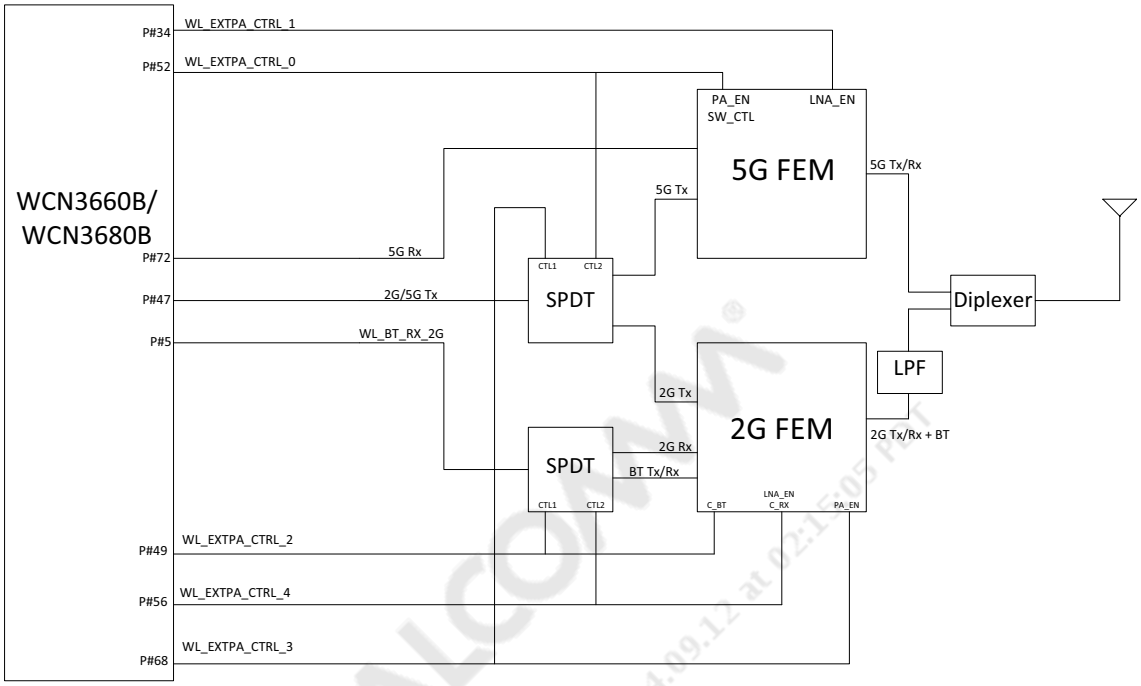
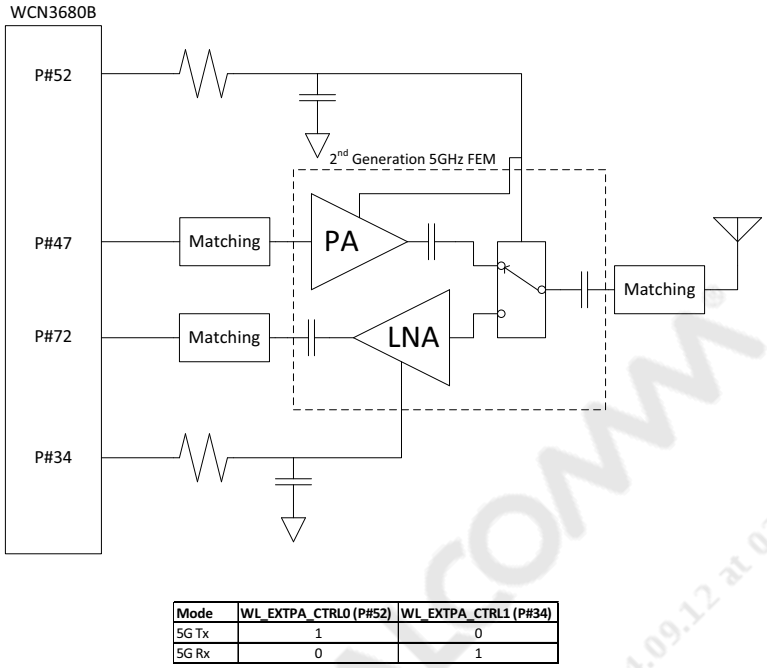


Mode	WL_EXTPA_CTRL_0	WL_EXTPA_CTRL_1	WL_EXTPA_CTRL_2	WL_EXTPA_CTRL_3	WL_EXTPA_CTRL_4
Off	Low	Low	Low	Low	Low
TX2G	Low	Low	Low	High	Low
RX2G	Low	Low	Low	Low	High
BT	Low	Low	High	Low	Low
TX5G	High	Low	Low	Low	Low
RX5G	Low	High	Low	Low	Low
TX5G+BT	High	Low	High	Low	Low
RX5G+BT	Low	High	High	Low	Low

Figure 3-6 RF switch control for dual-band external FEMs



Mode	WL_EXTPA_CTRL0 (P#52)	WL_EXTPA_CTRL1 (P#34)
5G Tx	1	0
5G Rx	0	1

Figure 3-7 RF switch control for 2nd generation 5 GHz-only external FEM

Table 3-16 5 GHz RF Tx performance – external PA driver

Specification	Comments	Tx EVM	Units
DA chain EVM channel BW = 20 MHz	-21 dBm ≤ P_{DA} ≤ -10 dBm	-36.00	dB
DA chain EVM channel BW = 40 MHz	-21 dBm ≤ P_{DA} ≤ -10 dBm	-34.50	dB
DA chain EVM channel BW = 80 MHz	-21 dBm ≤ P_{DA} ≤ -10 dBm	-34.00	dB

Table 3-17 2 GHz RF Tx performance – external PA driver

Specification	Comments	Tx EVM	Units
This information will be provided in a future revision			

3.9.4 WLAN 5 GHz RF Rx

The WCN3680B/WCN3660B device WLAN RF receiver is specified for the WLAN 802.11n standard.

Table 3-18 5 GHz/20 MHz RF performance – Rx sensitivity

Parameter	Condition	Min	Typ	Max	Units
RF input frequency range		4.9	–	5.85	GHz
11a (6 Mbps)	At WCN3680B/WCN3660B WL_BT_RFIO_5G port	–	-90.6	–	dBm
11a (54 Mbps)	At WCN3680B/WCN3660B WL_BT_RFIO_5G port	–	-75.6	–	dBm
11n, HT20 (MCS0)	At WCN3680B/WCN3660B WL_BT_RFIO_5G port	–	-89.6	–	dBm
11n, HT20 (MCS7)	At WCN3680B/WCN3660B WL_BT_RFIO_5G port	–	-74.0	–	dBm
11n, HT40 (MCS0)	At WCN3680B/WCN3660B WL_BT_RFIO_5G port	–	-87.6	–	dBm
11n, HT40 (MCS7)	At WCN3680B/WCN3660B WL_BT_RFIO_5G port	–	-71.0	–	dBm
11ac, VHT20 (MCS0)	At WCN3680B WL_BT_RFIO_5G port	–	-89.6	–	dBm
11ac, VHT20 (MCS7)	At WCN3680B WL_BT_RFIO_5G port	–	-74.0	–	dBm
11ac, VHT20 (MCS8)	At WCN3680B WL_BT_RFIO_5G port	–	-68.6	–	dBm
11ac, VHT40 (MCS0)	At WCN3680B WL_BT_RFIO_5G port	–	-87.6	–	dBm
11ac, VHT40 (MCS7)	At WCN3680B WL_BT_RFIO_5G port	–	-71.0	–	dBm
11ac, VHT40 (MCS8)	At WCN3680B WL_BT_RFIO_5G port	–	-64.6	–	dBm
11ac, VHT40 (MCS9)	At WCN3680B WL_BT_RFIO_5G port	–	-63.6	–	dBm
11ac, VHT80 (MCS0)	At WCN3680B WL_BT_RFIO_5G port	–	-85.6	–	dBm
11ac, VHT80 (MCS7)	At WCN3680B WL_BT_RFIO_5G port	–	-66.1	–	dBm
11ac, VHT80 (MCS8)	At WCN3680B WL_BT_RFIO_5G port	–	-60.6	–	dBm
11ac, VHT80 (MCS9)	At WCN3680B WL_BT_RFIO_5G port	–	-59.6	–	dBm

3.9.5 WLAN analog interface between host and WCN3680B/WCN3660B

The analog interface signals between the WLAN digital baseband of the wireless connectivity subsystem (WCS) in the host and WCN3680 devices are listed in Table 3-19. The I/Q baseband analog interface consists of four transmission lines shared between the Tx and Rx paths. In Tx mode these four lines are used to connect DAC output pins to Tx BBF input pins; the ADC input pins and Rx BBF output pins are in high-Z mode. For Rx mode, conversely, the four lines are used to connect the Rx BBF output pins to ADC input pins as the DAC outputs and Tx BBF inputs are in high-Z mode.

Table 3-19 Analog interface signals

Signal name	Direction (with respect to RF)	Description
WL_BB_IN	Analog I/O	Baseband analog I negative, multiplexed between TX_IN and RX_IN on the RF side. See Table 3-20.
WL_BB_IP	Analog I/O	Baseband analog I positive, multiplexed between TX_IP and RX_IP on the RF side. See Table 3-20.
WL_BB_QN	Analog I/O	Baseband analog Q negative, multiplexed between TX_QN and RX_QN on the RF side. See Table 3-20.
WL_BB_QP	Analog I/O	Baseband analog Q positive, multiplexed between TX_QP and RX_QP on the RF side. See Table 3-20.

The electrical specifications of the interface signals can be found in Table 3-20.

Table 3-20 Analog I/Q interface specifications

Specification	Comments	Min	Typ	Max	Units
Tx mode operation					
Tx I or Q input impedance for normal operation mode, single-ended	DC to 45 MHz	–	15 Ω || 1 pF	–	Ω
Tx I or Q input impedance for high-Z mode, single-ended	DC to 45 MHz	–	>1 M Ω || < 2 pF	–	Ω
Maximum interconnect capacitance I or Q, single-ended [1]	External parasitic capacitance on I or Q inputs due to board routing, connector, etc.	–	–	7	pF
Amplitude droop in normal operation mode	At 45 MHz, due to Tx I or Q input impedance parasitic capacitance	–	–	0.1	dB
Mean I/Q phase imbalance	Measured up to 45 MHz	-0.2	–	0.2	Degree
Mean I/Q amplitude imbalance	Measured up to 45 MHz	-0.5	–	0.5	%
Tx mode, AC current positive or negative inputs (I or Q)		–	250	–	µApp
Tx mode, common mode voltage on either positive or negative input (I or Q)		–	0.3	–	V
Rx mode operation					
Single-ended output impedance for normal operation (I or Q)	DC to 45 MHz	–	80	–	Ω
Single-ended output impedance for high-Z mode (I or Q)	DC to 45 MHz	–	>1 M Ω || < 2 pF	–	Ω
Rx I/Q output voltage range		0	–	1.6	V_{pp}
Amplitude droop in normal operation mode	At 45 MHz, due to Rx I or Q output impedance parasitic capacitance	–	–	0.1	dB

Table 3-20 Analog I/Q interface specifications (cont.)

Specification	Comments	Min	Typ	Max	Units
Mean I/Q phase imbalance	Measured up to 45 MHz	-0.2	–	0.2	Degree
Mean I/Q amplitude imbalance	Measured up to 45 MHz	-0.5	–	0.5	%
Common mode voltage on either positive or negative output (I or Q)		–	0.55	–	V
Rx drive capability Normal mode (driving internal ADC), single-ended		300 Ω || 8 pF			
Rx drive capability, resistive Test mode (driving external pin)	0 to 45 MHz	10	–	–	kΩ
Rx drive capability, capacitive Test mode (driving external pin)	0 to 40 MHz	–	–	1	pF
Maximum DC offset after calibration	Measured at BB IQ interface	-60	–	60	mV

1. 50 Ω strip transmission lines should be used for I/Q baseband analog interface signals.

3.9.6 WLAN Tx power detector

The WCN3680B/WCN3660B IC includes an integrated detector for monitoring WLAN transmissions near the high end of its dynamic range, thereby ensuring that the maximum level is achieved for each channel and data-rate configuration without exceeding spurious emission and EVM requirements. Three different operation scenarios are supported by the Tx power detector:

- Measurements based on the internal PA output
- Measurements based on the external PA output
- Bypass when using an external power detector – the external detector's output is connected to the WLAN_PDET_IN pin, which is multiplexed with the internal power detector's output to the power detect ADC input

Table 3-21 WLAN Tx power-detector performance specifications

Parameter	Comments	Min	Typ	Max	Units
Frequency range		2.400	–	5.850	GHz
Input RF power detector	Using external coupler only, no external power detect circuit.	-6	–	4.0	dBm
Input DC power detect voltage range	Using external coupler and external power detect	0.2	–	1.0	V
Output accuracy	Within 10 dB of the top segment of the dynamic range	-0.15 -0.25	– –	0.15 0.25	dB dB
Output PDADC	Range of input RF power mapped to 8 bits	3	–	124	ADC counts

Table 3-21 WLAN Tx power-detector performance specifications (cont.)

Parameter	Comments	Min	Typ	Max	Units
Output resolution	For every change in 1 dB in 10 dB of the top segment	10	–	–	ADC counts
Output response time [1]		–	4	–	µs
DC/RF turn-on time		–	–	2	µs
ADC common mode voltage		–	0.6	–	Bits

1. The signal subject to measurement is deterministic (always the same 4 µs segment within the WLAN preamble), so the expected response after 4 µs can be calibrated.

Additional comments pertaining to the WLAN Tx power detector:

- The output response is calibrated, so it does not need to be linear in dB or voltage.
- The DC offset error is compensated by software.
- The turn-on and turn-off times are programmable.

3.10 BT radio

3.10.1 BT RF Tx

BT RF transmitter specifications are listed according to three operating modes: the basic rate (Table 3-22), the enhanced data rate (Table 3-23), and low-energy mode (Table 3-24). All typical performance specifications, unless noted otherwise, are based on operation at room temperature (+25°C) using default parameter settings and nominal supply voltages.

Table 3-22 BT Tx performance specifications: basic rate, class [123]

Parameter	Comments	Min	Typ	Max	Units
RF frequency range [4]		2402	–	2480	MHz
RF output power (GFSK)	Maximum power setting	10.5	13[3]	15.5	dBm
Transmit power-control range [5]	Over multiple steps	30	–	–	dB
Transmit power-control step size [5]	Power change, each control step	2	–	8	dB
20 dB bandwidth	GFSK only	–	–	1	MHz
Adjacent channel power	At 1 MHz BW				
±2 channels		–	–	-20	dBm
±3 or more channels		–	–	-40	dBm
Frequency deviations:					
Normal ($\Delta f1_{avg}$)		140	–	175	kHz
Packets exceeding 115 kHz ($\Delta f2_{max}$)		99.9	–	–	%
Frequency tolerance [6]		-75	–	+75	kHz

Table 3-22 BT Tx performance specifications: basic rate, class [1][2][3]

Parameter	Comments	Min	Typ	Max	Units
Carrier frequency drift					
Maximum drift rate within 50 µs		-20	–	+20	kHz
Maximum length 1-slot packet		-25	–	+25	kHz
Maximum length 3-slot packet		-40	–	+40	kHz
Maximum length 5-slot packet		-40	–	+40	kHz
Tx noise power in mobile phone bands [5]	Measured without bandpass filter				
869 to 960 MHz	CDMA, GSM	–	-124	–	dBm/Hz
1570 to 1580 MHz	GPS	–	-143	–	dBm/Hz
1805 to 1910 MHz	GSM	–	-135	–	dBm/Hz
1930 to 1990 MHz	CDMA, WCDMA, GSM	–	-135	–	dBm/Hz
2010 to 2170 MHz	CDMA, WCDMA	–	-130	–	dBm/Hz

1. User measurement results could be affected by measurement uncertainty, as specified in the Bluetooth TSS, Section 6.10.
2. WCN3660B and WCN3680B also support ANT features since ANT shares the same radio as BT BR. Compliance to Bluetooth basic rate specifications ensure ANT compliance as well.
3. For ANT applications, RF output power is 4 dBm typical.
4. Center frequency f = 2402 + k, where k is the channel number (all values in MHz).
5. This specification is required at room temperature (+25°C) and nominal supply voltages only.
6. Initial carrier frequency deviation from Tx center frequency before any packet information is transmitted.

Table 3-23 BT Tx performance specifications: enhanced data rate [1]

Parameter	Comments	Min	Typ	Max	Units
RF frequency range [2]		2402	–	2480	MHz
RF output power [3]					
π/4-DQPSK		–	11	–	dBm
8DPSK		–	11	–	dBm
EDR power-control step size [3]	Power change, each control step	2	–	8	dB
DEVM for π/4-DQPSK					
> 99% of measured blocks		–	–	30	%
RMS for any measured block		–	–	20	%
Peak		–	–	35	%
DEVM for 8DPSK					
> 99% of measured blocks		–	–	20	%
RMS for any measured block		–	–	13	%
Peak		–	–	25	%
In-band spurious emissions					
±1 MHz offset from center		–	–	-26	dBc
±2 MHz offset from center		–	–	-20	dBm
≥ ±3 MHz offset from center		–	–	-40	dBm

Table 3-23 BT Tx performance specifications: enhanced data rate [1] (cont.)

Parameter	Comments	Min	Typ	Max	Units
Frequency errors					
Packet error (ω_i)	Initial error, all packets	-75	–	+75	kHz
Block error (ω_o)	Error for RMS DEVM, all blocks	-10	–	+10	kHz
Total error ($\omega_i + \omega_o$)	Total, all blocks	-75	–	+75	kHz
Tx noise power in mobile phone bands [4]	Measured without bandpass filter				
869 to 960 MHz	CDMA, GSM	–	-124	–	dBm/Hz
1570 to 1580 MHz	GPS	–	-143	–	dBm/Hz
1805 to 1910 MHz	GSM, DCS	–	-135	–	dBm/Hz
1930 to 1990 MHz	GSM, PCS, CDMA, WCDMA	–	-135	–	dBm/Hz
2010 to 2170 MHz	WCDMA	–	-130	–	dBm/Hz

1. User measurement results could be affected by measurement uncertainty, as specified in the Bluetooth TSS, Section 6.10.
2. Center frequency f = 2402 + k, where k is the channel number (all values in MHz).
3. EDR power measured in the GFSK header.
4. This specification is required at room temperature (+25°C) and nominal supply voltages only.

Table 3-24 BT Tx performance specifications: low-energy mode

Parameter	Comments	Min	Typ	Max	Units
RF frequency range [1]		2402	–	2480	MHz
Average output power (P_{AVG}) [2]	Maximum output power setting	–	4	–	dBm
In-band emissions					
f_{TX} ± 1 MHz		–	–	-26	dBc
f_{TX} ± 2 MHz		–	–	-20	dBm
f_{TX} ± (3 + n) MHz		–	–	-30	dBm
Modulation characteristics	Recorded over 10 test packets				
$\Delta f1_{avg}$		225	–	275	kHz
$\Delta f2_{max} \geq 185$ kHz		99.9	–	–	%
$\Delta f1_{avg}/\Delta f1_{avg}$		0.8	–	–	–
Carrier frequency offset and drift	f_{TX} is the nominal Tx frequency				
$f_n - f_{TX}$, n = 0, 1, 2, 3...k		-150	–	+150	kHz
$\lvert f_0 - f_n \rvert$, n = 2, 3, 4...k		–	–	50	kHz
$\lvert f_1 - f_0 \rvert$		–	–	20	kHz
$\lvert f_n - f_{n-5} \rvert$, n = 6, 7, 8...k		–	–	20	kHz

1. Center frequency f = 2402 + k, where k is the channel number (all values in MHz).
2. May set to any equivalent BR power level.

3.10.2 BT RF Rx

BT RF receiver specifications are listed according to three operating modes: the basic rate (Table 3-25), the enhanced data rate (Table 3-26), and low-energy mode (Table 3-27). All typical performance specifications, unless noted otherwise, are based on operation at room temperature (+25°C) using default parameter settings and nominal supply voltages.

Table 3-25 BT Rx performance specifications: basic rate [1]

Parameter	Comments	Min	Typ	Max	Units
RF frequency range [2]		2402	–	2480	MHz
Sensitivity	BER ≤ 0.1%	–	-95	-91	dBm
Maximum usable input [3]	BER ≤ 0.1%	0	–	–	dBm
Carrier-to-interference ratios (C/I) [3]	BER ≤ 0.1%				
Co-channel		–	–	11	dB
Adjacent channel (±1 MHz)		–	–	0	dB
Second adjacent channel (±2 MHz)		–	–	-30	dB
Third adjacent channel (±3 MHz)		–	–	-40	dB
Intermodulation [3, 4, 5]		-39	–	–	dBm

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Table 3-25 BT Rx performance specifications: basic rate [1] (cont.)

Parameter	Comments	Min	Typ	Max	Units
Out-of-band blocking [3, 6]	Measured without bandpass filter				
■ BT					
□ 30 to 2000 MHz		-10	–	–	dBm
□ 2000 to 2400 MHz		-27	–	–	dBm
□ 2500 to 3000 MHz		-27	–	–	dBm
□ 3000 to 12750 MHz		-10	–	–	dBm
■ Cellular blocking					
■ CDMA2000™		-7	–	–	dBm
□ 410 to 420 MHz		-7	–	–	dBm
□ 450 to 460 MHz		-7	–	–	dBm
□ 479 to 484 MHz		-7	–	–	dBm
□ 777 to 792 MHz		-7	–	–	dBm
□ 806 to 849 MHz		-7	–	–	dBm
□ 872 to 925 MHz		-7	–	–	dBm
□ 1710 to 1785 MHz		-7	–	–	dBm
□ 1850 to 1910 MHz		-7	–	–	dBm
□ 1920 to 1980 MHz		-7	–	–	dBm
■ GSM					
□ 450 to 460 MHz		-1	–	–	dBm
□ 479 to 484 MHz		-1	–	–	dBm
□ 777 to 792 MHz		-1	–	–	dBm
□ 824 to 849 MHz		-1	–	–	dBm
□ 876 to 915 MHz		-1	–	–	dBm
□ 1710 to 1785 MHz		-1	–	–	dBm
□ 1850 to 1910 MHz		-1	–	–	dBm
■ WCDMA					
1710 to 1785 MHz		-2	–	–	dBm
1850 to 1910 MHz		-2	–	–	dBm
1920 to 1980 MHz		-2	–	–	dBm

1. User measurement results could be affected by measurement uncertainty, as specified in the Bluetooth TSS, Section 6.10.
2. Center frequency f = 2402 + k, where k is the channel number (all values in MHz).
3. This specification is required at room temperature (+25°C) and normal supply voltages only.
4. Maximum interferer level to maintain 0.1% BER; interference signals at 3 MHz and 6 MHz offsets.
5. Intermodulation performance specification is valid with minimum BPF insertion loss of 1.5 dB.
6. Continuous power in mobile phone bands, -67 dBm desired signal input level. The stated typical values in mobile phone bands are average values measured in accordance with Bluetooth TSS, with less than 24 exceptions.

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Table 3-26 BT Rx performance specifications: enhanced data rate [1]

Parameter	Comments	Min	Typ	Max	Units
RF frequency range [2]		2402	–	2480	MHz
Sensitivity	BER ≤ 0.01%				
π/4-DQPSK		–	-95	-91	dBm
8DPSK		–	-86	-84	dBm
Maximum usable input [3]	BER ≤ 0.1%				
π/4-DQPSK		-15	–	–	dBm
8DPSK		-15	–	–	dBm
Carrier-to-interference ratios (C/I) [3]	Selectivity, BER ≤ 0.1%				
Co-channel					
π/4-DQPSK		–	–	13	dB
8DPSK		–	–	21	dB
Adjacent channel (±1 MHz)					
π/4-DQPSK		–	–	0	dB
8DPSK		–	–	5	dB
Second adjacent channel (±2 MHz)					
π/4-DQPSK		–	–	-30	dB
8DPSK		–	–	-25	dB
Third adjacent channel (±3 MHz)					
π/4-DQPSK		–	–	-40	dB
8DPSK		–	–	-33	dB

1. User measurement results could be affected by measurement uncertainty, as specified in the Bluetooth TSS, Section 6.10.
2. Center frequency f = 2402 + k, where k is the channel number (all values in MHz).
3. This specification is required at room temperature (+25°C) and normal supply voltages only.

Table 3-27 BT Rx performance specifications: low-energy mode

Parameter	Comments	Min	Typ	Max	Units
RF frequency range [1]		2402	–	2480	MHz
Sensitivity		–	-98	–	dBm
Carrier-to-interference ratios (C/I)					
Co-channel		–	–	20	dB
Adjacent channel (±1 MHz)		–	–	15	dB
Second adjacent channel (±2 MHz)		–	–	-17	dB
Third adjacent channel (±3 MHz)		–	–	-27	dB
Out-of-band blocking					
30 to 2000 MHz		-10	–	–	dBm
2003 to 2399 MHz		-27	–	–	dBm
2484 to 2997 MHz		-27	–	–	dBm
3000 MHz to 12.75 GHz		-10	–	–	dBm
Intermodulation		-50	–	–	dBm
Maximum input signal level		0	–	–	dBm
PER report integrity		50	–	–	%

1. Center frequency f = 2402 + k, where k is the channel number (all values in MHz).

3.11 FM performance specifications

The WCN3680B/WCN3660B FM performance specifications are defined in this section.

3.11.1 FM analog and RF performance specifications

The following sections provide performance specifications for the FM RF receiver and analog audio over the full operating power supply voltage range and temperature range shown in Table 3-2.

3.11.1.1 FM radio receiver

Table 3-28 FM radio (with RDS) Rx performance specifications [1]

Parameter	Comments	Min	Typ	Max	Unit
RF-specific					
Input frequency range		76	–	108	MHz
Channel frequency step		–	50 100 200	–	kHz
RF input impedance FM_HS_RX	At 92.5 MHz input frequency	–	150/10	–	Ω/pF
Sensitivity	Modulated with 1 kHz audio tone 22.5 kHz frequency deviation with 75 µs de-emphasis on Tester audio bandwidth: 300 Hz–15 kHz (A-weighted) 26 dB signal-to-noise ratio	–	-3	–	dBµV
RDS sensitivity	2 kHz RDS frequency deviation 95% of blocks decoded with no error Over 5000 blocks	–	15	–	dBµV
Receiver small signal selectivity ±200 kHz interference ±400 kHz interference	3.5 µV EMF wanted RF input signal level Modulated with 1 kHz audio tone 22.5 kHz frequency deviation Tester audio bandwidth: 300 Hz–15 kHz (A-weighted) 26 dB signal-to-noise ratio	 35 60	 50 63	 – –	 dB dB
In-band spurious rejection	1 mV wanted RF signal input level Modulated with 1 kHz audio tone 22.5 kHz frequency deviation Tester audio bandwidth: 300 Hz–15 kHz (A-weighted) 26 dB signal-to-noise ratio	35	–	–	dB
Input third-order intercept point (IP3)		-18	–	–	dBm

Table 3-28 FM radio (with RDS) Rx performance specifications [1] (cont.)

Parameter	Comments	Min	Typ	Max	Unit
Maximum RF input level	Maximum on-channel input level 76-108 MHz. Δf = 75 kHz, L = R, fmod = 1 kHz, pre/de-emphasis = 75 µs Note: THD ≤ 0.6% for mono and 1% for stereo at maximum RF input at room temperature.	118	–	–	dBµV
Seek/tune time	To within ±5 kHz of final frequency	–	–	9	ms
Audio-specific					
De-emphasis time constant		– –	50 75	– –	µs µs
Audio (S + N)/N Mono	Modulated with 1 kHz audio tone 1 mV RF input signal level 22.5 kHz frequency deviation with 75 µs de-emphasis on Tester audio bandwidth: 300 Hz–15 kHz (A-weighted)	57	65	–	dB
Audio (S + N)/N Stereo	Modulated with 1 kHz audio tone 1 mV RF input signal level, 75 kHz frequency deviation with 75 µs de-emphasis on. Tester audio bandwidth: 300 Hz–15 kHz (A-weighted)	53	58	–	dB
Audio THD Mono, 1 kHz, 75 kHz dev Mono, 1 kHz, 100 kHz dev Stereo, 3 kHz, 75 kHz dev	Modulated with 1 kHz audio tone 1 mV RF input signal level with 75 µs de-emphasis on Tester audio bandwidth: 300 Hz – 15 kHz (A-weighted)	 – – –	 0.4 0.5 0.9	 0.8 1 1.5	 % % %
Audio frequency response low	Mono -3 dB point 0 dB at 1 kHz 1 mV RF input signal level 22.5 kHz frequency deviation with 75 µs pre-emphasis on	–	–	20	Hz
Audio frequency response high	Mono -3 dB point 0 dB at 1 kHz 1 mV RF input signal level 22.5 kHz frequency deviation with 75 µs pre-emphasis on	15	–	–	kHz
Audio output mute attenuation Left Right Left and right	Modulated with 1 kHz audio tone 1 mV RF input signal level 22.5 kHz frequency deviation with 75 µs de-emphasis on Tester audio bandwidth: 300 Hz–15 kHz (A-weighted)	 80 80 80	 – – –	 – – –	 dB dB dB
Soft mute start level	3 dB mute attenuation	3	8	10	µV EMF

Table 3-28 FM radio (with RDS) Rx performance specifications [1] (cont.)

Parameter	Comments	Min	Typ	Max	Unit
Soft mute attenuation at 1.4 µV EMF RF input signal level	Modulated with 1 kHz audio tone 22.5 kHz frequency deviation with 75 µs de-emphasis on Tester audio bandwidth: 300 Hz–15 kHz (A-weighted)	10	39	30	dB
AM suppression	Modulated with 1 kHz audio tone >20 µV EMF RF input signal level 22.5 kHz frequency deviation with 75 µs de-emphasis on Tester audio bandwidth: 300 Hz–15 kHz (A-weighted) 30% AM modulation index	40	57	–	dB
Stereo channel separation SNC on	Modulated with 1 kHz audio tone 75 kHz frequency deviation 40 µV RF input signal level	4	10	16	dB
Stereo channel separation SNC off	Modulated with 1 kHz audio tone 75 kHz frequency deviation 30 µV RF input signal level	30	40	–	dB
Mono/stereo blend start voltage	1 dB stereo channel separation; SNC on	–	28	–	µV EMF
Mono/stereo switching hysteresis	SNC off; 1 kHz mod; 75 kHz dev; 9% pilot; R = 0, L = 1	–	3	–	dB

1. All RF input voltages are potentially different across input, unless EMF is explicitly stated.

Table 3-29 FM receiver selectivity [1, 2, 3, 4, 5, 6]

Category	Modulation type	Test frequencies (MHz)		Typical blocker input power (dBm)
		FM channel	WAN blocker	
NA 700L	CDMA	99.9	698.5	-52
NA 700L	CDMA	102.5	716.7	-52
NA 700L	WCDMA	99.9	698.5	-47
NA 700L	WCDMA	102.5	716.7	-47
NA 700H	CDMA	87.5	786.7	-52
NA 700H	CDMA	88.3	793.9	-52
NA 700H	WCDMA	87.5	786.7	-47
NA 700H	WCDMA	88.3	793.9	-47
US cellular	GSM	91.7	824.5	-45
US cellular	GSM	94.5	849.7	-45
US cellular	CDMA	91.7	824.5	-42
US cellular	CDMA	94.5	849.7	-42
US cellular	WCDMA	91.7	824.5	-37
US cellular	WCDMA	94.5	849.7	-37
GSM 900	GSM	97.9	880.3	-45

Table 3-29 FM receiver selectivity [1, 2, 3, 4, 5, 6] (cont.)

Category	Modulation type	Test frequencies (MHz)		Typical blocker input power (dBm)
		FM channel	WAN blocker	
GSM 900	GSM	101.7	914.5	-45
CDMA 900	CDMA	97.9	880.3	-42
CDMA 900	CDMA	101.7	914.5	-42
WCDMA 900	WCDMA	97.9	880.3	-37
WCDMA 900	WCDMA	101.7	914.5	-37
UMTS 1500	WCDMA	84.1	1428.1	-37
UMTS 1500	WCDMA	85.5	1451.9	-37
GSM 1800	GSM	100.7	1710.3	-45
GSM 1800	GSM	105.1	1785.1	-45
PCS	GSM	97.5	1850.5	-45
PCS	GSM	100.7	1911.3	-45
PCS	CDMA	97.5	1850.5	-42
PCS	CDMA	100.7	1911.3	-42
PCS	WCDMA	97.5	1850.5	-37
PCS	WCDMA	100.7	1911.3	-37
IMT	CDMA	101.3	1922.7	-42
IMT	CDMA	104.3	1979.7	-42
IMT	WCDMA	101.3	1922.7	-37
IMT	WCDMA	104.3	1979.7	-37
BT/WLAN	BT	104.5	2401.1	-43
BT/WLAN	BT	107.9	2479.3	-43
UMTS 2600	WCDMA	100.1	2500.1	-41
UMTS 2600	WCDMA	102.9	2570.1	-41

1. All levels are at chip input.
2. Wanted signal at 5 dBμV (-102 dBm 50 Ω or +10.8 dBμV EMF) input; f_{mod} = 1 kHz, Δf = 22.5 kHz SINAD = 26 dB, BAF = 300 Hz to 15 kHz (A-weighted) de-emphasis = 50 μs.
3. CDMA blocker is modulated reverse link. 1.2288 Mb/s chip rate.
4. WCDMA blocker is modulated reverse link. 3.84 Mb/s chip rate.
5. GSM blocker is modulated; MSK modulation; Gaussian filter BT = 0.3; fs = 270.8333 ks/s; and bursting 1/8 timeslots.
6. BT blocker is modulated with mod index = 0.315; bursting with DH1 packets.

3.11.2 FM RDS interrupt

At reset, the RDS interrupt signal is disabled. After reset, the host may enable the interrupt and set the NVM parameters associated with the interface. The software supports the following NVM parameters for configuring the interrupt behavior:

- Inactive mode: tri-state or output
- Internal pull (if inactive mode is set to tri-state): up, down, or no-pull

The FM RDS interrupt uses a digital I/O pin that receives power from the VDD_IO_1P8 supply. Its I/O performance specifications meet the requirements stated in Section 3.5.

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4 Mechanical Information

Mechanical information for the WCN3680B/WCN3660B IC is presented in this chapter, including physical dimensions, visible markings, ordering information, moisture sensitivity level, and thermal characteristics. Additional details pertaining to these topics are included in the *Wafer-Level Package User Guide* (80-VJ241-3), which is available for download at https://support.cdmatech.com (the CDMATech Support Website).

4.1 Device physical dimensions

The WCN3680B/WCN3660B IC is available in the 79B WLNSP that includes extra ground pins for improved grounding, mechanical strength, and thermal continuity. The 79B WLNSP package has a 3.805 × 3.82 mm body with a maximum height of 0.63 mm. Pin 1 is located by an indicator mark on the top of the package. The 79B WLNSP outline drawing is shown in Figure 4-1.

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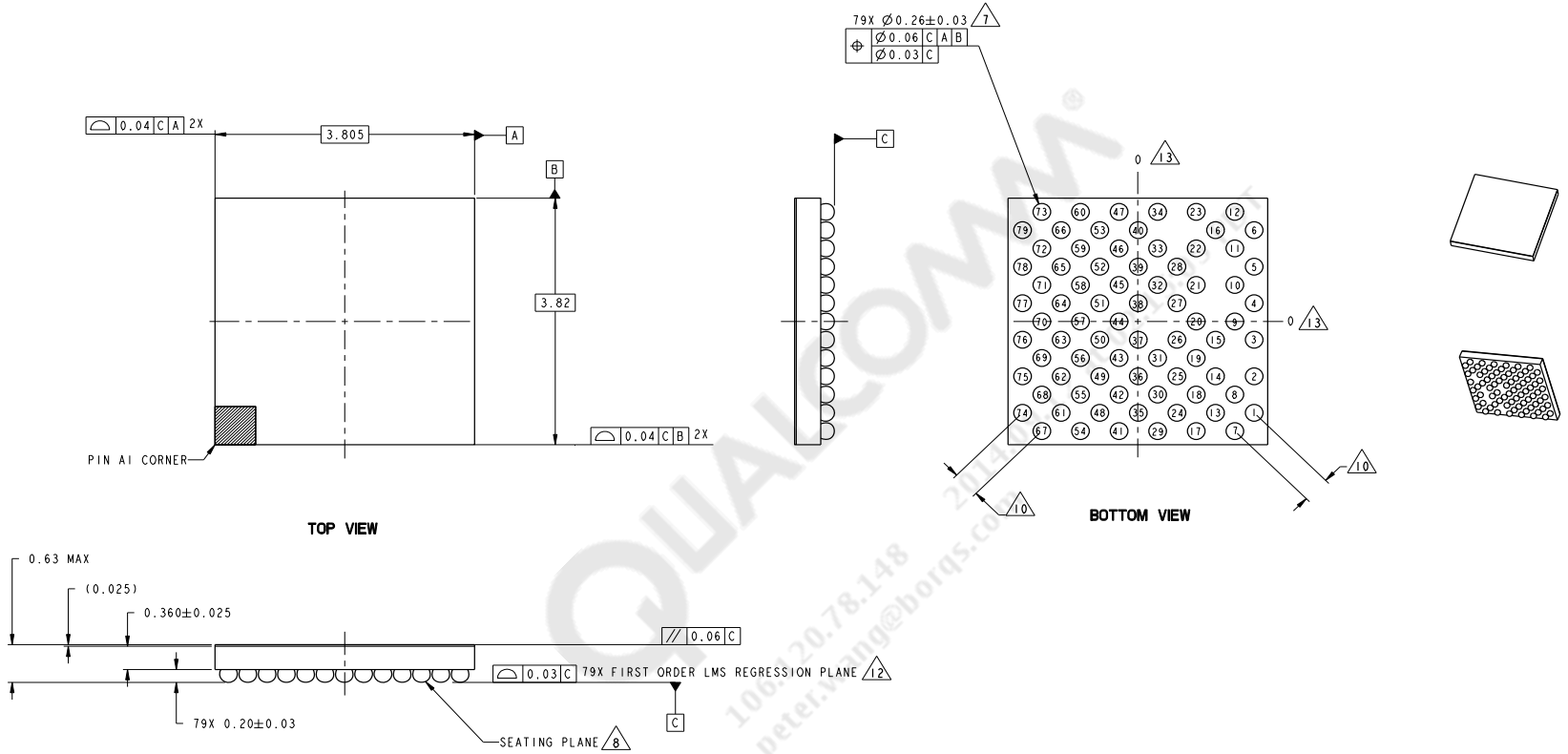

13 BALL COORDINATES ON PAGE 52 LOCATED FROM PACKAGE CENTER (0,0).

12 PRIMARY DATUM -C- IS DETERMINED BY THE FIRST ORDER LMS REGRESSION PLANE THROUGH THE SPHERICAL CROWNS OF ALL SOLDER BALLS ON THIS SIDE OF PACKAGE.

11. WLP PACKAGE SIZE = DESIGN DIE SIZE + 40UM KERF WIDTH.

10 MINIMUM BALL PITCH IS 0.400 MM.

9. THE SURFACE FINISH OF THE PACKAGE SHALL BE EDM CHARLILLE #24-#27.

8 THE SEATING PLANE IS DEFINED BY THREE NON-COLINEAR BALLS THAT SUPPORT THE FREE STANDING PACKAGE WHEN IT IS PLACED ON A FLAT SURFACE. THE VECTORS FORMED BY THE THREE BALLS SHALL ENCOMPASS THE CENTER OF GRAVITY WHEN IT IS PROJECTED ONTO THE SEATING PLANE.

7 DIMENSION MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO THE PRIMARY DATUM -C-.

5. QUALCOMM SUPPLIED ELECTRONIC DATABASE(S) ARE FOR REFERENCE ONLY. DIMENSIONAL INFORMATION ON CURRENT REVISION OF RELEASED DRAWING TAKES PRECEDENCE OVER ELECTRONIC DATABASE(S).

3. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-2009.

2. ALL DIMENSIONS SHOWN ON THIS DRAWING ARE IN MILLIMETERS (MM) .

1. INTERPRET DRAWING PER ASME Y14.100.

NOTES: UNLESS OTHERWISE SPECIFIED.

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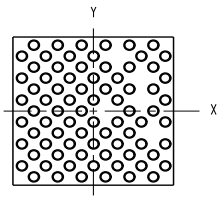
Figure 4-1 79B WLNSP outline drawing



Ball Number	Ball Pad Center (x)	Ball Pad Center (y)		Ball Number	Ball Pad Center (x)	Ball Pad Center (y)
1	1.7055	-1.415		41	-0.2755	-1.698
2	1.7055	-0.849		42	-0.2755	-1.132
3	1.7055	-0.283		43	-0.2755	-0.566
4	1.7055	0.283		44	-0.2755	0
5	1.7055	0.849		45	-0.2755	0.566
6	1.7055	1.415		46	-0.2755	1.132
7	1.4225	-1.698		47	-0.2755	1.698
8	1.4225	-1.132		48	-0.5585	-1.415
9	1.4225	0		49	-0.5585	-0.849
10	1.4225	0.566		50	-0.5585	-0.283
11	1.4225	1.132		51	-0.5585	0.283
12	1.4225	1.698		52	-0.5585	0.849
13	1.1395	-1.415		53	-0.5585	1.415
14	1.1395	-0.849		54	-0.8415	-1.698
15	1.1395	-0.283		55	-0.8415	-1.132
16	1.1395	1.415		56	-0.8415	-0.566
17	0.8565	-1.698		57	-0.8415	0
18	0.8565	-1.132		58	-0.8415	0.566
19	0.8565	-0.566		59	-0.8415	1.132
20	0.8565	0		60	-0.8415	1.698
21	0.8565	0.566		61	-1.1245	-1.415
22	0.8565	1.132		62	-1.1245	-0.849
23	0.8565	1.698		63	-1.1245	-0.283
24	0.5735	-1.415		64	-1.1245	0.283
25	0.5735	-0.849		65	-1.1245	0.849
26	0.5735	-0.283		66	-1.1245	1.415
27	0.5735	0.283		67	-1.4075	-1.698
28	0.5735	0.849		68	-1.4075	-1.132
29	0.2905	-1.698		69	-1.4075	-0.566
30	0.2905	-1.132		70	-1.4075	0
31	0.2905	-0.566		71	-1.4075	0.566
32	0.2905	0.566		72	-1.4075	1.132
33	0.2905	1.132		73	-1.4075	1.698
34	0.2905	1.698		74	-1.6905	-1.415
35	0.0075	-1.415		75	-1.6905	-0.849
36	0.0075	-0.849		76	-1.6905	-0.283
37	0.0075	-0.283		77	-1.6905	0.283
38	0.0075	0.283		78	-1.6905	0.849
39	0.0075	0.849		79	-1.6905	1.415
40	0.0075	1.415				

Figure 4-2 WCN3680B/WCN3660B pin locations

4.2 Device marking

Section 4.2.1 provides the device marking information for WCN3680B; Section 4.2.2 provides the device marking information for WCN3660B.

4.2.1 WCN3680B

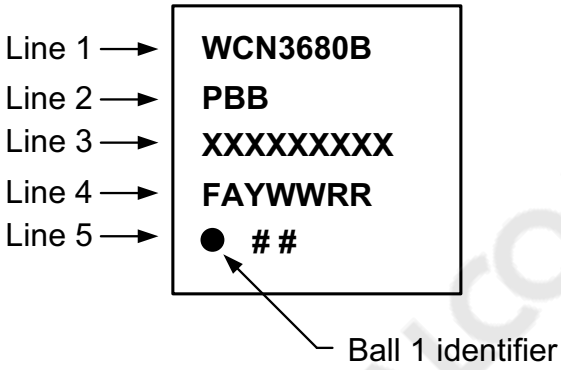


Figure 4-3 WCN3680B part marking (top view – not to scale)

Table 4-1 WCN3680B part marking line descriptions

Line	Marking	Description
1	WCN3680B	QCA product name
2	PBB	P = Configuration code BB = Feature code
3	XXXXXXXXX	XXXXXXXXX = wafer lot number
4	FAYWWRR	F = Source of supply code for wafer fab locations ■ When F = A: □ Fabrication = TSMC A = Source of supply code for assembly location ■ When A = A: □ Assembly = TSMC, BP2B, Taiwan ■ When A = B: □ Assembly = Amkor, ATT3, Taiwan Y = Single-digit year WW = Two-digit work week of current year (based on calendar year) RR = Product revision ■ RR = Engineering sample version □ 05 = Engineering sample 1 (ES1, CS)
5	##	## = Two-digit wafer number

4.2.2 WCN3660B

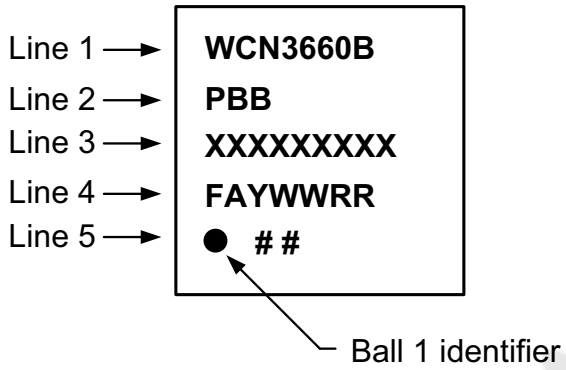


Figure 4-4 WCN3660B part marking (top view – not to scale)

Table 4-2 WCN3660B part marking line descriptions

Line	Marking	Description
1	WCN3660B	QCA product name
2	PBB	P = Configuration code BB = Feature code
3	XXXXXXXXX	XXXXXXXXX = wafer lot number
4	FAYWWRR	F = Source of supply code for wafer fab locations ■ When F = A: □ Fabrication = TSMC A = Source of supply code for assembly location ■ When A = A: □ Assembly = TSMC, BP2B, Taiwan ■ When A = B: □ Assembly = Amkor, ATT3, Taiwan Y = Single-digit year WW = Two-digit work week of current year (based on calendar year) RR = product revision ■ RR = Engineering sample version □ 05 = Engineering sample 1 (ES1, CS)
5	##	## = Two-digit wafer number

4.3 Device ordering information

This device can be ordered using the identification code shown in Figure 4-5.

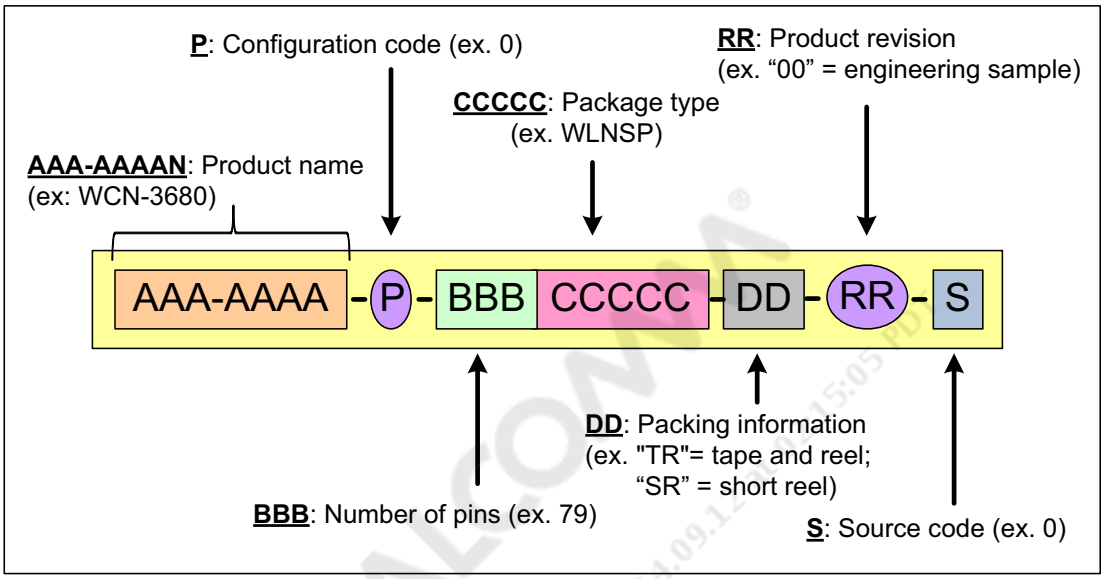


Figure 4-5 Device identification code

An example can be as follows: WCN-3680-0-79WLNSP-TR-00-0.

The P and RR values are more completely defined in Section 4.2.

4.4 Device moisture-sensitivity level

During device qualification, QCA follows the latest revision IPC/JEDEC J-STD-020 standard to determine the IC’s moisture-sensitivity level (MSL). See Chapter 7 for more information.

To ensure proper SMT assembly, procedures must follow the MSL and maximum reflow temperature specified on the shipping bag labels or barcode labels accompanying all WCN3680B/WCN3660B IC shipments.

Additional MSL information is included in:

- Section 5.2 – Storage
- Section 5.3 – Handling
- Section 7.1 – Reliability qualifications summary
- *ASIC Packing Methods and Materials Specification* (80-VK055-1)

4.5 Thermal characteristics

The WCN3680B/WCN3660B device in its 79B WLNSP package has typical thermal resistances as listed in Table 4-3.

Table 4-3 Device thermal resistance

Parameter		Comments	Typ	Unit
θ_{JA}	Thermal resistance, J-to-A	Junction-to-ambient (still air) [1]	49.0	°C/W

1. Junction-to-ambient thermal resistance (θ_{JA}) is calculated based on the total package power dissipation (200 mW); ambient temperature is 85°C.

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5 Carrier, Storage, and Handling Information

Information about shipping, storing, and handling the WCN3680B/WCN3660B IC is presented in this chapter. Additional details are available in the *Wafer-Level Package User Guide* (80-VJ241-3), which can be downloaded from the CDMATech Support Website (https://support.cdmatech.com).

5.1 Shipping

5.1.1 Tape and reel information

The single-feed tape carrier for the WCN3680B/WCN3660B device is illustrated in Figure 5-1; this figure also shows the proper part orientation. The tape width is 12 mm, and the parts are placed on the tape with a 8 mm pitch. The reels are 330 mm (13 inch) in diameter, with 178 mm (7 inch) hubs. Each reel can contain up to 5000 devices.

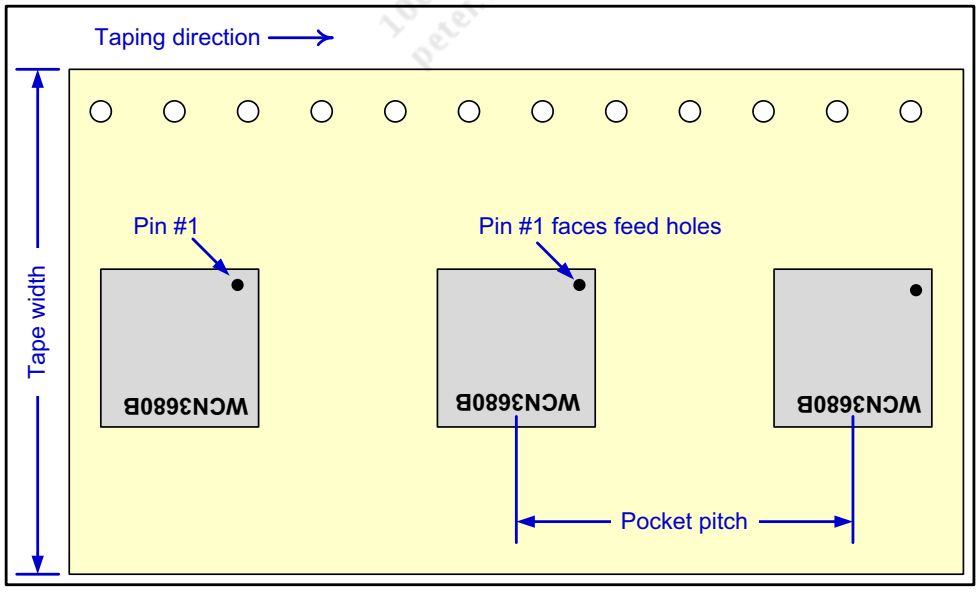

Figure 5-1 Carrier tape drawing with part orientation

The carrier tape and reel features are based on the EIA-481 standard. Individual pocket designs can vary from vendor to vendor, but it is designed to hold the part for shipping and loading onto SMT manufacturing equipment while protecting the body and balls from damaging stresses. The WLNSPs are packaged in tape and reel with their solder balls facing down.

Tape-handling recommendations are shown in Figure 5-2.

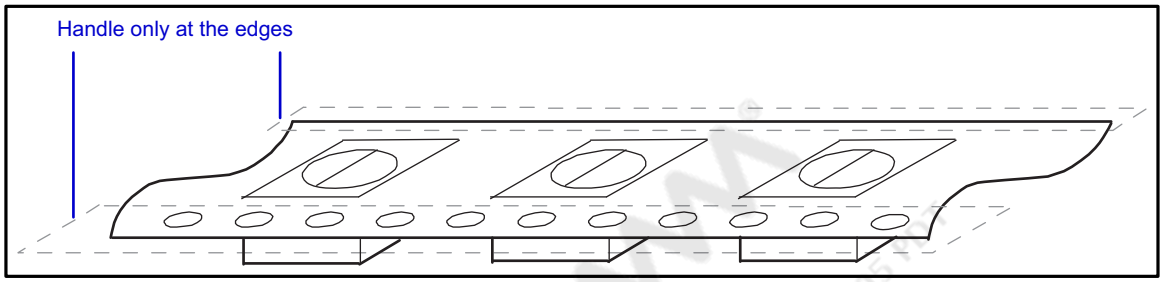

Figure 5-2 Tape handling

5.1.2 Packing for shipment (including barcode label)

Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) document for all packing-related information, including barcode label details.

5.2 Storage

5.2.1 Storage conditions

WCN3680B/WCN3660B devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, anti-static bags. Refer to the *ASIC Packing Methods and Materials Specification* (80-VK055-1) document for details for the expected shelf life.

5.2.2 Out-of-bag duration

WCN3680B/WCN3660B devices may be kept outside the moisture barrier bag on the factory floor indefinitely without detrimental moisture absorption.

5.3 Handling

Unlike traditional IC devices, the silicon in the WCN devices is not protected by an over-mold and there is no substrate; hence, these devices are relatively fragile.

Tape handling was described in Section 5.1.1. Other handling guidelines are presented below.

NOTE To eliminate damage to the silicon die due to improper handling, the following recommendations should be followed:

- Do not use tweezers, as that may cause damage to the silicon die. QCA recommends using a vacuum tip to handle the device.
- Carefully select a pickup tool to avoid any damage during the SMT process.
- Do not make contact with the device when reworking or tuning components that are in close proximity to the device.

For more details on handling, please review the *Wafer Level Package (WLP) Device Handling Guidelines* (80-ND595-1) document.

5.3.1 Baking

Wafer level packages, including this device, should not be baked.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

QCA products must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

Refer to Section 7.1 for the WCN3680B/WCN3660B device ESD ratings.

6 PCB Mounting Guidelines

Guidelines for mounting the WCN3680B/WCN3660B device onto a PCB are presented in this chapter, including land pad and stencil design details, surface mount technology (SMT) process characterization, and SMT process verification.

NOTE For the most accurate and up-to-date mounting details, refer to the latest revision of the *Wafer-Level Package User Guide* (80-VJ241-3), which can be downloaded from the CDMATech Support Website (https://support.cdmatech.com). Mounting suggestions presented in this chapter are provided for convenience only.

The WCN3680B device is Pb-free internally and externally; it is also BrCl-free, RoHS-compliant, and e1(SAC). Its solder balls use the SAC405 composition.

NOTE QCA defines its lead-free (or Pb-free) semiconductor products as having a maximum lead concentration of 1000 ppm (0.1% by weight) in raw (homogeneous) materials and end products. QCA package environmental programs, RoHS compliance details, and tables defining pertinent characteristics of all QCA IC products are described in the *IC Package Environmental Roadmap* (80-V6921-1).

6.1 Land pad and stencil design

The land pattern recommendations are based on QCA internal characterizations using Pb-free solder pastes on an eight-layer test PCB and a 100-micron thick stencil. The PCB land pattern for the 79B WLNSP package is the same whether SnPb or Pb-free solder is used.

NOTE Click the link below to download the 79B WLNSP land/stencil drawing (LS90-N2742-1) from the CDMATech Support Website.

- https://downloads.cdmatech.com/qdc/drl/objectId/09010014814e39ee

Clicking the link above will take you directly to the CDMATech Support Website (https://support.cdmatech.com), prompting a document download for that specific drawing (assuming you have permission to view it).

Subscribing to a drawing

To be notified about changes to a drawing, you can subscribe to it. Click the **Help** button to download the latest revision of *Using CDMATech Support Documents and Downloads User Guide* (80-V7273-1), which includes general subscription instructions.

6.2 Daisy-chain interconnect drawing

Daisy-chain packages use the same processes and materials as actual products. The daisy-chain interconnect drawing shows how packages should be attached to a characterization PCB. All SMT development described in Section 6.3 can be performed using daisy-chain packages. A bias can be applied, and solder-joint resistance can be monitored.

NOTE Click the link below to download the 79B WLNSP daisy-chain interconnect drawing (DS90-N2742-1) from the CDMATech Support Website.

- https://downloads.cdmatech.com/qdc/drl/objectId/09010014814e3c2c

Clicking the link above will take you directly to the CDMATech Support Website (https://support.cdmatech.com), prompting a document download for that specific drawing (assuming you have permission to view it).

Subscribing to a drawing

To be notified about changes to a drawing, you can subscribe to it. Click the **Help** button to download the latest revision of *Using CDMATech Support Documents and Downloads User Guide* (80-V7273-1), which includes general subscription instructions.

6.3 SMT development and characterization

The information presented in this section describes QCA board-level characterization process parameters. It is included to assist customers when starting their SMT process development; it is not intended to be a specification for customer SMT processes.

NOTE QCA recommends that customers follow their solder paste vendor recommendations for the screen-printing process parameters and reflow profile conditions.

QCA characterization tests attempt to optimize the SMT process for the best board-level reliability possible. This is done by performing physical tests on evaluation boards, which may include:

- Bend cycle
- Drop shock
- Temperature cycling

QCA recommends characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile ***prior to PCB production***. Review the land pattern and stencil pattern design recommendations in Section 6.1 as a guide for characterization.

QCA does not endorse any particular underfill products.

Optimizing the solder-stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

Daisy-chain packages are suitable and available for SMT characterization; ordering information is included in the *Wafer-Level Package User Guide* (80-VJ241-3).

Reflow profile conditions typically used by QCA for SnPb and lead-free systems are given in Table 6-1.

Table 6-1 QCA typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Lead-free (high-temperature) condition limits
Preheat	Initial ramp	3°C/sec max
Soak	Dry out and flux activation	150 to 190°C 60 to 120 sec
Reflow	Time above solder-paste melting point	40 to 75 sec
	Peak temperature	250°C
Cool down	Cool rate – ramp to ambient	6°C/sec max

6.4 SMT peak package-body temperature

QCA recommends the following limits during the SMT board-level solder attach process:

- SMT peak package-body temperature of 250 ºC, the temperature that must not be exceeded as measured on the package-body's top surface.
- Maximum duration of 30 sec. at this temperature.

Although the solder-paste manufacturer's recommendations for optimum temperature and duration for solder reflow must be followed, the QCA recommended limits must not be exceeded.

6.5 SMT process verification

QCA recommends verification of the SMT process prior to high-volume PCB fabrication, including:

- Electrical continuity
- X-ray inspection of the package installation for proper alignment, solder voids, solder balls, and solder bridging
- Visual inspection
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume (insufficient, acceptable, or excessive)

7 Part Reliability

7.1 Reliability qualification summary

Table 7-1 WCN3680B/WCN3660B reliability qualification report for a device from TSMC and WLNSP package from TSMC and Amkor

Tests, standards, and conditions	Sample # lots	Results (TSMC)	Results (Amkor)
Average failure rate (AFR) in FIT (λ) failures per billion device-hours Functional HTOL: JESD22-A108	535 3 lots	λ = 15 FIT	N/A
Mean time to failure (MTTF) t = 1/λ (million hours)	535 3 lots	67	N/A
ESD – human body model (HBM) rating JESD22-A114-B	3	Pass ± 2000 V, all pins	N/A
ESD – charged device model (CDM) rating JESD22-C101-D	3	Pass ± 500 V, all pins	N/A
Latch-up (overcurrent test): EIA/JESD78 Trigger current: ±100 mA; temperature: 85°C	6	Pass	N/A
Latch-up (Vsupply overvoltage): EIA/JESD78 Trigger voltage: 1.5 × V; temperature: 85°C	6	Pass	N/A
Moisture resistance test (MRT): MSL 1; J-STD-020 **3 X reflow cycles at 255 +5/-0C**	462 3 lots	Pass	Pass
Temperature cycle: JESD22-A104 Temperature: -55°C to +125°C; number of cycles: 1000 Minimum soak time at min/max temperature: five minutes Cycle rate: two cycles per hour (CPH) **Preconditioning:** JESD22-A113 **MSL: 1 reflow temperature: 255°C+5/-0°C**	231 3 lots	Pass	Pass
Unbiased highly accelerated stress test (UHAST) JESD22-A118 Preconditioning: JESD22-A113 **MSL: 1 reflow temperature: 255 +5/-0°C**	231 3 lots	Pass	Pass
High temperature storage life: JESD22-A103 Temperature 150°C, 1000 hours	78 3 lots	Pass	Pass

Table 7-1 WCN3680B/WCN3660B reliability qualification report for a device from TSMC and WLNSP package from TSMC and Amkor (cont.)

Tests, standards, and conditions	Sample # lots	Results (TSMC)	Results (Amkor)
Physical dimensions: JESD22-B100-A Package outline drawing: NT90-N2742-1	15	Pass	Pass
Solder ball shear; JESD22-B117 After 10x reflow cycles 260°C -5/+0°C	40 balls (four balls per sample × 10 samples)	Pass, all balls sheared in ductile mode	Pass, all balls sheared in ductile mode

7.2 Qualification sample description

WCN3680B device characteristics

Device name: WCN3680B

Package type: 79B WLNSP

Package body size: 3.805 mm × 3.82 mm × 0.63 mm

BGA ball count: 79

BGA ball composition: SAC405

Processes: 65 nm RF CMOS

Fab site: See note.

Assembly sites: See note.

Solder ball pitch: 0.4 mm minimum

NOTE See the *WCN3680B Device Revision Guide* (80-WL007-4) for fab and assembly sites.

WCN3660B device characteristics

Device name: WCN3660B

Package type: 79B WLNSP

Package body size: 3.805 mm × 3.82 mm × 0.63 mm

BGA ball count: 79

BGA ball composition: SAC405

Processes: 65 nm RF CMOS

Fab site: See note.

Assembly sites: See note.

Solder ball pitch: 0.4 mm minimum

NOTE See the *WCN3660B Device Revision Guide* (80-WL302-4) for fab and assembly sites.

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